國立交通大學

材料科學與工程學系

碩士論文

結合高介電質材料與三五族半導體之金氧半電容研究

Study of High-k/III-V MOS Capacitors

研 究 生：宋先敏

指導教授：張　翼　博士

中華民國九十八年八月

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碩士論文

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摘要

互補式金氧半場效電晶體之發展將在到達 22 奈米結點時遇到瓶頸，結合高介電質材料與高電子遷移率三五族半導體的研究逐漸受到重視。由於有著極佳的載子傳導特性，三五族金氧半場效電晶體將會是未來高頻低操作偏壓應用的選擇。然而高介電質材料與三五族半導體的介面問題始終阻礙著三五族金氧半元件的發展。隨著薄膜沉積技術的進步，原子層沉積法以及分子束磊晶技術已經能夠成長高品質的介電材料於三五族半導體上研究金氧半電容的特性。

本論文主要利用分子束磊晶機台成長二氧化鉿，氧化鐠和氧化鈰來製作金氧半電容並研究其特性。我們在二氧化鉿與砷化銦鎵的電容上得到了等效氧化層厚度為 2.9 奈米的良好尺寸微縮特性，並在具有高銦含量的電容上發現了載子反轉的行為。

我們同時也研究了具有相當高介電常數的氧化鐠以及氧化鈰的電容特性，並發現若以氧化鐠取代二氧化鉿將可得到較高的聚集電容值。費米能帶釘扎的問題也在元件退火溫度的研究中得到解決。

氧化鐠與氧化鈰組成的層狀結構的電容特性也同時被研究。我們發現針對層狀結構所作的二步驟退火將可以增加元件的聚集電容值，其原因我們將利用穿透式電子顯微鏡的圖片來說明。

Study of High-k/III-V MOS Capacitors

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National Chiao Tung University

Abstract

Due to its superior carrier transport capability, III-V based MOS field effect transistor technology has the potential of being used for future high frequency low power application. However, the lack of high quality native oxides has been the obstacle for years. Thanks to high-k dielectric deposition technology improvement, high quality gate dielectrics can now be deposited on III-V material for MOS capacitor studies, which is very important before fabricating III-V MOSFETs.

In this thesis, molecular beam epitaxy (MBE) was used to deposit HfO_2, Pr_6O_{11}, and CeO_2 for MOS capacitors study. Good scalability was obtained with equivalent oxide thickness (EOT) equal to 2.9nm on $HfO_2/In_xGa_{1-x}As$/InP MOS capacitors. The inversion behavior was also observed for high indium concentration $In_xGa_{1-x}As$, the mechanism is discussed in this thesis.

Pr_6O_{11} and CeO_2, which have very high dielectric constant, were also deposited on $In_xGa_{1-x}As$ for MOS capacitor study. It was found that after replacing HfO_2 with Pr_6O_{11}, the accumulation capacitance increases owing to the high dielectric constant of Pr_6O_{11}. The annealing temperature was characterized to unpin the surface Fermi level.

The CeO_2/ Pr_6O_{11} gate stack structure was also studied; two step annealing was introduced to improve the accumulation capacitance. The reason of the capacitance increase was also observed by cross-sectional TEM image.

誌謝

兩年的碩士生活一轉眼便過去，在這之中經歷了許許多多的事情，每件都令我如數家珍並且心懷感激。首先感謝老師在我當初找指導教授四處碰壁時願意讓我加入複合物半導體實驗室，可以說沒有老師便沒有今天的回憶更無法認識我所珍惜的大家，每每看到老師獨自留在辦公室處理事情到深夜都令我對老師工作的態度感到尊敬，實驗室也因老師的帶領才有今天的茁壯。其次是帶我的林岳欽學長，跟在學長身邊的兩年我學到了不只是技術，更多的是做人處事的道理，後者將會是我未來數十年在社會上打滾時所奉行的金科玉律，如果沒有這兩年的磨練或許我在社會上可能會走得更跌跌撞撞。在材料分析上我要感謝延儀學長和宏偉學長的幫忙，深夜的歐傑分析有兩位陪伴都不會孤單。我同時也要謝謝我第一個合作的外國朋友 Dang，真的很謝謝你與我討論分析數據，每次都能有很多心得。再來是我寶貝的同學老皮、阿伯、黑妞、小麥、阿K和蘇煜翔，一同打拼的兩年是無法磨滅的復刻回憶，尤其是老皮跟阿伯，謝謝你們在我剛進入交大這個陌生環境時主動找我聊天介紹你們的同學給我認識，讓我結交了不少朋友。最後是與我朝夕相處的 409 的大家，不論是以前的鴨王、小丸子、小禮和大琦還是現在的宏偉、珍珍、鼎鈞、柏菁和俊佑，能夠和你們同一間研究室是我最大的幸運，與你們天馬行空不著邊際的談天是支持我每天進出無塵室的動力，每次想起都讓我莞爾一笑，也謝謝你們在逼著聽我抱怨時還願意給我安慰與鼓勵。我想跟你們每個人都說一句話表達我的感謝。給宏偉：希望你一切的努力都有收穫能讓你早點畢業，不要被實驗上的挫折打敗，你是我看過最厲害的人。給珍珍：偷偷跟妳說，我當初第一眼看到妳的時候就想要是妳能坐 409 就真的太好了，每次看到妳都覺得很愉快忍不住就會笑出來，妳真的有散播快樂的能力。給柏菁：你超認真的但還是不要讓自己壓力太大，有這麼正的女朋友夫復何求咧，謝謝你常常很晚還陪我吃宵夜，朋友就是降當的。給鼎鈞：說真的，有時你不聽話我超怒的，但當我觀察到你對你所專注的事情都能做得很好以及能堅持自己的意見時，我反而變得

非常的羨慕，希望你能在你的事業上有所成就，開公司時記得照顧學長一下。給俊佑:雖然我常常說你長得壞壞的但其實我是想跟你說我覺得你看起來超酷的，腿又長又會跳舞講話又好笑讓我超級忌妒的。

最後的最後，我要謝謝親愛的爸爸、媽媽還有阿姨從小對我無微不至的照顧，讓我不需要考慮課業之外其他的事情順利的拿到碩士學位，將來請讓我來照顧你們。

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Chapter 1

Introduction

1.1 Research motivation

Moore's Law predicts that the numbers of transistors on an integrated circuit will double every two years. In order to continue this trend, the size of the transistors must be minimized. Strained-Si channel with SiGe buffer layer was used to increase the channel mobility and hence improve the device performance [1-2]. But when the device size was further scaled down to 45nm node, the SiO_2 was too thin to prevent direct tunneling. High-k dielectric has since been introduced as an alternative gate oxide. However consumer product's urgent need of high performance device have forced the transistor size further scaling down to its limit. According to the ITRS roadmap for semiconductor (Figure 1-1), silicon is expected to scale to 22 nm. III-V semiconductor material has been researched actively as alternative channel material to silicon for complementary metal-oxide-semiconductor (CMOS) applications at the 22 nm technology node and beyond due to its intrinsic superior transport property.

1.2 Challenges for high-k/III-V MOS devices

To meet the demands of ITRS roadmap and follow Moore's law, various solutions like high-k dielectrics and high mobility channels including stained-Si, germanium and III-V materials have been researched rigorously. Silicon technology is predicted to reach its limit when entering 22nm node, germanium and III-V material are expected to be alterative p- and n-type channel material for high speed application due to their superior transport properties than silicon as shown in figure 1-2. For III-V materials, characteristics like direct band gap and band engineering have been used in

optoelectronic and high frequency applications. How to integrate III-V material with high-k dielectrics is the challenge to be dealt with now.

The main challenge for integrating high-k on III-Vs is the interface issue. Unlike silicon, the lack of high quality native oxide has been the main obstacle for decades, limiting the implementation of logical and digital applications. Great number of interface traps in the forbidden gap pin the Fermi level, causing so called Fermi level pinning phenomenon, which makes devices unworkable [3]. Many efforts have been done to solve this problem, including anodic treatment, thermal and plasma oxidation of III-V semiconductor surface, but all failed to give electrically and thermodynamically stable gate insulator with low interface traps.

In the past few years, sulfide and ammonia pretreatments were proved to effectively reduce the native oxide and passivate the semiconductor surface. With advanced deposition technology, high quality gate oxide like MBE grown $Ga_2O_3(Gd_2O_3)$ [4], or ALD grown Al_2O_3 [5-8] and HfO_2 [9-12] with low interface trap density of $\sim 10^{11} eV^{-1}cm^{-2}$ could be achieved. In this study, MBE was used to deposit HfO_2, Pr_6O_{11}, and CeO_2 on high indium concentration $In_xGa_{1-x}As$ for MOS capacitors.

HfO_2, owing to its good thermal stability, high dielectric constant and also high energy band gap, it is widely studied on silicon as well as III-V semiconductors. Pr_6O_{11} was used in this study due to it provides high dielectric constant of 32 and similar energy band gap as HfO_2. As for the CeO_2, the energy band gap of CeO_2 is very low, only 3.2eV, and exhibits very diffusive characteristic when directly depositing on InGaAs. But its relatively high dielectric constant of 52 [13] and single crystalline structure inspired us to integrate it with InGaAs by applying gate stack structure.

Most MOS capacitor studies on $In_xGa_{1-x}As$ semiconductor substrate were related to low indium concentration (x=0~0.2) [14-16], but few regarded to high indium

concentration. In this thesis, various high-k/ $In_xGa_{1-x}As$ configured MOS capacitors with high indium concentration (x=0.53, 0.7 and 1) were demonstrated.

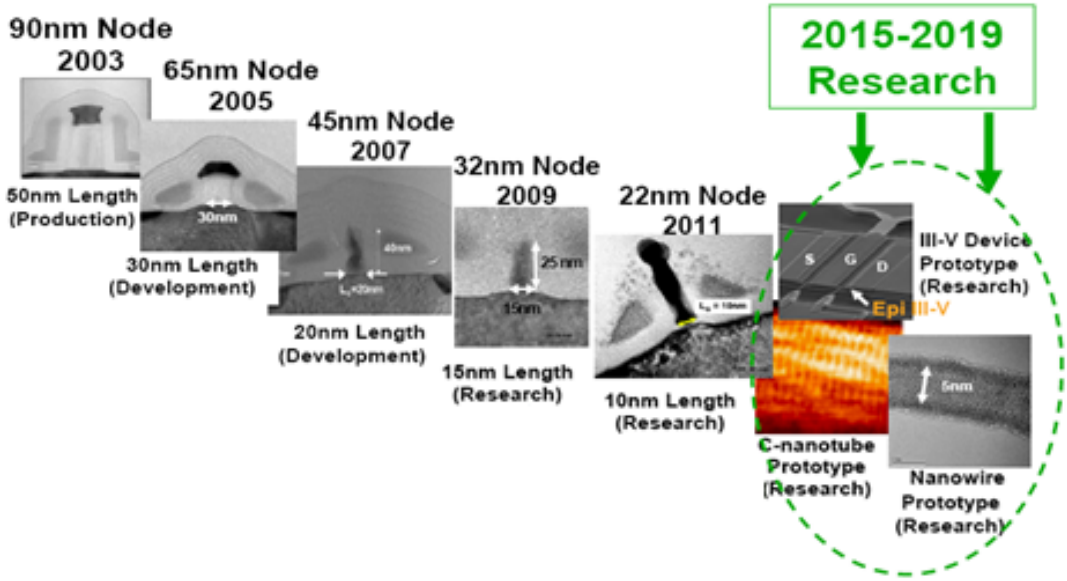


Fig. 1-1 ITRS roadmap of CMOS scaling

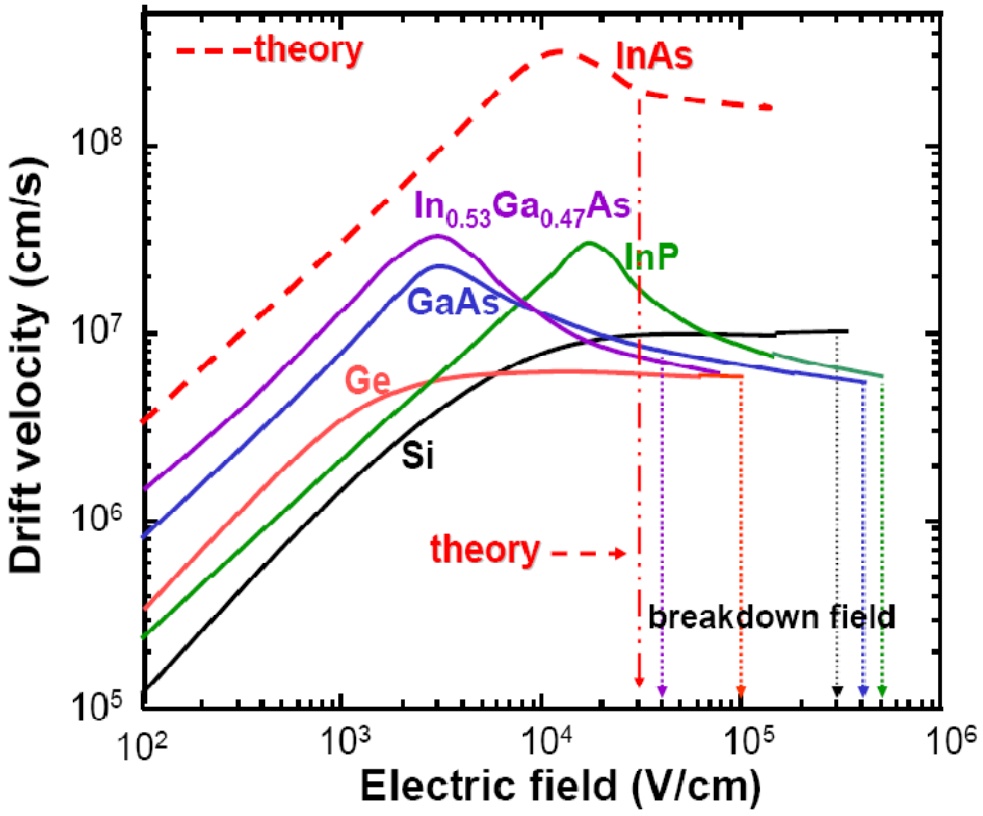


Fig. 1-2 Drift velocities vs. electrical field as a parameter of semiconductors

Chapter 2

Metal-Oxide-Semiconductor Capacitors

The primary reason to study Metal-Oxide-Semiconductor capacitor (MOSCAP) is to understand the principle operation as well as the detailed analysis of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). The MOSCAP is very important in semiconductor device because it is very useful in the study of semiconductor interface. In practical application, it is the kernel of MOSFET, which is the most important device in integrated circuits. It also can be used as a storage capacitor in integrated circuits. In this chapter, the basic MOS structure and its four different modes of operation namely accumulation, depletion, inversion and flatband are studied.

2.1 Basic structure and principle of operation

The MOS capacitor structure is illustrated in figure 2-1. On the top is the gate metal followed by a thin oxide layer; below the thin oxide layer are the semiconductor substrate and the back side metal forming an Ohmic contact.

According to different doping types in substrates, MOS capacitors can be categorized into two types: NMOS with p-type substrate and PMOS with n-type substrate due to inversion layer contains electrons in p-type substrate and holes in n-type substrate. Following discussions are all using p-type substrate based MOS capacitor.

Figure 2-2 is the band diagram of an ideal MOS. Where qØm and qØs stand for work function of metal and semiconductor respectively, which is the energy difference between the Fermi level and vacuum level. And qX is the electron affinity, the energy difference between the conduction band and the vacuum level in semiconductor. Eg is the energy band gap of semiconductor and $q\psi_B$ is the energy difference between

Fermi level E_F and intrinsic Fermi level E_i. The ideal MOS is defined as: (a) at zero bias, the work function difference between metal and semiconductor qØms is zero.

$$q\emptyset ms \equiv (q\emptyset m - q\emptyset s) = q\emptyset m - \left(qX + \frac{Eg}{2} + q\psi_B\right) = 0 \qquad (1)$$

In other words, the energy band is flat when there is no applied voltage, thus, figure 2-2 is also referred as ***flatband*** condition. (b) The only charges that exist in the capacitor under any biasing conditions are those in the semiconductor and those with equal but opposite sign on the metal surface adjacent to the oxide.(c) There are no carrier transport through the oxide under any direct current biasing conditions, on the other hand, the resistivity of oxide is infinite [17].

For ideal MOS capacitor, when one applies positive or negative voltage, the capacitor will be operated in three cases. For instance, when a negative voltage is applied to the NMOS, the excess positive carriers (holes) will accumulate at the oxide-semiconductor interface. In this condition, the band near the interface is bent upward as shown in figure 2-3. The upward bending of intrinsic Fermi level E_i at the interface will increase the energy difference E_i-E_F, which in turn give rise to an enhanced hole concentration. This is called ***accumulation condition***.

When small positive voltage is applied, the energy band is bent downward, as shown in figure 2-4, the majority carriers will be depleted, and the capacitor is now operating in ***depletion condition***.

As an even larger positive voltage is applied, the energy band bent even more, the intrinsic Fermi level at interface is now crossing over the Fermi level, as shown in figure 2-5. In this case, the interface between oxide and semiconductor is like n-type semiconductor, which means, the positive voltage starts to induce electrons at the interface. In this case, the amount of minority carrier (electron) is greater than majority carrier (hole), the interface is thus inverted, an inversion layer is formed, and

the capacitor is in ***inversion condition***.

In the beginning, the electron concentration is larger than n_i but still smaller than substrate doping concentration N_A, the capacitor is in ***weak inversion***. Once the electron concentration in inversion layer reaches N_A, the condition ***strong inversion*** will occur.

Figure 2-6 shows the energy band diagram at the interface of oxide and p-type semiconductor. The electrostatic potential ψ is defined as zero in the bulk of the semiconductor and positive when the band is bent downward, where ψs is the surface potential, by using this concept, the electron density and hole density can be written as a function of ψ:

$$n_P = n_i \exp\left(\frac{q\psi - q\psi_B}{kT}\right) \quad (2a)$$

$$P_P = n_i \exp\left(\frac{q\psi_B - q\psi}{kT}\right) \quad (2b)$$

And at the interface, the surface carrier densities are:

$$n_s = n_i \exp\left(\frac{q\psi_S - q\psi_B}{kT}\right) \quad (3a)$$

$$P_s = n_i \exp\left(\frac{q\psi_B - q\psi_S}{kT}\right) \quad (3b)$$

And since $\psi_B = \frac{kT}{q}\ln\frac{N_A}{n_i}$ equation (3a) and (3b) can be rewritten as

$$n_s = \frac{{n_i}^2}{N_A}\exp\left(\frac{q\psi_S}{kT}\right) \quad (3c)$$

$$P_s = N_A \exp\left(-\frac{q\psi_S}{kT}\right) \quad (3d)$$

The above discussions of flat-band, accumulation, depletion and inversion are summarized below:

$\psi_S < 0$	Accumulation of holes (bands bend upward)
$\psi_S = 0$	Flat-band condition
$\psi_B > \psi_S > 0$	Depletion of holes (bands bend downward)

$\psi_S = \psi_B$ Midgap with n_s=n_p=n_i (intrinsic condition)

$\psi_S > \psi_B$ Inversion (bands bend downward)

2.2 Differential MOS capacitance

The behavior of small-signal capacitance variation with gate bias of MOS capacitor can provide further understanding of the electrical behavior of the MOS system. The static MOS capacitance is defined as $C \equiv \frac{Q}{V}$, where Q is the total charge on the capacitor and V is the gate bias. The small-signal differential capacitance per unit area is:

$$C' \equiv \frac{dQ_S'}{dV_G} \tag{4}$$

For $V_G = V_{OX} + \psi_S$ with $V_{OX} = \frac{Q_S d}{\epsilon_{OX} A} = \frac{Q_S' d}{\epsilon_{OX}}$, equation (4) becomes:

$$C' = \frac{dQ_S'}{\frac{d}{\epsilon_{OX}} dQ_S' + d\psi_S} = \frac{1}{\frac{d}{\epsilon_{OX}} + \frac{d\psi_S}{dQ_S'}} = \frac{1}{\frac{1}{C_{OX}'} + \frac{1}{C_D'}} \tag{5}$$

where C_D' stands for semiconductor capacitance per unit area or depletion-layer capacitance per unit area. Equation (5) also implies that the total capacitance of the MOS capacitor is the series of the fixed capacitance of the oxide and the variable capacitance of the semiconductor as shown in figure 2-7, which depends on the applied gate voltage through the Ψ_S.

When the MOS capacitor is in depletion mode, equation (5) can be rewritten as

$$C' = \frac{1}{\frac{1}{C_{OX}'} + \frac{1}{\frac{\epsilon_S}{W}}} \tag{6}$$

Once the depletion region width reaches its maximum (V_G=V_T), the capacitance has it minimum value, the capacitance per unit area at maximum depletion becomes:

$$C' = \frac{1}{\frac{d}{\epsilon_{OX}} + \frac{W_m}{\epsilon_S}} \text{ (MOS capacitance at maximum depletion)} \tag{7}$$

When the capacitor is in accumulation mode, depletion region diminishes. The capacitance has its maximum value which is equal to C_{OX}'.

$$C' = \frac{1}{\frac{d}{\epsilon_{OX}}} = \frac{1}{\frac{1}{C_{OX}'}} = C_{OX}' \text{ (MOS capacitance in accumulation)} \quad (8)$$

When the applied voltage $V_G > V_T$, there are two extreme conditions: at low frequency, the electron in inversion layer can follow the AC small-signal, the capacitance of the inversion region is equal to the accumulation capacitance, the minority carriers are in thermal equilibrium with the small-signal; and if the frequency is high enough that the minority carriers can not follow, the capacitance will remain unchanged from its value at $V_G = V_T$, which is the minimum capacitance of the maximum depletion.

The capacitance per unit area of depletion, accumulation and inversion of high and low frequency are shown in figure 2-8.

2.3 Non-ideal MOS capacitor

The discussions in former chapters were all assumed that the capacitor is ideal. For non-ideal MOS capacitor there are work function difference, qØms, between gate metal and semiconductor, and also the charge in the oxide need to be considered, which will all change the flat-band voltage of the capacitor.

The work function difference

The work function of a semiconductor qØs, which is the energy difference between the vacuum level and the Fermi level, varies with doping concentration. For a given metal with a fixed work function, the work function difference between the metal and semiconductor is defined as $q\emptyset_{ms} \equiv q\emptyset_m - q\emptyset_s$.

Figure.2-9(a) shows the energy band diagram of an isolated metal and an isolated semiconductor with a oxide layer between them. At thermal equilibrium, the Fermi level should be aligned and the vacuum level should be continuous, which results in the band diagram shown in Fig.2-9(b), the band bending is to accommodate the work function difference. When there is work function difference, the flat-band voltage no longer be zero, an additional voltage must be applied to make the energy band flat.

The flat-band voltage difference between non-ideal and ideal capacitor is

$$\Delta V_{FB} = V_{FB} - V_{FB}^{O} = \emptyset_{ms}. \quad (9)$$

2.3.1 Interface traps and oxide charges

Except for the work function difference, the MOS capacitor will also be affected by charges in oxide and traps in the oxide-semiconductor interface. The basic classification of these traps and charges are shown in Fig.2-10. They are interface-trapped charge (Q_{it}), fixed-oxide charge (Q_f), oxide-trapped charge (Q_{ot}) and mobile ionic charge (Q_m).

With considering Øms, Q_f, Q_{ot}, and Q_m, the flat-band voltage shift becomes

$$\Delta V_{FB} = V_{FB} - V_{FB}^{O} = \emptyset_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_O} \quad (10)$$

The C-V curves of ideal and non-ideal MOS capacitor are shown in Fig.2-11 (a) and (b), respectively. The presence of Øms, Q_f, Q_{ot}, and Q_m shift the flat-band voltage by an amount given by equation (10); if there are large amounts of interface-trapped charges, the interface-trapped charges will vary with surface potential and make the C-V curve stretched-out, which is as shown in Fig.2-11(c).

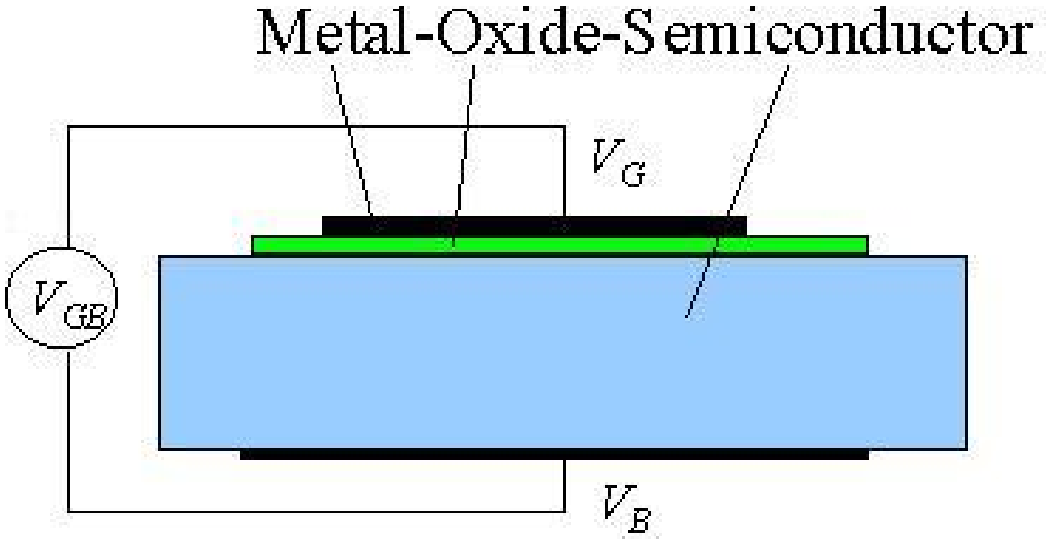


Fig. 2-1 Basic Metal-oxide-semiconductor capacitor structure

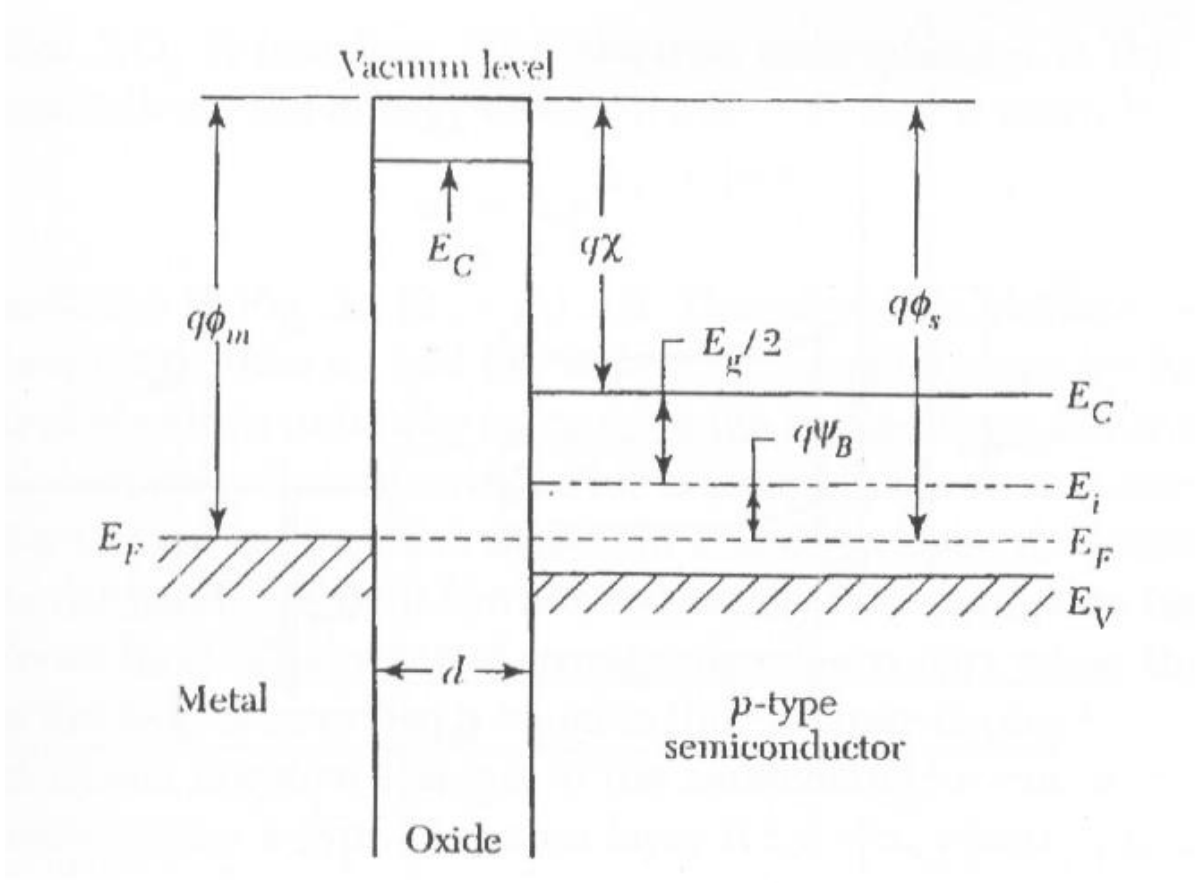


Fig. 2-2 Energy band diagram of an ideal MOS capacitor at V=0 [17]

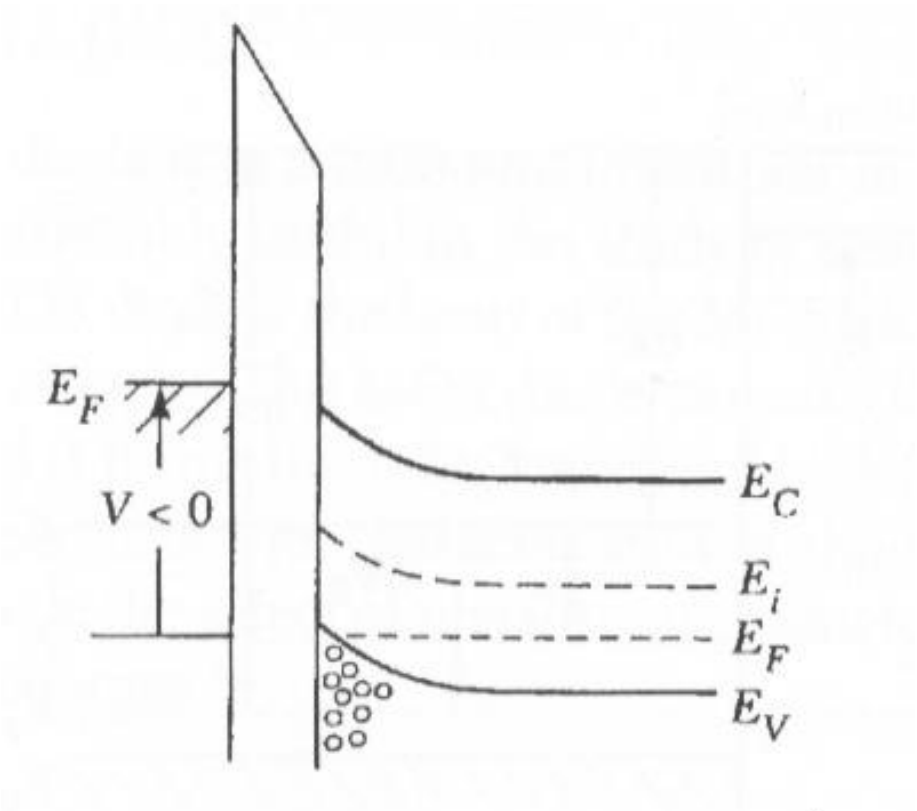


Fig. 2-3 Energy band diagram of an ideal MOS capacitor in accumulation [17]

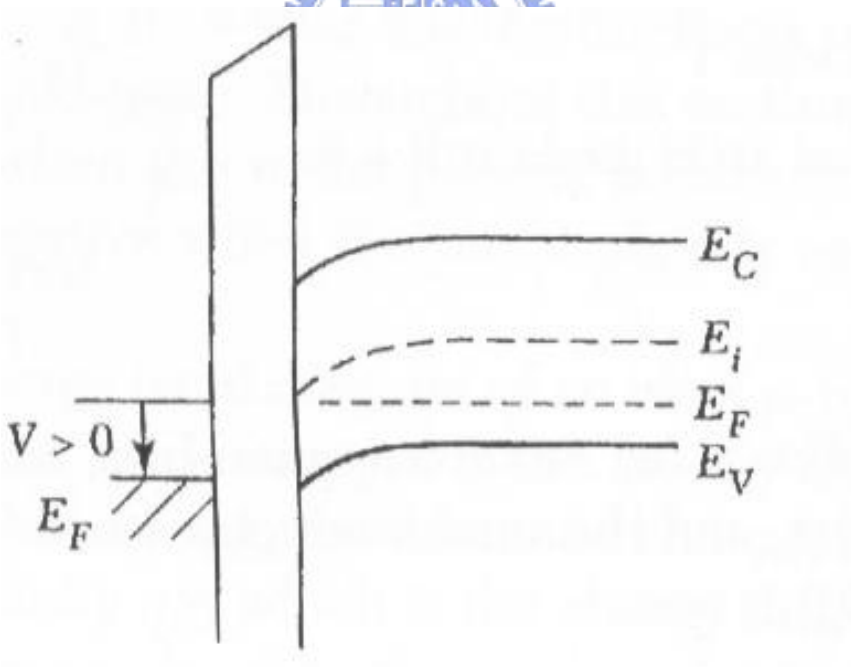


Fig. 2-4 Energy band diagram of an ideal MOS capacitor in depletion [17]

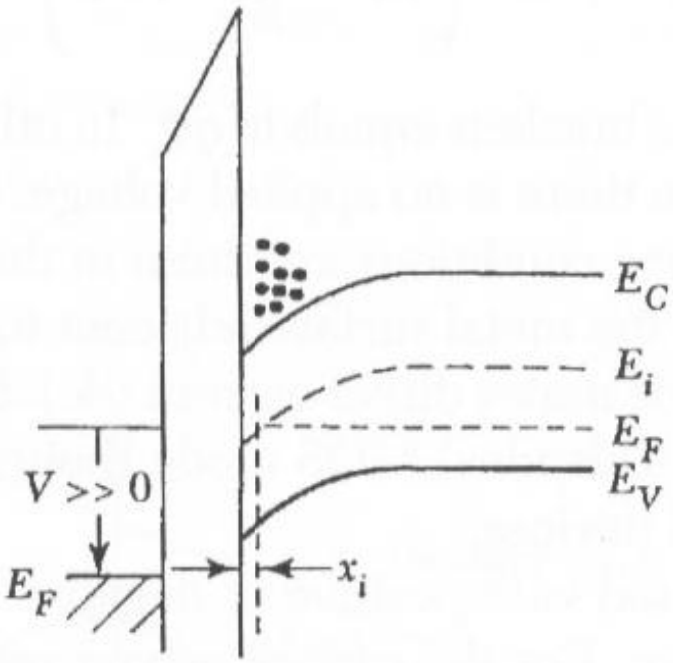


Fig. 2-5 Energy band diagram of an ideal MOS capacitor in inversion [17]

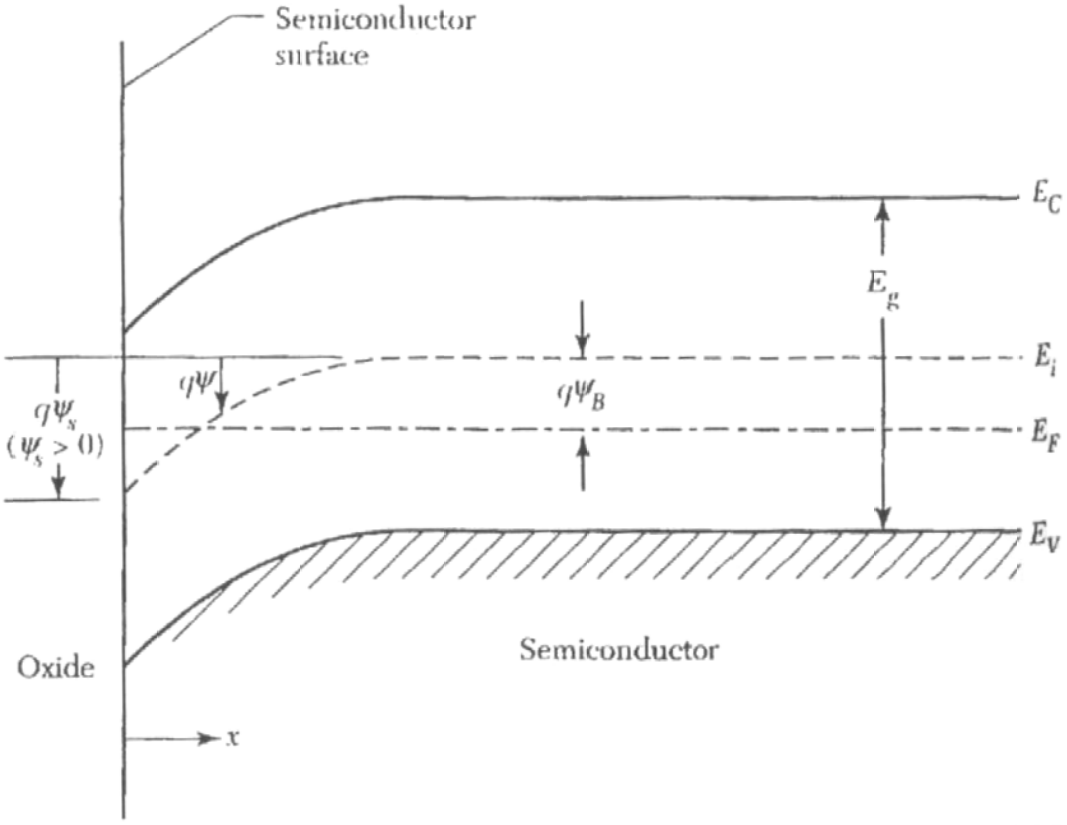


Fig. 2-6 Energy band diagrams at the surface of a p-type semiconductor [17]

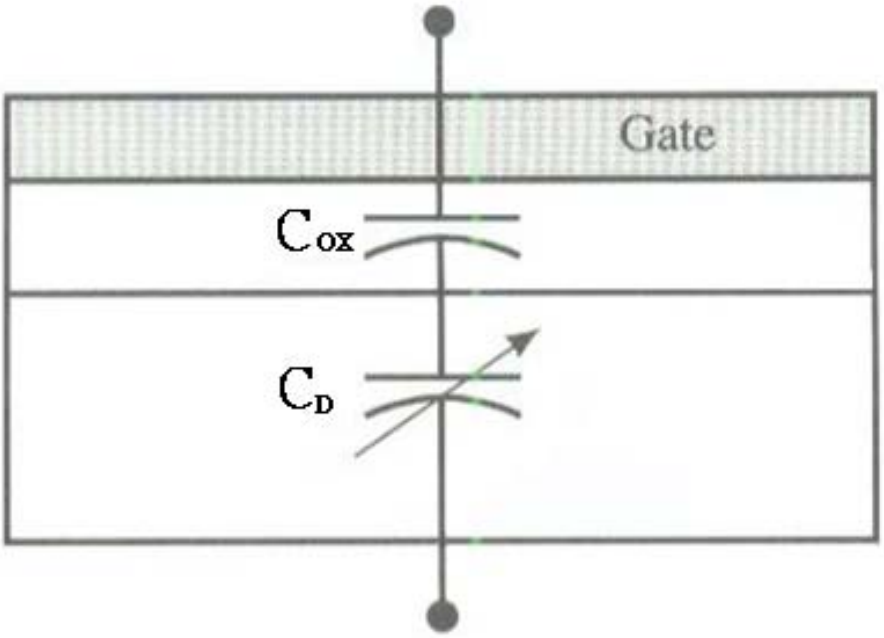


Fig. 2-7 Cross section of an MOS capacitor showing a simple equivalent circuit of oxide capacitance C_{OX} and semiconductor capacitance C_D in series [17]

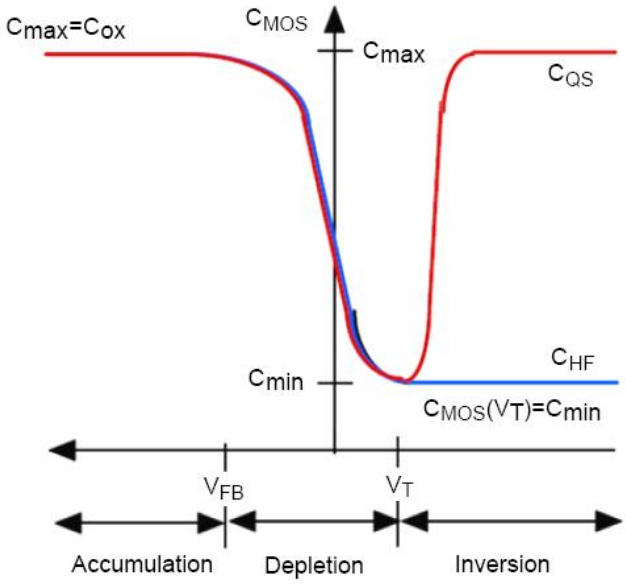


Fig. 2-8 Schematic low- and high-frequency C-V curves showing accumulation, depletion and inversion

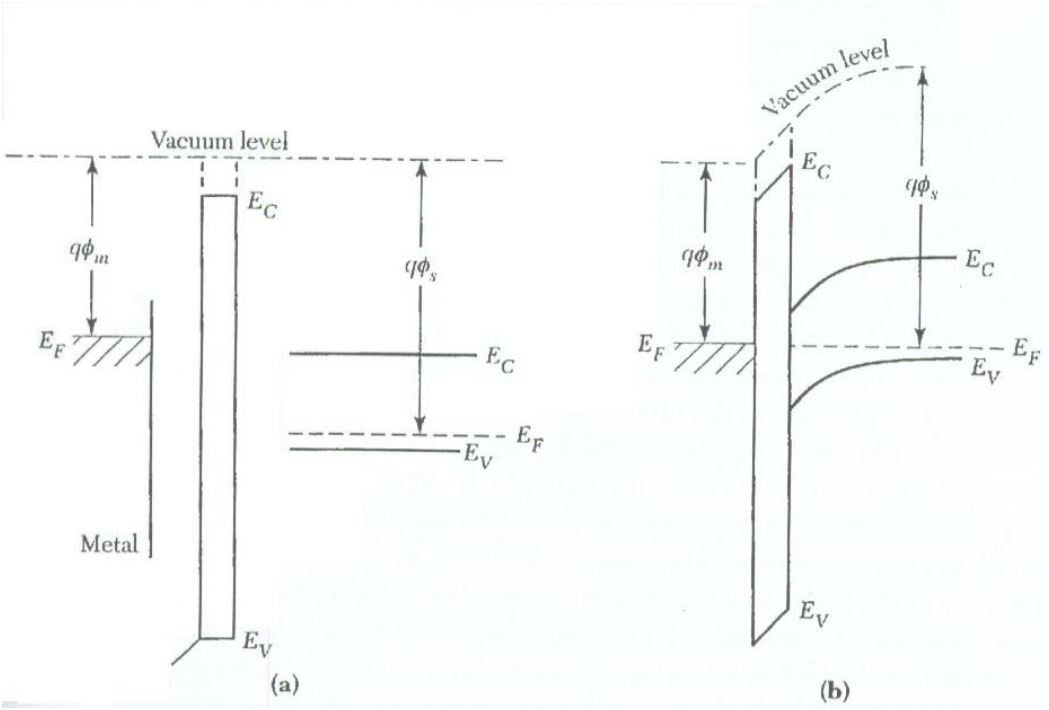


Fig. 2-9 (a) Energy band diagram of an isolated metal and an isolated semiconductor with an oxide layer between them. (b) Energy band diagram of an MOS capacitor in thermal equilibrium [17]

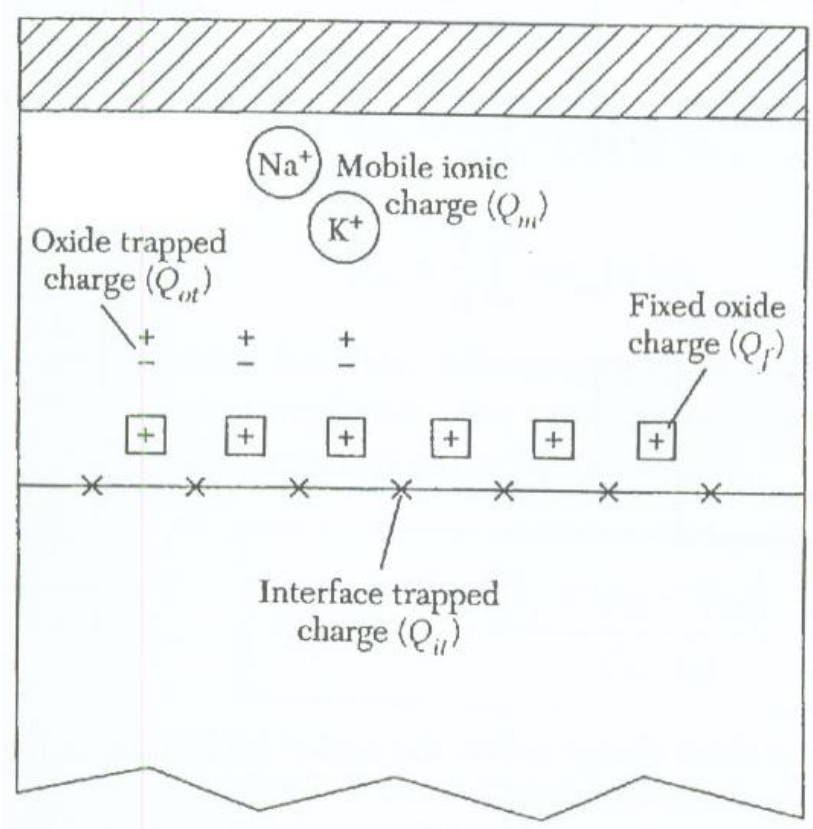


Fig. 2-10 Schematic charges distribution of thermally oxidized silicon [17]

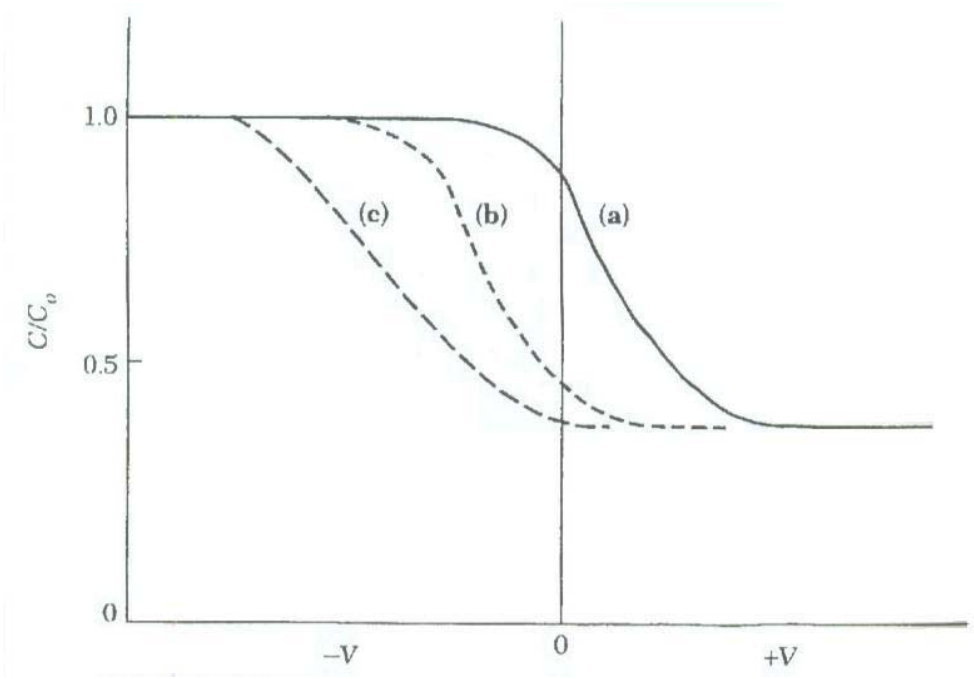


Fig. 2-11 Effect of a fixed oxide charge and interface traps on the C-V characteristics of an MOS capacitor [17]

Chapter 3

High-k/III-V MOS Capacitors Review

3.1 Criteria for choosing high-k dielectrics

1. Dielectric constant and barrier height:

When choosing the gate dielectrics, usually the dielectric constant is the number of thumbs we will consider. But as the thickness is decreasing, preventing direct tunneling is also the main function of gate dielectric. Thus the energy band gap and the barrier height are becoming more important. Table 3-1 lists the dielectric constants and energy band gap of commonly used high-k candidates [18] and figure 3-1 and figure3-2 show the calculated band offsets of oxides on GaAs and InAs [19].

2. Thermal stability:

Thermal stability is important due to many MOS process undergo high temperature ambient, including rapid thermal annealing (RTA). To avoid current leakage and sufficiently storage charges, the amorphous type or single crystalline gate dielectrics with high re-crystallization temperature are required.

3. Good interface property:

Interface quality is the most important issue for MOS devices. Carriers at the oxide-semiconductor interface will be trapped if the interface states or traps density (D_{it}) are too high. For silicon MOS devices, the interface trap density is usually on the order of $10^{10}eV^{-1}cm^{-2}$, but for III-V MOS devices, it was always two or three orders higher than that, which was the main problem for III-V MOS device operation and the origin of Fermi level pinning. Figure 3-3 shows the schematic diagram for Fermi level pinning phenomenon [20]. The high density of interface traps will pin the Fermi level, capture and emit carriers at the interface, which make the device unworkable or result in frequency dispersion among C-V curves measured at different frequency. With the

surface pretreatment before deposition, the native oxide of III-V materials which was considered to be the origin of interface traps and with lower-k value could be reduced. Also with the progress of vacuum technology and new methods for depositing high-k dielectrics, like Atomic Layer Deposition (ALD) and Molecular Beam Epitaxy (MBE), the inversion type III-V MOSFET has been fabricated, but the device performance still need to improve.

3.2 Device characterization

3.2.1 C-V measurement

To get the capacitance-voltage characteristic, one can connect the front side and backside electrodes of the device with LCR impedance analyzer probes. By changing the frequency of the supplied AC signal, the high and low frequency CV curves can be plotted. Following are some parameters which are often used to judge the device performance:

1. Equivalent oxide thickness (EOT)

$\mathrm{EOT} = \frac{t_{ox} \times k_{SiO_2}}{k}$. It is used to characterize how the given dielectric can achieve the same capacitance of thin SiO_2 layer with thicker physical thickness.

2. Flatband voltage

Flatband voltage is of importance due to it determines the gate voltage at which there are no charge in the semiconductor. It separates the accumulation and depletion conditions. The ideal flatband voltage can be determined by setting the work function difference in the simulation tool and assuming there are no trap charges existing in the oxide or oxide/semiconductor interface. By comparing the flatband capacitance between the simulated and measured curves, the flatband voltage shift ΔV_{FB} determines the oxide quality.

3. Hysteresis

Hysteresis is measured by sweeping the gate voltage forth and back. The amount of hysteresis stands for the amount of charges trapped by the defects in the oxide, thus it can be used to determine the oxide quality. The clockwise hysteresis implies the negative charges were trapped; on the other hand, the counterclockwise hysteresis implies the positive charges were trapped by the defects. The defects extracted from hysteresis are also called slow trapping states, where the interface traps are fast trapping states.

4. Frequency dispersion

Frequency dispersion is the phenomenon of accumulation capacitance varying with operation frequency. In silicon MOS capacitors, it is due to leakage current of ultra thin oxide, making the capacitor can not storage charge, causing the total capacitance decrease. For high-k/III-V case, the oxide thickness is not as thin as silicon MOS, the causing of frequency dispersion is the poor quality interface where large amounts of interface traps exist at the semiconductor surface. The interface traps are frequency dependent, it will capture and emit charges distorting the C-V curves causing frequency dispersion, and more seriously, will induce Fermi level pinning and stop the device operating.

3.2.2 Conductance measurement

The quality of oxide/semiconductor interface remains essential for MOS device performance. One direct effect moving from traditional Si MOSFET to III-V MOSFET is the high interface state densities (Dit), which are known to strongly affect driving current of the devices.

Some methods have been utilized to evaluate Dit, for example, low frequency method (quasi-static method), high frequency method (Terman method), charge pumping and

conductance method. The first two methods use the capacitance-voltage relationship extracting the Dit, the equivalent components models includes: oxide capacitance, depletion layer capacitance and interface-trap capacitance. Since the depletion-layer capacitance is in parallel with interface trap capacitance, difference in capacitance must be calculated, which leads to inaccuracies in extracting the information of interface state. Further more, although the low frequency quasi-static method was the most common one for dielectrics with low leakage current, but with extremely shrinkage of device size, the leakage current associated with direct tunneling through a thin oxide makes the measurement difficult to perform. Charge pumping is a very sensitive to the interface states but it requires fully processed MOSFET device. In this research, we used conductance method to characterize the interface properties of the MOS capacitors. In chapter 3.2.3, the principle of conductance method of extracting Dit is introduced.

3.2.3 Extract Dit from conductance method

In 1967, Nicollian and Goetzberger of Bell Lab. gave a detailed and comprehensive discussion for the conductance method, in which conductance is directly related to the interface traps, which can give more accurate results. The data extraction is based on the measurement of the equivalent parallel conductance, G_P, of a MOS capacitor as a function of bias voltage and frequency as shown in figure 3-4 [21]. The conductance representing the lossy mechanism from interface trap, capturing and emitting carriers, is an index of the interface trap density. Figure 3-5 shows the equivalent circuit of the measurements [22], where C_{OX}, C_S, C_{it}, represent oxide capacitance, semiconductor capacitance and interface trap capacitance respectively.

The above assumption neglected the series resistance of substrate and oxide leakage current. From the measured capacitance C_m and conductance G_m, the parallel

conductance G_P is given by equation (1), and Dit is given by equation (2),

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{OX}^2}{G_m^2 + \omega^2 (C_{OX} - C_m)^2} \quad (1)$$

$$D_{it} = \frac{2.5}{q} \left(\frac{G_P}{\omega}\right)_{max} \quad (2)$$

Where $(G_P/\omega)_{max}$ is the peak value from a G_P/ω-frequency plot.

But actually the device does exist series resistance for thin oxide or leaky oxide. The equivalent circuit is converted to figure 3-5(d) with G_t stands for tunnel conductance and r_s stands for series resistance. Equation (1) becomes

$$\frac{G_P}{\omega} = \frac{\omega C_{OX}^2 (G_c - G_t)}{G_c^2 + \omega^2 (C_{OX} - C_c)^2} \quad (3)$$

Where

$$C_c = \frac{C_m}{(1 - r_s G_m)^2 + (\omega r_s C_m)^2} \qquad G_c = \frac{\omega^2 r_s C_m C_c - G_m}{r_s G_m - 1} \quad (4)$$

The series resistance is determined y biasing the device into accumulation region

$$r_s = \frac{G_{ma}}{G_{ma}^2 + \omega C_{ma}^2} \quad (5)$$

C_{ma} and G_{ma} are the measured capacitance and conductance in accumulation. The tunnel conductance G_t is determined from G_c by setting the $\omega \to 0$

$$G_c = \frac{G_m}{1 - r_s G_m} \quad (6)$$

For r_s and G_t equal to 0, equation (3) reverts to equation (1).

Table 3-1 Comparison of relevant properties for high-K candidates [18]

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8[a]	Amorphous
Y_2O_3	15	5.6	2.3[a]	Cubic
La_2O_3	30	4.3	2.3[a]	Hexagonal, cubic
Ta_2O_5	26	4.5	1–1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.[c] (rutile, anatase)
HfO_2	25	5.7	1.5[a]	Mono.[b], tetrag.[c], cubic
ZrO_2	25	7.8	1.4[a]	Mono.[b], tetrag.[c], cubic

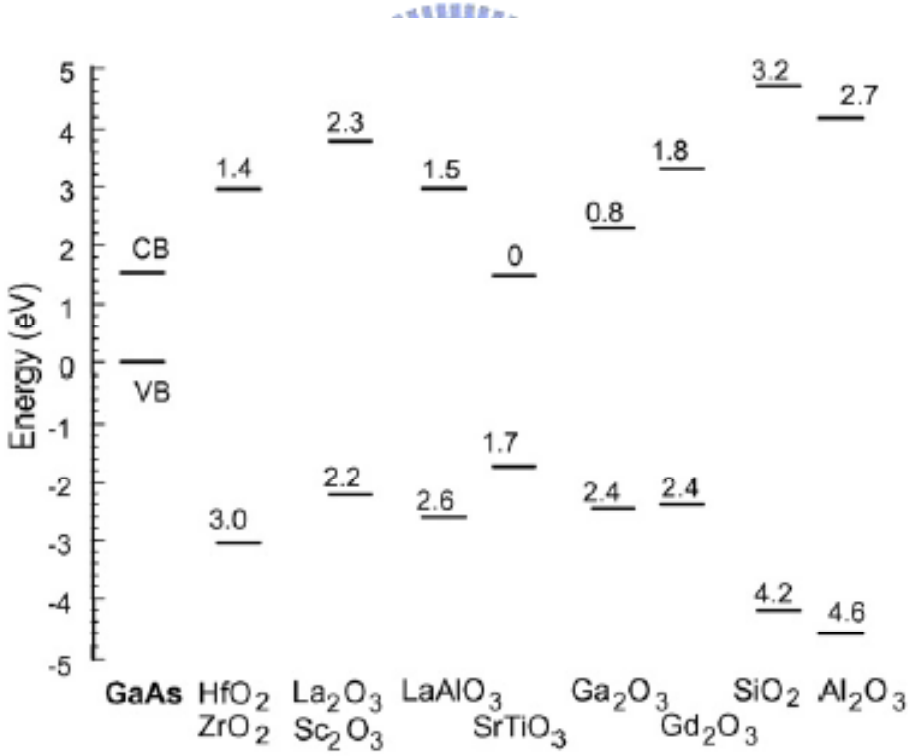


Fig. 3-1 Schematic band offsets of high-k dielectrics on GaAs [19]

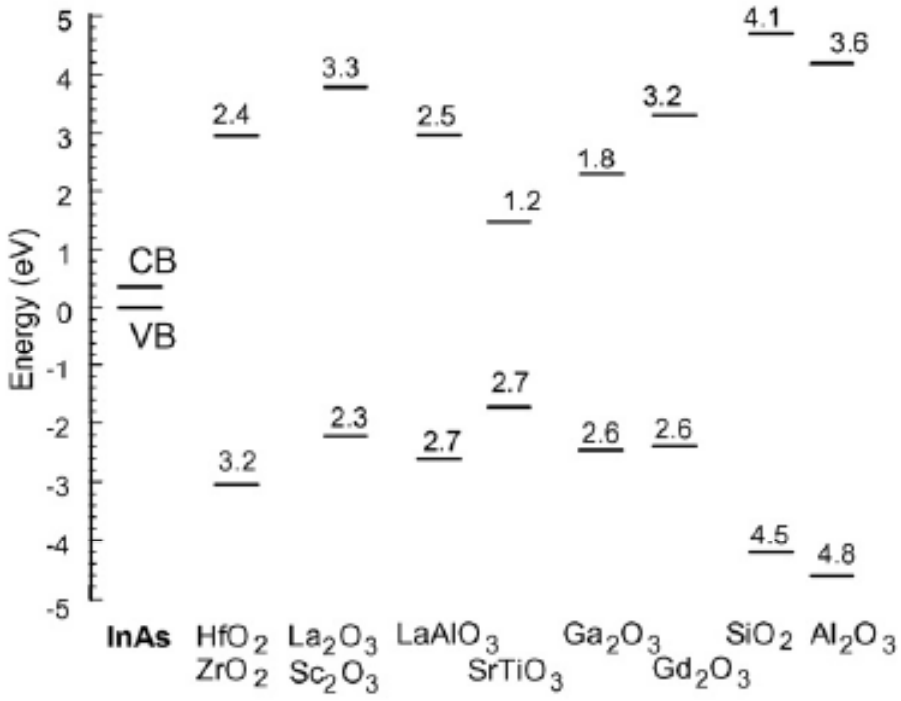


Fig. 3-2 Schematic band offsets of high-k dielectrics on InAs [19]

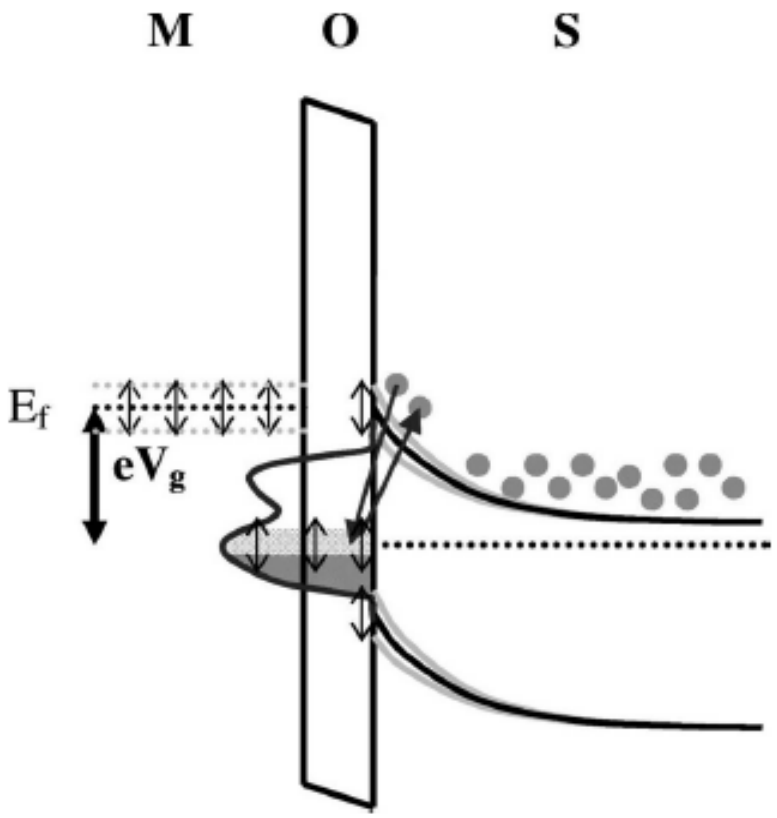


Fig. 3-3 Schematic Fermi level pinning phenomenon [20]

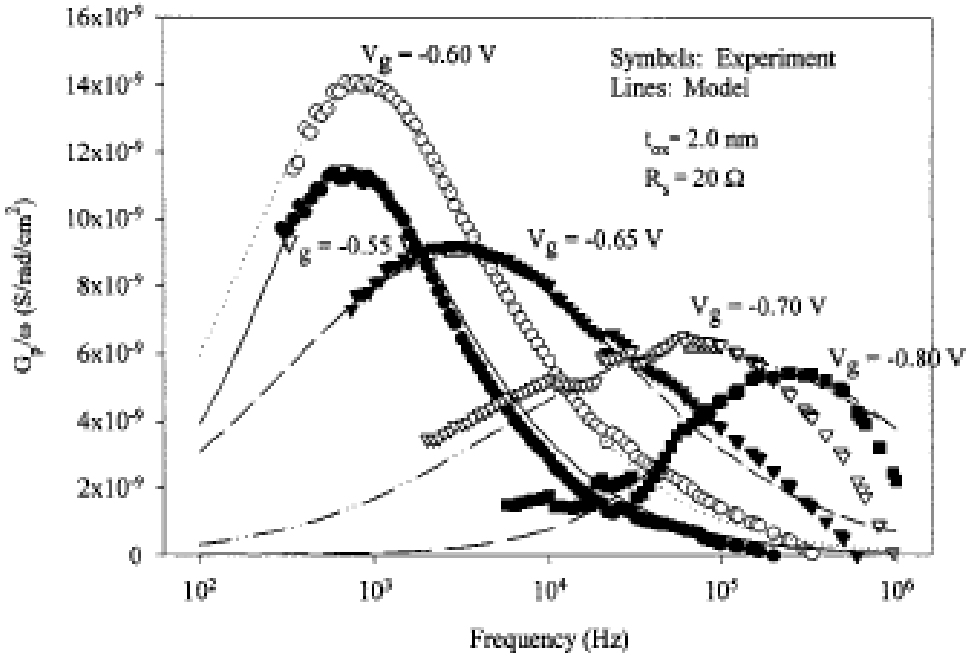


Fig. 3-4 Schematic experimental and modeled interface state conductance [21]

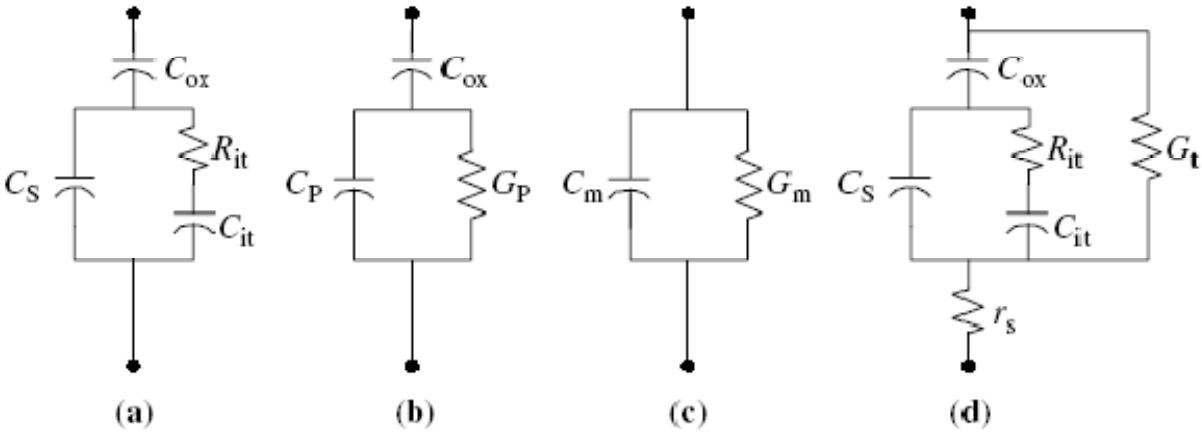


Fig. 3-5 Equivalent circuits for conductance measurement: (a) MOS-C with interface trap time constant $\tau_{it}=R_{it}C_{it}$, (b) simplified circuits of (a), (c) measured circuit, (d) including series r_s resistance and tunnel conductance G_t [22]

Chapter 4

Experimental

In this chapter, the structures which were used in this study and the experiment process flow will be described.

4.1 Device structures

The first structure contains 100nm silicon-doped $In_{0.53}Ga_{0.47}As$ layer(n-type, $5x10^{17}cm^{-3}$) which was grown on (001) InP substrate by MBE as shown in figure 4-1(a). The second structure contains 5nm $In_{0.7}Ga_{0.3}As$ layer and 10nm $In_{0.53}Ga_{0.47}As$ layer (both are silicon-doped with doping concentration of $5x10^{17}cm^{-3}$) on (001) InP substrate as shown in figure 4-1(b). The third structure contains 5nm InAs layer, 10nm $In_{0.7}Ga_{0.3}As$ layer and 3nm $In_{0.53}Ga_{0.47}As$layer (all are n-type with silicon doping concentration of $5x10^{17}cm^{-3}$) on (001) InP substrate as shown in figure 4-1(c).

4.2 Process flow

4.2.1 Wafer cleaning

The first step is wafer cleaning. The wafers were immersed into ACE and IPA, each for 5 minutes to remove contaminant, and then they were dried by blowing nitrogen gas.

4.2.2 Surface treatment

Surface treatment is a very important step before depositing high-k dielectric on high speed III-V semiconductor. The untreated surfaces are reported to leave native oxide, which will affect the performance. After the treatment, the native oxide is eliminated and a thin passivation film is formed on the top of the semiconductor, which prevents

inner semiconductor react with oxygen in atmosphere.

The $(NH_4)S_X$ was chosen as surface treatment solution. The dilute HF:H_2O (1:100) solution was first applied for removing the native oxide, followed by dipping the wafer in $(NH_4)S_X$ for 30 minutes at room temperature. The depth of the passivating thin film can be determined by the immersing time and reacting temperature.

4.2.3 High-k dielectric deposition

After surface treatment, the wafers were transferred into MBE chamber immediately to prevent them stay too long in atmosphere.

Several high-k dielectrics configuration were chosen to apply on the III-V substrates. Some were deposited singly and some were grown on the other dielectric which was deposited in advance to form composite dielectrics. The rapid thermal annealing (RTA) was held after high-k dielectrics deposition to improve the oxide-semiconductor interface quality, two or only one step RTA process for the composite oxide were also performed to achieve better device characteristics.

4.2.4 Electrodes metal formation

Finally, aluminum was chosen as gate and backside metal, which was deposited by electron gun evaporation.

The schematic process flow is shown in Fig. 4-2

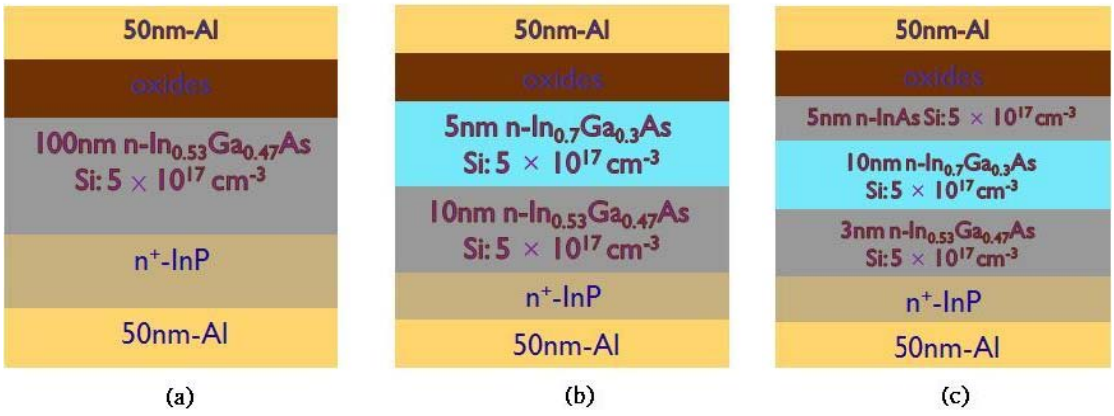


Fig.4-1 Structures of MOS capacitor in this study

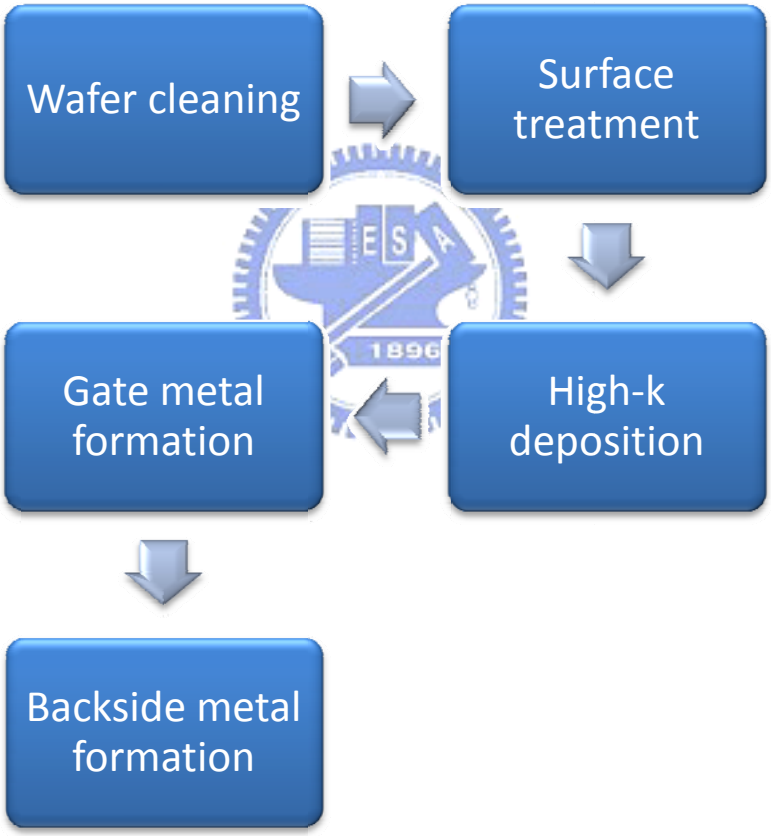


Fig. 4-2 Process flow of High-k/III-V MOS capacitor fabrication

Chapter 5

Results and discussion

5.1 Study of HfO_2/ $In_xGa_{1-x}As$ MOS capacitors

HfO_2 was first deposited on $In_{0.53}Ga_{0.47}As$ with varied thickness of 12nm, 9nm and 6nm for oxide scaling study. Its C-V characteristic is shown in figure 5-1. The equivalent oxide thickness extracted from 10kHz curves were 5.76nm, 3.5nm and 2.9nm, respectively, which showed good scalability. The curves in the negative voltage region exhibited well inversion behavior, which could be referred as unpinning of Fermi level [23]. The deep-depletion phenomenon for devices with 9nm and 6nm HfO_2 can be explained that the minority carriers could not follow the high frequency small signal, keep biasing the device will further increase the depletion region, resulting in deep-depletion phenomenon [24]. Whether the thickness affects the inversion phenomenon is still under research.

After successfully investigating the $HfO_2/In_{0.53}Ga_{0.47}As$ capacitors, HfO_2/InAs MOS capacitors were also studied, the thickness of HfO_2 was 9nm. The devices were annealed under different temperatures to observe the accumulation capacitance change and the inversion behavior. Figure 5-2 shows the C-V characteristic of the devices which were annealed at 500^OC and 400^OC. The HfO_2/InAs devices didn't exhibit deep-depletion as $HfO_2/In_{0.53}Ga_{0.47}As$ devices performed. This could be explained that the minority carrier response time could be shorter in InAs due to its smaller band gap, shorter minority carrier life time (τ_L) and higher intrinsic carrier concentration ($1.25x10^{15}cm^{-3}$ for InAs, $3.96x10^{11}cm^{-3}$ for $In_{0.53}Ga_{0.47}As$). Furthermore, defects and impurities can also act as source for generation of minority carriers and bulk traps may shorten the minority carrier life time [25]. To fully understand the

minority carrier behavior of device, C-V curves measured at different temperature is still on the progress.

In figure 5-2 (b), device underwent 400^{O}C annealing showed large frequency dispersion at low frequency as compared to the device underwent 500^{O}C annealing, which may due to the interface traps' response. For silicon MOS capacitor, the dispersion phenomenon may due to a very thin and lossy gate dielectric; many models have been constructed to explain this phenomenon [26-27]. But for III-V MOS research, the dispersion phenomenon is mainly due to the interface traps, although mechanism is still not very well understood. Figure 5-3(a) shows the equivalent circuits including interface traps effects. C_{OX} and C_D are the oxide capacitance and semiconductor depletion layer capacitance, respectively [28]. C_{it} and R_{it} are the capacitance and resistance associated with the interface traps. They are also the function of energy. The product $C_{it}R_{it}$ is defined as the interface trap life time τ_{it}, which determines its frequency behavior. The parallel branch of figure 5-3 (a) can be converted into a frequency-dependent capacitance C_P and a frequency-dependent conductance G_P in parallel with each other as shown in figure 5-3 (b). C_P and G_P which were mentioned in former chapter can also be written as

$$C_P = C_D + \frac{C_{it}}{1+\omega^2\tau_{it}^2} \quad (1)$$

$$\frac{G_P}{\omega} = \frac{C_{it}\omega\tau_{it}}{1+\omega^2\tau_{it}^2} \quad (2)$$

At low frequency, R_{it} can be neglected, and C_D is in parallel with C_{it}. If the measurement frequency is too high for interface traps to respond, then C_{it} and R_{it} can be ignored. The simplified equivalent circuits for both conditions are shown in figure 5-3 (c) and (d). The measured capacitances for these two conditions are:

$$C_{LF} = \frac{C_{OX}(C_D+C_{it})}{C_{OX}+C_D+C_{it}} \quad (3)$$

$$C_{HF} = \frac{C_{OX}C_D}{C_{OX}+C_D} \quad (4)$$

For silicon MOS capacitors, when measured at low frequency and biased at the accumulation region, C_D is very large due to no depletion region forms, and C_{it} can be neglected owing to high quality interface. Thus the total capacitance is equal to C_{OX}. But for III-V case, the capacitance of interface traps must be considered, and is frequency dependent, so that the capacitance is varied with frequency, causing frequency dispersion. Even measured at high frequency, if the frequency is not sufficiently high so that the traps can not response, the frequency dispersion will also be found in high frequency curve. The interface trap distribution for two annealing temperatures measured at various bias are shown in figure 5-4, 400^{O}C annealed device exhibited larger interface traps than 500^{O}C annealed device, which could explain the large frequency dispersion in 400^{O}C annealed C-V curve.

Finally the hysteresis performance of two annealing temperature is shown in figure 5-5. 108mV for 400^{O}C annealed device and 214mV for 500^{O}C annealed device. We would expect the value could be lower than 100mV after optimizing the annealing temperature.

5.2 Capacitance increase by replacing Pr_6O_{11} to HfO_2 as gate oxide on $In_xGa_{1-x}As$

To investigate the capacitance increasing by replacing Pr_6O_{11} to HfO_2 on InGaAs channel, two type oxides with the same thickness were grown on $In_{0.7}Ga_{0.3}As$ channel. Figure 5-6 shows the C-V curve of these two devices. The accumulation capacitance was arising apparently in Pr_6O_{11} applied sample. The inversion phenomenon was not clear, which may due to high interface traps.

Figure 5-7 compares the capacitance-voltage characteristic of Pr_6O_{11} (10nm)/$In_{0.53}Ga_{0.47}As$ devices annealed at 450, 500 and 550^{O}C. The accumulation

capacitance of 450^{O}C annealed device showed almost no saturation. The transition from accumulation to depletion was not very sharp, indicating poor interface quality. After increasing annealing temperature to 500^{O}C, the transition became conspicuous, and the accumulation capacitance began to saturate, but the inversion behavior still not very apparent as compared to former device using HfO_2, indicating Fermi level pinning at the oxide/semiconductor interface. The 550^{O}C annealed device showed inversion behavior, which we speculate that the Fermi level was unpinned. The deep-depletion phenomenon of 550^{O}C annealed sample could be explained that more oxide charges (including fix oxide charges and oxide trap charges) were generated during high temperature annealing, which caused large hysteresis as compared to the 500^{O}C annealed device, which is shown in the inset of figure 5-7 (b). The other possible explanation for the deep-depletion phenomenon in the 550^{O}C device could be in the microstructure view. Figure 5-8 shows the TEM image of the 550^{O}C annealed device, the oxide is neither single-crystalline nor amorphous, but poly-crystalline type, which provided leakage current paths for the minority carriers. Since the minority carriers tunnel through the oxide to the gate electrode, the inversion layer could not form [29]. Again, the depletion region will continue to increase to maintain charge balance when keep biasing the device, which resulting in deep-depletion.

From the discussion, we expect that the accumulation capacitance could increase if single-crystalline of amorphous type Pr_6O_{11} could be grown for better insulation capability.

5.3 Capacitance increase by using two-step annealing process on CeO_2/Pr_6O_{11} gate stack structure

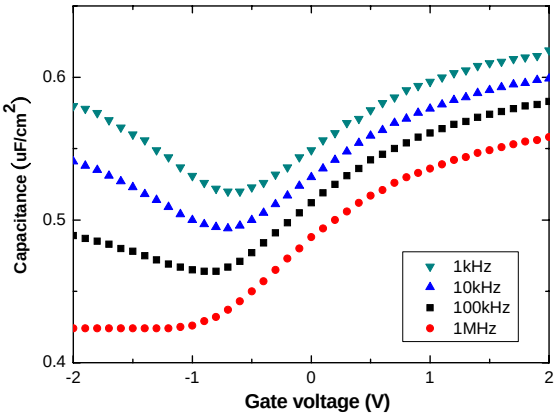
Figure 5-9(a) shows the C-V curve of directly deposited CeO_2 on $In_{0.7}Ga_{0.3}As$ The device exhibited no capacitor function, and figure 5-9(b) is the TEM image and EDX analysis of the device. Serious inter-diffusion was found in the device, great amount of indium, gallium and arsenic were detected in the CeO_2, which should not occur for a gate dielectric.

Based on previous study, Pr_6O_{11} was chosen as a diffusion barrier. Figure 5-10 shows the cross-sectional TEM image and EDX analysis of CeO_2 (8nm)/Pr_6O_{11} (6nm)/InAs device. After applying 4nm Pr6O11 beneath the CeO2 the diffusion was suppressed. The EDX analysis indicated some InGaAs contents still existing in oxide layer, but the device exhibited normal C-V characteristic as shown in figure 5-11.

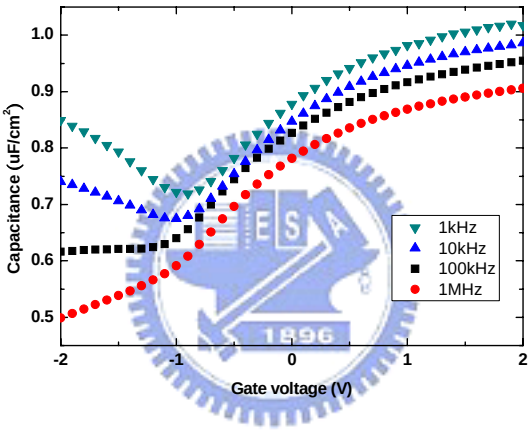
Figure 5-11 compares the C-V characteristic between two annealing process for CeO_2 (8nm)/Pr_6O_{11} (6nm)/InAs device. Both of two devices exhibited inversion behavior, which we ascribed to the high intrinsic carrier density and short minority carrier response time of low energy band gap InAs layer. The device underwent only one-step annealing process after Pr_6O_{11} deposition showed lower accumulation capacitance than that underwent two-step annealing process. Two-step annealing consists of first step annealing at $500^{O}C$ after Pr_6O_{11} deposition and second step annealing at $400^{O}C$ after CeO_2 deposition, while one-step annealing only consists of first step annealing after Pr_6O_{11} deposition. The increase of accumulation capacitance was owing to the thickness decrease of Pr_6O_{11} after the second step annealing as shown in figure 5-12, showing the effectiveness of two-step annealing process on those devices with two oxides as gate dielectrics.

To further increase the accumulation capacitance the CeO_2 thickness was reduced to 6nm, totally 10nm CeO_2/Pr_6O_{11} on InAs. Figure 5-13 compares the C-V characteristics of two devices with different first step annealing temperature, and both underwent second step annealing at 400^OC after CeO_2 deposition. For the device first annealed at 500^OC, the capacitance increase was due to the decrease of the CeO_2 thickness, but it also accompanied with leakage current increase. The C-V curve of the device first annealed at 550^OC showed more severe current leakage than 500^OC annealed device, which we ascribed to the re-crystallization of Pr_6O_{11} generated current leakage paths. Figure 5-14 shows the TEM images of the first step 500^OC and 550^OC annealed devices.

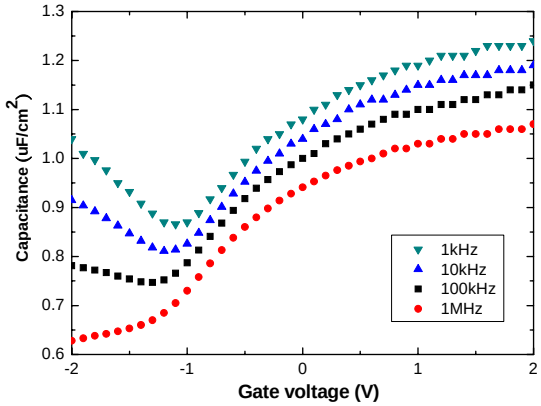
Table 5-1 summarizes the EOT of the CeO_2/Pr_6O_{11}/InAs devices. As compared to the HfO_2 gated devices shown in Table 5-2, the CeO_2/Pr_6O_{11} gate stack structure showed large EOT than HfO_2, which was not the result we expected. Except for the thickness for the CeO_2/Pr_6O_{11} gate stack were larger than HfO_2, the poly-crystalline structure and rough surface of the gate stack couldn't effectively storage the charges which resulted in low accumulation capacitance.



(a)

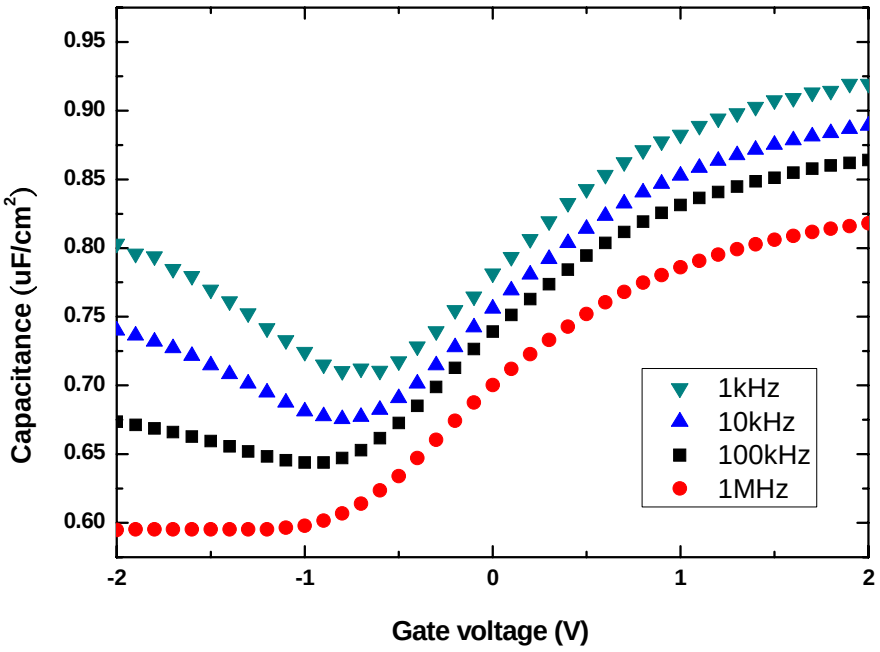


(b)

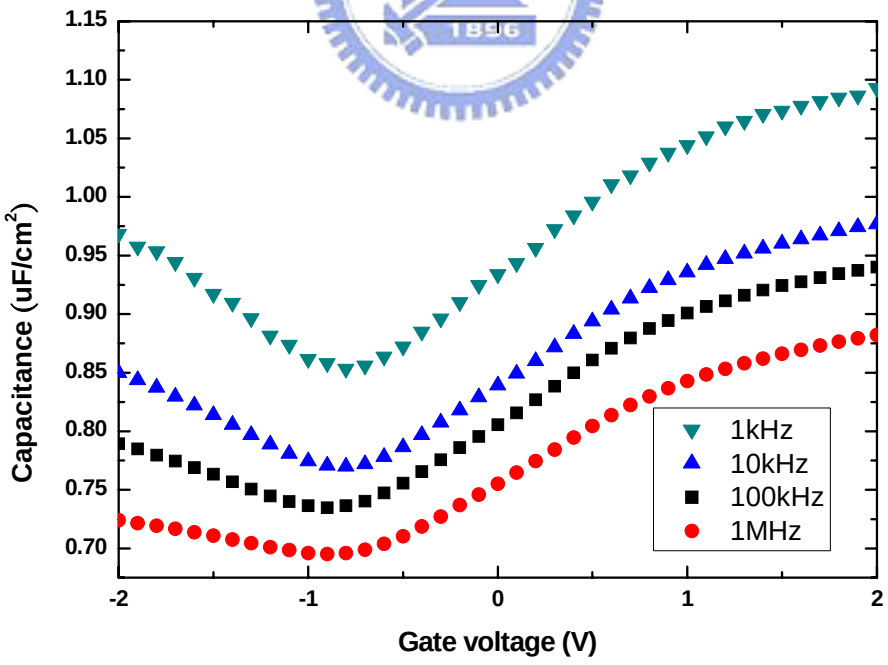


(c)

Fig. 5-1 C-V curves of (a) 12nm, (b) 9nm and (c) 6nm HfO_2 on $In_{0.53}Ga_{0.47}As$ PDA at $600^{O}C$



(a)



(b)

Fig. 5-2 C-V curves of HfO_2 (9nm)/InAs devices. (a) PDA at 500^{O}C. (b) PDA at 400^{O}C

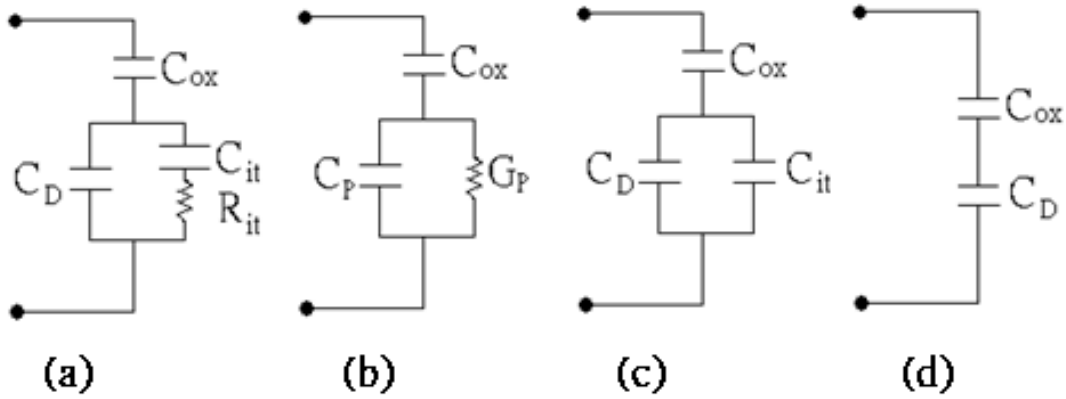
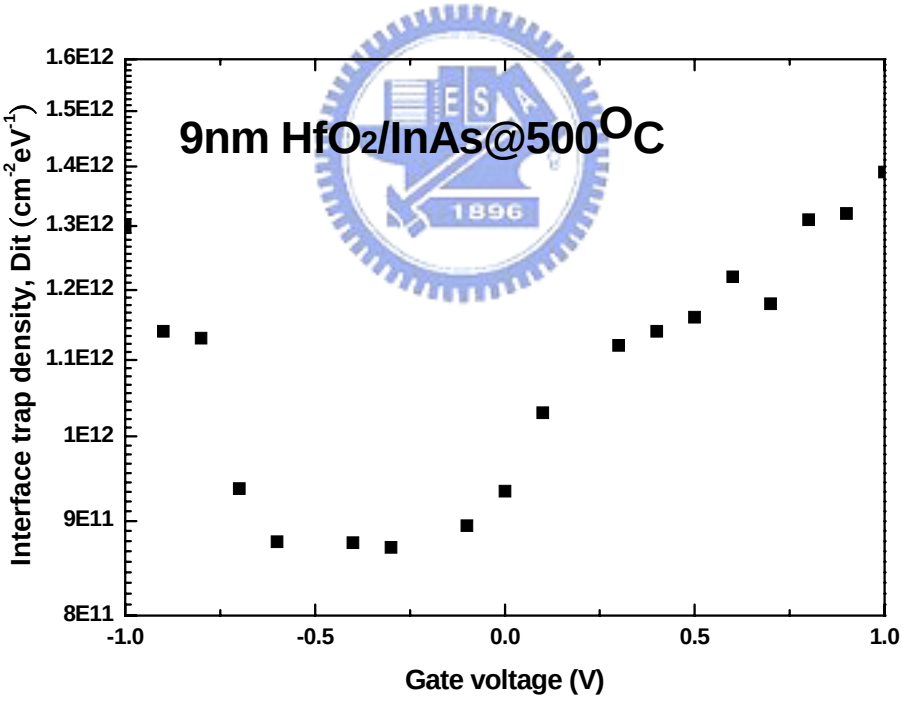
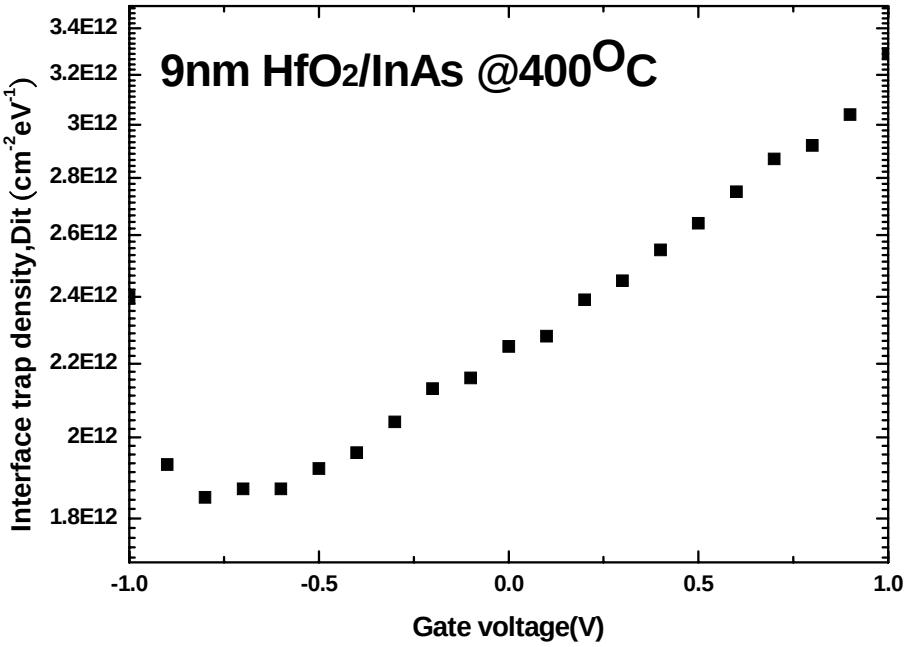


Fig. 5-3 (a)-(b) Equivalent circuits including interface trap effects, C_{it} and R_{it}. (c) Low frequency case. (d) High frequency case. [28]



(a)



(b)

Fig.5-4 Interface trap densities for (a) 500^{O}C (b) 400^{O}C annealed devices

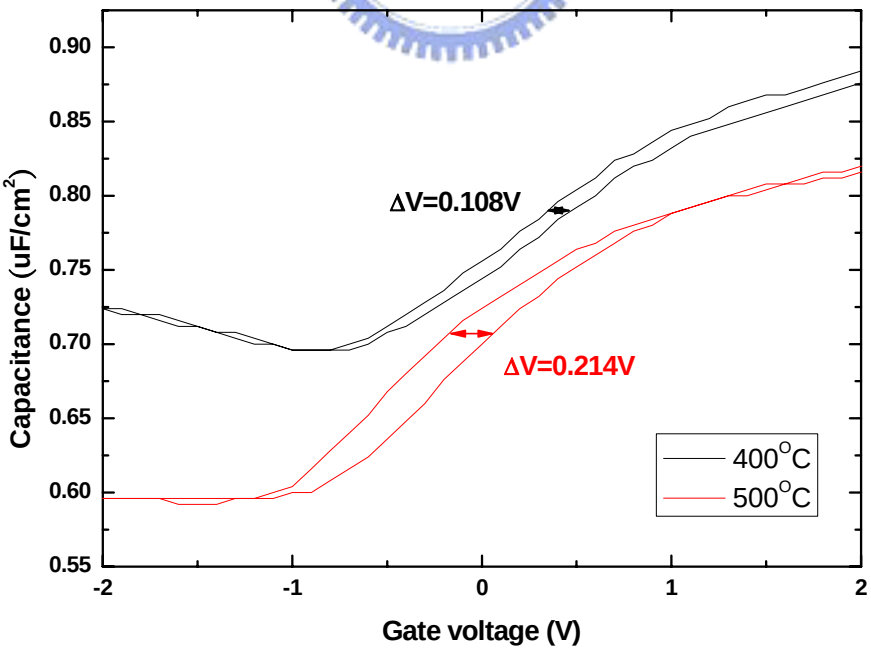
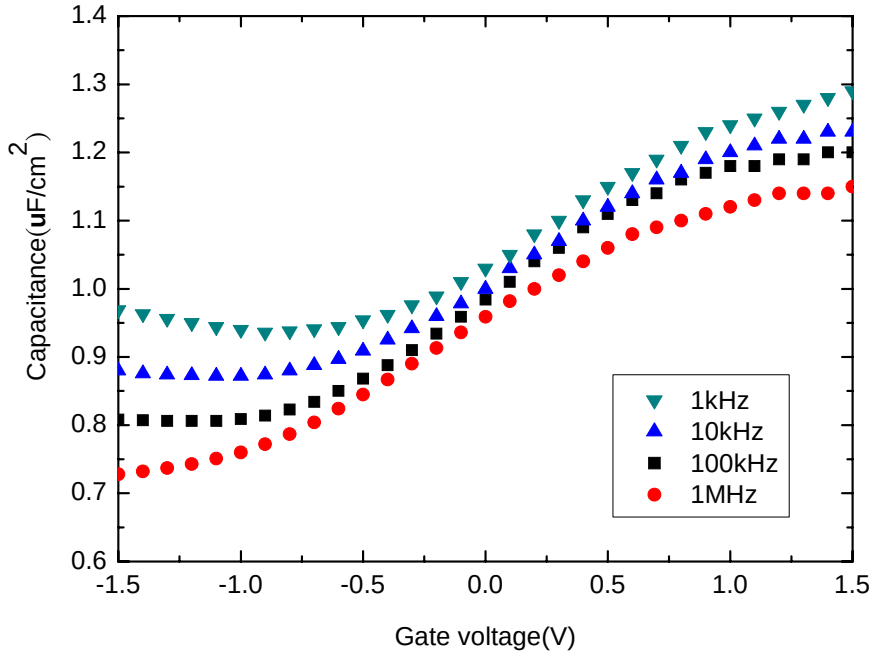
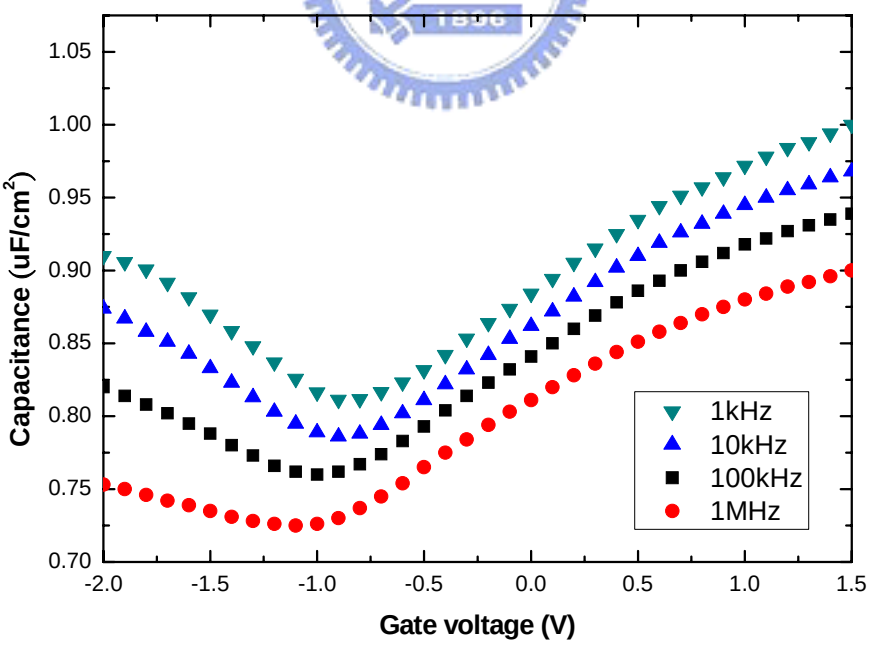


Fig. 5-5 Hysteresis of HfO_2 (9nm)/InAs devices.

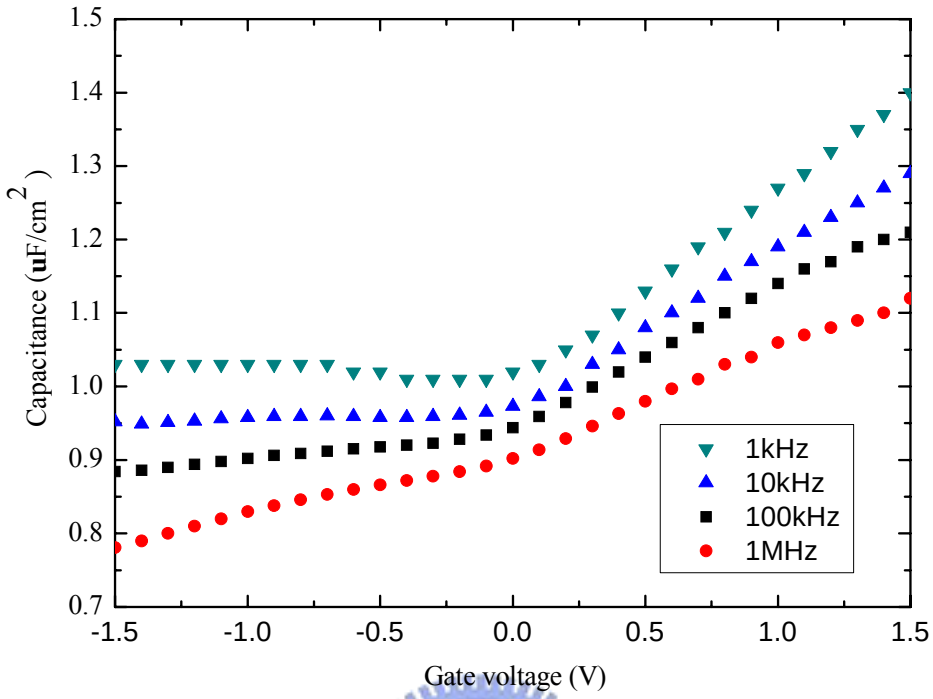


(a)

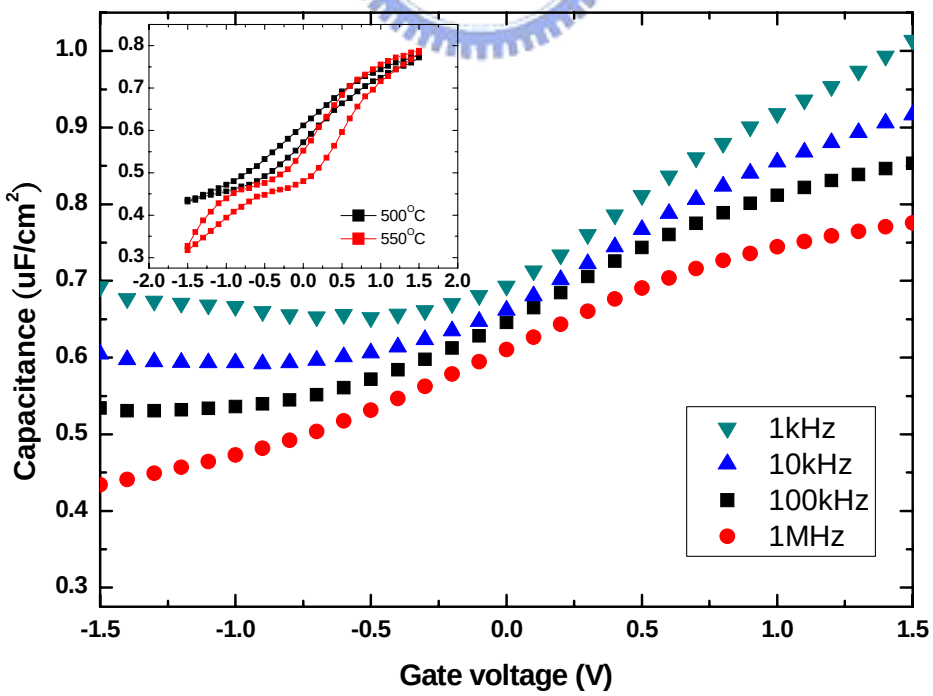


(b)

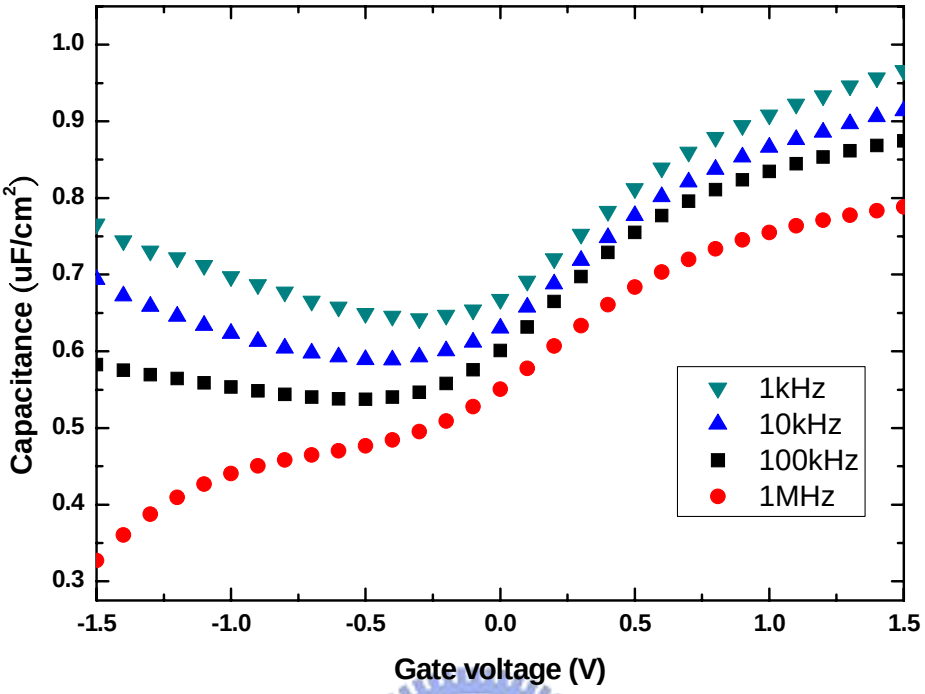
Fig. 5-6 Comparison of C-V characteristics between (a) 9nm Pr_6O_{11} and (b) 9nm HfO_2 on $In_{0.7}Ga_{0.3}As$


Capacitance (uF/cm^2)
Gate voltage (V)
1kHz
10kHz
100kHz
1MHz

(a)


Capacitance (uF/cm^2)
Gate voltage (V)
1kHz
10kHz
100kHz
1MHz
500°C
550°C

(b)



(c)

Fig. 5-7 C-V curves of Pr_6O_{11} (10nm)/$In_{0.53}Ga_{0.47}As$ devices (a) PDA at 450^{O}C. (b) PDA at 500^{O}C (c) PDA at 550 ^{O}C. The hysteresis of 1MHz curves of two samples are shown in the inset figure.

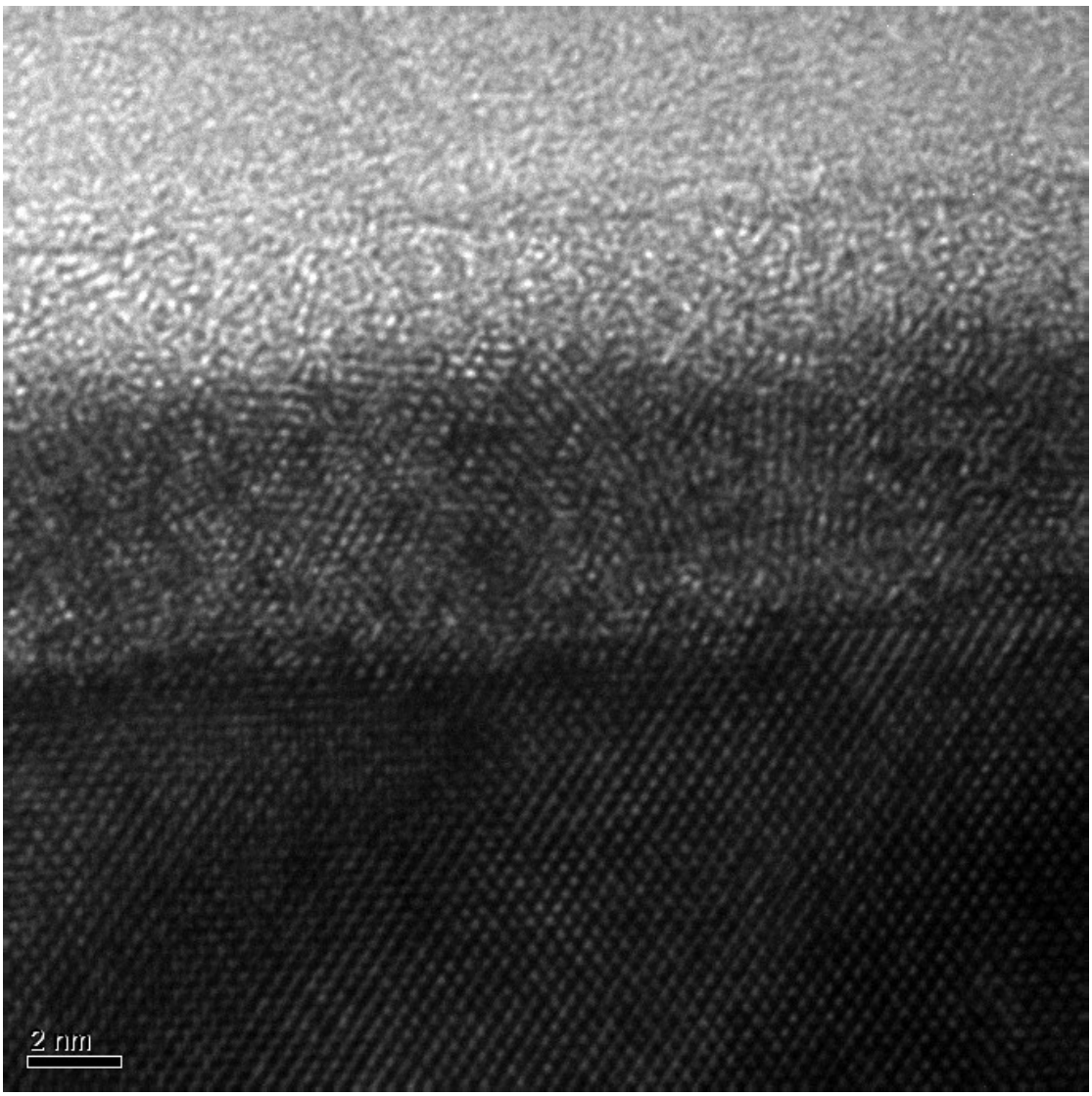
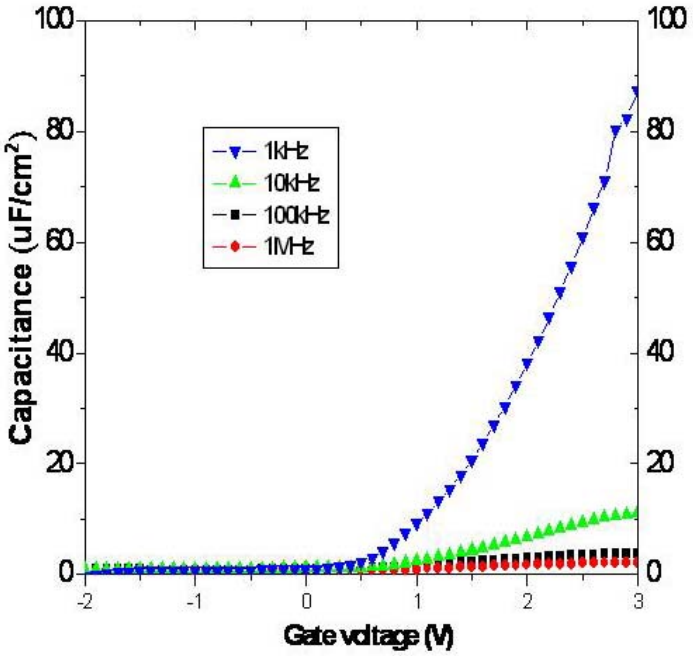
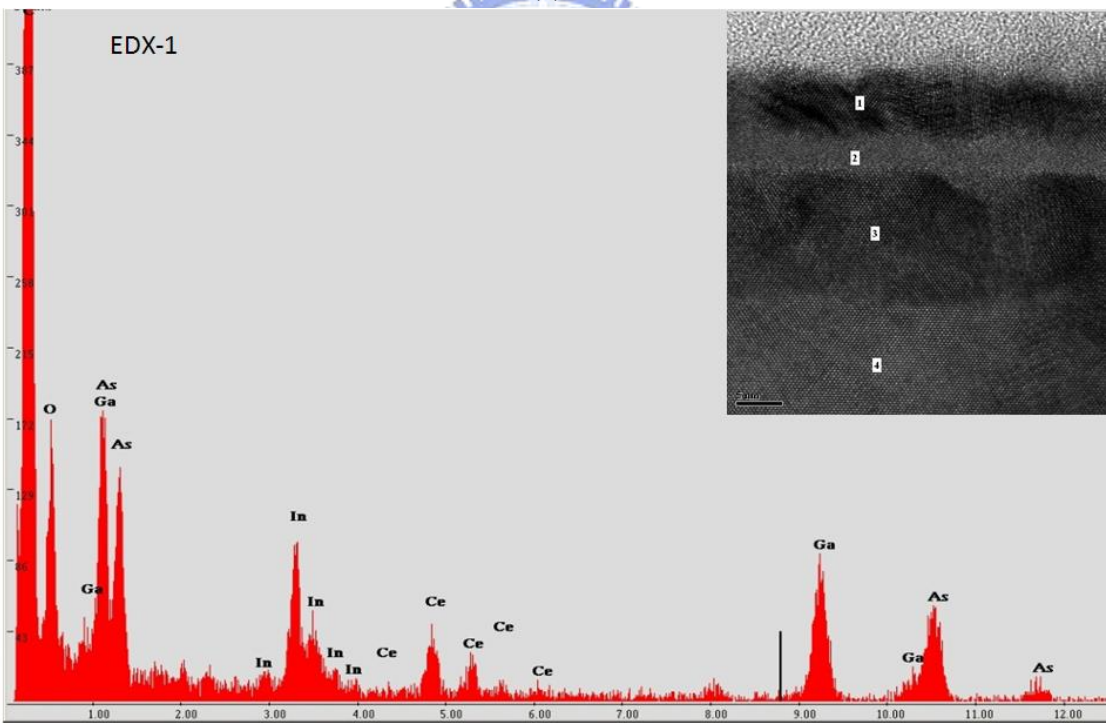


Fig. 5-8 TEM image of 550^{O}C annealed $Pr_6O_{11}/In_{0.53}Ga_{0.47}As$ device



(a)



(b)

Fig. 5-9 (a) C-V curve, (b) TEM image and EDX analysis of CeO_2(9nm)/$In_{0.7}Ga_{0.3}As$ InP device.

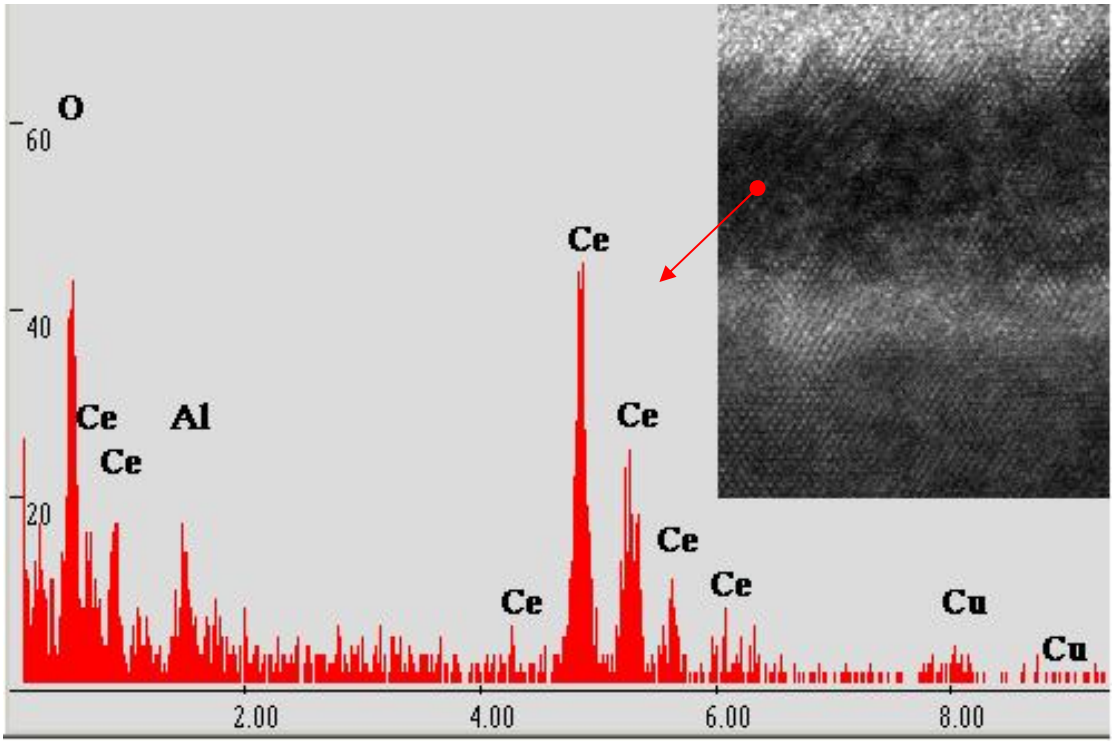
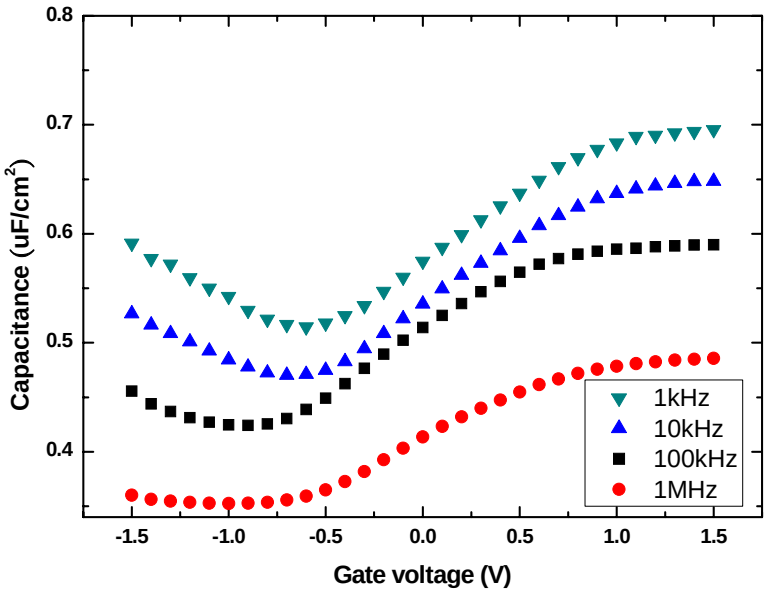
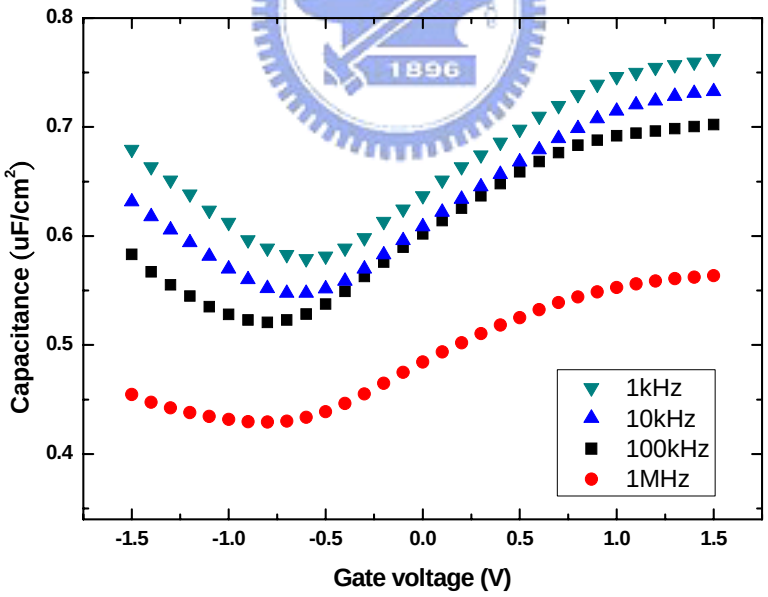


Fig. 5-10 TEM image and EDX analysis of CeO_2(8nm)/Pr_6O_{11}(4nm)/InAs device

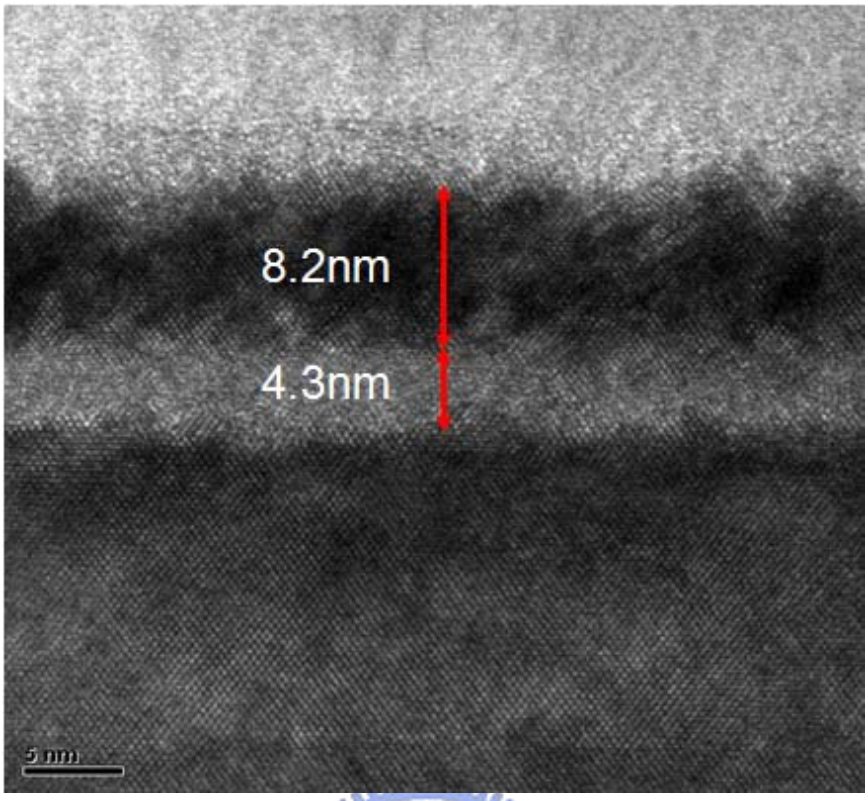


(a)

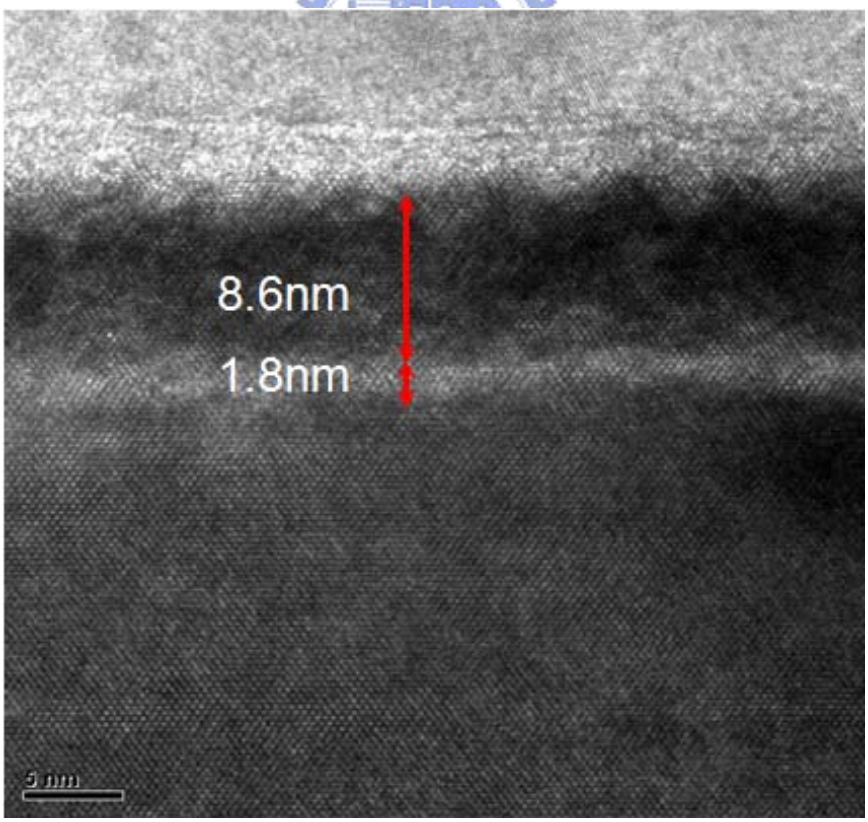


(b)

Fig. 5-11 Comparison of C-V characteristic between (a) one-step annealing process (only Pr_6O_{11} was annealed at 500^{O}C), and (b) two-step annealing process (Pr6O11 was first annealed at 500^{O}C, second step annealing was performed at 400^{O}Cafter CeO_2 deposition) for CeO_2 (8nm)/Pr_6O_{11} (4nm)/InAs devices

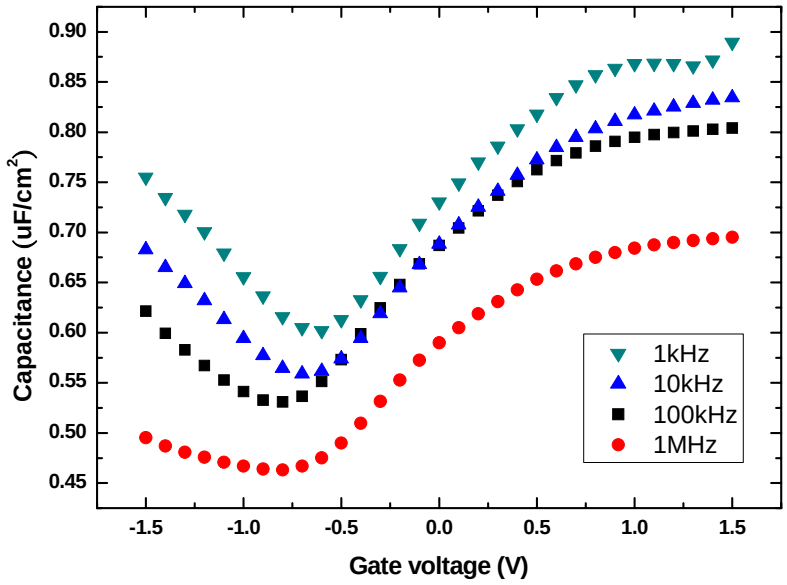


(a)

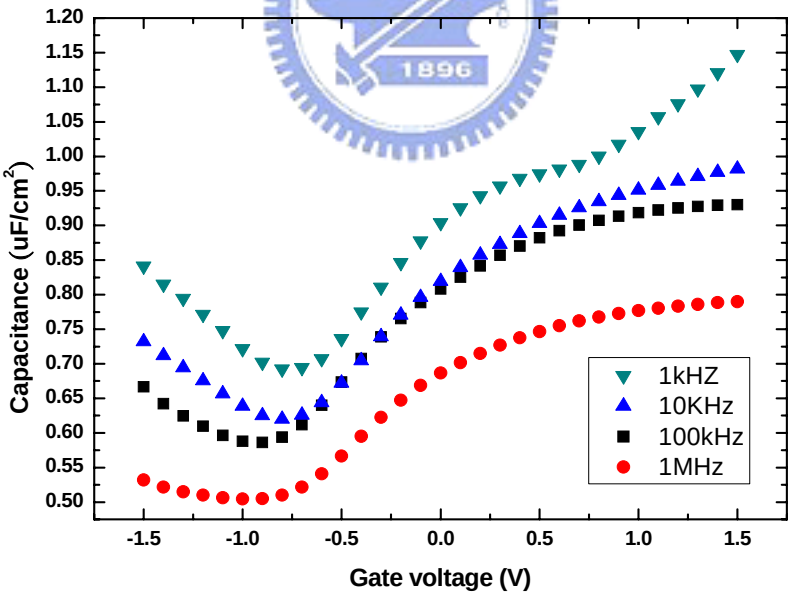


(b)

Fig. 5-12 TEM images of (a) one-step annealed and (b) two-step annealed CeO_2 (8nm)/Pr_6O_{11} (4nm)/InAs devices.

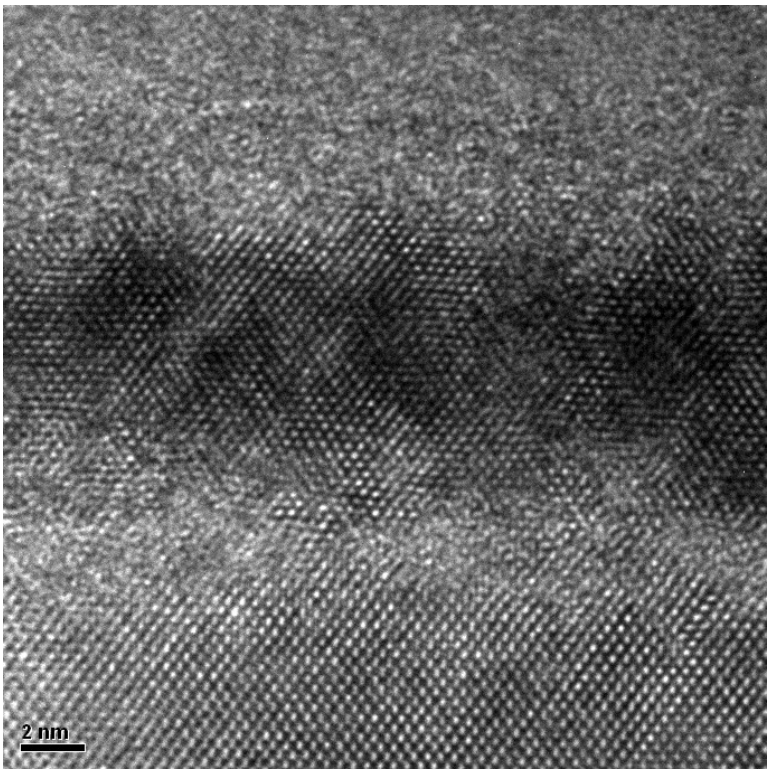


(a)

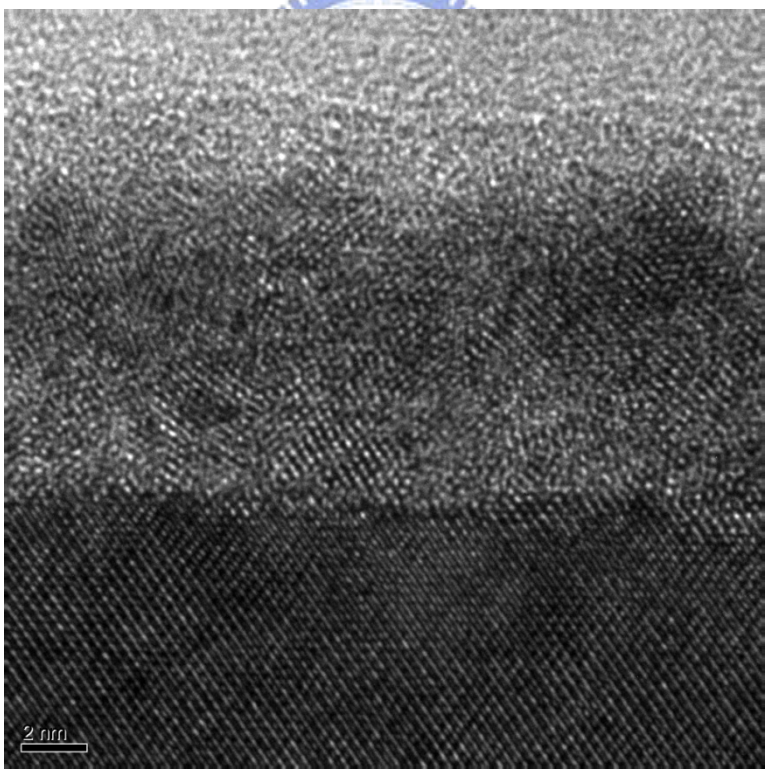


(b)

Fig. 5-13 C-V curves of CeO_2(6nm)/Pr_6O_{11}(4nm)/InAs devices of different annealing temperatures. (a) Pr_6O_{11} was first annealed at 500^{O}C, followed by 400^{O}C annealing after CeO_2 deposition. (b) Pr_6O_{11} was first annealed at 550^{O}C, followed by 400^{O}C annealing after CeO_2 deposition.



(a)



(b)

Fig. 5-14 TEM images of CeO_2(6nm)/Pr_6O_{11}(4nm)/InAs devices first step annealed at (a) 500^{O}C (b) 550^{O}C. And both annealed at 400^{O}C after 6nm CeO_2 deposition. The Pr_6O_{11} beneath the CeO_2 transform from amorphous type to poly-crystalline as the annealing temperature increase

Table 5-1 Extracted equivalent oxide thickness (EOT) from 10kHz curve of CeO_2/Pr_6O_{11}/InAs devices

@10kHZ	Two-step annealed			One-step annealed
Samples*	A	B	C	D
EOT(nm)	3.51	4.14	4.71	5.32

* A: CeO_2 (6nm)/Pr_6O_{11} (4nm)/InAs/$In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$/InP ($Pr_6O_{11}$ first PDA at 550^{O}C, CeO_2 second PDA at 400^{O}C)

B: CeO_2 (6nm)/Pr_6O_{11} (4nm)/InAs/$In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$/InP ($Pr_6O_{11}$ first PDA at 500^{O}C, CeO_2 second PDA at 400^{O}C)

C: CeO_2 (8nm)/Pr_6O_{11} (4nm)/InAs/$In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$/InP ($Pr_6O_{11}$ first PDA at 500^{O}C, CeO_2 second PDA at 400^{O}C)

D: CeO_2 (8nm)/Pr_6O_{11} (4nm)/InAs/$In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$/InP (Only Pr_6O_{11} first PDA at 500^{O}C)

Table 5-2 Extracted equivalent oxide thickness (EOT) from 10kHz curve of HfO_2 (9nm)/InAs devices

@10kHz	PDA at 400^{O}C	PDA at 500^{O}C
EOT(nm)	3.49	3.85

Chapter 6

Conclusion

The HfO_2, Pr_6O_{11} and CeO_2/Pr_6O_{11} were deposited on n-$In_xGa_{1-x}As$ for MOS capacitors studies. $HfO_2/In_{0.53}Ga_{0.47}As$ MOS capacitors showed good scalability with minimum EOT of 2.9nm for 6nm HfO_2 device. The inversion behavior of the devices was also studied. The high frequency inversion behavior was more pronounced for device with high indium concentration, possibly due to the smaller band gap of InAs because it has higher intrinsic carrier concentration and shorter carrier life time, which resulted in short minority carrier response time which makes the carriers follow the small signal and form inversion layer. The PDA temperature for HfO2/InAs devices was also characterized. $400^{O}C$ annealed device showed larger frequency dispersion than $500^{O}C$ annealed device, which was possibly due to the high interface trap density.

Pr_6O_{11} was used to replace HfO_2 to increase the capacitance of the MOS capacitor, the capacitance was increased owing to the high dielectric constant, but the inversion behavior was not apparent due to high interface trap pinning of the Fermi level. High temperature annealing may unpin the Fermi level and form inversion layer, but it also resulted in deep-depletion phenomenon. The deep-depletion phenomenon could be due to more oxide charges were induced during annealing process, which can be examined from the hysteresis performance. Also the poly-crystalline structure provided the current leakage paths. To balance the charge lost due to inversion, depletion region will further expand exceeding its thermal equilibrium width, resulted in deep- depletion phenomenon.

The CeO_2/Pr_6O_{11} gate stack was also applied on InAs. Two step annealing process

was performed to increase the accumulation capacitance. The increase was due to the oxide thickness decrease during second step annealing process after CeO_2 deposition. The thickness of the gate stack was also characterized, CeO_2(6nm)/Pr_6O_{11} gate stack exhibited larger leakage current than 8nm CeO_2 due to the decrease of physical thickness. Device annealed at 550^OC showed more severe current leakage than device annealed 500^OC, which was due to the poly-crystallized gate oxide.

As compared to HfO_2 gated device, the CeO_2/Pr_6O_{11} gate stack structure didn't show the high-k characteristics, which may due to the rough surface and poly-crystallized structure provided the current leakage path which caused the device unable to store charge sufficiently. But since both CeO_2 and Pr_6O_{11} have relatively high dielectric constant, especially for single crystal CeO_2 with dielectric constant of 52, the CeO_2/Pr_6O_{11} gate stack would be the potential high-k stack candidate. As for HfO_2 gated devices, due to its good scalability and thermal stability, and the well pronounced inversion behavior observed in high indium concentration $In_xGa_{1-x}As$, the $HfO_2/In_xGa_{1-x}As$ would be the most potential MOS devices in future CMOS industry.

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