國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

用於管道模式類比對數位轉換器的背景校準技術

Background Calibration Techniques for Pipelined Analog-to-Digital Converters

研 究 生 ：劉鴻志

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中華民國 九十四 年 十 月

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博士論文

A Dissertation

Submitted to Department of Electronics Engineering

College of Electrical Engineering and Computer Science

National Chiao-Tung University

in partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

in

Electronics Engineering

October 2005

Hsin-Chu, Taiwan, Republic of China

中華民國九十四年十月

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摘要

基於 DSP 信號處理設備的迅速增長, 促使了對於一個類比對數位轉換器具有更高的轉換率和更高的解析度的需要. 因為連續的振幅資訊的量子化需要類比模式操作, 類比對數位轉換器限制了 DSP 系統的貫輸量. 管道模式類比對數位轉換器被證明能夠運作在很高速, 但他們的解析度被限制於元件的不匹配, 有限的運算放大器增益,直流補償,電荷注入錯誤和元件的非線性. 自已校準和背景校準技術已被開發用來改正這些非線形性. 數位式自已校準是一個非常有為的技術, 它可以改善基於交換電容器的管道模式類比對數位轉換器的準確性. 數位式自已校準最有吸引力的特點是附加最少的類比電路. 因而, 類比精確度問題被變換成複雜的數位信號處理電路, 允許這種方法受益於 CMOS 元件的縮小技術.

數位式自已校準具有低複雜和高準確性好處, 但多數實施需要管道級的重組, 不可避免地打亂正常類比對數位轉換器的操作. 為了減少這缺點, 數個背景校準技術已被開發使類比對數位轉換器可以連續地校準他們的內部管道級來跟隨環境的變動, 同時執行正常類比對數位的轉換. 背景校準的付出是迅速地越來越少, 因為隨著縮小技術的進步, 所需的數位電路佔據越來越少的面積.

本論文提出一個 15 位元每秒 40 百萬取樣以交換電容器實現的 CMOS 管道模式類比對數位轉換器. 高解析度的達成是應用一個基於相似性的背景校準技術能監

測重要管道級的轉移特性和連續地改正數字輸出代碼. 這個校準可以改正錯誤由於元件不匹配和有限的運算放大器增益. 這個類比對數位轉換器使用 0.25 微米 1P5M CMOS 的技術製造. 操作在每秒 40 百萬的採樣率時, 這個類比對數位轉換器達成最大 SNDR 的值是 73.5 dB, 最大 SFDR 的值是 93.3 dB. 晶片面積是 3.8×3.6 mm^2, 並且操作於 2.5 伏特的電力消耗是 370 mW.

Background Calibration Techniques for Pipelined Analog-to-Digital Converters

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Abstract

The rapid growth of DSP-based signal processing equipments prompted a need for a analog-to-digital converter (ADC) with higher conversion rates and higher resolutions. Since quantization of continuous amplitude information requires analog operations, ADCs often limit the throughput of DSP based systems. Pipelined ADCs have been shown to work at very high speeds but their resolution is limited by component mismatches, operational amplifier (opamp) finite gain, offsets, charge injection errors and component non-linearity. Self calibration and background calibration techniques have been developed to correct for these non-linearities. Digital self-calibration is a very promising technique to improve the accuracy of switched capacitor based pipeline ADCs. The most attractive feature of digital self-calibration is the minimum extra analog circuit involved. Thus, analog precision problems are translated into the complexity of digital signal processing circuits, allowing this approach to benefit from CMOS device scaling.

Digital self-calibration has the advantage of low complexity and high accuracy, most implementations need reconfiguration of the pipeline stages, which inevitably disrupt the normal A/D operation. To diminish this deficiency, several background calibration schemes have been developed to enable ADCs to continuously calibrate their internal pipeline stages to track environmental changes while simultaneously performing the normal A/D conversions. The cost of background calibration is decreasing rapidly because the required digital circuits occupy less and less area in scaled technologies.

This thesis presents a 15-b 40 MS/s switched-capacitor CMOS pipelined ADC. High resolution is achieved by using a correlation-based background calibration technique that can continuously monitor the transfer characteristics of the critical pipeline stages and correct the digital output codes accordingly. The calibration can correct errors associated with capacitor mismatches and finite opamp gains. The ADC was fabricated using a 0.25 μm 1P5M CMOS technology. Operating at a 40 MS/s sampling rate, the ADC attains a maximum signal-to-noise-plus-distortion ratio (SNDR) of 73.5 dB and a maximum spurious-free-dynamic-range (SFDR) of 93.3 dB. The chip occupies an area of 3.8×3.6 mm^2, and the power consumption is 370 mW with a single 2.5 V supply.

Acknowledgements

First, I would like to thank my advisor Prof. Jieh-Tsorng Wu for his support and guidance in my research. Whenever I encounter the difficulties or problems, he is always patient to give me the direction and encouragement.

I wish to thank my classmates, Miss Zwei-Mei Lee for C model buildup and simulation and chip layout. I also thank Mr. Ju-Ming Chou, Mr. Chang-Tsung Fu, and Mr. Chi-Wei Fan for their support. The authors would like to thank Ting-Hao Wang, Jane Lu, and Ruei-Shiuan Tzeng of the Silicon Integrated System Corp. for engineering support, and Cheng-Yeh Wang of the National Chiao-Tung University for valuable technical discussions. The authors also thank the National Chip Implementation Center for chip fabrication. Without their help, this project would never be done well.

Finally, I would like to express my greatest appreciation to my wife, Miss Judith Cheng, my children, and other members of my family for their unconditional support and encouragement.

HUNG-CHIH LIU

National Chiao-Tung University
2005, October

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

With the continuing exponential advances of integrated circuit process technology, the number of transistors per square millimeter of silicon doubles every 18 months. At the same time transistors have become more and more faster, making possible ever-increasing clock rates and the implementations of highly sophisticated architectures and algorithms in digital circuits. This trend will set to continue for at least another decade without slowing down.

However, the use of modern sub-micron CMOS transistor in analog circuits design is not too much beneficial. Two major limitations on analog components are reduced power-supply voltages and high output conductance that make the design of high linear, high dynamic range analog building blocks an increasingly challenging task. Thus, more and more analog functions are being implemented with digital signal processing techniques. Digital signal processing (DSP) has been proved over the past decade to be a robust and cost effective way of signal processing. Fig. 1.1 shows the basic topology of a DSP-based system. A programmable-gain amplifier (PGA) is usually placed in front of the ADC, adapting the loss variation of the signal transmission path in order to ease the dynamic range requirement for the ADC. Thus, PGA usually determines the overall linearity of the system. The interface between the real world analog signal and DSP function block is implemented by an analog-to-digital converter (ADC).

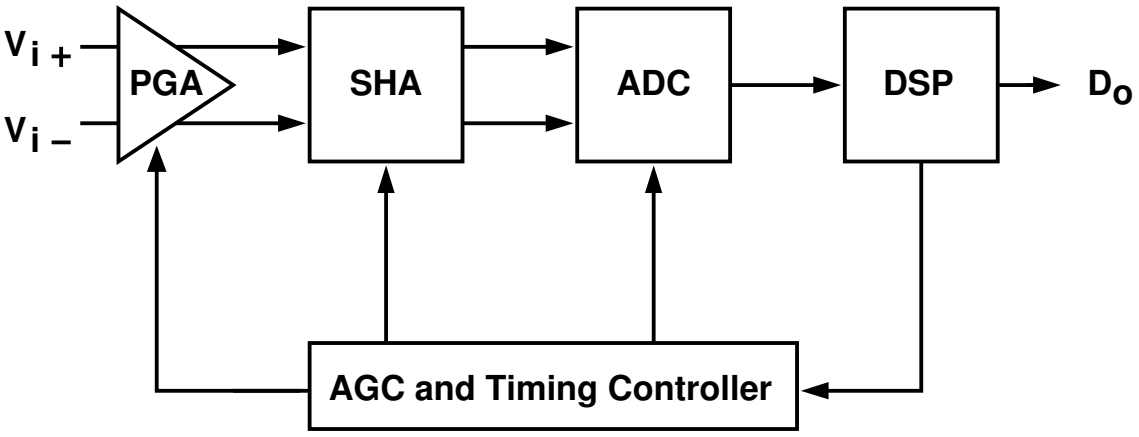

Figure 1.1: Block diagram of a DSP-based system.

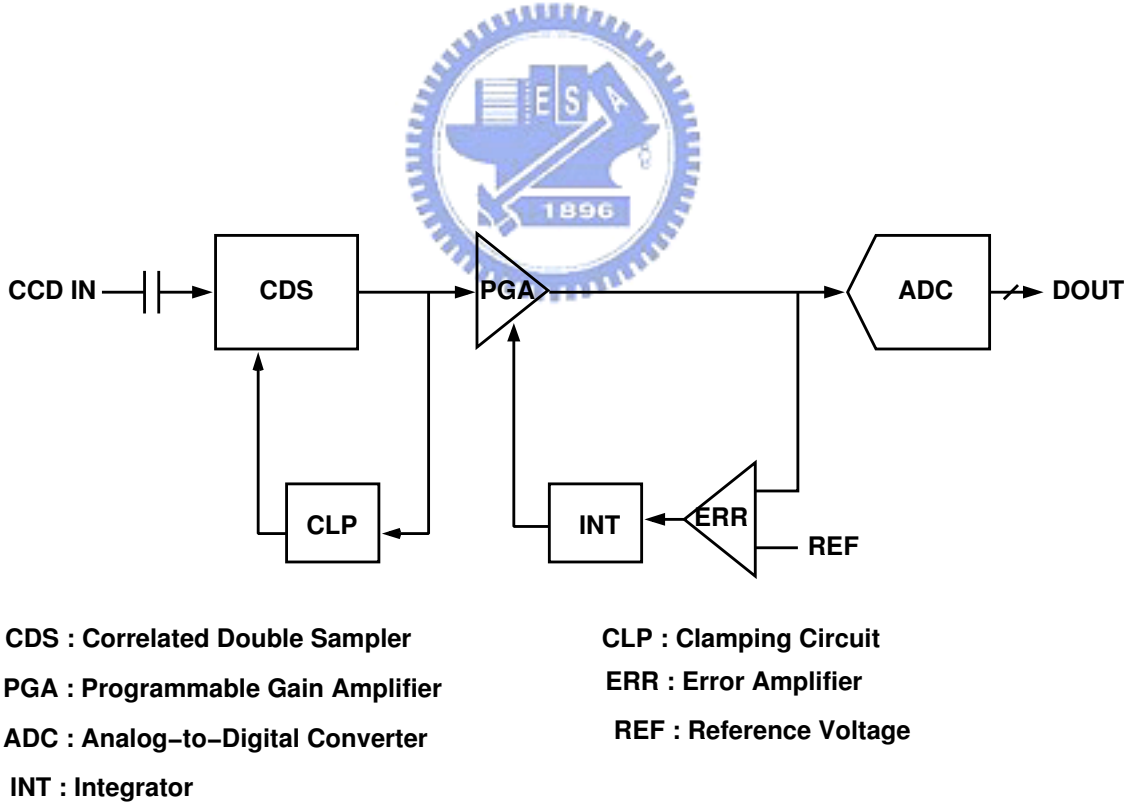

Figure 1.2: Conventional CCD front-end scheme.

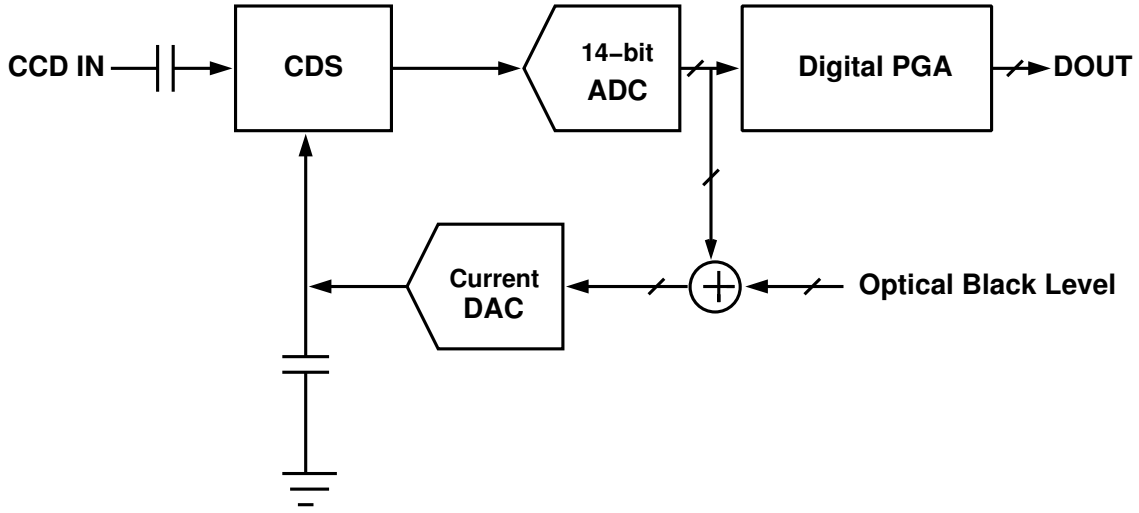

Figure 1.3: New CCD front-end scheme.

For example, in portable digital imaging equipment such as camcorders and digital still cameras, there is a strong need for low-noise, low-power, and robust CCD front-ends. Conventional front-ends shown in Fig. 1.2 usually utilize a complex analog programmable gain amplifier which realizes a gain curve linear in dB as a function of the gain code in front of a 10-bit ADC and thus most signal conditions necessary for the CCD systems were performed in the analog domain. The analog PGA consumes substantial power, adds more noise, has difficulty in realizing high gain and has an inherent non-linearity problem of gain curve. A new CCD front-end scheme shown in Fig. 1.3 utilizes all digital PGA to solves above problems associated with the analog PGA and realizes much better performance [2]. However, A high resolution of the ADC is inevitably required to compensate for the lost information associated with the digital amplification by the digital PGA. Another examples of applications are broadband communication transceivers such as Gigabit Ethernet, Cable Modems, ADSL,...etc. The feasibility of ADSL systems depends highly on the feasibility of both D/A and A/D converters of its analog front-end (AFE) since typical specifications require very high resolutions (13-16 bits) for input signal bandwidths up to 1.104 MHz.

From the discussions above, the rapid growth of DSP-based signal processing equipments prompted a need for a ADC with higher conversion rates and higher resolutions. Since quantization of continuous amplitude information requires analog operations, ADCs

often limit the throughput of DSP based systems. The Pipelined architecture offers a good trade-off among power, sampling rate and chip area for Nyquist-rate ADC when compared to flash ADC, subrange ADC and successive approximation ADC. While the speed of pipelined ADCs has exceeded 100 mega-samples per second (MSPS) in CMOS technology [3] [4] [5] [6] [7], the commonly achieved resolution is still bound within the range of 8-12 effective number of bits (ENOBs) due to a variety of issues that arise. For instance, a switched-capacitor (SC) implementation is sensitive to mismatch in the capacitors that set the digital-to-analog converter (DAC) levels and interstage gain, variations in the finite gain of the operational amplifier (opamp), the accuracy of the reference voltage, and charge injection from switches. While several of these effects can be minimized by special design techniques and careful layout, but some are difficult to circumvent. Most pipelined ADCs with more than 12-bit resolution will usually require some kind of linearity enhancement techniques.

Trimming or calibration are traditionally used to overcome this problem. Trimming has the advantage of being transparent to the user, but it cannot track variations over time caused by component aging and temperature changes. Self-calibration schemes exist that can alleviate this limitation. Although the calibration can be accomplished in the analog domain [8], fully digital approaches are preferred in deep sub-micron technologies owing to the lower cost of the added digital circuitry [9] [10] [11] [12] [13] [14] [15].

While digital self-calibration has the advantage of low complexity and high accuracy, most implementations need reconfiguration of the pipeline stages, which inevitably disrupt the normal A/D operation. Thus, in applications that cannot afford idle time, the ADCs can only be calibrated in the power-on state. This power-on calibration may become insufficient for high-resolution ADCs, whose accuracy requirement for the interstage gain cannot tolerate significant variation in opamp's dc gain. Furthermore, the opamp's dc gain is hard to maintain against supply-voltage and temperature variation.

To diminish this deficiency, several background calibration schemes have been developed to enable ADCs to continuously calibrate their internal pipeline stages to track environmental changes while simultaneously performing the normal A/D conversions. The cost of background calibration is decreasing rapidly because the required digital circuits occupy less and less area in scaled technologies.

In this thesis, we employ a robust background calibration scheme to correct the static A/D conversion errors [16] [17] [18]. Random analog signals are sequentially injected into the critical pipeline stages through the split capacitors for measuring the stages's transfer characteristics. All static errors due to component mismatches and finite opamp gains are corrected in the digital domain. This calibration scheme requires only slight modifications to the standard pipeline stages. No additional high-resolution ADC is needed. For the critical analog signal path, no extra capacitive loading is added, thus its operating speed is not degraded. This calibration scheme is also robust since its effectiveness does not rely on the input's amplitude distribution. The measurement results of this 15-bit 40-MS/s ADC chip fabricated in a 0.25-μm CMOS technology demonstrate the feasibility of this calibration scheme.

1.2 Organization

The organization of the thesis is as follows:

Chapter 2 gives a overview of the pipelined A/D architecture. Error sources in single pipeline stage are discussed. A generalized mathematical approach is introduced to analyze pipeline ADC. The theory of redundancy and digital correction is also addressed. Several SC implementations of pipeline stage are studied. In Chapter 3, a pipelined ADC architecture is presented and its limitations are studied. several existing calibration schemes are reviewed. The proposed background calibration scheme is introduced and shows how the static errors due to component mismatches can be overcome. Chapter 4 describes the design of the ADC prototype. The key components such as the sample-and-hold circuit, opamps, the comparator and calibration blocks are described. An experimental prototype ADC has been fabricated, and its measurement results are presented along with discussion on key performances. Finally, chapter 5 draws conclusions and makes recommendations for future work.

Chapter 2

Principles of Pipelined ADCs

2.1 Introduction

Fig. 2.1 shows the common topology of a pipelined ADC, which consists of a cascade of P stages. Each pipeline stage needs not be identical. Fig. 2.2 gives a basic configuration which comprises an sample-and-hold amplifier (SHA), a low resolution coarse ADC (sub-ADC), a DAC (sub-DAC), and a subtracter. In operation, each stage initially samples and holds the output from the previous stage and the held input is then converted into a low resolution digital code by the sub-ADC and back into an analog representation by the sub-DAC. Finally, the SHA amplifies the difference between the held analog signal and the reconstructed analog representation to give the residue for the next stag.

The primary advantage of pipelined ADCs is that they provide high throughput rates and occupy small die areas. Both advantages stem from the use of S/H technique which

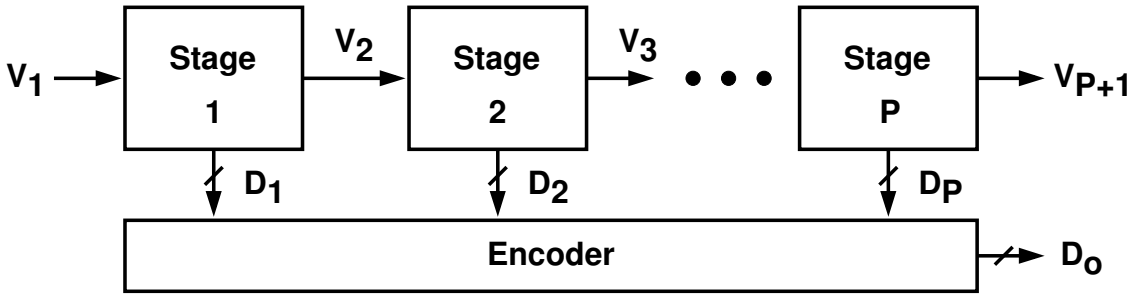

Figure 2.1: A pipelined ADC.

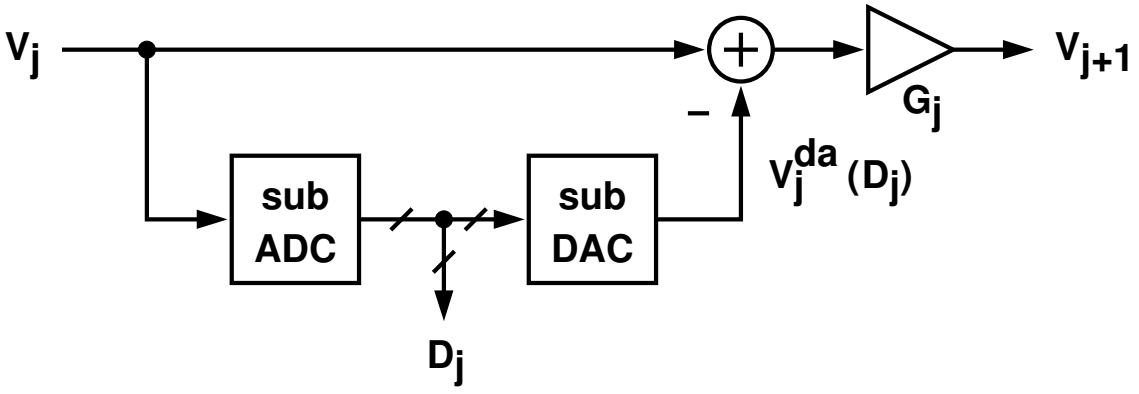

Figure 2.2: Block diagram of a pipeline stage.

allows each of the stages to operate concurrently; that is, at any time, the first stage operates on the most recent sample while all other stages operate on residues from previous samples. If the sub-ADCs are realized with flash converters, pipelined architectures require only two main clock phases per conversion. Hence the maximum throughput rate can be quite high. In additional, since all stages operate concurrently, the number of stages used to obtain a given resolution is not constrained by the required throughput rate. The speed of a pipelined ADC is limited only by the settling of the interstage SHA.

The sections in chapter 2 are arranged as follows: Section 2.2 describes the generalized mathematical description which is applied to characterize the transfer function of multistage ADC. Section 2.3 gives the definition of minimal base-2 converter. Section 2.4 presents the error sources of the pipeline stage. Section 2.5 shows how to translate the minimal pipeline stage into the redundant stage and how the digital error correction works. Section 2.6 introduces the application of generalized mathematical description on three pipelined ADC examples with different redundant schemes. The CMOS circuit implementations of the pipeline stages are shown in Section 2.7. Finally, the summary is drawn in Section 2.8.

2.2 Generalized Mathematical Description

To develop a generalized view of multistage A/D conversion, a single stage is taken into concern first. The input signal is assumed to be bipolar, while analysis in a unipolar case

could be readily derived from the bipolar result. Besides, it is always possible to view a unipolar signal as a bipolar one centered around the mid-scale reference level.

Let V_1 be the bipolar input signal to the stage and V_r be the system reference level. To simplify the analysis, it is sometimes more convenient to work with a normalized input V_{1n} defined as

$$V_{1n} = \frac{V_1}{V_r} \tag{2.1}$$

where

$$-1 \leq V_{1n} \leq 1 \tag{2.2}$$

Fig. 2.2 shows a converter stage, here dubbed the j-th stage. The analog input V_j is compared with a number of reference levels, V_j^{ref}, using a sub-ADC, which consists of a comparator string and a voltage divider that operates off the main reference. The comparator outputs provide a rough digital representation, called D_j, of the input voltage in thermometer format. A flash section with M comparators generates $M + 1$ possible codes. The sub-ADC is followed by a reconstructing sub-DAC. Depending on the value of D_j, its output can be one of $M + 1$ possible voltages, $V_j^{\mathrm{da}}(D_j)$, which is then subtracted from the input signal.

The difference signal $(V_j - V_j^{\mathrm{da}}(D_j))$ is then amplified by a SHA. The amplifier with a gain of G_j amplifies the difference signal to a level compatible with the input range of the following stage. The resultant signal is called the residue and noted as V_{j+1}. G_j can assume any value greater than 1, positive or negative. It is possible that there is an input-referred offset which cannot be distinguished from the variation of the $V_j^{\mathrm{da}}(D_j)$'s. The S/H action allows for several stages to be cascaded in a pipelined fashion. Cascading more stages yields a higher resolution.

Refer back to Fig. 2.1 where there are P nominally identical stages, numbered from P (last, or least significant stage) to 1 (input, or most significant stage). For each stage (designated by its number, j, in subscript), the digital code D_j can be expressed as a function of the input voltage V_j. The $M + 1$ possible digital words for D_j are hereby

designated as integers: 0 (for 00...0), 1 (for 10...0) $\cdots$ through M (for 11...1) [12].

$$D_j = \begin{cases} 0 & \text{for} \quad V_j < V_j^{ref}[0] \\ 1 & \text{for} \quad V_j^{ref}[0] \leqslant V_j < V_j^{ref}[1] \\ & \cdots \\ M & \text{for} \quad V_j^{ref}[M-1] < V_j \end{cases} \tag{2.3}$$

For any given D_j, a general equation can be derived for the residue V_{j+1} as a function of V_j.

$$V_{j+1} = G_j \times \left[V_j - V_j^{\text{da}}(D_j)\right] \tag{2.4}$$

Inverting (2.4) gives the input V_j as a function of output V_{j+1}:

$$V_j = V_j^{\text{da}}(D_j) + \frac{V_{j+1}}{G_j} \tag{2.5}$$

The expression for the input voltage of stage j can then be expanded to

$$V_j = V_j^{\text{da}}(D_j) + \frac{V_{j-1}^{\text{da}}(D_{j-1})}{G_j} + \frac{V_{j-1}}{G_j G_{j-1}} \tag{2.6}$$

Further expanding the expression and evaluating it for $j = 1$ gives the input voltage V_1 of the pipelined converter with P stages as [19]:

$$V_1 = V_1^{\text{da}} + \frac{V_2^{\text{da}}}{G_1} + \frac{V_3^{\text{da}}}{G_1 G_2} + \cdots + \frac{V_P^{\text{da}}}{G_1 G_2 \ldots G_{P-1}} + Q \tag{2.7}$$

where $Q = V_{P+1}/(G_1 G_2 \ldots G_P)$ represents the quantization error of the entire A/D conversion. This general equation is based on the assumptions that the basic linear input-output relationship holds for each stage. In order for this to be true, there must be no over-ranging at any point in the multistage ADC system.

The ADC's digital output, D_o, is calculated from D_j, for $j = 1, \cdots, P$, by applying (2.7) and letting $D_o = V_1 - Q$. Both V_j^{da} and G_j, for $j = 1, \cdots, P$, are design parameters available to the designer. The first P terms of (2.7) are the ones of use while the last term is neglected. Representing the inherent quantization error, this last term originates from the fact that the analog residue of the last stage is not converted, unlike its siblings in previous stages. It decreases drastically as the number of converter stages (P) or the gain of the interstage amplifiers G_j increase.

The same reasoning applies to cyclic converters as well, in which the residue from a single stage is fed back to that same stage for successive conversions. Algorithmically, there is no difference between such arrangement and a pipeline one. (2.7) applies to both equally, as long as the stage subscript j is interpreted as the designation of a sample in time rather than a stage in a spatial arrangement.

2.3 Minimal Base-2 Converter

The ADC's digital output D_o is most easily obtained from the D_j when the stages are designed for what we call "minimal" (as opposed to "redundant") operation [12]. The procedure is further simplified when the converter is based on a radix of 2, i.e., when the gain of all interstage amplifiers is exactly a power of 2. Many multi-stage converter designs are of the minimal base-2 type.

A minimal design is characterized by an integer nominal gain value G_j and reference levels V_j^{ref} chosen so as to divide the input range (assumed to be normalized between -1 and 1) in as many equal parts as the absolute value of the gain, G_j. Hence, the number of comparators, M, is $|G_j| - 1$. The V_j^{ref} are integer multiples of a fixed voltage increment, $\Delta V = 2/|G_j|$, so that $V_j^{ref}(D_j) = -1 + (D_j + 1)\Delta V = -1 + (D_j + 1)2/|G_j|$, for $0 \le D_j < M$.

The number of sub-DAC levels $V_j^{\mathrm{da}}(D_j)$ is equal to G. the $V_j^{\mathrm{da}}(D_j)$'s of each stage are also integer multiples of $\Delta V = 2/|G_j|$. For positive and negative G the $V_j^{\mathrm{da}}(D_j)$ are given by $V_j^{\mathrm{da}}(D_j) = -1 + (D_j + 1/2)\Delta V = -1 + (D_j + 1/2)2/|G_j|$ for $0 \le D_j \le M = G_j - 1$.

Fig. 2.3 demonstrates three minimal designs for stages with nominal gain of 2, 3 and 4, respectively. It also shows the transfer function of each stage, i.e., the relationship between V_j and V_{j+1}. Assuming ideal components, the transfer function of each stage exhibits a regular saw-tooth behavior. As long as the input signal to a stage is within the nominal input range, $-1, \cdots, 1$, its residue is guaranteed to be within the same range. Since all stages are equal, the residue will fit the input range of the next stage. The last residue will be limited to $-1, \cdots, 1$, and the resultant quantization error, Q, will be limited

$$0 \le Q \le \frac{2}{G_1 G_2 \ldots G_P} \approx \frac{2}{|G^P|} \tag{2.8}$$

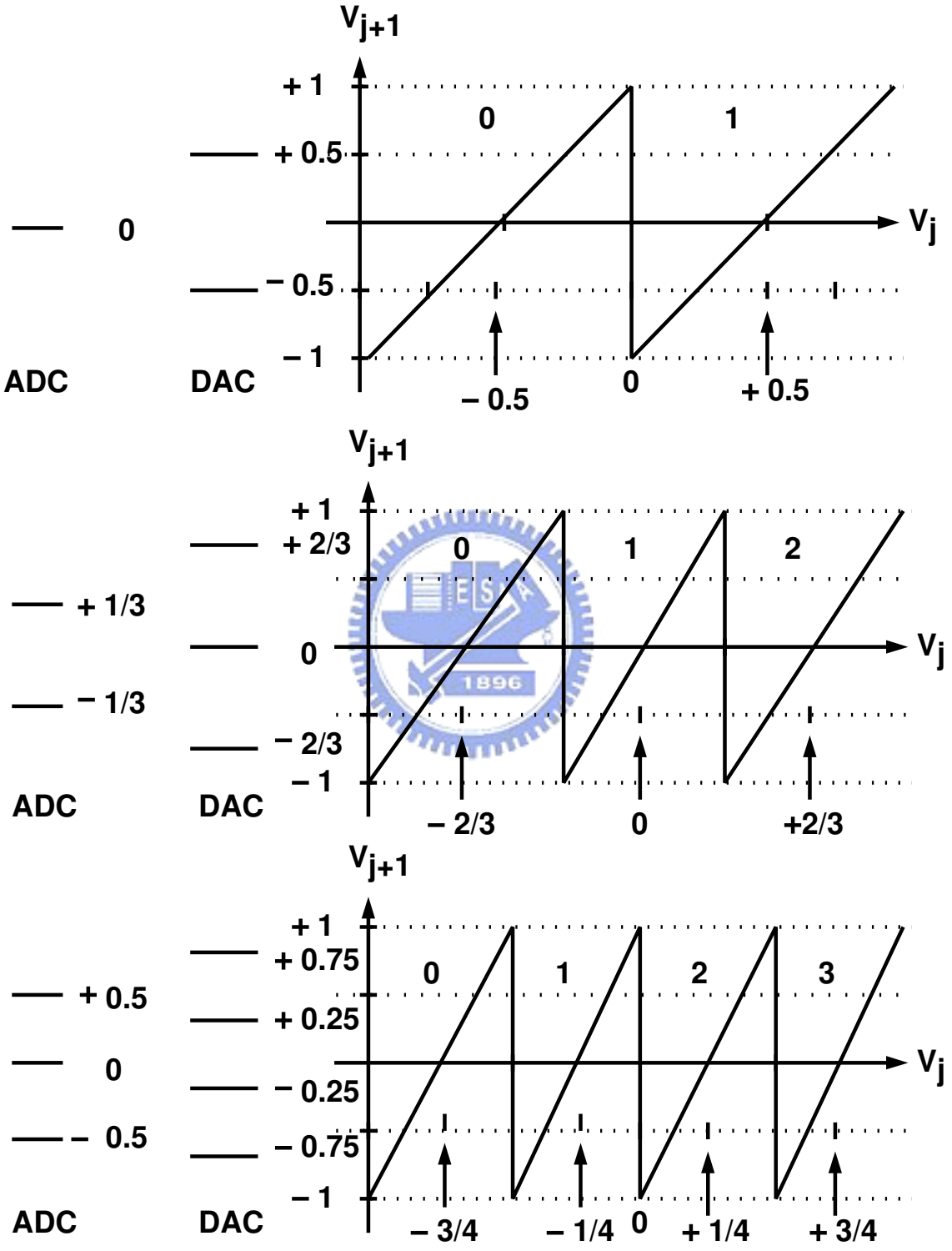

Figure 2.3: Minimal Design.

Q represents the inherent uncertainty on the conversion result and G is the nominal gain. In a classic, ideal N-bit converter, the corresponding quantization error range would be $2/2^N$, which is also defined as 1 LSB (for "least significant bit"). By extension, we are denning 1 LSB as follows:

$$1\text{LSB} = \frac{2}{|G|^P} \tag{2.9}$$

Similarly, the relationship between the input range and the range of the quantization error (1 LSB) can be expressed as the effective number of bits, N_{eff}.

$$N_{eff} = \log_2(\frac{2}{1\text{LSB}}) = P\log_2(|G|) \tag{2.10}$$

The effective number of bits per stage, n_{eff} is given by:

$$n_{eff} = \log_2(|G|) \tag{2.11}$$

For a minimal base-2 converter, $G = 2^n$. (Note that $n_{eff} = n$.) It is easy to derive the binary conversion result – simply convert the D_j of successive stages from M-bit thermometer code to n-bit straight binary, and combine the P individual n-bit words into an N-bit (with $N = nP$) conversion result through concatenation. Furthermore, $0 \leq Q \leq 2/2^{nP} = 2/2^N$=1 LSB. This expression is consistent with the conventional definition of an N-bit converter

2.4 Error Sources in a Pipelined Stage

The performance of a pipelined ADC is limited by the nonlinearity of the sub-ADC and sub- DAC, as well as the gain error of the interstage SHA. The nonlinearity in the sub-ADC is due to comparator offsets and reference voltage errors. Both errors lead to a decision-level shift of the sub-ADC. The non-ideal effects in the sub-DAC include offset, gain error, and nonlinearity. Gain error in the interstage SHA stems from by a variety of sources. In a pipeline using switched capacitor gain stages, these error sources could include capacitor mismatches and finite opamp gains. In this section, we will discuss these sources and derive interpretations for them [20] [21].

The flash ADC in each pipelined stage compares the stage input to a set of reference voltages and output the resultant digital code. Unless otherwise stated, it is assumed

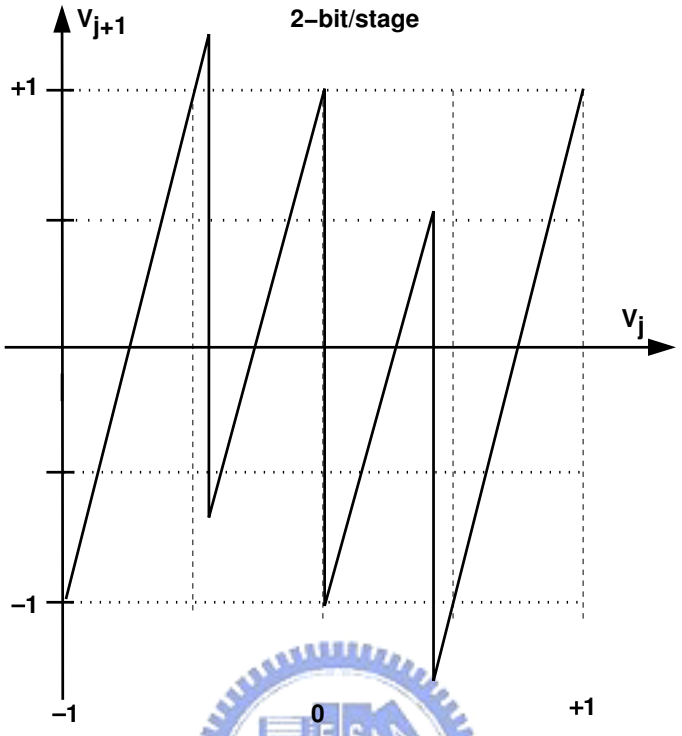

Figure 2.4: Transfer curve of a pipelined stage with threshold offsets.

that the sub-DAC and gain block in the stage are ideal. The comparator tries to find out the difference of between the two input signals whilst an internal offset voltage factors into this difference. Thus when the two inputs are close to each other, the comparator may make a wrong decision and a wrong reference is subtracted from the input. The aforementioned internal offsets are due to comparator offsets and reference voltage errors. Both errors result in a decision level shift(or threshold offset) of the sub-ADC. For the 2-bit/stage case, the effect of this decision-level shift on the residue transfer is shown in Fig. 2.4. As can be seen, the residue voltage can be larger than the input range of the following stage, resulting in the saturation of the next stage. As a result, missing decision level occurs.

After the input is digitized by the sub-ADC, a sub-DAC converts the derived code back to an analog signal. It can be shown that the offset of the sub-DAC gives rise only to a constant equivalent input offset of the ADC. On the other hand, the gain error and the nonlinearity in the sub-DAC limit the resolution of the whole ADC. The sub-DAC gain error has the same effect on performance as the interstage SHA gain error. The nonlin-

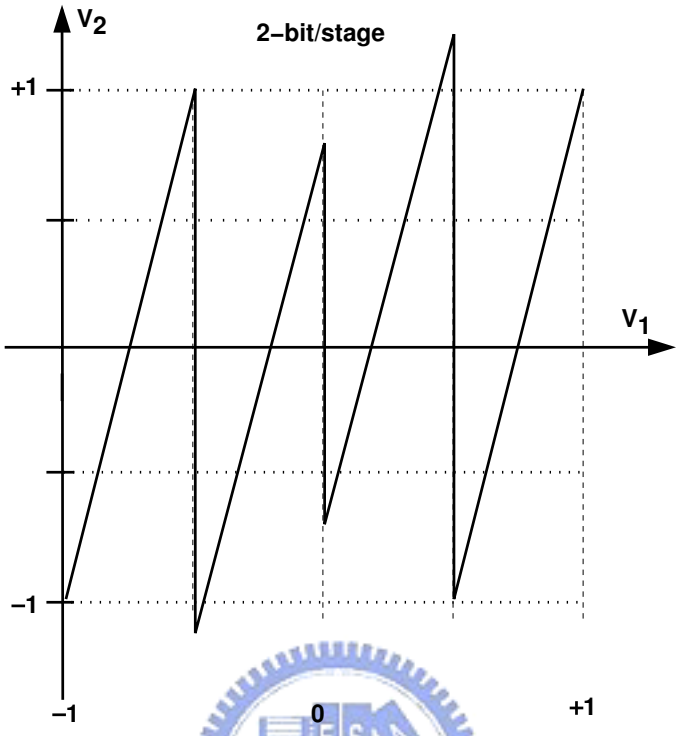

Figure 2.5: Transfer curve of a pipelined stage with non-ideal DAC references.

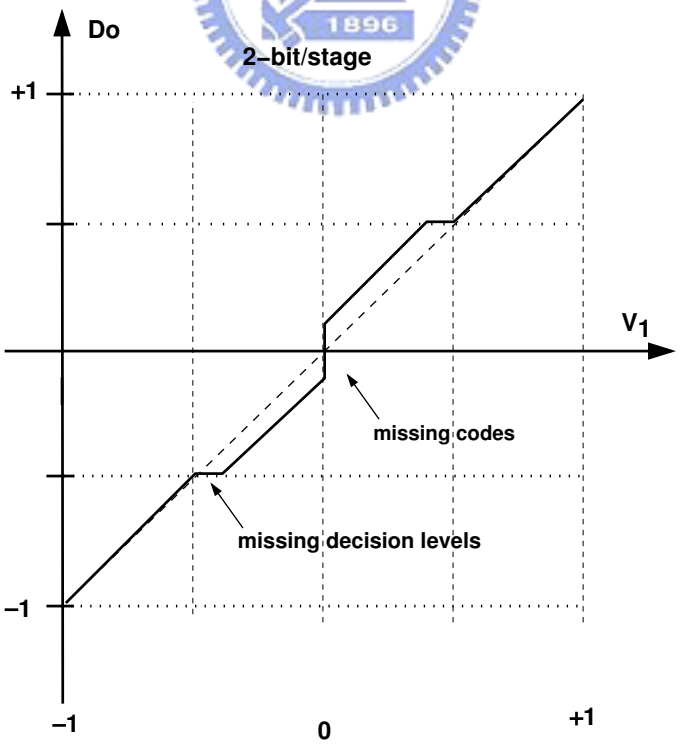

Figure 2.6: non-ideal-DAC effect on the whole ADC characteristic.

earity of the sub-DAC is the most important error source in a pipelined ADC. Fig. 2.5 gives the transfer curve of a pipelined stage with non-ideal DAC while Fig. 2.6 shows its effect on the overall ADC characteristic (Assume only the first stage is nonideal, the remaining stages are ideal). As can be seen, the sub-DAC nonlinearity results in both missing code and missing decision levels (i.e. saturation of the next stages). The primary source of the non-ideal sub-DAC reference levels in switched-capacitor implementation is capacitor mismatch.

The difference between the input analog signal and the sub-DAC analog output is then amplified by SHA. The transfer curve of a pipelined stage with interstage gain error is shown in Fig. 2.7. Fig. 2.8 demonstrates its effect on the overall ADC characteristic. As can be seen, too small of an interstage gain results in missing codes of the entire ADC, while too large of an interstage gain leads to missing decision levels. If there are mismatches in stage gains in the pipeline, the overall transfer curve will be a zigzag curve instead of a straight line as in the ideal case.

In a CMOS technology, SC circuit techniques are commonly used to implement a pipelined ADC. In this case,the non-ideal effects in the interstage amplifier are determined by the capacitor mismatches, finite opamp gain and gain-bandwidth product (GBW).

2.5 Digital Error Correction with Redundancy

It is not difficult to see from the discussion in last section that a multistage ADC with the minimal configuration is highly sensitive to errors in the threshold offsets, the sub-DAC errors and the interstage gain errors. Nevertheless, a digital error correcting scheme based on (2.7), which will be discussed in Chapter 3, can be employed to compensate for the sub-DAC and gain errors. As long as each term on the right hand side of (2.7), except Q, is derived from the actual values of converter components rather than nominal values, an almost exact approximation to the input voltage can be achieved. Note that the errors do not stem directly from incorrect reference levels. This is actually quite self-evident since V_j^{ref}'s do not appear in (2.7). Errors in reference levels weigh on the system indirectly in that the residue of one stage exceeds the input range of the next stage, causing missing decision levels.

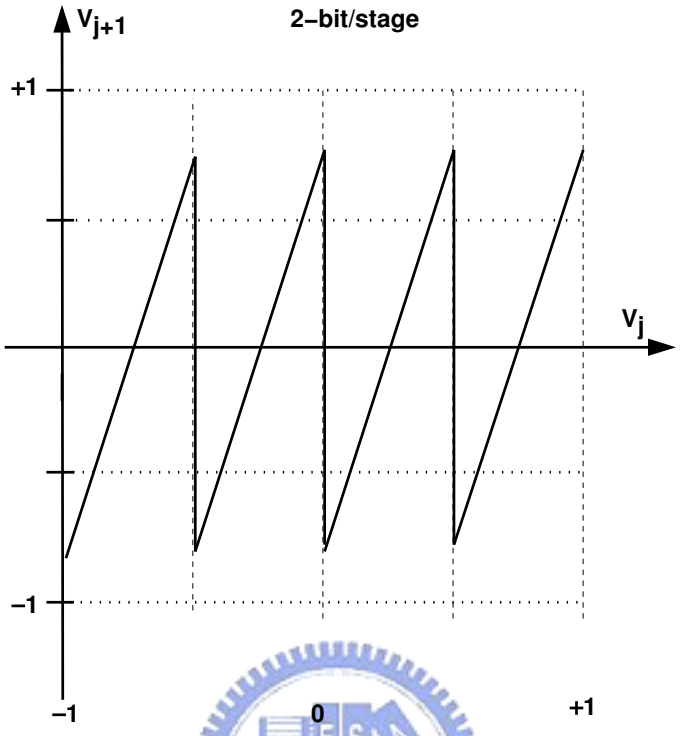

Figure 2.7: Transfer curve of a pipelined stage with interstage gain error.

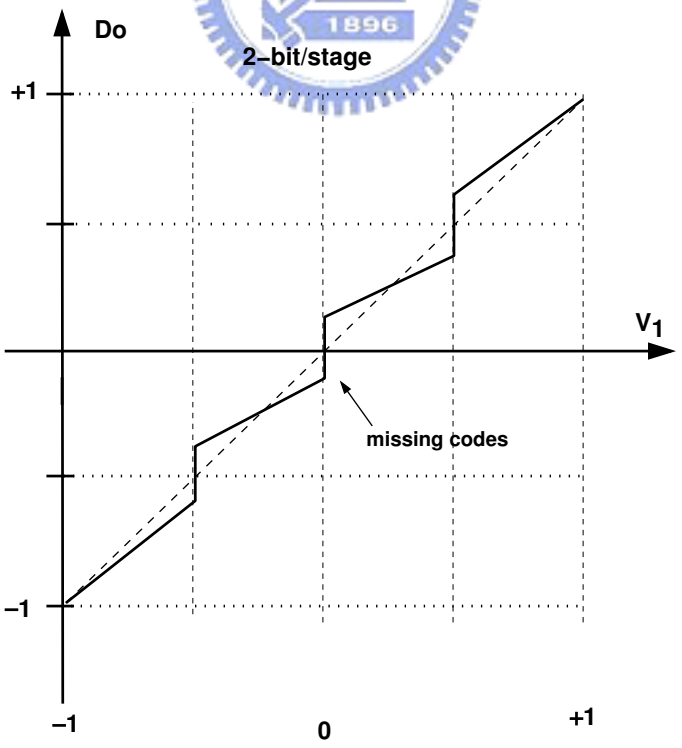

Figure 2.8: interstage-gain-error effect on the whole ADC characteristic.

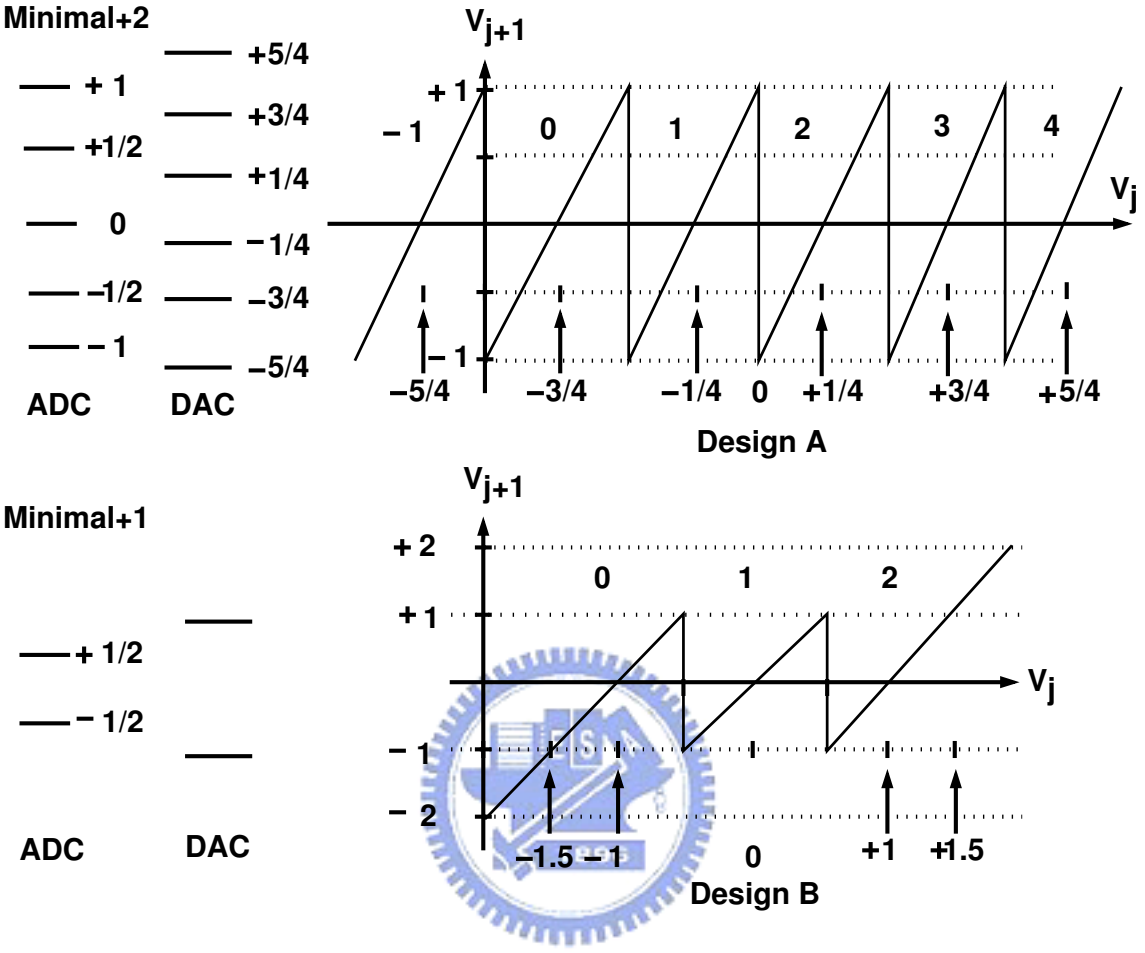

Figure 2.9: Redundant stages.

Assuming ideal interstage amplifiers (i.e. linear over a wide range of input signals), (2.7) remains valid even when the comparator makes a wrong decision. But when a residue exceeds the input range of the subsequent stage, this causes the next residue to be even further out of range. Finally, the last residue value becomes so large that (2.8) no longer holds. The quantization error becomes significant. In addition, some of the amplifiers may clip, which makes things even worse.

The problem can be solved by increasing the input range of each stage beyond the nominal output range of the previous stage. This guarantees that the residues remain limited and the overall quantization error is less than 1 LSB. The input range can be increased using a design where $M > |G_j| - 1$. This is done by either increasing the comparator number or decreasing the interstage gain with respect to the minimal design.

The former approach is often preferred because the nominal gain can remain integer – even a power of 2. Two possible designs of redundant stage with nominal gain of 4 and 2 are shown in Fig. 2.9, as well as their transfer curves.

Design A uses two extra (redundant) comparators compared with the minimal case, at the top and bottom of the range. $V_j^{ref}(D_j) = -1 + (D_j + 1)\Delta V = -1 + (D_j + 1)2/|G_j|$, for $-1 \leq D_j < M + 1$ and $V_j^{\mathrm{da}}(D_j) = -1 + (D_j + 1/2)\Delta V = -1 + (D_j + 1/2)2/|G_j|$ for $-1 \leq D_j \leq M + 1$, where M equals 3. One can verify that this provides an overrange capability of $\pm 2/|G_j|$. We will call this arrangement *minimal* + 2 [12].

Design B uses one redundant comparator compared with the minimal case and offsets both the $V_j^{ref}(D_j)$ and the $V_j^{\mathrm{da}}(D_j)$ by minus a half ΔV. $V_j^{ref}(D_j) = -1+(D_j+1/2)\Delta V = -1+(D_j+1/2)2/|G_j|$, for $0 \leq D_j < M+1$ and $V_j^{\mathrm{da}}(D_j) = -1+D_j\Delta V = -1+2D_j/|G_j|$ for $0 \leq D_j \leq M + 1$, where M equals 1. This arrangement has been described as implementing a "Redundant Signed Digit" (RSD) algorithm or the 1.5b/stage algorithm [22] [23]. We hereby call it "minimal + 1." One can verify that this provides an overrange capability of $\pm 2/(2|G_j|)$.

Either of the two redundant schemes mandate modifications in the derivation of the conversion result of (2.7) from D_j and $V_j^{\mathrm{da}}(D_j)$ for the base-2 converters, resulting in slightly more complex logic circuitries [24] [25]. However, the gain in robustness can be spectacular.

As a summary, to build pipelined ADCs with large tolerance to component nonidealities, one can employs redundancy technique that provides an overrange capability to permits large decision level shift and prevents threshold offsets from limiting the resolution of the converter. In this section, the method for the minimal base-2 converter to be translated into some specific types of redundant schemes is revealed, once the relationship between D_j and $V_j^{\mathrm{da}}(D_j)$ is derived, the conversion result can be found by substituting it into (2.7). In this technique, the sum of the individual stage resolutions is greater than the total resolution. The redundancy is then removed by a digital-correction algorithm, eliminating altogether the effects of sub-ADC nonlinearity and interstage offset on the overall linearity. In many previous implementations, the digital-correction algorithms have applied addition and subtraction to correct errors.

2.6 Pipelined ADC Examples

In this section, three examples of multistage ADC are examined. In each case the ADC operation is presented with the aid of the generalized mathematical description developed in Section 2.2. The examples contain detailed description of static input-output characteristics and digital code assignments. The treatment in this section is at the system/algorithm level. The objective here is to review multistage ADC architecture with different algorithmic features such as digital correction/redundancy and code assignment scheme.

Before processing, first a review of binary representation of real numbers is presented. A real number r lying between 0 and 1 (i.e. a unipolar number) with binary representation $B = b_1 b_2 b_3 \cdots b_P$, where the bits b_i have value either 0 or 1, can be written as

$$r = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N} = \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{2.12}$$

In some sense, the terms in the above summations can be regarded as binary fractions. For this purpose of this work, the following representation of a bipolar number r lying between -1 and $+1$ is used:

$$r = -1 + 2 \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{2.13}$$

This is similar to the unipolar number representation referenced to -1 with a total range of value 2.

2.6.1 Example 1

This example illustrates a pipelined ADC with 1 bit stage which has one extra redundancy comparator. This scheme has been described earlier in previous section. We have called it "minimal+1". The scheme also has been employed in a high-speed CMOS pipeline implementation [22]. In this example, the stage has a gain of two but has two threshold levels. The transfer characteristic is shown in Fig. 2.9. The terminology "1.5 bits per stage" is sometimes used to describe this stage [22] [26]. Note that the overall converter resolution is $P + 1$ bits with P stages. The static parameters are listed in Table 2.1.

Table 2.1: Static parameters of the 1.5bit/stage.

Input range	[-1, + 1](normalized to V_r)
sub-ADC threshold levels	$\{-1/4, 1/4\}$
3 digital codes	$\{0, 1, 2\}$ or $\{00, 01, 10\}$
3 sub - DAC levels	$\{-1/2, 0, 1/2\}$
Interstage gain	G = 2
Number of bits	n = 2(net, after digital correction:n=1)

The single pipelined stage input-output relation is

$$V_{j+1} = 2 \times \left[V_j - V_j^{\mathrm{da}}(D_j)\right] \tag{2.14}$$

From (2.7), the expression for the quantized analog output can be expressed as:

$$V_{1n} = V_1^{\mathrm{da}} + \frac{V_2^{\mathrm{da}}}{2} + \frac{V_3^{\mathrm{da}}}{2^2} + \cdots + \frac{V_P^{\mathrm{da}}}{2^{P-1}} = \sum_{j=1}^{P} \frac{V_j^{\mathrm{da}}(D_j)}{2^{j-1}} \tag{2.15}$$

Next, the relation between the digital codes and the corresponding sub-DAC levels is

$$V_j^{\mathrm{da}}(D_j) = \frac{-1}{2} + \frac{D_j}{2} \tag{2.16}$$

where $D_j = 0, 1, 2$. Substituting this expression into (2.15) gives

$$V_{1n} = \sum_{j=1}^{p} \frac{-\frac{1}{2} + \frac{D_j}{2}}{2^{j-1}} = -1 + \frac{1}{2^P} + \sum_{j=1}^{p} \frac{D_j}{2^j} \tag{2.17}$$

Thus, the $1/2^P$ term in (2.17) is simply a shift of $1/2$ LSB. The D_j in (2.17) may be considered $2-$bit numbers. Therefore, the summation in (2.17) corresponds to *addition with one bit overlapped between adjacent stages* [19].

2.6.2 Example 2

This example illustrates a pipelined ADC with 1-bit stage but the first stage has three redundancy comparators. In this example, the first stage has a gain of two but has four threshold levels. We call it "minimal+3", and the remaining stages are 1.5-bit-per-stage. The transfer characteristic is shown in Fig. 2.10.

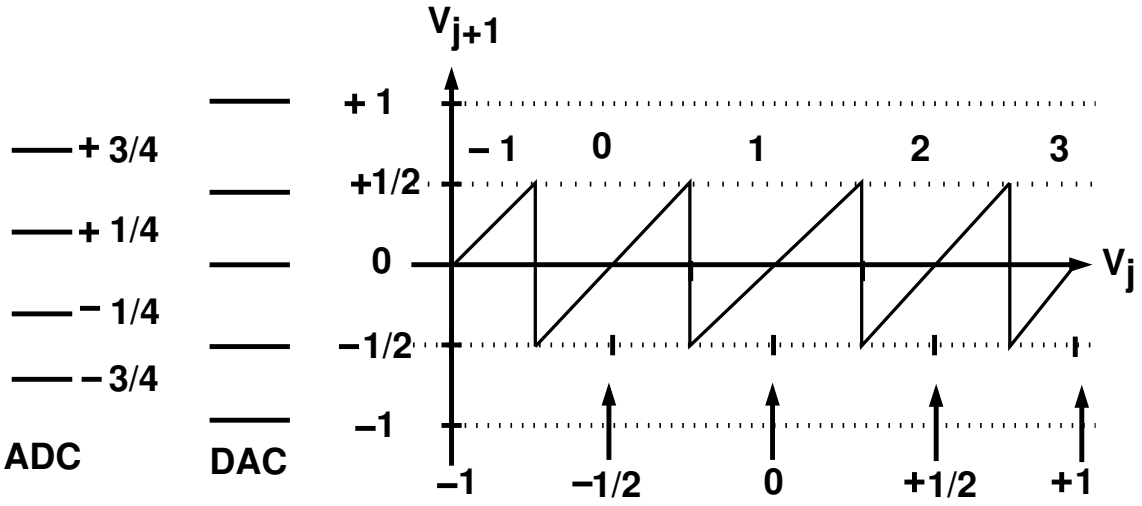

Figure 2.10: Transfer function of 1.5-bit per stage with dynamic range doubling.

Table 2.2: Static parameters of the DRD stage.

Input range	[-1, +1](normalized to V_r)
4 sub - ADC threshold levels	{-3/4, -1/4, 1/4, 3/4}
5 digital codes	{-1, 0, 1, 2, 3 } or {-01, 00, 01, 10, 11}
5 sub - DAC levels	{-1, -1/2, 0, 1/2, 1}
interstage gain	G = 2
Number of bits	n = 2(net, after digital correction:n = 1)

This scheme has been employed in an 80 MHz 10b pipeline ADC [27], while a similar technique with 3-bit MDAC in the first stage of a pipeline ADC has been presented [28]. The two additional comparators determine whether the input signal is smaller than $-3/4$ or larger than $3/4$, and in these two range the stage implements the algorithm $(2V_j + 2)$ or $(2V_j - 2)$, respectively. It can be seen in Fig. 2.10 that the amplifier output swing is now halved with respect to the previous implementation (i.e. 1.5-bit stage), a property that propagates to all the following stages, still of the conventional 1.5−bit type. The authors call this method as Dynamic-Range-Doubling (DRD) algorithm. The static parameters of the DRD stage are listed in Table 2.2.

Here, as in Algorithm Example 1, the individual stage input-output relation for DRD

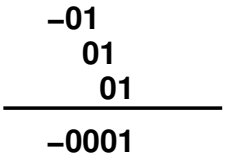

Figure 2.11: Conversion result of the DRD example.

is

$$V_{j+1} = 2 \times \left[V_j - V_j^{\mathrm{da}}(D_j)\right] \tag{2.18}$$

As can be seen, for the first stage the relation between the digital codes and the corresponding sub-DAC levels is the same as (2.16).

$$V_j^{\mathrm{da}}(D_j) = \frac{-1}{2} + \frac{D_j}{2} \tag{2.19}$$

where $D_j = -1, 0, 1, 2, 3$. Substituting this expression into (2.18) gives the expression for the amplitude-quantized analog output as that in (2.17),

$$V_{1n} = -1 + \frac{1}{2^P} + \sum_{j=1}^{p} \frac{D_j}{2^j} \tag{2.20}$$

The $1/2^P$ term in (2.17) is simply a shift of $1/2$ LSB, and the summation in (2.20) employs an overlapped addition to generate the final code. The presence of a negative number (-1) complicates thing a little somewhat. What it actually means that the range is extend slightly since a code more negative than all 0's is now possible.

To see how this works out, consider a pipeline ADC consisting a cascade of one DRD stage and two 1.5−bit stages. Let the input be $V_{1n} = -1 + \varepsilon$, where ε is a positive voltage of magnitude much smaller than 1 LSB at the overall ADC resolution. The outputs from the three stages are as follows: $D_1 = -1 = -01$, $D_2 = 0 = 01$, $D_3 = 0 = 01$ The final output is then obtained from an overlapped addition as given in Fig. 2.11. It can be seen that the output code is -1. This could be used as an indication of the underrange signal.

2.6.3 Example 3

This example illustrates a pipelined ADC with overrange capability. Fig. 2.12 shows the transfer characteristic of a 1-bit stage. In this case the interstage gain is two and there is

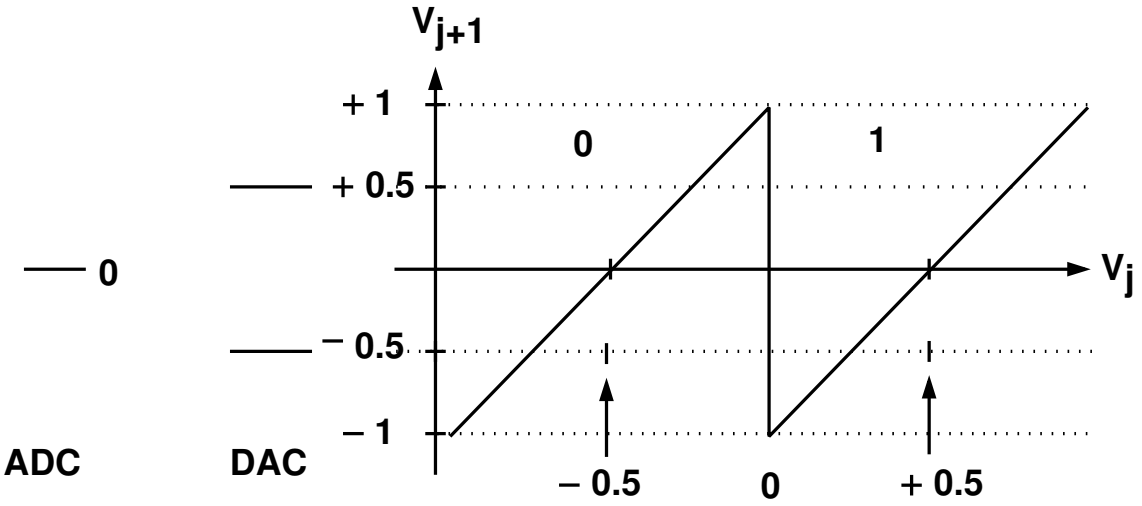

Figure 2.12: Transfer characteristic for the 1-bit converter.

only one transition boundary in the transfer characteristic. Due to the lack of redundancy, if the analog residue in one stage is outside the -1 to +1 range, this analog residue is amplified by two at each subsequent stage and eventually reaches the limiting region of the output voltage at a later stage. This scenario determines the missing decision levels in the overall transfer characteristic. This can usually be avoided by using a "radix< 2" conversion stage for the ADC [10] [13]. The drawback with such an approach is that a gain< 2 per stage is obtained by using extra capacitors and switches that eventually become a significant part of the stage loading, which becomes especially troublesome at high conversion speeds.

A better solution is to use overrange stages with an analog input range larger than one from -1 to +1, such that any residue input outside the -1 to +1 region will be converted back to the nominal -1 to +1 range [14] [29].

Fig. 2.13 shows the transfer characteristic of one overrange stage. This scheme has been presented in an single-ended 20 MHz 12-bit pipeline ADC [14]. Such an overrange stage has a nominal gain of two, equivalent to resolving one bit of resolution, but at the same time it can correct residues up to $1/2$ outside the nominal -1 to +1 range for the input voltage.

Consider a pipeline ADC consisting of a cascade of P stages. An overrange stage is inserted every three 1-bit stages, as shown in Fig. 2.14. Whether it's one overrange

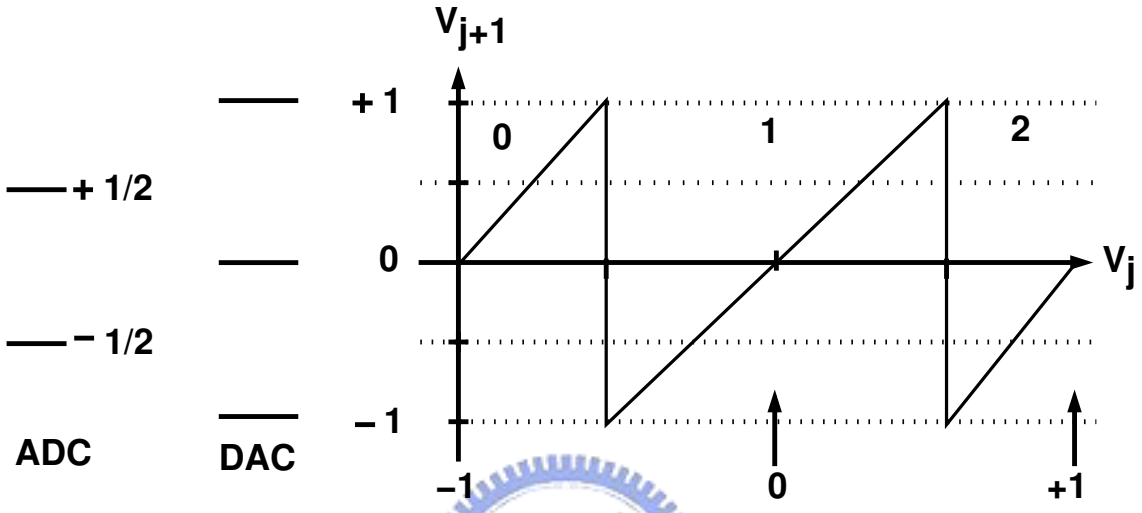

Figure 2.13: Overrange transfer characteristic.

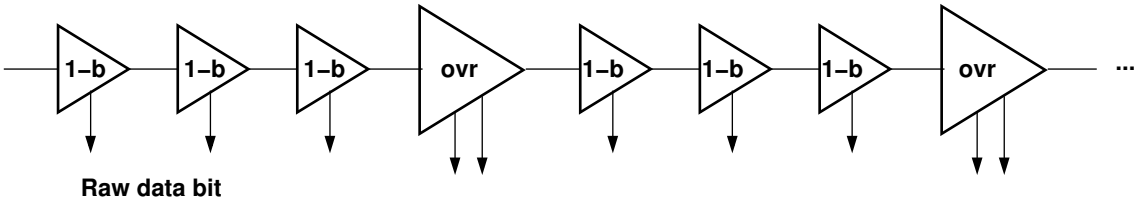

Figure 2.14: Architecture of the ADC including overrange stages.

Table 2.3: Static parameters of the 1-bit/stage.

Input range	[-1, + 1](normalized to V_r)
1 sub-ADC threshold levels	{0 }
2 digital codes	{0, 1 }
2 sub - DAC levels	{-1/2, 1/2}
interstage gain	G = 2
Number of bits	n = 1

stage per three 1-bit stages or any number of 1-bit stages depends on the magnitude of the worst-case errors that might occur in the analog path.

Table 2.4: Static parameters of the overrange stage.

Input range	[-1, + 1](normalized to V_r)
2 sub - ADC threshold levels	{-1/2, 1/2}
3 digital codes	{0, 1, 2} or {00, 01, 10}
3 sub - DAC levels	{-1, 0, 1}
interstage gain	G = 2
Number of bits	n = 2(net, after digital correction: n = 1)

The static parameters of the 1-bit per stage and the overrange stage are respectively listed in Table 2.3 and Table 2.4. The input-output relationship of individual stages for the 1-bit stage and overrange stage is given by

$$V_{j+1} = 2 \times \left[V_j - V_j^{\mathrm{da}}(D_j)\right] \tag{2.21}$$

As in the Algorithm Example 1, writing the expression for the amplitude-quantized analog output voltage gives

$$V_{1n} = V_1^{\mathrm{da}} + \frac{V_2^{\mathrm{da}}}{2} + \frac{V_3^{\mathrm{da}}}{2^2} + \cdots + \frac{V_P^{\mathrm{da}}}{2^{P-1}} = \sum_{j=1}^{P} \frac{V_j^{\mathrm{da}}(D_j)}{2^{j-1}} \tag{2.22}$$

Again, a relation between the digital codes and the corresponding DAC levels is in need. By looking at the codes D_j and the corresponding DAC levels $V_j^{\mathrm{da}}(D_j)$, it is clear that the

relation between them is given by, for the 1-bit per stage

$$V_j^{\mathrm{da}}(D_j) = \frac{-1}{2} + D_j \tag{2.23}$$

where D_j=0, 1, and for the overrange stage

$$V_j^{\mathrm{da}}(D_j) = -1 + D_j \tag{2.24}$$

where D_j=0, 1, 2.

Substituting this expression into (2.21) gives

$$\begin{aligned} V_{1n} &= (-\frac{1}{2} + D_1) + \frac{1}{2}(-\frac{1}{2} + D_2) + \frac{1}{4}(-\frac{1}{2} + D_3) + \frac{1}{8}(-1 + D_4) + \frac{1}{16}(-\frac{1}{2} + D_5) + \cdots \\ &= \sum_{j=1}^{p} \frac{-\frac{1}{2}}{2^{j-1}} + \sum_{j=1}^{[\frac{p}{4}]} \frac{-1}{2^{4j}} + \sum_{j=1}^{p} \frac{D_j}{2^{j-1}} \\ &= -1 + (\frac{1}{2^p} - \frac{1}{15}(1 - (\frac{1}{2^4})^{[\frac{p}{4}]})) + 2\sum_{j=1}^{p} \frac{D_j}{2^j} \\ &= bipolar\ code + coding\ offset + raw\ output \end{aligned} \tag{2.25}$$

The -1 on the right-hand side of (2.25) is expected, since this is a bipolar system. The next three terms in the bracket on the right-hand side constitute the coding offset. While smarter coding schemes may exist, the only difference is the expression of coding offset. Because the coding offset is a constant value depending on the number of pipeline stages (P), the actual conversion results can be easily obtained by adding the raw output and the coding offset.

The advantage of the generalized mathematic description presented in Section 2 is now evident: for a given stage transfer characteristic and given dc parameters, it provides a systematic way to work out a precise approach to combine the stage output codes D_j in order to generate the correct amplitude-quantized ADC output. Furthermore, it facilitates thorough study of the use of different static parameters, e.g., shifted sub-ADC thresholds or sub-DAC levels, or different code assignment schemes. It also allows examination of how such possible alternative schemes weigh on the complexity of the precise way that the outputs codes are combined to produce the final ADC output.

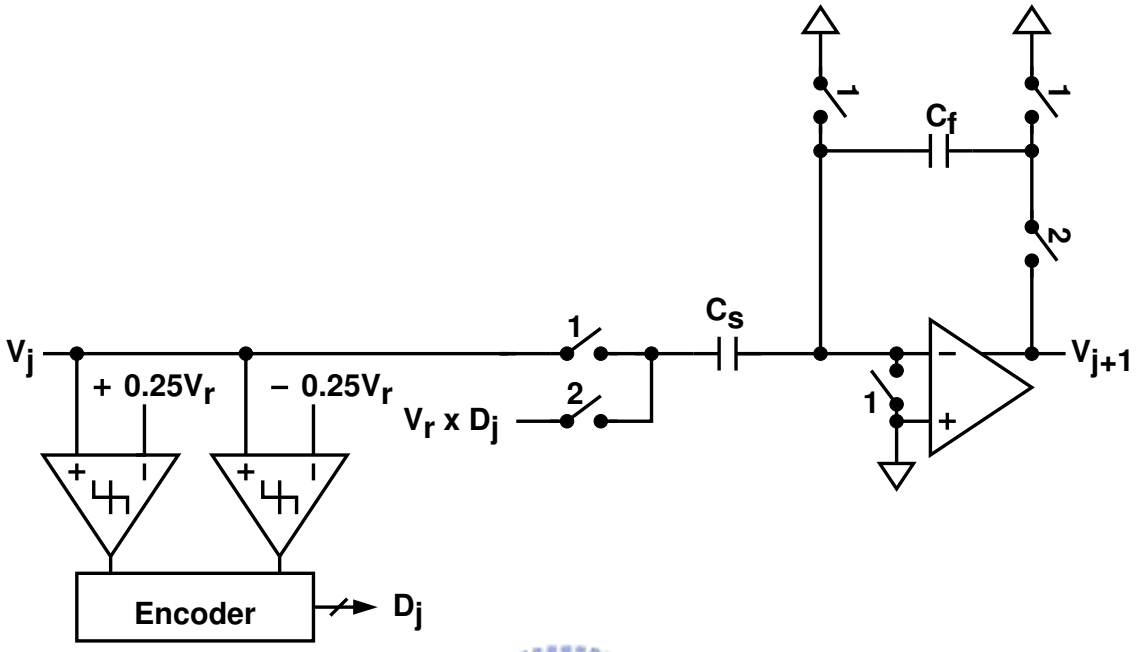

Figure 2.15: A SHA schematic.

2.7 CMOS Circuit Implementation

In CMOS technologies, a pipeline stage for A/D conversion generally consists of a set of voltage-mode comparators and a switched-capacitor (SC) multiplying digital-to-analog converter (MDAC). The MDAC combines the functions of a sample-and-hold, a digital-to-analog converter, a subtracter and a voltage-mode amplifier [30] [9].An SC MDAC employs an opamp with a capacitor feedback network to provide linear voltage amplification.

Fig. 2.15 gives the schematic of a conventional sample-and-hold amplifier (SHA) applied to a radix-2 1.5-bit switched-capacitor pipeline stage. The ϕ_1 and ϕ_2 are standard non-overlapping clocks. Each switch is closed when its controlling clock signal is high and open otherwise. Assume that the opamp is ideal except being with a limited gain A_0. The sub-ADC is made of two comparators with thresholds at $+0.25V_r$ and $-0.25V_r$, respectively. When clock ϕ_1 is high, V_j is sampled onto the capacitor C_s, the capacitor C_f is reset to ground. The digital code, $D_j \in \{-1, 0, +1\}$, is obtained by comparing V_j with $+0.25V_r$ and $-0.25V_r$. When clock ϕ_2 is high, C_f is connected to the opamp output, and C_s is connected to one of the three possible voltage $\{-V_r/2, 0, +V_r/2\}$ depending on the

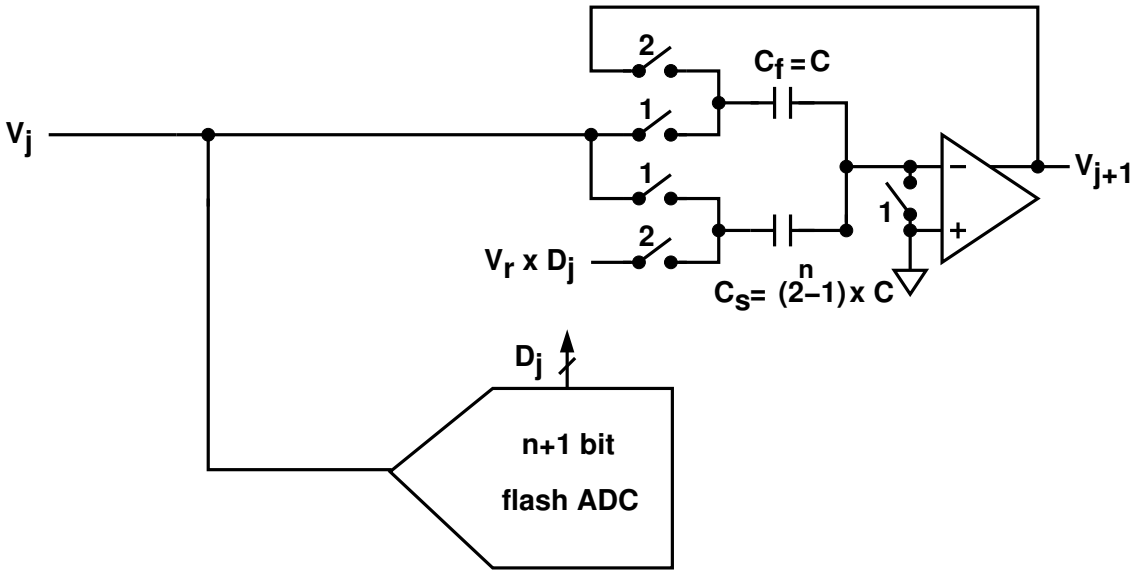

Figure 2.16: A general model of a SC pipeline stage.

outcome of the comparator. The output V_{j+1} can be written as:

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) - V_j^{\mathrm{os}} \right] \tag{2.26}$$

with

$$\hat{G}_j = \frac{C_s}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{2.27}$$

and

$$\hat{V}_j^{\mathrm{da}}(D_j) = \frac{V_r}{2} \times D_j \tag{2.28}$$

where C_p denotes the parasitic capacitance associated with the opamp's negative input. The realized j-th stage gain factor, $\hat{G}_j$, is a function of capacitor ratios, and the opamp's dc gain, A_0. The V_j^{os} term accounts for the offset effect of the j-th stage, including opamp's input-referred offset voltage and charge injection from analog switches. If the opamp gain A_0 is infinite and the capacitor matching is perfect with $C_s = 2C_f$, the close loop gain G_j is exactly two.

A variation on the scheme mentioned above is to use the same physical capacitor for both acquisition and residue amplification, namely, with the two actions sharing the feedback capacitor C_f. Fig. 2.16 illustrates the particular configuration of interest here.

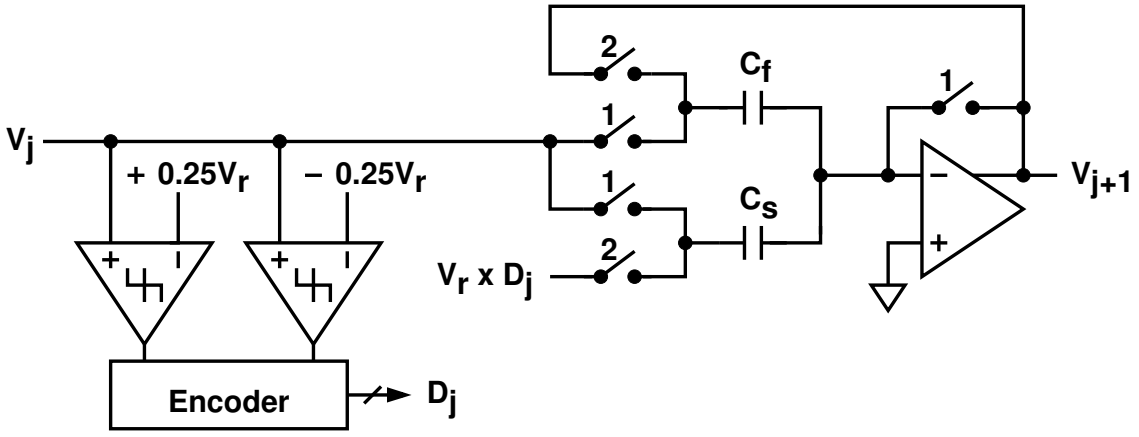

Figure 2.17: A radix-2 1.5-bit switched-capacitor (SC) pipeline stage.

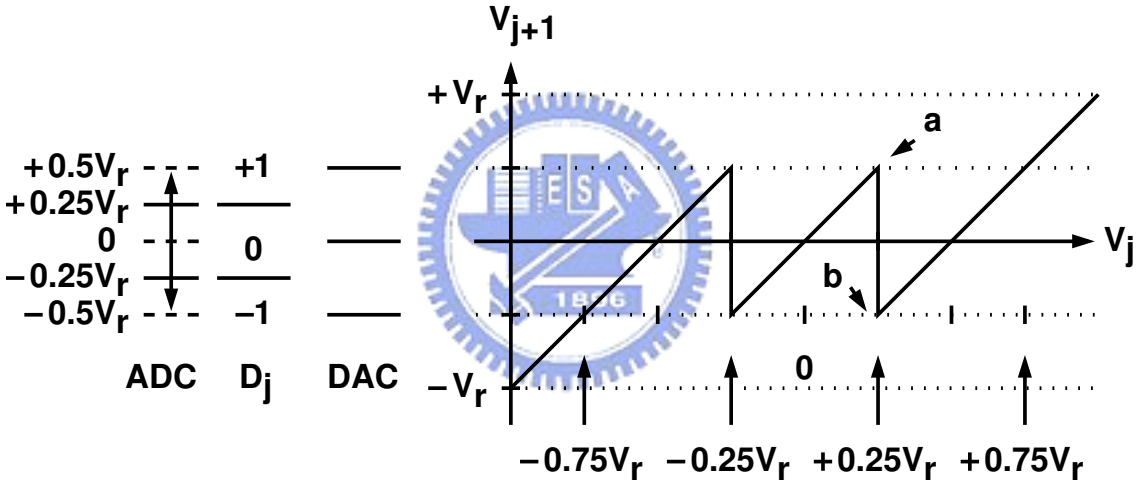

Figure 2.18: The conversion characteristic of the radix-2 1.5-bit SC pipeline stage.

It has a resolution of $n+1$ bits per stage, and an interstage gain of 2^n [26]. The sub-DAC function is performed by a set of capacitors with a reference voltage source V_r. When the input signal is applied, each stage samples and quantizes the signal to its per-stage resolution of $n+1$ bits, subtracts the quantized analog voltage from the signal by connecting the bottom plate of capacitors $C_S(=(2^n-1)\times C)$ to V_r, and passes the amplified residue to the next stage for finer conversion. The sub-ADC section is composed of $(2^{n+1}-2)$ comparators. The digital correction can tolerate the offset voltage of each comparator up to $\pm V_r/2^{n+1}$. The net resolution per stage after digital correction and redundancy removal is n bits.

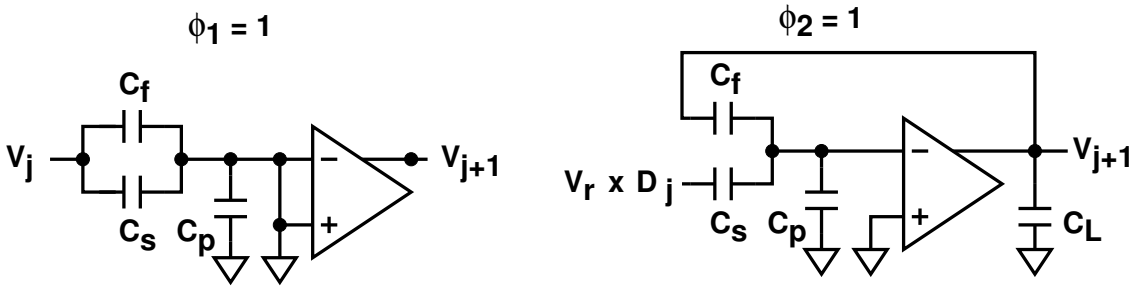

Figure 2.19: The operations of the radix-2 1.5-bit SC pipeline stage.

For $n = 1$, Fig. 2.17 reduced to a radix-2 1.5-bit switched-capacitor pipeline stage with shared feedback capacitor. The corresponding conversion characteristic is shown in Fig. 2.18. The sub-ADC is composed of two comparators with thresholds at $+0.25V_r$ and $-0.25V_r$, respectively. The opamp and the two capacitors, C_f and C_s, form a multiplying digital-to-analog converter, which performs the functions of sample-and-hold, digital-to-analog conversion, subtraction and voltage amplification. As shown in Fig. 2.19, when clock ϕ_1 is high, V_j is sampled onto capacitor C_f and C_s. The digital code, $D_j \in \{-1, 0, +1\}$, is obtained by comparing V_j with $+0.25V_r$ and $-0.25V_r$. When clock ϕ_2 is high, C_f is connected to the opamp output, and C_s is connected to one of the three possible voltage $\{-V_r, 0, +V_r\}$ depending on the outcomes of the comparators. Charge-conservation analysis shows that the $\hat{G}_j$ is

$$\hat{G}_j = \frac{C_s + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{2.29}$$

and

$$\hat{V}_j^{\mathrm{da}}(D_j) = V_r \cdot \frac{C_s}{C_s + C_f} \times D_j \tag{2.30}$$

Let $A_0 = \infty$ and $C_s = C_f$, an ideal transfer characteristic is obtained with $G_j = 2$ and $V_j^{\mathrm{da}}(D_j) = 0.5V_r \times D_j$.

By sharing the feedback capacitor C_f, a key advantage of this configuration is the improved feedback factor obtained when compared with the SHA mentioned above. Detailed discussion regarding this will be presented in later Chapter.

Fig. 2.20 shows a schematic of the DRD implementation mentioned in the algorithm example 2 of Section 2.6. The sub-ADC is composed of four comparators with thresholds at $-0.75V_r$, $-0.25V_r$, $0.25V_r$ and $+0.75V_r$ respectively. When clock ϕ_1 is high, V_j is

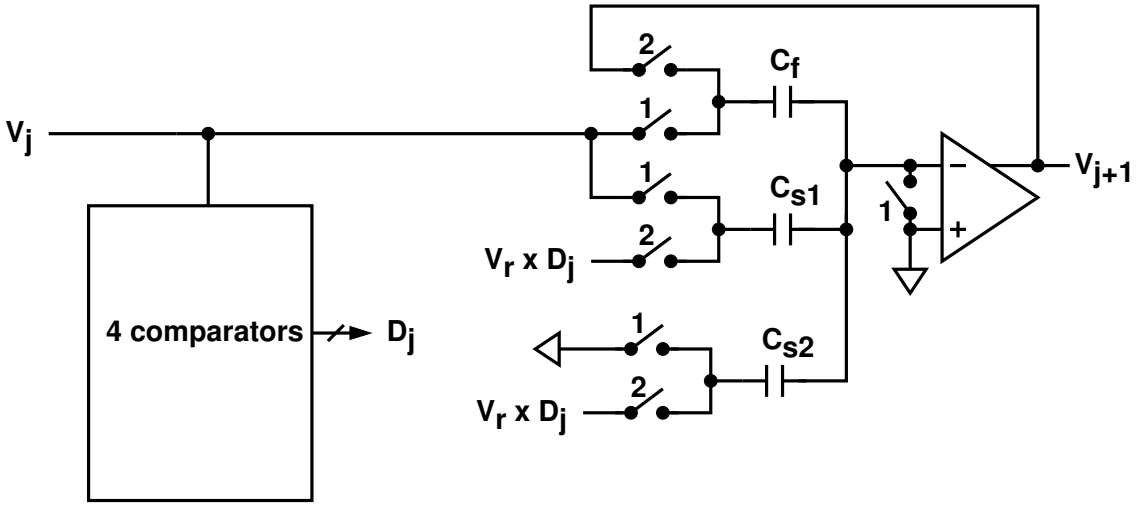

Figure 2.20: A 1.5bit stage with dynamic range doubling.

sampled onto capacitor C_f and C_{s1}. The C_{s2} is on the reset state. The digital code, $D_j \in \{-2, -1, 0, +1, +2\}$, is obtained by comparing V_j with $-0.75V_r$, $-0.25V_r$, $0.25V_r$ and $+0.75V_r$. When clock ϕ_2 is high, C_f is connected to the opamp output, and C_{s1} and C_{s2} are connected to one of the three possible voltage $\{-V_r, 0, +V_r\}$ depending on the outcomes of the comparators. Again, the output V_{j+1} is the same as (2.26) but the $\hat{G}_j$ is

$$\hat{G}_j = \frac{C_{s1} + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_{s1}+C_{s2}+C_f+C_p}{C_f}} \tag{2.31}$$

and

$$\hat{V}_j^{\mathrm{da}}(D_j) = \frac{V_r}{2} \cdot \frac{C_{s1} + C_{s2}}{C_{s1} + C_f} \times D_j \tag{2.32}$$

If the opamp gain A_0 is infinite and the capacitor matching is perfect with $C_{s1} = C_f$, the close loop gain G_j is exactly two.

2.8 Summary

In this chapter, the generalized mathematical description can be considered as a systematic approach to analyze and think about multistage A/D converter algorithms. Error sources in the pipeline stage are described in details. Minimal base-2 A/D converters are highly sensitive to suffer several nonlinearities caused by these error sources. An efficient method

is presented to describe the redundant schemes extended from the minimal base-2 architectures and also remove the magic or mystery of digital error correction. The usefulness of generalized mathematical description is proved by the illustrations of three examples of multistage ADC with different redundant schemes. Finally, The CMOS circuit implementations of the pipeline stage are presented, and the static errors of the MDAC are almost caused by component mismatches, finite opamp gain and the parasitic capacitance associated with the opamp's negative input.


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Chapter 3

Pipelined ADC Calibration Techniques

3.1 Introduction

The influence of sub-ADC's threshold shift, charge injection, capacitor mismatch and finite opamp gain on the performance of an ADC can be lowered through careful circuit design and layout technique. However, in high-resolution, high-linearity applications, the extent to which the influence can be suppressed is rarely sufficient. Considerable effort has recently been devoted to the development of calibration techniques that enable the realization of high-speed, high-linearity data converters in scaled CMOS VLSI technologies. Trimming and self-calibration techniques are such methods developed to serve this purpose. Trimming has the advantage of being transparent to the user but the disadvantage of being unable to track variation over time. Self-Calibration techniques measure errors by the converter itself and subtract the code errors during the normal operation. Some of the self-calibrations are based on adding circuit enhancements to reduce the error to a tolerable level. The analog self-calibration techniques require separate calibration DACs and precision analog components to compensate for gain errors in the MDACs. The analog DAC/gain calibration is one example of this type of techniques [8]. Other techniques do not attempt to fix the error but instead are based on design changes that make the error more tolerable. Digital calibration are examples of techniques that work this way [9].

Self-calibration techniques fall into two categories: (1) foreground calibration, which is calibration performed during the system power-up or standby, (2) background cali-

bration or continuous calibration. Foreground calibrations are limited in that the normal operation has to be interrupted to start the calibration cycle. Foreground calibrations further suffers from the lack of tracking capability. Therefore it is sensitive to temperature variations, supply voltage drift and device aging. Background calibration addresses this limitation and enables a converter to run calibration at any given time to track device and environment variations.

Either foreground or background techniques, these techniques can be further classified into two main groups depending on whether the calibration is performed in the analog or in the digital domain. Although the code errors are calculated in the digital domain, they are actually subtracted in the analog domain using a separate calibration DAC and precision analog components [31] [8] [32]. On the other hand, digital self-calibration techniques which subtract the code errors in the digital domain, do not require sophisticated analog circuits but put extra burden on the digital part and require either additional stages or additional resolution in each calibrated stage to overcome the loss in effective resolution due to digital truncation errors [9] [10] [11]. However, the cost of the calibration is increased complexity in the digital domain, the scaling law predicted by Moore is dramatically reducing the area and power dissipation of the digital processing, making the ADC architecture with digital calibration more compatible with the characteristics of modern CMOS processes.

From Section 3.2 to 3.3, several existing self-calibration techniques are reviewed, including analog calibration techniques, digital foreground calibration techniques and background calibration techniques. Section 3.3 presents the theory of digital calibration with mathematic descriptions. Section 3.4 describes the proposed digital background calibration technique. Section 3.5 has further examinations on three existing background calibration techniques. Section 3.6 draws the summary.

3.2 Analog Calibration Techniques

With the analog calibration technique, the errors of components (e.g. sub-DAC and residue amplifier) are measured and then corrected until they match with precision reference sources [32] [31] [8]. A block diagram illustrating the analog self-calibration system

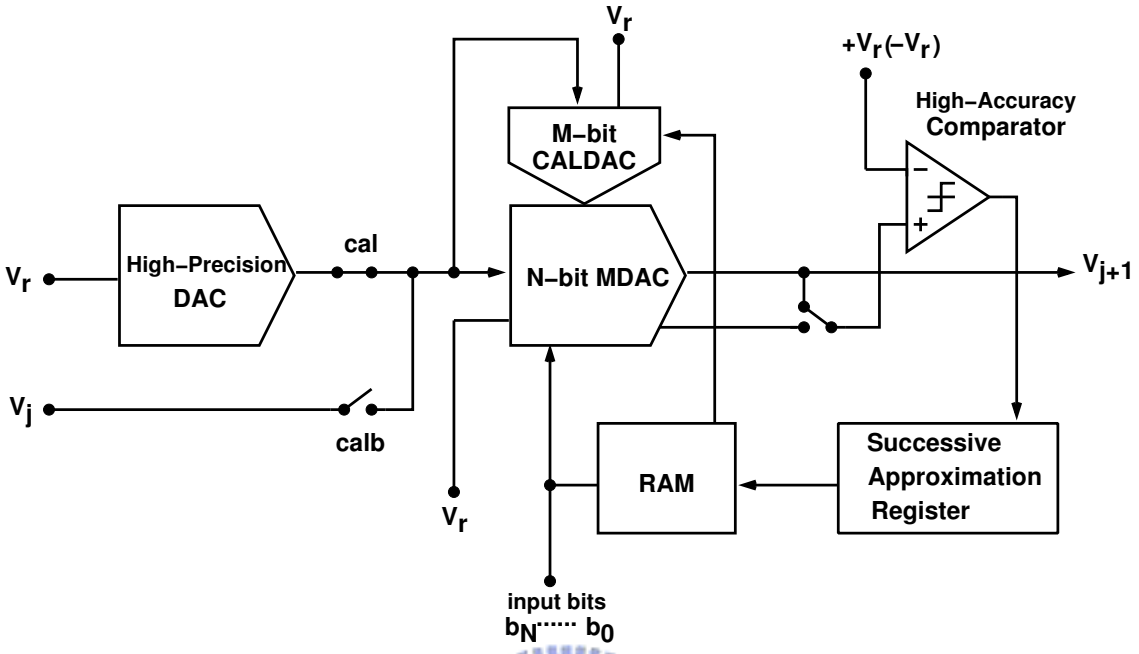


Figure 3.1: Block diagram illustrating the analog self-calibration system.

based on a high-precision reference DAC is shown in Fig. 3.1. Besides an N-bit MDAC, the analog part includes three extra blocks to implement the calibration technique: a high precision reference DAC, a high accuracy comparator, and an M-bit calibrating DAC. The digital part is composed of a random access memory and a successive-approximation register.

The system operates in two mode: the calibrating mode, where the errors in the N-bit MDAC are digitized and stored for subsequent correction, and the conversion mode where the self-calibrated MDAC provide the functions required in the front-end stage. Therefore, additional switches are required to facilitate different modes of operation.

In the calibration mode, the high precision reference DAC generates a predetermined precision voltage as the input signal into the MDAC. The input bits $b_N \cdots b_0$ take on one set of predetermined digital codes and pass into the sub-DAC to generate a corresponding analog voltage. The high precision comparator combined with successive approximation register (SAR) force the MDAC output to gradually approximate to $+V_r$ or $-V_r$. The calibrating DAC generates the required error voltage to compensate the MDAC.

The analog calibration technique needs the high precision reference DAC and high

precision comparator. Both components require special circuit design techniques or self-calibrated method to function properly [32].

3.3 Digital Calibration Techniques

The analog calibration technique described in the previous section requires a calibration DAC for the correction of each stage. The added calibration DAC increases the complexity and capacitive loading on opamps. Digital calibration techniques, which subtract the codes errors in the digital domain, have been introduced to relieve the accuracy requirements of analog calibration circuits. While digital calibration has the advantages of low complexity and high accuracy, most implementations are performed in the foreground. That means it needs to schedule calibration cycles that would interrupt normal ADC operation. Even if the calibration can be done during the system power-up or standby, the calibration should be run at all times to track device and environmental variations. The ideal solution to avoid the foreground interruptions is to operate calibration circuits all the time so that measurement cycles can be hidden in background and enables a converter to function in the presence of environmental fluctuations by continuously correcting for errors without disturbing normal ADC operation. More recently, several background calibration schemes have been proposed.

An extra pipeline stage can be employed to substitute the stage being calibrated [33], so that the normal operation need not be stopped during calibration. The disadvantage of this technique is that it results in fixed pattern noise due to periodic substitution of stages. A skip-and-fill algorithm was proposed to create the needed time slots for calibration [34] [35]. In this algorithm, the conversion of input sample is randomly skipped, and a sample of calibration signal is converted instead. The missing input samples are later filled in with nonlinearly interpolated data. The skip-and-fill method is relatively simple and accurate for implementation, but the input-signal bandwidth has to be limited to avoid performance degradation due to interpolated regeneration of skipped samples.

The adaptive digital calibration algorithm (or background calibration using reference ADC) was proposed to treat analog impairments in a pipeline ADC in analogy to distortion in communication channels; component errors from all stages of the pipeline

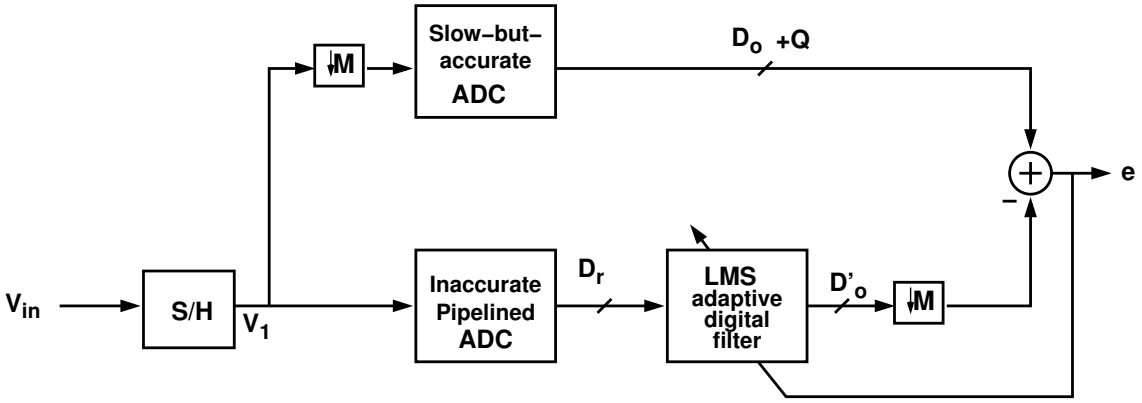


Figure 3.2: Error correction of pipelined ADC with adaptive least mean square algorithm.

are removed simultaneously using an adaptive finite-impulse response(FIR) digital filter. Fig. 3.2 shows the architecture of adaptive digital calibration algorithm [36] [37]. The output raw code D_r of a high speed, inaccurate pipelined ADC is applied to an adaptive digital filter(ADF) before being decimated; a parallel, slow-but-accurate ADC is used to obtain D_o; the ADF tap values are updated using a least mean square(LMS) algorithm driven by the error signal $e = D_o - D_r$ and the update is performed at the speed of the slow ADC. After calibration, the linearity of the pipeline is limited by the linearity of the slow-but-accurate ADC. The analog overhead is the slow-but-accurate ADC which can be a self-calibrated cyclic ADC or a Sigma-Delta ADC. The problem for the architecture is that the input signal should be large enough to fully calibrate the whole ADC.

In recent years, the correlation-based background calibration techniques have attracted attention since most of the calibration procedures can be undertaken in the digital domain. To calibrate a pipeline stage, all the correlation-based schemes involve introducing a known random term into the stage, and then measuring the stage's transfer characteristic by extracting the random term from the ADC digital output. The schemes differ in (1) how the problem is formulated; (2) how the random term is introduced, and (3) how the errors are corrected. Some schemes require an extra low-speed high-resolution ADC to determine the magnitude of the injected signal [38] [39]. If a pipeline stage includes a multi-bit sub-DAC, the mismatch errors in the sub-DAC can be eliminated by the DAC noise cancellation technique [40]. Correcting the pipeline stage's gain error can further improve the A/D resolution [41] [42] [43] [44]. The gain error correction technique of

[41] demands an increase of the required opamp's output range and an increase of complexity in the sub-DAC design [42] [43]. In the [42] [43] case, the required opamp's output range is increased by 50%. While the continuous gain correction technique of [44] does not increase the required opamp's output range, its performance depends on the accuracy of the sub-ADC [43], and it cannot function properly under certain input conditions. A random signal can also be injected into the pipeline stage by randomly switching the thresholds of the stage's internal comparators [45]. However, the scheme also requires the input to frequently appear near the thresholds of the comparators. Another technique that also involves switching the thresholds, switches the D/A configurations as well [46]. Both the conversion gain and nonlinear terms of the transfer characteristic of a pipeline stage can be statistically extracted from code distances at the same input location between two randomly-switching circuit configurations. However, to collect sufficient information, the scheme requires that the input appears frequently in certain locations. The original design also cannot correct D/A nonlinearity [46]. From Section 3.5.1 to 3.5.3, we give a detailed study of some calibration methods mentioned above. But an example of a background GEC scheme presented in Section 3.3.2 is utilized to be a comprehensive view of the correlation-based calibration method, it is intended to provide some background.

3.3.1 Foreground Calibration Techniques

In the digital foreground calibration technique, The ratios of components are measured, quantized by the remaining stages of the ADC, and then stored digitally. No effort is made to correct the components to make them match with each other. In normal operation, the stored results of the measurements are combined with the digital output of the ADC to generate a corrected digital one with improved linearity. While digital calibration of monolithic pipelined ADCs has been a popular research topic since 1990s. Most of previous works implemented it by inspecting the ADC transfer curve [9] [10] [11] [13] [14] [15]. Almost no solid mathematical foundation was established. In [12], a complete digital correction scheme and an iterative algorithm called "accuracy bootstrapping" are introduced, but it is still not clear and exact.

First, a 1.5-bit stage is used here to illustrate the concept of the digital calibration

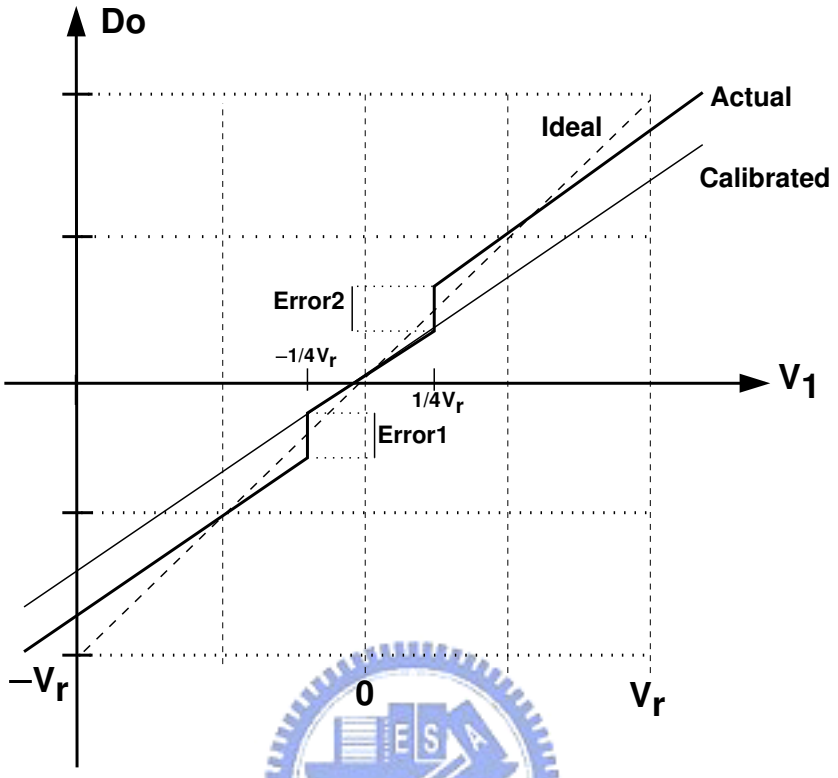


Figure 3.3: Transfer curve for 1.5-bit/stage pipeline ADC when interstage gain G > 2.

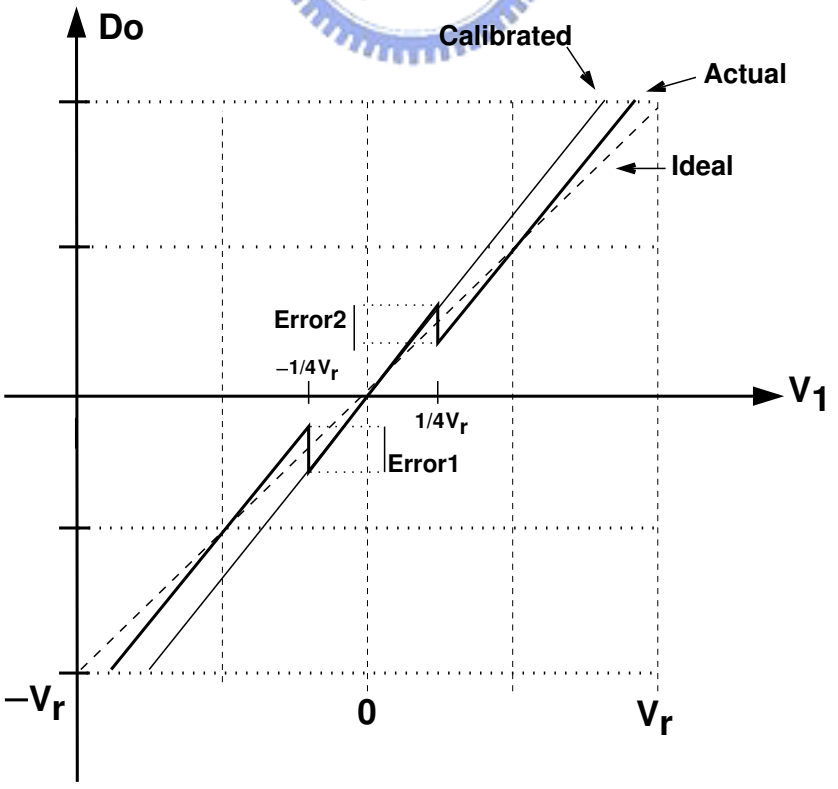


Figure 3.4: Transfer curve for 1.5-bit/stage pipeline ADC when interstage gain G < 2.

by the inspection of the ADC transfer curve [15]. Assume that a pipeline ADC consists of a cascade of P identical 1.5-bit stages and only the first stage has a gain error. For a pipeline stage, the accuracy of the interstage gain is very important. It is noted that the interstage gain error in a 1.5-bit stage causes two discontinuous sections in the ADC transfer curve near $\pm\frac{1}{4}V_r$. Fig. 3.3 shows the ADC transfer curve for an interstage gain less than two, while Fig. 3.4 shows the ADC transfer curve for an interstage gain greater than two. The Ideal transfer curve is drawn between the positive full-scale point and negative full-scale point by way of the zero point. When the interstage gain is exactly two with no errors in the circuit, the Actual transfer curve will be on the top of the Ideal transfer curve. However, when the interstage gain is less than two, as shown in Fig. 3.3, the Actual transfer curve will have two missing code sections located near the analog inputs of $+\frac{1}{4}V_r$ and $-\frac{1}{4}V_r$. Near these two analog inputs, the interstage transfer functions are switching from one region to another and the residues of the next stage are not accurate due to the interstage gain error. The number of missing codes (Error1 and Error2 in Fig. 3.3) at each point depends on the magnitude of the interstage gain error.

During the calibration cycle, Error1 and Error2 of the first stage are measured by the remaining stages(the second stage to P-th stage) and stored as calibration constants. During normal operation, the calibration constant Error1 is added into the ADC digital output whenever the analog input is below $-\frac{1}{4}V_r$. Similarly, the calibration constant Error2 is subtracted from the ADC digital output whenever the analog input is above $+\frac{1}{4}V_r$. After the calibration, the Calibrated transfer curve becomes a straight line, as shown in Fig. 3.3. But in the case of Fig. 3.4, during normal operation, the calibration constant Error1 is subtracted from the ADC digital output whenever the analog input is below $-\frac{1}{4}V_r$ and Error2 is added to the ADC digital output whenever the analog input is above $+\frac{1}{4}V_r$. After the calibration, the Calibrated transfer curve becomes a straight line, as shown in Fig. 3.4. The theory of digital calibration will be discussed in details below.

Redundancy solves the problem of threshold shifts in sub-ADC's, but not in the V^{da}'s and the G's. However, based on (2.7), a digital error correcting scheme that compensates for the sub-DAC and gain errors can be derived. With the behavior of pipeline stages governed by (2.26) rather than (2.4), for $j = 1, \cdots, P$, the overall A/D characteristic also deviates from the ideal one if (2.7) is still employed to compute the ADC's output

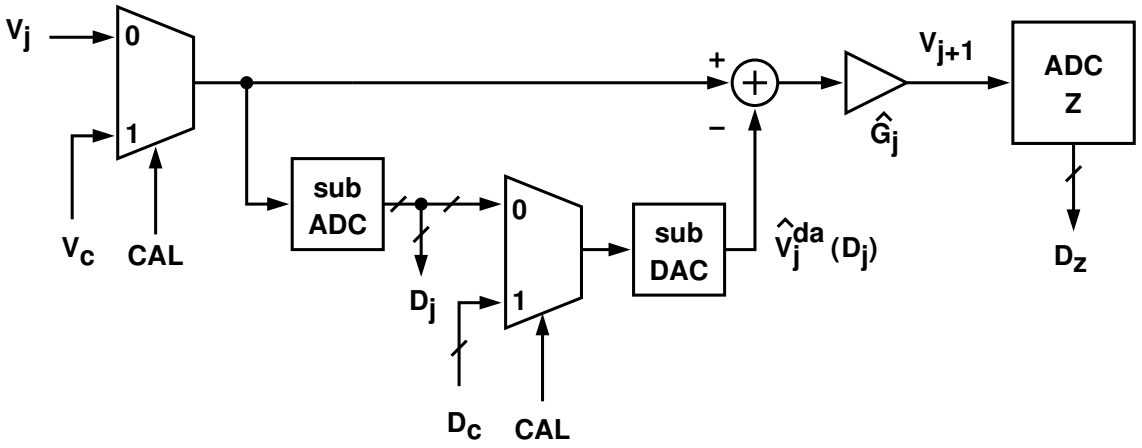


Figure 3.5: Digital calibration of the j-th pipeline stage.

code. It can be shown that the offset terms, V_j^{os} for $j = 1, \cdots, P$, contribute only to the overall A/D offset. Conversely, nonlinear A/D conversion occurs if $\hat{G}_j \neq G_j$ and $\hat{V}_j^{\text{da}}(D_j) \neq V_j^{\text{da}}(D_j)$. To achieve high resolution, values of both $\hat{G}_j$ and $\hat{V}_j^{\text{da}}(D_j)$ must be obtained to replace G_j and $V_j^{\text{da}}(D_j)$ in (2.7).

Normally in pipelined ADCs, a z-ADC is employed to calibrate $\hat{G}_j$ and $\hat{V}_j^{\text{da}}(D_j)$ of the j-th pipeline stage as demonstrated in Fig. 3.5, with z-ADC being the backend stages comprising of the $(j+1)$-th, $(j+2)$-th, ..., and P-th pipeline stages. The z-ADC quantizes the output of the j-th stage, V_{j+1}, and generates a corresponding digital code, D_z. If the z-ADC has a linear transfer characteristic, then V_{j+1} can be denoted as:

$$V_{j+1} = \hat{G}_j \cdot \left[V_j - \hat{V}_j^{\text{da}}(D_j) - V_j^{os}\right] = \frac{G_z}{\hat{G}_z} \cdot D_z + O_z + Q_z \tag{3.1}$$

This A/D conversion has a gain error of $G_z/\hat{G}_z$, an offset of O_z and a quantization error of Q_z. Here, G_z represents the specified gain factor and $\hat{G}_z$ is the realized gain factor.

When "CAL" signal is equal to "1", the j-th stage enters the state of calibration. In the calibration state, the predetermined signal V_c instead of V_j is passed into the j-th stage as the input signal, and the predetermined digital code D_c instead of D_j enters the sub-DAC to generate a corresponding analog voltage. Thus, the height of every vertical transition in the V_{j+1} vs. V_j transfer curve of Fig. 3.6 is measured and quantized by the z-ADC. The procedures include setting the j-th stage's input, V_j, and its sub-DAC output, $\hat{V}_j^{\text{da}}(D_c)$ to predetermined voltages. The V_{j+1} values at points, for example, a and b or c and d, are

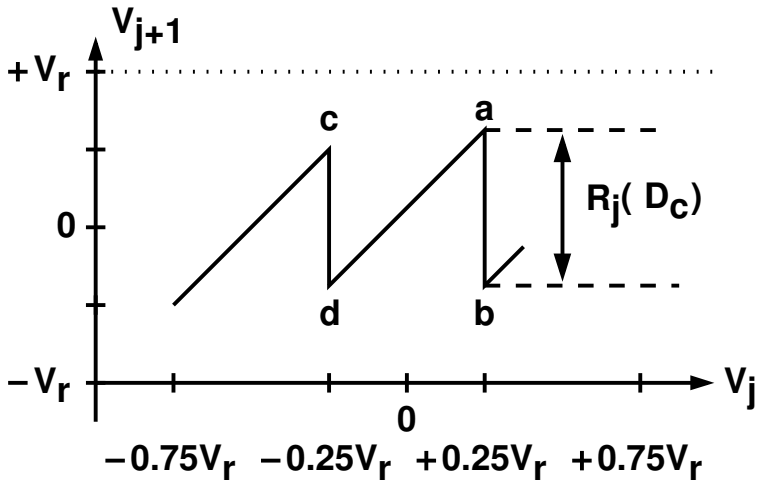


Figure 3.6: The conversion characteristic of a radix-2 1.5-bit SC pipeline stage under calibration.

measured separately [10] [12] [13] [14] [15] [16] [17] [18]. The residue output at point a can be written as

$$\begin{aligned} V_{j+1,a} &= \hat{G}_j \cdot \left[V_c - \hat{V}_j^{\mathrm{da}}(D_a) - V_j^{os}\right] \\ &= \frac{G_z}{\hat{G}_z} \cdot D_{z,a} + O_z + Q_{z,a} \end{aligned} \tag{3.2}$$

and the residue output at point b can be expressed as

$$\begin{aligned} V_{j+1,b} &= \hat{G}_j \cdot \left[V_c - \hat{V}_j^{\mathrm{da}}(D_b) - V_j^{os}\right] \\ &= \frac{G_z}{\hat{G}_z} \cdot D_{z,b} + O_z + Q_{z,b} \end{aligned} \tag{3.3}$$

Subtracting the two measurements gives

$$V_{j+1,b} - V_{j+1,a} = \hat{G}_j \cdot \left[\hat{V}_j^{\mathrm{da}}(D_b) - \hat{V}_j^{\mathrm{da}}(D_a)\right] = \frac{G_z}{\hat{G}_z} \cdot (D_{z,b} - D_{z,a}) + (Q_{z,b} - Q_{z,a}) \tag{3.4}$$

By taking the average of multiple measurements, the $Q_{z,b} - Q_{z,a}$ quantization error term is eliminated due to noise dithering. Let $D_j \in \{0, 1, 2, \cdots\}$. For a $D_c > 0$, the calibration measurements yield

$$\hat{G}_j \cdot \left[\hat{V}_j^{\mathrm{da}}(1) - \hat{V}_j^{\mathrm{da}}(0)\right] = \frac{G_z}{\hat{G}_z} \cdot D_{z,1}$$

$$\hat{G}_j \cdot \left[\hat{V}_j^{\mathrm{da}}(2) - \hat{V}_j^{\mathrm{da}}(1)\right] = \frac{G_z}{\hat{G}_z} \cdot D_{z,2}$$

...

$$\hat{G}_j \cdot \left[\hat{V}_j^{\mathrm{da}}(D_c) - \hat{V}_j^{\mathrm{da}}(D_c - 1)\right] = \frac{G_z}{\hat{G}_z} \cdot D_{z,D_c} \tag{3.5}$$

Thus,

$$\hat{G}_j \cdot \left[\hat{V}_j^{\mathrm{da}}(D_c) - \hat{V}_j^{\mathrm{da}}(0)\right] = \frac{G_z}{\hat{G}_z} \cdot D_z(D_c) \tag{3.6}$$

and

$$D_z(D_c) = D_{z,1} + D_{z,2} + \cdots + D_{z,D_c} \tag{3.7}$$

The offset term of the j-th stage, V_j^{os}, can be chosen so that $\hat{V}_j^{\mathrm{da}}(0) = 0$. Then, Equation 3.6 becomes

$$R_j(D_c) = \hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_c) = \frac{G_z}{\hat{G}_z} \cdot D_z(D_c) \tag{3.8}$$

The transition height in Fig. 3.6 is the step size of $R_j(D_c)$ when the digital code, D_c, is changed by 1. The above equation can be rearranged as:

$$\hat{V}_j^{\mathrm{da}}(D_c) = \frac{G_j G_z}{\hat{G}_j \hat{G}_z} \cdot T_j(D_c) \tag{3.9}$$

where $T_j(D_c)$ is defined as

$$T_j(D_c) = \frac{D_z(D_c)}{G_j} \tag{3.10}$$

The digital values of $T_j(D_c)$ are stored and used to generate the ADC's output codes.

During normal A/D conversion operation, the combined A/D conversion for the j-th stage followed by the z-ADC can be expressed as:

$$V_j = \hat{V}_j^{\mathrm{da}}(D_j) + V_j^{\mathrm{os}} + \frac{V_{j+1}}{\hat{G}_j} \tag{3.11}$$

Combining (3.11), (3.1), and (3.9), gives

$$\begin{aligned} V_j &= \frac{G_j G_z}{\hat{G}_j \hat{G}_z} \cdot T_j(D_j) + V_j^{\mathrm{os}} + \frac{1}{\hat{G}_j} \cdot \left[\frac{G_z}{\hat{G}_z} \cdot D_z + O_z + Q_z\right] \\ &= \frac{G_j G_z}{\hat{G}_j \hat{G}_z} \cdot \left[T_j(D_j) + \frac{D_z}{G_j}\right] + \left(V_j^{\mathrm{os}} + \frac{O_z}{\hat{G}_j}\right) + \frac{Q_z}{\hat{G}_j} \\ &= \frac{G_{jz}}{\hat{G}_{jz}} \cdot D_{jz} + O_{jz} + Q_{jz} \end{aligned} \tag{3.12}$$

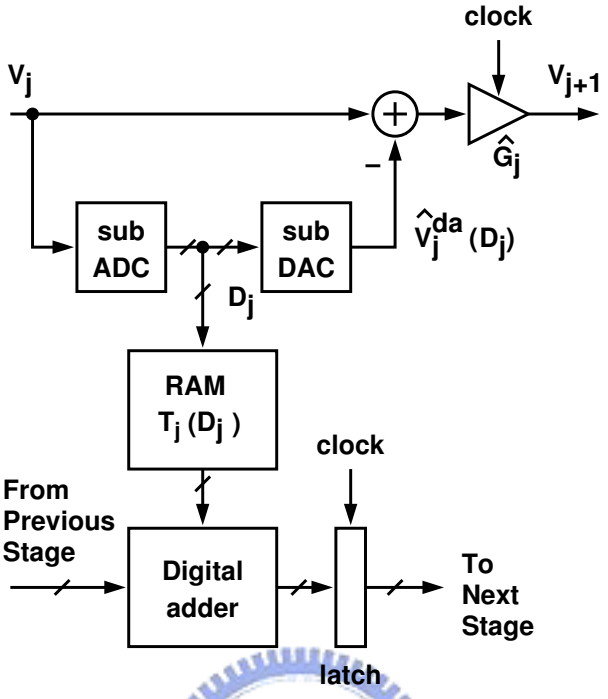


Figure 3.7: Converter stage with look-up table.

where

$$\text{Digital Output} = D_{jz} = T_j(D_j) + \frac{D_z}{G_j} \tag{3.13}$$

$$\text{Gain Error} = \frac{G_{jz}}{\hat{G}_{jz}} = \frac{G_j G_z}{\hat{G}_j \hat{G}_z} \tag{3.14}$$

$$\text{Offset} = O_{jz} = V_j^{\text{os}} + \frac{O_z}{\hat{G}_j} \tag{3.15}$$

$$\text{Quantization Error} = Q_{jz} = \frac{Q_z}{\hat{G}_j} \tag{3.16}$$

Thus, the combined j-th stage and z-ADC has a linear A/D conversion characteristic if D_{jz} of (3.13) is used as the combined digital output. The conversion carries a new gain error of $G_{jz}/\hat{G}_{jz}$ and a new offset of O_{jz}. The combined quantization error, Q_{jz}, is reduced by a factor of the stage gain, $\hat{G}_j$. The similarity between (3.12) and (3.1) indicates that $j+z$ ADC with the linear conversion characteristic of (3.12) can then be used to calibrate the preceding $(j-1)$-th stage.

With (3.10), each stage of the converter consists of associating a digital look-up table, as depicted in Fig. 3.7. Each stage is addressed by the local digital codes of the stage,

and generates one term of (2.7). The terms are summed in a pipelined fashion in order to form the conversion result. No matter what the *actual* values of gains and sub-DAC levels are, the converter can be linearized(within the limits of the quantization error) by using appropriate digital values ($T_j(D_c)$) in the look-up table. No tuning of analog components is necessary, as long as the digital values are computed accurately.

Using equation (3.9) - (3.12), (2.7) is rewritten as below (G_j is the *nominal* interstage gain of the j-th stage, offset errors in pipeline stages are ignored for simplicity):

$$\frac{\hat{G}_1\hat{G}_2\cdots\hat{G}_P}{G_1G_2\cdots G_P}V_1 = \frac{\hat{G}_1\hat{G}_2\cdots\hat{G}_P}{G_1G_2\cdots G_P}\hat{V_1^{da}} + \frac{\hat{G}_2\hat{G}_3\cdots\hat{G}_P}{G_1G_2\cdots G_P}\hat{V_2^{da}} + \cdots + \frac{\hat{G_{P-1}}\hat{G}_P}{G_1G_2\cdots G_P}\hat{V_{P-1}^{da}} + \frac{\hat{G}_P}{G_1G_2\cdots G_P}\hat{V_P^{da}} + \frac{\hat{V_{P+1}}}{G_1G_2\cdots G_P} \tag{3.17}$$

The V_{P+1} can be written as follow:

$$V_{P+1} = \frac{G_z}{\hat{G}_z}\cdot D_z + O_z + Q_z \tag{3.18}$$

Using equation (3.9), (3.10) and (3.18) and substituting into (3.17) gives

$$\hat{m}V_1 = \left[\left[\left[\left[\left[\frac{T_1(D_1)}{G_1G_2\cdots G_P}\right]G_1 + \frac{T_2(D_2)}{G_1G_2\cdots G_P}\right]G_2 + \cdots\right]G_{P-2} + \frac{T_{P-1}(D_{P-1})}{G_1G_2\cdots G_P}\right]G_{P-1} + \frac{T_P(D_P)}{G_1G_2\cdots G_P}\right]G_P + Q_{Pz} + O_{Pz} \tag{3.19}$$

where $\hat{m}$ is a gain error defined as

$$\hat{m} = \frac{\hat{G}_1\hat{G}_2\cdots\hat{G_{P-1}}\hat{G}_P\hat{G}_z}{G_1G_2\cdots G_{P-1}G_PG_z} \tag{3.20}$$

, the offset contributed by the z-ADC is became as

$$O_{Pz} = \frac{O_z\hat{G}_z}{G_1G_2\cdots G_{P-1}G_PG_z} \tag{3.21}$$

and the P-stages' combined quantization error Q_{pz} is

$$Q_{Pz} = \frac{1}{G_1G_2\cdots G_{P-1}G_PG_z}(Q_z\hat{G}_z + D_zG_z) \tag{3.22}$$

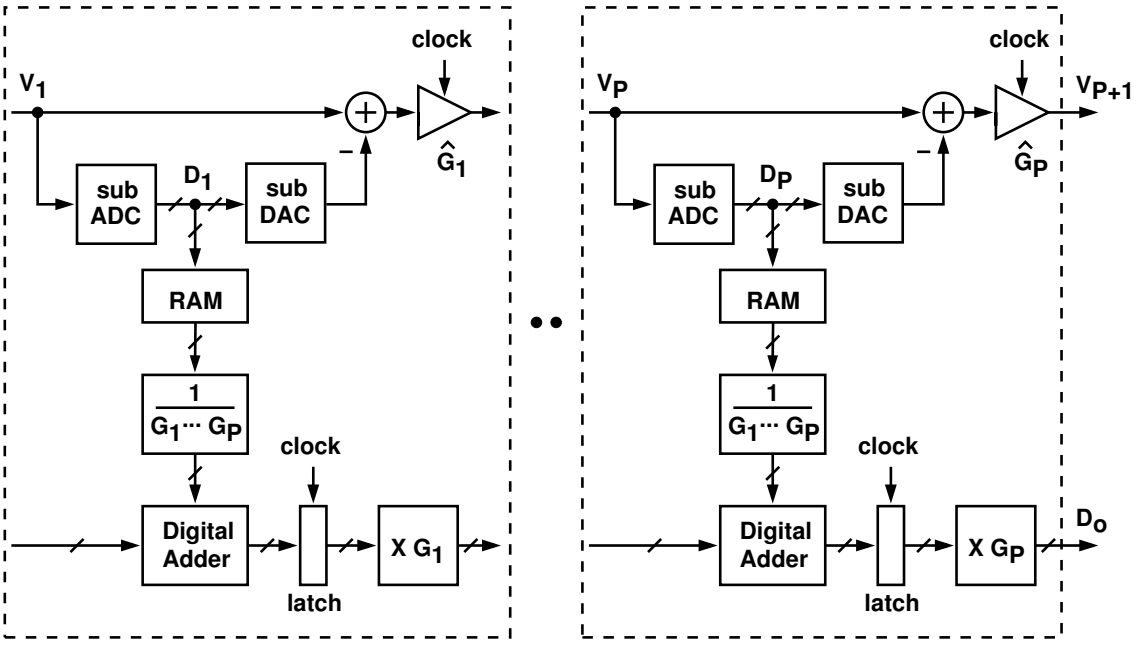


Figure 3.8: Pipelined ADC architecture with look-up table.

The conversion result D_o is now rewritten as follows:

$$D_o = \left[\left[\left[\left[\left[\frac{T_1(D_1)}{G_1G_2\cdots G_P}\right]G_1 + \frac{T_2(D_2)}{G_1G_2\cdots G_P}\right]G_2 + \cdots\right]G_{P-2} + \frac{T_{P-1}(D_{P-1})}{G_1G_2\cdots G_P}\right]G_{P-1} + \frac{T_P(D_P)}{G_1G_2\cdots G_P}\right]G_P \tag{3.23}$$

The architecture that calculates the conversion result according to (3.23), is shown in Fig. 3.8. The look-up tables contain the $T_j(D_c)$ values.

The above equation expresses the conversion result in a recursive way. It indicates that, when translated into hardware, this form results in identical design for each stage. After the calibration, the calibrated transfer curve becomes a straight line but it is scaled by $\hat{m}$(as the example shown in Fig. 3.3 and Fig. 3.4). If only the static errors (finite opamp gains and capacitor mismatches) exist in pipeline stages, the $\hat{m}$ is linear. In this case it does not introduce any error except that it reduces or increasing the signal amplitude by a small portion. If $\hat{m} < 1$, the final digital output from the ADC never reaches the extremes of the digital output range (all ”1”’s or all ”0”’s), so missing codes still exist in these locations. If $\hat{m} > 1$, the final digital output from the ADC can easily reach the extremes of the digital

output range with no remaining missing codes. Only a slight degradation in dynamic range results. The scaling factor $\hat{m}$ can be recovered (i.e. $\hat{m} = 1$) by quantizing two known input, e.g., $V_1 = -V_r$ and $V_1 = +V_r$. For the case of $\hat{m} < 1$, it is possible to fully recover $\hat{m} = 1$, But in the case of $\hat{m} > 1$, missing codes still exist around these locations of $-V_r$ and $+V_r$. Owing to this fact, before the input reaches the extreme voltages ($-V_r$ or $+V_r$), some of the pipeline stages in the pipelined ADC have saturated or clipped.

Digital correction by look-up tables based on (3.23) requires knowledge of the weights W. Some authors referred to the stored digital values as "weights," W [19] [12]. The calibration procedure is summarized as follows: Based on (3.8), the calibration procedure starts with individually measuring all the sub-DAC levels of each converter stage, using the remaining stages of the pipeline. The measured results are used to update the look-up tables of that stage, and the process is repeated until each stage has been calibrated. The complete calibration is done by calibrating from the tail stage (stage P) to the front stage (stage 1) of the pipeline.

The accuracy requirement of the stages is loosen toward the end. It turns out that usually we only need to calibrate the front few stages to improve the differential nonlinearity (DNL) of the system. In the calibration mode, the calibrated code representations of the sub-DAC levels are stored in memory cells. In the conversion mode, the sub-ADC of each stage digitizes the analog input and output the coarse code as an address code into the memory cell to look for the appropriate code representation of the sub-DAC levels of that stage. The weights of each stage are added together to get the final output code. The DNL of the ADC system is greatly improved in expense of digital memories and adders. Therefore, no multiplications are needed in the calibration.

3.3.2 Correlation-Based Background Calibration

Fig. 3.9 illustrates one possible background GEC scheme based on correlation [47]. The key blocks are: a pseudorandom number generator (PRNG), a 1-bit DAC, the ADC under calibration, a digital multiplier with variable gain G_v, and a digital accumulator (ACC). The sequence q generated by the PRNG is binary and approximately white. It has zero mean and is uncorrelated with the input signal S. The q signal is scaled by a constant

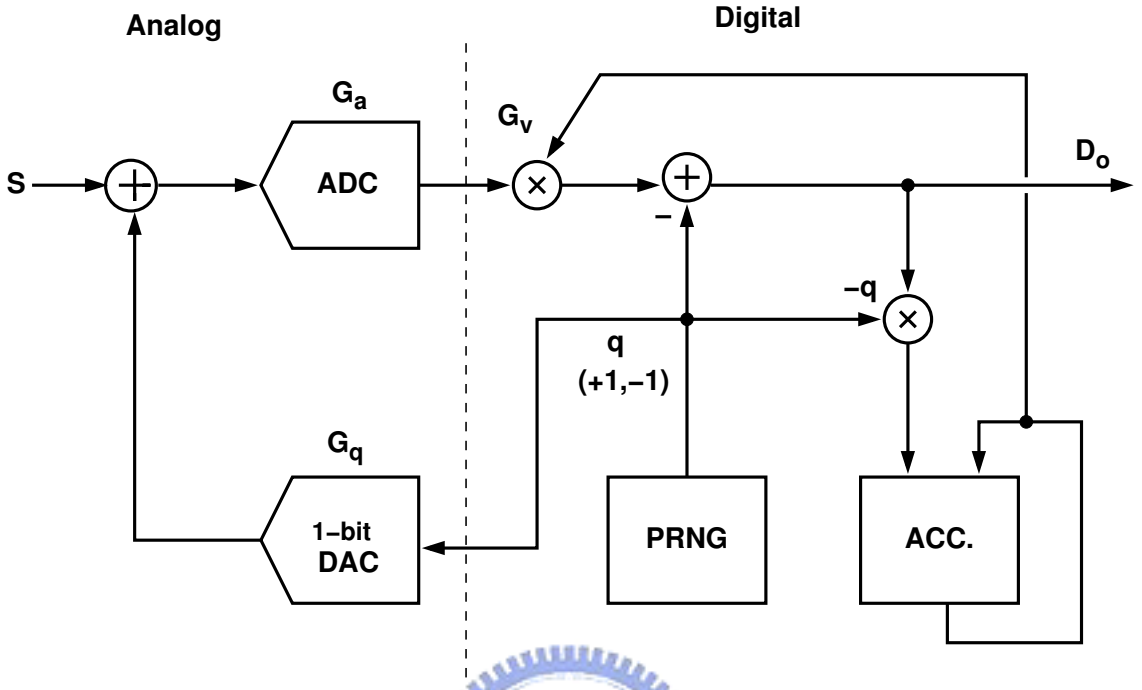


Figure 3.9: The gain calibration loop to illustrate the correlation-based calibration method.

G_q and then added to the input of the ADC. The pseudorandom noise travels through the ADC which contains the actual gain G_a. Finally, to maintain the same SNR, the added q signal is subtracted from the ADC's output in the digital domain to get the difference D_o as the ADC final output. Then D_o is multiplied by q and accumulated to determined the gain G_v through feedback.

A linear model is used to simplify the analysis. Assume the ADC and DAC are represented as linear amplifiers with constant gain of G_a and G_q. Consider the two paths from the PRNG to the inputs of the subtracter that computes D_o. If the random-number gain in one path, which is $G_q \times G_a$ times the variable gain G_v, does not equal the random-number gain in the other path (which is unity), the subtraction of the calibration signal is not complete at the output, leaving a random-number residue in D_o. In general, D_o comprises of two parts: one is related to the input signal S, the other is related to the random-number residue. When D_o is multiplied by the random number q, the term that contains the product of S and q is averaged out by the accumulator since the random number is uncorrelated with the input signal. However, the term that contains $q^2 = 1$ has a nonzero mean value

and will produce a nonzero output from the digital accumulator. The key of the scheme is that the variable gain G_v is continuously updated through negative feedback. If the digital accumulator is ideal, its dc gain is infinite and the negative feedback will force its input to be zero mean. This occurs when the average random-number residue in D_o is driven to zero, or equivalently when the average gain applied to the random number in the path through the ADC ($G_q \times G_a$ times the average G_v) equals one.

The equations used to compute the variable gain G_v are

$$G_v[n+1] = G_v[n] - q[n]D_o[n] \tag{3.24}$$

and

$$D_o[n] = G_a G_v[n] S[n] + G_q G_a G_v[n] q[n] - q[n] \tag{3.25}$$

where n is a discrete-time index. Substituting (3.25) into (3.24) and using q^2=1 because $q = \pm 1$ gives

$$G_v[n+1] = G_v[n] + 1 - G_q G_a G_v[n] - G_a G_v[n] S[n] q[n] \tag{3.26}$$

Take the expected value of both sides of (3.26). Since q is uncorrelated with the input signal $S[n]$, the last term in (3.26) approaches zero. Therefore

$$\overline{G_v[n+1]} = 1 + \overline{G_v[n]}(1 - G_a G_q) \tag{3.27}$$

If the mean of the variable gain $G_v[n]$ converges, then

$$\lim_{n\to\infty} \overline{G_v[n+1]} = \lim_{n\to\infty} \overline{G_v[n]} \tag{3.28}$$

Substituting (3.28) into (3.27) gives

$$\overline{G[\infty]} = \frac{1}{G_q G_a} \tag{3.29}$$

Therefore, as $n \to \infty$, the average path gain in steady state ($G_q G_a \overline{G}_v[\infty]$) is unity, and the average noise power added at the input is completely removed at the output. Finally, the average steady-state gain of the calibrated ADC path is

$$G_a \overline{G[\infty]} = \frac{1}{G_q} \tag{3.30}$$

G_q is a known parameter. Thus the ADC actual gain G_a can be recovered.

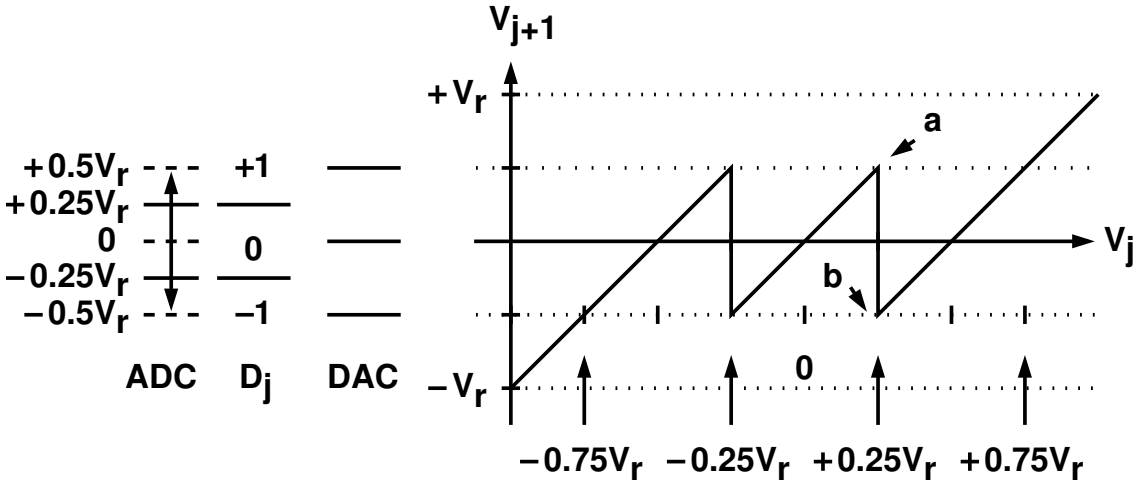


Figure 3.10: The conversion characteristic of the radix-2 1.5-bit SC pipeline stage.

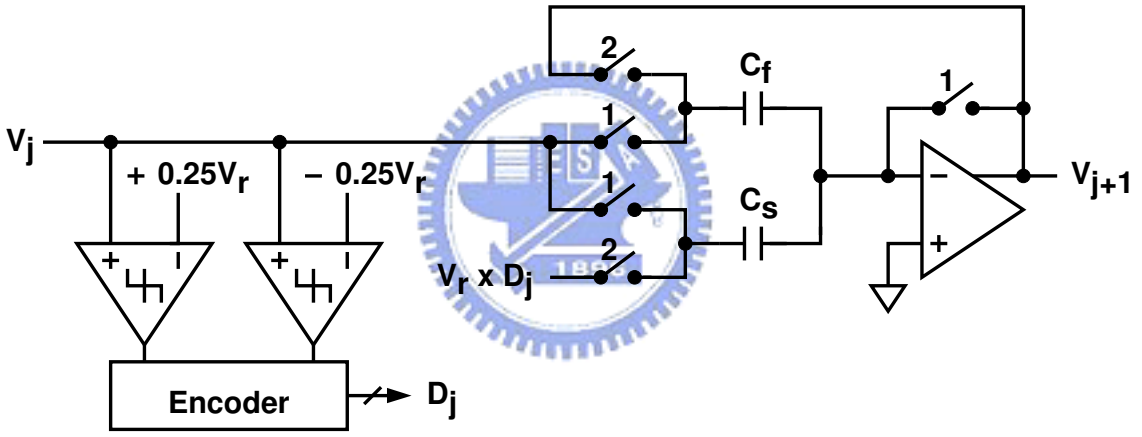


Figure 3.11: A radix-2 1.5-bit switched-capacitor (SC) pipeline stage.

3.4 A New Digital Background Calibration technique

Starting this section, it is assumed unless otherwise stated that the pipelined stage (or MDAC) used for discussion and illustration is always the structure of 1.5-bit stage with shared feedback capacitor to simplify our analysis. But the proposed analysis procedure is not restricted to this scope. It can be extended and applied on other structures. The conversion characteristic are shown in Fig. 3.10. The SC implementation of the 1.5-bit MDAC is shown in Fig. 3.11.

From Fig. 3.11, assuming the operational amplifier has a finite linear gain of A_0, and C_p denotes the parasitic capacitance associated with the opamp's negative input. The

interstage transfer function can be derived as follows: if $V_j > +\frac{1}{4}V_r$,

$$V_{j+1} = \hat{G}_j \times \left[V_j - V_r \cdot \frac{C_s}{C_s + C_f} \right] \tag{3.31}$$

If $-\frac{1}{4} < V_j < +\frac{1}{4}V_r$,

$$V_{j+1} = \hat{G}_j \times V_j \tag{3.32}$$

If $-\frac{1}{4}V_r < V_j$,

$$V_{j+1} = \hat{G}_j \times \left[V_j + V_r \cdot \frac{C_s}{C_s + C_f} \right] \tag{3.33}$$

with

$$\hat{G}_j = \frac{C_s}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{3.34}$$

If $A_0 \to \infty$ and $C_s = C_f$, the interstage transfer function can be written as

$$V_{j+1} = 2V_j \pm V_r \quad \text{or} \quad V_{j+1} = 2V_j \tag{3.35}$$

Equation 3.35 is the ideal transfer function for a 1.5-bit pipeline stage and is shown graphically in Fig. 2.18.

From (3.31) − (3.33), the finite gain A_0 of the interstage operational amplifier and capacitor mismatch between C_s and C_f can easily alter the transfer function from (3.35). Finite gain A_0 of the operational amplifier lowers the ideal interstage gain of two, as does a value of C_f greater than C_s. Finite gain A_0 also increases the effect of the parasitic capacitance C_p at the operational amplifier input nodes. This input capacitance can drain out charge during ϕ_2, leading to an incomplete transfer of the charge on C_s to C_f, thereby aggravating the deviation from ideal operation. Fig. 3.12(a) shows the residue transfer function when the interstage gain is less than two. The interstage gain can also be greater than two, which happens when capacitor C_s is greater than C_f. Fig. 3.12(b) shows the residue transfer function when the interstage gain is greater than two. Charge injection from sampling switches also contributes to the error in the interstage transfer function, but only adding an offset to the signal.

When a 1-bit/stage structure was adopted in pipelined ADCs, missing decision levels and missing codes have been reported [10] [13] [14]. Using a digital calibration algorithm, a stage is calibrated by tying its input to 0 V, so the residue output is below $+V_r$ or above

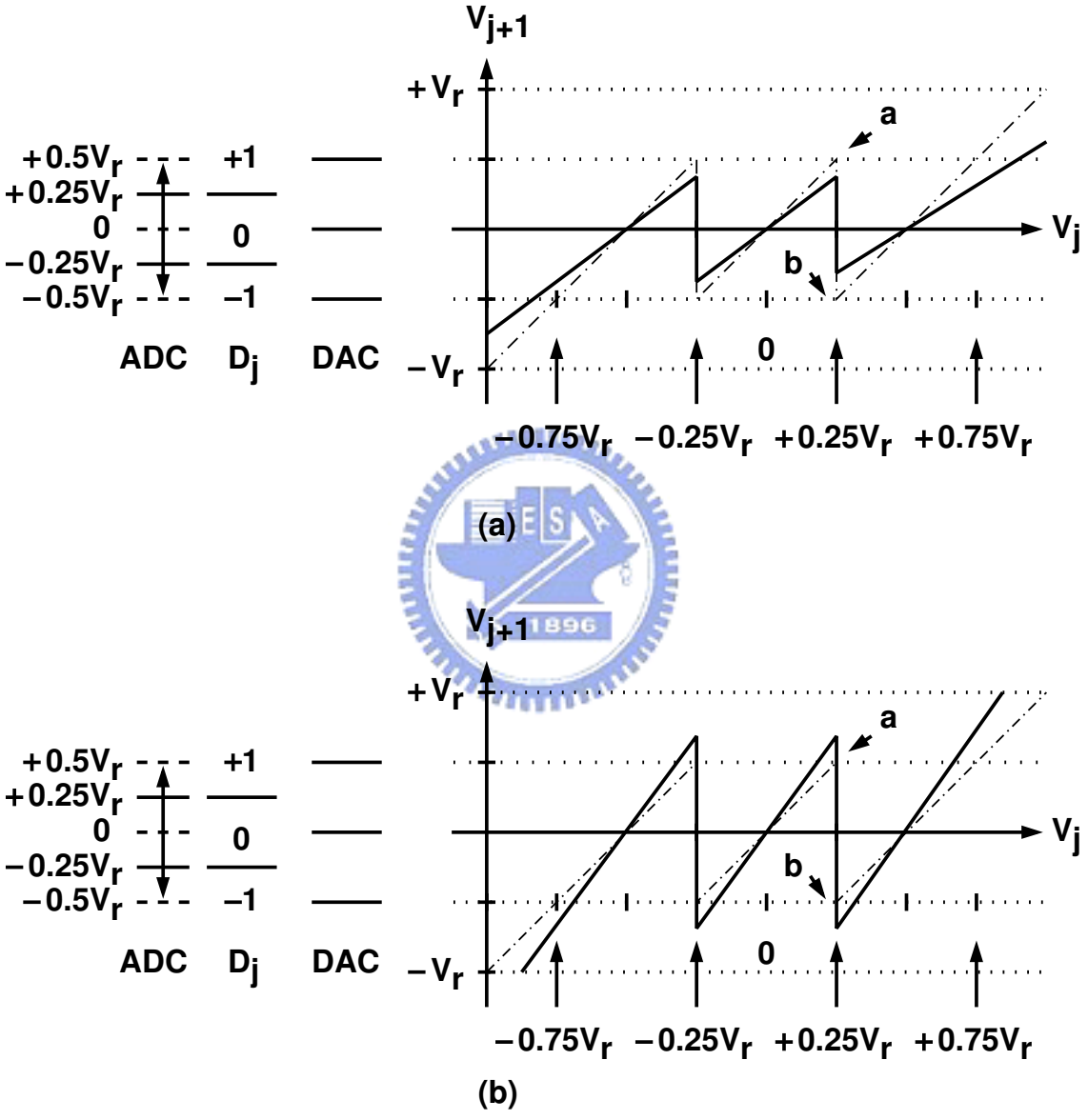


Figure 3.12: Nonideal transfer function. (a) Gain < 2. (b) Gain > 2.

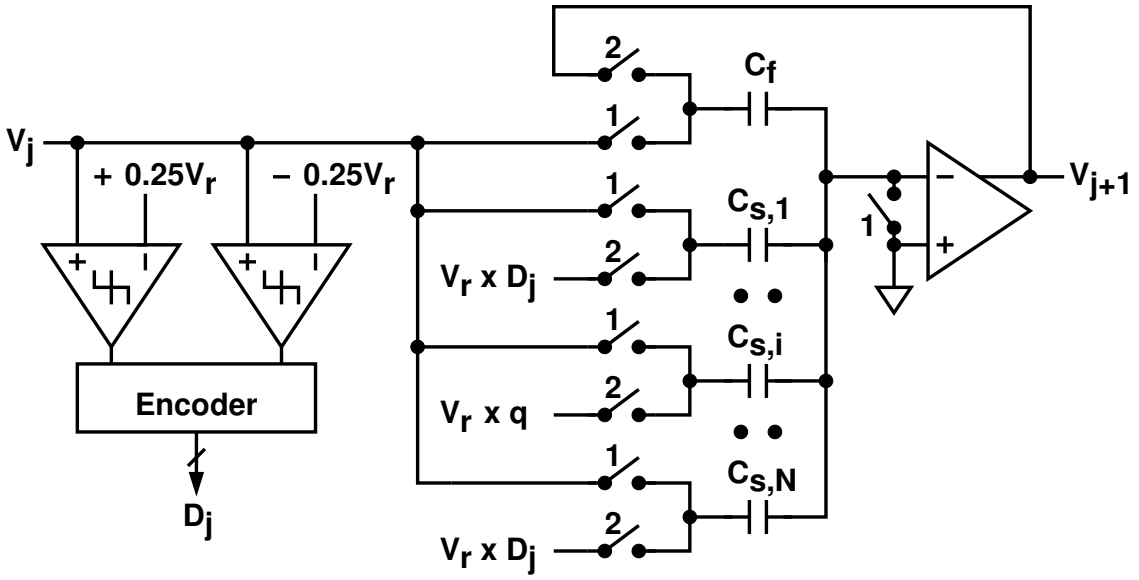


Figure 3.13: A radix-2 1.5-bit SC pipeline stage for background calibration.

$-V_r$. However, when the interstage gain is actually greater than two (possibly due to capacitor mismatch or uncompensated charge injection), the digital calibration fails, since the residue output of a stage is either above $+V_r$ or below $-V_r$ and so a missing decision level results. In order to prevent from saturating a residual output during calibration (and thus avoiding missing decision levels), the interstage gain must be less than two [10] [13] - Or better, introduce overrange stage into the pipeline ADC [14].

When a digital calibration algorithm is applied to a 1.5-bit/stage pipeline structure, only missing codes are likely to exist, not missing decision levels [11] [15]. If incorrect comparator decisions are made for residue inputs that are near the decision thresholds ($\pm\frac{1}{4}V_r$), then the next residue output will still be near $\pm\frac{1}{2}V_r$, rather than near or beyond saturation ($\pm V_r$). Therefore, the interstage gain variations, capacitor mismatch, and charge injection errors would not cause missing decision levels in a 1.5-bit/stage pipelined ADC.

As depicted in (2.29), the realized gain, $\hat{G}_j$, is a function of capacitor ratios as well as the opamp's dc voltage gain, A_0. Since A_0 is sensitive to temperature and supply voltage variations, $\hat{G}_j$ needs to be constantly calibrated in high-resolution ADCs.

The proposed background calibration scheme measures and quantizes $R_j(D_c)$ in (3.8) without interrupting the normal A/D conversion [16] [17] [18]. To achieve this, a modified

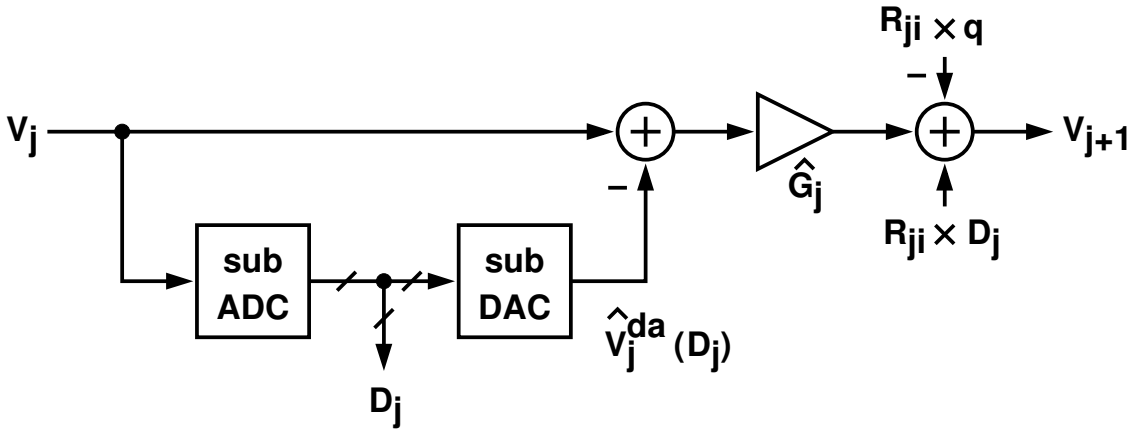


Figure 3.14: Model for the modified pipeline stage.

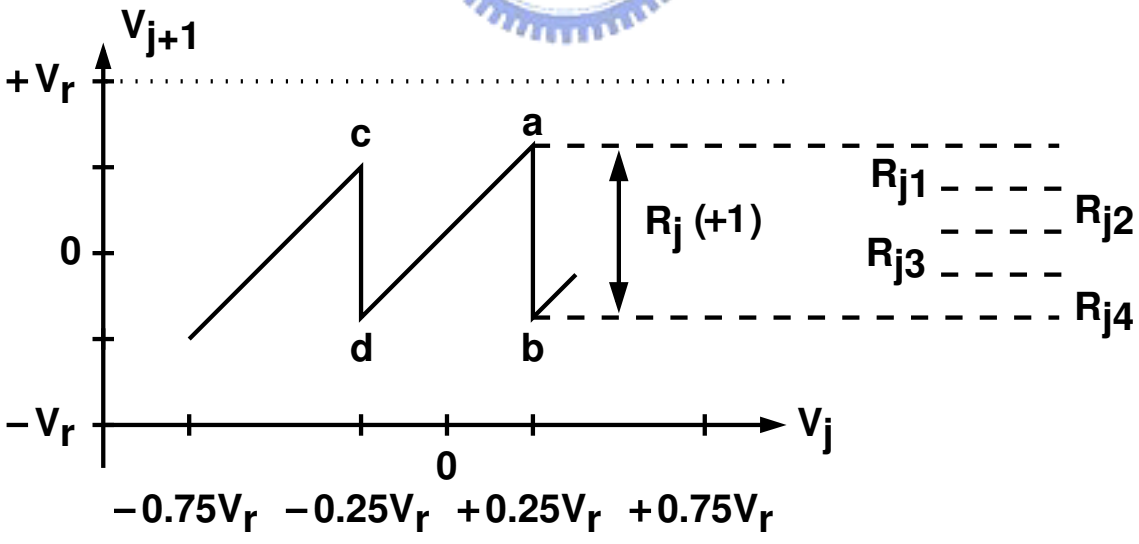


Figure 3.15: The relationship between R_{ji} and R_j.

SC pipeline stage as shown in Fig. 3.13 is used. The existing capacitor C_s is split into N fragments such that

$$C_s = C_{s,1} + C_{s,2} + \cdots + C_{s,N} \tag{3.36}$$

When the clock ϕ_1 is high, all capacitors C_s and C_f are connected together to sample the input signal V_j. When the clock ϕ_2 is high, all the C_s capacitors are connected to $D_j \cdot V_r$, except the $C_{s,i}$ capacitor which is connected to $q \cdot V_r$. The q signal is a digital binary-valued sequence generated from a pseudo random generator. To measure $R_j(+1)$, the value of q alternates between $+1$ and 0. To measure $R_j(-1)$, q alternates between -1 and 0. Fig. 3.14 shows the model for this modified pipeline stage. The model has the following transfer characteristic:

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) - V_j^{\mathrm{os}}\right] + R_{ji}(D_c) \cdot D_j - R_{ji}(D_c) \cdot q \tag{3.37}$$

where

$$R_{ji}(D_c) = \hat{G}_j \times D_c \times V_r \cdot \frac{C_{s,i}}{C_s + C_f} \tag{3.38}$$

The digital code D_c is either $+1$ or -1, depending on the polarity of q. The gain factor $\hat{G}_j$ is defined in (2.29). As depicted in Fig. 3.15, $R_{ji}(D_c)$ is a subsection of the transition step height in the V_{j+1} vs. V_j transfer function. The relationship between $R_{ji}(D_c)$ and $R_j(D_c)$ can be expressed as:

$$R_j(D_c) = \hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_c) = R_j(D_c - 1) + \sum_{i=1}^{N} R_{ji}(D_c) \tag{3.39}$$

Thus, $R_j(D_c)$ can be reconstructed from $R_{ji}(D_c)$ and used for digital output correction.

Fig. 3.16 shows the scheme for extracting $R_{ji}(D_c)$ in the background during normal A/D operation. The value of $R_{ji}(D_c)$ is estimated by quantizing V_{j+1} to obtain D_z using the succeeding z-ADC and then low-pass filtering the $q' \times D_z$ product in the digital domain, where q' has the same waveform pattern as q but alternates between $+1$ and -1. By multiplying both (3.1) and (3.37) with q' and applying time-domain averaging, an expression is obtained for the output of the low-pass filter (LPF), D_y. Suppose that q' has a mean value of 0 and is uncorrelated with V_j, then

$$\frac{G_z}{\hat{G}_z} \cdot D_y = -\overline{q'q} \times R_{ji}(D_c) = -\frac{1}{2} \times R_{ji}(D_c) \tag{3.40}$$

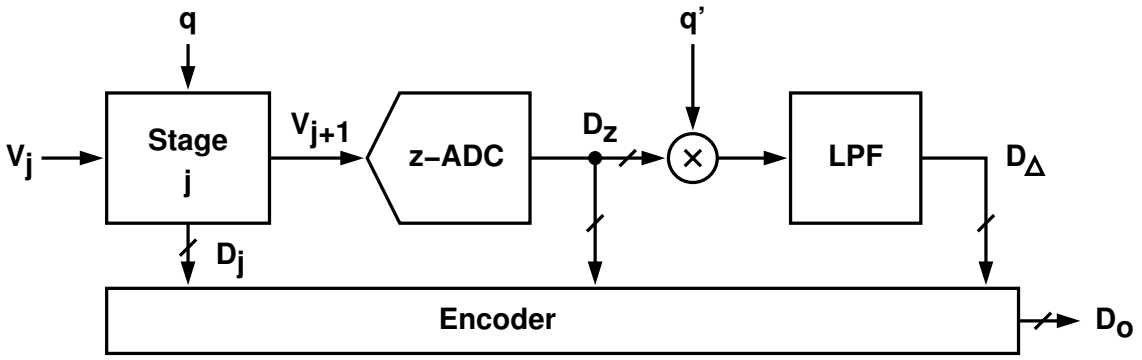


Figure 3.16: Background calibration block diagram.

The value of $T_j(D_c)$ can be computed by applying (3.40), (3.39) and (3.10). For normal A/D operation, the digital output D_o is derived from D_k, for $k = 1, \cdots, (j-1)$, and the D_{jz} of (3.13). Notably, the raw D_z digital output from the z-ADC contains the last two terms of (3.37) which must be subtracted from D_z before calculating D_{jz}. Once D_y of (3.40) is found, these two extra terms can be entirely removed from D_z. During the extraction of $R_{ji}(D_c)$, the time-domain averaging process also eliminates the effects of the z-ADC's offset, O_z, and quantization error, Q_z, as long as q and V_j remain uncorrelated.

The aforementioned procedures for calibration and A/D conversion can be conducted simultaneously without interrupting each other. The errors due to capacitor mismatches and finite opamp gains can all be corrected. As shown in Fig. 3.13, the only modification to a pipeline stage required by this calibration scheme is splitting the existing C_s capacitor. This modification does not increase the capacitance seen by the opamp's input, thus it does not degrade the operating speed of the original pipeline stage.

The injection of random sequence R_{ji} into the j-th stage also increases its required operating output range. As shown in Fig. 2.18, if V_j is limited to the range $\pm 0.5V_r$, then the additional output range is:

$$\Delta V_{j+1} = \pm \hat{G}_j \times V_r \cdot \frac{C_{s,i}}{C_s + C_f} \tag{3.41}$$

For a given opamp's output voltage range, the R_{ji} injection reduces the available signal range for the normal A/D operation, and hence decreases the achievable dynamic range of the ADC. This adverse impact can be mitigated by choosing a smaller value for C_s to reduce $\hat{G}_j$. Another approach is to split C_s into more capacitors, i.e., increasing N and

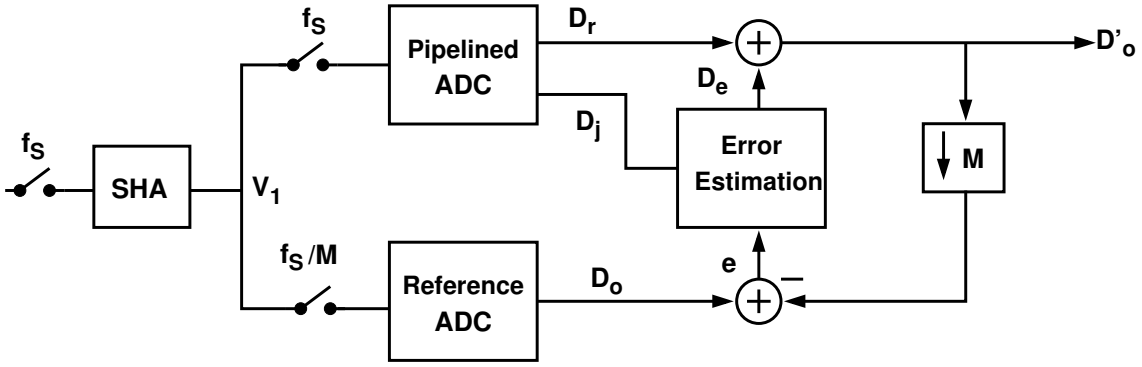


Figure 3.17: Background calibration using reference ADC.

resulting in smaller $C_{s,i}$, for $i = 1, \cdots, N$.

3.5 Other Background Calibration Techniques

In this Section, Three kinds of digital background calibration techniques published in literatures are introduced. The method of analysis developed in section 3 is applied to gain more insight into their techniques. The first method called "background calibration using reference ADC" treats analog impairments in a pipeline ADC in analogy to distortion in communication channels. The background calibration is achieved through a self-calibrated algorithmic ADC by the LMS algorithm. The second method called "DNC plus GEC background calibration" combines the DAC noise cancellation technique and the gain error correction technique to eliminate the mismatch of sub-DAC and interstage gain error. Finally, the method called "redundant residue mode for background calibration" randomly switches the pipeline stage between two distinct overlapping residue transfer functions to measure the residue distances (or the step heights) which are estimated by evaluating cumulative histograms of the digital conversion results.

3.5.1 Background Calibration Using Reference ADC

The calibration architecture is shown in Fig. 3.17. The system comprises of an input SHA, a pipelined ADC core, a self-calibrated algorithmic ADC, and a LMS error estimator. The pipelined ADC is fast but not very accurate and operates at a sampling rate of f_S. The

algorithmic ADC is slow but accurate and samples one out of every M SHA outputs V_1. Therefore, its sampling rate is f_S/M. The correspondent post-processing pipelined ADC output D_r subtracted from algorithmic ADC output D_o generates the error signal e. The LMS error estimator takes e and D_j from the uncalibrated pipeline stages as input and generates digital correction term D_e. The calibrated output $D_o^{'}$ is the sum of D_e and the raw output D_r of the pipelined ADC. Assume that the sub-DAC in each pipeline stage is linear and contains only gain error, i.e.,

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) - V_j^{os}\right] = \frac{G_z}{\hat{G}_z} \cdot D_z + O_z + Q_z \tag{3.42}$$

$$\hat{V}_j^{\mathrm{da}} = A_{R,j} \times D_j \times (1 + \varepsilon_j) = V_j^{\mathrm{da}} \times (1 + \varepsilon_j) \tag{3.43}$$

$$\hat{G}_j = G_j \times (1 + \delta_j) \tag{3.44}$$

where $A_{R,j}$ is the averaged value of the sub-DAC's LSB, ε_j is the sub-DAC gain error and δ_j is the interstage gain error in the j-th stage.

Neglecting quantization errors gives

$$\begin{aligned} V_1 &= D_r \\ &= \hat{V}_1^{\mathrm{da}} + \frac{\hat{V}_2^{\mathrm{da}}}{\hat{G}_1} + \frac{\hat{V}_3^{\mathrm{da}}}{\hat{G}_1\hat{G}_2} + \cdots + \frac{\hat{V}_P^{\mathrm{da}}}{\hat{G}_1\hat{G}_2\cdots\hat{G}_{P-1}} + O \\ &= \left[V_1^{\mathrm{da}} + \frac{V_2^{\mathrm{da}}}{G_1} + \frac{V_3^{\mathrm{da}}}{G_1G_2} + \cdots + \frac{V_P^{\mathrm{da}}}{G_1G_2\cdots G_{P-1}}\right] + h_0 + h_1 \cdot D_1 + h_2 \cdot D_2 + \cdots + h_P \cdot D_P \\ &= D_o + h_0 + h_1 \cdot D_1 + h_2 \cdot D_2 + \cdots + h_P \cdot D_P \\ &= D_o + D_e \end{aligned} \tag{3.45}$$

where D_e=$h_0 + h_1 \cdot D_1 + h_2 \cdot D_2 + \cdots + h_P \cdot D_P$,h_0 is the overall ADC offset,h_1=$A_{R,1} \cdot \varepsilon_1$, h_2=$A_{R,2} \cdot (\varepsilon_2 - \delta_1)/G_1$,$\cdots$, and h_P=$A_{R,P} \cdot (\varepsilon_P - \delta_1 - \delta_2, \cdots, -\delta_{P-1})/(G_1G_2\cdots G_{P-1})$.

Fig. 3.18 shows the LMS error estimator. The transfer function of LMS error estimator

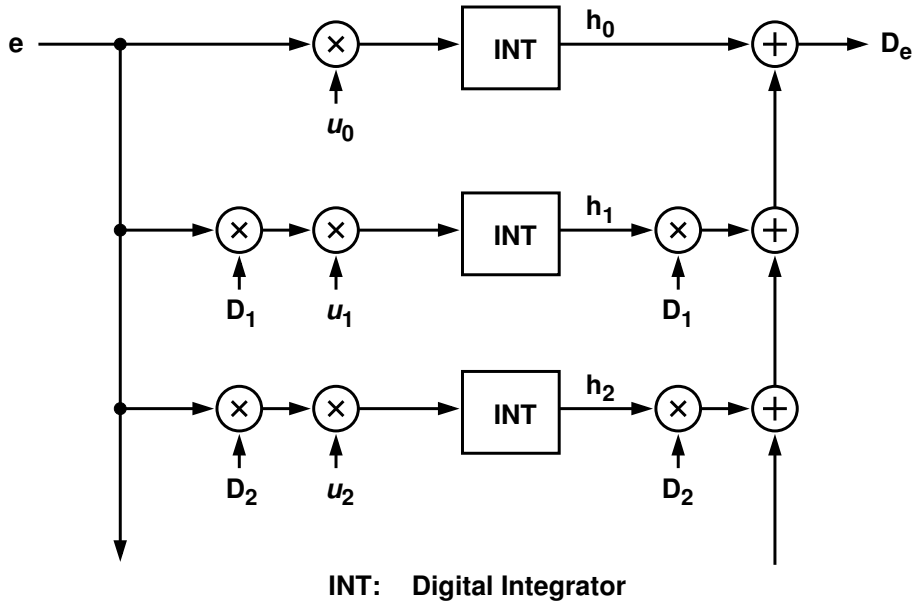


Figure 3.18: Least-Mean-Square (LMS) error estimator.

is written as:

$$
\begin{aligned}
D_e[k] &= \sum_{j=0}^{P} (h_j[m] \cdot D_j[k]) \\
D_o^{'}[k] &= D_r + D_e \\
e[m] &= D_o[m] - D_o^{'}[m] \\
h_j[m+1] &= h_j[m] + \mu_j \cdot e[m] \cdot D_j[m]
\end{aligned}
\tag{3.46}
$$

where μ_j is a scaling factor, it is used to balance the accuracy and convergent time.

The error e updates the parameters h's inside the LMS error estimator to minimize the mean-squared error (MSE), $E[e^2]$, which is the average value of e^2. Accumulator in the LMS error estimator and negative feedback combine to minimize the MSE, thus the calibrated output $D_o^{'}$ approaches the algorithmic output in steady state [37].

3.5.2 DNC Plus GEC Background Calibration

Pipelined ADCs tend to be sensitive to component mismatches in their internal sub-DACs. the component mismatches give rise to error, referred to as DAC noise, which is not attenuated or cancelled along the pipeline as are other types of noise. The j-th pipeline

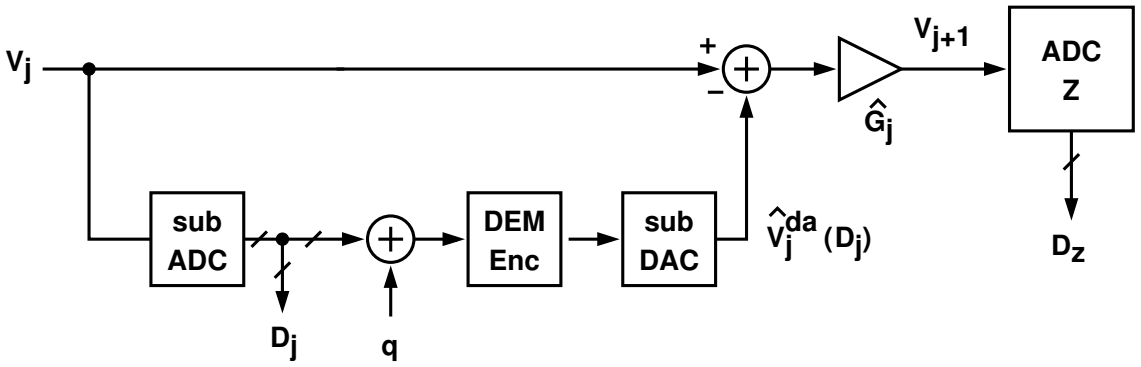


Figure 3.19: DNC plus GEC calibration of j-th stage .

stage followed by a ZADC under study for the DAC noise cancellation (DNC) and the gain error correction (GEC) is shown in Fig. 3.19. The pipeline stage consists of a sub-ADC, a SHA, a subtracter, a dynamic element matching (DEM) sub-DAC and a adder. The random signal q which serve the purpose of GEC is added to the sub-ADC output D_j by the adder. Before entering the sub-DAC, the combined output $(q+D_j)$ is encoded by the DEM encoder which is used to randomize the mismatches of the sub-DAC. DEM improves the SFDR of a pipelined ADC by converting harmonic distortion into white noise which is uncorrelated with the other signals in the pipelined ADC. However, the DAC noise increases the overall noise floor of the pipelined ADC, so SFDR is improved at the expense of SNR [48] [49]. Fortunately, the DEM encoder causes the noise to have a predictable structure. The DNC technique improves the SNR by exploiting this structure to estimate the DAC noise and remove it from the ADC output [43]. The sub-DAC comprises of several parallel 1-bit DACs. The segmented tree-structured DEM digital encoder consists of k switching blocks which randomly permutes the connections between the thermometer encoded input bits and the switched-capacitor 1-bit DACs. Each switching block generates a corresponding switching sequence, a_k, which is restricted to the values -1, 0,and 1. The value of a_k is made by a bit sequence from a pseudorandom number generator and the switching block input. Each pseudorandom sequence is designed to well approximate a white zero-mean random process that is uncorrelated with all other signals in the ADC. The DNC is similar to spread spectrum modulation of several dc "message signals"; The unknown constants, Δ_k's which depend only on the mismatch errors, are modulated by the known a_k's "spreading codes". A DNC logic implements a simple dig-

ital spread-spectrum "receiver", or correlator, that estimates the Δ_k terms and use them to cancel the sub-DAC noise in the pipelined ADC digital output. The nonideal interstage gain $\hat{G}_j$ results in imperfect cancellation of the flash ADC quantization noise at the pipelined ADC output. The GEC technique adds a pseudorandom two-level signal to the output of sub-ADC to obtain an estimate of the interstage gain $\hat{G}_j$. Given the gain error estimate, correction could be performed by multiplying the digitized residue and adding the resulting correction signal to the overall ADC output. The DNC plus GEC technique can be described in the mathematical description as bellow.

A sub-DAC with non-ideal terms can be expressed as:

$$\hat{V}_j^{\mathrm{da}}(D_{in}) = A_{R,j} \times \sum_k [a_k \cdot (1 + \Delta_k)] = V_j^{\mathrm{da}}(D_{in}) + A_{R,j} \times \sum_k (a_k \cdot \Delta_k) \tag{3.47}$$

$$V_j^{\mathrm{da}}(D_{in}) = A_{R,j} \times \sum_k a_k = A_{R,j} \times D_{in} \tag{3.48}$$

where $a_k \in \{-1, 0, +1\}$, $D_{in} = \sum_k a_k$, k is the number of the switching blocks, Δ_k are mismatch terms and $\sum_k \Delta_k = 0$. The DEM encoder is used to randomize a_k and Δ_I.

The V_j can be written as:

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j + q) - V_j^{os}\right] = \frac{G_z}{\hat{G}_z} \cdot D_z + O_z + Q_z \tag{3.49}$$

where $q \in \{-1, 0, 1\}$ is a random sequence. Thus, we have

$$\hat{G}_j \times \left[V_j - V_j^{\mathrm{da}}(D_j) - A_{R,j} \times \sum_k (a_k \cdot \Delta_k) - A_{R,j} \times q \times (1 + \Delta_I) - V_j^{os}\right] = \frac{G_z}{\hat{G}_z} \cdot D_z + O_z + Q_z \tag{3.50}$$

Applying correlation and averaging with a_k and q gives

$$E[a_k \times V_{j+1}] = -\hat{G}_j \times A_{R,j} \times \Delta_k \times E[a_k^2] = \frac{G_z}{\hat{G}_z} \cdot E[a_k \times D_z] \tag{3.51}$$

$$E[q \times V_{j+1}] = -\hat{G}_j \times A_{R,j} \times E[q^2] = \frac{G_z}{\hat{G}_z} \cdot E[q \times D_z] \tag{3.52}$$

From (3.51), the sub-DAC's mismatch terms,$\hat{G}_j A_{R,j} \Delta_k$ for all k, are extracted from $E[a_k \times D_z]$. Once $\hat{G}_j A_{R,j} \Delta_k$ are found, the $\hat{G}_j A_{R,j} \sum_k (a_k \cdot \Delta_k)$ error term can be eliminated from D_z. $\hat{G}_j A_{R,j}$ term is extracted from $E[q \times D_z]$. The $\hat{G}_j A_{R,j}$ represents the transition height

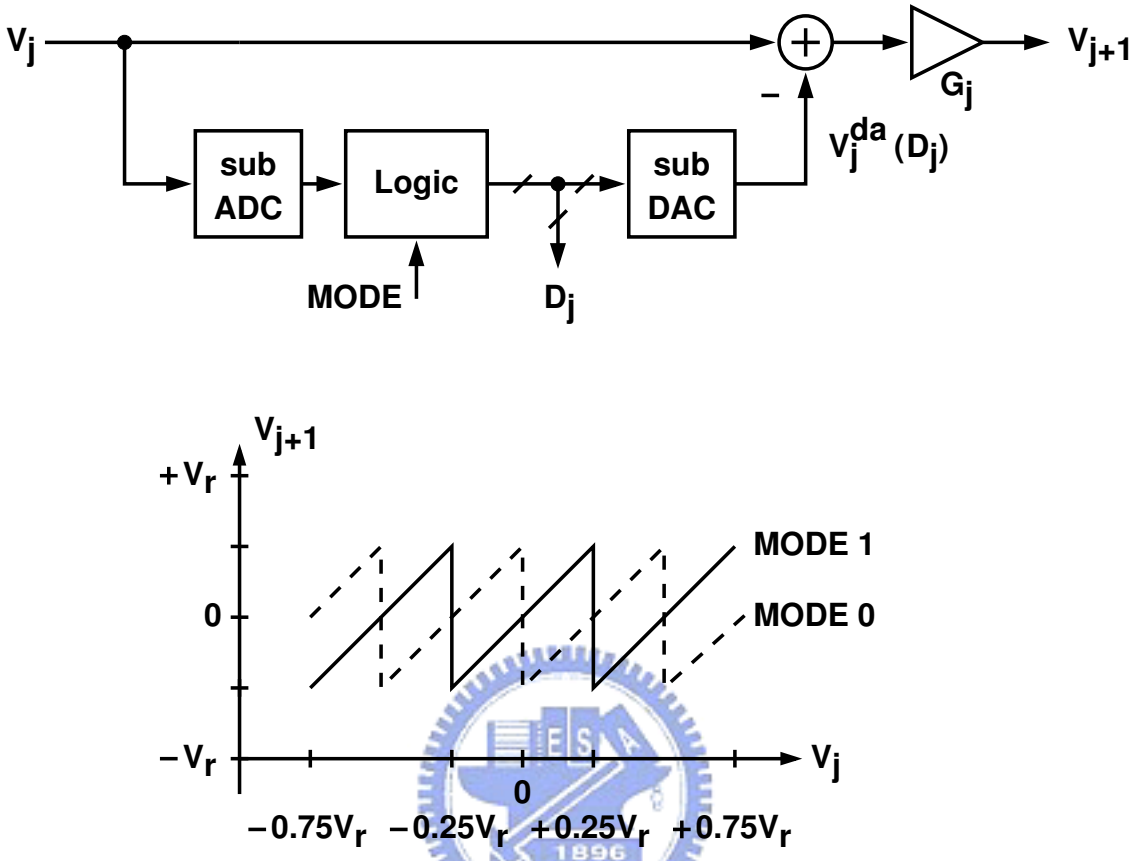


Figure 3.20: Pipeline stage with two-residue transfer characteristics.

in the V_{j+1} vs. V_j transfer curve. Once $\hat{G}_j A_{R,j}$ is obtained, the ADC's digital output can be corrected to eliminate error caused by the gain error of $\hat{G}_j$ and $A_{R,j}$. Note that the injection of the random sequence q increases the required V_{j+1} range.

3.5.3 Redundant Residue Mode for Background Calibration

One of the key ingredients for this background calibration technique is the usage of two different sets of sub-ADC and sub-DAC characteristics for the j-th stage as shown in Fig. 3.20. Through the addition of a simple digital block and the extra redundant residue mode in the sub-ADC and sub-DAC, the j-th stage can switch between two distinct overlapping residue transfer functions. In principal, the two residues of Fig. 3.20 can be used interchangeably and would yield identical conversion results in the case of ideal stage operation [46]. If the sub-DAC is ideal, from Fig. 3.21, it is apparent that the step height h_1

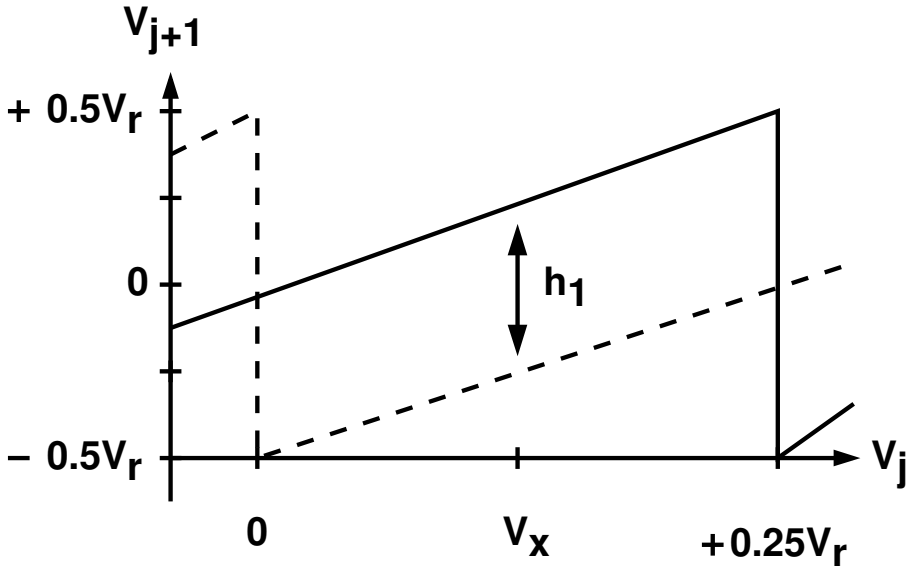


Figure 3.21: Ideal residue segment detail.

is equal to $R_j(D_c)/2$.

If it were possible to process constant input voltage using both characteristics, the distances would be directly determined from the individual back-end conversion results. However, to avoid the need for constant inputs, the authors developed a statistic based estimation technique to be exactly approximate to h_1 [46]. The distance estimation process is based on evaluating cumulative histograms of the digital back-end conversion results. Refer to Fig. 3.22. A binary random number generator switches the two residue modes with equal probability and independent of the sample value for each input sample to the j-th stage. The cumulative histogram count $CH(r_0)$ is found by counting the number of samples for $V_a \leq V_j \leq V_b$ and $V_{j+1} \leq r_0$ in MODE 0. Similarly $CH(r_1)$ can be found in MODE 1. With the random modulation in progress, and after processing a large number of samples, the top bins $CH(r_1)$ are evaluated and compared to the bottom bins $CH(r_0)$. From the close match, $CH(r_1) = CH(r_0)$, the distance estimate H_1 is obtained. Let $H_1 = r_1 - r_0$, H_1 is an asymptotically unbiased estimate of the true residue distance h_1. For increasingly large sample sizes, the estimate approaches the true value.

Fig. 3.23 shows the pipeline stage with non-linear transfer characteristics. This situation may occur when the low gain opamp or open-loop structure is adopted in the design of the MDAC. But from multiple h_i measurements at different V_j locations, it is possible

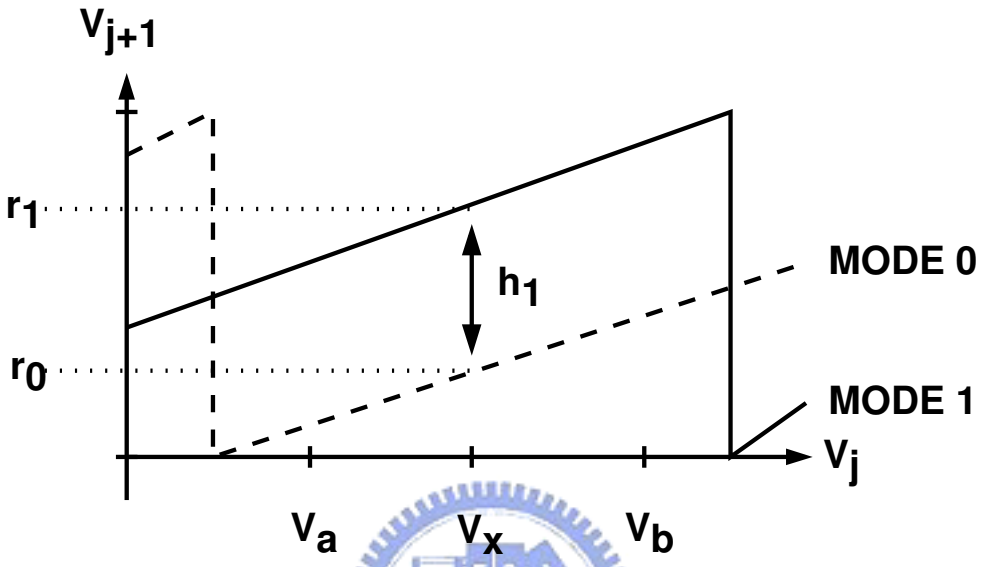


Figure 3.22: Distance estimate from closest cumulative count.

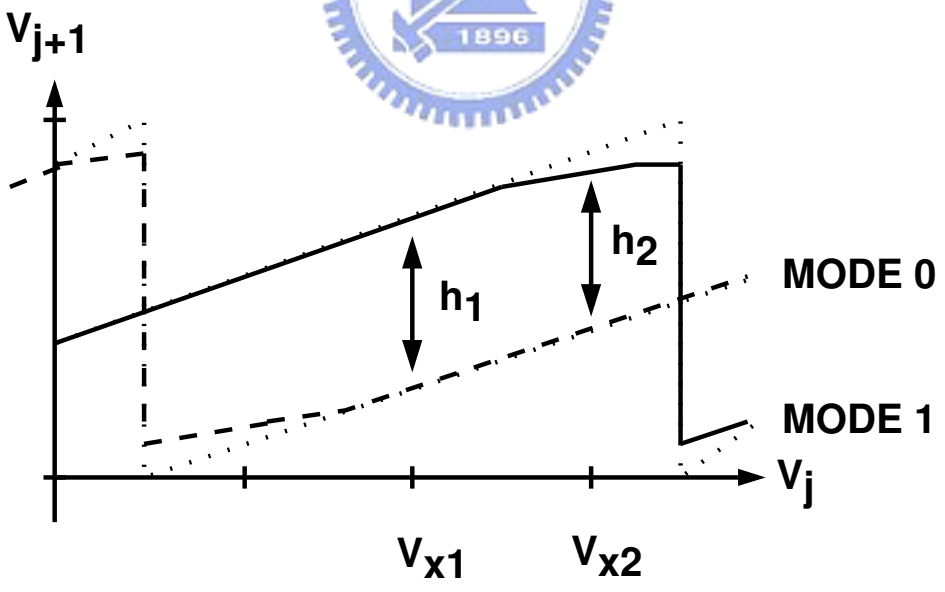


Figure 3.23: Non-linear residue segment details.

to estimate the non-linear terms of the V_{j+1} v.s. V_j transfer characteristic [46]. However, the calibration effectiveness depends on the statistic behavior of the V_j.

3.6 Summary

In this chapter, several existing self-calibration techniques have been discussed. Among those techniques, digital self-calibration techniques which subtract the code errors in the digital domain, do not require sophisticated analog circuits but put extra burden on the digital part and require either additional stages or additional resolution in each calibrated stage to overcome the loss in effective resolution produced by digital truncation errors during calibration. Although the cost of the calibration is increased complexity in the digital domain, but the scaling law predicted by Moore makes the ADC architecture with digital calibration more compatible with the characteristics of modern CMOS processes.

Foreground digital calibration techniques are popular in the past ten years and successfully applied on several commercial products. However, No solid mathematical foundation is provided to support these techniques. The theory of digital calibration based on the generalized mathematical description described in Chapter 2 is introduced to bridge the gap. Foreground calibrations are limited to the extent that the normal operation has to be interrupted to start the calibration cycle. Foreground calibrations further suffer from the lack of tracking capability, therefore it is sensitive to temperature, supply voltage drift and device aging. Background calibration addresses this limitation and enables a converter to run calibration nonstop to track device and environment variations.

The correlation-based background calibration techniques have drawn attention since most of the calibration procedures can be carried out in the digital domain. To calibrate a pipeline stage, the correlation-based schemes all involve introducing a known random term into the stage, and then measuring the stage's transfer characteristic by extracting the random term from the ADC digital output. Three published background calibration techniques have been demonstrated here and their weaknesses and benefits also are discussed in details.

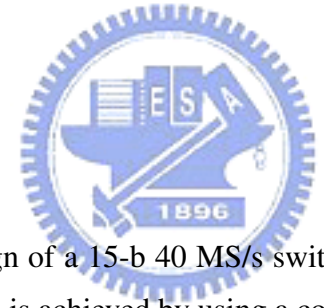
From the theory of digital calibration, the conversion result is expressed in terms of weights or digital values. By dividing the step heights of MDAC in a pipeline stage and

injecting a random signal into the MDAC, the knowledge of weights can be recovered without interrupting the normal analog-to-digital operation.

Chapter 4

A 15-b 40 MS/s CMOS Pipelined ADC

4.1 Introduction



This chapter presents the design of a 15-b 40 MS/s switched-capacitor CMOS pipelined A/D converter. High resolution is achieved by using a correlation-based background calibration technique that can continuously monitor the transfer characteristics of the critical pipeline stages and correct the digital output codes accordingly, which is based on the calibration technique described in the previous chapters. The calibration can correct errors associated with capacitor mismatches and finite opamp gains.

All issues related to designing switch-capacitor blocks such as amplifier design,capacitance values and the sub-ADC comparators are addressed in this Chapter as well. Section 4.2 describes the architecture used in the prototype. Section 4.2.2 contains the stage gain requirement for these uncalibrated pipeline stages. Section 4.3.1 describes the design of the operational amplifier. Section 4.3.2 presents the design of the sample-and-hold amplifier. The comparators used in the sub-ADC are shown in Section 4.3.3. Section 4.4 discusses the design of digital blocks. Experimental Results are shown in Section 4.5. Finally, the summary is given in Section 4.6.

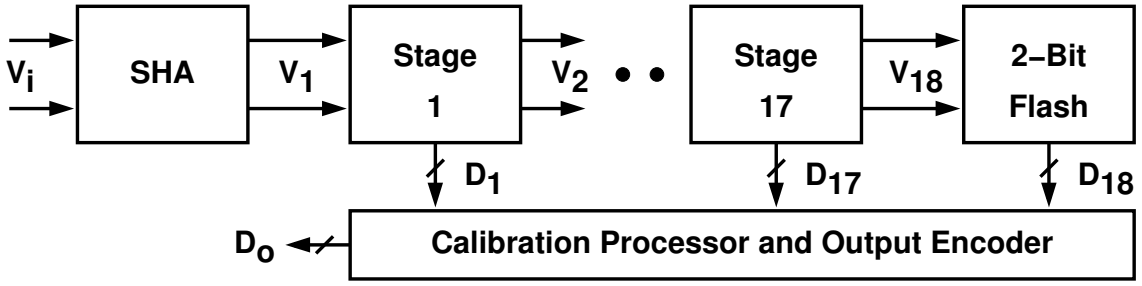


Figure 4.1: Block diagram of the ADC prototype.

4.2 Architecture

Fig. 4.1 shows the block diagram of the prototype. The entire design can be divided into analog part and digital part. The analog part consists of a front-end sample-and-hold amplifier (SHA), 17 radix-2 1.5-bit SC pipeline stages and a final 2-bit flash stage. The entire analog signal path is fully differential so as to minimize the effects of common-mode noises and to suppress even-order distortions. The digital part comprises of calibration processor and output encoder.

Only the first five pipeline stages, i.e. from the 1st stage to the 5th stage, were designed to employ the proposed background calibration scheme. In each of these stages, hereafter called "the calibrated stage", its C_s capacitor is split into four equal parts, i.e. $N = 4$ in (3.36). The remaining uncalibrated pipeline stages, from the 6th stage to the 18th stage, constitute a 14-bit ADC with approximately 11-bit effective resolution. The resolution is limited mainly by the matching accuracy of the MIM capacitors.

All voltage references are externally supplied. The system clock is generated by frequency-dividing an external clock by two to ensure a duty cycle of 50%.

4.2.1 Pipeline Stage Design

In Chapter 2, two possible ways to implement the 1.5-bit MDAC are shown in Fig. 2.15 and Fig. 2.17 respectively. The first architecture, referred to as a conventional SHA, requires three equal-value capacitors (two for sampling and one for integrating). The

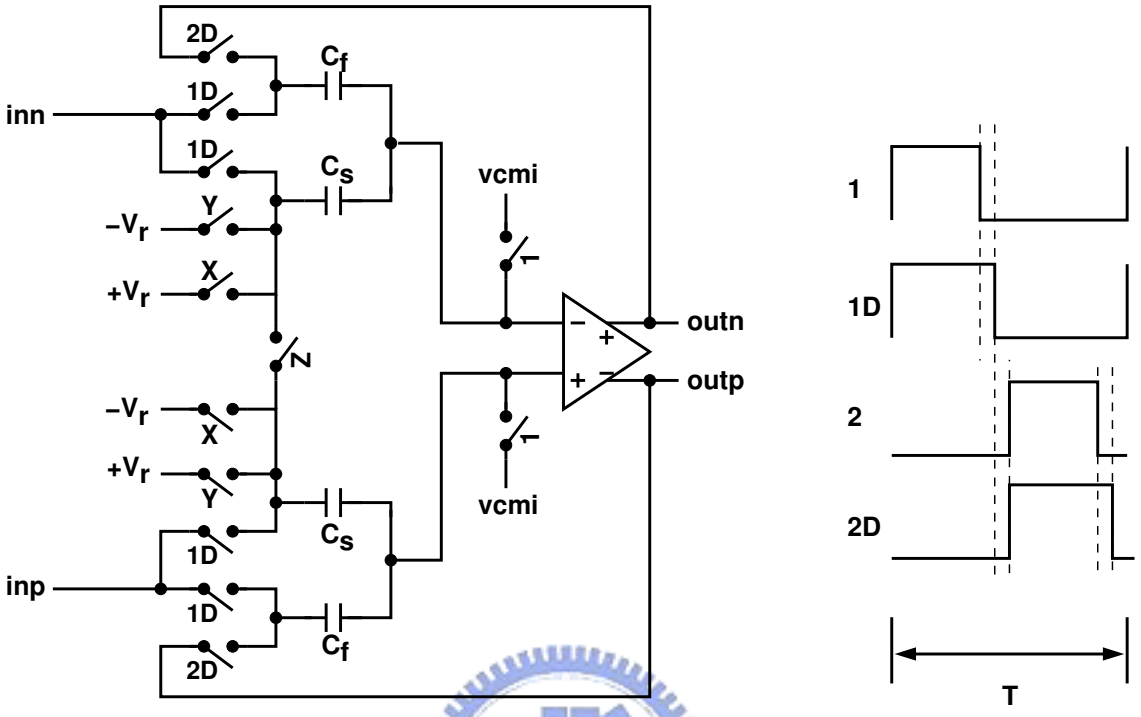


Figure 4.2: (a) Schematic of the 1.5-bit MDAC; (b) non-overlapping clock phases.

feedback factor β for this MDAC in its closed loop configuration is given by

$$\beta = \frac{C_f}{2C_s + C_f + C_p} \tag{4.1}$$

where C_p denotes the parasitic capacitance associated with the opamp's negative input. Note that the reciprocal of the feedback factor β is not equal to the closed-loop gain of the stage, although in some circumstance they might be close. The second architecture, referred to as a 1.5-bit MDAC with shared feedback capacitor, requires two equal value capacitors (one for sampling and the other for sampling and integrating). The feedback factor is

$$\beta = \frac{C_f}{C_s + C_f + C_p} \tag{4.2}$$

The feedback factor of the first architecture is ideally $1/3$, while the ideal β of the second architecture is $1/2$, neglecting parasitic capacitance C_p. Ideally the later needs only $2/3$ of the GBW to achieve the same closed-loop bandwidth, which is important because the MDAC speed limits the conversion rate of the ADC. Thus, the 1.5-bit MDAC with shared feedback capacitor is chosen in our design. The fully differential implementation

of the resulting MDAC is shown in Fig. 4.2, which consists of an opamp, four equal sized capacitors and 13 switches.

ϕ_1 and ϕ_2 are two non-overlapping clocks, while ϕ_{1D} is a delayed version of ϕ_1 but still non-overlapping with ϕ_2. When ϕ_1 and ϕ_{1D} are high, analog inputs are acquired by all four capacitors to perform the bottom-plate sampling scheme and the operational amplifier is being reset at the same time. At the end of ϕ_1, the four input switches open later than the sampling switch S1 to minimize the charge injection from the input switches to the sampling capacitors C_s and C_f, because the top plate of the capacitors are in a high impedance state.

During ϕ_2 (charge transfer phase), the integrating capacitors C_f are connected to the opamp output and the sampling capacitors C_s are connected to each other or the positive reference $+V_r$ or the negative reference $-V_r$ depending on the state of digital inputs X,Y and Z.

The implementation of the calibrated 1.5-bit MDAC is almost the same as the one shown in Fig. 4.2 except that the C_s is divided into four equal parts. Four types of extra control signals came from the digital blocks serve to control and manage the calibration process. "$Calibration\_Enable$" signals select one of the five calibrated stages to be calibrated. "$Cap\_selection$" signals enable one of the four split capacitors to enter into calibration state in the calibrated stage. "$Rj\_selection$" signal finds the value of $R_j(+1)$ or $R_j(-1)$ of the split capacitor under calibration. The "q" signal adds pseudorandom noise into the MDAC.

4.2.2 Stage Accuracy Requirement

In the pipeline architecture, the accuracy requirement on each stage is different because the stage resolution decreases down the pipeline with the per-stage resolution. For example, for a 15-bit ADC with the net resolution of 1-bit stage, the first stage has to meet 15-bit accuracy requirement. However, the next stage need only deliver a 14-bit accuracy. Lower stage means that design constraint are more relaxed, and in terms of pipeline stage design this translates into relaxed requirements on interstage amplifier gain accuracy, sub-DAC accuracy, and thermal noise.

First, consider that the ADC comprises of P stages of the 1.5-bit MDAC with shared feedback capacitor and the total resolution is N bits. For the accuracy requirement of the stage j, the combined gain error in the interstage amplification should be less than $1/2^{N-j}$ of the full scale input range ($2V_r$) where $N-j$ is the resolution of the next stage. The output V_{j+1} can be written as:

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j)\right] \tag{4.3}$$

and

$$\hat{G}_j = (\frac{C_s + C_f}{C_f}) \cdot (1 - e^{-\frac{t}{\tau}}) \cdot \frac{1}{1 + \frac{1}{A_0} \cdot \frac{1}{\beta}} \tag{4.4}$$

where β is defined in (4.2), A_0 is the opamp finite gain, and the exponential term in the second bracket is the settling time of the single pole opamp (τ is the time constant for the SC gain block configuration). Refer to Fig. 3.6, the step height between a and b or c and d can be written as

$$\hat{H} = \hat{G}_j \times \frac{V_r}{2} \tag{4.5}$$

and the ideal step height is

$$H = 2 \times \frac{V_r}{2} \tag{4.6}$$

For no missing codes, the difference ε between the ideal step height and actual step height should be less than the 1 LSB of the next stage. However, each pipeline stage is specified such that all accumulated errors at the end of the conversion process remain inside 0.5 LSB. Although 1 LSB is enough for monotonicity, 0.5 LSB is specified to be a safe design. In this case, the error term can be found from

$$\varepsilon = H - \hat{H} = \left(2 - (\frac{C_s + C_f}{C_f}) \cdot (1 - e^{-\frac{t}{\tau}}) \cdot \frac{1}{1 + \frac{1}{A_0} \cdot \frac{1}{\beta}}\right) \times \frac{V_r}{2} \leq \frac{2V_r}{2^{N-j}} \cdot \frac{1}{2} \tag{4.7}$$

Ignore high-order error terms, and let $C_f = (1 + \Delta)C_s$

$$\varepsilon \approx \frac{\Delta}{2} + e^{-\frac{t}{\tau}} + \frac{1}{A_0 \cdot \beta} < \frac{1}{2^{N-j}} \tag{4.8}$$

From above, in order to achieve an N-bit linearity, requirements on opamp DC gain and capacitor matching can be determined. For opamp gain, with a conservative design, the gain is given by

$$\frac{1}{A_0 \cdot \beta} \leq \frac{1}{2^{N-j}} \cdot \frac{1}{4} \tag{4.9}$$

$$A_0 \geq 2^{N-j+2} \cdot \frac{C_s + C_f + C_p}{C_f} \tag{4.10}$$

Note that the error budget for the amplifier gain error is 0.125 LSB of the remaining stages. If C_p is ignored, the above expression becomes 2^{N-j+3}. For the same reason, the opamp output has to settle to $1/2^{N-j} \cdot \frac{1}{2} = 1/2^{N-j+1}$ (the error budget for the settling error is 0.25 LSB of the remaining stages), and for the single pole system, the required number of time constants can be found from

$$(N - j + 1) \cdot \tau \cdot \ln(2.0) \leq T_{settle} \tag{4.11}$$

where T_{settle} is the allowed settling time, usually $75\% \sim 90\%$ of a half clock period, depending on the design style. Usually, the margin is left for the non-overlapping of $\phi 1$ and $\phi 2$, the required slewing time of slew-rate limited opamp design and the data transferred time between sub-ADC and sub-DAC,respectively.

Let the error budget for the capacitor mismatch error be 0.125 LSB of the remaining stages. The matching requirement on the capacitors is determined as follow:

$$\Delta < \frac{1}{2^{N-j}} \cdot \frac{1}{4} \cdot 2 = \frac{1}{2^{N-j+1}} \tag{4.12}$$

This sets the matching requirement on C_s and C_f of each stage.

However, in the modern CMOS process, the matching property of capacitors can be up to 10$\sim$ 11 bits. In this case of N being smaller than 11, the gain errors induced from capacitor mismatches can be ignored. Thus, the error budgets for the remaining terms are both 0.25 LSB. Then, the requirement for the opamp gain is expressed as

$$A_0 \geq 2^{N-j+1} \cdot \frac{C_s + C_f + C_p}{C_f} \tag{4.13}$$

and the constraint for the settling time constant is the same as (4.11).

Besides the above deterministic error components, the other error source is the random component whose dominant source is thermal noise. Considering that the main sources of thermal noise are the ON-resistances of the switches and the opamps of the MDACs and of the frontend Sample-and-Hold. Assuming that thermal noise is additive Gaussian, the power of the thermal noise is then described by its variance, and the variance should be much less than the LSB to maintain sufficiently high SNR for the pipeline stage with

N-bit accuracy requirement. The root mean square (rms) value of the total thermal noise referred to the input of the stage j, $\sigma_{total,j}$, is given by

$$\sigma_{total,j} = \sqrt{V_{no,j}^2 + \frac{V_{no,j+1}^2}{2} + \frac{V_{no,j+2}^2}{2^2} + \cdots} \tag{4.14}$$

where $V_{no,j}$ are the output referred rms noise contributions of the 1.5-bit MDAC. The output referred noise introduced by each MDAC can be expressed approximately as

$$V_{no,j}^2 \cong \frac{k \cdot T_c \cdot \Theta_S}{C_s + C_f} \tag{4.15}$$

and the noise factor

$$\Theta_S = (1 + \frac{R_{ON} \cdot C_s^2 + R_a \cdot (C_s + C_f)^2}{\tau \cdot (C_s + C_f)}) \tag{4.16}$$

where R_{ON} and R_a are,respectively, the ON-resistance of the CMOS switches (X,Y,or Z in Fig. 4.2) during the residue amplification phase and the equivalent noise resistance of the amplifier [50]. Assume that the amplifier in MDAC is a operational transconductance amplifier (OTA) and its transconductance is g_m. Since the transistors of the differential pair will typically operate in strong inversion, the equivalent noise resistance is approximately $R_a \cong 2 \cdot \gamma \cdot /3/g_m$, where γ represents the excess noise factor. For some commonly used OTA topologies and with appropriate sizing of the current sources, γ values are assumed to be between 2 and 3.

Relation (4.16) was obtained for a single-ended MDAC. In a full-differential MDAC, the capacitors noise contribution is doubled, while the amplifier noise remains unchanged. Therefore, the noise factor Θ_D for a full-differential MDAC becomes:

$$\Theta_D = 2 \cdot (1 + \frac{R_{ON} \cdot C_s^2 + \frac{R_a}{2} \cdot (C_s + C_f)^2}{\tau \cdot (C_s + C_f)}) \tag{4.17}$$

4.3 Analog Circuits

This section introduces the circuit design of analog building blocks used in the prototyped ADC. General analysis and design techniques of each building block are overviewed. These analog circuits include the operational amplifier in the MDAC, the sample-and-hold amplifier and comparators in the sub-ADC.

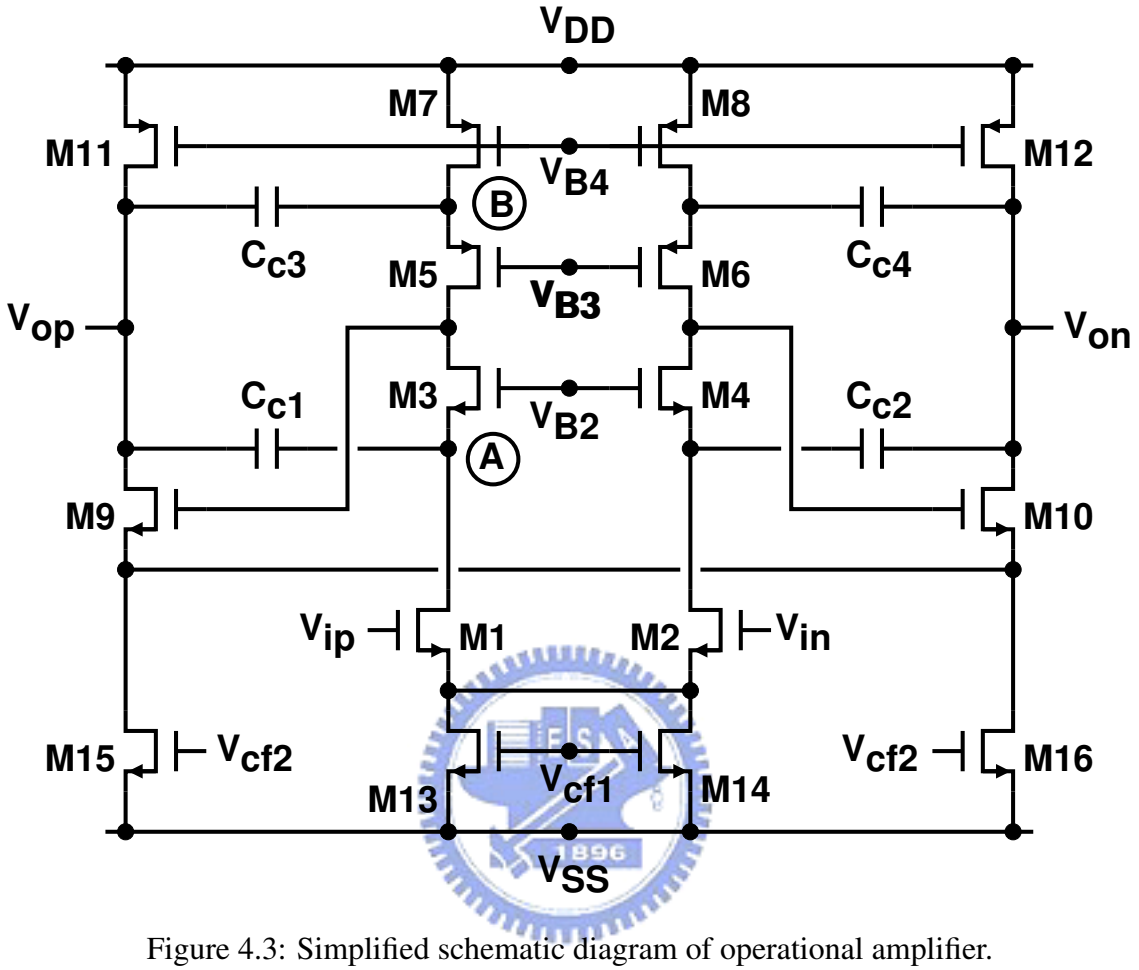


Figure 4.3: Simplified schematic diagram of operational amplifier.

4.3.1 Operational Amplifier

Fig. 4.3 shows the topology of the opamps used in the SHA and all pipeline stages. Compared to a single-stage amplifier, a two-stage amplifier can achieve much higher gain, while easily meeting the output swing requirement. The fully differential two-stage configuration consists of a telescopic first stage followed by a common-source second stage [35] [28]. The overall dc voltage gain is more than 90 dB. Although the calibration technique described in the previous section eliminates the adverse impact of the opamp's finite voltage gain, nonlinear properties in the opamp's dc transfer function are error sources that can not be removed. Thus, the opamp is preferred to have a large gain.

With a 2.5 V supply, the opamp can provide a differential output voltage range as large as 2.8 V_{pp}. The opamp's output range must be large enough to cover the entire range of

V_{j+1} in (2.26), plus the extra residue resulted from the offsets of the comparators, plus the additional range for the R_{ji} injection. From (3.41), the required output range in this design with $N = 4$ is 25% more than that of a conventional design.

The opamp's signal path consists of only n-channel devices to maximize the operating speed [51]. However, to ensure closed-loop stability, the parasitic pole created by the second stage in a two-stage amplifier needs to be pushed beyond its closed-loop bandwidth. The parasitic pole is located approximately at g_{m9}/C_{LT}, where g_{m9} is the transconductance of M9, and C_{LT} is the effective load capacitance. The standard miller compensation has a pole-splitting effect, which moves one pole to a lower frequency and the other to a high frequency. The two-stage amplifier employs the hybrid cascoded compensation scheme, which creates two real poles, two complex poles at a higher frequency, and three zeros. This scheme of compensation yields a higher amplifier bandwidth compared to the standard Miller and conventional cascoded compensation techniques at the cost of more complex design procedure for the settling behavior of the amplifier. This implies that ,for practical designs, design equations will be necessary for computer optimizations [52]. The two capacitors, C_{c1} and C_{c2}, serve as cascoded Miller compensation and generate zero pairs located at $\pm\sqrt{\frac{C_{c1}\cdot C_A}{g_{m3}\cdot g_{m1}}}$, where C_A is the total capacitance at node A, g_{m3} is the transconductance of M3, and g_{m1} is the transconductance of M1 [53] [54]. However, this compensation scheme may suffer from insufficient gain margin due to the peaking of the magnitude response beyond the unity-gain bandwidth, caused by the non-dominant poles [54]. The addition of C_{c3} and C_{c4} generates a left-half-plane zero at $\frac{g_{m5}}{C_{c3}+C_B}$ that can be carefully placed to avoid peaking, where C_B is the total capacitance at node B, and g_{m5} is the transconductance of M5. [55] [56]. The entire compensation method is similar to the nested cascoded Miller compensation [57].

The required number of time constants of the MDAC is governed by (4.11). The minimum required open-loop unity-gain bandwidth f_{unity} of the opamp is found from

$$f_{unity} \geq \frac{1}{\beta} \times \frac{1}{2\pi\tau} = \frac{C_s + C_f + C_p}{C_f} \times \frac{1}{2\pi\tau} \tag{4.18}$$

In the first pipeline stage, the opamp dissipates 22.5 mW of power and achieves a unity-gain frequency of 650 MHz with $C_s = C_f = 2$ pF and an external load of 4 pF.

Two separate switched-capacitor common-mode feedback circuits are used to generate

Table 4.1: Transistor dimensions of the opamp used in the first MDAC.

Transistor	Width(μm)/Length(μm)
M1, M2	240/0.5
M3, M4	200/0.3
M5, M6	200/0.5
M7, M8	300/1.2
M9, M10	800/0.25
M11, M12	1300/1.2
M13, M14	300/1.2
M15, M16	1300/1.2

control voltage V_{cf1} and V_{cf2} for the first and second stages of the opamp [51] [58]. The input common-mode voltage is set to 0.95 V, and the output common-mode voltage is set to 1.35 V.

To reduce power dissipation, device scaling along the pipeline has been adopted. However, due to the limited design time, the scaling strategy used is far from optimal. In this prototype, the SHA and the first five pipeline stages use identical opamps. The opamps and capacitors are reduced by half in the next six stages. Another scaling by half is applied to the remaining stages. The transistor dimensions of the opamp used in the first MDAC are listed in Table 4.1.

4.3.2 Sample-and-Hold Amplifier

The architecture employed for the front-end SHA is shown in Fig. 4.4. The SHA impacts some very key characteristics of the ADC such as SFDR and noise floor. The configuration adopts a conventional flip-around configuration, which acquires the input on the sampling capacitors during the track phase, and flips the same capacitors to the output during the hold phase. Theoretically, the opamp does not have to provide charge to the sampling capacitor, both slewing speed and feedback factor are enhanced. The feedback factor β_{SHA}, which measures the portion of the output signal being fed back to the amplifier's input is shown below

$$\beta_{SHA} = \frac{C_{s1}}{C_{s1} + C_p} \tag{4.19}$$

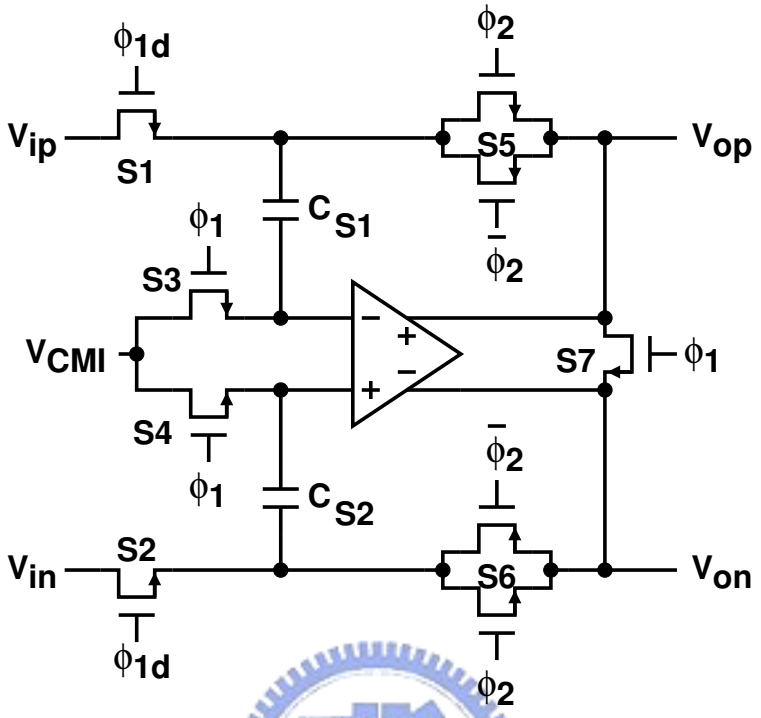


Figure 4.4: Simplified schematic diagram of sample-and-hold amplifier (SHA).

where C_p denotes the parasitic capacitance associated with the opamp's negative input. Neglecting C_p, the ideal β_{SHA} of the flip around SHA is 1. If the opamp is ideal, the transfer curve is a straight line with a slope of 1. However, the finite dc gain of an opamp introduces a gain error in the actual transfer curve. The transfer function can be expressed as:

$$\frac{V_{op}}{V_{ip}} = \frac{1}{1 + \frac{1}{A_{SHA}} \cdot \frac{1}{\beta_{SHA}}} \tag{4.20}$$

where A_{SHA} is the DC gain of the SHA. Therefore, if the product of $A_{SHA}\beta_{SHA}$ which represents the loop gain of the feedback system is low, the gain will be less than 1.

The maximum achievable performance of a SHA is usually limited by the transient behavior of the close-loop SHA in the hold mode, distortion caused by the finite dc gain of the opamp and the sampling switch, and noise contributed mainly from the sampling switch and the clock jitter. For the input SHA, the gain error can be tolerated if the ADC does not require absolute scale. This can be represented as having a linear gain block in front of a ideal SHA. If the gain is *linear*, then it does not introduce any error except reducing the signal amplitude by a small portion. Despite this, at the end of the sampling

phase the output voltage still needs to be settled down to its desired voltage value. The settling behavior of a SHA may have two parts: slew-rate limit and linear settling. The slew-rate limit prolongs the total settling time, thus it reduces the maximum achievable clock rate. The required settling time of the SHA is still governed by (4.11) and the error of the front-end SHA must be smaller than 0.5 LSB to achieve N bit linearity (assume a slew-rate limited SHA). Thus, the minimum required open-loop unity-gain bandwidth $f_{unity-SHA}$ of the SHA is written as

$$f_{unity-SHA} \geq \frac{1}{\beta_{SHA}} \times \frac{1}{2\pi\tau_{SHA}} = \frac{C_{s1}+C_p}{C_{s1}} \times \frac{(N+1)\cdot ln(2.0)}{2\pi \cdot T_{settle}} \tag{4.21}$$

where T_{settle} is the allowed settling time. The SNR limitation from jitter can be calculated via the classic formula [59]

$$SNR_{jitter} = -20 \cdot \log_{10}(2\pi f_{IN}\sigma_{jitter}) \tag{4.22}$$

where f_{IN} is the frequency of the input signal, and σ_{jitter} is the RMS timing error of the sampling clock. This effect increases proportionally with signal frequency.

In a actual SHA, the transfer curve is not a straight line but rather a line with some curvatures which mean harmonic distortions in the actual circuit behavior. In the hold phase, the negative feedback around the SHA reduces its distortion by the loop gain, $A_{SHA}\beta_{SHA}$, to obtain a highly linear transfer characteristic. In an ADC, the non-ideal transfer curve in a SHA will induce large integral non-linearity error causing harmonic distortion and intermodulation distortion. Therefore, for the ADC to achieve resolution greater than 15 bits, the SHA may require a high dc opamp gain more than 90 dB. The opamp circuit in the SHA is the same type used in the MDAC.

When compared with other SHA topologies, there are several advantages of the flip-around architecture [51]. One of them is low power consumption. Since its β is high, the required closed-loop bandwidth of a flip-around SHA ideally is the same as its native GBW. This results in significant power saving. Another advantage is low noise power from the amplifier. During the hold phase, the input-referred noise power of the SHA is

$$V_{no,SHA}^2 = \frac{S_a \cdot G_n^2 \cdot BW_n}{G_{sig}^2} \tag{4.23}$$

where S_a is the input-referred noise power density of the amplifier, G_n is the noise gain, G_{sig} is the signal gain, and BW_n is the noise bandwidth. Assuming the amplifier with its noise dominated by the input transistors, its input-referred noise power density is $S_a = 4kT_c \cdot R_a = 16kT_c/(3 \cdot g_m)$. Assuming that the amplifier can be model as a single-pole system, the noise bandwidth is $BW_n = (\pi \cdot g_m \cdot \beta)/(2 \cdot C_{LT})$, where C_{LT} is the effective load capacitance. The noise gain is $1/\beta$, and the signal gain is 1. Thus, (4.23) can be rewritten as

$$V_{no,SHA}^2 = \frac{8\pi \cdot kT_c}{3\beta \cdot C_{LT}} \tag{4.24}$$

(4.24) shows that the high β of the flip-around SHA provides significant reduction in the noise power of the amplifier.

This one has the additional advantage of having no-gain error due to capacitor mismatch, since the sampling capacitor are also used as holding capacitors. The flip-around SHA has one main drawback. If the signal common mode V_{sig_cm} differs from the SHA's output common mode V_{out_cm}, then during the hold phase, the common mode feedback circuit of the SHA forces the output to be V_{out_cm} and causes the amplifier's input common mode to take a step $\Delta V_{in\_vcm} = V_{out\_cm} - V_{sig\_cm}$. Therefore, to accommodate various signal common modes and handle single-ended signals, the amplifier needs a large input common-mode compliance.

The flip-around architecture was chosen for the noise advantage and fast settling behavior. To employ the bottom-plate sampling technique, S1 and S2 switches are turned off after S3 and S4 have been turned off. In high-speed low-voltage designs, the MOS switch's on-resistance is a significant limitation on the tracking speed and the settling time. Moreover, the on-resistance has a nonlinear voltage dependence, which leads to distortion when tracking continuous time signal. To reduce the on-resistance, a voltage higher than the supply can be used to control the switches. In a typical realization, the switch transistor gate voltage is locally boosted with a charge pump circuit. It is also possible to have the switch gate voltage track the switch input voltage with some offset. This yields two advantages. First, the circuit's long-term reliability is improved since the gate-drain voltage of the switch transistor never exceeds the supply voltage. Second, the on-resistance becomes almost constant, which significantly reduces the distortion.

The gate-controlling clocks for S1 and S2 are generated from two constant-V_{GS} boot-

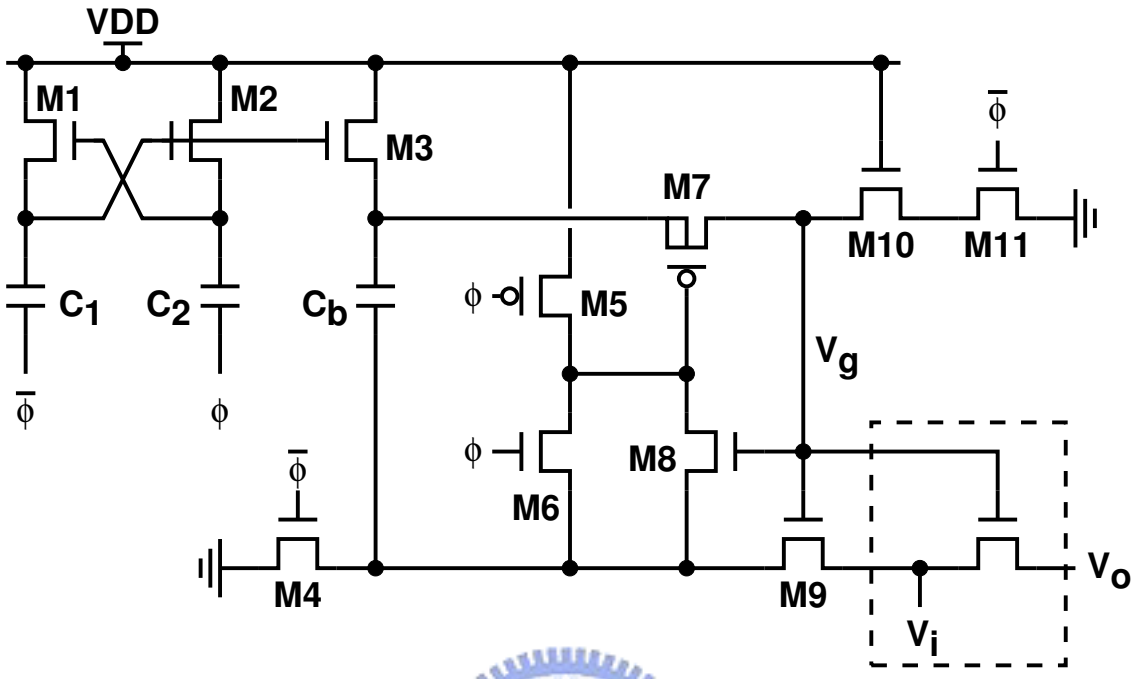


Figure 4.5: Boostrapped clock generator for SHA's input sampling switches [1].

strapped clock generators [60] [1]. Fig. 4.5 shows a simplified bootstrapped circuit, which was designed to observe device reliability consideration. This switch is conceptually a single NMOS transistor, as shown in Fig. 4.4. The use of constant-V_{GS} clocks work to reduce the device sizes of S1 and S2 and also decrease the distortion caused by charge injection from the switches. The values of the input sampling capacitors C_{S1} and C_{S2} are both 4 pF.

4.3.3 Comparator

In the pipeline architecture, the error from a large comparator offset in the sub-ADC of each pipeline stage can be easily compensated with digital correction. For a 1.5-bit per-stage resolution, the comparator offset up to $\pm V_r/4$ can be corrected. In other words, with a reference voltage of 1V, comparator offset up to $\pm 250mV$ can be tolerated. This allows the use of no-static-power dissipating dynamic comparators without any continuous time pre-amplification. However, Because of the injection of R_{ji} random signal, The comparator offset up to $\pm V_r/8$ can be tolerated through digital correction in the prototype.

Therefore, the comparator used in all pipeline stage consists of a preamplifier, followed by a regenerative latch. In typical dynamic cross-couple inverter latches, process variations and mismatches can result in large offset voltage. The preamplifier used here ensures that the offset requirement still can be met.

The preamplifier is capable of accepting a fully differential input, and comparing it to a differential reference without the benefit of an input sampling network. The preamplifier topology is shown in Fig. 4.6. The output of the circuit are given by the difference between the two current I_{op} and I_{on}:

$$I_{out} = \frac{-g_m}{2}((V_{in} - V_{RN}) + (V_{RP} - V_{ip})) - \frac{-g_m}{2}((V_{RN} - V_{in}) + (V_{ip} - V_{RP})) \qquad (4.25)$$

If the bias currents match exactly, the output current is proportional to $(V_{ip} - V_{in}) - (V_{RP} - V_{RN})$. A more standard topology is shown in Fig. 4.7 [61]. The differential output current is identical to (4.25), but there is a significant difference between the two. Assume that a full-scale input signal is being compared to the maximum reference. For the I_{out} to be proportional to the differential input voltage, the absolute differential input $|V_{id}| = \left|V_{ip} - V_{in}\right|$ must be smaller than $\sqrt{2}(V_{gs} - V_T)$, where $V_{gs} - V_T$ is the bias for the input devices. For example, if the devices in the differential pair were biased with a $V_{gs}-V_T$=150mV, and 450mV was to be applied across the input terminals, then one side of the differential pair would be completely turned off, while the other would carry all of the tail current. However, considering the tradeoff between bandwidth and power, $V_{gs} - V_T$ should be kept as small as possible, without, however, being biased into subthreshold region, to achieve the highest bandwidth for the smallest power. Note that $g_m = \frac{2I_{ss}}{V_{gs}-V_T}$, where I_{ss} is the current of transistor M5 or M6. Therefore, making the $V_{gs} - V_T$ as large as the full scale input range adversely affects either the speed or the power consumption of the circuit and also reduces the available headroom of the input stage.

However, the design in Fig. 4.6 does not have this problem. Since V_{ip} and V_{RP} are one pair, and V_{in} is paired with V_{RN}, both differential pair will be operated well within their linear range of operation even when both the input and reference are near their maximum values. When the input deviates greatly from the reference voltage, the differential pair will become unbalance. This is however less important because a comparator needs to work well in the range when the signal is near the crossing point with the reference. To

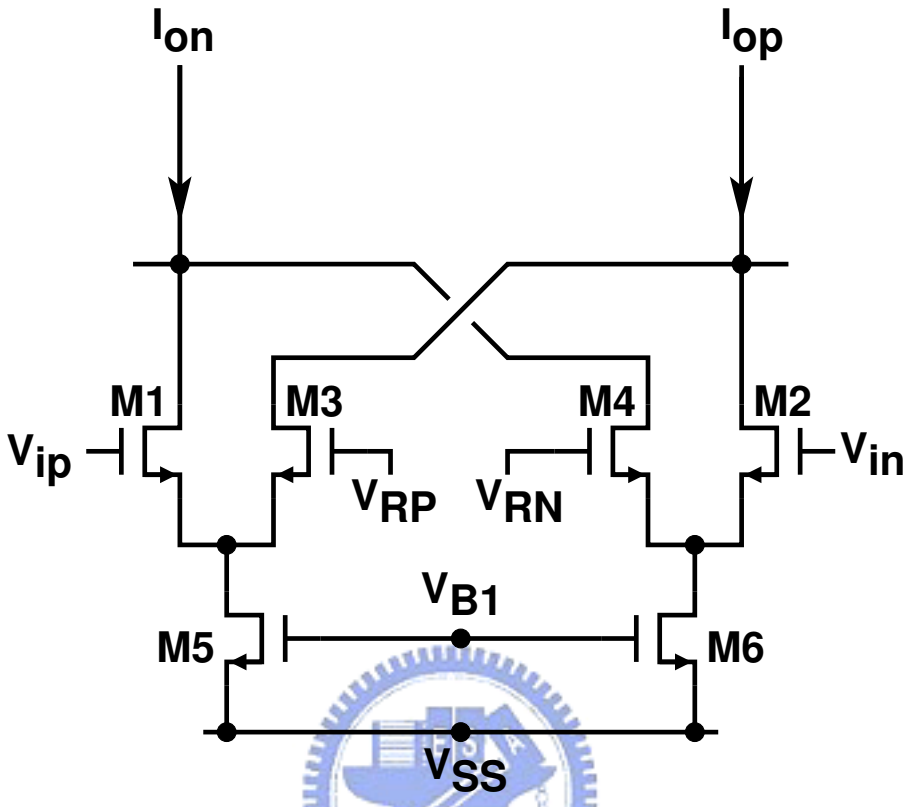


Figure 4.6: Schematic diagram of preamplifier 1.

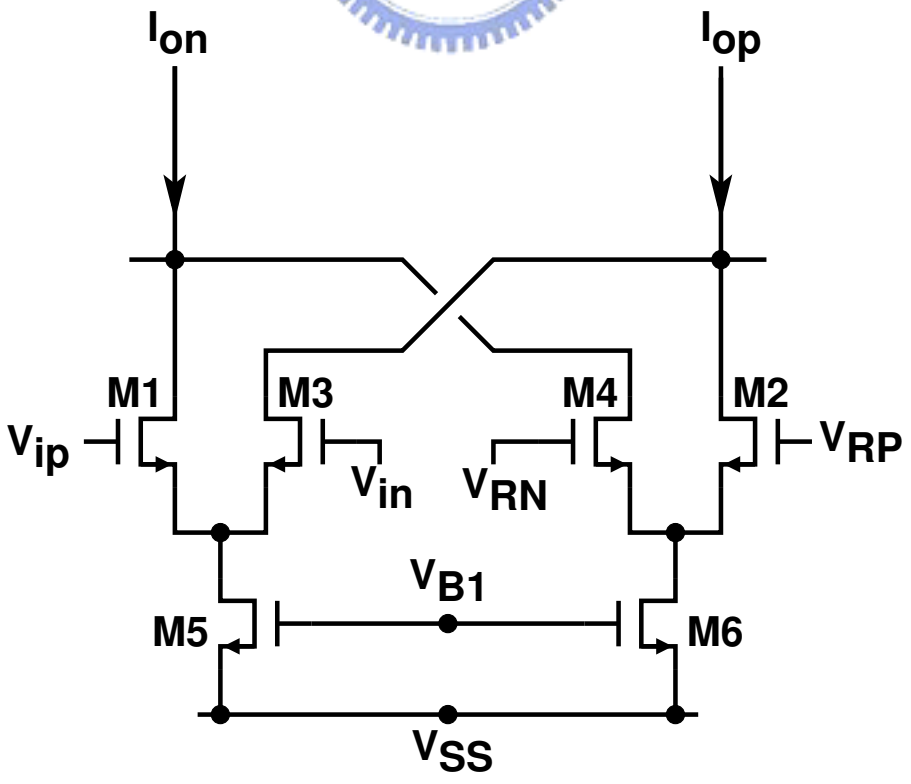


Figure 4.7: Schematic diagram of preamplifier 2.

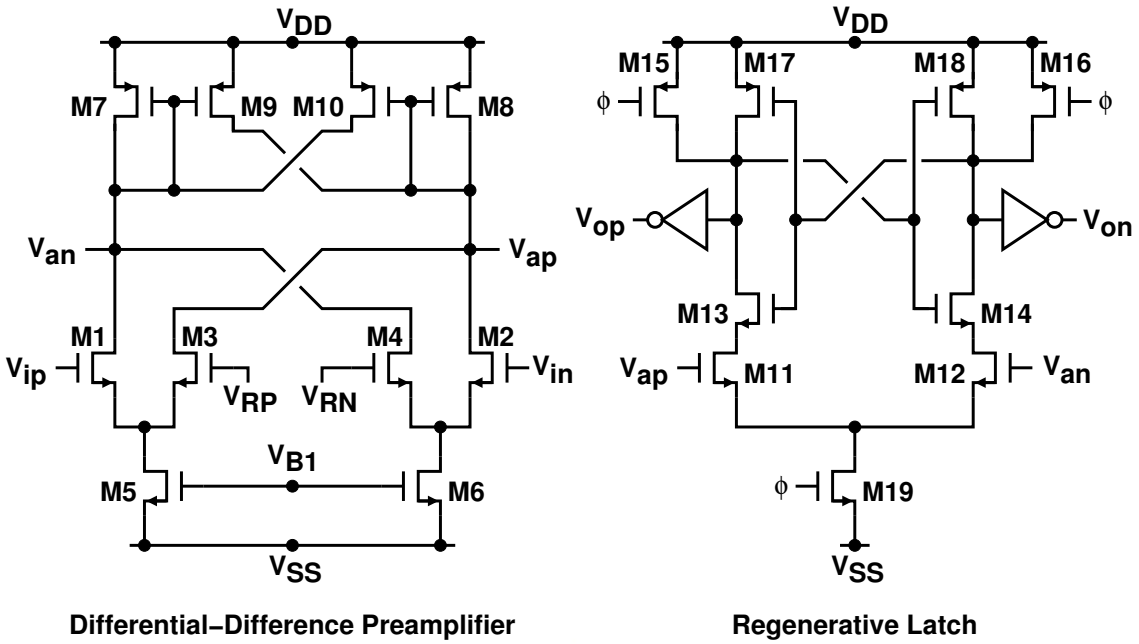


Figure 4.8: Schematic diagram of comparator.

prevent the common mode difference between input signal and reference voltage from translating into differential signal, the common-mode voltage of input signal should be set to $\frac{V_{RP}+V_{RN}}{2}$.

The overall comparator topology is shown in Fig. 4.8. The comparator consists of a differential-difference preamplifier with a voltage gain of 9, followed by a regenerative latch. The active loads formed by transistors M7,M8,M9 and M10 acts as a current-to-voltage converter with a high output impedance. The dynamic comparator uses a set of two NNOS transistors, M11 and M12, operating in the active region and connected to the preamplifier. These transistors can be regarded as a voltage-to-current translator which generates the current difference. As the upper cross-coupled latch (M13,M14,M17 and M18) has positive regeneration when the control signal ϕ goes high, the drain currents of the active switching NMOS are steered to reach the final state determined by the current difference.

In Fig. 3.13, the threshold voltages for the two comparators are $\pm 0.25V_r$. In this design, the differential V_r is 1.4 V, and its common-mode voltage is 1.35 V. Thus, the corresponding reference voltages for V_{RP} and V_{RN} in Fig. 4.8 are 1.525 V and 1.175 V

Table 4.2: Transistor dimensions of the comparator.

Transistor	Width(μm)/Length(μm)
M1, M2, M3, M4	16/0.5
M5, M6	20/1.2
M7, M8	3/0.35
M9, M10	2.8/0.35
M11, M12	8/0.25
M13, M14	8/0.25
M15, M16	2/0.35
M17, M18	12/0.25

respectively. The transistor dimensions of the comparator are listed in Table 4.2.

4.4 Digital Circuits

Digital functional blocks, such as calibration processor and output encoder, are also integrated in the same chip. Due to the immense complexity of this system, the background calibration algorithm was first verified with behavioral C before functional mixed VERILOG/VHDL simulations are performed. For this purpose, VHDL models were developed for all analog blocks including offset and mismatches related errors. For the digital block, the algorithm first was translated into RTL codes in VHDL, which RTL was then combined with the analog VHDL models to verify the functionality of the design. Finally, RTL was synthesized to generate the structural VERILOG descriptions based on the standard cell models. The layout based on the synthesized VERILOG descriptions was automatically placed and routed by commercial CAD software.

Fig. 4.9 shows the block diagram of the R_{ji} extractor. The low pass filter (LPF) in Fig. 3.16 is realized with a simple accumulator. The digital output from the z-ADC, D_z, is first correlated with the random sequence q' before being integrated by the accumulator. The resulting output D_y is taken only after M cycles of integration, where M is the period of the random sequence q.

Referring to Fig. 4.9, the analog signal can be assumed to be embedded in V_{j+1} for nominal A/D conversion is uniformly distributed between $+0.5V_r$ and $-0.5V_r$ and the

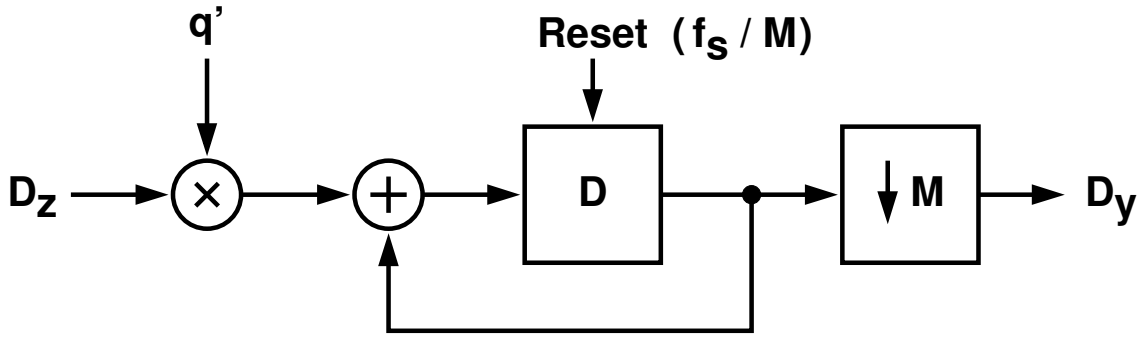


Figure 4.9: Block diagram of R_{ji} extractor.

quantization step size for a Z-bit z-ADC is $V_r/2^Z$. This V_{j+1} causes a fluctuation in D_y, resulting in a varying R_{ji}. The variance of R_j can be expressed as [18]:

$$\sigma^2\left(R_j\right) = N \times \sigma^2\left(R_{ji}\right) = N \times \frac{1}{M}\sigma^2\left(V_{j+1}\right) = \frac{N}{M} \times \frac{V_r^2}{12} \tag{4.26}$$

where N is the number of C_s fragments as defined in (3.36). By letting $\sigma\left(R_j\right)$ be smaller than one half of the z-ADC's quantization step size, the following is obtained:

$$M \geq \frac{N}{3} \times 2^{2Z} \tag{4.27}$$

Thus, the required calibration time for the j-th stage is $2N \times M = (2/3)N^2 \cdot 2^{2Z}$. Obviously, large M is required for high resolution, but it also leads to slow calibration process. (4.27) demonstrates that in order to attain 15-bit ADC using the pipeline stage shown in Fig. 3.13 with $N = 4$, one can choose $M_1 = 2^{28}$ for the 1st stage, $M_2 = 2^{26}$ for the 2nd stage, $M_3 = 2^{24}$ for the 3rd stage, and $M_n = 2^{30-2n}$ where n is the stage number. However, simulation reveals that the resulting ADC does not reach 15-bit resolution due to the accumulation of R_j errors from the cascaded stages. A better choice is to have $M_1 = 2^{28}$, $M_2 = 2^{27}$, $M_3 = 2^{26}$, and $M_n = 2^{29-n}$ where n is the stage number.

To simplify the design of this ADC prototype, $M = 2^{28}$ is chosen for all calibrated stages. For this ADC prototype, only the first five pipeline stages are calibrated. For one calibration cycle, the calibration proceeds backward and sequentially, i.e., from the 5th stage toward the 1st stage. When calibrating the 5th stage, the z-ADC is the pipeline from the 6th stage to the 18th stage. When calibrating the 4th stage, the z-ADC is the pipeline from the calibrated 5th stage to the 18th stage. When the j-th stage is under calibration,

the $R_{ji}(D_c)$ values are measured sequentially for $i = 1, 2, 3, 4$ and $D_c = -1, +1$. A total of eight R_{ji} values have to be measured for each calibrated stage. These values are used to compute $R_j(-1)$ and $R_j(+1)$. The value for $R_j(0)$ is preset to 0. A total of 40×2^{28} sampling periods are required to complete one calibration cycle, which translates to 4.5 minutes for a sampling rate of 40 MS/s. During the initial power-up, the full-cycle calibration time is reduced to 0.065 second by shorting the SHA's inputs to zero and setting $M = 2^{16}$. By shorting the inputs, the $\sigma^2\left(V_{j+1}\right)$ term in (4.26) becomes zero, and M can be reduced to speed up the calibration process.

The total logic gate count of the chip is approximately 27,000. The largest adder is the 48-bit accumulator used in the R_{ji} extractor. This ADC prototype does not require a multi-bit multiplier.

4.5 Experimental Results

Fig. 4.10 shows the chip micrograph of the fabricated ADC. The process is 0.25 μm 1P5M CMOS technology and has standard threshold voltage levels of 0.53 V and -0.53 V for NMOS and PMOS devices respectively. The chip dimensions are 3.8×3.6 mm^2. The die was packaged in a 64-pin TQFP package. Digital circuits occupy 12% of the total area. In mixed-signal chips, some strategies are required to minimize the impact of noise coupling from the digital circuitry to the sensitive analog circuitry via the common substrate. In this layout, the following approach was taken. The digital and analog blocks use separate power lines. Because an n-well process was used, the digital and analog PMOS transistors were naturally isolated by separate wells. The NMOS transistors, however, interact with each other via the common substrate. Because the substrate material is made of lightly doped p- material, traditional isolation using deep n-well guard rings to collect noise is effective enough. Thus, the analog block is surrounded by analog V_{DD} and V_{SS} power lines. Decoupling capacitors formed by PMOS and NMOS devices are buried underneath the analog power lines. This guard-ring structure shields noise coupled from the digital block via the substrate.

For the analog NMOS transistors, it is important that the source-to-body voltage is constant. Otherwise, if these voltages move relative to each other, the drain current is

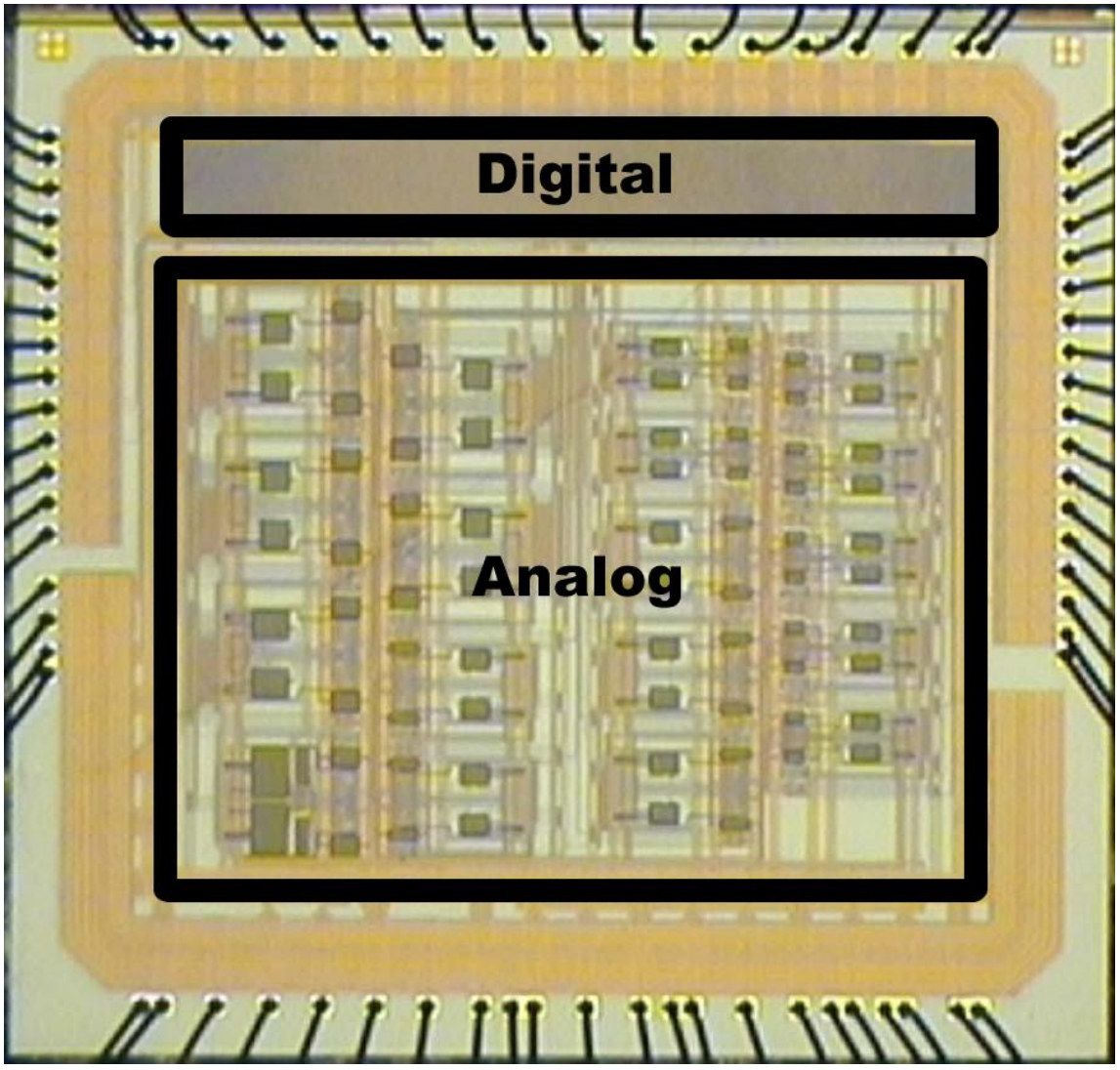


Figure 4.10: ADC chip micrograph.

modulated through the body effect. Therefore, it is important to locally have a low-resistance path from body to source. In the layout, a p+ substrate ring was placed around each NMOS analog transistor. This ring was then contacted to analog V_{SS} power lines, which is at the same potential as the source for common-source devices. This helps keep the source and the body at the same potential.

Operating at a 40 MS/s sampling rate under a single 2.5 V supply, the analog block consumes a total of 350 mW of power while the digital block consumes only 20 mW.

In order to evaluate the 15-bit ADC properly,the test system was carefully configured to minimize various effects, such as input signal distortion,test-board noise,and clock jitter, which would destroy the measurements. A four-layer printed circuit board was used to provide good power and ground planes and to shield all critical signal paths. The sinewave generator is the Agilent 14438c with 16-bit DAC output. The sinewave input signal is filtered with a 4-tap passive LC bandpass filter to further reduce any remaining harmonic distortion. Before going into the ADC, the single-ended sinusoidal source drives an external center-tapped transformer which then applies the resulting differential signal directly to the inputs of the converter. The output data from the ADC were collected by logic analyzer, the Agilent 16702B equipped with 32MB memory. The logic analyzer operated in sampling mode. The sampling clock also came from the ADC.

Fig. 4.11 and Fig. 4.12 show the ADC's differential nonlinearity (DNL) and integral nonlinearity (INL) characteristics obtained from code-density measurements. Notably, the LSB is normalized to 16-bit resolution in those figures. The number of registered output codes is approximately $3/4 \times 2^{16}$. Fig. 4.11 shows the ADC's native DNL and INL before activating the calibration processor. The DNL is $+1.2/-0.6$ LSB and the INL is $+15/-15$ LSB. Fig. 4.12 shows the ADC's DNL and INL after the background calibration is activated. The DNL is reduced to $+0.34/-0.25$ LSB and the INL is reduced to $+3.4/-4.0$ LSB.

Fig. 4.13 shows the ADC's output FFT spectra at a 40 MS/s sampling rate. The input is a differential 2.0 V_{pp} 8.30 MHz sinusoidal signal. Without calibration, the 3rd-order harmonic is the dominant distortion term, which is -76 dB below the fundamental signal. The signal-to-noise-plus-distortion ratio (SNDR) is 68 dB and the spurious-free dynamic range (SFDR) is 76 dB. After the background calibration is activated, the SNDR is im-

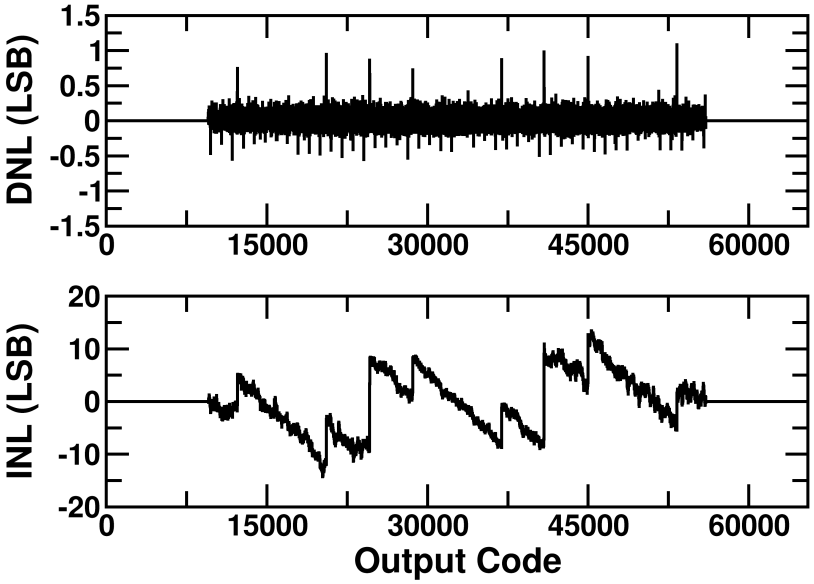


Figure 4.11: Measured DNL and INL at 40MS/s with calibration off.

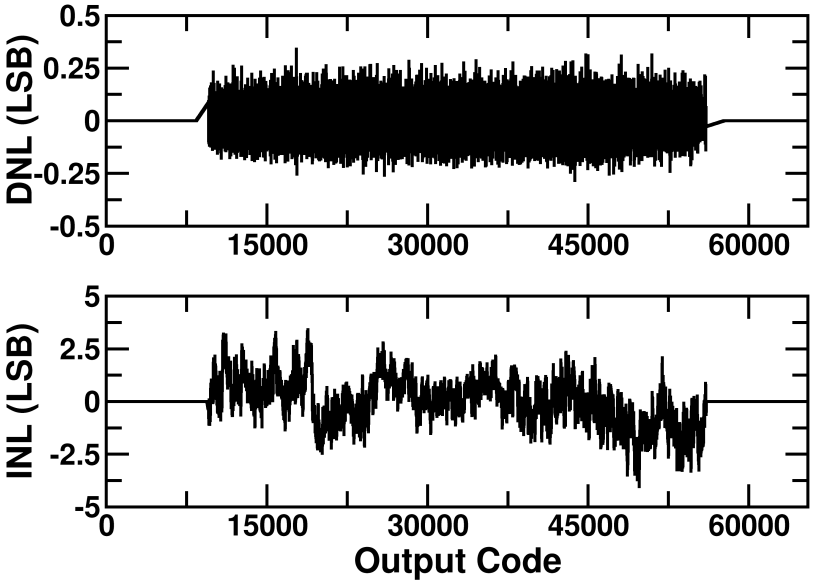


Figure 4.12: Measured DNL and INL at 40MS/s with calibration on.

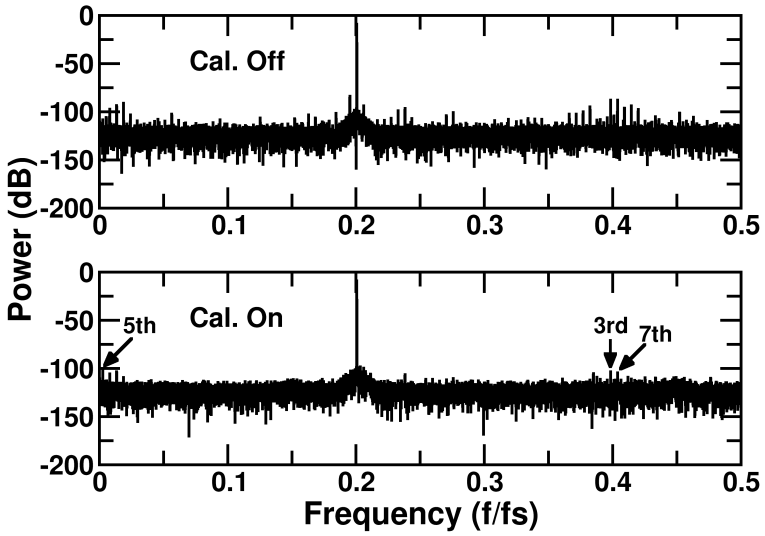


Figure 4.13: Measured output FFT spectra. The 2.0 V_{pp} 8.30 MHz differential sinusoidal input is sampled at 40 MS/s.

proved by 5.5 dB to 73.5 dB and the SFDR is improved by 17.3 dB to 93.3 dB. Notably, the ADC's signal-to–noise ratio (SNR) remains almost the same before and after calibration. The SNDR/SFDR improvement after calibration comes from the elimination of harmonic tones.

Fig. 4.14 shows the ADC's measured SNDR and SFDR versus input frequencies at a 40 MS/s sampling rate. The SNDR and SFDR change little up to the Nyquist frequency. Generally, the calibration can improve the SNDR by 5.5 db and the SFDR by 17 db. Fig. 4.15 shows the ADC's SNDR versus input signal level with calibration on and off respectively. The 1 MHz sinusoidal input is sampled at 40 MS/s. The data reveal that the total noise power, excluding distortions, is not affected by the input level. The noise power does not increase when the calibration is on. Thus, the random term R_{ji} injected into the analog signal path is fully removed in the digital output. The measured dynamic range is approximately 78.5 dB.

Table 4.3 summarizes the measured performance of the ADC prototype at room temperature.

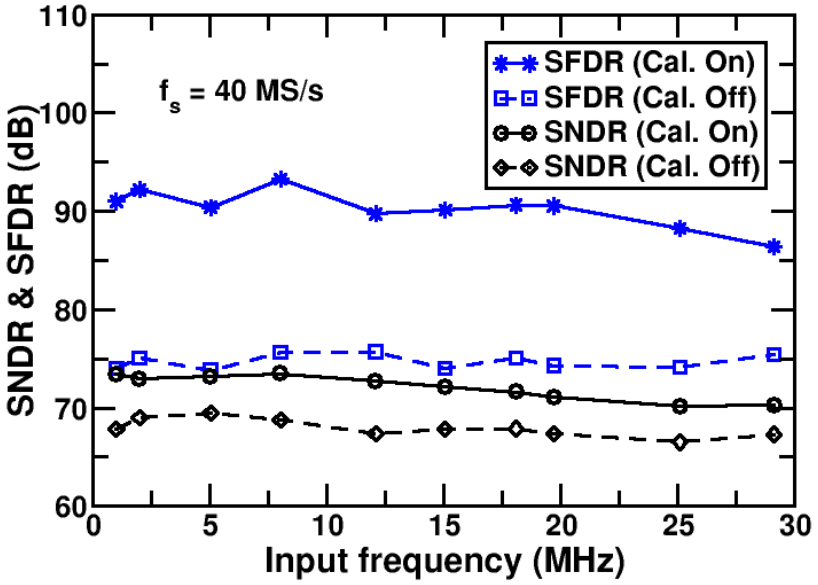


Figure 4.14: Measured SNDR and SFDR versus input frequency at 40 MS/s sampling rate.

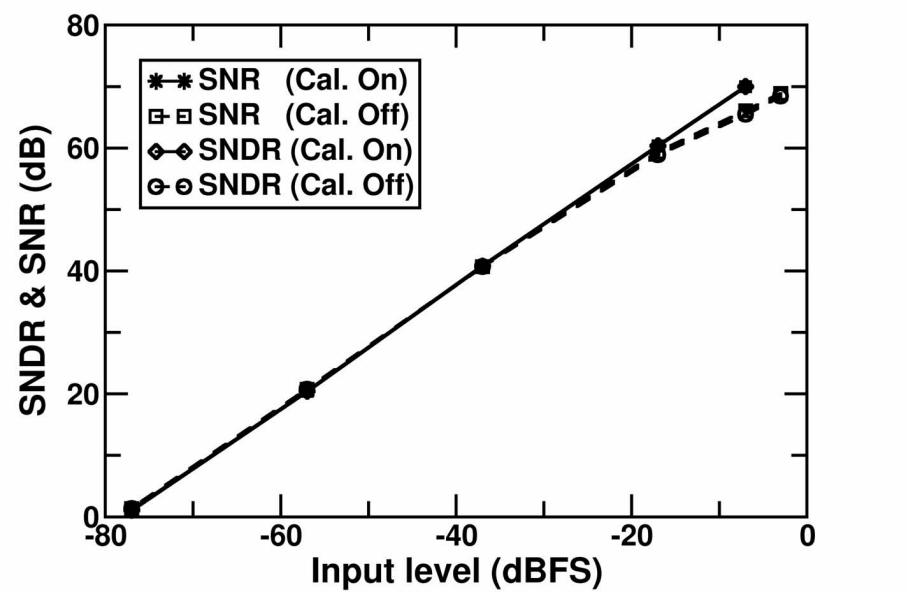


Figure 4.15: Measured SNDR and SNR versus input level. The 1 MHz differential sinusoidal input is sampled at 40 MS/s.

Table 4.3: ADC performance summary

Technology	0.25 μm CMOS
Chip Area	3.8×3.6 mm^2
Supply, V_{AA}/V_{DD}	2.5/2.5 V
Power, P_{AA}/P_{DD}	350/20 mW
Max. Sampling Rate	40 MS/s
Differential Input Range	2.1 V_{pp}
Number of Output Codes	$(3/4) \times 2^{16}$
DNL, normalized to 16 bits	$-0.25/+0.34$ LSB
INL, normalized to 16 bits	$-4.00/+3.40$ LSB
SFDR, f_s = 40 MS/s, f_{in}=8.03MHz	93.3 dB
SNDR. f_s = 40 MS/s, f_{in}=8.03MHz	73.5 dB

4.6 Summary

To verify the proposed background calibration technique, an experimental prototype was designed and fabricated. Besides the analog circuits, the digital blocks which contain the background calibration algorithms are also integrated into the same chip. The system consists of an input Sample-and-Hold followed by 17 radix-2 1.5-b SC pipelined stages and a final 2-b flash stage. Only the first five pipeline stages were designed to employ the proposed background calibration scheme.

The ADC was fabricated using a 0.25 μm 1P5M CMOS technology. The process has standard threshold voltage levels of 0.53 V and -0.53 V for NMOS and PMOS devices respectively. The maximum rated voltage supply is 2.5 V. Linear capacitors were implemented using metal-insulator-metal (MIM). The capacitance of these capacitors was approximately 1 fF/μm^2. The die was packaged in a 64-pin TQFP package. Operating at a 40 MS/s sampling rate, the ADC attains a maximum signal-to-noise-plus-distortion ratio (SNDR) of 73.5 dB and a maximum spurious-free-dynamic-range (SFDR) of 93.3 dB. The chip occupies an area of 3.8×3.6 mm^2, and the power consumption is 370 mW with a single 2.5 V supply.

Chapter 5

Summary and Future Works

5.1 Summary

The continuing aggressively CMOS device scaling and the maturity of digital CAD has made it possible to implement much analog functionality with DSP techniques. However, the analog-to-digital converter, which is required to interface digital processors to ”real life” signals such as radio, speech and image waveforms, will remain. The DSP-based system places a strong demand for high-speed and high-resolution ADCs. Pipelined ADCs have been shown to work at very high speeds but their resolutions are limited by component mismatches, opamp finite gain, offsets, charge injection errors and component non-linearity. Self calibration and background calibration techniques have been developed to correct for these non-linearities. Digital self-calibration is a very promising technique to improve the accuracy of SC-based pipeline ADCs. The most attractive feature of digital self-calibration is the minimum extra analog circuit involved. Thus, analog precision problems are translated into the complexity of digital signal processing circuits, allowing this approach to benefit from CMOS device scaling.

In this thesis, a mathematical description of the operation of the pipeline ADC first was presented to allows many algorithms and architectures to be viewed and compared within a unified framework. Terminology was defined and related to classic, uncorrected converters. Redundancy and digital error correction were described in a general way, and were shown to correct the comparator errors. Some examples of multistage A/D convert-

ers were examined, and in each case the ADC operation was presented in terms of the mathematical description. Then, based on the approach, the theory of digital calibration was derived and led naturally to consider the A/D conversion as a decomposition into look-up tables or "weights" that can be digitally calibrated.

By dividing the step heights of MDAC in a pipeline stage and injecting a random signal into the MDAC, the knowledge of weights can be procured without interrupting the normal analog-to-digital operation. The proposed calibration technique takes advantage of the digital redundancy architecture inherent to most pipelined ADCs. In the proposed method, the SNR is not degraded by the pseudorandom noise sequence injected into the system.

A high-resolution CMOS pipelined ADC consisting of 17 radix-2 1.5-bit switched-capacitor pipeline stages and a final 2-bit flash stage has been realized to demonstrate the feasibility of the proposed digital background calibration technique. A pipeline stage can be calibrated without interrupting its normal A/D operation by injecting a random sequence into its MDAC through the split $C_{s,i}$ capacitor. The calibration can correct the errors resulting from capacitor mismatches and finite opamp gains. All calibration procedures are conducted in the digital domain. The required modification to the analog signal path is minimal and is not crucial to the circuit's performance. This calibration scheme is also robust since its effectiveness does not rely on the input's amplitude distribution. Ultimately, the linearity of the calibrated ADCs is constrained by the opamps' nonlinear characteristics, the capacitors' voltage coefficients and the transient behavior of the circuitry.

The 15-bit 40-MS/s CMOS pipelined ADC was fabricated in a 0.25 μm CMOS technology. This chip occupied 3.8 × 3.6 mm^2 and dissipated 370 mW from a single 2.5 V supply. It achieves an SFDR of more than 90 dB and an SNDR of more than 73 dB. The calibration can improve SFDR by 17 dB and SNDR by 5.5 dB. The SNDR is limited by coupling noises. The maximum sampling rate is limited by the speed of the opamps.

Although only a radix-2 1.5-bit switched-capacitor pipeline stage was demonstrated herein, the principle of the proposed calibration technique is applicable to multi-bit pipeline stages and circuit configurations other than the switched-capacitor circuit.

5.2 Recommendations for Future Investigation

This section presents several suggestions for future investigations into the design of high-performance ADCs.

- The MDAC used in the ADC prototype is the 1.5-bit stage. The input-signal magnitude needs to be reduced to $\pm 3/4V_r$ to accommodate the injection of pseudorandom calibration signal. Adding more redundancy into the MDAC to reduce the amplitude of the residue output can get around the limitation. The DRD stage introduced in Chapter 2 is such kind of MDAC and deserves further study.

- The correlation-based algorithm converges very slowly. It takes fairly long time to achieve highly accurate results. The main reason is the strong interference from the input signal to the ADC. To mitigate this problem, the authors [45] place two identical ADCs in parallel to build a two-channel ADC. Behavioral simulations have been performed to verify their calibration scheme and reveal the possibility of high resolution ADCs. A prototype based on the calibration algorithm has been presented, but the achieved performance was not as good as their simulations [62]. Further study is warranted, though. Parallel calibration of the calibrated stages is another idea, but the MDAC should be modified to avoid overrange of the residue output. The DRD stage is one of the candidates.

- In the proposed calibration scheme, the errors due to capacitor mismatches and finite opamp gain are corrected but the nonlinear opamp gain is left alone. A common method of dealing with the problem of nonlinear opamp gain is to use a small signal range to simply avoid the highly nonlinear region of the gain characteristic. For example, apply the DRD stage as the first pipeline stage followed by the SHA, the conventional 1.5-bit per stage architecture can be operated with the analog input range at half of the full scale value. Actually the obvious alternative approach trades resolution for linearity. Other approaches worth of attention include continuously estimating and tracking the nonlinearity errors of the opamp and performing digital domain compensation [46] [63].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