國立交通大學

材料科學與工程學系

博 士 論 文

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摘要

鎳金屬誘發非晶矽薄膜結晶的技術(MIC)已經被廣泛地使用於製作低溫多晶矽(LTPS)薄膜電晶體(TFTs)。然而，由於鎳金屬雜質殘留於鎳金屬誘發多晶矽薄膜之中，高漏電流一直是鎳金屬誘發結晶多晶矽薄膜電晶體(MIC TFTs)的一個問題。因此，本論文的主要目的為減少鎳金屬雜質的殘留量，提升鎳金屬誘發結晶多晶矽薄膜電晶體的電特性，並進一步探討鎳金屬濃度對於其它重要電性質之影響。

首先，我們將化學氧化過濾層(chemical oxide filter layer)引入鎳金屬誘發結晶技術的流程，以降低鎳金屬誘發結晶多晶矽薄膜電晶體的漏電流，此方法很簡單且不需額外昂貴的儀器。在沉積鎳金屬之前，我們只需額外將已沉積好非晶矽薄膜的試片浸泡入化學溶液的一個步驟。由實驗結果發現，化學氧化層的引入成功地降低鎳金屬誘發多晶矽薄膜中的鎳金屬含量，也顯著地改善金屬誘發結晶多晶矽薄膜電晶體的電特性。相較於傳統

的金屬誘發結晶多晶矽薄膜電晶體 (MIC TFTs)，引入化學氧化物的金屬誘發結晶多晶矽薄膜電晶體(CF-MIC TFTs)呈現在最低洩漏電流下 14.3 倍，在開/關電流比增加 17.3 倍。其原因為化學氧化層可避免鎳金屬與非晶矽薄膜直接接觸，避免過量的鎳原子進入非晶矽薄膜並且使未反應的鎳金屬容易從表面除去。

除此之外，我們進一步地利用傳輸線的方法(transmission line method)研究鎳金屬濃度對源/漏串聯電阻(S/ D series resistance)的影響。鎳金屬的影響除了在已知的漏電流之外，鎳濃度的降低可能會造成金屬誘發結晶多晶矽薄膜電晶體的源/漏接觸電阻隨之變化，進而影響了元件的效能（驅動能力）。因此，我們獲得一個新發現—鎳金屬濃度和元件電阻之間的相互關係。由結果顯示，源/漏接觸電阻和通道電阻皆隨著金屬誘發結晶多晶矽薄膜之中的鎳金屬濃度減少而降低。近年來，關於主動式有機發光顯示器(AMOLED)的應用，電偏壓的可靠度(bias reliability)和熱穩定性(thermal stability)已成為主要關注的課題，尤其是當元件操作於熱載子(Hot carrier)狀態及高溫環境中。本研究中也探討了鎳金屬濃度對於電偏壓可靠度及熱穩定性的影響。結果發現，低鎳金屬殘留量的元件對於熱載子應力(hot carrier stress)和升溫操作下呈現較高的抵抗能力。以上現象證明，除了已知的漏電流，減少金屬誘發結晶多晶矽薄膜之中的鎳金屬濃度亦有利於源/漏接觸電阻，電偏壓可靠度和熱穩定性。

最後，我們提出了一個新的製作多晶矽薄膜電晶體的方法，驅入式鎳金屬誘發結晶(DIC)，主要是利用氟離子佈植的方式驅使鎳金屬進入非晶矽薄膜而進行後續的金屬誘發結晶。結果發現，此方法可以有效地減少鎳金屬濃度並且鈍化(passivate)二氧化矽與多晶矽界面附近的捕捉態(trap-state)，因而使得元件的電特性(尤其是漏電流)和熱穩定性都獲得相當地改善。然而，在開啟電流(on-state current)的部份無法獲得明顯的改善，其原因可能是由於離子佈植過程中造成的通道損害或缺陷產生所致。因此，我們將暫時的氧化層引入驅入式鎳金屬誘發結晶的製程中(DICC)，主要來降低由離子佈植過程中所造成的傷害，而獲得更進一步的改善。相較於傳統的金屬誘發結晶多晶矽薄膜電晶體，此方法製備的薄膜電晶體呈現在開/關電流比(I_{on}/I_{off})增加 9.7 倍，在最低洩漏電流(I_{min})則由 4.06 pA/μm 下降至 19.20 pA/μm，另外也呈現較好的可靠度。

Improved performance and reliability of MIC LTPS-TFTs using simply chemical oxide and drive-in nickel induced crystallization

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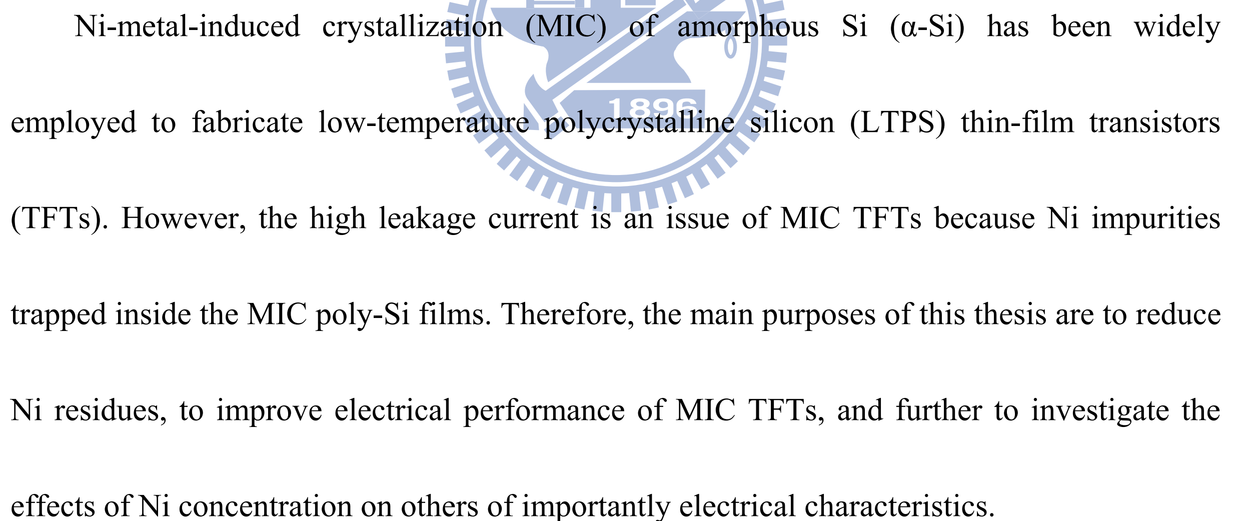


Abstract

Ni-metal-induced crystallization (MIC) of amorphous Si (α-Si) has been widely employed to fabricate low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs). However, the high leakage current is an issue of MIC TFTs because Ni impurities trapped inside the MIC poly-Si films. Therefore, the main purposes of this thesis are to reduce Ni residues, to improve electrical performance of MIC TFTs, and further to investigate the effects of Ni concentration on others of importantly electrical characteristics.

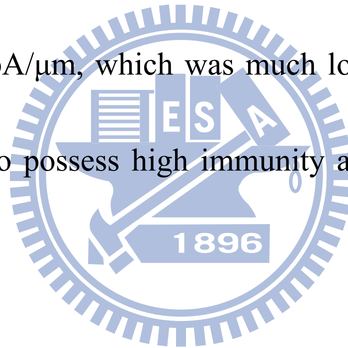
First, a chemical oxide filter layer was introduced into MIC processes to reduce the leakage current of MIC TFTs, which was simple and without extra expensive instrument. It just added a step of dipping α-Si coated sample into chemical solution before depositing the Ni film. It was found that Ni concentration was decreased successfully in MIC poly-Si films

and the electrical performance of MIC TFTs with chemical oxide layer was significantly improved. Compared with conventional MIC TFTs, CF-MIC TFTs shows a 14.3-fold decrease in the minimum leakage current and a 17.3-fold increase in the on/off current ratio. This is because the chemical oxide layer can avoid Ni directly contact with α-Si, avoid excess of Ni atoms into α-Si layer and remove unreacted Ni easily from surface.

Furthermore, the Ni concentration effect on source/drain (S/D) series resistance was investigated by transmission line method. In addition to well known Ni effects on leakage current, however, the S/D series resistance of MIC TFTs might be changed with reduction of Ni concentration, which also influences the device performance (driving ability). Therefore, we attained a new finding for the relation between Ni concentration and resistance. As the results, the S/D series resistance and channel resistance were decreased with the reduction of Ni concentration in MIC poly-Si. Recently, the bias reliability and thermal stability became major concerns for AMOLED display applications especially when devices are operated under hot carrier condition and high temperature environment. In this study, the effect of Ni concentration on bias reliability and thermal stability were also investigated. It was found that the low Ni residues device presented high immunity against the hot-carrier stress and elevated temperature. These findings proved that reducing Ni concentration in MIC films was also beneficial for S/D series resistance, bias reliability and thermal stability.

Finally, a new manufacturing method for poly-Si TFTs using drive-in Ni induced

crystallization (DIC) was proposed. In DIC, F^+ implantation was used to drive Ni in the α-Si layer. It was found that the electrical performance (especially leakage current) and thermal stability of DIC TFTs were improved due to the reduction of Ni concentration and passivation of trap states near the SiO_2/poly-Si interface. However, the on-state currents were nearly unchanged due to the channel damages/defects caused by ion implantation. Therefore, a cap oxide layer was introduced into DIC process (DICC) to reduce ion implant damages. Compared with that of MIC TFTs, the on/off current ratio (I_{on}/I_{off}) of DICC TFTs was increased by a factor of 9.7 from 9.21×10^4 to 8.94×10^5. The minimum leakage current (I_{min}) of DICC TFTs was 4.06 pA/μm, which was much lower than that of the MIC TFTs (19.20 pA/μm). DICC TFTs also possess high immunity against the hot-carrier stress and thereby exhibit good reliability.



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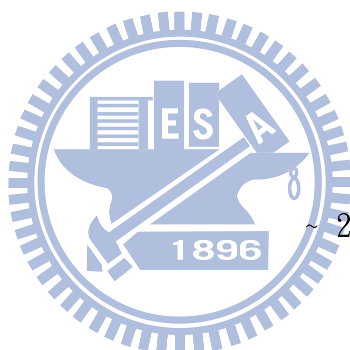

~2011 年 09 月 新竹 交大工六館

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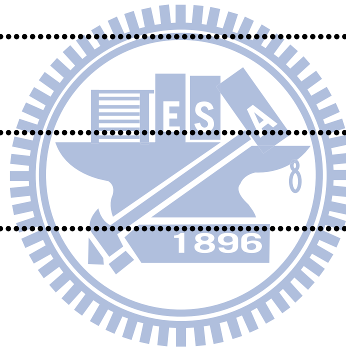

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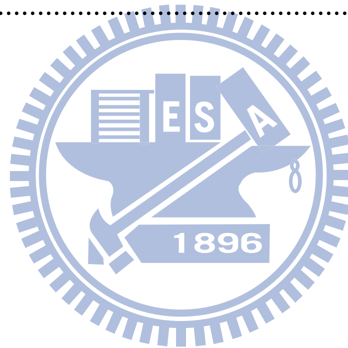

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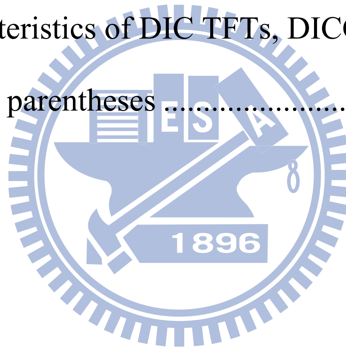


Chapter 1

Introduction

1.1 Overview of low temperature polycrystalline silicon thin-film transistors (TFTs) technology

The first generation of active matrix liquid crystal displays (AMLCDs) used amorphous silicon (α-Si) TFTs as the pixel switching device due to the advantages such as low temperature process (<350°C) [1]-[2] suitable for large area, non-expensive glass substrate and lower leakage current that is enabling for pixel switching. However, the low electron field effect mobility (typically < 1 cm^2/Vs) of α-Si TFTs limits the capability of advanced and integrated circuit. To achieve the adequate current for the grayscale of the frame, large size of α-Si TFTs device will result in lower resolution of the display. Polycrystalline silicon (poly-Si) TFTs technology is one of the potential methods to achieve the requirement of high-resolution TFT LCD due to high mobility.

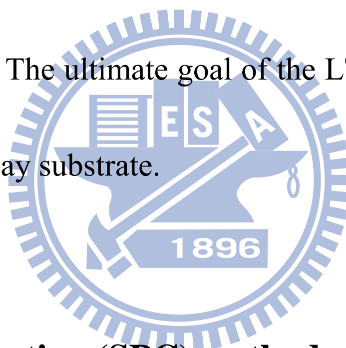
High temperature poly-Si TFTs had been fabricated by using chemical-vapor deposition in 1980, which achieved good carrier mobility (around 50 $cm^2/V\text{-}s$) and electrical characteristics [3]. These high temperature poly-Si TFTs were employed gate insulator SiO_2 grown thermally at 1050°C. However, the high temperature fabrication is unacceptable for

currently low-cost glass substrates. Recently, low-temperature poly silicon (LTPS) technologies have attracted significant interest from many research organizations around the world, and have been considered one of the most important next-generation large-area electronic techniques. Various applied devices regard LTPS as a potential solution for the future due to electrical performance and cost-down issue, such as displays, sensors, memories, and even other 3-dimensional complicated integrated circuits [4]-[6]. Several techniques for crystallization of α-Si at low temperature (below 600°C) have been developed to increase mobility, consequently to be able to integrate drive circuitry [7]-[8] and more compatible with the glass substrate. In fact, the field effect mobility of poly-Si TFTs are significantly higher than that of α-Si about two orders of magnitudes. The higher drive current allows small TFTs dimension to be used as the pixel switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance [9].

Moreover, the manufacturing of poly-Si TFTs can be combined with MOSFETs process on the inexpensive glass substrates, leading to cheaper expenditure. A various techniques have been investigated for crystallization of α-Si at low temperature such as: (1) solid phase crystallization (SPC) (2) excimer laser crystallization (ELC) (3) Ni-metal induced crystallization (MIC). In the following section, we will review the crystallization method that the above-mentioned.

1.2 Low temperature crystallization of amorphous silicon

Low temperature crystallization of α-Si films has been considered as the most important process step in the fabrication of LTPS TFTs. The quality of crystallized poly-Si films is quite sensitive to the performance of poly-Si TFTs. In poly-Si films, most defects are generated at the grain boundaries. Enlarging the grain size can promote the quality of poly-Si, as deposited poly-Si generally exhibits small grain size. In general, the poly-Si crystallized from α-Si usually has larger grain size than that of as-deposited poly-Si. Historically, solid phase crystallization [10] was the first technology to produce poly-Si films for display applications, followed by laser crystallization. The ultimate goal of the LTPS technology is to integrate the pixel-driving circuits on the display substrate.



1.2.1 Solid phase crystallization (SPC) method

α-Si is a thermodynamically metastable phase possessing a driving force for transformation to polycrystalline phase given a sufficient energy to overcome the initial energy barrier. Deposited α-Si thin films were transformed to poly-Si using SPC method has obtained better TFT device electrical performance [11] than as-deposited poly-Si films. For the SPC method, to crystallized α-Si films in a furnace at temperature about 600°C for duration time (about 24 h). The polycrystalline grains are generally in oval-shaped and large defect density exists in poly-Si films.

A key factor affecting crystallization is the nucleation rate in the α-Si films. The nucleation rate is strongly influenced by the selected deposition method and condition [12]-[13]. The structural order/disorder in the α-Si films affects the films to form stable nuclei. Higher disorder structure increases the energy barrier required to form the Si nuclei, this concept has been used in the past to increase the grain size of poly-Si films. Ideally, a small number of fast-growing nuclei are needed to maximize the grain size. However, the reality of the situation is that the probability that additional nucleation events will occur within the volume separating growing nuclei increases geometrically with the separation distance.

1.2.2 Excimer laser crystallization (ELC) method

By means of the melt-induced poly-Si growth, ELC method provides poly-Si material with high quality than SPC method. For the crystallization process, the laser is irradiated at the α-Si and the silicon is heated above 1200°C. However, only sustained for a very short time, therefore it will not damage the glass substrate. Moreover, there are two major transformation regimes (occurring at low and high laser energy, respectively) and one minor transformation regime in between (that so-called superlateral growth, or SLG) [14]-[15]. The low laser energy regime describes a situation where the incident laser is sufficient to induce melting of the silicon films, but it is low enough that a continuous layer of silicon at the maximum extent of melting. For this reason, this regime is referred to as the partial melting

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regime. The high laser energy regime corresponds to a situation that the laser energy is sufficiently high to completely melt the silicon film; this regime is also referred to as complete melting regime. In addition to these two regimes, a third regime has been found to exist within a very narrow experimental window in between the two main regimes. Despite the small extent of this region, it is nonetheless one with great technological significance, because the poly-Si films within the regime feature large-grained polycrystalline microstructures [16]. Although the highest quality poly-Si films were fabricated by ELC method, the poor grain size uniformity and high roughness ELC poly-Si films degraded the performance of TFTs [17].

1.2.3 Ni-metal induced crystallization (MIC) method

Solid phase crystallization of α-Si is needed a high temperature and longer annealing time for furnace annealing process. By using MIC method, the annealing time and temperature could be reduced, and the grain size of MIC poly-Si films uniformly over large area. In 1964, Wagner and Ellis [18] found that the presence of small amounts of a metallic phase could enhance the Si crystal growth. In general, two groups can be classified in the MIC mechanism. One is to form eutectics with Si (Al [19], Au [20], and Sb [21]) and another is metastable silicide forming metals (Ni [22]-[25], Pd [26]-[27] and Co [28]). For example, the Al/silicon eutectic temperature is 577°C [29], but crystallization and type conversion of

α-Si films in contact with Al occurs at temperatures as low as 200°C.

Figure 1-1 shows the diamond structure of Si and the fluorite structure of $NiSi_2$. The lattice constant of Si and $NiSi_2$ is 5.430 Å and 5.406 Å, respectively, leading to very small lattice mismatch of 0.4 % with Si. The Ni-metal is considerably suitable for the formation of epitaxial Si and is therefore employed for the fabrication of MIC poly-Si films in this thesis. When a Ni film is deposited on a c-Si substrate and annealed, the Ni_2Si with $PdCl_2$ structure forms at ~200°C and transforms into NiSi with the MnP structure at 350-750°C [30]. These two phase-transformations are diffusion-controlled processes. Finally the NiSi transforms into the end phase $NiSi_2$ by a nucleation-controlled process at high transformation temperature in the range 450-750°C. However, the NiSi transforming into the $NiSi_2$ is a diffusion-controlled process for the α-Si. Hence it's a low-temperature process as 350°C for $NiSi_2$ precipitate formation, as shown in Fig. 1-2 [31]. Subsequently, the $NiSi_2$ crystallites serve as the nuclei for crystallization. The diffusivity of Ni [32] in α-Si is higher than that in c-Si. Thus the needle-like Si crystallite forms due to the diffusion of Ni in the α-Si network. Figure 1-3 shows the equilibrium molar free-energy diagram [25] for $NiSi_2$ in with α-Si and c-Si. Initially, several Ni-Si phases form in the silicide region and the $NiSi_2$ phase is found near the Si region [24]. The chemical potential of the Ni atoms is lower at the $NiSi_2$/α-Si interface and that of the Si atoms is lower at the $NiSi_2$/c-Si interface. Thus there is a driving force for Ni atoms diffusing through $NiSi_2$ to α-Si and for Si atoms diffusing reversely. This result

indicates that the α-Si is consumed at the $NiSi_2$/α-Si during the migration of $NiSi_2$ crystallite. In 1993, C. Hayzelden and J. L. Batstone [25] found that a few layers of c-Si exist at the leading edge of the $NiSi_2$ precipitate. Therefore, they propose a possible modification of the growth mechanism, as shown in Fig 1-4. The nucleation of c-Si on $NiSi_2$ initially occurs and Si atoms then diffuse through $NiSi_2$ to c-Si, as illustrated in Fig 1-4 (a). Next a c-Si nucleates at the leading edge of a migrating $NiSi_2$ precipitate. Ni atoms then diffuse through $NiSi_2$ to α-Si due to its ability to lower the chemical potential at the $NiSi_2$/α-Si, as shown in Fig 1-4 (b). A fresh c-Si forms at the $NiSi_2$/α-Si interface and the process repeats. Finally the needle-like Si crystallite is formed after the migration of $NiSi_2$ in a-Si network, as shown in Fig 1-4 (c).

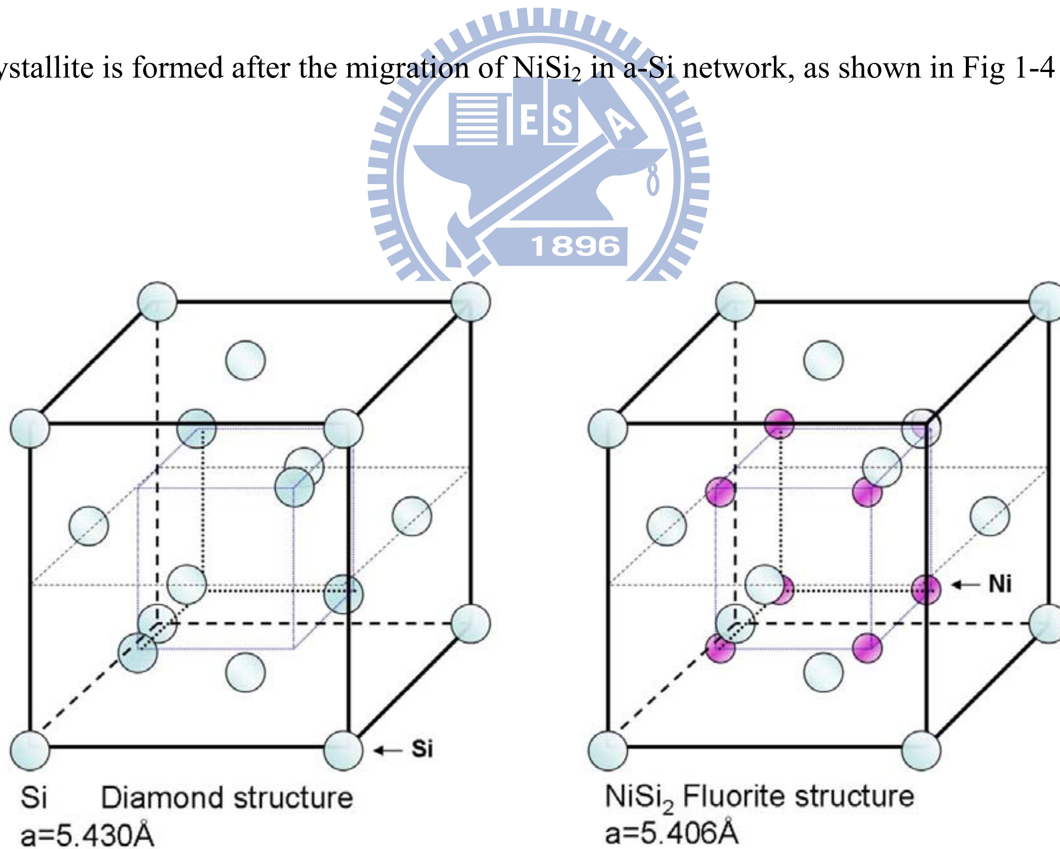

Fig. 1-1 The crystalline structures of Si and $NiSi_2$.

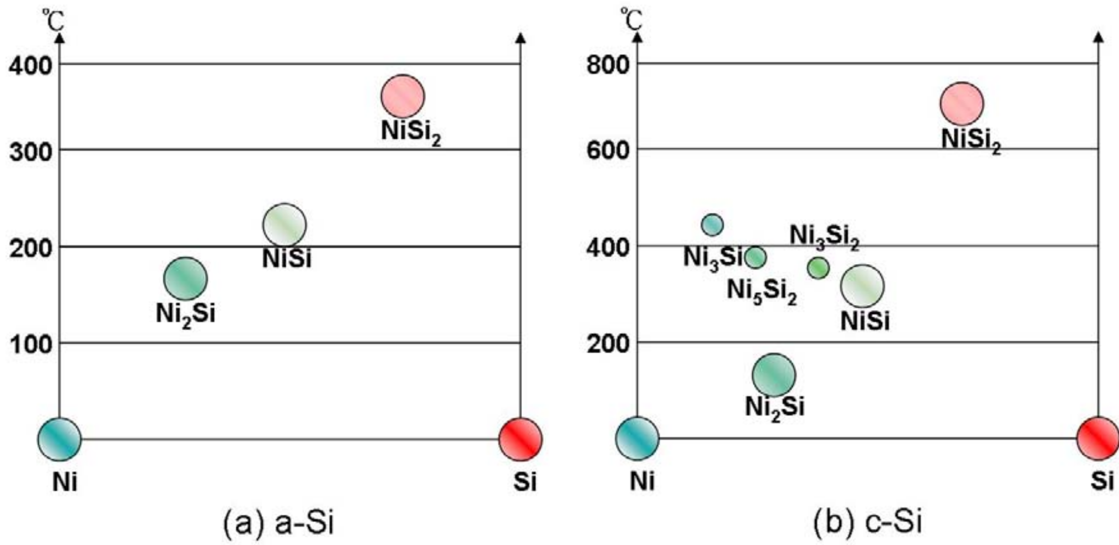

Fig. 1-2 The formation temperature map of thin-film Ni silicides on (a) α-Si, and (b) c-Si [31].

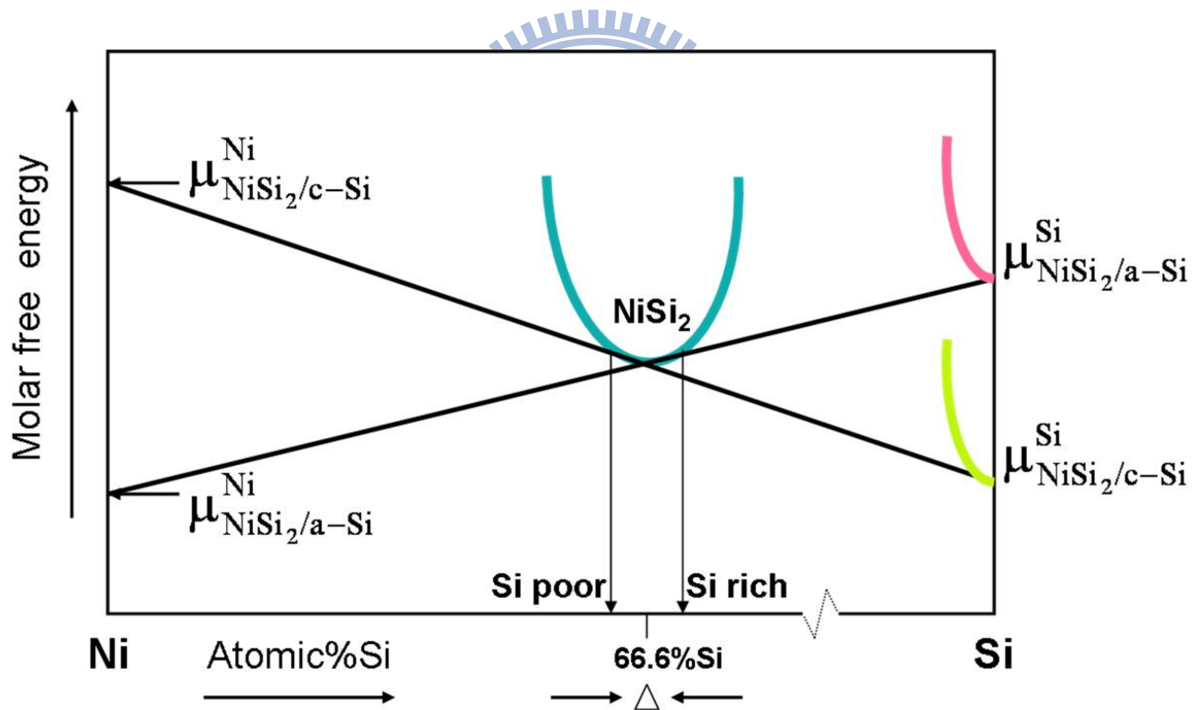

Fig. 1-3 The equilibrium molar free-energy diagram for $NiSi_2$ in contact with α-Si and c-Si [25].

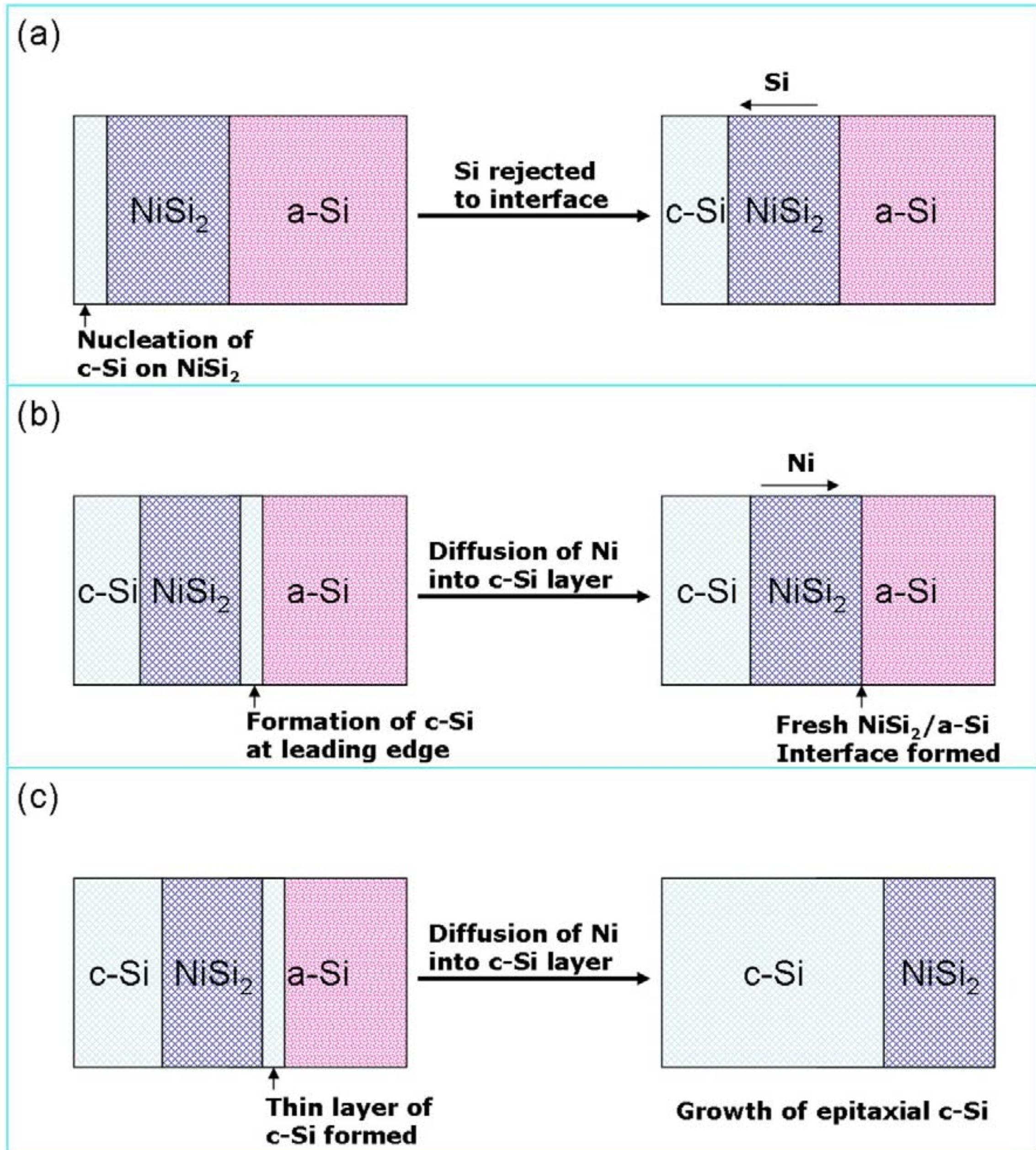

Fig. 1-4 A possible modification of the c-Si growth mechanism involving the formation of a thin layer of c-Si at the α-Si/$NiSi_2$ interface [25].

As a result, Ni is the undisputed metal of choice for silicide assisted crystallization. It should be noted that traces of $NiSi_2$ also remain within the c-Si that is left behind after the

growth phase. In practice, these metal and metallic compounds would degrade performance of device. Therefore, Ni concentration in MIC poly-Si should be reduced. The atomic layer deposition (ALD) and gettering method have been employed to reduce the amount of undesired metal impurity. However, both methods are complex and incur high cost.

In this thesis, we will focus on the Ni-metal induced crystallization method. Simultaneously, by using some simple technologies reduce Ni residues and further improve device performance.

1.3 Issues of polycrystalline silicon films

Compared with devices fabricated on single crystal silicon, poly-Si TFTs present a poor performance because numerous grain boundaries and intragranular defects exert a strong influence on device characteristics and degrade carrier transport, such as threshold voltage, subthreshold swing, leakage current, mobility and transconductance. The dangling bonds in poly-Si film grain boundaries serve as the trapping centers, which trap many free carriers (either electrons or holes) and consequently hinder carriers from conduction [33]-[35]. As shown in Fig. 1-5 [33], the trapped carrier will then deplete the charge nearby the grain boundaries and further a voltage barrier is built across the grain boundaries. Therefore, attempts have been made to modify or remove those grain boundaries owning to traps are associated with the dangling bonds at the grain boundaries. Hydrogen can passivate dangling

bonds and other defects at grain boundaries by terminating them with hydrogen atoms [35]. As the number of trapped carriers decreases, the potential barrier associated with the grain boundary also decreases [36].

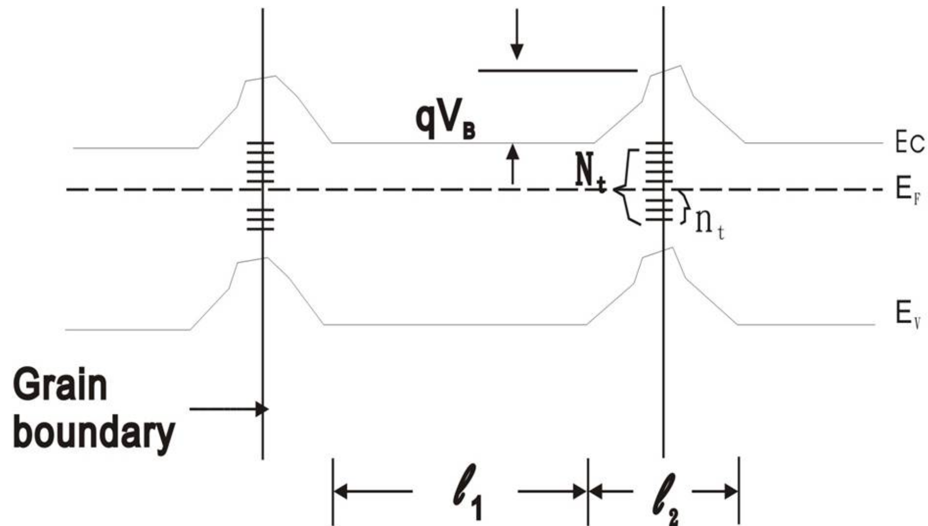

Fig. 1- 5 Schematic representation of band structure for inhomogenous-film model [33].

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1.4 Electrical characteristics of Ni-metal induced crystallization (MIC) TFTs

MIC method has some advantages over other crystallization methods such as lower equipment cost, better uniformity than ELC method, and lower thermal budget than SPC method. However, several intrinsic growth characteristics of MIC method always resulted in poor TFT performance, such as higher leakage current (I_{lk}) and poor electrical stability due to large Ni-related defect in Si/SiO_2 interface and grain boundary [37]-[41]. Fig. 1-6 illustrates

the leakage current model using band diagrams [42]-[44], the first situation in Fig. 1-6 (a) is described only the thermal activation of an electron from the valence band to the conduction band. The second situation in Fig. 1-6 (b), which is induced due to the trap or surface state in the band gap and as the drain bias increase, the activation energy decreases, this suggest that the high field in the drain depletion region has reduced the barrier that the electron must overcome. This situation comprises two steps: the first step is the thermal activation of an electron from the valence band to a trap state (E_t) in the band gap, and the second step is electron tunneling through this reduced barrier to the conduction band. As such, the dominate leakage current mechanism is thermionic field emission. The third situation in Fig. 1-6 (c) is induced under strong electric field, the dominate leakage current mechanism is pure tunneling. The tunneling length decreases as the electric field increases, in this situation, the presence of the trap state in the band gap assists the process by shorting the effective tunneling length of the electron. In addition, the trap state in the band gap plays an important role in the leakage current model. In the traditional MOSFET, those situations do not occur easily because the trap state is low. This causes different leakage current between MOSFET and TFTs.

As mentioned earlier, the Ni contamination within the MIC poly-Si films which was purposed to form the active layer of TFTs device, that the Ni impurity can degrade the minority carrier lifetime and increase the leakage current. The leakage current is proportional to the impurity concentration [44]-[45]. For this reason, reducing Ni contamination in MIC

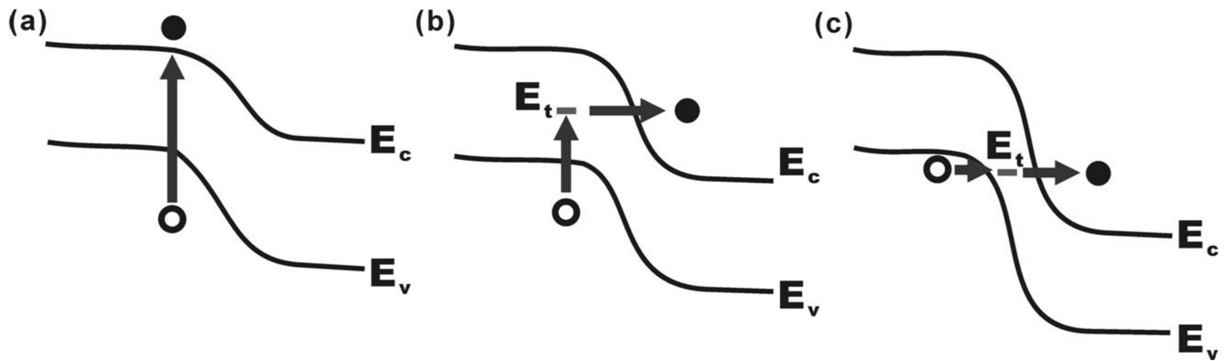


Fig. 1- 6 The band diagram for the leakage current model. (a) Case of weak electric field. (b) Case of medium electric field. (c) Case of strong electric field.

poly-Si is the first concern of this thesis.

1.5 Motivation and thesis organization

The major research subject of this thesis is Ni-metal-induced crystallization (MIC) of amorphous Si (α-Si), which has been widely employed to fabricate low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs). However, the high leakage current is an annoying issue of MIC TFTs because Ni residues trapped inside the MIC poly-Si films. The Ni residues could be reduced by gettering method or metal-induced crystallization through a cap layer (MICC). Gettering method was an efficient technology to capture Ni residues from poly-Si, but the process was complex and the on-state current of poly-Si films decreased. MICC used a SiNx cap layer to reduce Ni diffusion into poly-Si film, however that still needed high temperature and long annealing time, and the Ni degree of reduction is not

conspicuous. Besides, these two methods need extra expensive and complicated vacuum instrument. However, both methods are complex and incur high cost. Additionally, a hydrogen plasma treatment process has been utilized to eliminate the trap states of poly-Si film to improve the on-state current. However, the hydrogen concentration in the poly-Si film was hard to control, and the formed Si-H bonds were too weak to resist the hot carrier generation. Therefore, the main purpose of this thesis is to reduce Ni residues, to improve electrical performance of MIC TFTs, and further to investigate the effects of Ni concentration on others of importantly electrical characteristics.

The thesis is divided into five chapters listed following:

In chapter 1, overview of low temperature polycrystalline silicon TFT technology is reviewed, then the processes of low temperature crystallization of amorphous silicon, Issues of polycrystalline silicon films, and electrical characteristics of Ni-metal induced crystallization (MIC) TFTs. Finally, the motivation of this study and the outline of the dissertation are provided.

In chapter 2, a chemical oxide filter layer was introduced into MIC processes to reduce the Ni residues in poly-Si films, which was simple and without extra expensive instrument. The optimum thickness of chemical oxide layer in Ni reduction was extracted to fabricate TFT devices. Moreover, the electrical performance of MIC TFTs with and without chemical oxide was investigated.

In chapter 3, effect of Ni concentration on electrical characteristics of MIC TFTs was studied, including source/drain (S/D) series resistance, bias reliability and thermal stability. In this work, the transmission line method (TLM) test structure is employed to measure the S/D series resistance of a top-gate TFT device used to induce electrons into the channel. Moreover, the bias reliability and thermal stability was investigated under hot carrier condition and high temperature environment. The results of this chapter proved that how reducing Ni concentration affected the S/D series resistance, bias reliability and thermal stability.

In chapter 4, a new manufacturing method for poly-Si TFTs using drive-in Ni induced crystallization (DIC) was proposed to reduce Ni concentration and minimize the trap-state density. In DIC, F^+ implantation was used to drive Ni in the α-Si layer. To further improvement, a cap oxide layer was introduced into DIC process (DICC) to reduce ion implant damages. Simultaneously, bias reliability was also studied by using the hot-carrier stress.

In chapter 5, conclusions and future works are summarized respectively.

Chapter 2

Reduced Leakage Current of Nickel Induced Crystallization Poly-Si TFTs by a Simple Chemical Oxide Layer

2.1 Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for high resolution integrated active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light-emitting diodes (AMOLED) because they exhibit good electrical properties and can be used in the realization of system-on-glass (SOG) [47]-[48]. Intensive studies have been carried out to lower the crystallization temperature of amorphous silicon (α-Si) films. The solid phase crystallization (SPC) method is a well-established poly-Si formation technique [49]. The major drawback of SPC is that the α-Si films need to be annealed for about 24 h at 600°C, which is higher than the strain temperature of a normal glass substrate. In contrast, metal induced crystallization (MIC) and metal induced lateral crystallization (MILC) methods require a lower thermal budget and present a great on-state of electrical performance than SPC [40], [50], [51].

In MILC, Ni islands are selectively deposited on top of α-Si films and allowed to

crystallize at a temperature below 600°C. Unfortunately, the uniformity is poor, annealing time is long, and extra mask is needed to define the Ni window. In contrast, MIC method is much simple for commercial manufacturing. No extra mask is needed, the annealing time is short (0.5 - 5 h), and the uniformity is good. Compared with various metal, Ni-MIC process produces crystallized α-Si thin films of the best quality because $NiSi_2$ has the lowest lattice mismatch (0.4%) with Si [50]-[51] Unfortunately, Ni and $NiSi_2$ residues in the poly-Si film increased the leakage current and shifted the threshold voltage [52]-[53]. The Ni residues could be reduced by gettering method or metal diffusion filter layer (MICC). Gettering method was an efficient technology to capture Ni residues from poly-Si, but the process was complex and the on-state current of poly-Si films decreased [54]. MICC used a SiNx cap layer to reduce Ni diffusion into poly-Si film, however that still needed high temperature and long annealing time, and the Ni degree of reduction is not conspicuous [55]-[56]. Besides, these two methods need extra expensive and complicated vacuum instrument.

In this study, a simple chemical oxide layer was introduced between α-Si layer and Ni layer to avoid excess of Ni atoms into α-Si layer during MIC process. The manufacture processes were very simple and without extra expensive instrument. It was found that the minimum leakage current of poly-Si TFTs was greatly reduced.

2.2 Experimental procedure

N-channel poly-Si TFTs were investigated in this study. Figure 2-1 shows Schematic diagrams of process flow of chemical oxide filter MIC TFTs (CF-MIC). A 100-nm-thick undoped α-Si layer was deposited onto a 500-nm-thick oxide-coated Si wafer by low pressure chemical vapor deposition (LPCVD) system. To form chemical oxide MIC poly-Si, samples were dipped into a chemical solution of $3H_2SO_4 : 1H_2O_2$ for 20 min to form a chemical oxide filter layer on the top of α-Si. A 5-nm-thick Ni film was then deposited and subsequently annealed at 500°C for 1 h in N_2 for crystallization of α-Si. The unreacted Ni film and chemical oxide layer were then removed by wet etching.

The islands of poly-Si regions on the wafers were defined by Reactive ion etching (RIE). After cleaning process, a 100-nm-thick tetraethylorthosilicate/O_2 (TEOS) oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then a 100-nm-thick poly-Si film was deposited as the gate electrode by LPCVD. After defining the gate, self-aligned 35 keV phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} to form the source/drain and gate. The dopant activation was performed at 600°C for 24 h. A 500-nm-thick TEOS oxide layer was deposited as the passivation layer by PECVD, followed by a definition of contact holes. A 500-nm-thick Al layer was then deposited by thermal evaporation and patterned as the electrode. Finally, sintering process was performed at 400°C for 30 min in N_2 ambient.

It is worthy to note that this CF-MIC process does not need any additional annealing step and expensive vacuum equipment, and is compatible with conventional MIC processes.

For the purpose of comparison, solid phase crystallization (SPC) TFTs, and conventional MIC TFTs without chemical oxide layer were also fabricated under the same conditions.

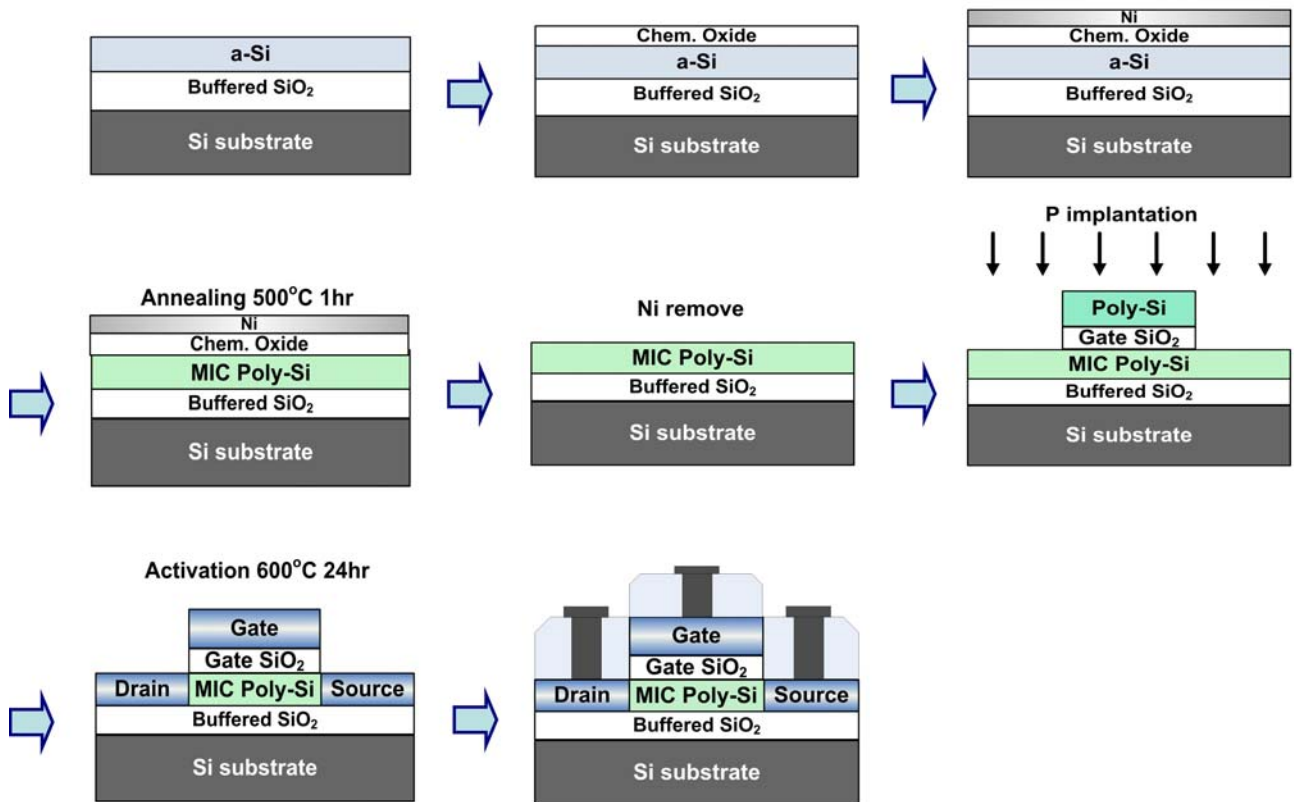


Fig. 2-1 Schematic diagrams of process flow of MIC TFTs with chemical oxide filter layer.

2.3 Results and discussion

2.3.1 Characterization of chemical oxide layer

The transmission electronic microscopy (TEM) cross-section image of chemical oxide layer was shown in Fig. 2-2. To examine the quality of chem-SiO_2, after the chem-SiO_2 layer was formed, platinum was deposited on top of the chem-SiO_2 for image contrast in TEM sample preparation. A relation of chemical oxide thickness versus immersed time was also investigated by TEM. As shown in Fig. 2-3, the chemical oxide growth controlled by diffusion of reactants through the pre-existing layer conformed to the model of oxide growth. The growth kinetic could be well represented with the expression (1) for the short time:

$$d = E \ln (1 + Ft) \quad (1)$$

where E and F are adjusted parameters proportional to the penetration depth of the species and to the concentration of the precursors, respectively [57]. In this work, there is an approximately saturation thickness of 3.4 nm after dipped for 10 min. For this reason, it is easy to achieve the same result when samples immersed into a chemical solution of $3H_2SO_4$: $1H_2O_2$ over 10 or 15 min. For purposed comparison, the stable parameter at 20 min of immersed time was chosen to investigate with conventional MIC, subsequently.

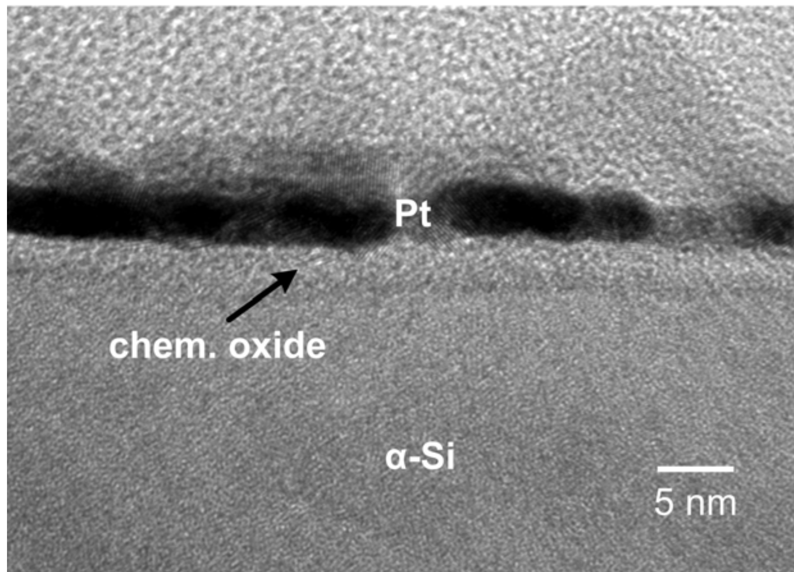


Fig. 2-2 TEM cross-section image of chemical oxide layer after dipped for 20 min. Platinum film deposited on the top of the chem-SiO_2 layer was for the TEM sample preparation.

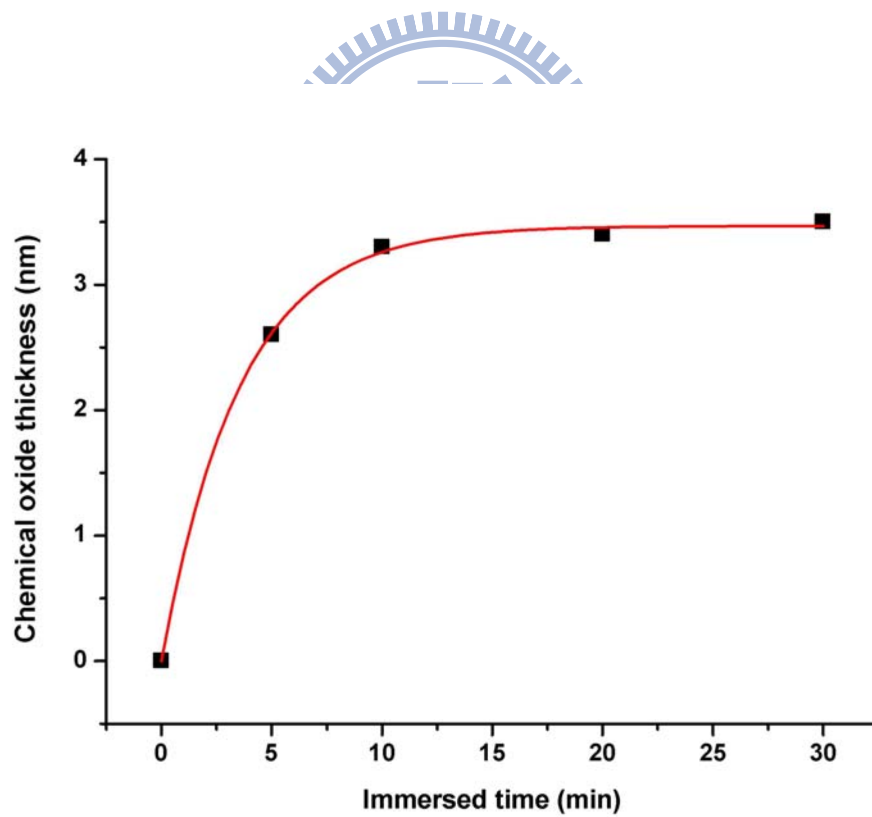


Fig. 2-3 Formation thickness of chemical oxide layer versus immersed time.

Figure 2-4 shows X-ray photoelectron spectroscopy (XPS) of Si2p peak for the chemical oxide on top of α-Si layer with 20 min dipping. Black line is the raw data and the other lines were obtained by the curve-fitting calculation. According to the detailed XPS studies of surface oxidation layer of Si, it was observed Si, SiO and SiO_2 peaks are located at binding energy of 99.6, 101.7 and 103.2 eV, respectively [58]-[60]. We believe that the signal of Si peak was obtained from the bottom layer (α-Si) because the thickness of chemical oxide layer is less than XPS sampling depth. Therefore, it can be clear to define that the chemical oxide is composed of SiO and SiO_2.

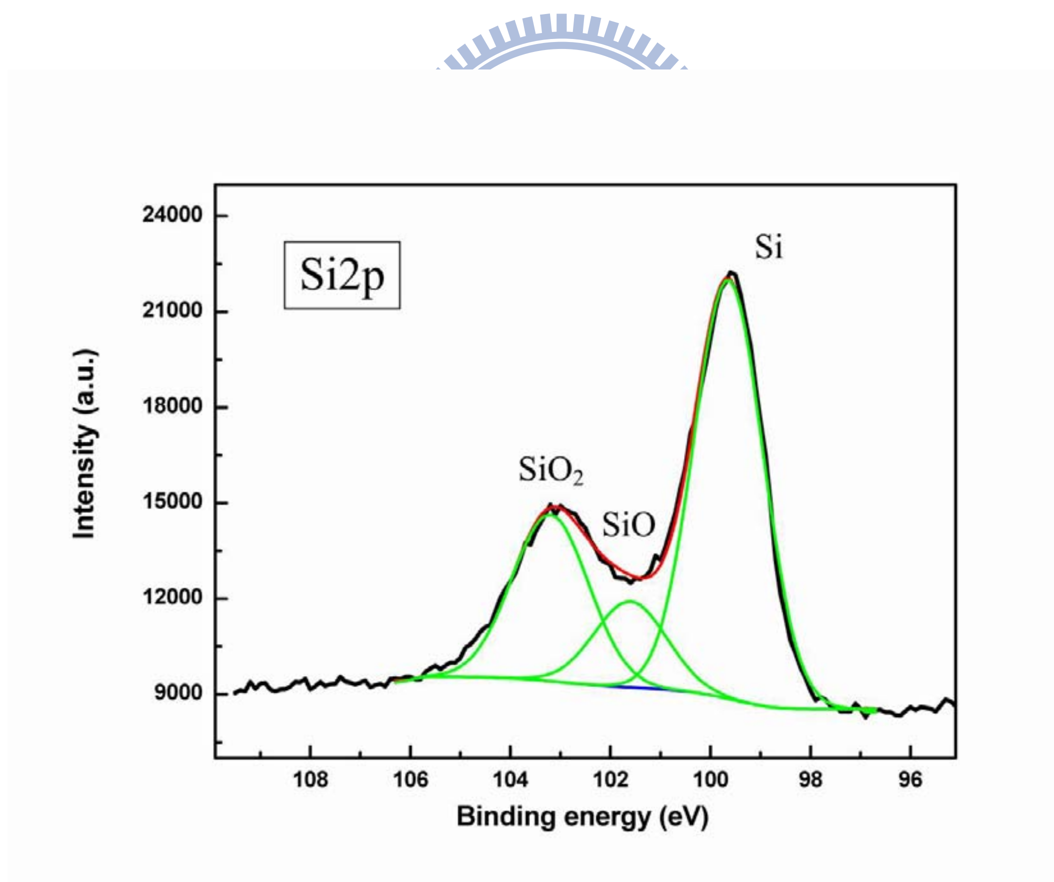


Fig. 2-4 X-ray photoelectron spectroscopy (XPS) of Si2p peak for the chemical oxide on top of α-Si layer.

2.3.2 Reduction of Ni concentration in MIC poly-Si films

To investigate the effect of chemical oxide on the reduction of Ni residues, samples were purposely dipped into a silicide-etching solution (HNO_3:NH_4F:H_2O = 4:1:50) after unreacted Ni film and chemical oxide layer were removed. As shown in Fig. 2-5, numerous holes were observed. These holes were residues of Ni silicides that had been etched away by the silicide-etching solution. The Ni residues in CF-MIC were much lower than those in conventional MIC. This reduction must be due to the introduction of chemical oxide layer in CF-MIC processes. Oxide filter layer can avoid Ni directly contact with α-Si and remove unreacted Ni easily from surface.

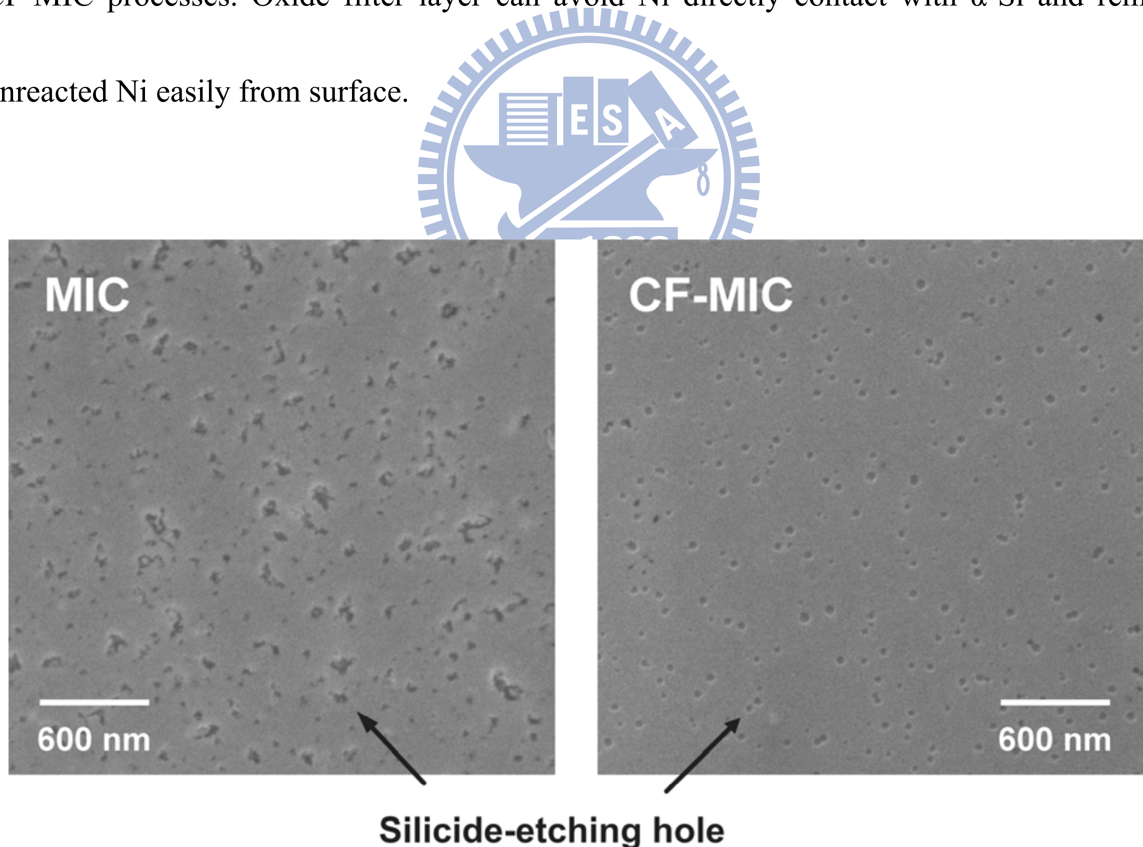


Fig. 2-5 SEM images of the silicide etching holes of MIC and CF-MIC poly-Si films.

Secondary-ion mass spectroscopy (SIMS) depth profile was also used to analyze the Ni concentrations (residues) in Si films (without silicide-etching process). As expected, Ni content in CF-MIC was much less than that in MIC as shown in Fig. 2-6. Obviously, chemical oxide layer can reduce the Ni concentrations in Si films. This is because the diffusivity of Ni in α-Si is 10^8 times higher than that in SiO_2 at 500°C [61]-[62]. As a result, chemical oxide serves as a filter, which can retard the in-diffusion of Ni into Si films. In other words, Ni concentrations in Si films were reduced.

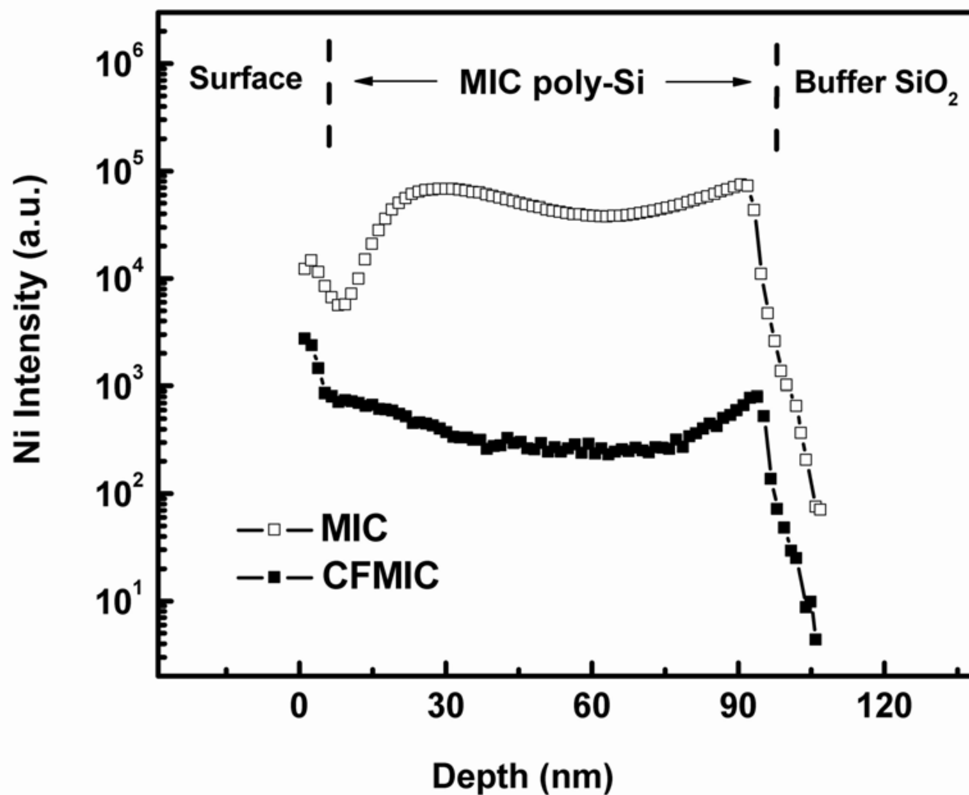


Fig. 2-6 SIMS depth profiles of nickel in the structure of MIC and CF-MIC poly-Si films.

Moreover, to investigate the Ni reduction in various thicknesses of chemical oxide layer, a relation of Ni intensity at a depth of 50 nm versus immersed time after MIC process is shown in Fig. 2-7. It conformed to the basic diffusion model to presented exponential decay as a function of immersed time and saturated at a minimum of Ni intensity after dipped for 10 min. The result indicated that the chemical oxide introduced between α-Si layer and Ni layer can greatly reduced Ni concentration in MIC TFTs depended on thickness of the chemical oxide. Hence the leakage current was improved to an optimum with the reduction of Ni concentration because of increased thickness of chemical oxide.

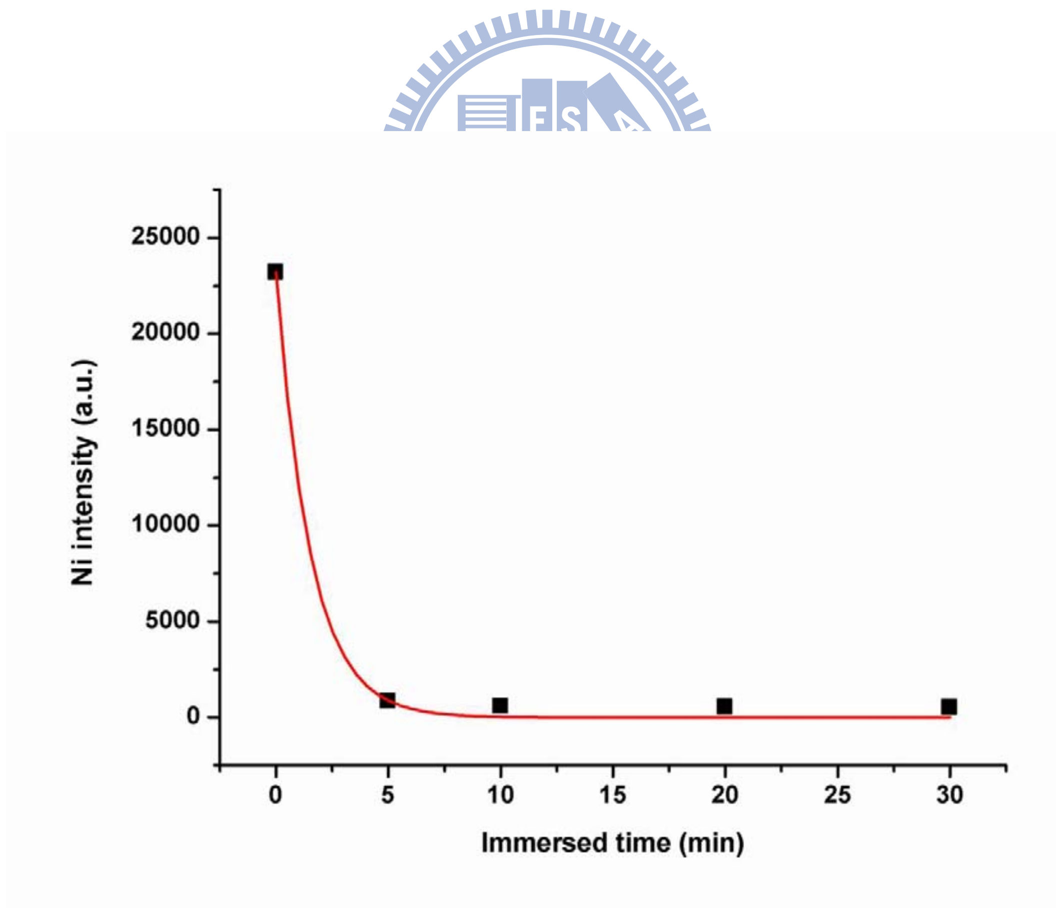


Fig. 2-7 A relation of Ni intensity at a depth of 50 nm versus immersed time by SIMS after MIC annealing.

2.3.3 Surface roughness of MIC poly-Si films after crystallization

After Ni film and chemical oxide were removed, their surfaces (without silicide-etching) were measured using atomic force microscopy (AFM) to identify the degree of texturing. As shown in Fig. 2-8, the root mean square surface (rms) roughness of CF-MIC surface (0.798 nm) was less than that of CF-MIC surface (1.348 nm). These results are in agreement with the MICC studies of Choi et al. [56], who found that MIC with cap layer can achieve a clean and smooth surface.

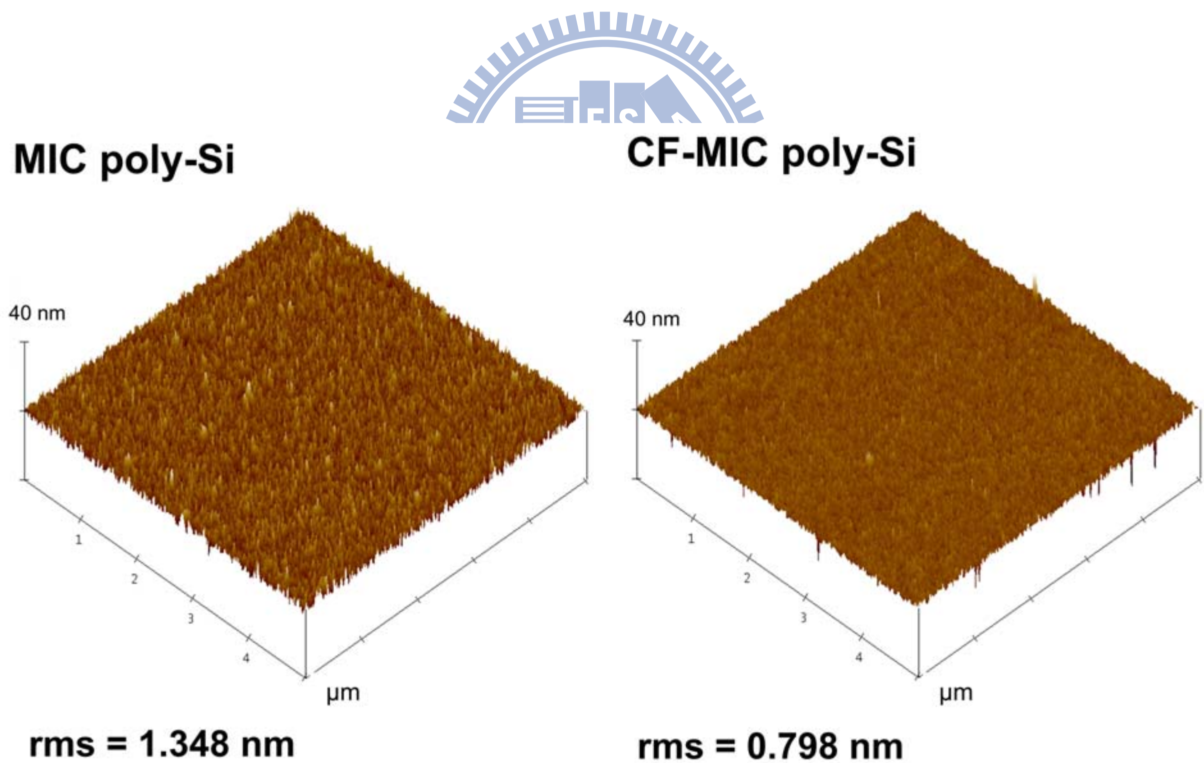
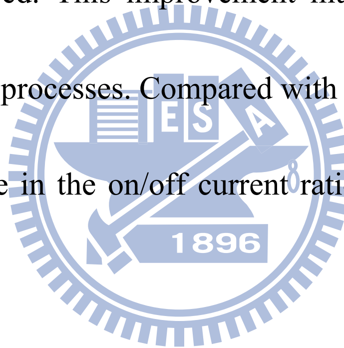


Fig. 2-8 surface roughness of MIC and CF-MIC poly-Si films

2.3.4 Electrical performance of MIC and CF-MIC TFTs

Figure 2-9 exhibits the I_D–V_G transfer characteristics of TFTs at a drain bias of 5 V. The device parameters were extracted at W/L = 10/10 μm, and ten TFTs were measured. The average values with standard deviations in parentheses were shown in Table 2-1. The threshold voltage (V_{th}) is defined at a normalized drain current of I_{DS} = (W/L) × 100nA at V_{DS} = 5V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at V_{DS} = 0.1V. As shown in Table 2-1, the electrical characters of CF-MIC TFTs were significantly improved. This improvement must be due to the introduction of chemical oxide layer in CF-MIC processes. Compared with conventional MIC TFTs, CF-MIC TFTs shows a 17.3-fold increase in the on/off current ratio and a 14.3-fold decrease in the minimum leakage current.



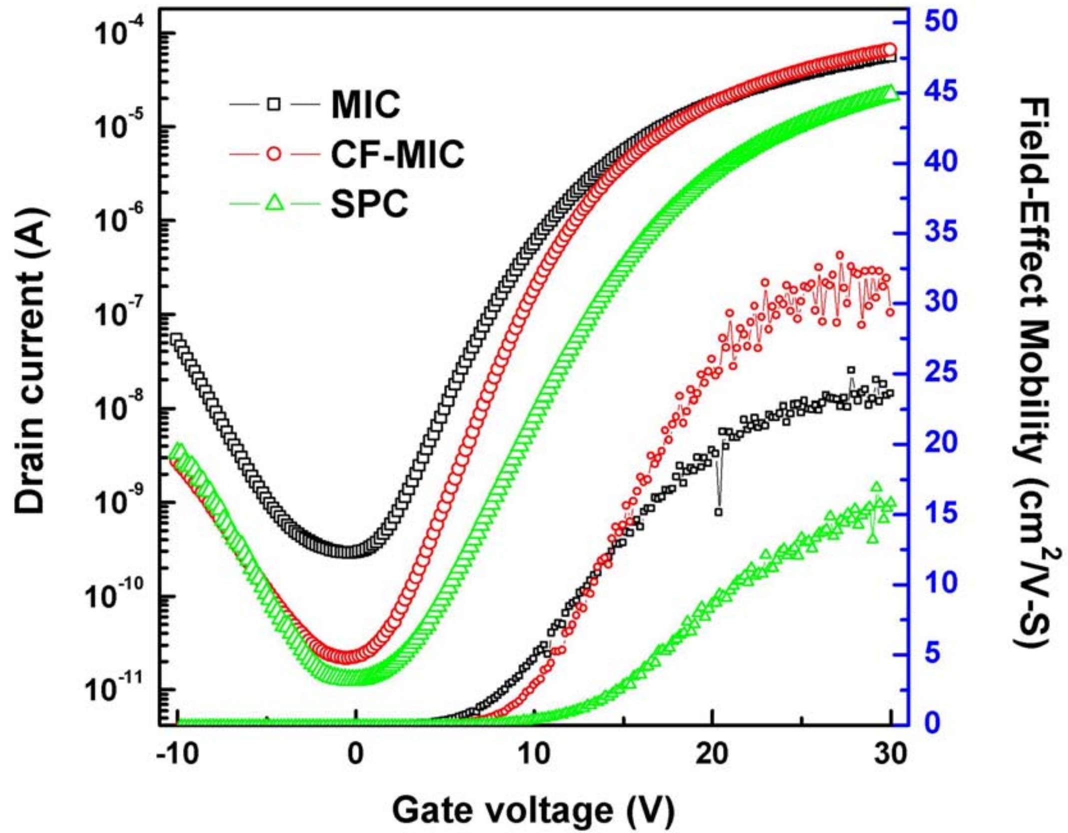


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Fig. 2-9 Typical I_{DS}-V_{GS} transfer characteristics and filed-effect mobility of of MIC, CF-MIC and SPC TFTs (W / L = 10 / 10 μm)

Table 2-1 Average device characteristics of MIC, CF-MIC and SPC TFTs with standard deviations in parentheses

W / L = 10 / 10 μm	MIC	CF-MIC	SPC
μ_{FE}(cm^2/V-S)	25.5 (2.39)	35.8 (2.65)	17.0 (1.26)
Vth (V)	7.11 (0.81)	8.73 (0.88)	13.02 (0.18)
S.S (V/decade)	1.86 (0.14)	1.81 (0.12)	1.83 (0.14)
Imin (pA/ μ m)	30.00 (3.71)	2.10 (0.12)	1.26 (0.08)
Max on/off ratio (10^5)	2.08 (0.48)	35.98 (5.21)	18.67 (1.18)

The leakage current improvement was attributed to the reduction of Ni concentration in the CF-MIC films. It is known that Ni-related defects might degrade electric performance because the trap states introduced dangling bonds and strain bonds [63]. The chemical oxide layer reduced content of Ni (Ni-related defect) into channel layer during MIC annealing process. With the reduction of the Ni concentration, the minimum leakage current was reduced and therefore the on/off current ratio was increased [64]-[65]. In addition, the carrier mobility also increased due to lower impurity scattering of Ni-related defects and grain boundaries. However, the V_{th} of CF-MIC was showed a positive shift compared with conventional MIC. The result is similar to earlier findings suggesting that the negative shift of V_{th} was caused by positive charge in high Ni residues poly-Si film [54].

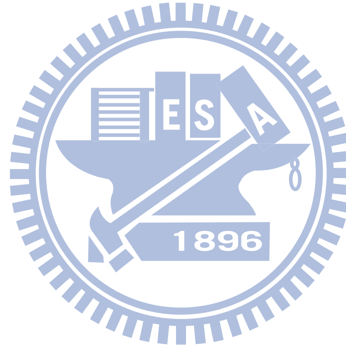
The electrical performances of SPC TFTs were also measured. As shown in Table 2-1, Fig. 2-9, the on/off current ratio of CF-MIC TFTs was higher than that of SPC TFTs. The leakage current of CF-MIC TFTs was as low that of SPC TFTs. This also demonstrated the reduction of Ni residues through the introduction of chemical oxide layer.

2.3.5 Influence of grain size on field-effect mobility

In general, the grains of MIC were crystallized from top to down and formed needle-like MIC grains [66]. Figure 2-10 shows the plane-view images of transmission electronic microscopy (TEM) of poly-Si films. The grain diameters of MIC and CF-MIC were

approximately 8~10 nm and 15~18 nm, respectively. The variation of grain size was attributed to the different Ni concentration during MIC annealing process [67]. The amount of nucleation site of $NiSi_2$ in MIC is higher than that in CF-MIC due to higher Ni concentration. Therefore, the grain size of MIC was less than that of CF-MIC.

In the MIC poly-Si films, dangling bonds in grain boundaries serve as the trapping centers, which trap many free carriers (either electrons or holes) and consequently hinder carriers from conduction [33]-[35]. For this reason, the field-effect mobility increased from 25.5 to 35.8 $cm^2 V^{-1} S^{-1}$ owning to the larger grain size in CF-MIC.



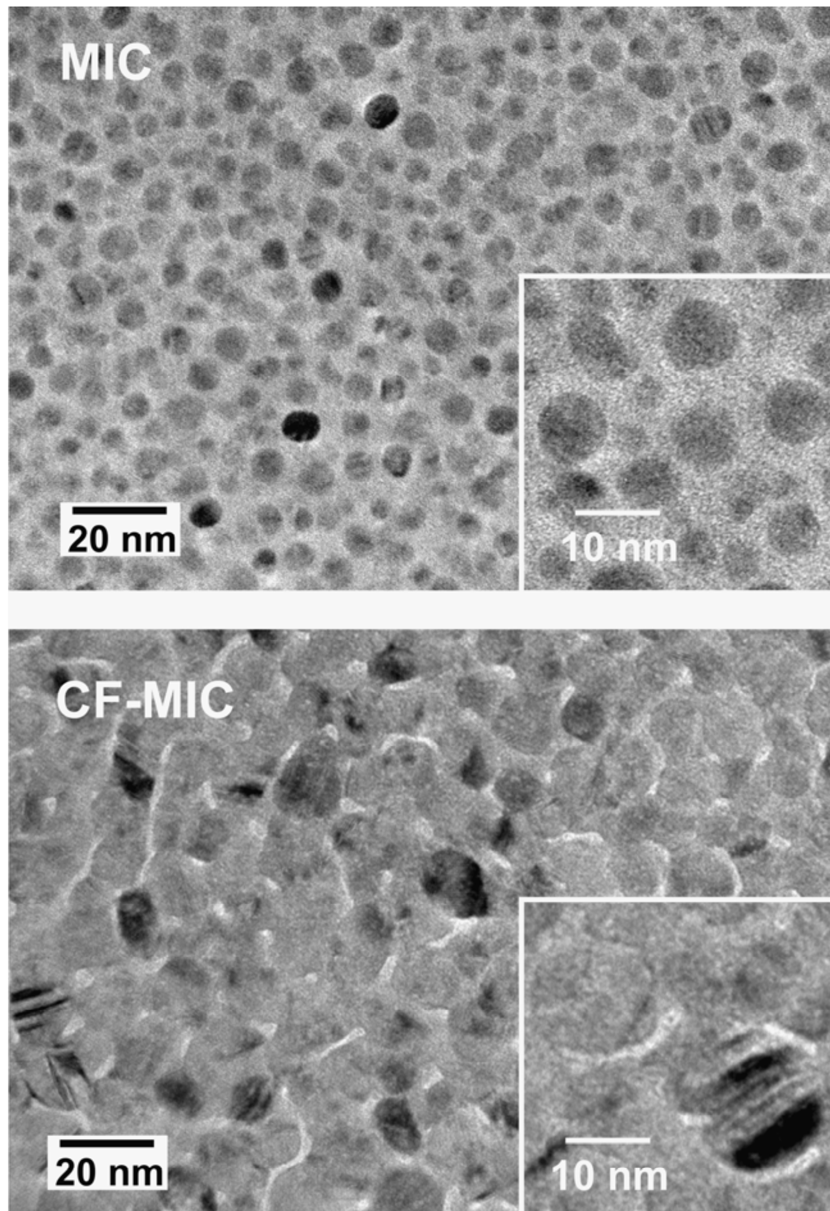


Fig. 2-10 The plane-view images of transmission electronic microscopy (TEM) of MIC and CF-MIC poly-Si films.

2.4 Summary

The chemical oxide filter layer was introduced into MIC processes to reduce the leakage current of MIC TFTs. The process was very simple and without extra expensive instrument. It just added α-Si coated sample into chemical solution before depositing the Ni film. The chemical oxide growth controlled by diffusion of reactants through the pre-existing layer conformed to the model of oxide growth and there is a saturation thickness of 3.4 nm after dipped for 10 min. It was also found that it conformed to the basic diffusion model to presented exponential decay as a function of immersed time and saturated at a minimum of Ni concentration after dipped for 10 min.

As the results, the electrical performance of MIC TFTs with chemical oxide layer was significantly improved, including in higher field-effect mobility, superior subthreshold slope, and higher on/off current ratio. Compared with conventional MIC TFTs, CF-MIC TFTs shows a 14.3-fold decrease in the minimum leakage current and a 17.3-fold increase in the on/off current ratio. This is because the chemical oxide layer can avoid Ni directly contact with α-Si, avoid excess of Ni atoms into α-Si layer and remove unreacted Ni easily from surface.

Chapter 3

Effect of Nickel Concentration on Electrical Characteristics of MIC TFTs: Source/Drain Series Resistance, Bias Reliability and Thermal Stability

3.1 Introduction

In recent years, low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been widely applied to high resolution integrated active-matrix organic light-emitting diodes (AMOLED), which exhibit good electrical properties and can be used in the realization of glass substrate [48]. In various fabrication for LTPS, metal-induced crystallization (MIC) is promising for use owing to its low cost, good uniformity, low crystallization temperature (~500℃) and short crystallization time (0.5 - 5 h) [50]-[51]. Unfortunately, Ni and $NiSi_2$ residues in the poly-Si film increases the leakage current and shifts the threshold voltage [52]-[53]. In chapter 2, the leakage current has been significantly reduced by decreasing the Ni concentration through use of a chemical oxide filter layer (CF-MIC).

Noteworthily, while most studies have focused only on reducing Ni contamination to improve the leakage current, lowering the Ni concentration may change the source/drain (S/D)

series resistance of MIC TFTs. Inevitably, the S/D series resistance negatively influences on the device performance, especially on-state current and mobility [68]-[70]. This phenomenon becomes seriously due to increased ratio of the S/D series resistance at short channel devices. Therefore, improving the performance of MIC TFTs requires understanding in detail how the Ni concentration affects S/D series resistance. However, to our knowledge, exactly how Ni concentration and series resistance are related at the S/D region has not been examined. In the part 1, the S/D series resistance of MIC TFTs was investigated by using transmission line method [69].

Moreover, bias reliability and thermal stability became major concerns for AMOLED display applications, especially when devices are operated under hot carrier condition and high temperature environment. It is known that hot carrier stress under high gate and high drain voltages decreases on-state current and increases the threshold voltage (V_{th}) [71]-[72]. Furthermore, devices in high temperature environment show a poor thermal stability leading to large leakage current and shifts V_{th} [73]-[74]. Although reducing Ni concentration is an effective way to improve leakage current, the Ni concentration effect on bias reliability and thermal stability was also important for AMOLED display application. It is interesting how the reduction of Ni concentration affect the bias reliability and thermal stability of MIC TFTs. In the part 2, the effect of Ni concentration on bias reliability and thermal stability were investigated, which were reflected the behavior at on-state and off-state region, respectively.

In this study, exactly how the Ni concentration affects these electrical characteristics of MIC TFTs is examined by using the conventional MIC and CF-MIC to represent high and low Ni concentration devices, respectively. Results of this study demonstrate that the S/D series resistance and channel resistance were decreased with the reduction of Ni concentration in MIC poly-Si. It was also found that reducing Ni concentration in MIC films was also beneficial for bias reliability and thermal stability.

3.2 Experimental procedure

Two kinds of MIC TFTs were investigated in this study, which were fabricated by using the method in chapter 2. One is "MIC" fabricated by conventional nickel-induced crystallization with high Ni concentration, and the other is "CF-MIC" fabricated by metal-induced crystallization through a chemical oxide layer with low Ni concentration. After the devices fabrication, transfer characteristics of TFTs were measured at room temperature by using KEITHLEY 4200 semiconductor parameter analyzer.

3.2.1 Transmission line method (TLM)

In the part 1, the source/drain (S/D) series resistance of TFTs was extracted by using transmission line method (TLM). In general, the TLM method is used to determine the series resistance to conducting materials. However, in this work, the TLM test structure is employed

to measure the series resistance of a top-gate TFT devices used to induce electrons into the channel. The extraction of S/D series resistance in these gated structures differs slightly from that of conventional TLM method since the measurement is performed at various gate voltages. The method is commonly used to determine the series resistance between the source and the drain of a transistor. It is comprised of the source resistance (R_S), the channel resistance (R_{CH}) and also the drain resistance (R_D). The total series resistance ($R_{S/D}$) is the sum of the resistance seen by R_S and R_D; $R_{S/D} = R_S + R_D$. As shown in Fig. 3-1, S/D series resistances are more complex in that they also include spreading resistance from the probe to the channel and sheet resistance from the contact electrodes.

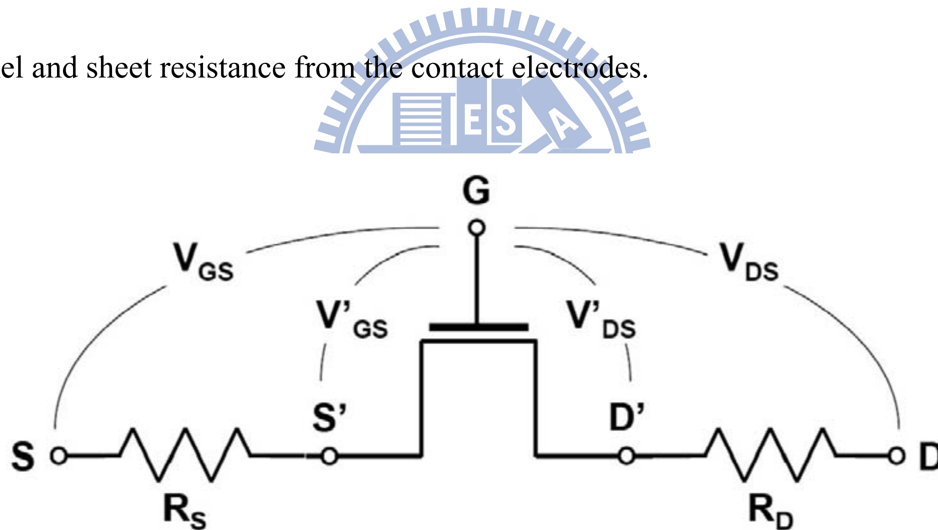


Fig. 3-1 Schematic diagrams of an intrinsic transistor with a lumped parameter representation of the S/D series resistance [75].

3.2.2 Hot carriers stress and thermal stress

In the part 2, the stressing voltage is setting at saturation region of on-state. Early studies have demonstrated that the degradation of device increased with stress voltage from 20 V to

30 V. In this case, the stress voltage was set at V_{DS} = 20 V and V_{GS} = 20 V for 7500 s [76]-[78]. In general, hot carriers are particles that attain a very high kinetic energy from being accelerated by a high electric field. These energetic carriers can be injected into normally forbidden regions of the device, as the gate dielectric, where they can get trapped or cause interface states to be generated. These defects then lead to threshold voltage shifts and on-state current degradation of TFT devices. Moreover, thermal stability was examined at elevated temperatures from 25 to 125°C. It is easy to the raise off-state curves with increase of operation temperature due to mechanism of thermionic field emission [79].

3.3 Results and discussion

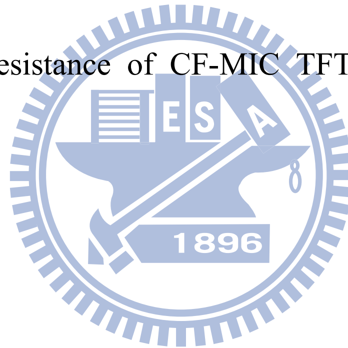
3.3.1 Effects of Ni concentration on source/drain series resistance

The transmission line method was employed to investigate the S/D series resistance ($R_{S/D}$), which is a standard approach for the extraction of the $R_{S/D}$ by fitting the ON-resistance (R_{ON}) as a function of the channel length. In the linear region of the TFT output characteristics (low drain voltage and high gate voltage), R_{ON} is assumed to consist of channel resistance (R_{CH}) and $R_{S/D}$. The ON-resistance can be estimated as the following equations:

$$R_{ON} = (\partial V_D / \partial I_D) = R_{CH} + R_{S/D}, \qquad R_{CH} = L / [W \mu_{ox} C_i (V_G - V_t)]$$

where C_i is the gate oxide capacitance per unit area and W, L, and V_t are the device channel width, length, and the intrinsic threshold voltage, respectively.

Figure 3-2 and figure 3-3 show the ON-resistance data of MIC TFTs and CF-MIC TFTs as a function of the channel length, respectively. The ON-resistance of TFTs were evaluated at V_D = 0.1 V of the TFT output characteristics. Notably, the transistors have a fixed channel width of 20 μm. The results showed that the ON-resistance increased with the increase of device channel length; a large ON-resistance in the high Ni concentration device (MIC TFTs) was also observed. By the linear fitting for different gate voltages, the interception with the y-axis indicated the S/D series resistance of TFTs. Figure 3-4 shows the extracted S/D series resistance and channel resistance as a function of the gate voltage. As the results, the S/D series resistance and channel resistance of CF-MIC TFTs were lower than those of the conventional MIC TFTs.



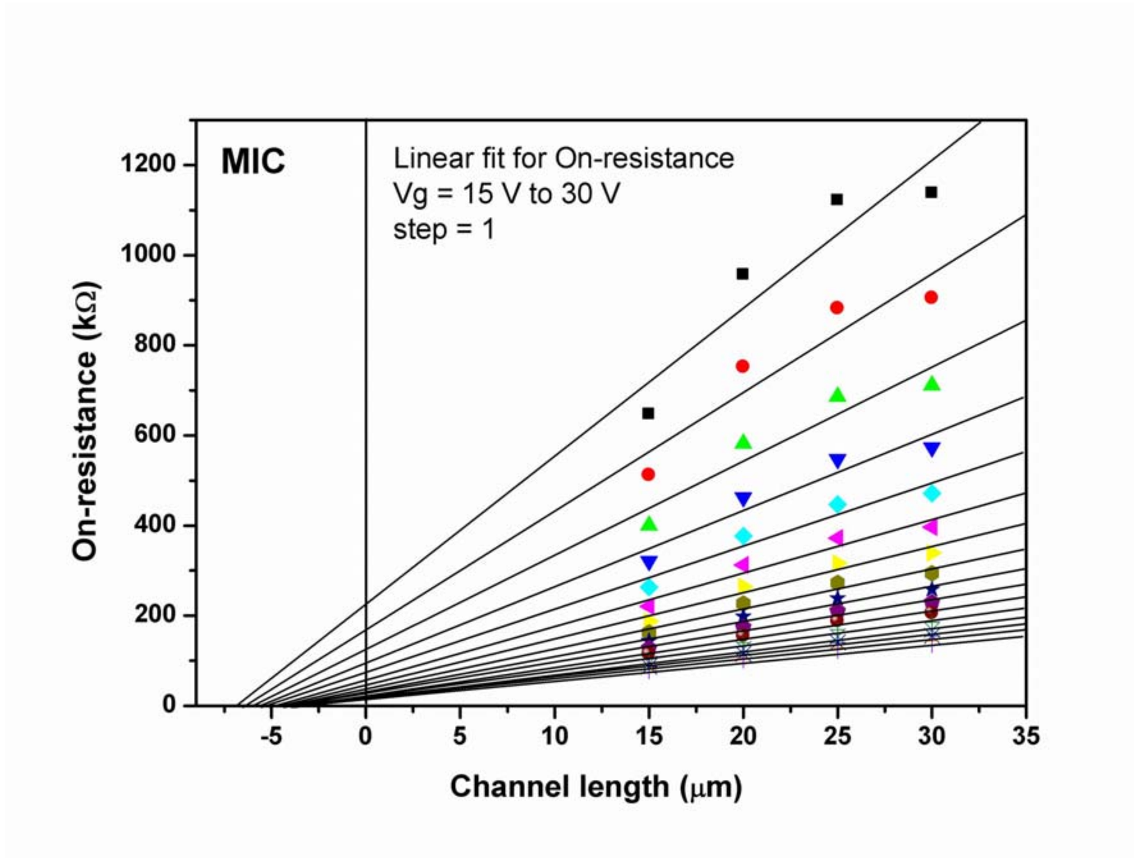


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Fig. 3-2 Measured On-resistance of conventional MIC TFTs as a function of channel length. The transistors have a channel width of 20 μm.

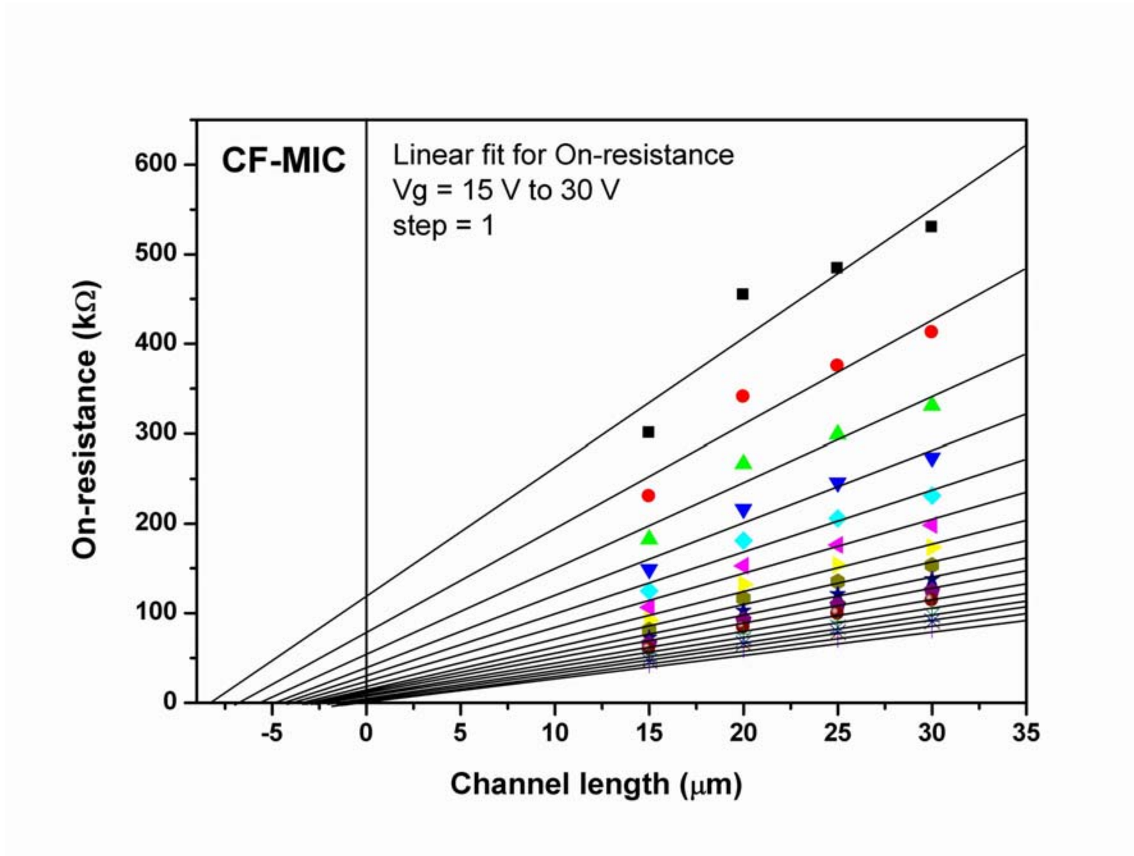

Fig. 3-3 Measured On-resistance of CF-MIC TFTs as a function of channel length. The transistors have a channel width of 20 μm.

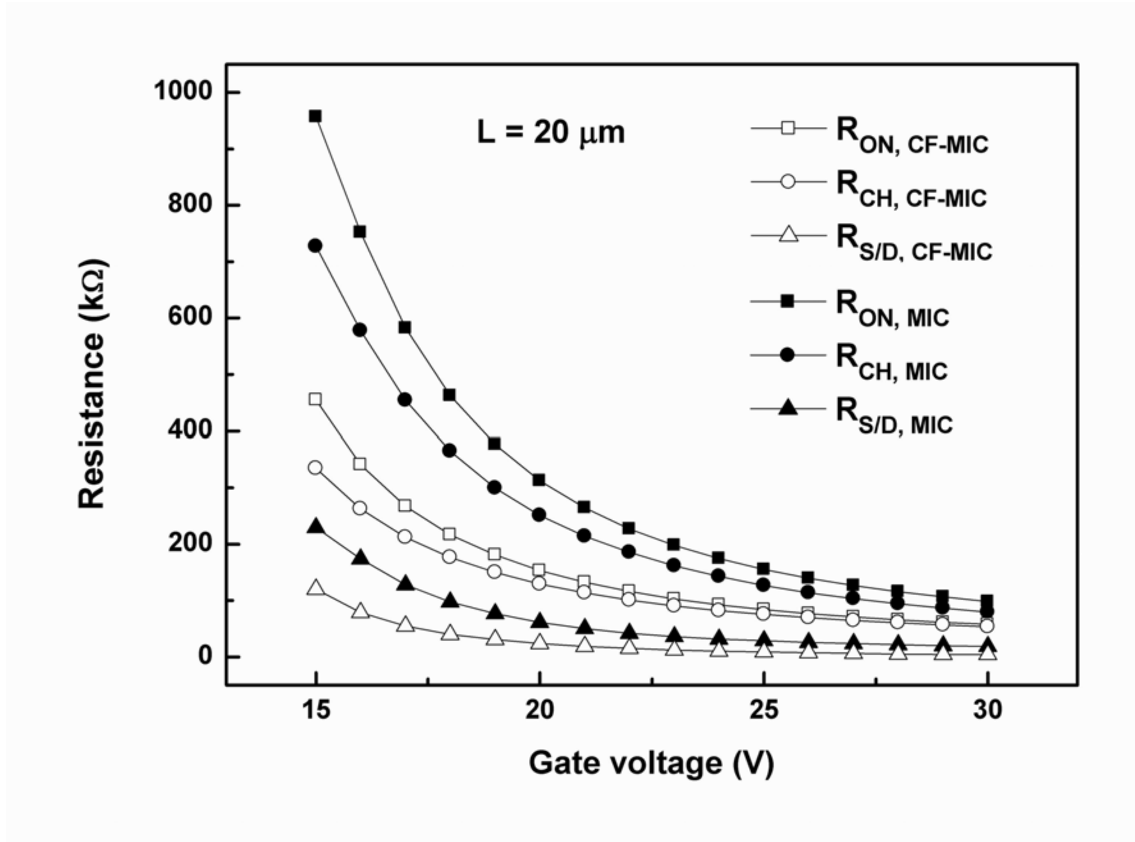

Fig. 3-4 The extracted S/D series resistance and channel resistance as a function of the gate voltage (W / L = 20 / 20 μm).

In the S/D region, the device with a high Ni concentration (MIC TFTs) exhibited a larger S/D series resistance than that of CF-MIC TFTs. Notably, the S/D series resistance can be affected by crystalline quality and dopant concentration in the S/D region. First, in terms of crystalline quality, samples were annealed at 600°C for dopant activation and re-crystallization after ion implantation because the poly-Si in S/D region was amorphized by a heavily doped implantation at a dosage of 5×10^{15} cm^{-2} [80]. Figure 3-5 shows the Raman spectra of undoped and heavily doped poly-Si films after dopant activation at 600°C for 24 h.

This figure reveals a poly-Si peak at 520 cm^{-1}. Meanwhile, no a-Si peak appears at 480 cm^{-1}, indicating that all samples are transferred to polycrystalline structure. The heavily doped poly-Si films show a lower Raman spectra intensity since re-crystallization of a-Si with Ni at 600°C is not oriented and growth is limited by formation of solid-state crystallization (SPC), subsequently lowering crystallinity in the S/D region, as shown in Fig. 3-6. Furthermore, the crystallinity of "CF-MIC + SPC" is superior to that of "MIC + SPC" because the less nucleation site of $NiSi_2$ causes a larger grain size in CF-MIC poly-Si films with a low Ni concentration [67]. However, the crystallinity of S/D region is not different in a general re-crystallization without Ni due to the only SPC mechanism. Second, the variation in S/D series resistance can also be attributed to the dopant concentration. As is well known, heavily doped implantation can significantly decrease the resistance of Si films. Unfortunately, Ni atoms serve as acceptor-like dopants in silicon [81], which counteract the effects of phosphorous doping and ultimately reduce the donor concentration in the S/D region. For this reason, high Ni concentration decreases the conductivity of the S/D region, leading to large S/D series resistance in MIC TFTs. As mentioned earlier, CF-MIC has a lower S/D series resistance than that of MIC because of a lower Ni concentration.

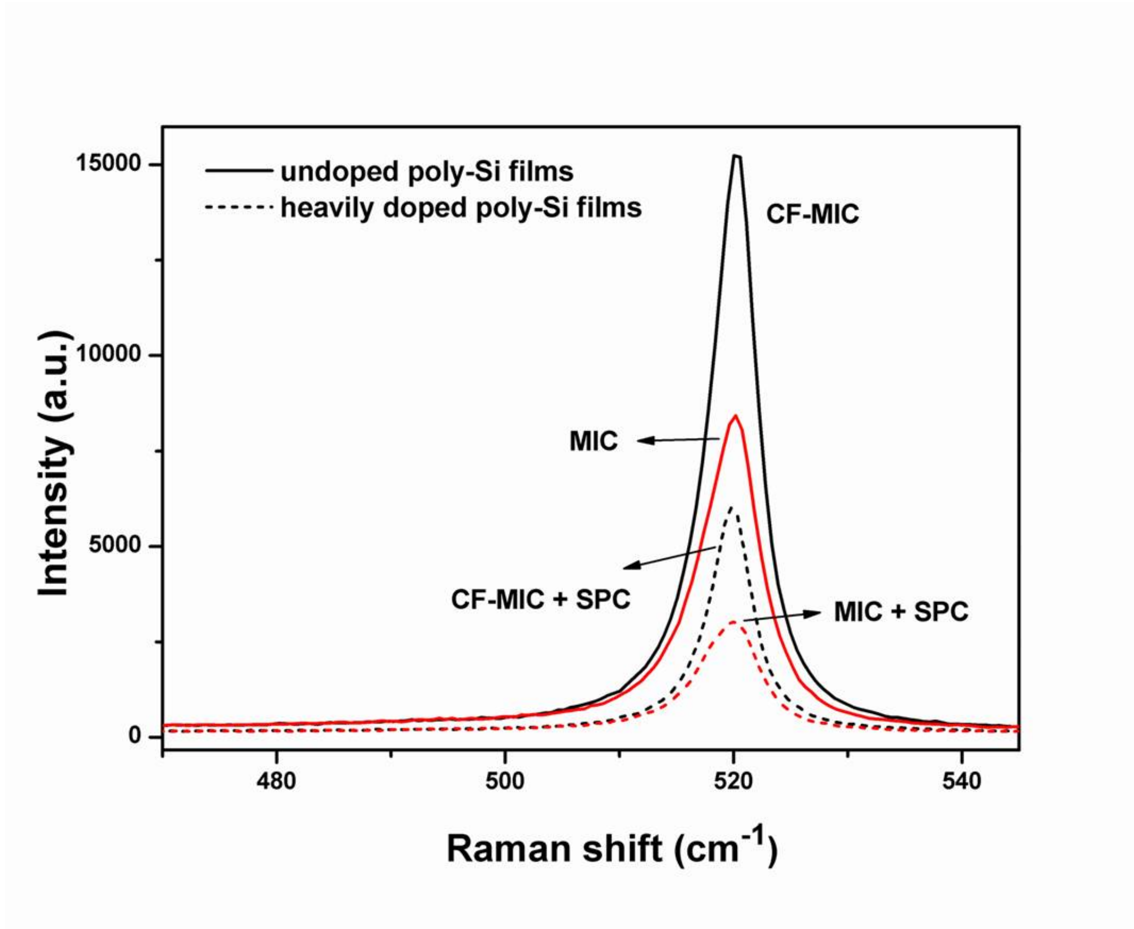

Fig. 3-5 Raman spectra of undoped and heavily doped MIC poly-Si films after dopant activation at 600°C for 24 h

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Moreover, in the channel region, MIC TFTs also shows a larger channel resistance (R_{CH}) due to the high trap-state density and impurity scattering (Ni-related defects). According to Fig. 3-5, CF-MIC presents a better crystalline quality than that of MIC at channel region. Figure 3-7 shows the effective trap state density (N_t) uses Levinson and Proano's method, which can estimate the N_t from the slope of the linear segment of ln [I_D / (V_G-V_{FB})] vs. 1 / $(V_G-V_{FB})^2$ at low V_D and high V_G, where V_{FB} is defined as the gate voltage that yields the

minimum drain current at V_D = 0.1 V [82]-[83]. Notably, the N_t of CF-MIC TFTs is 4.65×10^{12} cm^{-2}, smaller than that of MIC TFTs (6.08×10^{12} cm^{-2}). The results imply that the defects are minimized in CF-MIC TFTs due to the reduced Ni concentration. As mentioned earlier, the Ni atoms are obstructers for performance and S/D conductivity of the MIC TFTs. These results verified that it is an efficient means to improve the electrical characteristics of a channel and S/D region by reducing the Ni concentration in MIC TFTs.

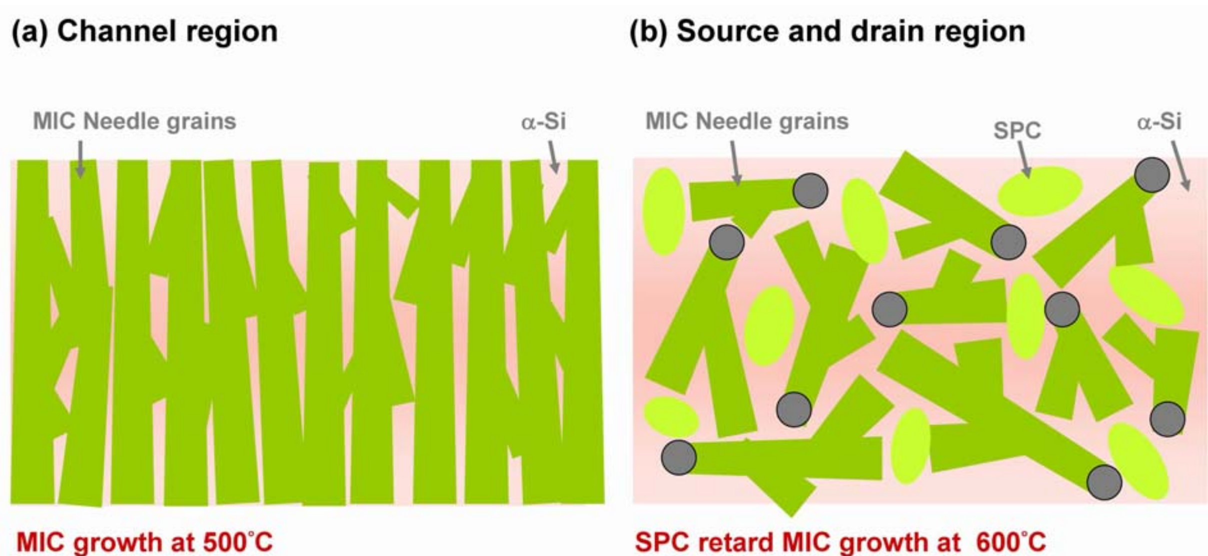
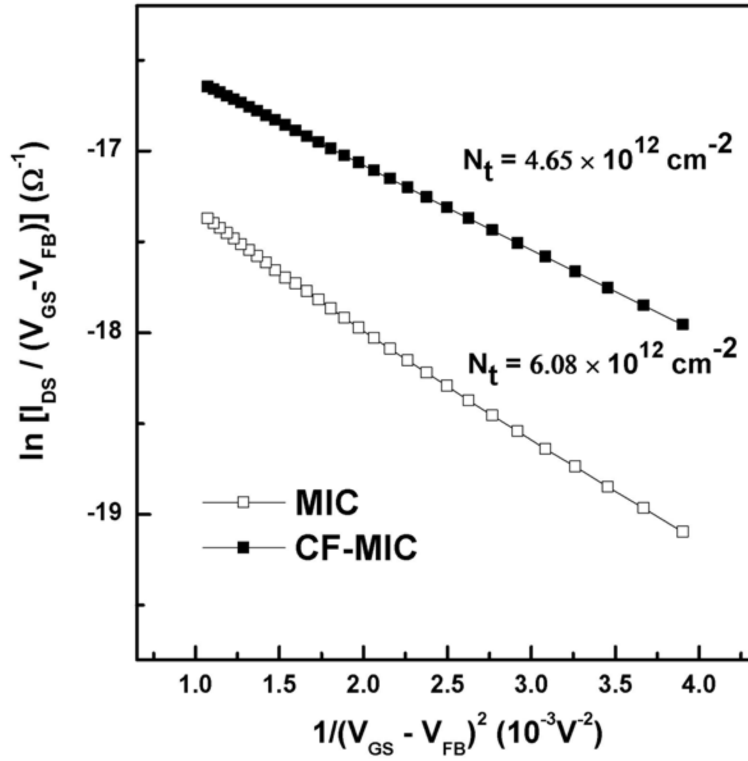


Fig. 3-6 Schematic diagrams of MIC growth at at 500°C and SPC retard MIC growth at 600°C .



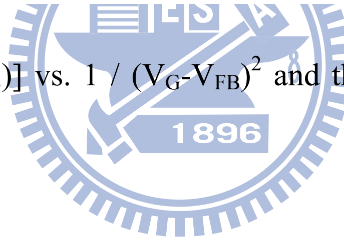


Fig. 3-7 Plot of ln [I_D / (V_G-V_{FB})] vs. 1 / $(V_G-V_{FB})^2$ and the extracted trap state density of MIC and CF-MIC.

3.3.2 Effects of Ni concentration on bias reliability

According to AMOLED display application, the bias reliability and thermal stability are considerably strict, compared to conventional AMLCD. Firstly, the bias reliability was examined under hot-carrier stress, which were performed at V_{DS} = 25 V and V_{GS} = 25 V for 7500 s. As shown in Figs. 3-8 and 3-9, the threshold voltage (V_{th}) is defined at a normalized drain current of I_{DS} = (W/L) × 100nA at V_{DS} = 5V, and the on-state current is defined at drain current at V_{GS} = 25V. The threshold voltage and the on-state current of devices were both

degraded because deep traps states were generated from the broken weak Si-Si and Si-H bonds [84]. Compared with conventional MIC, CF-MIC exhibits lower degradation in on-state current and threshold voltage shift. The results indicate that CF-MIC possess high immunity against the hot-carrier stress with reduction of Ni concentration. As mention earlier, the low Ni residues device (CF-MIC) presented the large grain size due to less nucleation site of $NiSi_2$. As shown in Fig. 3-10, there are many weaker Si-H and Si-Si bonds at grain boundary. CF-MIC is formed with larger grain size accompanied by fewer grain boundaries, hence leading to improved electrical reliability [85]-[86].

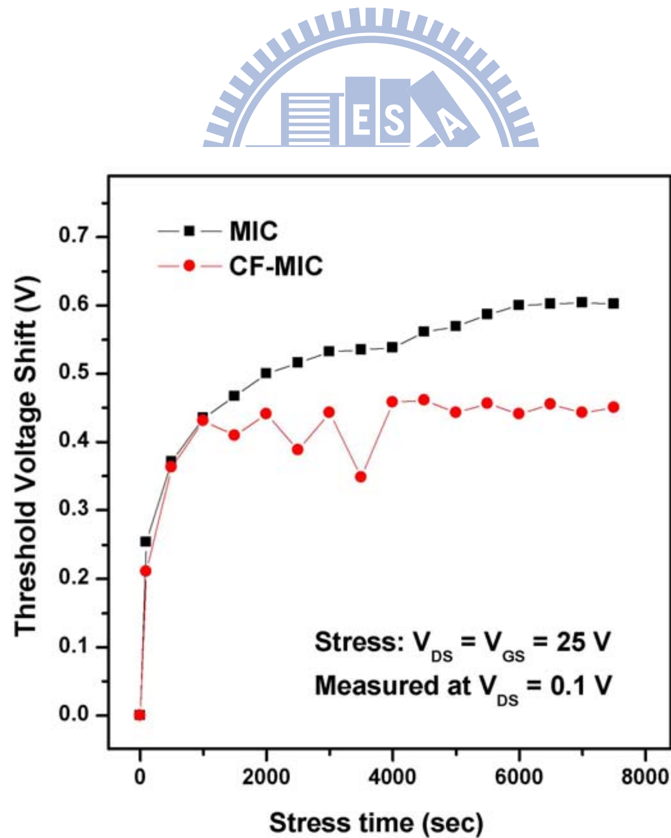
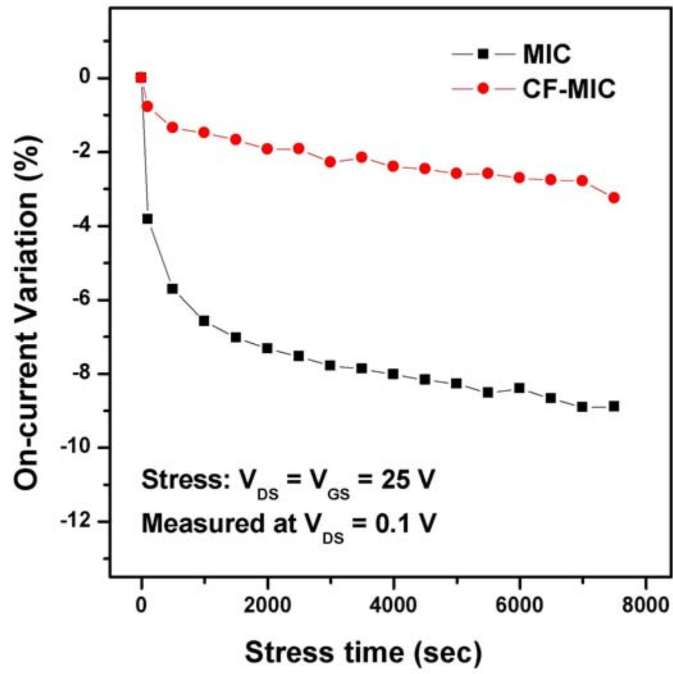


Fig. 3-8 Variation of threshold voltage versus hot-carrier stress time for MIC and CF-MIC.



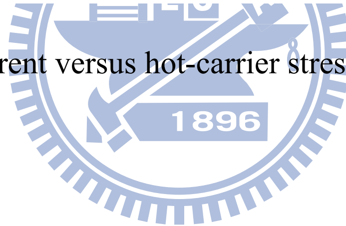


Fig. 3-9 Variation of on-state current versus hot-carrier stress time for MIC and CF-MIC

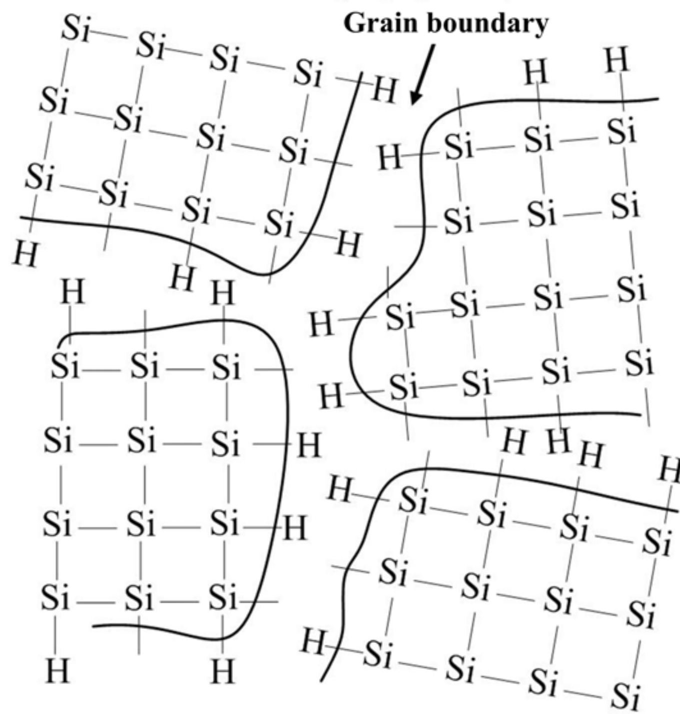
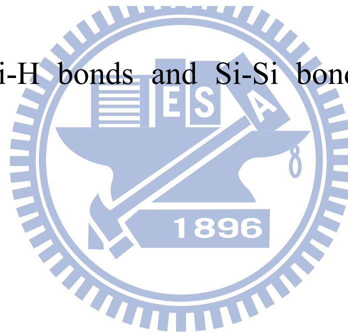


Fig. 3-10 Schematic weaker Si-H bonds and Si-Si bonds at MIC grain boundaries of plane-view.



3.3.3 Effects of Ni concentration on thermal stability

Also of concern is the thermal stability, which was examined at elevated temperatures. Figure 3-11 presents the I-V curves of the MIC and CF-MIC, which were performed at temperature from 25 to 125°C. As can be seen, the off-state curves were raised with increase of operation temperature. The threshold voltage shift and off-state current as a function of temperature were summary in Fig. 3-12. As the results, the threshold voltage and the minimum leakage current of devices were degraded with increasing the operation temperature. This is because nickel related donor-like defects were easy to release electrons when

operation temperature increased, thus increasing the leakage current and the negative shift of V_{th} [73], [87]. Compared with those of MIC, the thermal stability of CF-MIC was improved by introducing a chemical oxide layer, which is due to the reduction of Ni concentration in devices. Consequently, the increase of the leakage current and the negative shift of V_{th} of CF-MIC was less than that of MIC. In a word, it is a appropriate course to reduce Ni concentration in MIC TFTs, which shows not only better on-state reliability at bias stress but also better off-state stability at elevated temperature.

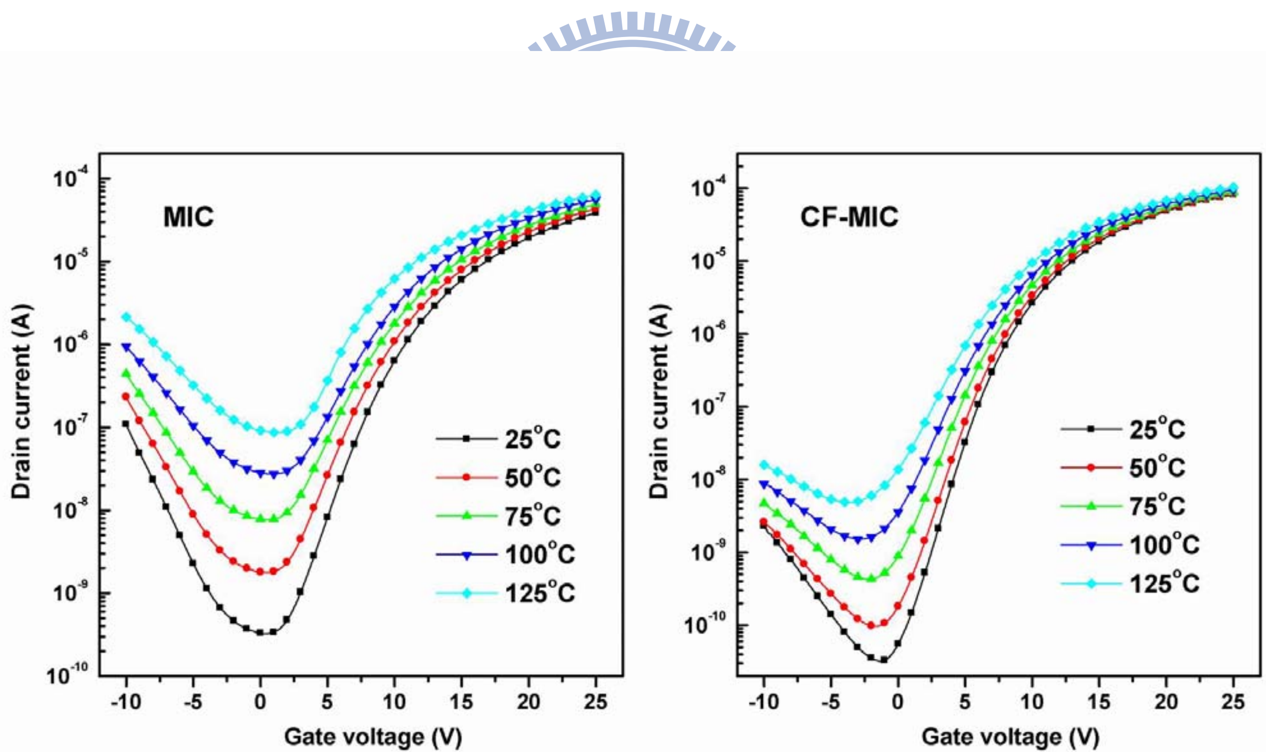


Fig. 3-11 I-V curves of the MIC and CF-MIC at temperature from 25 to 125°C .

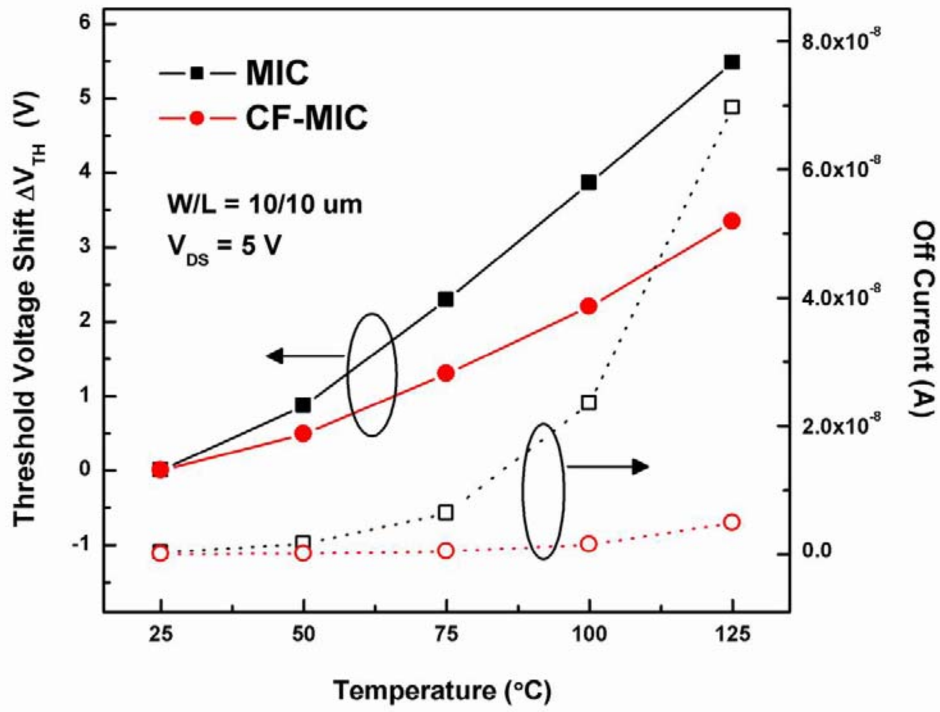


Fig. 3-12 Degradations of the threshold voltage and the minimum leakage current versus temperature at V_{DS} = 5 V.

3.4 Summary

It is well known that reducing Ni concentration in MIC films is an effective way to improve leakage current. This study investigated how Ni concentration affects electrical characteristics of MIC TFTs, such as S/D series resistance, bias reliability and thermal stability. For comparison, high and low Ni concentration devices were formed by using MIC TFTs with and without a chemical oxide layer, respectively.

In the part 1, we have provided further insight into how Ni concentration and resistance of MIC TFTs are related. Consequently, the channel resistance and S/D series resistance were decreased with the reduction of Ni concentration in MIC poly-Si due to better crystalline quality and lower degradation of donor concentration. This phenomenon is owing to that low Ni concentration formed less nucleation site of $NiSi_2$ to cause large grain size; Ni atoms serve as acceptor-like dopants in silicon, which counteract the effects of n-type doping, subsequently reducing the donor concentration in the S/D region.

In the part 2, the Ni concentration effect on bias reliability and thermal stability were investigated under hot carrier stress and elevated temperature, respectively. We have proved that reducing Ni concentration in MIC films was also beneficial for bias reliability and thermal stability. As the results, the low Ni residues device (CF-MIC) presented high immunity against the hot-carrier stress because larger grain size and fewer weak Si-H bonds. Moreover, it was also found that reducing Ni concentration can alleviate the degradations of

threshold voltage and off-state current at elevated temperatures because nickel related donor-like defects were easy to release electrons with increase of operation temperature.

In sum, results of chapter 2 and chapter 3 demonstrate that the Ni residues obstruct the performance, S/D conductivity, bias reliability and thermal stability. Consequently, these findings verified that reducing Ni residues is a significant way to improve electrical characteristics of MIC TFTs.

Chapter 4

Improved electrical characteristics and reliability of MIC TFTs Using Drive-In Nickel Induced Crystallization

4.1 Introduction

For use in active-matrix liquid crystal displays (AMLCDs) active-matrix organic light-emitting diodes (AMOLED), low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest because they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates [47]-[48]. Intensive studies have been carried out to reduce the crystallization temperature and time of amorphous silicon (α-Si) films. Metal-induced crystallization (MIC) is one of these efforts. The advantages of MIC include low cost, good uniformity, low crystallization temperature (~500℃) and short crystallization time (0.5 to 5 h). Unfortunately, Ni and $NiSi_2$ residues in the poly-Si film increased the leakage current and shifted the threshold voltage [52]-[53]. Therefore, Ni concentration in MIC poly-Si should be reduced to improve the off-state current. The atomic layer deposition (ALD) technology and gettering method have been employed to reduce the amount of undesired metal impurity. However, both methods are

complex and incur high cost [88]-[89], notably the device performance in on-state current is decreased [54].

To increase on-state current, hydrogen has been employed to eliminate the intragrain and grain boundary trap states in the poly-Si film [90]-[92]. However, the hydrogenated poly-Si TFTs suffer from a serious reliability issue, which is attributed to the weak Si-H bonds. Recent, several studies have devotedly demonstrated that introduction of fluorine (F) atoms can improve the performance and reliability of poly-Si TFTs, especially under electrical stress owning to strong Si-F bonds more stable than Si-H bonds [76], [93]-[94]. Unfortunately, the minimum off-state currents were almost unchanged, probably because the Ni concentration was constant.

This study proposes two processes for improving the performance of MIC TFTs. In the part 1, a new manufacturing method for poly-Si TFTs using drive-in Ni induced crystallization (DIC) was proposed. In DIC, F^+ implantation was used to drive Ni in the α-Si layer. In the part 2, a chemical oxide layer was introduced between the Ni and α-Si layer. With these two processes, the electrical performances of TFTs were both improved. Moreover, thermal stability and bias reliability of fluorinated MIC TFTs were investigated.

4.2 Part 1: Investigation of driven-in Ni induced crystallization (DIC)

F^+ implantation was used to drive Ni in the α-Si layer to induce crystallization (DIC) process to reduce the Ni concentration and replace weak Si-H bonds of MIC TFTs. The devices characteristics and thermal stability of fluorinated MIC TFTs were investigated.

4.2.1 Experimental procedure

N-type self-alignment poly-Si TFTs were investigated in this study. The preparation of DIC poly-Si began with four-inch Si wafer. A 100-nm-thick undoped α-Si layer was deposited onto a 500-nm-thick oxide-coated Si wafer by low pressure chemical vapor deposition (LPCVD) system. A 5-nm-thick Ni film was then deposited. Samples were subjected to F^+ implantation to drive Ni in the α-Si layer, as shown in Fig. 4-1(a). The projection range was set at the 15 nm of depth near surface of the α-Si layer. In this study, two dosages of F+ were used, 2×10^{13} and 2×10^{14} cm^{-2}. They were denoted as DIC-13 and DIC-14, respectively. The ion-accelerating energy was 10 KeV. To reduce the Ni contamination, the remained Ni film was then removed by a mixed solution of H_2SO_4 and H_2O_2 (Fig. 4-1(b)), and subsequently annealed at 500°C for 1 h in N_2.

TFT devices were fabricated by standard IC processes. As shown in Fig. 4-1(c), the islands of poly-Si regions on the wafers were defined by Reactive ion etching (RIE). Next, a 100-nm-thick tetraethylorthosilicate/O_2 oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then a 100-nm-thick poly-Si film

was deposited as the gate electrode by LPCVD. After defining the gate, self-aligned 35 keV phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} to form the source/drain and gate. Dopant activation was performed at 600°C in N_2 ambient for 12 h. After dopant activation, a 500-nm-thick SiO_2 layer was deposited by PECVD as passivation layer. Contact holes were formed and a 500-nm-thick Al layer was then deposited by thermal evaporation and patterned as the electrode as shown in Fig. 4-1(d). Sintering process was performed at 400°C for 30 min in N_2 ambient.

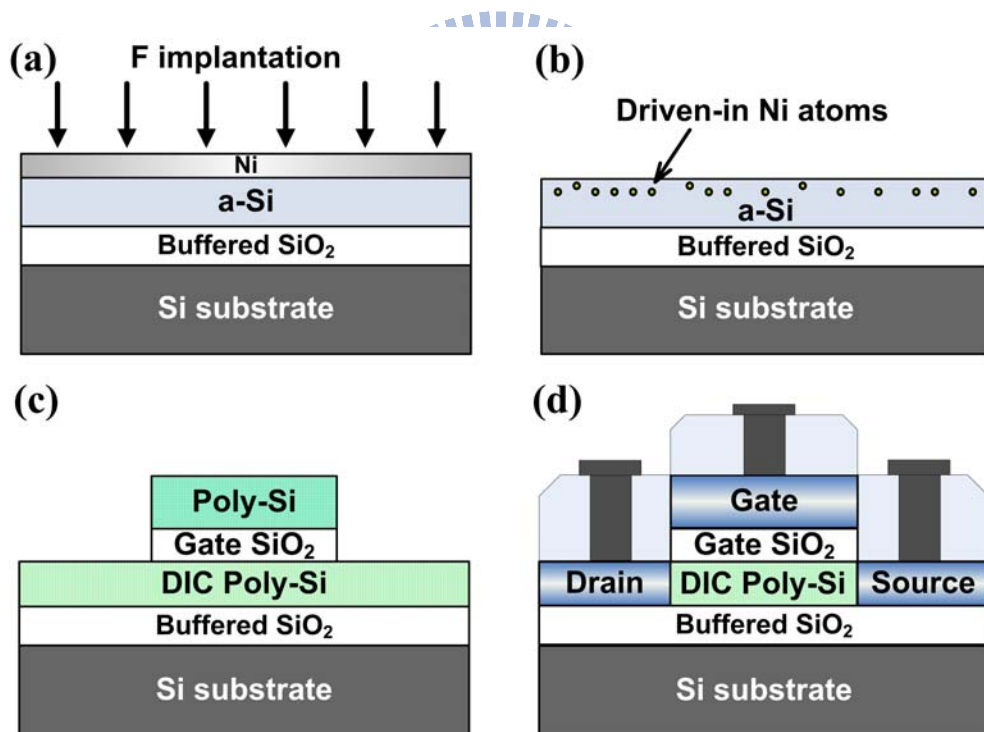
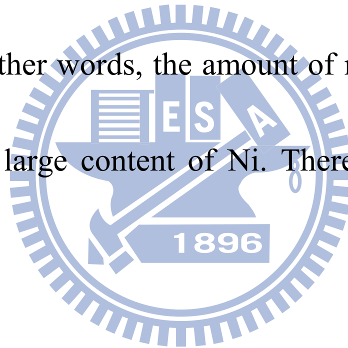


Fig. 4-1 Schematic illustration of DIC TFT fabrication process: (a) F^+ implantation to drive Ni in the α-Si layer, (b) removing of remained Ni film, (c) fabrication of TFT devices by standard IC processes, and (d) formation of source/drain and gate.

4.2.2 Results and discussion

4.2.2.1 Grain size and Ni concentration of MIC and DIC poly-Si film

The plane-view images of transmission electronic microscopy (TEM) were shown in Fig. 4-2. The grain diameters of MIC, DIC-13 and DIC-14 were 8~10 nm, 10~12 nm and 10~12 nm, respectively. The variation of grain size was attributed to the different Ni concentration during MIC annealing process. Figure 4-3 shows the secondary-ion mass spectrometry (SIMS) depth profiles of Ni in the structure of poly-Si films. As a result, Ni concentration in DIC was much lower than that in MIC because the DIC process did reduce Ni content in poly-Si films. In other words, the amount of nucleation site of $NiSi_2$ in MIC is higher than that in DIC due to large content of Ni. Therefore, the grain size of MIC was smaller than that of DIC.



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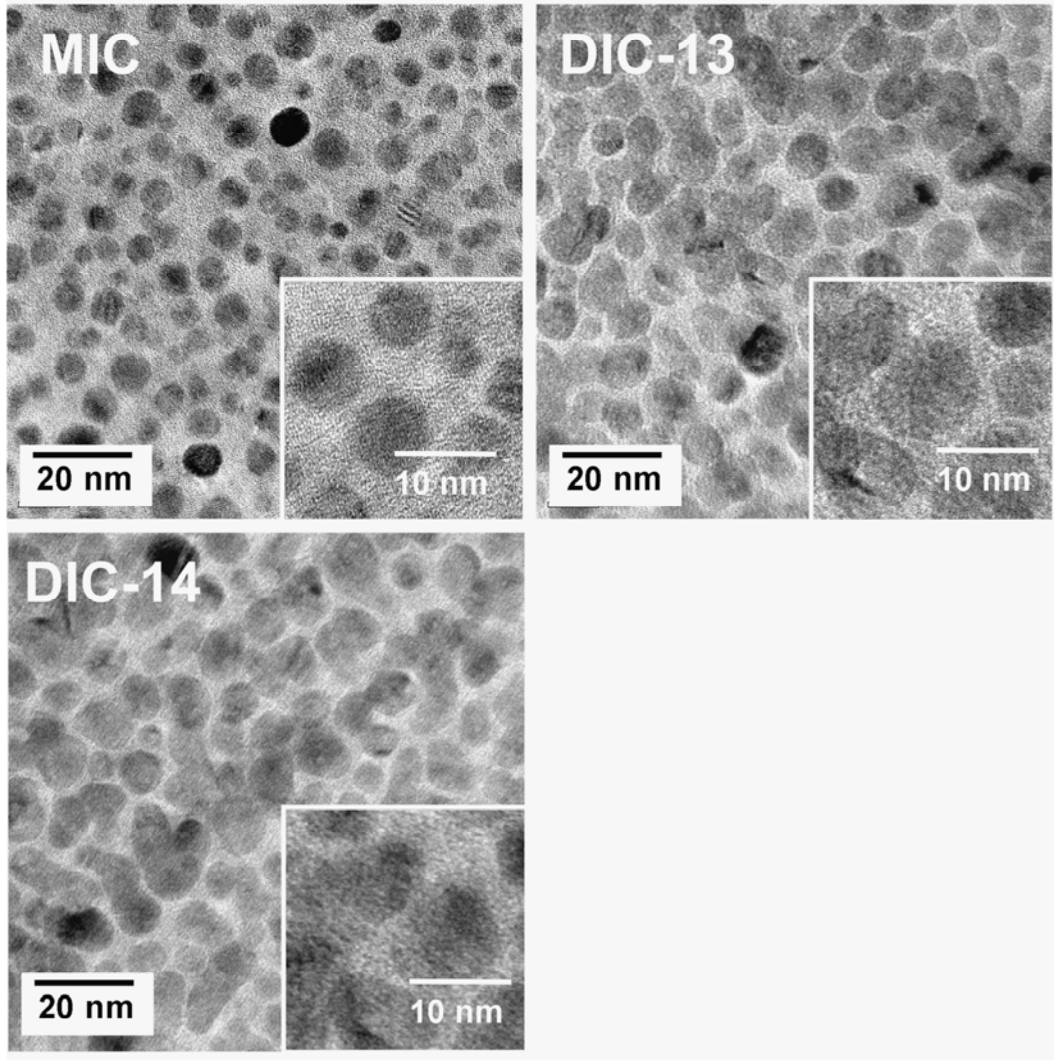

Fig. 4-2 The plane-view images of transmission electronic microscopy (TEM) of MIC and DIC poly-Si films

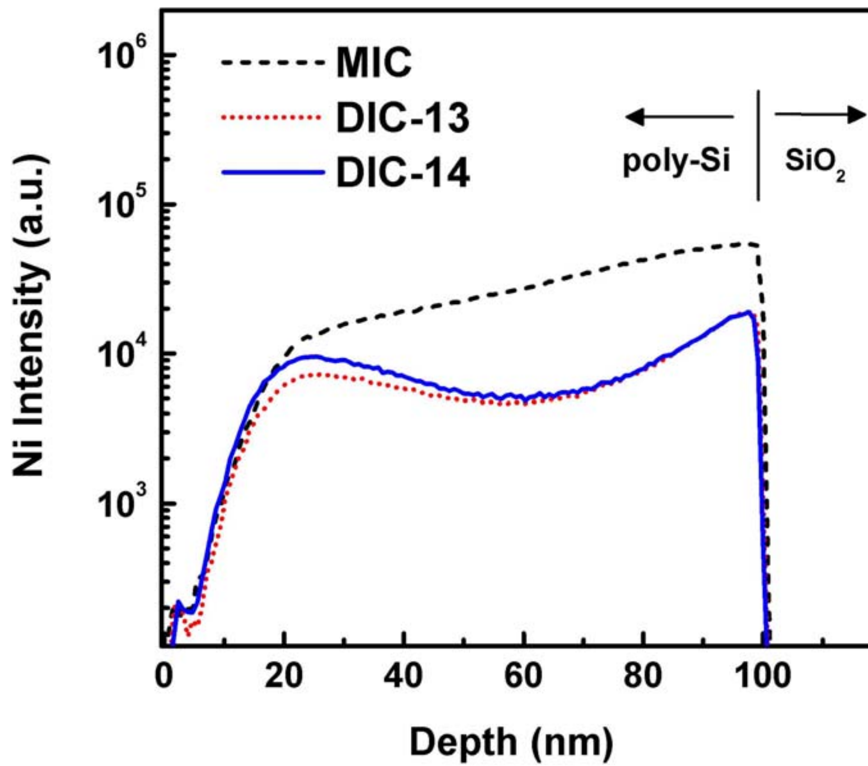

Fig. 4-3 Secondary-ion mass spectrometry (SIMS) depth profiles of Ni in the structure of MIC and DIC poly-Si films

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4.2.2.2 Electrical performance of MIC and DIC TFTs

Figure 4-4 displays the I_D–V_G transfer characteristics of TFTs. The measured and extracted key device parameters are summarized in Table 4-1. The device parameters were extracted at W/L = 10/10 μm, and ten TFTs were measured in each case to investigate the device-to-device variation. The average values with standard deviations in parentheses were shown in Table 4-1. The threshold voltage (V_{th}) is defined at a normalized drain current of I_{DS}

= (W/L) × 100nA at V_{DS} = 5V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at V_{DS} = 0.1V. It was found that the electrical characteristics (especially leakage current and on/off current ratio) of TFTs were improved by DIC processes. Compared with MIC TFTs, DIC TFTs shows a 2.98-fold decrease in the minimum leakage current and a 2.89-fold increase in the on/off current ratio. It was great improved in off-state which is the most importance of MIC TFTs.

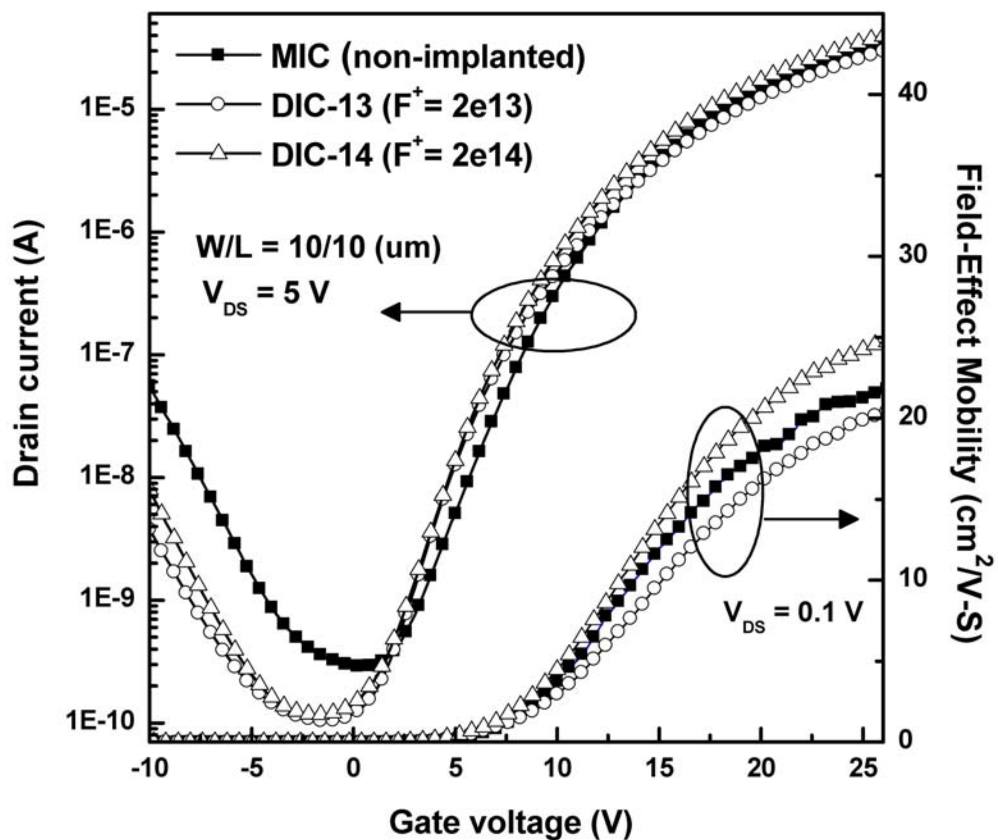


Fig. 4-4 Typical I_{DS}-V_{GS} transfer characteristics and filed-effect mobility of DIC TFTs and MIC TFT (W / L = 10 / 10 μm)

Table 4-1 Average device characteristics of DIC TFTs and MIC TFTs with standard deviations in parentheses

Device Parameters W / L = 10 μm / 10 μm	MIC	DIC-13	DIC-14
Field-Effect Mobility μ_{FE} (cm^2 / V-s)	**23.0 (1.38)**	**22.2 (1.12)**	**25.6 (0.82)**
Threshold Voltage V_{th} (V)	**8.09 (1.23)**	**7.46 (0.33)**	**7.07 (0.24)**
Subthreshold Slope S.S (V / dec)	**2.00 (0.09)**	**1.83 (0.05)**	**1.75 (0.11)**
Imin (pA/ μm)	**3.31 (0.54)**	**1.11 (0.05)**	**1.23 (0.07)**
Max on/off ratio ($\times 10^5$)	**1.57 (0.47)**	**3.72 (0.41)**	**4.54 (0.38)**
Interface trap density N_{it} (10^{12} cm^{-2})	**7.03 (0.32)**	**6.42 (0.19)**	**6.10 (0.39)**

4.2.2.3 Ni concentration effect on leakage current

The leakage current improvement was attributed to the reduction of Ni concentration in the poly-Si films. This is because, in the poly-Si film, Ni residues serve as deep level traps, which promote thermionic emission-dominated leakage current in the low-gate and drain voltage region [62]-[64]. Ni content in DIC was much lower than that in MIC as shown in Fig. 4-3. The DIC process did reduce Ni content in poly-Si films. With the reduction of the Ni concentration in DIC, the minimum leakage current was reduced and therefore the on/off current ratio was increased.

4.2.2.4 Effects of fluorine ion implantation

Besides, as shown in Fig. 4-5, F content in DIC-14 was much higher than that in DIC-13. High F content is present at the DIC/oxide interface, meaning F atoms have diffused to the interface to terminate defects. The effective interface trap states densities (N_{it}) near the SiO_2/poly-Si interface can be calculated as follows:

$$N_{it} = [(S.S./\ln 10)(q/kT)-1]\ (C_{ox}/q)$$

where C_{ox} is the capacitance of the gate insulator [95]. As shown in Table 4-1, the value of N_{it} was decreased with increase in dosage of F^+. Therefore, DIC TFTs presents good S.S. and V_{th} in the performance.

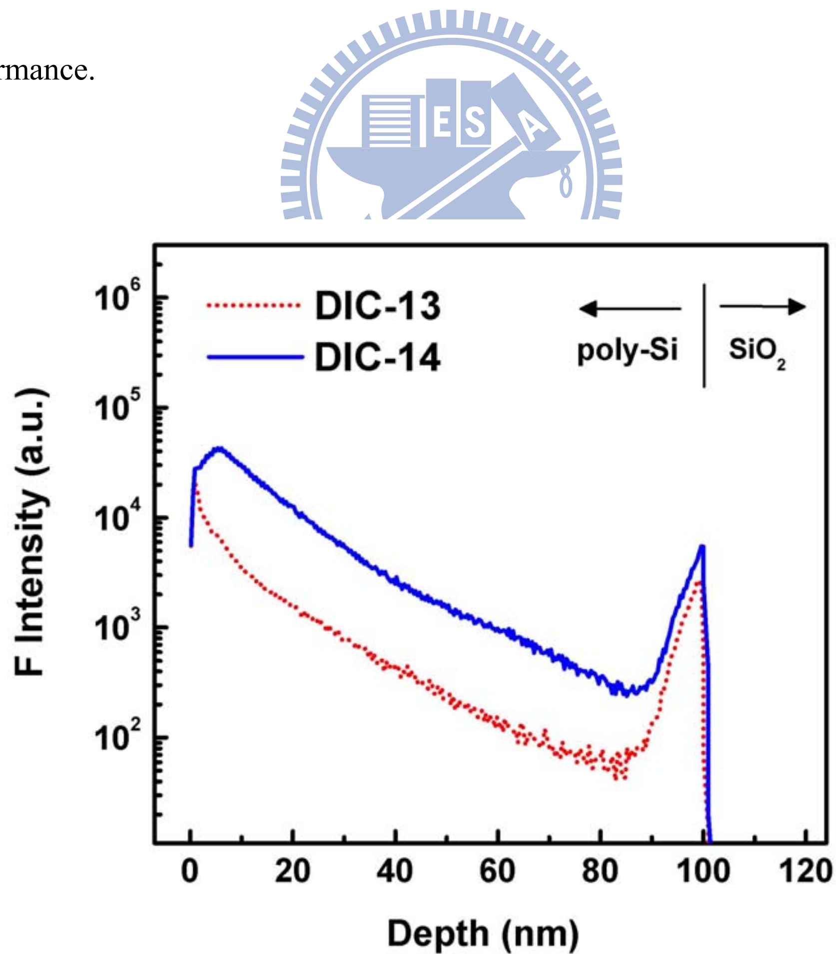


Fig. 4-5 SIMS depth profiles of Ni in the structure of MIC and DIC poly-Si films

Figure 4-6 shows schematic of F atoms eliminating dangling bonds and strain bonds. Since F atoms can passivate dangling bonds and strain bonds [78], the on-state currents of DIC TFTs were expected to be higher than those of MIC TFTs. However, Fig. 4-4 shows that the on-state current of DIC TFTs is similar to that of MIC TFTs. In this case, F passivation presented less improvement on the on-state current of DIC TFTs might due to the channel damage caused by ion implantation [76].

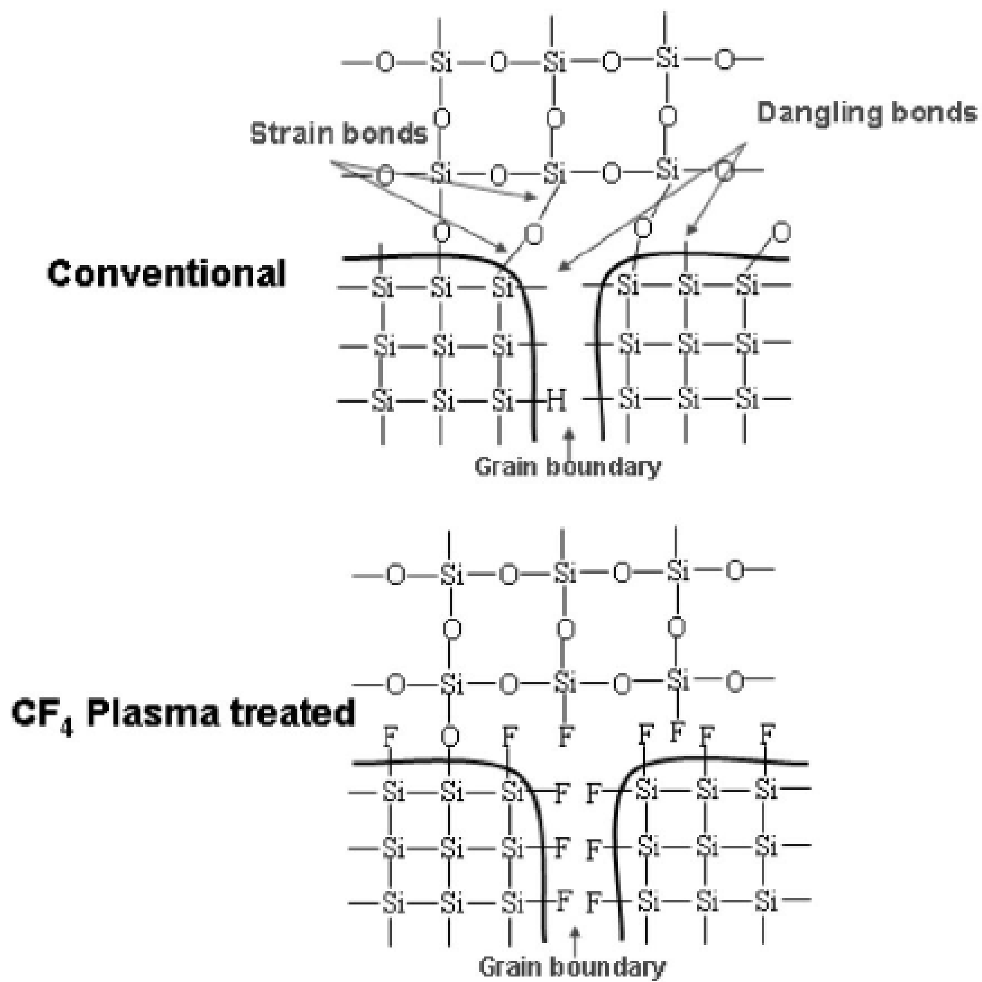
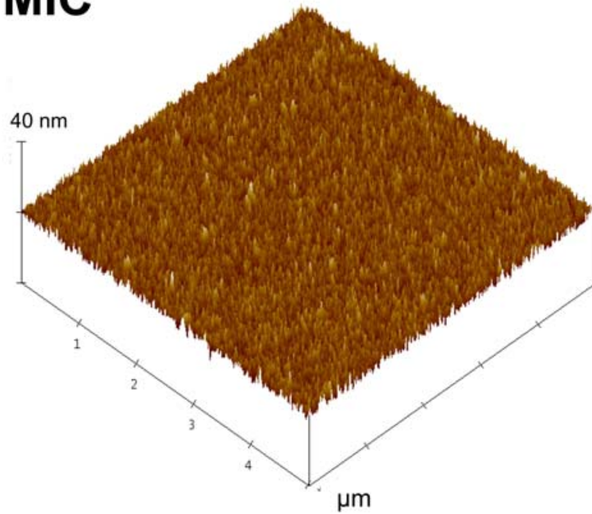
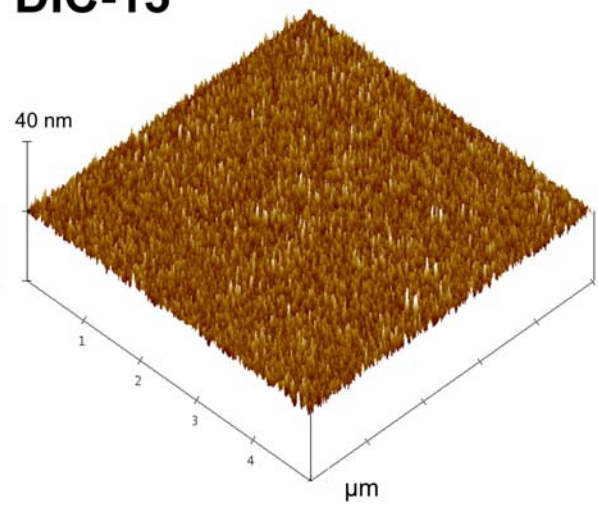


Fig. 4-6 Schematic of F atoms eliminating dangling bonds and strain bonds [78].

4.2.2.5 Surface roughness of MIC and DIC poly-Si films

The roughness of the poly-Si surfaces was measured by atomic force microscopy (AFM) after the remained Ni was removed. The roughness can reflect the degree of damage since the grain size of MIC, DIC-13 and DIC-14 are almost. At the same Si layer, AFM can demonstrate degree of collision at surface by implantation. Therefore, it can verify increasing defect indirectly. As shown in Fig. 4-7, the root mean square (rms) roughnesses of MIC, DIC-13 and DIC-14 films were 1.235 nm, 1.462 nm and 1.693 nm, respectively. The damage (rms roughness) did increase with the dosage of F^+.





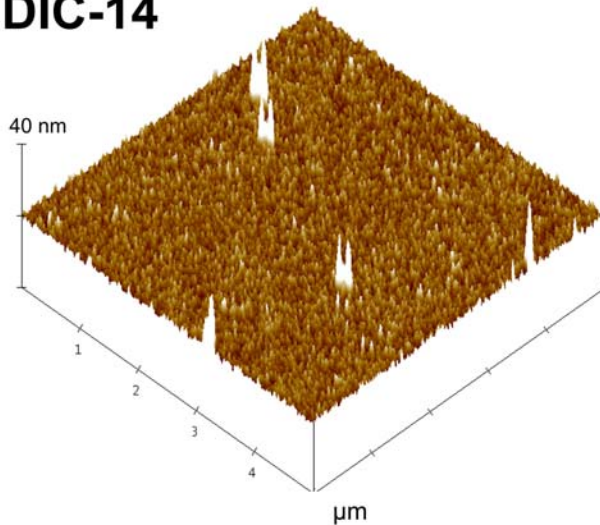
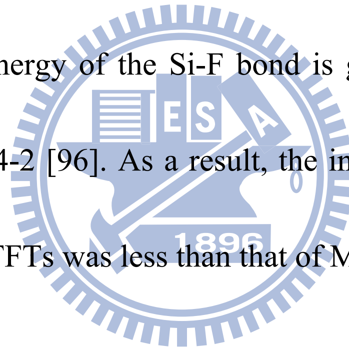


Fig. 4-7 Surface roughness of MIC and DIC poly-Si films

4.2.2.6 Thermal stability of MIC TFTs and DIC TFTs

The other important issue of poly-Si TFTs is the thermal stability, which was examined at elevated temperatures. Figure 4-8 presents the I-V curves of the MIC and CF-MIC, which were performed at temperature from 25 to 125°C. As can be seen, the off-state curves were

raised with increase of operation temperature. The threshold voltage shift and off-state current as a function of temperature were summary in Fig. 4-9. As shown in Fig. 4-9, the threshold voltage and the off-state current of TFTs were degraded with increase in annealing temperature from 25 to 125°C. This is because when temperature increased, nickel related donor-like defects were easy to release electrons, thus increasing the leakage current and the negative shift of V_{th} [87]. Compared with those of MIC TFTs, the thermal stability of DIC TFTs was improved by DIC processes, which is due to the reduction of Ni concentration in TFTs as shown in Fig. 3(a). The other factor that might affect the thermal stabilities is the bonding energy. The bonding energy of the Si-F bond is greater than that of the Si-Si and Si-H bonds, as shown in Table 4-2 [96]. As a result, the increase of the leakage current and the negative shift of V_{th} of DIC TFTs was less than that of MIC TFTs.



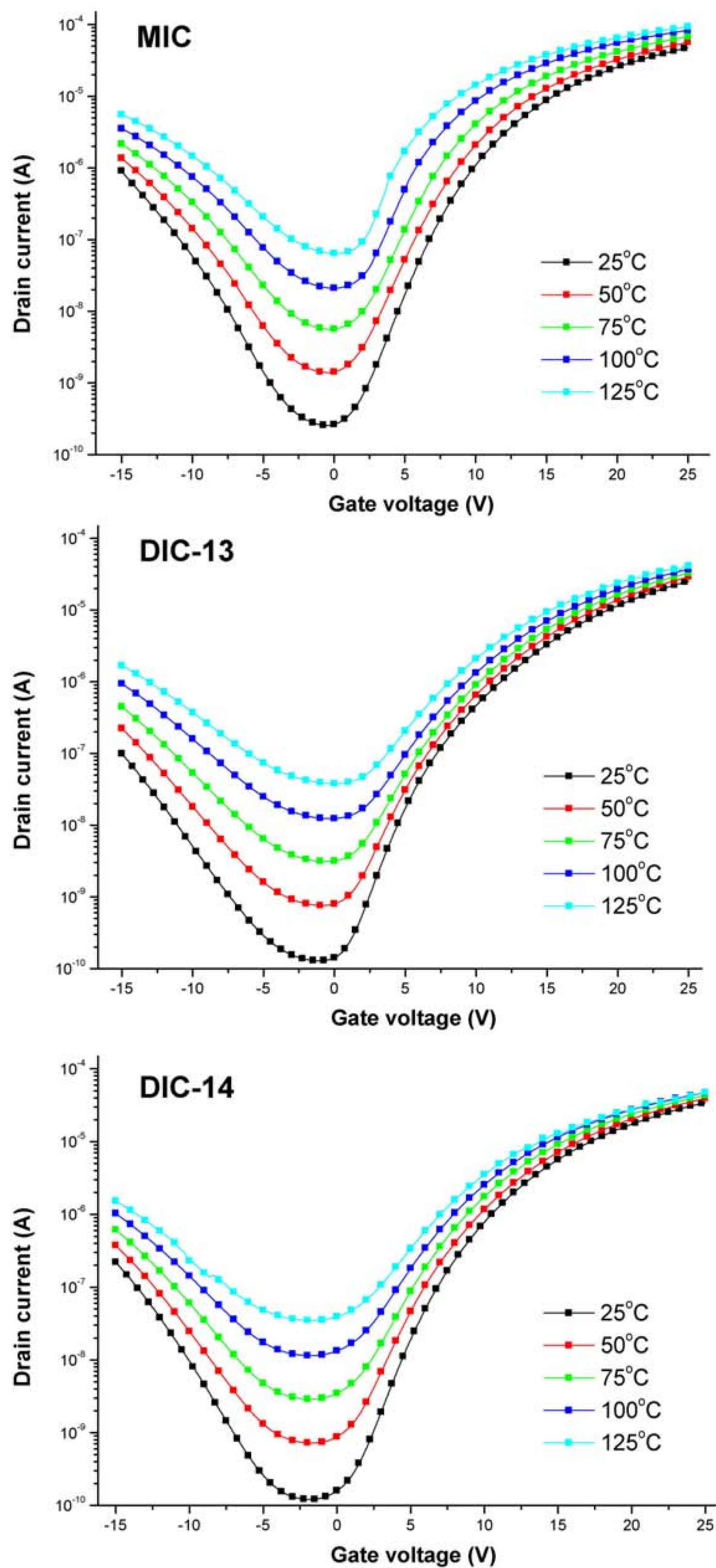


Fig. 4-8 I-V curves of the MIC and CF-MIC at temperature from 25 to 125°C.

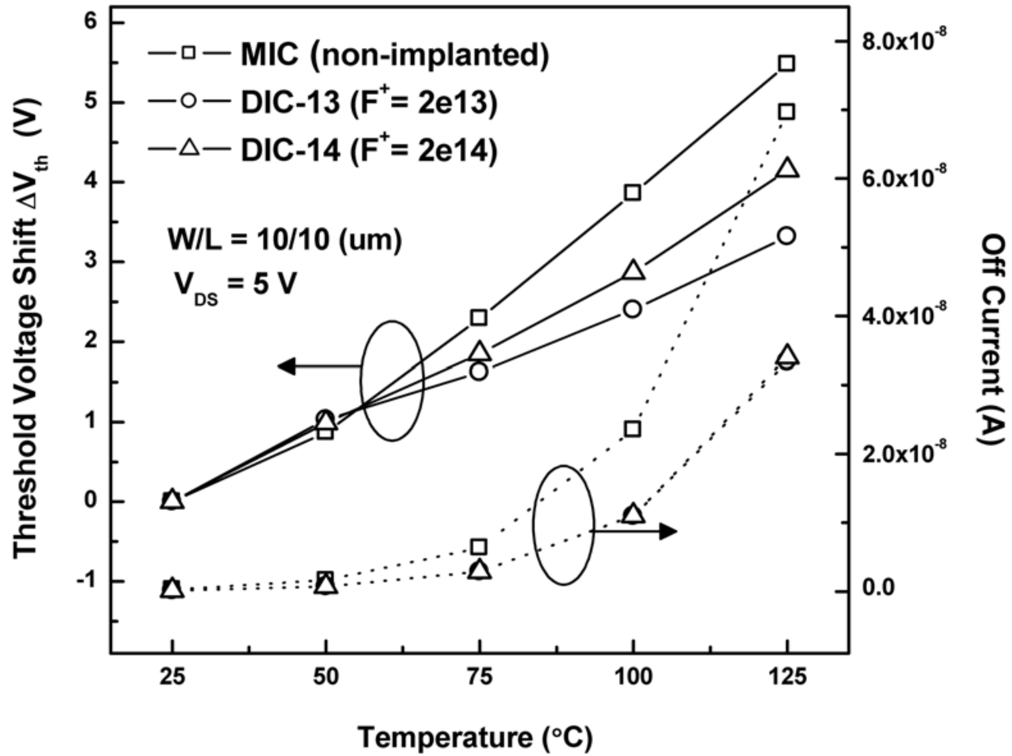


Fig. 4-9 The degradations of threshold voltage and off-state current versus temperature at V_{DS} = 5 V.

Table 4-2 The bonding energy of the Si-Si, Si-H and Si-F bonds [96].

	Si-Si	Si-H	Si-F
bonding energy	310 kJ/mole	293 ±1.9 kJ/mole	576.4 ±17 kJ/mole

4.2.3 Notability for driven-in Ni induced crystallization (DIC)

In DIC, F^+ implantation was used to drive Ni in the α-Si layer. Compared with MIC process, DIC process can effectively reduce the Ni concentration, thus reducing the Ni-related defects. As a result, DIC-14 TFTs exhibit higher field-effect mobility, lower subthreshold slope, lower threshold voltage, higher on/off current ratio, and lower interface trap-state density (N_{it}) compared with conventional MIC TFTs. It was also found that DIC process can greatly alleviate the degradations of threshold voltage and off-state current at elevated temperatures. This is attributed to the reduction of Ni concentration in TFTs, and the weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds.

However, on-state current of DIC TFTs were almost the same with MIC TFTs. This might because F passivation effect was not good enough to compensate the degradation from channel damage caused by ion implantation.

4.3 Part 2: Investigation driven-in Ni induced crystallization with a cap oxide (DICC)

4.3.1 Experimental procedure

Three kinds of poly-Si TFTs were investigated in this study: MIC TFTs, fabricated by the traditional Ni-MIC method; DIC TFTs, in which F^+ ions were implanted to drive Ni into the α-Si layer; and DICC TFTs, in which a chemical oxide layer was introduced into DIC

TFTs before F^+ implantation. To fabricate DICC TFTs, samples were dipped into a mixed solution of H_2SO_4 and H_2O_2 for 20 min to form a chemical oxide (chem-SiO_2) layer on top of the α-Si layer. A 5-nm-thick Ni film was then deposited. Samples were subjected to F^+ implantation to drive Ni into the α-Si layer, as shown in Fig. 4-11 (a).

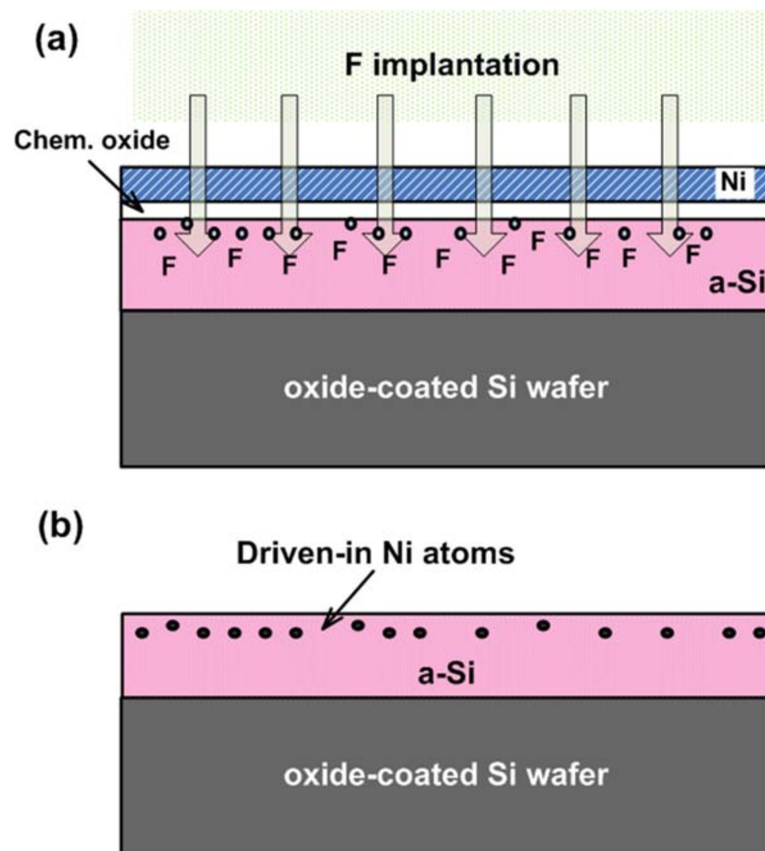


Fig. 4-10 Schematic illustration of DICC TFTs process: (a) F^+ implantation process to drive Ni in the α-Si layer, and (b) removing of remained Ni film and chemical oxide.

Figure 4-11 shows the simulation data of implantation for the DIC TFTs and DICC TFTs by using simulation software (SRIM). The projection range was set at a depth of 15 nm near the surface of the α-Si layer. To increase passivation effect, the dosage of fluorine ion was set at 2×10^{15} cm^{-2}. After ion implantation, the remaining Ni film and chemical oxide layer were then removed by wet etching Fig. 4-10 (b). The α-Si was subsequently annealed at 500°C for 1 h in N_2 to achieve crystallization. Notably, the deduced crystallization process parameters of all poly-Si films are summarized in Table 4-3.

Finally, devices were fabricated by standard IC processes as the same with chapter 2.

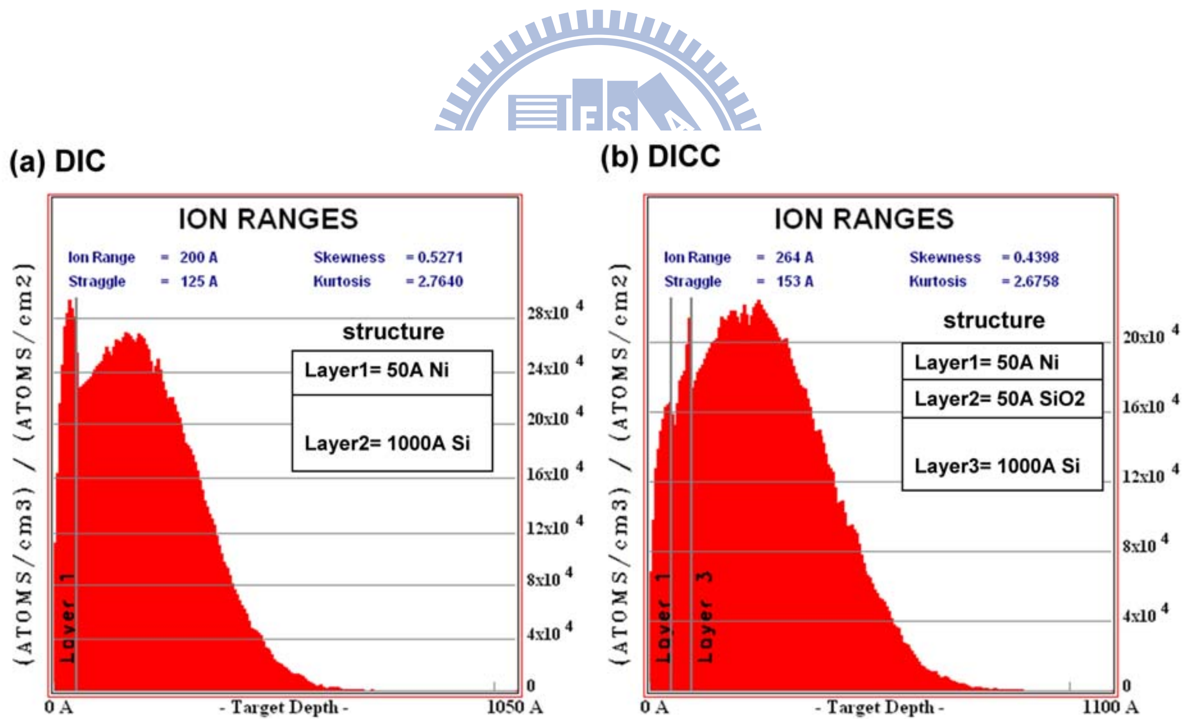


Fig. 4-11 Simulation data of DIC TFTs and DICC TFTs at 10 and 13 KeV, respectively.

Table 4-3 The deduced crystallization process parameters of all poly-Si films.

	Chem. oxide	Implant energy	Implant dosage
MIC	0	0	0
DIC	0	10 keV	5×10^{15}
DICC	3.5 nm	13 keV	5×10^{15}

4.3.2 Results and discussion

4.3.2.1 Transfer characteristics of DIC TFTs, DICC TFTs and MIC TFTs

Figure 4-12 exhibits the I_D–V_G transfer characteristics of TFTs at drain bias of 5 V for W/L = 10 μm /10 μm devices. The measured and extracted key device parameters are summarized in Table 4-4. Ten TFTs were measured in each case to investigate device-to-device variation; average values with standard deviations in parentheses are shown in Table 4-4. As expected, the minimum leakage current of DIC TFTs was much lower than that of conventional MIC TFTs. Unfortunately, the on-state current of DIC TFTs was lower than that of MIC TFTs. This degradation might be due to channel damage caused by ion implantation.

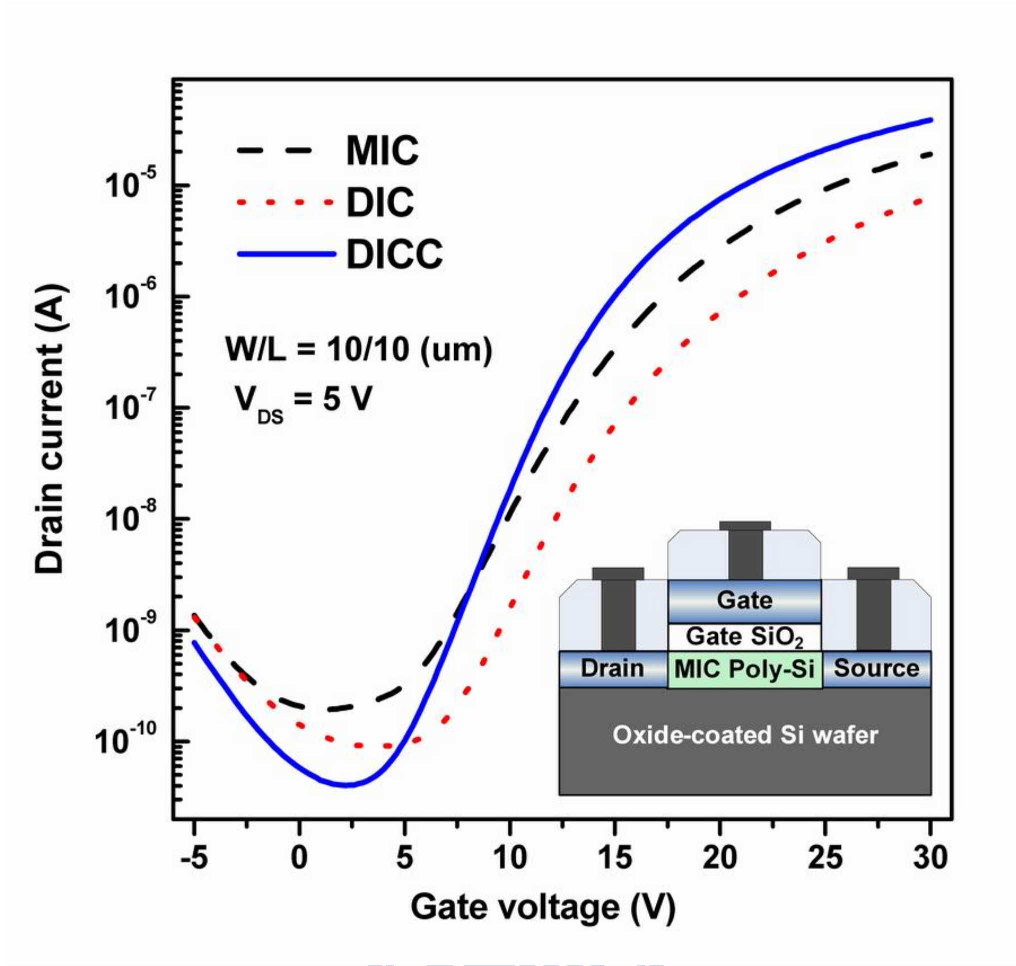


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Fig. 4-12 Typical I_{DS}-V_{GS} transfer characteristics of DIC TFTs, DICC TFTs and MIC TFTs.

Table 4-4 Average device characteristics of DIC TFTs, DICC TFTs and MIC TFTs with standard deviations in parentheses

W / L = 10 / 10 μm	MIC	DIC	DICC
μ_{FE} (cm^2 / V-s)	**15.60 (1.13)**	**10.85 (1.86)**	**26.70 (1.31)**
V_{th} (V)	**12.85 (0.71)**	**14.99 (1.03)**	**11.99 (0.18)**
S.S (V / dec)	**2.77 (0.12)**	**2.52 (0.14)**	**2.06 (0.03)**
Imin (pA/ μm)	**19.20 (1.02)**	**9.08 (3.79)**	**4.06 (0.22)**
Max on/off ratio ($\times 10^5$)	**0.92 (0.07)**	**1.25 (0.71)**	**8.94 (0.76)**

4.3.2.2 Optimization of device performance by DICC process

In order to improve this on-state current degradation, the DICC process (chemical oxide layer) was applied to the fabrication of DIC TFTs. As shown in Fig. 4-12, the on-state currents of TFTs were much improved by this DICC process. Compared with that of MIC TFTs, the on/off current ratio (I_{on}/I_{off}) of DIC TFTs was increased by a factor of 9.7 from 9.21 $\times 10^4$ to 8.94 $\times 10^5$. The leakage current (I_{off}) of DICC TFTs was 4.06 pA/μm, which was much less than that of DIC TFTs (9.08 pA/μm) and MIC TFTs (19.20 pA/μm). This improvement is attributed to the reduction of Ni concentration [62]-[64], which was verified by SIMS measurement. As shown in Fig. 4-13 (a), the Ni content in DICC was lower than that in DIC and MIC. Obviously, the Ni concentration in the channel layer was reduced by the introduction of the chemical oxide layer.

In addition, the improvement of the on-state current of DICC TFTs implies that the chemical oxide layer has ameliorated the channel damage caused by ion implantation. Moreover, as shown in Fig. 4-13 (b), high F content is present at the poly-Si/oxide interface, meaning that F atoms have diffused to the interface to terminate Ni-related defects [93]. The on-state current of DICC TFTs was expected to be higher than that of MIC TFTs since F atoms can passivate dangling and strain bonds (trap states) [76], [78], [93].

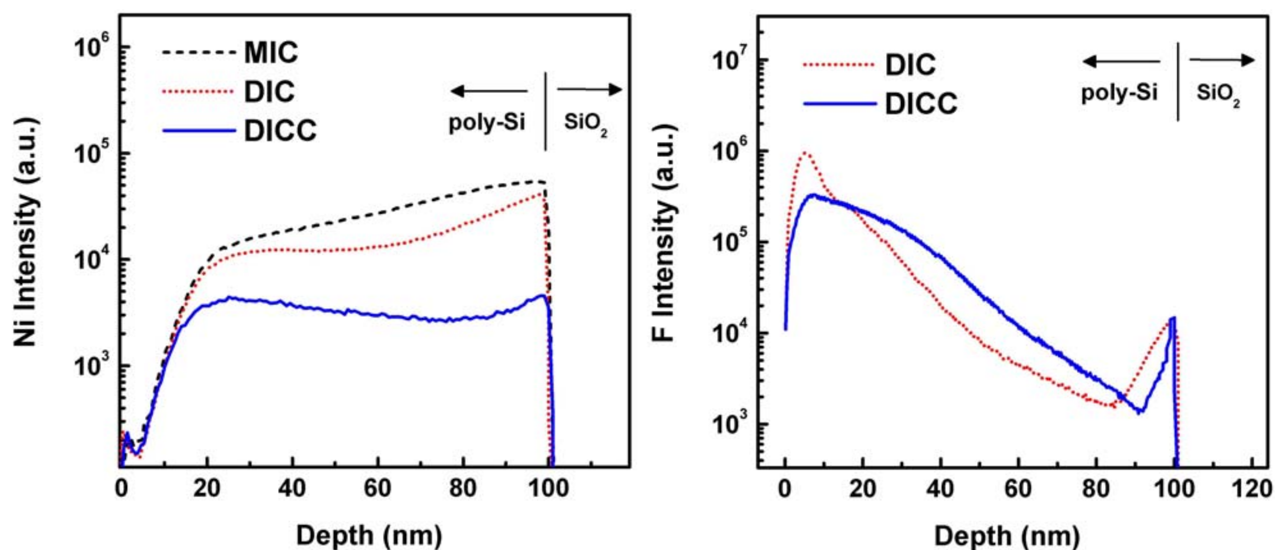
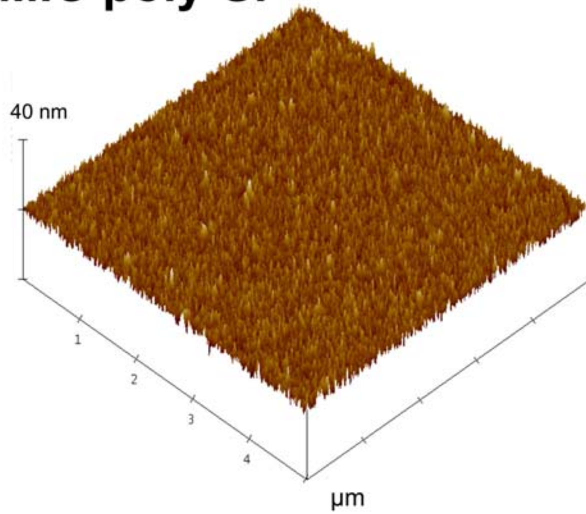
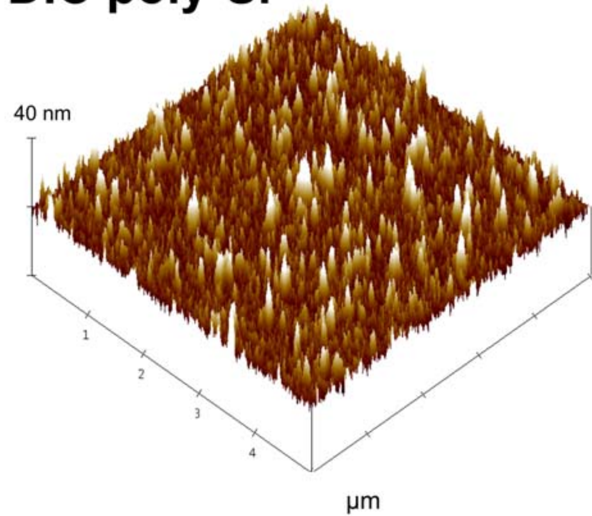


Fig. 4-13 SIMS depth profiles of (a) nickel and (b) fluorine in the structure of poly-Si films.

4.3.2.3 Effects of F^+ implantation on damage and passivation

To verify the interaction between implant damage and passivation of F^+ implantation on the channel layer, the surface roughness and effective trap state density (N_t) were measured. The damage of poly-Si surfaces (after the residual Ni and chemical oxide layer were removed) was assessed using atomic force microscopy (AFM). As shown in Fig. 4-14, the root mean square (rms) roughness of MIC, DIC and DICC films were 1.348 nm, 1.754 nm and 0.866 nm, respectively. DIC poly-Si has the roughest surface due to ion bombardment [77]. On the other hand, DICC poly-Si has the smoothest surface. The chemical oxide layer did improve surface roughness due to reduced implantation damage.





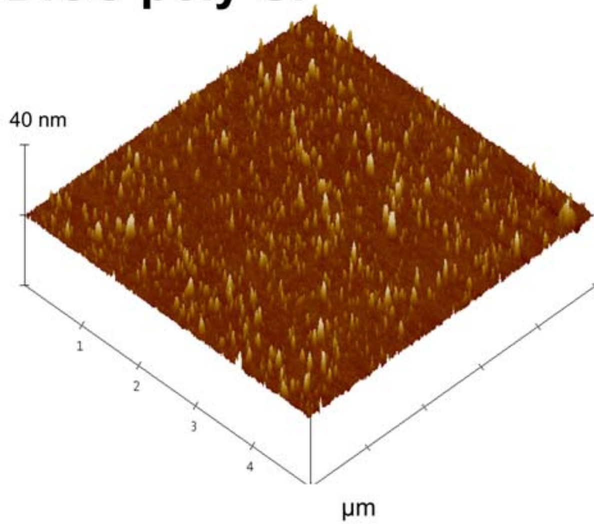


Fig. 4-14 Atomic force microscopy (AFM) images and the root mean square (rms) roughnesses of poly-Si after remained Ni and chemical oxide were removed.

The effective trap state density (N_t) was measured using Levinson and Proano's method, where N_t is estimated from the slope of the linear segment of ln $[I_{DS} / (V_{GS}\text{-}V_{FB})]$ vs. $1 / (V_{GS}\text{-}V_{FB})^2$ at low V_{DS} and high V_{GS}, where V_{FB} is defined as the gate voltage that yields the

minimum drain current at V_{DS} = 0.1 V [82]-[83]. As shown in Fig. 4-15, the N_t of DICC TFTs was 4.98×10^{12} cm^{-2}, which was much less than that of MIC TFTs (5.85×10^{12} cm^{-2}) and DIC TFTs (6.69×10^{12} cm^{-2}).

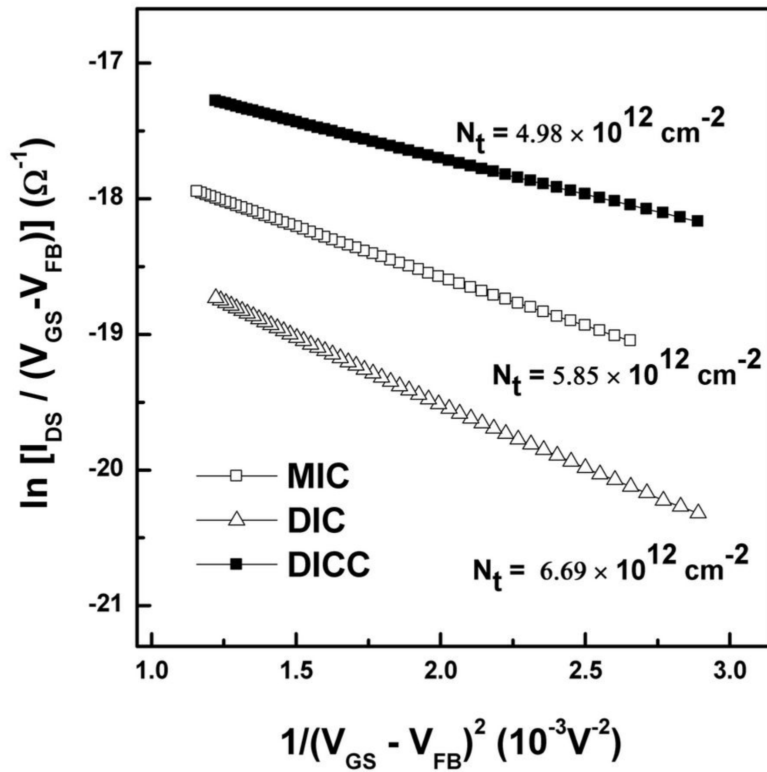


Fig. 4-15 The ln [I_{DS} / ($V_{GS}-V_{FB}$)] vs. 1 / $(V_{GS}-V_{FB})^2$ at low V_{DS} and high V_{GS} of TFTs.

4.3.2.4 Discussion about effect of defects on electrical performance

In other words, there were three major defects related to the performance of MIC TFTs: (1) Ni concentration (Ni-related defects), (2) grain boundaries and (3) channel damages. In DIC and DICC, F^+ implantation was employed to drive Ni into the α-Si layer. Compared with

MIC, DIC and DICC can reduce the Ni concentration, thus overcoming the Ni-related defects. Moreover, F atoms can passivate dangling bonds and strain bonds, thus improving the negative effects of grain boundaries. However, the on-state current of DIC TFTs was lower than that of MIC TFTs due to channel damage caused by ion implantation. In DICC, the chemical oxide layer was introduced between the Ni and α-Si layer to reduce channel damage. As a result, DICC TFTs has the highest on-state current.

4.3.2.5 Hot carrier effect on MIC TFTs and DICC TFTs

The other important issue of poly-Si TFTs is their reliability, which was examined under hot-carrier stress. In general, the stress voltage was set at the on-state saturation region. Early studies have demonstrated that the device degradation increased with stress voltage from 20 V to 30 V. In this case, the stress voltage was set at 25 V (V_{DS} = V_{GS} = 25 V for 2500 s) [76]-[78]. Figure 4-16 presents the I-V curves of the TFTs after various stress time. The threshold voltage (V_{th}) is defined at a normalized drain current of I_{DS} = (W/L) × 100nA at V_{DS} = 5V, and the on-state current is defined at drain current at V_{GS} = 25V. As shown in Figs. 4-17 and 4-18, the on-state current and the threshold voltage of TFTs were both degraded because dangling bonds were created due to the trapping of electrons at weak Si-Si and Si-H bonds [84], [97]. Compared with that of conventional MIC TFTs, the on-state current degradation of DICC TFTs is greatly improved by F^+ implantation. DICC TFTs also possess

high immunity against the hot-carrier stress and thereby exhibit lower ΔV_{TH} and $\Delta I_{ON}/I_{ON}$, compared with conventional MIC TFTs. This is because weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds [98], which could not be broken under hot-carrier stress, thus leading to improved electrical reliability.

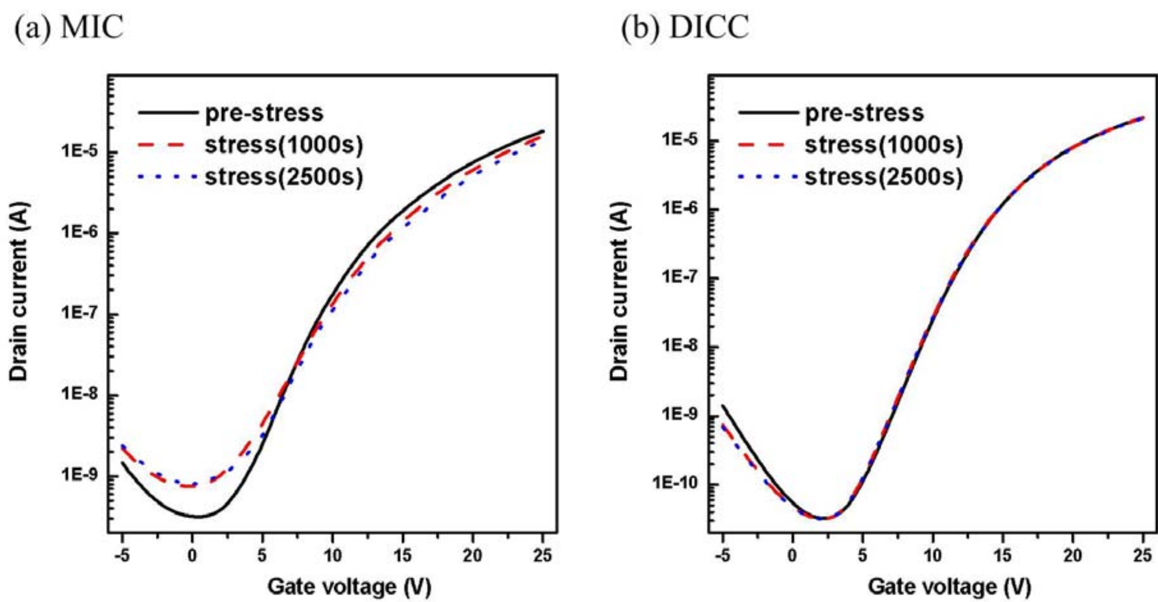


Fig. 4-16 The I-V curves of DICC TFTs and MIC TFTs after the stress.

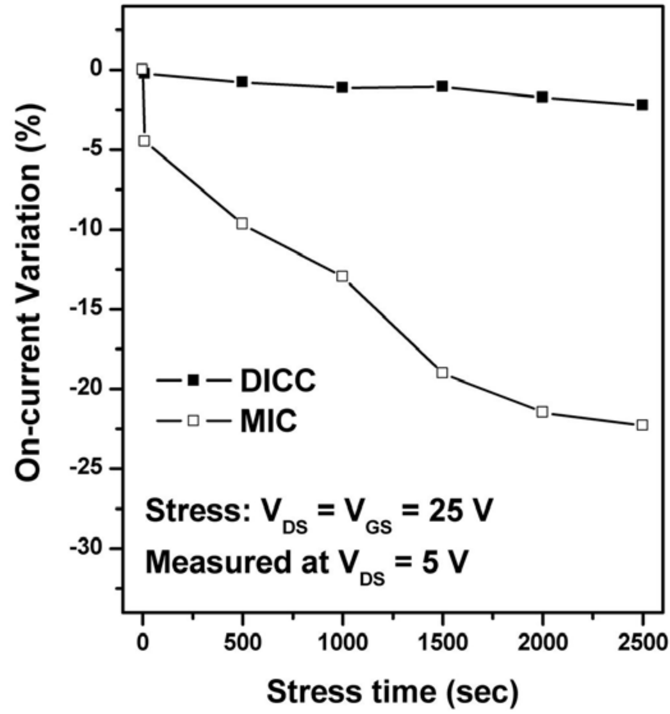
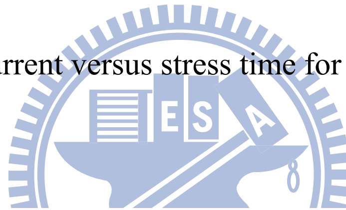


Fig. 4-17 Variation of on-state current versus stress time for the DICC TFTs and MIC TFTs.



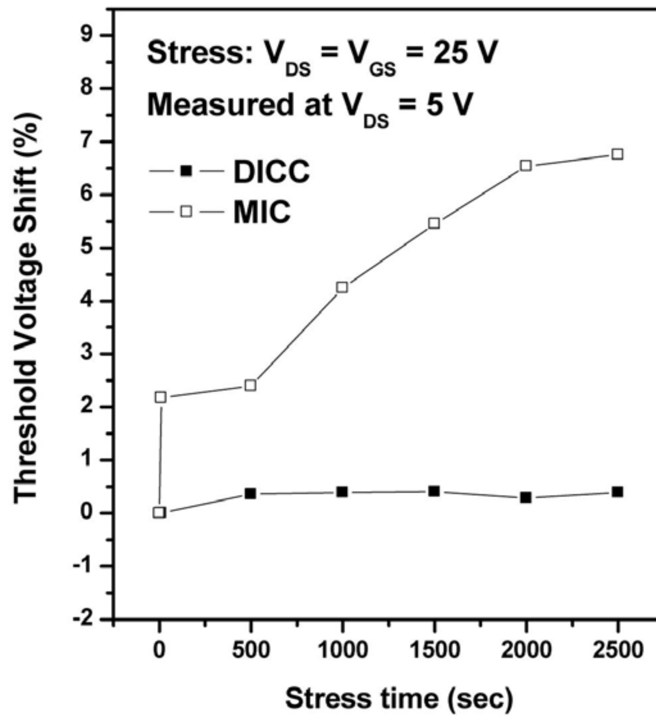


Fig. 4-18 Variation of threshold voltage shift versus stress time for the DICC and MIC TFTs.

4.3.3 Notability for driven-in Ni induced crystallization with a chemical oxide (DICC)

In DICC, a chemical oxide layer was introduced into DIC process to further improve the electrical performance and bias reliability. As a result, DICC TFTs had the highest on/off current ratio (9.21×10^4), which was much lower than that of MIC TFTs (8.94×10^5), since the chemical oxide can reduce content of Ni atoms into α-Si layer and retard ion implant damage. It was also found that DICC can greatly alleviate the threshold voltage and on-state current degradation under hot-carrier stress. DICC TFTs possess high immunity against the hot-carrier stress and thereby exhibit lower ΔV_{TH} and $\Delta I_{ON}/I_{ON}$ compared with conventional MIC TFTs. This is because weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds, which could not be broken under hot-carrier stress, thus leading to improved electrical reliability

4.4 Summary

MIC method has been used to reduce the crystallization time and temperature of α-Si owning to annealing time is short and the uniformity is good. However, Ni-related defects and grain boundaries would degrade the TFT performance. In this study, an investigation of poly-Si TFTs using DIC process had led to the development of a simple process for LTPS TFTs manufacturing.

The DIC method by use of F^+ implantation was supposed to reduce Ni concentration, and passivate dangling bonds. As expected, DIC process can effectively reduce the Ni concentration, thus reducing the leakage current. Unfortunately, the on-state current of DIC TFTs were nearly unchanged due to the channel damages caused by ion implantation. In DICC, we introduced a chemical oxide layer between the Ni and α-Si layer to further improve the electrical performance and bias reliability. As the results, DICC TFTs did not only present the much lower leakage current than DIC TFTs but also significantly improve in on-state current. This is because the chemical oxide layer can reduce content of Ni atoms into α-Si layer and retard F^+ implant damage. Furthermore, it was also found that DICC can greatly alleviate the threshold voltage and on-state current degradation under hot-carrier stress. DICC TFTs possess high immunity against the hot-carrier stress and thereby exhibit lower ΔV_{TH} and $\Delta I_{ON}/I_{ON}$ because weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds, which could not be broken under hot-carrier stress, thus leading to improved electrical reliability.

Chapter 5

Conclusions and future work

5.1 Conclusions

In this thesis, a number of methods have been carried out for fabrication of high-performance low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs), including Ni-metal-induced crystallization (MIC) of amorphous Si (α-Si) through a simply chemical oxide and driven-in Ni induced crystallization by using F ion implantation. Moreover, this thesis also entirely investigated how the Ni concentration affects the source/drain series resistance, bias reliability and thermal stability.

In chapter 2, the chemical oxide filter layer was introduced into MIC processes to reduce the leakage current of MIC TFT. The process was very simple and without extra expensive instrument. The chemical oxide growth controlled by diffusion of reactants through the pre-existing layer conformed to the model of oxide growth and there is a saturation thickness of 3.4 nm after dipped for 10 min. It was also found that it conformed to the basic diffusion model to presented exponential decay as a function of immersed time and saturated at a minimum of Ni concentration after dipped for 10 min. As the results, the electrical performance of MIC TFTs with chemical oxide layer was significantly improved, including in higher field-effect mobility, superior subthreshold slope, and higher on/off current ratio.

Compared with conventional MIC TFTs, CF-MIC TFTs shows a 14.3-fold decrease in the minimum leakage current and a 17.3-fold increase in the on/off current ratio. This is because the chemical oxide layer can avoid Ni directly contact with α-Si, avoid excess of Ni atoms into α-Si layer and remove unreacted Ni easily from surface.

In chapter 3, we have provided further insight into how Ni concentration and resistance of MIC TFTs are related. Consequently, the channel resistance and S/D series resistance were decreased with the reduction of Ni concentration in MIC poly-Si due to better crystalline quality and lower degradation of donor concentration. This phenomenon is owing to that low Ni concentration formed less nucleation site of $NiSi_2$ to cause large grain size; Ni atoms serve as acceptor-like dopants in silicon, which counteract the effects of n-type doping, subsequently reducing the donor concentration in the S/D region. Moreover, the Ni concentration effect on bias reliability and thermal stability were investigated under hot carrier stress and elevated temperature, respectively. We have proved that reducing Ni concentration in MIC films was also beneficial for bias reliability and thermal stability. As the results, the low Ni residues device (CF-MIC) presented high immunity against the hot-carrier stress because larger grain size and fewer weak Si-H bonds. Furthermore, it was also found that reducing Ni concentration can alleviate the degradations of threshold voltage and off-state current at elevated temperatures because nickel related donor-like defects were easy to release electrons with increase of operation temperature.

In chapter 4, electrical characteristics of MIC poly-Si TFTs using driven-in Ni induced crystallization (DIC) was investigated. In DIC, F^+ implantation was used to drive Ni in the α-Si layer. Compared with MIC process, DIC process can effectively reduce the Ni concentration, thus reducing the Ni-related defects. As a result, DIC-14 TFTs exhibit higher on/off current ratio and lower interface trap-state density (N_{it}) compared with conventional MIC TFTs. It was also found that DIC process can greatly alleviate the degradations of threshold voltage and off-state current at elevated temperatures. This is attributed to the reduction of Ni concentration in TFTs, and the weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds. However, the on-state current of DIC TFTs were nearly unchanged due to the channel damages caused by ion implantation. Therefore, a chemical oxide layer was introduced into DIC process (DICC) to further improve the electrical performance and bias reliability. As a result, DICC TFTs had the highest on/off current ratio (9.21×10^4), which was much lower than that of MIC TFTs (8.94×10^5), since the chemical oxide can reduce content of Ni atoms into α-Si layer and retard ion implant damage. It was also found that DICC can greatly alleviate the threshold voltage and on-state current degradation under hot-carrier stress. DICC TFTs possess high immunity against the hot-carrier stress and thereby exhibit lower ΔV_{TH} and $\Delta I_{ON}/I_{ON}$ compared with conventional MIC TFTs. This is because weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds, which could not be broken under hot-carrier stress, thus leading to improved electrical reliability.

5.2 Future works

According to the results in this thesis, there are some interesting topics that are valuable for the future research:

5.2.1 CF-MIC method combines with structure design

Leakage current is a key issue for circuit application of TFTs. Generally, it needs less than 1 pA/um at V_{DS} = 5V [99]. Unfortunately, the leakage current of MIC TFTs was usually poor. In this study, the other reason for the poor leakage current might be because of the limitation of our university facility. The gate insulator was deposited by PECVD system, which was also used to deposit other material including metal. Nevertheless, we did demonstrate “a simple chemical oxide layer” can reduce MIC leakage currents. This is one of the major purposes of this paper. As a result, the leakage current was significantly reduced from 30 to 2.1 pA/um. If CF-MIC process (chemical oxide) combined with other common structure (such as lightly-doped-drain (LDD) or thin channel structure [100], [101]), the leakage current might lower enough to fulfill the requirement for display application. It is necessary to point out that the high Ni concentration in MIC TFTs is the main factor for off-state current. The leakage current is hard to achieve requirement by only using structure design.

5.2.2 Fabrication of poly-Si thin film solar cell by using CF-MIC

Thin film crystalline Si solar cells have been prepared by MIC method, which performed MIC on three layer types in the solar cell structure including p-i-n, i-n and n layer [102]. However, the results showed that p-i-n prepared by MIC presented the lowest effective, opposite only n-layer prepared by MIC presented the most effective. The results indicate that the solar cell fabricated by MIC is unsuitable. In ideal, MIC poly-Si films have a potential to apply to solar cell because the orientation of needle-like MIC grain is benefit for free carrier transportation. Thus the degradation might due to high Ni contaminations trapped the generated electron-hole pairs. Our proposed CF-MIC method can effectively reduce Ni residues in MIC films and improve the electrical properties of MIC TFTs. Hence, the proposed method can be a candidate to solve this issue.

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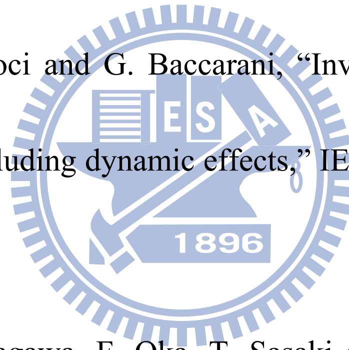

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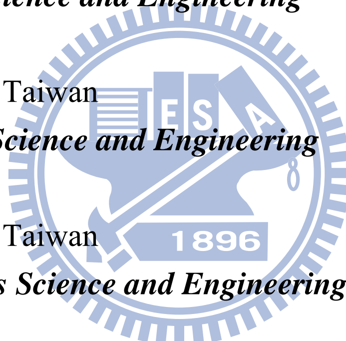

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Publication list

Journal Paper:

1. **Ming-Hui Lai**, YewChung Sermon Wu and Chih-Pang Chang, "Electrical performance and thermal stability of MIC Poly-Si TFTs improved using drive-in nickel induced crystallization," *Mater. Chem. Phys.* 126 (2011) 69-72.
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