國立交通大學

材料科學與工程研究所

博士論文

偏角度基板對穿隧層之效應與成長砷化鎵於鍺/矽基板上對低成本高效率多接面三五族太陽電池之應用

Substrate Misorientation Effects in Tunnel Junction Layers and GaAs Epitaxy Grown on Ge/Si Substrate for Low-cost High-efficiency III-V Multijunction Solar Cell Applications

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摘　　要

為了提升三五族太陽能電池在此領域之競爭力，首先必須要增加其光電轉換效率並降低其發電成本。在此論文中，我們證明偏角度基板對三五族多接面太陽能電池中砷化鋁鎵/砷化鎵穿隧層(AlGaAs/GaAs tunnel diodes, TDs)材料特性有一定影響。當砷化鋁鎵/砷化鎵穿隧層成長於 10 度砷化鎵基板上時，此時穿隧層表面粗糙度可降至 0.154nm 並產生最佳界面狀況。實驗結果也證實此基板可有效降低砷化鎵層中氧等不純物濃度；也可減少砷化鋁鎵層中非等向性位置(anisotropic sites)，進而減少此層在成長過程中不純物含量以提升三五族太陽能電池光電轉換效率。同時，我們也證實磷化銦鎵/砷化鎵(InGaP/GaAs)雙接面太陽電池中使用砷化鋁鎵/砷化鎵穿隧層(成長於 10 度砷化鎵基板上)可得到較高光電轉換效率(~20%)與外部量子效率(InGaP 子電池: 82% ; GaAs 子電池: 85%)。由高聚光測試(~185×)結果發現，使用砷化鋁鎵/砷化鎵穿隧層之磷化銦鎵/砷化鎵雙接面太陽電池之光電特性較使用磷化銦鎵/砷化鎵穿隧層之雙接面太陽電池來的高。此外，如果能將砷化鎵等三五族材料成長於矽基板上取代傳統以鍺為基板的模式，將可大大降低三五族太陽能電池發電成本。本研究發現將變溫砷界面層成長於經過 650 度熱退火之鍺/矽基板可有效改善隨後成長之砷化鎵層磊晶品質(表面粗糙度:1.1nm；缺陷密度: ~2x$10^{7}$$cm^{-2}$)。本研究亦證實由於砷-鍺、鎵-鍺間鍵節能量之不同與低砷流量之緣故，使砷化鎵/鍺/矽異質結構間之砷與鍺原子內部擴散可有效被抑制。此實驗結果證明變溫砷界面層成長於鍺/矽基板上對未來欲成長三五族微電子元件或光電元件於矽基板上將具有極大潛力。

Substrate Misorientation Effects in Tunnel Junction Layers and GaAs Epitaxy Grown on Ge/Si Substrate for Low-cost High-efficiency III-V Multijunction Solar Cell Applications

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ABSTRACT

To further promote the competitiveness of III-V multijunction solar cells in the field, the conversion efficiency of solar cells has to increase while their cost must be reduced. In this thesis, we have demonstrated that the material properties of the P^{++}-AlGaAs/N^{++}-GaAs tunnel diodes (TDs) could be affected by misoriented GaAs substrates for III-V multijunction solar cell applications. The best surface morphology (0.154nm) and interface sharpness for the TDs were obtained on the (100) tilted 10° off toward [111] GaAs substrate. TD materials grown on this substrate can efficiently reduce oxygen-incorporation in N^{++}-GaAs layer, and also reduce the anisotropic sites for oxygen-incorporation in the P^{++}-AlGaAs layers. We also proved that InGaP/GaAs dual junction solar cells with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10°off GaAs substrates exhibit superior photovoltaic conversion efficiency (~20%) when operated at one sun, and produces higher EQE (~82% for InGaP top cell and 85% for GaAs bottom cell) as compared to the P^{++}-GaAs/N^{++}-InGaP TD. The cell design with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10°off GaAs substrates also displays superior

I-V characteristics when these solar cell devices were operated at higher concentration ratios (~185×). On the other hand, production cost of III-V multijunction solar cells can be largely reduced while III-V materials, such as GaAs epitaxy, are grown on Si substrates instead of traditional Ge substrates. We have demonstrated that the As prelayer grown using graded-temperature technique on the Ge/Si substrate annealed at 650℃ effectively improves the epitaxial quality of GaAs epitaxy (roughness: 1.1 nm, dislocation density: ~$2x10^{7}cm^{-2}$). Furthermore, the interdiffusion of Ge and As atoms in the GaAs/Ge/Si heterostructure can be effectively suppressed by the graded-temperature As prelayer because of the difference in energies between As-Ge and Ga-Ge bonds and low As flux. These results suggest that the graded-temperature As prelayer grown on Ge/Si substrate has great potential for use in the growth of III-V nanoelectronic devices and optoelectronic devices on the Si substrate.

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Chapter 1

Introduction

1.1 Brief introduction to photovoltaic industry

Solar energy is one of fastest growing industries in the energy field. Some research reports that total global new PV system installations reached 18.2GWp in 2010. However, the global PV market including silicon-base, thin film, organic solar cells, declines rapidly in 2011. Major reductions in subsidy levels are occurring across the major European PV markets in 2011. As European markets account for 80% of global demand, this will have a decisive effect on supply and demand in the global PV industry. However, the PV markets of China, India, America, Australia and other countries also have a great deal of growth momentum, which could even be sufficient to offset the impact of weakening European demand.

Many PV companies, including silicon-base, III-V thin film solar cells et al., are built in Taiwan in recent years because of good environment and opportunity. In Taiwan the technique of semiconductor, panel, electronic component industries is very mature and suitable for developing photovoltaic industry. Now the investments in PV industry in Taiwan main focus on Si-base solar cells because these type solar cells possess low cost and low threshold on the field. The conversion efficiency of commercial crystalline Si solar cells is only about 20%. Furthermore, Si-base solar cells cannot be operated at higher concentrated system. In order to gain higher conversion efficiency new investments on III-V thin film solar cells (concentrated

photovoltaic solar cells, CPVSCs) started in 2005. III-V solar cells (CPVSCs) are a “special innovation” in PV industry, which is operated under high concentrated ratios and is suitable in arid places or mid-arid places. III-V solar cell efficiency under high concentrated ratios is 60% in theory and 42% in production, considerably two times higher than traditional Si-based solar cells as shown in Fig.1-1. The basic properties of concentrated III-V multijunction solar cells will be discussed in next section.

1.2 Concentrated III-V multijunction solar cells and its challenges

Concentrated Photovoltaic technology uses several optical lenses (Fresnel) to focus large amounts of sunlight onto small photovoltaic surfaces to generate electricity more efficiently than traditional PV as show in Fig. 1-2. The greater efficiency comes from the photovoltaic cells used in CPV, which can be III-V multijunction cells instead of the crystalline silicon cells used in traditional PV systems. Fig.1-3 shows the typical distribution of solar radiation on the surface of the earth and if one could design the band gap of the III-V solar cells in a monolithic multijunction form having multiple semiconductor layers with different band gaps, the majority of the solar spectrum can be captured by the combination of cells.

Gallium arsenide (GaAs) is often used as middle junction in III-V multijunction solar cells that have nearly optimal band gap of 1.42eV. The conversion efficiency of GaAs single junction solar cells is about 25% [1]. It implies GaAs epitaxy, which is direct band gap

electric structure, as middle cell in III-V multijunction solar cells can absorb majority of visible light (~750nm) of solar radiation without any heating generation. Additional, the band gap distribution of GaAs-based materials, such as indium gallium arsenide (InGaAs), can be adjusted to absorb other solar energies with different wavelength by varying the elemental composition. Although III-V multijunction solar cells possess highest conversion efficiency (42%) in the world and can be operated at concentrator system, they are very expensive and are currently only used in high performance applications such as satellites and power plants due to their cost.

All CPV systems have an III-V multijunction solar cell device, a concentrator system including Fresnel lens and active solar tracking. In order to reduce the cost and increase the competitiveness of CPV, suncycle concentrator system is used instead of regular concentrator system in recent work [2] as shown in Fig. 1-4. The suncycle concentrator system is a compact concentrator solar panel which can be installed as a rooftop unit in both commercial and residential buildings. It uses optical technology for concentrating sunlight on an III-V solar cell. Optimization algorithms help to track the movements of the sun, making the most of the available sunlight. On the other hand, the promotion of conversion efficiency of III-V multijunction solar cells and the reduction of epitaxial cost during III-V material growth are also an efficient way to decrease overall CPV cost. The detailed description about decreasing the production cost of III-V multijunction solar cell will be shown in the chapter 2.

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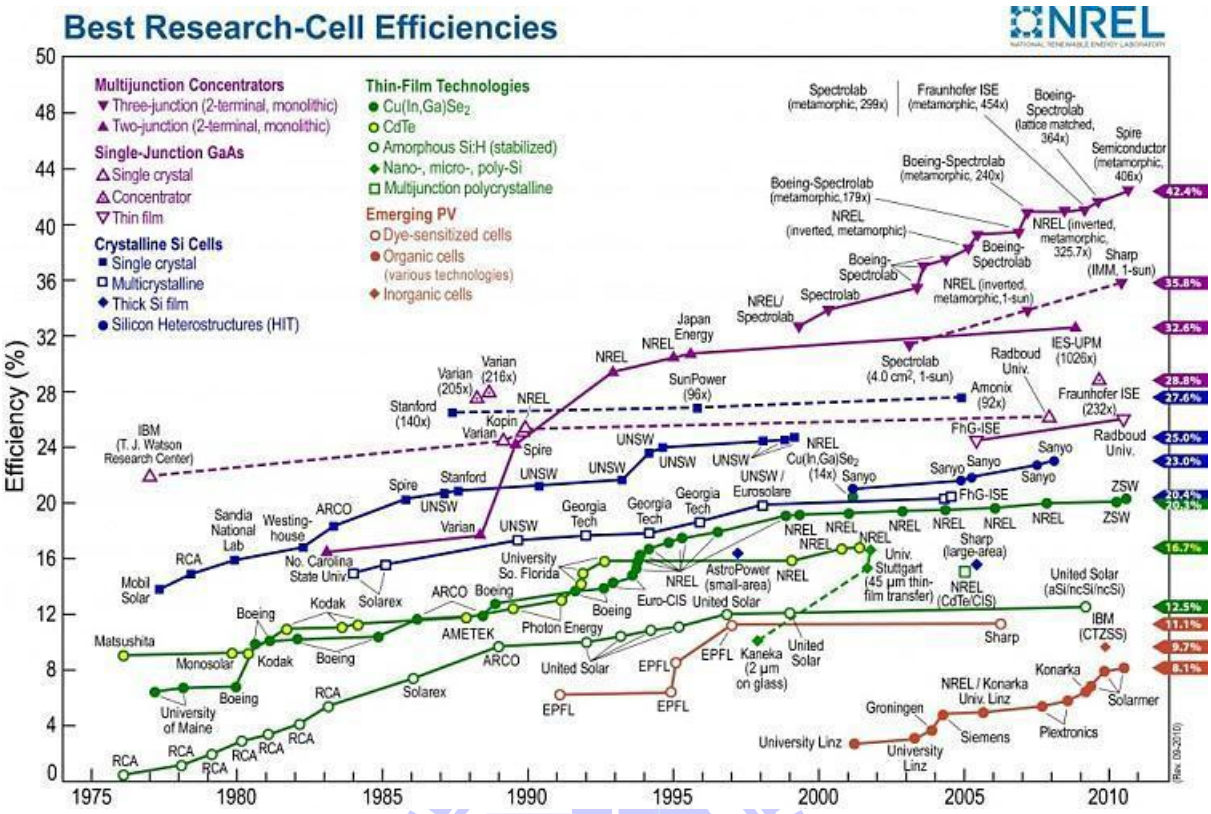

Figure 1-1 Best research solar cell efficiencies reported by NREL

Figure 1-2 Concentrated III-V multijunction solar cells

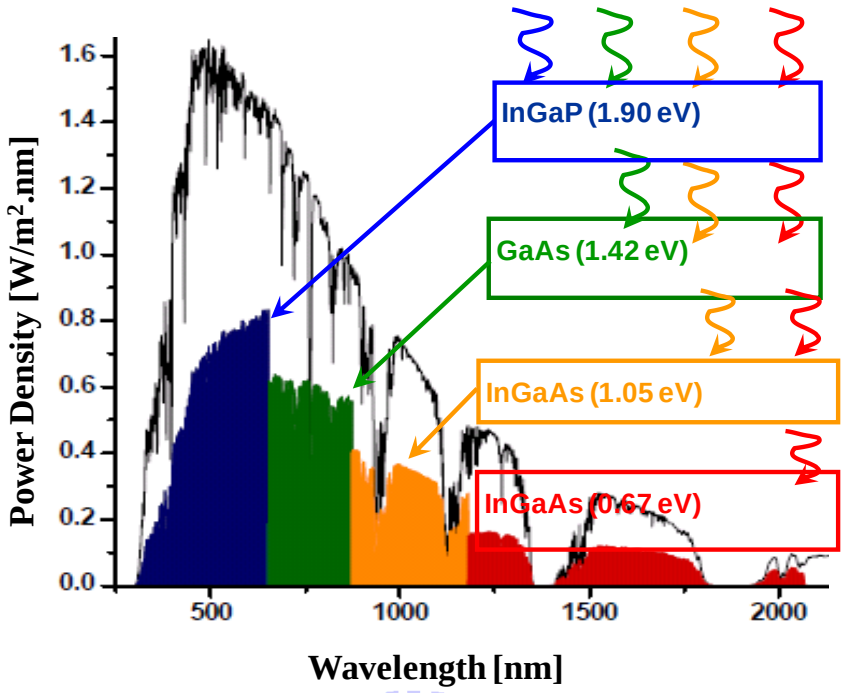

Figure 1-3 Absorption spectrum of III-V multijunction solar cells with different band gaps on earth

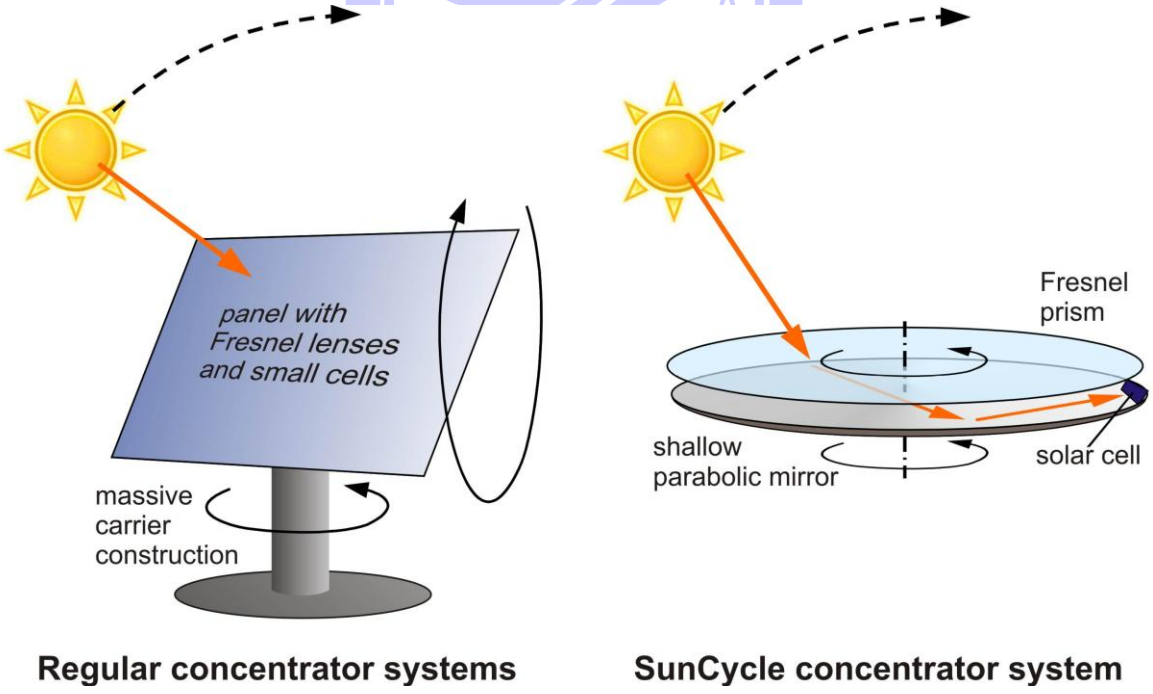

Figure 1.4 Images of regular concentrator systems and suncycle concentrator system

Chapter 2

Development of low-cost high-efficiency III-V solar cells

2.1 Methods for improving efficiency of III-V solar cells

PV energy conversion is the direct production of electrical energy in the form of current and voltage from electromagnetic (i.e., light) energy. The basic four steps needed for photovoltaic energy conversion are: (a) a light absorption process which causes a transition in a material from a ground state to an excited state. (b) the conversion of the excited state into a free negative-charge and a free positive-charge carrier pair, (c) a discriminating transport mechanism, which causes the resulting free negative-charge carriers to move in one direction (to the contact of a cathode) and the resulting free positive-charge carriers to move in another direction (to the contact of a anode), (d) combining with an arriving positive-charge carrier, thereby returning the absorber to the ground state. In order to improve the conversion efficiency of III-V multijunction solar cells, we have to know these basic fundamental and find out some materials or methods to enhance the solar cell efficiency. Here, some methods for increasing the conversion efficiency will be generalized and shown in the following.

(A) Antireflection coating (AR coating) or surface texture: a structured surface of III-V multijunction solar cells enhances the optical path length and reduces the optical reflection while light inject into solar cell devices.

(B) Lower series resistance (R_s): converted energy losses due to the series resistance caused

by large currents (J_{sc}) decrease the conversion efficiency of III-V multijunction solar cells under high concentration ratios. R_s becomes a dominant factor of cell efficiency with increasing current. If shunt resistance (R_{sh}) of III-V solar cells is sufficiently large to be neglected, the I–V characteristics of the solar cells including series resistance (Rs) are shown in equation (2.1):

$$I = I_0\left\{\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right\} - I_{sc}. \tag{2.1}$$

Therefore, the contact resistance has to be reduced sufficiently using optimal N-GaAs contact material and P-Ge contact material to minimize series resistance losses when III-V solar cells was operated for concentrator applications.

(C) High Epitaxial quality for III-V solar cell devices: the I-V characteristic of III-V solar cell devices mainly depends on superior epitaxial quality. For III-V solar cell devices, the poor quality results in smaller shunt resistance which decreases open-current voltage (V_{oc}). Besides, structure of III-V multijunction solar cells include back surface field (BSF) layer, base layer, emitter layer, window layer and tunnel diode (TD) grown between two subcells. It is more complicated than other devices; therefore, the growth technology is very important per united component of III-V solar cell devices to further increase conversion efficiency.

(D) Substrates: The growth of III-V solar cell devices has been restricted to lattice matched, crystalline substrates such as GaAs and germanium (Ge). Ge has been the substrate

material of choice for commercial III-V solar cell devices because it offers the opportunity to form a bottom photovoltaic junction as well as being more powerful in production cost as compared with GaAs substrate, thereby allowing the use of a thinner substrate, resulting in a lower mass solar cell. Unfortunately, Ge substrate offers no capability to integrate the finished photovoltaic device into a flexible module and its price still higher than Si substrate leading to the development limitation of III-V multijunction solar cells.

2.2 Tunnel diode development in III-V multijunction solar cells

Tunnel diode (TD) is one of the important issues affecting III-V multijunction solar cell performance. The problems of TD growth are related to the demand of obtaining transparent and uniformly highly doped layer without degradation of surface morphology. The thickness of the TD has to be about several ten nanometers, while the doping concentration have to be achieved around 10^{19}-10^{20} cm^{-3}. The reaching of the high doping level is complicated by the fact that P-type and N-type dopant (i.e., SiH_4, DeTe, TMZn, CB_{r4}…) may require different growth temperature and growth parameters, making more difficult to obtain abrupt doping profile. Because of high doping concentration in TD material the interdiffusion from TD to BSF layer have to be avoided. The double heterostructure (DH) TD was found to be useful for suppressing unwanted interdiffusion from the tunnel diode [1-3]. On the other hand, the dopant materials with lower diffusion coefficient, such as CBr_4 and DeTe, are also chosen to

replace other dopants during the TD growth. Once an abrupt doping profile is obtained, the TD in III-V multijunction solar cells must resist to the thermal load produced by the growth cycle of the solar cell structure. The detailed description for obtaining high quality TD without any interdiffusion will be shown in chapter 3 and then InGaP/GaAs dual junction solar cells with different TD materials will be also discussed in chapter 4.

2.3 Integration of III-V material on Si substrate

Currently, the installation of III-V multijunction solar cells (InGaP/InGaAs/Ge) is limited by the relatively high cost of III-V solar cells as compared to silicon-based solar cells [4]. Therefore, the integration of the GaAs/Ge heterostructure on Si substrates as an alternative template for low cost and high conversion efficiency III-V based solar cells has attracted much attention [5,6]. Si has many advantages as compared to traditional Ge and GaAs substrates that contain higher thermal conductivity, lower weight, lower cost, and extensive development to solar cell processes using traditional Silicon-base process technologies. For terrestrial solar cells, a graded SiGe interlayer as buffer layer is often grown on Si substrate to relax strains because of larger lattice mismatch (4.2%) between Si and Ge generates many dislocations in the deposited Ge layer [7]. In this thesis, we have cooperation with Dr. Yamamoto in Innovations for High Performance Microelectronics (IHP), Germany. Low threading dislocation density (TDD) Ge bulk was grown on Si substrate without any SiGe

buffer layer by Yuji Yamamoto et al. using reduced pressure chemical vapor deposition (RPCVD) [8]. Low TDD of ~$7\times10^{5}cm^{-2}$ is achieved for 4.7μm Ge thick layer with a lower surface roughness (RMS~0.44nm). If III-V multijunction solar cells can be grown on Ge/Si substrate using GaAs-base buffer layer to replace traditional InGaP/(In)GaAs/Ge solar cells, the cost of CPVSCs will be further decreased. The detailed description for III-V material (GaAs) on Ge/Si substrate will be shown in chapter 5.

2.4 Motivation

The development of an advanced technique that can enhance photovoltaic conversion efficiency while maintaining the lower APD formation and depressed interdiffusion in the GaAs/Ge system is necessary for the development of low-cost and high-efficiency III-V optoelectronic devices on Si substrate.

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Chapter 3

Effect of Substrate Misorientation on the Material Properties of GaAs/ $Al_{0.3}Ga_{0.7}As$ Tunnel Diodes

3.1 Principles of a tunnel diode

A tunnel diode (TD) forms the electrical connection between two subcells in multijunction photovoltaic cells where electrons tunnel from occupied energy states on N^{++} side of the barrier to unoccupied energy states on the P^{++} side. The current density of a tunneling diode is composed of three components as shown in equation (3.1) and the current-voltage (I-V) characteristics for a tunnel diode is shown in Fig. 3-1.

$$J= J_{tunnel} +J_{excess} + J_{thermal} \quad (3.1)$$

These components are J_{tunnel}, the band-to-band tunneling current density, J_{excess}, the excess current density, and $J_{thermal}$, the minority-carrier diffusion current density or thermal current density. The forward bias of a tunnel diode is increased from zero, the quantum mechanical tunneling leads to an increase of current at first. It reached a peak value and then decreases. Combining the forward diode characteristic with the tunneling curve yields an idealized characteristic as shown by the solid line in Fig. 3-1.

The band-to-band current component is shown in Eq. (3.2)

$$J_{tunnel} = J_{peak}\left(\frac{V}{V_{peak}}\right) exp\left(1-\frac{V}{V_{peak}}\right) \quad (3.2)$$

Where V is the drive voltage, J_{peak} is the current density and V_{peak} is voltage at the onset of the

negative differential resistance region, respectively. The maximum value of tunneling current occurs at $V_{peak} = (V_n+V_p)/3$. The detailed equation in the term V_{peak} has been determined to be in Eq. (3.3).

$$V_{peak} = \frac{V_n + V_p}{3} \approx \frac{k_B T}{3q}\left[\ln\frac{N_d}{N_c} + \ln\frac{N_a}{N_v} + 0.35\left(\frac{N_d}{N_c} + \frac{N_a}{N_v}\right)\right] \quad (3.3)$$

where V_n is the amount of degeneracy on the n side, $[V_n = (E_{Fn}-E_c)/q]$, where E_{Fn} is the electron quasi-Fermi energy and E_c is the conduction band energy. V_p is the amount of degeneracy on the P side, $[V_p= (E_v- E_{Fp})/q]$, where E_{Fp} is the hole quasi-Fermi energy and E_p is the valance band energy. k_B is Boltzmann's constant, T is the temperature, q is the charge, N_d is the donor concentration, N_a is the acceptor concentration, N_c is the effective density of states in the conduction band. Actually, the probability of band-to-band tunneling decreases with an increase in the forward bias because of the decrease of the field term. Hence the peak-current point shifts to the left and occurs at a lower voltage.

The second component is excess current shown in the valley region (in Fig. 3-1). There is a minimum current point in the region where the tunneling characteristic meets the forward-diode characteristic. In this idealized curve, the current at this minimum point can be very small. The ratio of peak tunneling current to the valley point can be very high. There is a certain amount of "excess" current which raises the minimum current to such a value that the practical peak-current-to valley-current ratio is in the order of 10 to 20. They are not accounted for by the tunneling mechanism and the thermal current. The excess current

component is:

$$J_{excess} = J_{valley} \exp\left[\frac{4}{3}\left(\frac{m^*_{eff}\epsilon_s}{N^*_{eff}}\right)^{1/2}(V - V_{valley})\right] \tag{3.4}$$

where J_{valley} is the current density and V_{valley} is the voltage at the end of the negative differential resistance region. The excess current component is the most difficult term to determine theoretically because a high degree of knowledge of the growth conditions and environment must be known and quantified, so effects, such as from traps and dislocations, are known prior to device growth. This current joins the exponential excess current and the direct tunneling current and forms a smooth but higher valley. Brody [1] suggested that the valley excess current was caused by tunneling between tailing states which have been separated from the band edge by the heavy doping.

The third component is thermal or minority carrier diffusion current shown in Eq. (3.5) and Fig. 3-1.

$$J_{thermal} = J_o\left[\exp\left(\frac{qV}{k_BT}\right) - 1\right] \tag{3.5}$$

where

$$J_o = qn_i^2\left[\frac{1}{N_a}\sqrt{\frac{D_n}{\tau_n}} + \frac{1}{N_d}\sqrt{\frac{D_p}{\tau_p}}\right] \tag{3.6}$$

where n_i is the intrinsic carrier concentration, D_n is the electron drift diffusion coefficient, D_p is the hole drift diffusion coefficient, τ_n is the electron lifetime, and τ_p is the hole lifetime.

Detailed descriptions of the band diagram and IV characteristics in various states of operation of a tunnel junction are shown in Fig. 3-2. Figure 3-2(a) shows the reverse-biased configuration. Electrons can tunnel easily from p-type side to n-type side when tunnel diodes was operated at larger the reverse-bias. Figure 3-2(b) shows the device in thermal equilibrium. The Fermi-level is the same for n-type and p-type material and no net current is generated under this condition. Figure 3-2(c) shows the band-to-band tunneling. As the forward bias is increased, more occupied states on the electron side coincide with unoccupied states on the hole side. This occurs up to a maximum tunneling current where $E_{Fn} - E_V = E_C - E_{Fn}$ as shown in Figure 3-2(d). Figure 3-2(e) shows negative differential resistivity (NDR) region where the overlap of occupied states on the electron side and the unoccupied states on the hole side decreases to a point where there is no longer any overlap between the two. The current does not go to zero because the excess current component is non-negligible. Figure 3-2 (f) shows minority-carrier injection current or thermal current as obtained in standard p-n junction diodes.

For an actual tunnel diode, there is also the substance resistance and the contact resistance of the loads. These resistances occur in series with the diode and modify the I-V curve by shifting the high current portion of the characteristic to a higher voltage. This modification is more noticeable at the peak-current point (I_{peak}), where a small increase of voltage can be a significant percentage of the total amount. Figure 3-3 shows the shift of the peak current by

the series resistance [2].

3.2 Properties of GaAs/$Al_{0.3}Ga_{0.7}As$ tunnel diode

AlGaAs epitaxy is potentially of great important for many high-speed electronics and optoelectronic devices [3,4], because the lattice parameter different between GaAs and AlGaAs is very small, which avoids the generation of undesirable interface states. AlGaAs epitaxy with excellent minority carrier mirror properties in optoelectronic devices may be also used for the P-type material due to stronger bonding strength between Alumina (Al) atoms and carbon (C) atoms, avoiding the high optical absorption of P-type GaAs. Therefore, GaAs/AlGaAs heterostructure is very suitable as tunnel diode (TD) materials for III-V solar cell application.

The use of heterojunction TD (GaAs/$Al_xGa_{1-x}As$) with higher conduction band also offset [5] provides higher tunneling current (J_{tunnel}) as compared to the traditional GaAs/GaAs TD structure. However, $Al_xGa_{1-x}As$ epi-layers are known to be sensitive to oxygen and carbon impurities, which produces excess current (J_{excess}) via energy states inside the band gap. It has been reported that the reduction of these impurities from an AlGaAs epi-layer can be achieved using shorter growth interruption [6], liquid metal bubblers [7] and (311) oriented GaAs substrates [8,9]. But it is difficult to use these methods for commercial applications because of surface roughness and wafer cleaving problems [6~9].

Alternatively, oxygen incorporation in AlGaAs can also be reduced by using a higher growth temperature (> 750°) and a higher V/III ratio. However, the increase of growth temperature and V/III ratio will lead to the reduction of carbon doping level during the GaAs/$Al_xGa_{1-x}As$ TD growth [10,11]. Therefore, the development of an advanced technique which decreases oxygen-incorporation while maintaining high carbon doping in P^{++}-AlGaAs is necessary for the GaAs/$Al_xGa_{1-x}As$ TD application.

3.3 Growth of GaAs/ $Al_{0.3}Ga_{0.7}As$ heterostructure on misoriented GaAs substrates

Misoriented GaAs substrate is widely used to produce the optimum surface morphologies for essentially all V/III semiconductors, including GaAs. Furthermore, Kuech and Veuhoff [12] found that a effect of substrate morientation on carbon incorporation that they contributed to the increased affinity of CH_3 radicals for electron-rich As surface. J. van de van et al. [13] also reported a significant increase in mobility as well as the net carrier concentration due to a decrease in the carbon concentration as the misorientation angle was increased form 0° to 4°. A expected mechanism is related to the reaction velocity of the steps on the surface at which atoms are incorporated during material growth [13]. For small misorientation, the number of steps is small, resulting in a large reaction velocity on the surface. The repidly moving steps "trap" carbon before it can interact with atomic H. The trapped "CH_3" radical is suggested to form a second to an adjacent Ga, leading to release of H atoms and incorporation of carbon

atom into the solid. Increasing the misorientation may increase the number of steps on the surface. This leads to an increased time for interaction of CH_3 adsorbed to a Ga at a step with AsH, producing CH_4. Similar behavior is also observed for [110] and [-110] oriented steps, as shown in Fig. 3-4. An alternate explanation is related to the rate of production of atomic H on the surface from the pyrolysis of AsH_3 [14]. The presence of surface steps and kinks is postulated to increase the AsH_3 pyrolysis rate and the local production of H and AsH species on the surface that react with CH_3 to produce CH_4. This will, of course, reduce the rate of carbon incorporation into the solid.

An abrupt increase in carbon incorporation is observed for (311)A substrate orientation. High carbon incorporation for this orientation has also been observed for AlGaAs [14] and InGaAs [15]. This suggests that (311)A substrate orientation possesses higher step density which leads to highest AsH_3 local pyrolysis rate and a minimal amount of carbon incorporation. It proves that misorientated substrates have been used to reduce the background carbon concentration in undoped GaAs epitaxial layers [12,13]. Recently, this concept is also used in undoped GaAs/$Al_{0.3}Ga_{0.7}As$ quantum well in order to obtain superior surface morphology and optical properties by using substrates with small misorientation angles, i.e. from 0~0.6°[16]. Although there have been a number of reports on the impurity-incorporation in GaAs and AlGaAs [12~14,16], the properties and impurity incorporation mechanism of the GaAs/$Al_xGa_{1-x}As$ TDs grown on misorientated GaAs substrates remained unclear.

3.4 Experiment

In this part, we report on the investigation of the growth of GaAs/$Al_{0.3}Ga_{0.7}As$ TDs on misorientated substrates for multijunction III-V solar cell applications. The (100) substrates were cut 0°, 2°. 6°, 10°,15° off toward the [111] direction. The structure used in the study was N^{++}-GaAs(1~3x$10^{19}cm^{-3}$, 30~40nm)/P^{++}-$Al_{0.3}Ga_{0.7}As$(1~5x$10^{19}cm^{-3}$, 30~40nm) with GaAs as the buffer layer. Growth is performed with metal organic chemical vapor deposition (MOCVD, EMCORE D180) system. Trimethylgallium (TMG) and trimethylaluminum (TMAl) were used as group III source, whereas pure arsine (AsH_3) with low H_2O content was used as group V source. The precursors for P-type and N-type dopant were carbon-tetrabromide (CBr_4) and dimethyl-telluride (DMTe), respectively. The growth temperature was varied from 600℃ to 640℃ and was determined by PYRO sensors. The V/III ratios used were 45 and 12 for the growth of GaAs and $Al_{0.3}Ga_{0.7}As$, respectively. All films in this study were grown at low-pressure of 40 torr with hydrogen flow rate of 28000sccm. Atomic Force Microscopy (AFM) was used to investigate the surface morphology and roughness of the GaAs/$Al_{0.3}Ga_{0.7}As$ TDs; Secondary Ion Mass Spectrometry (SIMS) was used to identify the dopant distribution and the relative impurity contents in the GaAs/$Al_{0.3}Ga_{0.7}As$ TDs. The crystalline quality and carbon-incorporation of the GaAs/$Al_{0.3}Ga_{0.7}As$ TDs were inspected using high-resolution x-ray diffraction (HRXRD).

3.5 Results and discussion

3.5.1 Effect of substrate misorientation on the surface morphologies of GaAs/AlGaAs Tunnel diodes

Figure 3-5 illustrates the AFM images of GaAs/$Al_{0.3}Ga_{0.7}As$ TDs grown on GaAs substrates with different misorientation angles. The root mean square (RMS) roughness of GaAs/$Al_{0.3}Ga_{0.7}As$ TDs grown on 0°, 2°, 6°, 10°,15° off oriented GaAs substrates were about 1.23 Å, 1.52 Å, 2.03 Å, 1.54 Å, and 2.74Å, respectively. The TD surface morphology is closely related to the substrate orientation, film thickness, film composition, dopant type, and doping concentration. The thickness and dopant type were constant for all samples in this study. According to the AFM results, the GaAs/$Al_{0.3}Ga_{0.7}As$ TDs grown on 0°, 2° and 10° off GaAs substrates have smoother surface. The rougher surface morphology for GaAs/AlGaAs TDs grown at other misorientation angles may be caused by the following reasons. First, the dopant diffusion in heavily doped GaAs/$Al_{0.3}Ga_{0.7}As$ layers may lead to the degradation of the morphology of the epitaxial layers [17]. Secondly, the surface also becomes rougher with the increase of Al composition in $Al_xGa_{1-x}As$ layer, especially for x=15~45% [18]. Finally, the increase of oxygen-incorporation into GaAs layer may also further reduce the surface smoothness of a GaAs/AlGaAs heterostructure [19]. S. Nayak et al. [19] reported that surface roughness of GaAs epitaxy decreases with increase of oxygen doping concentration during material growth as shown in Fig. 3-6 and Table 3-1. The surface morphology could be

affected, consisting of 3D clusters, by a bulk oxygen doping concentration of larger than $10^{19}cm^{-3}$. There are many factors that can affect the surface morphology of GaAs/AlGaAs TD; therefore, we will further discuss the relationship between impurity and epitaxial quality for GaAs/AlGaAs TD grown on misorientated GaAs substrate.

3.5.2 The properties and impurity incorporation mechanism of the GaAs/AlGaAs tunnel diodes grown on misorientated GaAs substrates

Figure 3-7(a) illustrates the SIMS depth profiles of oxygen in the GaAs/$Al_{0.3}Ga_{0.7}As$ TD layers grown on GaAs substrates with different misorientations. Oxygen is known as deep acceptor and non-radiative trap, which decreases the tunneling probability of electrons in GaAs/$Al_{0.3}Ga_{0.7}As$ TDs. In this study, it is found that oxygen atoms in the heavily doped GaAs/$Al_{0.3}Ga_{0.7}As$ TDs are mobile enough to segregate at the surface, or be trapped at the interface [20,21]. The SIMS data also indicates that less oxygen contamination was found in the P^{++}-AlGaAs layer grown on 10° off GaAs substrates as compared to those grown on other misorientations. The amount of impurity in AlGaAs depends on Al content [22] and availability of anisotropic sites [23]. The anisotropic sites possess high affinity for contaminant incorporation. The variations of Al content in P^{++}-AlGaAs layer are displayed in Fig. 3-7(b). It indicates a sharp increment in Al content when the GaAs/$Al_{0.3}Ga_{0.7}As$ TDs were grown on the 0° and 2° off GaAs substrates. However, the oxygen concentration does

not follow the initial Al content increment and it suggests that the existence of anisotropic sites is a more important factor than Al content for oxygen-incorporation in the P^{++}-AlGaAs layer. The use of 10° off GaAs substrate can practically reduce the anisotropic sites; therefore, it is a practical technique besides the increase of growth temperature and V/III ratio, to suppress the oxygen-incorporation in P^{++}-AlGaAs layer of a GaAs/$Al_{0.3}Ga_{0.7}As$ TD.

According to the SIMS and AFM results, the surface morphology of a GaAs/$Al_{0.3}Ga_{0.7}As$ TD was not affected by the dopant elements because carbon and tellurium as P type and N type dopant atoms are less mobile during the III-V film growth. The reason for the degradation of the GaAs/$Al_{0.3}Ga_{0.7}As$ TD surface morphology is mainly due to higher oxygen content in the N^{++}-GaAs layer [19], as shown in Figure 3-7(a). The substrates with larger offcut, such as 10°, have more Ga atoms exposed on the surface. They can effectively reduce the number of As vacancies on the surface and thus reduce the sticking coefficient for oxygen incorporation [21]. Moreover, smoother surface is also observed for material grown on small misorientations, such as 0°, which have higher oxygen contamination as compared to 10° off, due to the Gibbs-Helmholtz surface free energy [24]. The surface free energy increases with the substrate misorientation angle. Higher misorientation angles imply the existence of a quasi-liquid layer during material growth, leading to an unstable morphology with a hill-and-valley structure on the top surface [25]. These results demonstrated in Fig. 3-5 and Fig. 3-7(a) indicate that (100) substrates 10° off toward [111] not only reduce the content of

oxygen-impurity in the N^{++}-GaAs layers but also reduce Gibbs-Helmholtz surface free energy to produce a smooth surface on the GaAs/$Al_{0.3}Ga_{0.7}As$ TDs.

Figure 3-8 illustrates the HRXRD results of the GaAs/$Al_{0.3}Ga_{0.7}As$ TDs grown on different misorientation GaAs substrates. The lattice contraction model [26] describes the relationship of lattice constant variation as a function of carbon-incorporation as shown in equation (3-7):

$$\triangle a = N_{CAs}\,(r_c - r_{As})(1+\rho) \qquad (3\text{-}7)$$

where $\triangle a$ is lattice constant variation; N_{CAs} is the density of carbon atoms on the arsenic sites; r_c and r_{As} are the covalent radii of carbon (0.774 Å) and arsenic (1.225Å), respectively; ρ is the compensation ratio of N_{CGa}/N_{CAs}; N_{CGa} is the density of carbon atoms on Ga sites. Equation (3-7) shows that the carbon-incorporation may induce the lattice contraction [26,27]. Substitutional carbon atoms in the lattice of the GaAs/AlGaAs heterostructure will reduce the mean lattice constant of the structure. The observed peak splitting for AlGaAs XRD peaks as shown in Fig. 3.8 increases with the increasing misorientation angle, meaning that these spectra are carbon-incorporation related [27]. It demonstrates that carbon doping efficiency, not the background carbon doping, increases with the increase of the misorientation angle during the GaAs/$Al_{0.3}Ga_{0.7}As$ TDs growth. The same trend can be observed for the carbon concentration in the AlGaAs layers grown with different misorientation angles, as shown in Fig. 3-7(d). If substitutional carbon atoms were incorporated in the group III sites, they would

occupy the Ga sites rather than Al sites due to the stronger Al-C bond (66Kcal/mole) as compared to the Ga-C bond (59Kcal/mole) [18,28]. However, the Al content in the 15° off GaAs substrate decreases rapidly, but the Ga content does not have apparent change during the P^{++}-$Al_{0.3}Ga_{0.7}As$ growth, as can be observed in Fig. 3-7(b) and (c). It is believed from these data that the bonding strength between Al-C and Ga-C could be changed [29] and substitutional carbon would be incorporated in the Al sites resulting in the reduction of Al composition of a GaAs/$Al_{0.3}Ga_{0.7}As$ TD when the 15° off substrates were used.

3.6 Summary

It has been demonstrated that the misorientation of GaAs substrates has a direct effect on the material properties of the N^{++}-GaAs/P^{++}-AlGaAs TDs for multijunction III-V solar cell application. The best surface morphology and interface sharpness for the TDs were obtained on the (100) tilted 10° off toward [111] GaAs substrate. Results show that the TD materials grown on this misoriented substrate can overcome the limitation of high surface free energy and with reduced sticking coefficient for oxygen-incorporation in the N^{++}-GaAs layers. Besides, this substrate has also reduced the anisotropic sites for oxygen-incorporation in the P^{++}-AlGaAs layers. These results can be used for the growth of inverted metamorphic multijunction solar cell structures, which is built on GaAs based substrates and inverted onto other substrates [30].

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Table 3-1 Surface rms roughness (ρ in nm) and wavelength of periodic (λ in nm) surface structure in 1μm thick GaAs (001) with several concentrations of O are shown. The λ and amplitude (*A* in nm) are shown up to 10^{18} cm^{-3} [O] in GaAs. The breakdown of periodic structure at higher oxygen concentrations makes analysis not meaningful there.

	[O] in GaAs (cm^{-3})					
	10^{20}	2.6×10^{19}	3×10^{18}	2.6×10^{17}	2×10^{16}	Nominally undoped
σ(1 μm×1 μm)	37.2±10	5.91±1.0	0.98±0.1	0.58±0.1	0.55±0.1	0.62±0.1
σ(5 μm×5 μm)	56.7±10	24.19±10	2.09±1.0	1.21±0.2	0.90±0.2	0.76±0.1
λ at max. A^2			30.8	40.6	46.1	56.2
max. A			1.41	1.73	1.90	2.21
λ at (A^2/2)			25–44	32–60	38–55	44–72

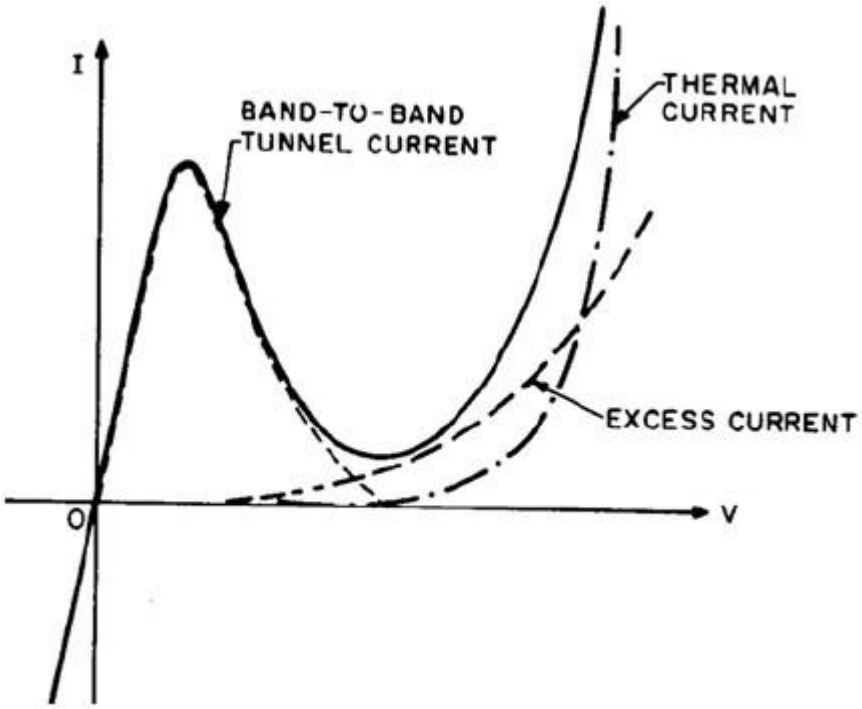

Figure 3-1 Diagram of I-V characteristics of a tunnel diode including three components [1]

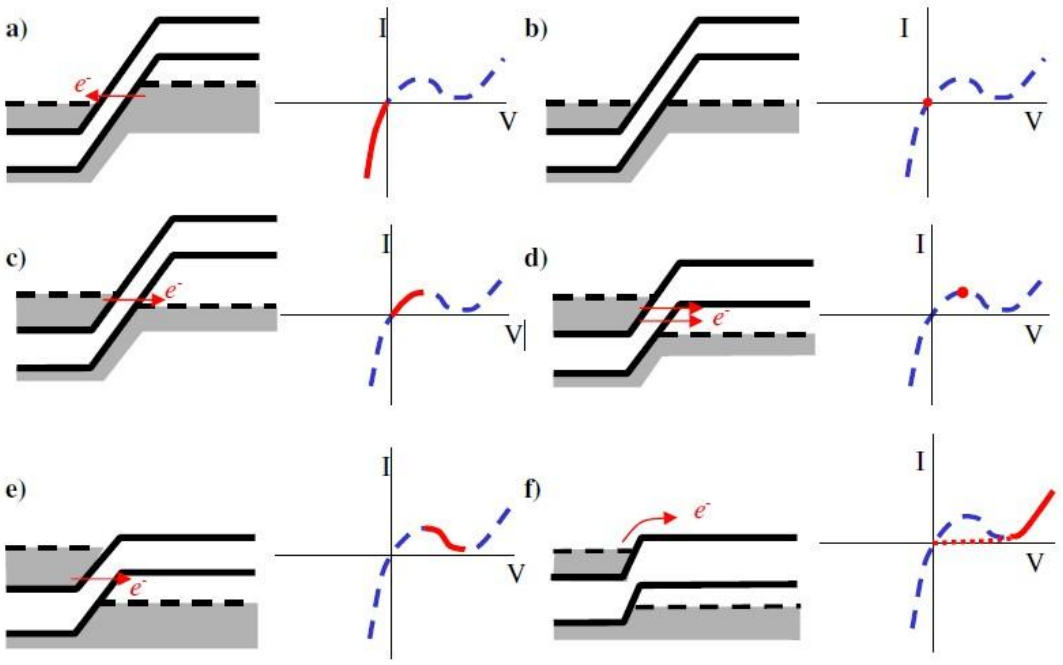

Figure 3-2 Diagram of a tunnel diode (a) reverse-biased tunneling, (b) thermal equilibrium, (c) forward-biased tunneling, (d) maximum forward-biased tunneling current, (e) negative differential resistance, (f) minority-carrier injection current.

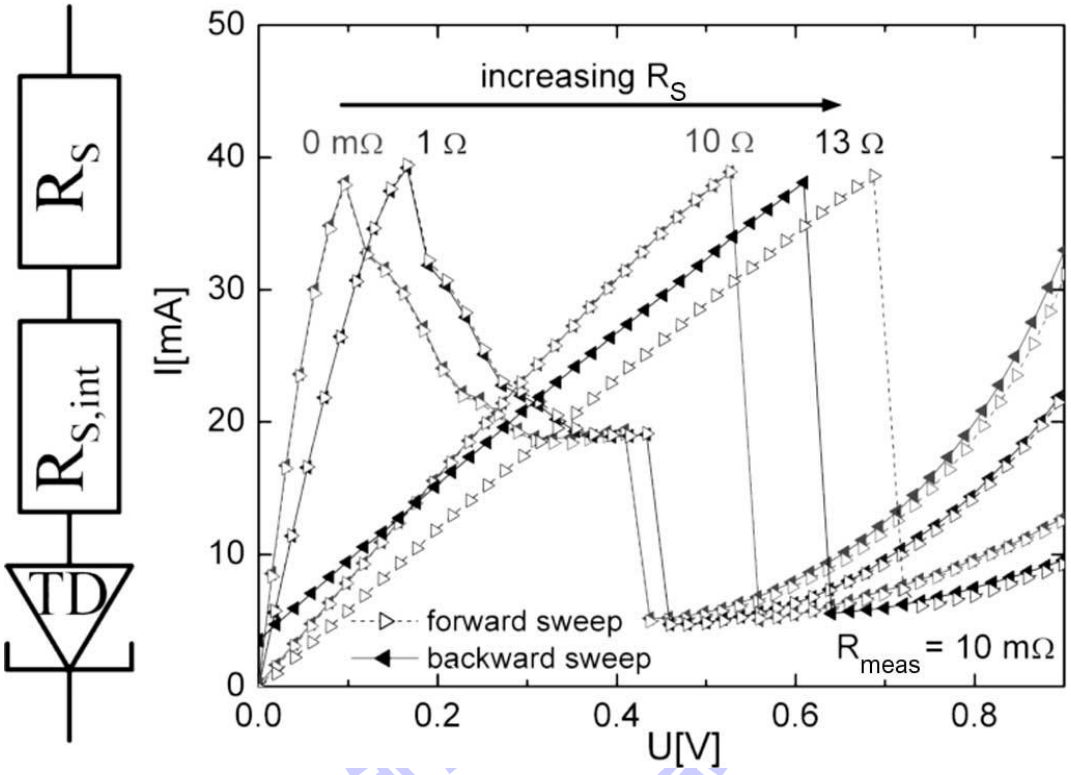

Figure 3-3 Equivalent circuit diagram of a test structure with isolated tunnel diode. An additional resistor R_S was used to simulate high internal serial resistances. Right: Influence of internal serial resistance on the I–V characteristic of a GaAs tunnel diode. The graph with R_S = 0 Ω shows the I–V characteristic of the tunnel diode used. Increasing R_S (1 Ω) leads to a sheared I–V curve and then results in a discontinuity (10 Ω). Very high R_S (13 Ω) finally causes a different characteristic for the forward and backward voltage sweeps (hysteresis). [2]

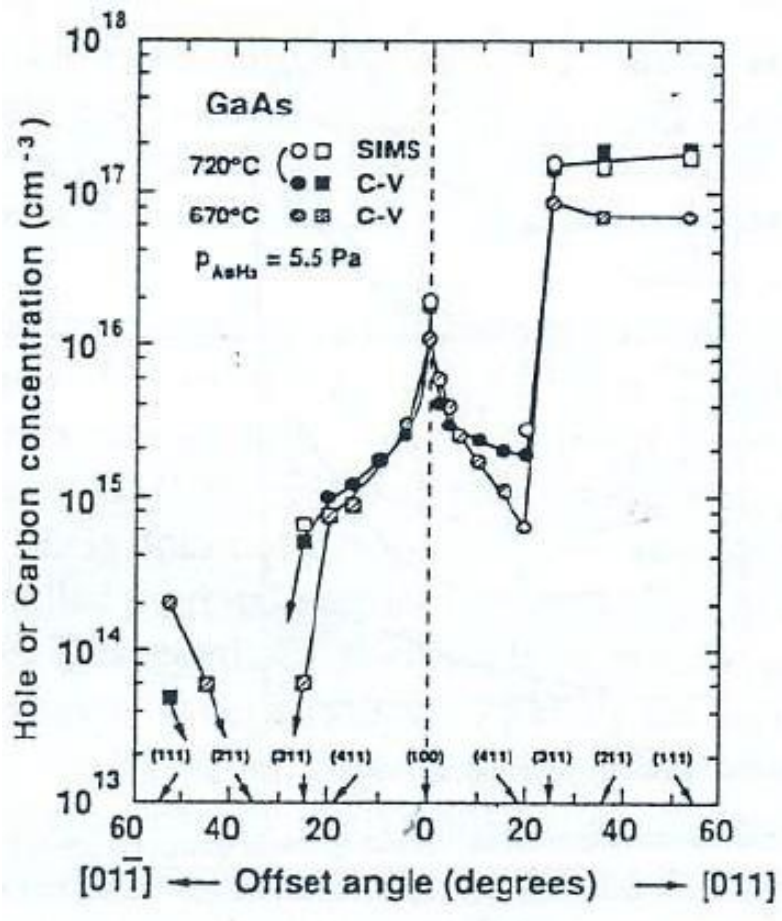

Figure 3-4 Dependence of hole or carbon concentration on orientation for GaAs. Square symbols represent results on poor surface morphology. [13]

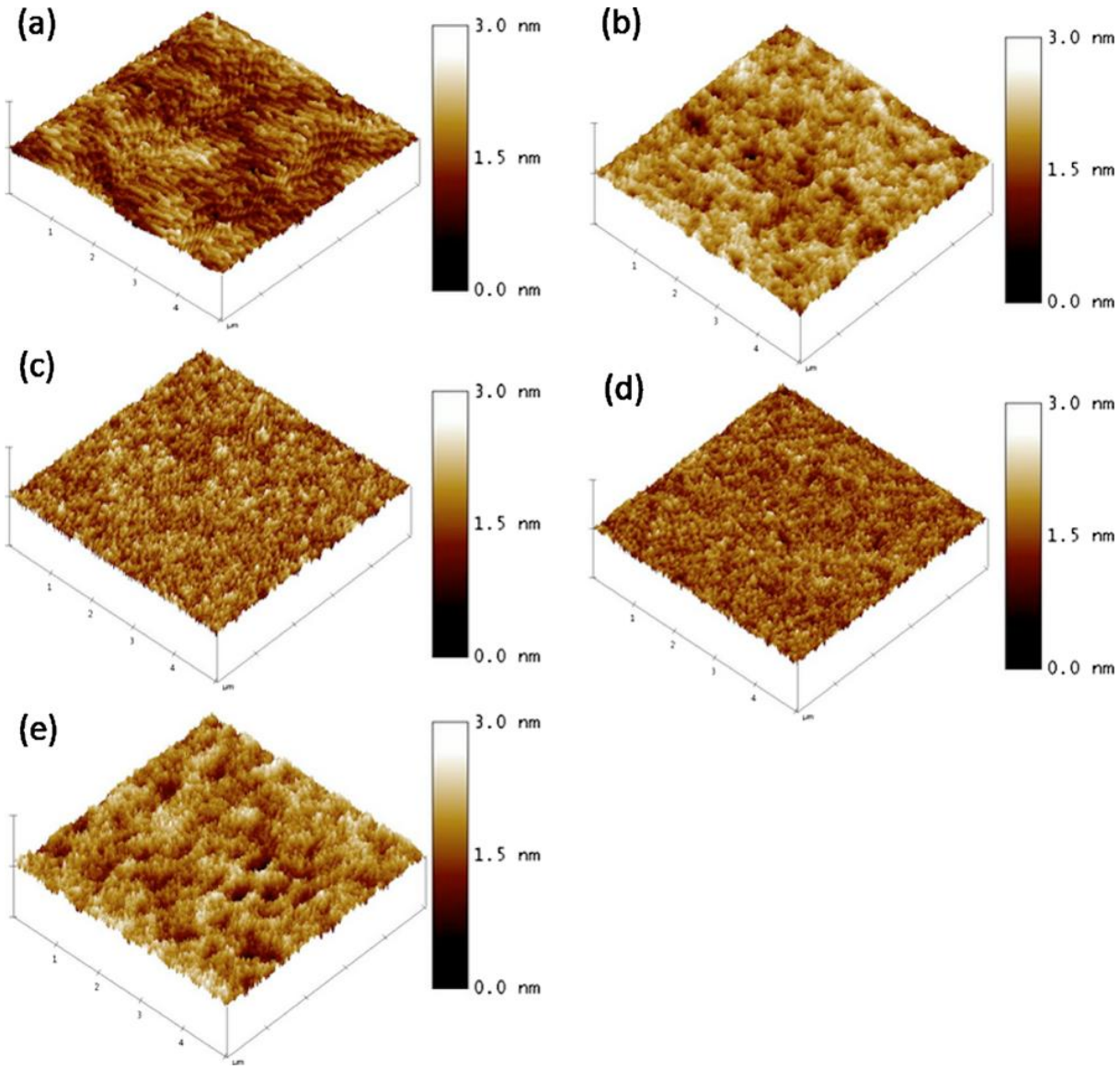

Figure 3-5 The AFM images (5μm×5μm) of GaAs/$Al_{0.3}Ga_{0.7}As$ TDgrown on GaAs substrates offcut by (a) 0°, (b) 2°, (c) 6°, (d) 10°, and (e) 15°.

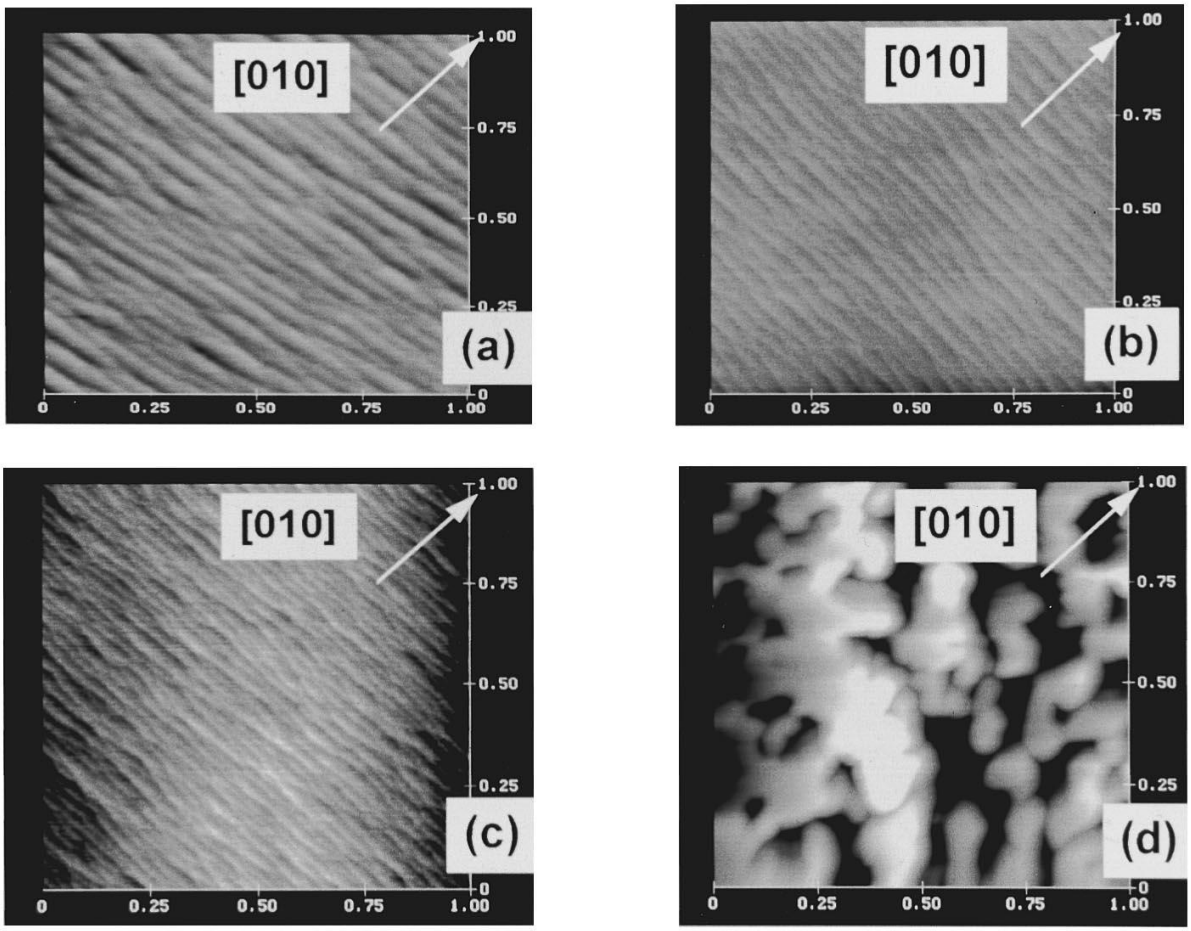

Figure 3-6 AFM images of oxygen doped GaAs; (a) nominally undoped, (b) 10^{16}, (c) 10^{18}, and (d) 10^{20} cm^{-3}. A periodic ripple structure in the miscut direction is established through step bunching for all but the highest doping levels. The ripple wavelength decreases as [O] increases. The 3D-cluster growth takes place at highest doping. [19]

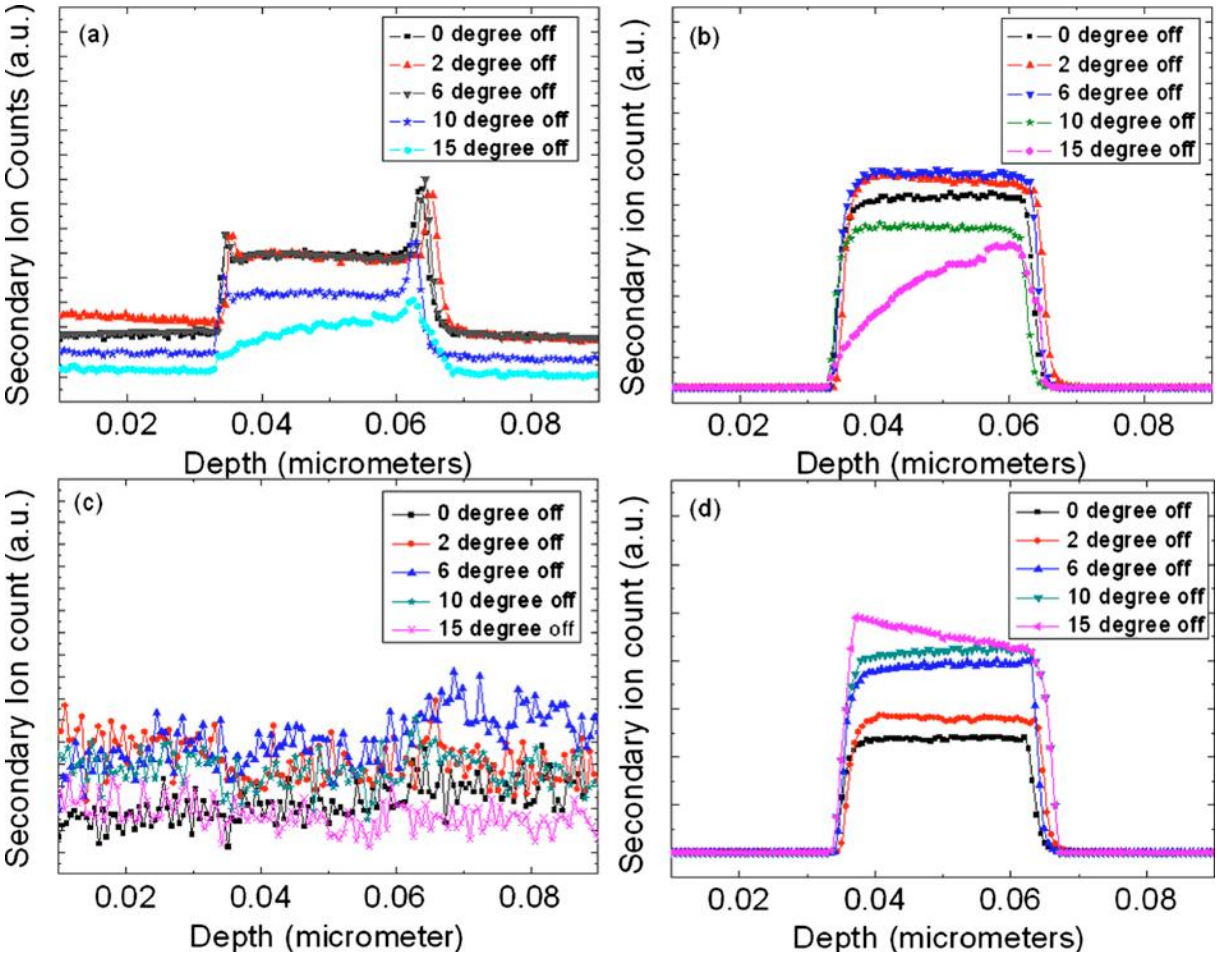

Figure 3-7 Depth profiles of (a) oxygen impurity, (b) aluminum and (c) gallium (d) carbon obtained by SIMS for the GaAs/$Al_{0.3}Ga_{0.7}As$ TDs with different substrate misorientation.

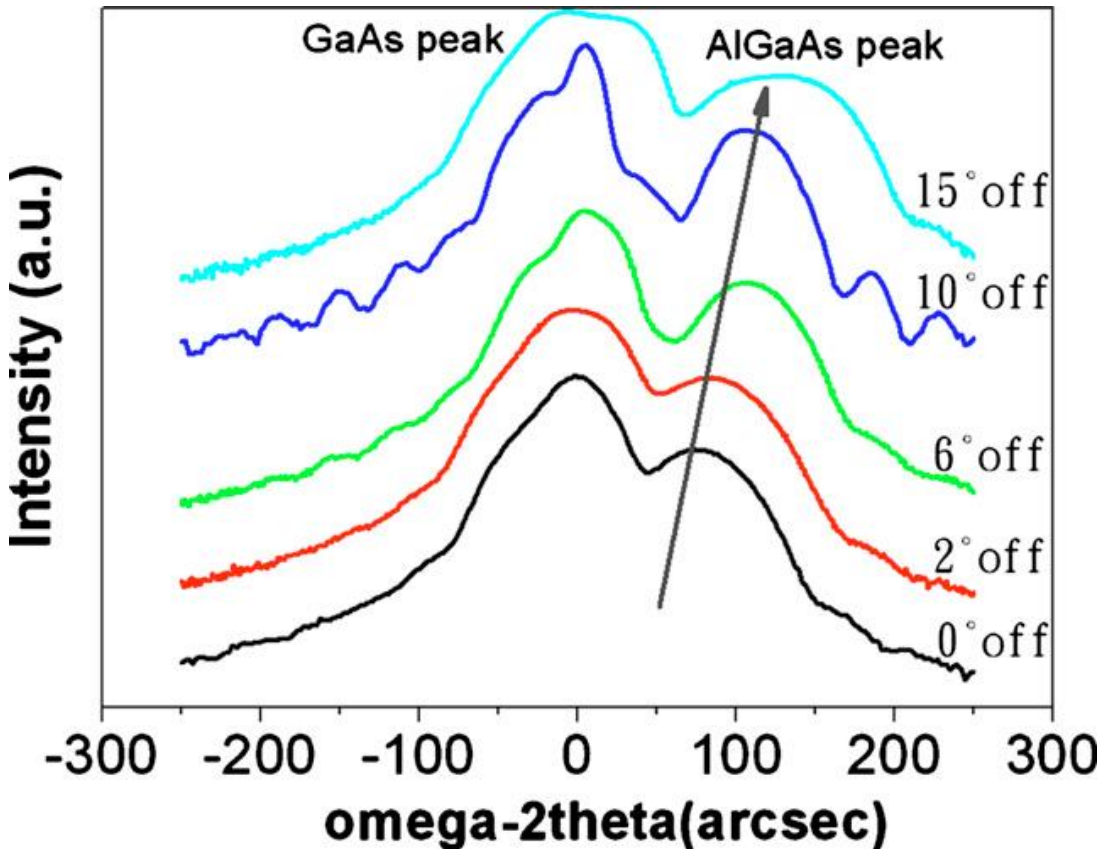

Figure 3-8 HRXRD rocking curves of GaAs/$Al_{0.3}Ga_{0.7}As$ TDs grown on misoriented GaAs substrates.

Chapter 4

An $In_{0.5}Ga_{0.5}P$/GaAs Dual-junction Solar Cell with GaAs/AlGaAs Tunnel Diodes Grown on 10° off Misorientation GaAs Substrates

4.1 Introduction

The InGaP/GaAs lattice-matched system has gained significant attention in recent years for high-efficiency solar cells in both space and terrestrial applications [1,2]. The tandem combination of an optically thin InGaP top cell and a GaAs bottom cell has a theoretical efficiency of 34%. The real conversion efficiency of InGaP/GaAs dual-junction solar cells has been improved to close to 30% in the last decade [3,4]. J. W. Leem et al. [5] reported that the short-circuit current density (J_{sc}) of InGaP/GaAs dual-junction solar cells is strongly dependent on the top and bottom cell thicknesses. As the base thickness of the top InGaP cell in an InGaP/GaAs dual-junction solar cell with GaAs/GaAs tunnel diode (TD) becomes thicker, the J_{sc} is increased for the top cell, whereas the J_{sc} in the bottom cell is decreased, as shown in Fig.4-1. This implies that thicker base thickness for InGaP top cell can enhance light absorption, and thus increase J_{sc} for a InGaP/GaAs dual-junction solar cell. The base thickness of GaAs (bottom) cell is optimized at 2~3μm, allowing the maximized current matching values for both AM1.5G and AM0 illuminations.

Besides, for InGaP/GaAs dual-junction solar cells, the fabrication of effective and stable TD is very important because of its series connection of the top and bottom cells. The design

of the TD structure and the current matching between InGaP top cell and GaAs bottom cell should be optimized through numerical modeling including TD to achieve high conversion efficiency [7]. The conversion efficiency of InGaP/GaAs dual-junction solar cells with different TD structure was also simulated for by J. W. Leem et al. [5]. Figure 4-2 shows the short-circuit current density (J_{sc}) as a function of the base thickness of top InGaP cell in a InGaP/GaAs dual-junction solar cell with InGaP/InGaP TD for the AM1.5G and AM0 solar spectra. With InGaP/InGaP TD, the J_{sc} is increased to 10.7mA/cm^2 for AM1.5G (13.69mA/cm^2 for AM0) as compared with Fig. 4-1. The wideband gap TD, such as InGaP/InGaP homostructure, does not absorb incident light in the long wavelength region compared to GaAs/GaAs TD. Therefore, higher J_{sc} can be achieved in an InGaP/GaAs dual-junction solar cell with higher band-gap TD. This concept is matched with Takamoto et al. [8], they reported that thin and wide band gap TD is necessary for III-V multijunction solar cell to minimize optical absorption and increase tunnel peak current density (J_{tunnel}), as shown in Fig. 4-3.

However, homostructure TD, such as GaAs/GaAs or InGaP/InGaP, is not suitable for III-V multijunction solar cell due to smaller conduction band offset. The detailed reason will be discussed in the following. The basic theory of pn junction tunneling was developed by Keldysh and Kane [9,10] and the tunneling current density can be expressed as follows:

$$J = A\ \exp(-BE_b^{3/2}/E_F)(\bar{E}/2)D = A\ \exp(-BE_b^{1/2}qW)(\bar{E}/2)D \qquad (4.1)$$

where

$$A = \frac{qm^*}{2\pi^2\hbar^3}, \quad B = \frac{\pi(m^*)^{1/2}}{2^{3/2}q\hbar},$$

$$\bar{E} = \frac{2^{5/2}q\hbar E_F}{3\pi(m^*)^{1/2}E_b^{1/2}} = \frac{2^{5/2}\hbar E_b^{1/2}}{3\pi(m^*)^{1/2}W},$$

$$qE_F W = E_b \text{ and } D = \int [F_C(E) - F_V(E)]$$

$$\times[1 - \exp(-2E_S/\bar{E})]dE.$$

In these equations, m^* is the tunneling effective mass, W is the tunneling barrier width, E_F is the electric field in the tunneling region, E_b is the tunneling barrier height (equals Eg for simple case), $F_C(\ )$and $F_V(\ )$ are Fermi–Dirac functions for the conduction and valence bands and E_S=min(E_1 ,E_2) with E_1 and E_2 the energies measured from the band edges. This equation (4.1) implies that tunneling current density can be increased with decrease of electron effective mass, tunneling barrier width and band gap.

Figure 4-4 shows the semiconductor band edges around the junction resulting from such a numerical calculation for a model tunneling junction with a band gap of 1.9 eV both with and without a conduction band edge difference [11]. The tunneling width is about 42% of the classically calculated depletion layer width, as shown in Fig. 4-4. Also it is seen that the tunneling width is reduced when a conduction band offset exists. The AlGaAs/GaAs heterostructure itself possesses larger energy-band difference in the conduction band than the GaAs/InGaP heterostructure [12] which can effectively reduce tunneling width and increase

tunneling current. This implies that heterostructure TD, such as AlGaAs/GaAs, with higher conduction band offset is necessary for development of high-efficiency III-V multijunction solar cells.

As III-V solar cell devices have to be operated at higher concentration ratios, TD is also a very important component. If, at higher concentrations, the peak current density (J_{peak}) in the TD is lower than the short-circuit current density (J_{sc}), the overall performance of the III-V solar cell is dramatically affected. Currently, for III-V multijunction solar cells, wide band-gap materials with a low electrical resistivity, such as AlGaAs and InGaP, are adopted as TD materials because of lower optical absorption. In fact, the increase in the band gap of TD materials made from III-V semiconductors results in a decrease in the tunneling current density, as shown in Fig. 4-3. This implies that the reduction of impurities in TDs, such as oxygen atoms that act as a nonradiative trap, plays the dominant role when higher band gap materials are used.

AlGaAs epitaxy is also potentially of great importance for many high-speed electronic and optoelectronic devices [13,14], because the difference in the lattice parameter between GaAs and AlGaAs is very small, and this avoids the generation of undesirable interface states. However, AlGaAs epitaxy as a TD material is known that to have serious oxygen problem as compared with InGaP epitaxy for III-V multijunction solar cells. The InGaP TDs show a lower interface recombination rate than AlGaAs TDs when electrons move away from the

TDs interface. In chapter 3, we proved that the 10° off misorientation GaAs substrates not only reduce the oxygen-impurity content in N^{++}-GaAs/P^{++}-AlGaAs TD, but also produce high quality TD with smooth surface and sharp interface [15]. Although the 10° off misorientation GaAs substrate has been found efficiently reduce nonradiative traps in N^{++}-GaAs/P^{++}-AlGaAs TD, a dual-junction solar cell grown on 10° off misorientation GaAs substrates using a N^{++}-GaAs/P^{++}-AlGaAs TD has not yet been reported.

4.2 Experiment

In this part, we report the comparative results of InGaP/GaAs dual-junction solar cells with a N^{++}-InGaP/P^{++}-GaAs TD (sample A) and with a N^{++}-GaAs/P^{++}-AlGaAs TD (sample B), both grown on 10° off misorientation GaAs substrates, and also of a N^{++}-InGaP/P^{++}-GaAs TD grown on 6° off misorientation GaAs substrates (sample C), which have been grown using a metal organic chemical vapor deposition (MOCVD, EMCORE D180) system. Trimethylgallium (TMG), trimethylaluminum (TMAl) and trimethylindium (TMIn) were used as group III sources, whereas arsine (AsH_3) and phosphine (PH_3) were used as group V sources. The precursors for p-type and n-type dopants were carbon-tetrabromide (CBr_4) and dimethyl-telluride (DMTe), respectively. For GaAs/AlGaAs TDs, AlGaAs epi-layers may be easily accomplished higher doping levels with carbon doping compared to GaAs. The GaAs epitaxy used for the n-type side in the TDs was found to have lower optical absorption

because of generation of Burstein-Moss shift[4]. The band gap of the n-type GaAs in the TDs is slightly increased with increase of doping concentration, resulting in more light passing through to the GaAs cell. For an InGaP/GaAs TD, carbon-doped InGaP was not used in this study because carbon is very difficult to embed in InP-based materials by MOCVD. All films in this study were grown at low-pressure of 40 torr with hydrogen flow rate of 28000sccm.

4.3 Results and discussion

Figure 4-5 shows the cross-section of the InGaP/GaAs dual-junction solar cell with different TD materials. The framed GaAs bottom cell consists of a 0.1 μm InGaP back surface field (BSF) layer, a 3μm GaAs base layer, a 0.1μm GaAs emitter layer, and a 0.05 μm InGaP window layer. The InGaP top cell consists of a 0.03 μm AlInP BSF layer, a 0.5 μm InGaP base layer, a 0.05 μm InGaP emitter layer, and a 0.03 μm AlInP window layer. A Ni(6 nm)/Ge(50 nm)/Au(100 nm)/Ni(45 nm)/Au(250 nm) was used as the front contact, whereas a Ti(50 nm)/Pt(60 nm)/Au(250 nm) was used as the back contact in this study. The antireflection coating is a single layer of Si_3N_4 with a thickness of 75 nm.

Figure 4-6 shows the current-voltage (I-V) characteristics of the InGaP/GaAs dual-junction solar cells with P^{++}-GaAs/N^{++}-InGaP (sample A), and P^{++}-AlGaAs/N^{++}-GaAs TDs (sample B) grown on 10° off GaAs substrate and with P^{++}-GaAs/N^{++}-InGaP TD grown on 6° off GaAs substrate (sample C), respectively. The 6° off GaAs substrates were often used

as substrates for III-V solar cell applications [16-18], which makes it easy to transfer the growth parameters to Ge substrates. Therefore, it is suitable as a standard reference for the dual-junction solar cell grown on misorientation GaAs substrates in this study. Table 4.1 shows the performance relationship of samples A, B and C measured at one sun, including open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), Fill factor (FF) and conversion efficiency (Eff.). According to the experimental results, J_{sc} of sample A is smaller than that of samples B and C. J_{sc} generated by a III-V multijunction solar cell is dependent on the incident light and can be simulated using the following equation [19]:

$$J_{sc} = \int_0^{\infty} \eta_c(E)\big(1 - R(E)\big)a(E)b_s(E)dE \tag{4.2}$$

where $\eta_c(E)$ is the probability of electrons collected under illumination; R(E) is the probability of photon reflection; a(E) is the probability of absorption of a photon of energy E; and $b_s(E)$ is the incident spectral photon flux density. Equation (4.2) shows that poor quantum efficiency (QE) may lead to a reduction of J_{sc} for a solar cell device operated under illumination. The QE depends upon the cell design and the epitaxial quality. The external quantum efficiency (EQE) of sample A is lower than that of samples B and C, as shown in Fig. 4.7, implying that the epitaxial quality of sample A has deteriorated.

In order to define the reason for the degeneration of the epitaxial quality of sample A, photoluminescence (PL) using a 532 nm laser source was employed to identify the band gap and epitaxial quality. We found that the band gap of the InGaP cell of sample A is 1.92eV,

which is larger than samples B and C (both 1.84~1.85eV). It is suggested that a transition of ordering/disordering InGaP epitaxy may occur in sample A when the higher substrate misorientation angle (10° off) was adopted [20,21]. The poor epitaxial quality of sample A is attributed to crystal defects associated with disordered structures in the matrix, which further decreases QE and J_{sc} of III-V solar cells devices. Experiments also confirmed that InGaP/GaAs dual-junction solar cells with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10° off GaAs substrate (sample B) does not generate disordering InGaP epitaxy during material growth, and thus acquires superior I-V characteristics. Besides, the slope of sample A is lower than that of samples B and C, as shown in Fig. 4-6, suggesting that the series resistance (Rs) for sample A is higher than for the others. Higher series resistance also leads to a low FF and J_{sc} for III-V solar cells devices.

The dependence of the characteristics of the dual-junction solar cell grown on 10° off GaAs substrate, on the different TD materials, such as P^{++}-GaAs/N^{++}-InGaP and P^{++}-AlGaAs/N^{++}-GaAs, has been compared using the spectral responses of the EQE of the dual-junction solar cells, as shown in Fig. 4.7. The spectral response of the dual junction with the P^{++}-GaAs/N^{++}-InGaP TD grown on 6° off GaAs substrate is also shown in Fig. 4.7. Non-square shape in the spectral responses of the InGaP top cell has been observed owing to higher reflection losses (10~50%) in the range of 300 to 500nm. According to the experimental results, we found that the total EQE of the dual-junction solar cells with the

P^{++}-AlGaAs/N^{++}-GaAs TD (sample B) is higher than that of the P^{++}-GaAs/N^{++}-InGaP TD (sample A) at the same misorientation angle (10° off). The maximum EQE of sample B is 82% for the InGaP top cell and 85% for the GaAs bottom cell. An increase in the EQE of the GaAs bottom cell of sample B has been confirmed, and this is due to the lower absorption losses in the P^{++}-AlGaAs/N^{++}-GaAs TD as compared to sample A. On the other hand, sample B obviously exhibits an improvement in total EQE compared to the traditional dual junction with a P^{++}-GaAs/N^{++}-InGaP TD grown on 6° off GaAs substrate (sample C), suggesting that 10° off misorientation GaAs substrates not only reduce the content of contamination in N^{++}-GaAs/P^{++}-AlGaAs TDs but also produce high light-trapping and carrier-collection efficiencies when solar light was injected into solar cell devices.

To further understand the difference in the I-V characteristics at higher concentration ratios, samples B and C were also operated under average solar concentrations of around 185× and the results are shown in Fig. 4-8. Experiments confirmed that the Fill Factor (FF) and conversion efficiency of samples B and C both decrease at higher concentration ratios because of larger series resistances (Rs). The thickness of the front contact used in this study is too thin (~450nm), which results in larger Rs when solar cell devices are operated at higher concentration ratios. Only one operating point A in Fig. 4-8 is found in the I-V curve of sample C, implying that the Rs value is lower than the negative differential resistivity [22,23] even if the thickness of the front contact is not sufficient. For III-V multijunction solar cells,

lower Rs value relative to the negative differential resistivity of the tunnel diode is necessary. On the other hand, a sharp current drop occurs at lower voltage of 2.1 V for sample C, and no dip in the I-V characteristic exists for sample B. These results indicate that, at higher concentration ratios (185×), the P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10° off GaAs substrate generates higher peak current density (J_{peak}) than that of the P^{++}-GaAs/N^{++}-InGaP TD grown on 6° off GaAs substrate.

When the tunneling current density of a TD (J_{peak}) in III-V multijunction solar cell is lower than the short-circuit current density of the cell (J_{sc}) at higher concentration ratios, the probability of an electron tunneling from occupied states to unoccupied states on the hole side is decreased, and a current drop occurs at lower voltage. The AlGaAs/GaAs heterostructure itself possesses larger energy-band difference in the conduction band than the GaAs/InGaP heterostructure [24,25], which can effectively increase the tunneling current of a TD by reducing the tunneling barrier and tunneling width when III-V solar cell devices are operated at higher concentration ratios.

4.4 Summary

In summary, we have demonstrated that, compared to cell design with a P^{++}-GaAs/N^{++}-InGaP TD (sample A), InGaP/GaAs dual junction solar cells with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10°off GaAs substrates (sample B) exhibit superior

photovoltaic conversion efficiency (~20%) when operated at one sun. According to the experimental results, InGaP/GaAs dual-junction solar cell with a P^{++}-GaAs/N^{++}-InGaP TD grown on 10°off GaAs substrate may generate disordering structures, which decrease QE and J_{sc} of III-V solar cells devices, during material growth. Besides, higher Rs for sample A also imply the degeneration of FF and J_{sc} of III-V solar cells devices as shown in Fig. 4-6. Moreover, InGaP/GaAs dual-junction solar cell with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10° off misorientation GaAs substrates produces higher EQE (~82% for InGaP top cell and 85% for GaAs bottom cell) as compared to the P^{++}-GaAs/N^{++}-InGaP TD as shown in Fig.4-7 . Furthermore, when these solar cell devices were operated at higher concentration ratios, they displayed superior I-V characteristics compared to the traditional dual-junction solar cell grown on 6° off misorientation GaAs substrates, as shown in Fig. 4-8. These results suggest that 10° off misorientation GaAs substrates for cell design with a P^{++}-AlGaAs/N^{++}-GaAs TD not only produce high light-trapping and carrier-collection efficiencies but also generate higher peak current density (J_{peak}) at higher concentration ratios (185×) than that of a P^{++}-GaAs/N^{++}-InGaP TD grown on 6° off GaAs substrate, even if the thickness of ohmic contact in this study is not sufficient.

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Table 4-1 I-V characteristics of the InGaP/GaAs dual-junction solar cells with different tunnel diodes grown on misoriented GaAs substrates

Tunnel junction	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)
Sample A (10° off)	2.07	10.5	72.0	15.78
Sample B (10° off)	2.03	11.9	79.8	19.24
Sample C (6° off)	2.04	12.1	79.2	19.55

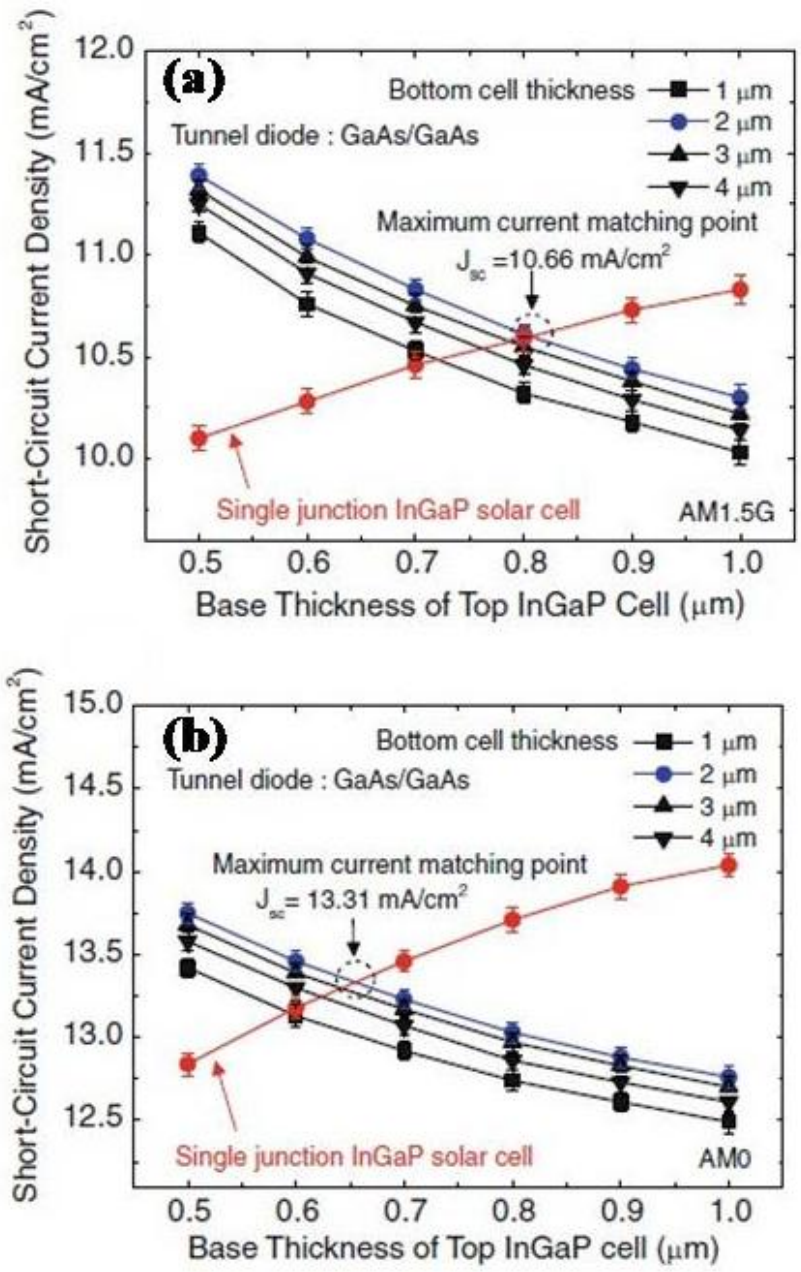

Figure 4-1 Short-circuit current density (J_{sc}) as a function of the base thickness of top InGaP cell in a InGaP/GaAs dual-junction solar cell with GaAs/GaAs tunnel diode for AM1.5G (a) and AM0 (b) solar spectra. [5]

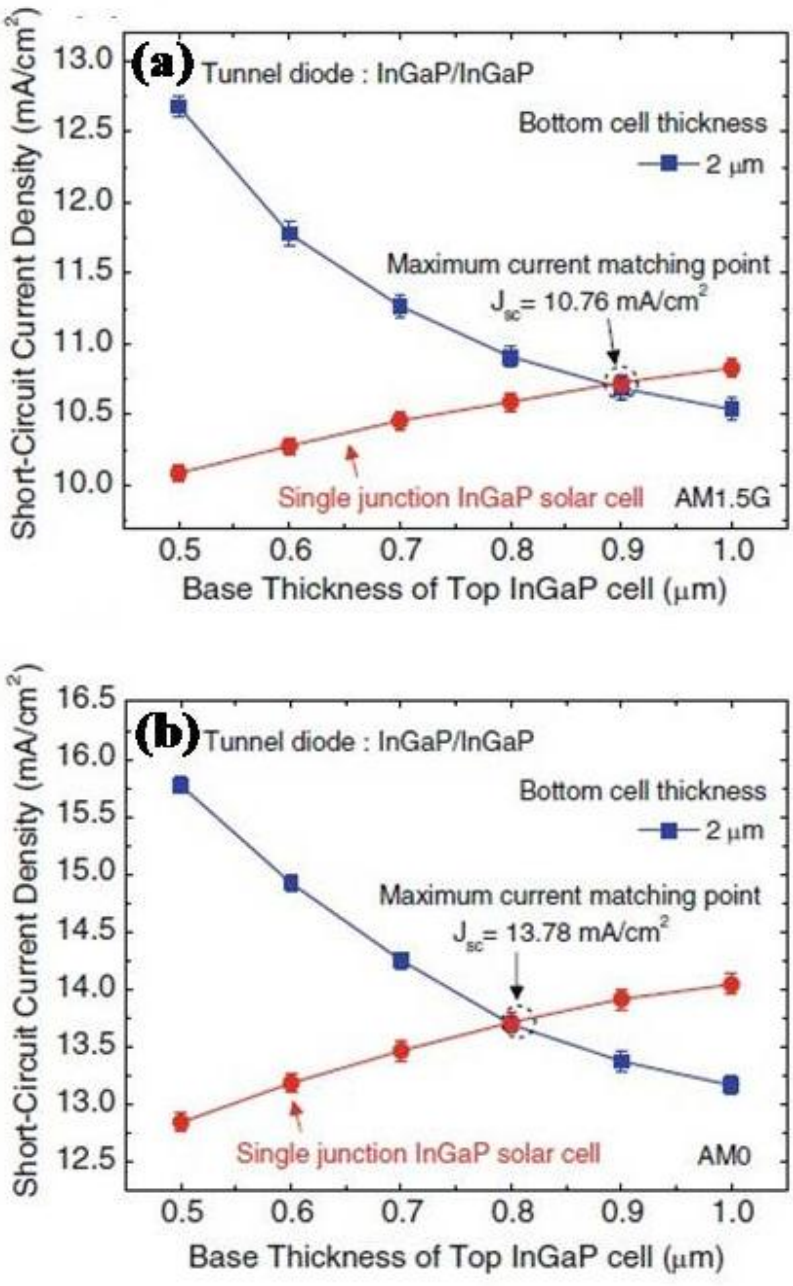

Figure 4-2 Short-circuit current density as a function of the base thickness of top InGaP cell in a monolithic InGaP/GaAs DJ solar cell with InGaP/InGaP tunnel diode for AM1.5G (a) and AM0 (b) solar spectra. [5]

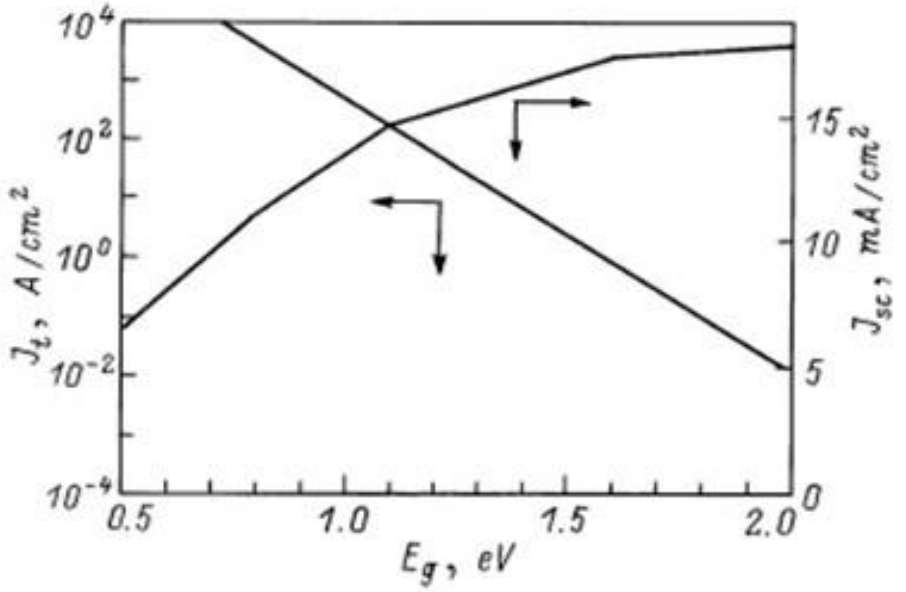

Figure 4-3 Calculated tunnel peak current density (J_{tunnel}) and short-circuit current density of GaAs bottom cell (J_{sc}) as a function of bandgap energy (E_g) of the tunnel junction [8]

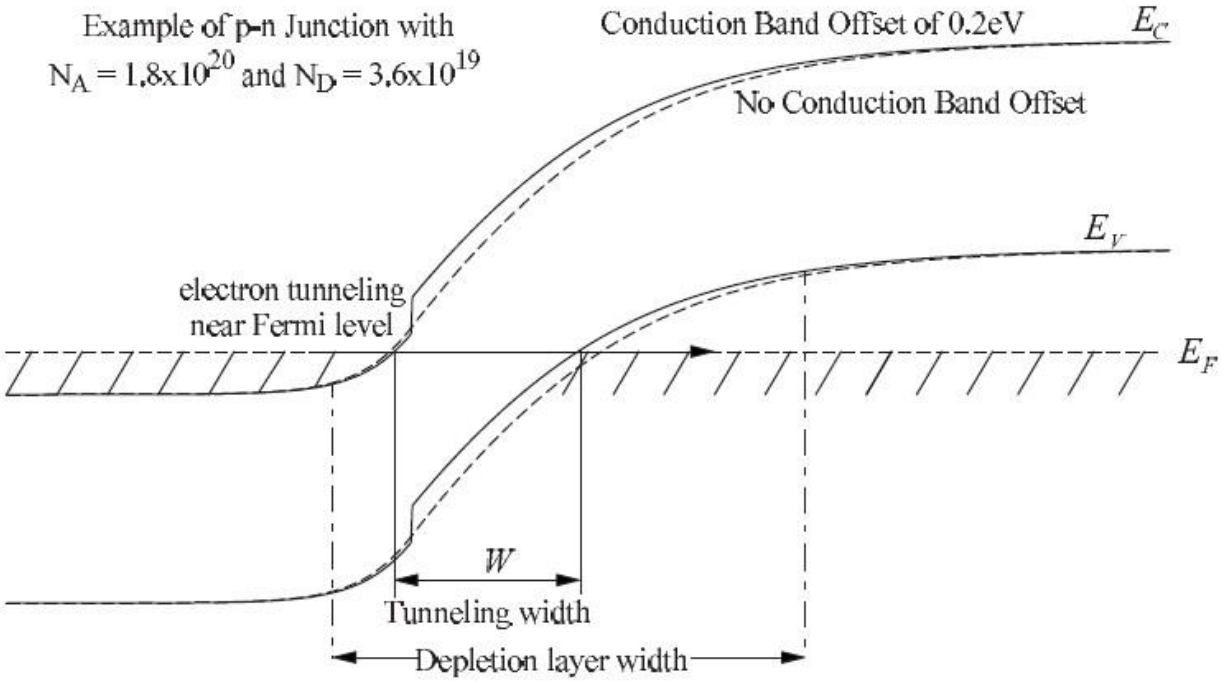

Figure 4-4 Example of junction tunneling width and depletion layer width [11]

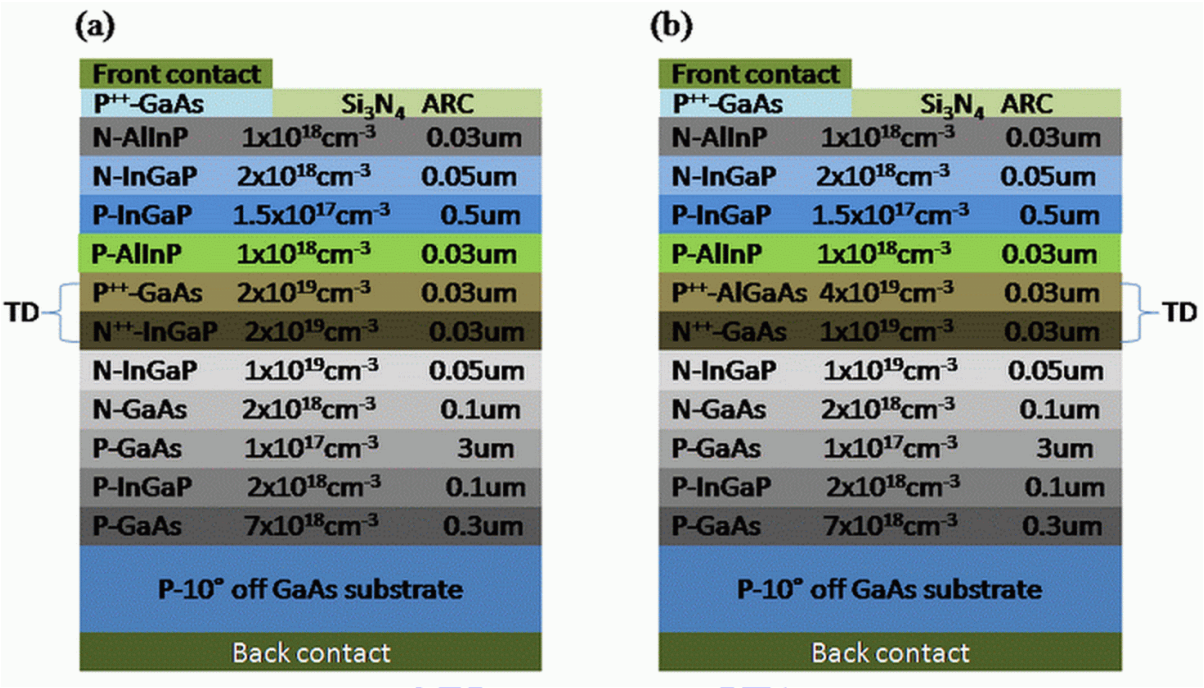

Figure 4-5 A cross-section of InGaP/GaAs dual-junction solar cell with different tunnel diode materials: (a) the cell design with P^{++}-GaAs/N^{++}-InGaP, (b) the cell design with P^{++}-AlGaAs/N^{++}-GaAs.

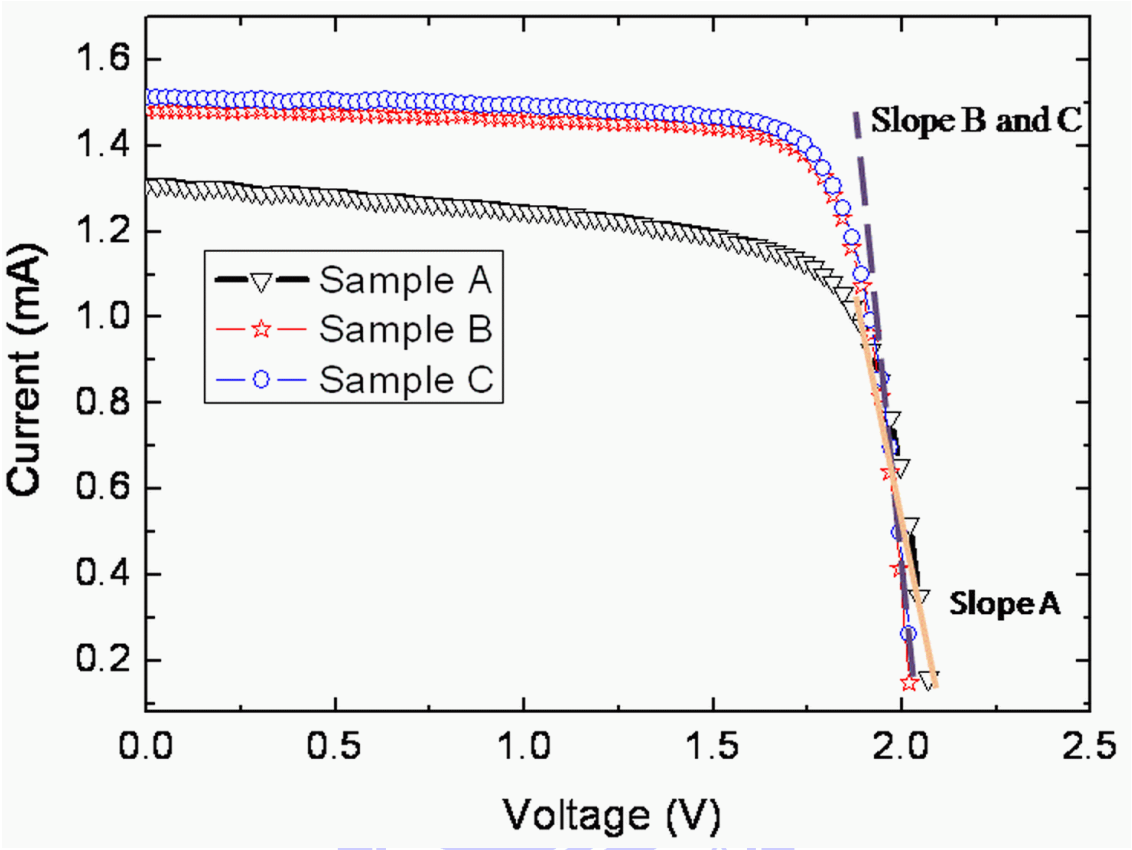

Figure 4-6 The current-voltage (I-V) characteristics of InGaP/GaAs dual-junction solar cells measured at one sun. Sample A: the cell design with a P^{++}-GaAs/N^{++}-InGaP tunnel diode (TD) grown on 10° off misorientation GaAs substrates; sample B: the cell design with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10° off misorientation GaAs substrates; sample C: the cell design with a P^{++}-GaAs/N^{++}-InGaP TD grown on 6° off misorientation GaAs substrates.

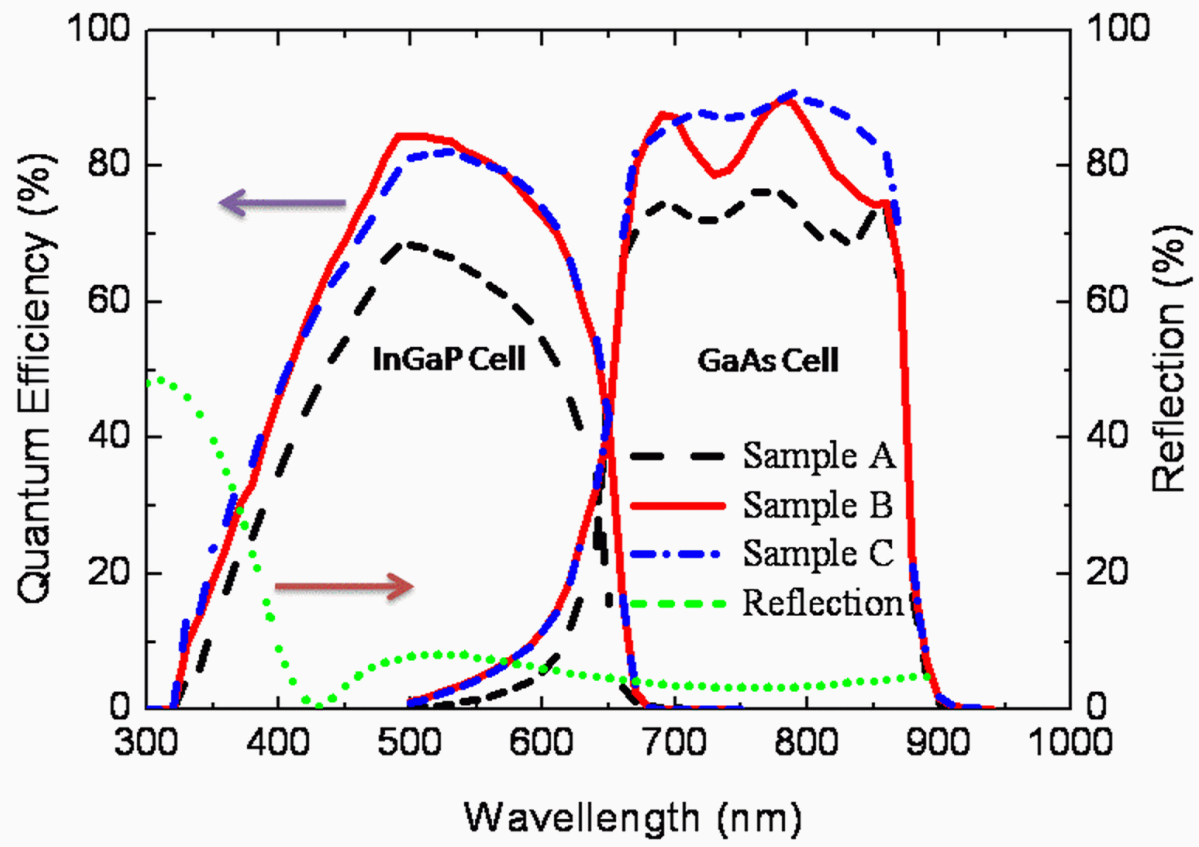

Figure 4-7 External quantum efficiency (EQE) of InGaP/GaAs dual-junction solar cells. Sample A: the cell design with a P^{++}-GaAs/N^{++}-InGaP tunnel diode (TD) grown on 10° off misorientation GaAs substrates; sample B: the cell design with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10° off misorientation GaAs substrates; sample C: the cell design with a P^{++}-GaAs/N^{++}-InGaP TD grown on 6° off misorientation GaAs substrates

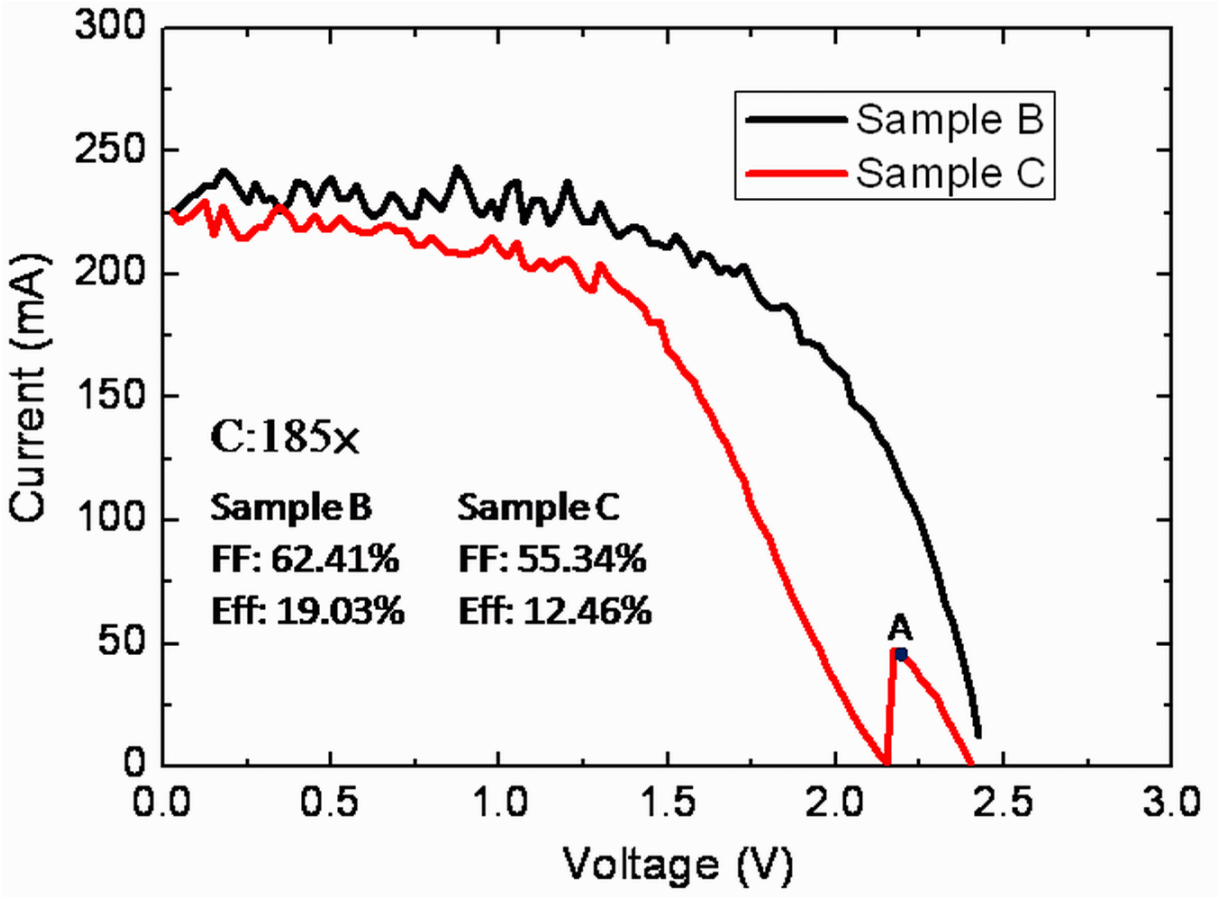

Figure 4-8 The current-voltage (I-V) characteristics of InGaP/GaAs dual-junction solar cells operated at higher concentration ratios (185×). Sample A: the cell design with a P^{++}-GaAs/N^{++}-InGaP tunnel diode (TD) grown on 10° off misorientation GaAs substrates; sample B: the cell design with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10° off misorientation GaAs substrates; sample C: the cell design with a P^{++}-GaAs/N^{++}-InGaP TD grown on 6° off misorientation GaAs substrates.

Chapter 5

Growth of GaAs epitaxy on Ge/Si substrates using graded-temperature arsenic prelayer

5.1 Material characteristics of GaAs on Ge/Si substrate

The integration of the GaAs/Ge/SiGe heterostructure on Si substrates as an alternative template for low cost and high conversion efficiency III-V based solar cells has attracted much attention [1,2]. However, many growth challenges exist in the GaAs/Ge heterostructure, including anti-phase domains (APDs), misfit dislocations, and the interdiffusion of the Ga, As, and Ge atoms. The lattice constant and thermal coefficient between GaAs and Ge epitaxy is very small as shown in Table. 5-1. Therefore, the effect of lattice mismatch and thermal expansion coefficient on the growth of GaAs on Ge/Si substrate can be neglected in this study.

5.1.1 Anti-phase domains (APDs) formation

Anti-phase domain (APD) is the region of a crystal where the atomic arrangements are of the opposite to that of perfect lattice system. Generally APDs form anti-phase boundary (APB) with the parent lattice as shown in Fig. 5-1. The shaded region B is the example of an APD. In this figure, GaAs is grown on misoriented Ge (or Si) substrate. The misorientation causes the growth of APD of region B. As seen, due to the APD, the Ga sites 1, 1', 2, 2', 3, 3' are bonded

to another anti-site Ga forming the APB which affects the epitaxial quality and surface morphology of GaAs/Ge/Si heterostructure. APD formation in the GaAs/Ge heterostructure can be suppressed by adjusting growth conditions such as the growth temperature, the substrate misorientation angles, and the Ge film annealing process [3-5]. The abovementioned methods will help us to optimize the growth parameters for GaAs/Ge/Si heterostructure growth.

5.1.1.1 Effect of growth temperature on APDs formation

As shown in Fig. 5-2, the GaAs crystal is composed of two sublattices, each face centered cubic (FCC) and offset with respect to each other by half the diagonal of the FCC cube. This crystal configuration is known as cubic sphalerite or zinc blende. The two possible sublattice locations of the GaAs epitaxy on Ge are shown in Fig. 5-3. The “GaAs-A” domain corresponds to the first atomic layer on the Ge surface is arsenic (As), while “GaAs-B” means that the first atomic layer on the Ge substrate surface is gallium (Ga). The different between GaAs-A and GaAs-B is the arrangement of their polar [111] axes, that is, a reversal of the location of the As and Ga atoms in sublattices. At a growth temperature that is closer to the interface between GaAs-A and GaAs-B as shown in Fig. 5-4, larger APDs will be formed during the GaAs/Ge heterostructure growth. The transformation of APD-free to APDs to APD-free with increment of growth temperature has been reported [6]. According to the

experimental results by M. K. Hudait et al. [7], half maximum (FWHM) of GaAs peak of GaAs/Ge heterostructure can be reduced from 50.8 arcsec to 45.5 arcsec when growth temperature is increased from 600℃ to 650℃. The narrowness of the FWHM of GaAs epitaxial film indicates the microstructure quality of the film is improved. The influence of the growth temperature on the surface morphology of GaAs/Ge heterostructure can be seen in Fig. 5-5. The two-dimensional (2D) and three-dimensional (3D) AFM topographical images of 3μm×3μm scanning sizes are shown in Fig. 5-5 as a function of growth temperature at 650℃ and 750℃, respectively. It can be observed that a much smoother surface is achieved for the sample grown at higher growth temperature. According to the references in [4,6,7], we know that growth temperature is very important issue for GaAs/Ge heterostructure using Metalorganic Chemical Vapor Deposition (MOCVD). More APDs will be generated at the interface between GaAs and Ge epitaxy when inappropriate growth temperature was adopted.

5.1.1.2 Effect of misoriented substrate on APDs formation

Both two orientations (GaAs-A and GaAs-B) of GaAs epitaxy are nucleated on Ge substrate, distinct domains of each sunlattice, separated by anti-phase boundaries (APBs) may propagate well into the GaAs epitaxy. In order to suppress APDs formation the control of the substrate surface is also an efficient way. The surface of non-polar semiconductor materials such Ge and Si is characterized by dimer reconstructed terraces separated by step [9-11].

Pairing, or dimerization, of adjacent fourfold coordinated Ge atoms exposed on the (100) surface which reduces the number of dangling bonds per atom from two to one. The physical equation describes the relationship of steps density variation as a function of misorientation angles as shown in equation (5-1):

$$\omega = h \tan^{-1}\varphi \qquad (5\text{-}1)$$

Where the ω is the density of steps on the surface; h is the height of the step; φ is the misorientation angles. Equation (5-1) shows that higher misorientation angles may promote the generation of steps on the surface to reduce APDs formation. Fig. 5-6 displays TEM images of GaAs grown on Ge substrate with different misorientation angles (6° and 0°). It is observed clearly GaAs grown on 6° off Ge substrate do not have APDs generation around the GaAs/Ge interface; on the contrary, the penetration of APDs from Ge layer to GaAs is also observed when 0° off Ge substrate was adopted [5]. L. Lazzarini et al. [12] also verified that lower misorientation angles (≦4°off) may result in APDs formation during GaAs/Ge heterostructure growth.

The model [13] is used to explain the reversal of the sublattice locations between GaAs grown on (100) Ge off toward (111) substrates with small and larger misoriented angles as shown in Fig. 5-7. This model assumes:

(a) The initially nucleated GaAs at surface steps are of the type GaAs-A in their sublattice location.

(b) The nuclei formed on the surface, GaAs-B, have the reversed sublattice location.

For Ge substrate with a larger misorientation angle, of which the surface between the steps are very narrow, the steps are so close that no nucleus can be formed on the surface, as shown in Fig. 5-7(a). The nuclei at the steps can coalesce soon. Overgrowth on such surface may result single domain GaAs with the sublattice orientation being the same as the initially nucleated one, the GaAs-A, and a smooth surface is obtained, as shown in Fig. 5-7(b). For Ge substrate with a small misorientation angle of which the width of the terraces between the steps is larger than that of lager disorientation angle, nuclei formed on the terraces will dominate, as shown in Fig. 5-7(c). The nuclei at the steps will be surrounded by the nuclei on the terrace so that they are not able to connect with each other. Overgrowth on such surface may have the result that initially nucleated GaAs at the steps may become less dominant during further growth and at last will annihilate, as shown in Fig. 5-7(d). According to the growth mechanism mentioned above, the suppression of APDs formation can be achieve using Ge substrate with higher misorientation angles (≧4°off)) during GaAs/Ge heterostructure growth.

5.1.1.3 Effect of high-temperature substrate annealing on APDs formation

High-temperature substrate annealing process carried out prior GaAs epitaxial growth is also another efficient way to suppress APDs formation during GaAs/Ge heterostructure

growth. This way is related to the transformation of steps states on the Ge surface being similar to the mechanism of misoriented substrates. The difference in surface steps generation between substrate annealing and misoriented substrates is growth-temperature gradient. The step numbers of misoriented Ge surface is stable than substrate annealing technique because we can choose Ge substrate with higher misorientation angles before GaAs/Ge heterostructure growth. If you want to change the configuration of surface steps existed originally on misoriented Ge surface to suppress APDs formation, the substrate annealing process is a good choice. The detailed description of high-temperature substrate annealing will be discussed in the following.

The purpose for high-temperature substrate annealing process can be separated into two parts: (a) it can remove native oxide on the Ge surface before the growth. (b) it can transform the single-step configuration into desired double-step surface state on the Ge substrates. The Ge substrate without substrate annealing may result in APDs formation near the interface of GaAs/Ge heterostructure as shown in Fig. 5-8(a) [14]. On the contrary, no APDs formation is achieved for GaAs epitaxy grown on Ge substrate annealed at 640℃ as shown in Fig. 5-8(b). Here, we know that annealing temperature is key point for substrate annealing process. High temperature annealing induces a favorable surface transition equivalent to the use of misoriented Ge substrates.

The transformation of surface steps for substrate annealing process, illustrated in Fig. 5-9,

along [110] directions lead to reflection of Ge surface from the original (100) orientation. A single atomic-layer steps, shown in Fig. 5-9(a), feature single or any odd-integer number of steps, such that on alternating terraces, the exposed sublattice domain shifts, rotating the dimer bond by 90°. For S_A ("S" is single-layer steps) steps the dimerization axis on the upper terrace is perpendicular to the step edge, whereas S_B steps means that the dimerization axis on the upper terrace is parallel to step edge. As shown in Fig. 5-9(b), this configuration consist of double atomic-layer steps (D_A and D_B: D is double-layer steps), or even-number layer steps, separating terraces of the same exposed sublattice where all dimmers lie parallel to the step edges. In this case, the configuration of D_B steps is favorable than D_A steps owing to the different in energy as shown in Table 5-2 [15]. On the other hand, the step formation energy of D_B is also lower than that of $S_A + S_B$. It means that high-temperature substrate annealing may transfer single-layer steps into double-layer steps [16].

In general, the abovementioned methods induce atomic surface steps on the Gesubstrate. The formation of surface steps can boost the single-domain GaAs-A growth, in which the first atomic layer on the surface of Ge layer is arsenic (As) atoms, and promote the self-annihilation of APDs during GaAs/Ge heterostructure growth. Besides, Luo et al. [5] also pointed out that anti-phase boundaries (APBs) in the GaAs/Ge heterostructure were the routes for Ge diffusion into the GaAs layer. They demonstrated that termination of APD formation led to reduction in the interdiffusion in the GaAs/Ge heterostructure.

5.1.2 Interdiffusion between GaAs and Ge epitaxy

The optimal growth temperature for GaAs epitaxial growth using MOCVD is about 650℃, whereas the growth temperature for Ge epitaxy is about 400℃ [17]. The different in optimal growth temperature between GaAs and Ge epitaxy is a stern challenge during GaAs/Ge heterostructure growth. The atoms of Ga and As in GaAs epitaxy will diffuse into Ge layer which forms unwanted P-N junction in Ge epitaxy. Moreover, Ge atoms in Ge layer also diffuse into GaAs layer which forms N-type layer in GaAs epitaxy due to the use of higher growth temperature. The unwanted P-N junction in subcells of III-V multijunction solar cells will seriously cause a short circuit and affect the conversion efficiency. In order to decrease the interdiffusion probability of As and Ge atoms, a low-temperature epitaxial technique and various interfacial layers such as AlAs, Ga, and As [18,19] were used for the GaAs/Ge heterostructure growth.

5.1.2.1 Low-temperature epitaxial technique

The diffusion mechanism of GaAs/Ge heterostructure is well described by Arrhenius equation [20] as shown in equation (5-2).

$$D=D_0 \exp(-E_a/k_BT) \quad (5\text{-}2)$$

Where D_0 is pre-exponential factor, E_a is activation energy, k_B is Boltzmann's constant and T is the absolute growth temperature. The equation shows the diffusion probability

exponentially dependents on growth temperature and thus the use of lower growth temperature can efficiently decrease the interdiffusion probability of Ga, As and Ge atoms during GaAs/Ge heterostructure growth. The diffusion length of As atoms is deeper than Ga atoms for high-temperature GaAs growth [21] as shown in Fig. 5-10 and therefore the suppression of As interdiffusion from GaAs to Ge layer is main challenge than that of Ga and Ge atoms. The concentration of excess As in a GaAs epitaxy grown at the low substrate temperature by Molecular-beam Epitaxy (MBE) is extremely large in comparison with those in the equilibrium phase diagram where the concentration of excess As is only 0.1% at the melting point [22]. However, the low-temperature growth of GaAs on the Ge layer led to the formation of GaAs-B domain, which generated APDs in the GaAs layer, and As-antisite defects on the terraces [4,23]. In this thesis we have to further consider the growth temperature related to the APDs formation and interdiffusion problems during GaAs/Ge heterostructure.

5.1.2.2 The insertion of As, Ga, and AlAs prelayers between GaAs and Ge layers

It is known that the interdiffusion occurs easily at GaAs-Ge heterointerface. To avoid the interdiffusion of As, Ga, Ge atoms during GaAs/Ge heterostructure growth, an alternative to growth of GaAs on Ge layers is to use a prelayer, which creates a near-GaAs lattice constant but has few defects. Recently many materials such as AlAs, Ga and As were used as prelayers

[18,19,24,25]. An AlAs prelayer grown on Ge substrate prior GaAs epitaxy can suppress the interdiffusion because of high bonding energy. If unwanted interdiffusion occurs during GaAs/Ge heterostructure, the atomic bonds in GaAs epitaxy must be broken and then diffused into Ge substrate. The bonding energy of Al-As in the AlAs prelayer is higher than that of Ga-As. Thus, the AlAs prelayer suppresses efficiently the interdiffusion of Ge atoms as shown in Fig. 5-11. On the other hand, Ga and As prelayers are also the candidate for suppressing interdiffusion during GaAs/Ge heterostructure growth. According to the experimental results by B. Galiana et al. [19], the initiation of GaAs with the typical procedure of using a Ga prelayer decreases the As diffusion into Ge substrate as well as the Ge diffusion into the GaAs epitaxy and results in improved solar cell characteristics.

Although a thin AlAs prelayer grown between GaAs and Ge epitaxy suppressed the interdiffusion of Ge atoms, diffusion of Al atoms into the GaAs epitaxy was observed at higher growth temperatures (>540℃) [18]. In contrast, the growth of the Ga prelayer between Ge and GaAs epitaxy decreased the As and Ge interdiffusion as compared to the growth of As prelayer [19], but the APD formation in GaAs/Ge system was difficult to avoid. Since Ga prelayer tends to aggregate easily, As prelayer is preferred to manage uniform coverage on the Ge surface. Therefore, controlling the growth temperature and As flux is a very important concept to realize single-phase GaAs growth. However, arsenic atoms tend to interact with Si or Ge surfaces and change surface reconstructions to reduce the number of dangling bonds

[26,27].Several researchers have reported As–As dimers form on the Si surface [27-29].Some of these results are, however, contradictory in defining which growth condition produces different orientations of As dimers (perpendicular or parallel to the step edges) on vicinal Si surfaces. Bringans et al. [26] described that As dimers could be added to a Si surface with an orientation that was perpendicular to step edges for substrate temperature in the range 400–600 ℃, and the surface had predominantly double-layer steps.

5.2 Experiment

In this part we present the use of an As prelayer grown using graded-temperature technique for the suppression of APD formation. This layer is also found to improve the surface morphology and reduce the interdiffusion during the GaAs/Ge/Si heterostructure growth. All samples in this study were grown by low-pressure metal organic chemical vapor deposition (MOCVD, EMCORE D180) using trimethylgallium (TMG) and arsine (AsH_3) as the source materials. The substrates used were the Ge epitaxy on Si (001) substrate with 4° off misorientation toward the [110] direction. A detailed description of the growth of Ge epitaxy on Si substrate can be found elsewhere [30]. The As prelayer was deposited onto the Ge epitaxy while the substrate temperature was ramped from 300 to 420℃. Then, GaAs layers with different V/III ratios (11~75) were grown on the As/Ge/Si heterostructure by a low-temperature epitaxial technique (450℃). The Ge/Si substrate was annealed at 650 ℃ to

generate atomic surface steps before the GaAs/As epitaxial growth [3]. All parameters in this study are shown in Fig. 5-12. The surface morphology of the GaAs/Ge/Si heterostructure with graded-temperature As prelayer was examined using atomic force microscopy (AFM). The threading dislocation density and crystalline quality of the grown sample was estimated using transmission electron microscopy (TEM) and high resolution X-ray diffraction (HRXRD), respectively. Finally, the interdiffusion of Ga, Ge and As atoms in the samples was determined by secondary ion mass spectrometry (SIMS).

5.3 Results and discussion

In this part, all of samples were predeposited on the Ge/Si substrate using graded-temperature As prelayer. To suppress the unwanted interdiffusion while maintaining lower APDs formation, the graded-temperature As prelayer was inserted between GaAs and Ge epitaxy. Besides, the effect of III-V ratio, growth temperature and annealing process on the GaAs/As/Ge/Si heterostructure are also discussed in the following.

5.3.1 Effect of V/III ratios on the surface morphology of GaAs grown on Ge/Si substrate using graded-temperature arsenic prelayer

Figure 5-13 illustrates the AFM images of the GaAs/As epitaxy grown on the Ge/Si heterostructure. The root mean square (RMS) roughness of the samples was about 7.0, 2.3,

12.1, 15.6, and 21.7nm for the GaAs layers grown with V/III ratios of 11, 20, 30, 50, and 75, respectively. A large variation in the surface roughness with hill-and-valley structures was observed for the samples grown with inappropriate V/III ratios.

At the low V/III ratio of 11 (i.e., lower As flow), the possibility of Ga atoms being incorporated into GaAs epitaxy exceeds that of As atoms, leading to poor surface morphology and APD formation [31,32]. For V/III ratios larger than 30, the surface morphology becomes rougher because of the different growth rates at different growth orientations [33]. The growth rate of GaAs epitaxy in the [110] direction is faster than that in the [-110] direction for higher V/III ratios and at lower growth temperature [33,34]. The arsine dependence of the [110] and [-110] growth rates under constant TMGa partial pressure is represented in Fig. 5-14. The [-110] growth rate as well as the vertical growth rate are almost constant in the range of 1.1×10^{-4} to 3.7×10^{-3} atm, corresponding to $[AsH_3]/[TMG]=1.7$-58. The [110] growth rate also remained constant above $[AsH_3]$ of 1.8×10-3 atm, but it decreased below this $[AsH_3]$. It is noteworthy that crossing between the [110] and [-110] growth rate occurs around an $[AsH_3]$ of 4×10^{-4} atm. The remarkable results obtained in this study are summarized in the following.

(A) The [110] growth rate is higher than [-110] at high V/III ratio and low growth temperature.

(B) The [110] growth rate decreases with decreasing $[AsH_3]$ partial pressure, while [-110] growth rate remains constant.

At high V/III ratio and low growth temperature, a large number of As species impinge

onto a Ge epitaxial surface and the desorption probability for As species is low. In this condition the Ge epitaxial surface is considered to be covered with As species. Fig. 5-15 shows the cross sections of the [110] and [-110] steps. According to this model, we found that the probability of As incorporation into the step sits is higher than that on flat Ge epitaxial surface, migrating Ga atoms are easily caught at the [110] and [-110] steps. Here, the Ga atom caught at the [110] steps is bound with three bonds; one to step side and two to the step bottom, while the Ga at the [-110] steps is bound with two bonds; both to the step bottom as shown in Fig. 5-15. It is clear from the model shown in Fig. 5-15 that migrating Ga atoms can be easily incorporated into the [110] steps than [-110] steps. Therefore, the [110] growth rate is higher than [-110] at high V/III ratio and low growth temperature.

It is known that a high V/III ratio is required for the growth of the GaAs/Ge/(Si) heterostructure without any interfacial layer [31,35]. The results shown in Fig. 5-13(a)~(e) indicate that the graded-temperature As prelayer sufficiently improves the surface morphology of GaAs epitaxy grown on Ge/Si substrate at a low V/III ratio of 20, even at a growth temperature of 450℃. This growth technology can effectively decrease the cost for GaAs/Ge/Si heterostructure growth.

5.3.2 Effect of high-temperature substrate annealing on the quality of GaAs grown on Ge/Si substrate using graded-temperature arsenic prelayer

Controlling the surface structure is another efficient way to suppress APD formation prior to the GaAs growth [3]. Figure 5-16 illustrates the cross-sectional TEM images of the GaAs epitaxy (V/III: 20) grown on the Ge/Si heterostructure using a graded-temperature As prelayer. It can be seen that many APDs were formed in the GaAs layer on the unannealed Ge/Si substrate (threading dislocation density: ~$1\times10^{8}cm^{-2}$), as shown in Fig. 5-16(a). For the substrate annealed at 650℃, an APD-free GaAs epitaxy with lower dislocation density (~$2\times10^{7}cm^{-2}$) was obtained (Fig. 5-16(b)). These results suggest that, following the short annealing process at high temperature, surface transition may occur on the Ge surface that generates many extra atomic surface steps [3] to provide better As coverage. It is also demonstrated that the smallest RMS roughness of 1.1nm was achieved for the samples grown using the graded-temperature As prelayer with substrate annealing process at 650℃, as shown in Fig. 5-13(f). Experiments confirmed that annealing the Ge/Si substrate at >600℃ before dropping to the nucleation temperature is essential for single-domain GaAs growth.

According to the reference [4,23] described before, maybe GaAs-B is the dominant when the growth temperature was reduced from 650℃ to 420℃ in this study. However, it should be noted that the configuration of double atomic-layer steps as shown in 5-9(b) is favorable than single atomic-layer steps owing to the different in energy as shown in Table 5-2 [15]. On the

other hand, the step formation energy of double atomic-layer steps is also lower than that of single atomic-layer steps when high-temperature substrate annealing was adopted. It means that high-temperature substrate annealing may transfer single-layer steps into double-layer steps [16]. Therefore, surface transition kinetics are most likely to be limited upon cooling to high temperature. The temperature-dependent surface transition that normally leads to GaAs-B nucleation elsewhere has been quenched, and that the high temperature preference for GaAs-A has been preserved.

Growth temperature including annealing temperature is very important parameter for GaAs/Ge/Si heterostructure. In normal condition, which means that no As prelayer was used during material growth, GaAs grown at too low temperature resulted in an excess As point defects, which enhance the nucleation loops. These loops expanded during the subsequent high temperature GaAs growth, which generated high threading dislocation density in the thick GaAs epitaxy [37]. In contrast, GaAs grown on Ge/(Si) substrate without As prelayer at higher growth temperature and low growth rates may result in the formation of an unwanted p-n junction due to simultaneous interdiffusion of Ga and As into Ge epitaxy, which in turn reduces the solar cell efficiency. In my study, the graded-temperature As prelayer was grown on Ge/Si substrate with substrate annealing process prior GaAs epitaxial growth. We fear that the arsenic atoms in the graded-temperature As prelayer interact with Ge atoms and change surface reconstructions and then affect the quality of GaAs epitaxy. In the selective-area

diffraction pattern diffracted from the GaAs/As interface area, only the GaAs diffraction spots exist along [110] zone axis as shown in Fig. 5-16(b). Different crystal structure has been not existed from that of GaAs. This observation suggests that the graded-temperature arsenic prelayer enhances the As concentration on the Ge surface, which can be verified by Fig. 5-17, and does not generate different crystal structure in the GaAs/As epitaxy. This implies that As coverage formed on the Ge/Si substrate did not change the structural configuration of GaAs/Ge epitaxy. The As prelayer grown on the Ge/Si substrate annealed at 650℃ modifies the surface morphology of the GaAs epitaxy and reduces the APD formation.

Figure 5-18 illustrates the HRXRD results of the GaAs/As epitaxy on both the unannealed Ge/Si substrate and the Ge/Si substrate annealed at 650℃. In regard to the change of GaAs Bragg angle (~45arcsec) for these two samples, we speculated that carbon incorporation may have played a role in the GaAs epitaxy with low V/III ratios. The lattice contraction is attributed to the incorporation of substitutional carbon during the growth of the III-V materials, as discussed in a recent study [36]. The HRXRD and SIMS results show that the substrate annealing process effectively reduced carbon incorporation into the GaAs epitaxy, as shown in Fig. 5-18 and Fig. 5-19. Furthermore, full width at half maximum (FWHM) value of the GaAs peak decreased from 402 to 250 arcsec, which confirms that annealing step improves the GaAs crystal quality.

5.3.3 Effect of graded-temperature arsenic prelayer on the interdiffusion of GaAs/Ge/Si heterostructure

The As prelayer was deposited onto the Ge epitaxy while the growth temperature was ramped from 300 to 420℃. It is demonstrated that the graded-temperature arsenic prelayer grown on a Ge/Si substrate annealed at 650℃ not only improves the surface morphology (roughness: 1.1nm) but also reduces the anti-phase domains' (APDs) density in GaAs epitaxy (dislocation density: ~$2\times10^{7}cm^{-2}$) as shown in Fig. 5-13, 5-16 and 5-18. High quality GaAs epitaxy can increase III-V solar cell efficiency grown on Si substrate. However, the interdiffusion is another important issue, which forms unwanted P-N junction in the cell, for high efficiency and low cost III-V solar cells. Figure 5-20 illustrates the SIMS depth profiles of Ge, As, and Ga atoms in the GaAs epitaxy grown on the Ge/Si heterostructure using the graded-temperature As prelayer. It is found that the interdiffusion of Ge into GaAs was suppressed for all the samples with ultrathin graded-temperature arsenic prelayer. Because the energy of the As-Ge bond (35.8 kcal/mol) is much lower than that of the Ga-Ge bond (46.7 kcal/mol) as shown in Table 5-3 [38], the Ge atoms segregate at the As prelayer before the deposition of the GaAs layer at low growth temperature. On the other hand, this implies that the As atoms can diffuse into the Ge layer easily and react with the Ge atoms. The incorporation probability of As atoms in the GaAs/Ge system could be described by Barnett et al. [39] and shown in Equation (5-3).

$$J^{net}=\alpha^{In}+d\theta_s/dt \qquad (5\text{-}3)$$

The incorporation rate α^{In} = N·GT, where N and GT are the As concentration and growth rate in the film respectively. The net flux $J^{net} = J^{sup}-J^{des}$, where J^{sup} represents the supplying flux of AsH_3 and J^{des} is the total desorption flux. The As surface coverage, $d\theta_s/dt$, is zero at steady state. At steady state, this net flux represents a flux of AsH_3 (J^{net}) which is successfully decomposed and incorporated and should be equal to the incorporation rate (α^{In}). As the As concentration N is increased at higher III-V ratio, the incorporation rate α^{In} and the net flux J^{net} increases according to the equation. For V/III ratios larger than 20 (i.e., larger As flux), the larger J^{net} resulted in significant As interdiffusion as shown in Fig. 5-20(a)–(d). For GaAs epitaxy with a V/III ratio of 20 and the graded-temperature As prelayer on the Ge/Si heterostructure annealed at 650℃, virtually no As interdiffusion was observed as shown in Fig. 5-20(e). As judged from the SIMS and TEM results, the As prelayer grown using graded-temperature technique is also an excellent candidate for suppressing interdiffusion of the Ga, As, and Ge atoms.

5.4 Summary

In summary, we have demonstrated that the As prelayer grown using graded-temperature technique on the Ge/Si substrate annealed at 650℃ effectively improves the surface morphology of GaAs epitaxy (roughness: 1.1 nm) and avoids the need for high V/III ratios, unlike in traditional growth techniques [31,35]. The thin GaAs epitaxy grown on the Ge/Si substrate also contains lower APD density (~$2x10^{7}cm^{-2}$) and lower carbon incorporation when the graded-temperature As prelayer and substrate annealing process were adopted. These results suggest that the generation of atomic steps on the Ge surface promotes As deposition at lower growth temperature and boosts single-domain GaAs-A growth during the heterostructure growth of GaAs/As/Ge/Si. Furthermore, we also demonstrate that the interdiffusion of Ge and As atoms in the GaAs/Ge/Si heterostructure can be effectively suppressed by the graded-temperature As prelayer because of the difference in energies between As-Ge and Ga-Ge bonds and low As flux. These excellent results suggest that the graded-temperature As prelayer grown on Ge/Si substrate has great potential for use in the growth of III-V nanoelectronic devices and optoelectronic devices on the Si substrate.

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Table 5-1 Lattice constants and thermal expansion coefficients of GaAs and Ge

Material	Lattice constant	Thermal expansion coefficient
Ge	5.675 Å	$5.75\times10^{-6}K^{-1}$
GaAs	5.653 Å	$5.8\times10^{-6}K^{-1}$

Table 5-2 Step formation energies per unit length on Ge (001) surface [15]

Step	Energy (eV/a)
S_A	0.01 ± 0.01
S_B	0.15 ± 0.03
D_A	0.54 ± 0.10
A_B	0.05 ± 0.02

Bond (Ga site)-(As site)	Bond energy (kcal/mol)
Ga-As	47.7
Zn-As	84.4
Cd-As	52.0
Hg-As	38.8
B-As	72.9
Al-As	62.0
In-As	36.0
Si-As	38.1
Ge-As	35.8
Sn-As	34.1
Ga-Si	49.0
Ga-Ge	46.7
Ga-Sn	45.0
Ga-N	96.8
Ga-P	58.4
Ga-Sb	58.2
Ga-S	80.4
Ga-Se	69.5
Ga-Te	58.6

Table 5-3 Single-bond energy used for the calculation [38]

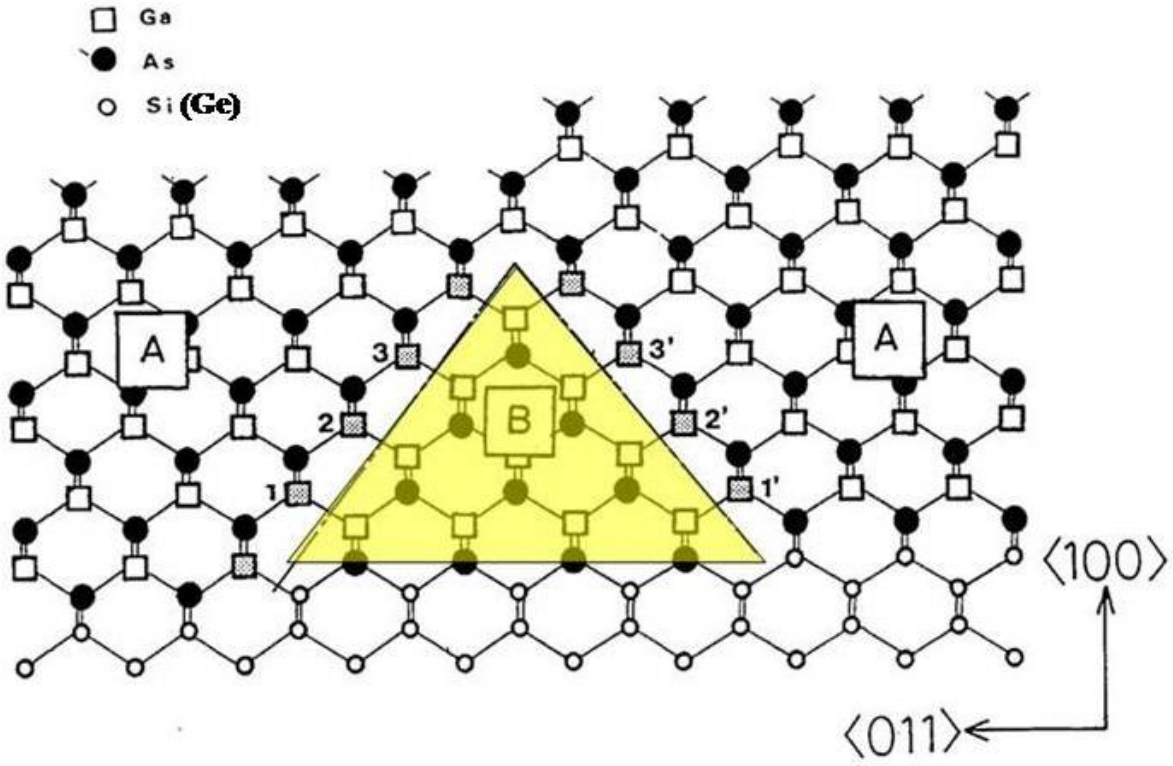

Figure 5-1 Anti-pahase formation of polar semiconductor materials on non-polar semiconductor materails

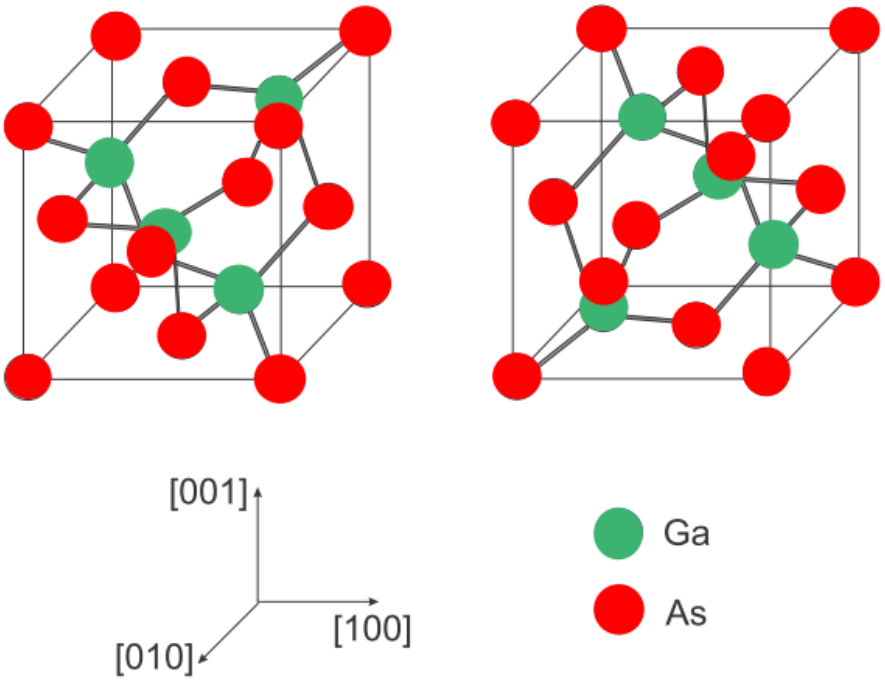

Figure 5-2 Schematic drawings of GaAs crystal structure

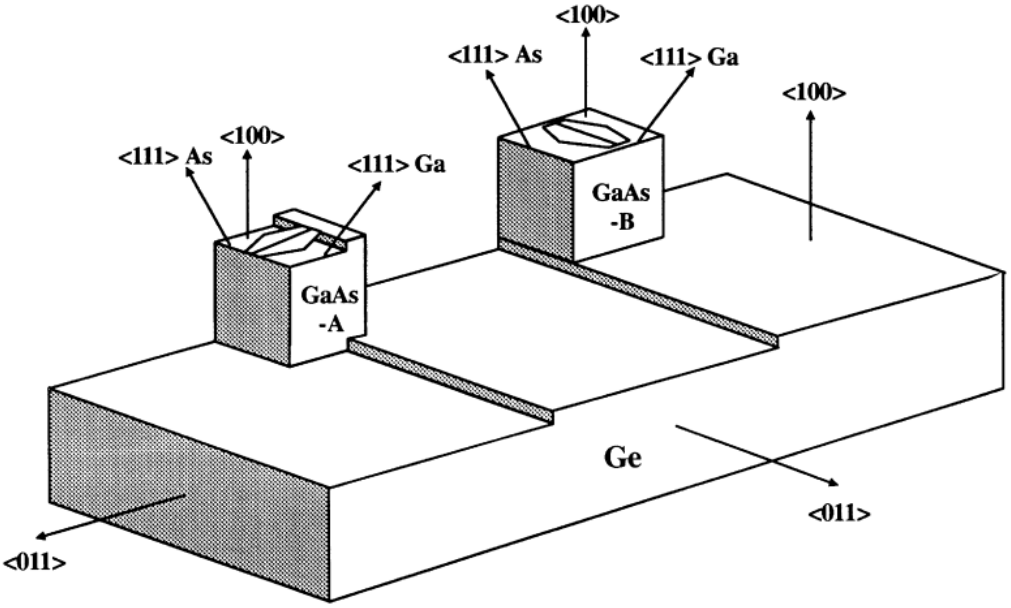

Figure 5-3 The two possible sublattice locations of Ga and As atoms in GaAs grown on Ge epitaxy

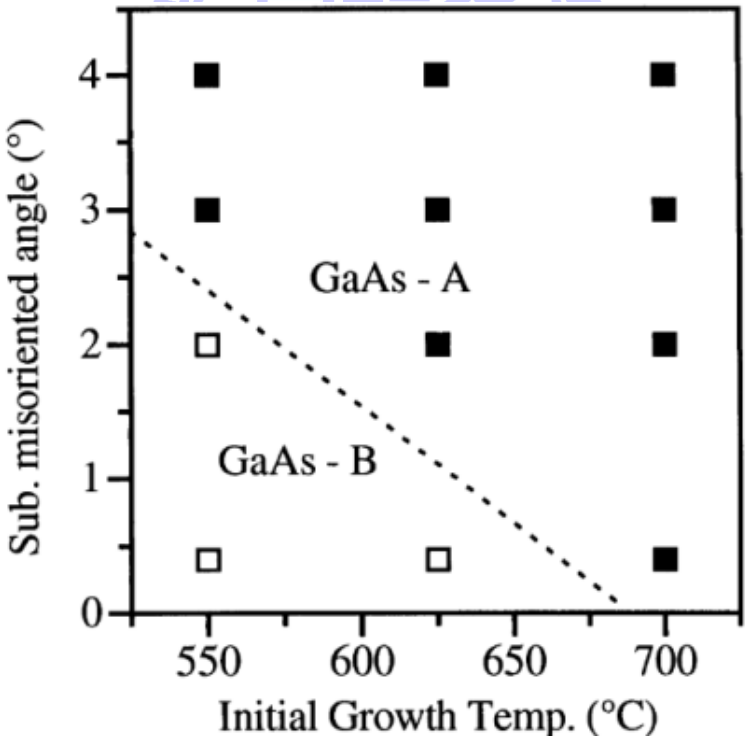

Figure 5-4 Sublattice location phase diagram as a fuction of growth temperature and disorientation angle for GaAs on Ge (100) off towards (111) [6]

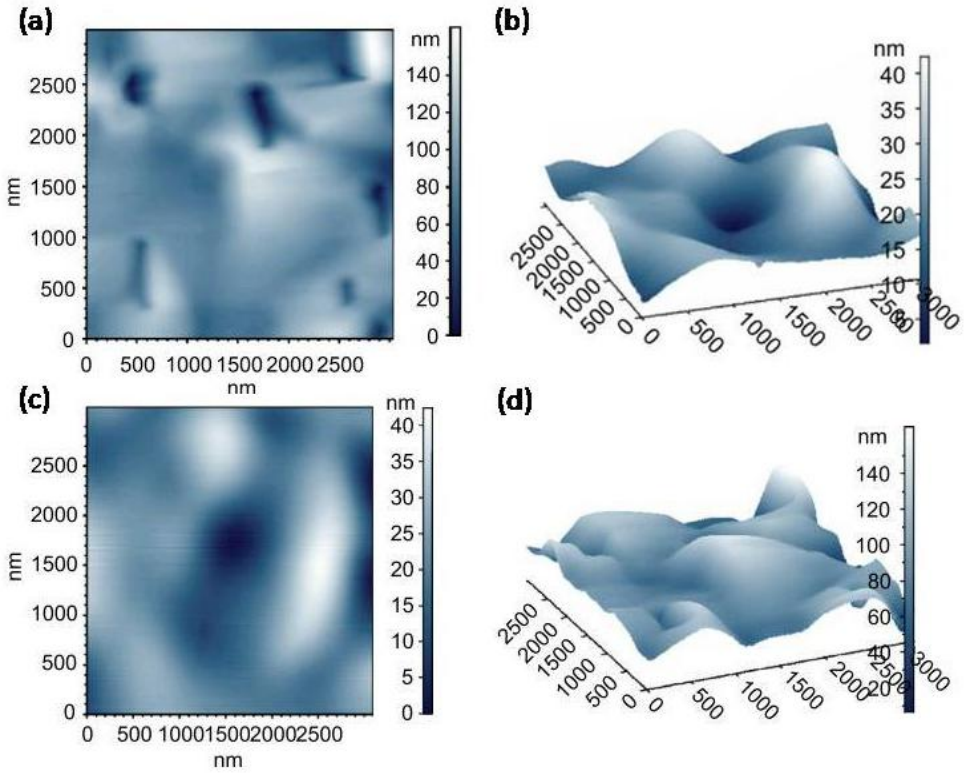

Figure 5-5 2-D and 3-D AFM topographical images of the GaAs epitaxial layers grown on 6° off-oriented Ge substrate with growth temperature at (a)(b) (b) 650℃ and (c)(d) 750℃. [4]

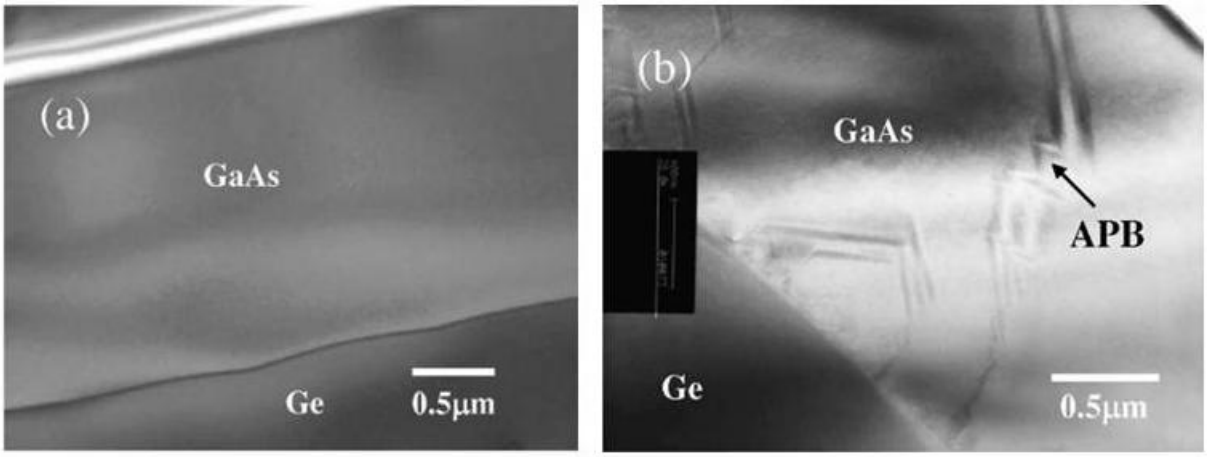

Figure 5-6 TEM images of GaAs grown on Ge substrate with different misorientation angles (a) 6° and (b) 0°. [5]

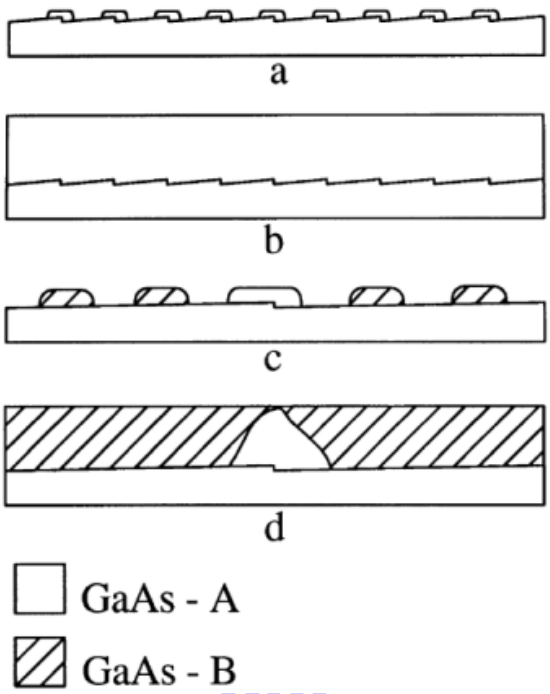

Figure 5-7 A model to explain the reversal of the sublattice locations between GaAs grown on (100) Ge off toward (111) substrates with small and larger misoriented angles. (a) Nucleation on Ge substrate with larger misoriented angles: nuclei form only at steps. (b) Overgrowth on such surface results in that the initial nuclei are connected with each other so that single-phase domain of GaAs-A is achieved. (c) Nucleation on Ge substrate with small misoriented angles: nuclei form at steps and on the terraces.(d) Overgrowth on such surface resultsin that the initial nuclei at the steps are surrounded by theAPDs. [13]

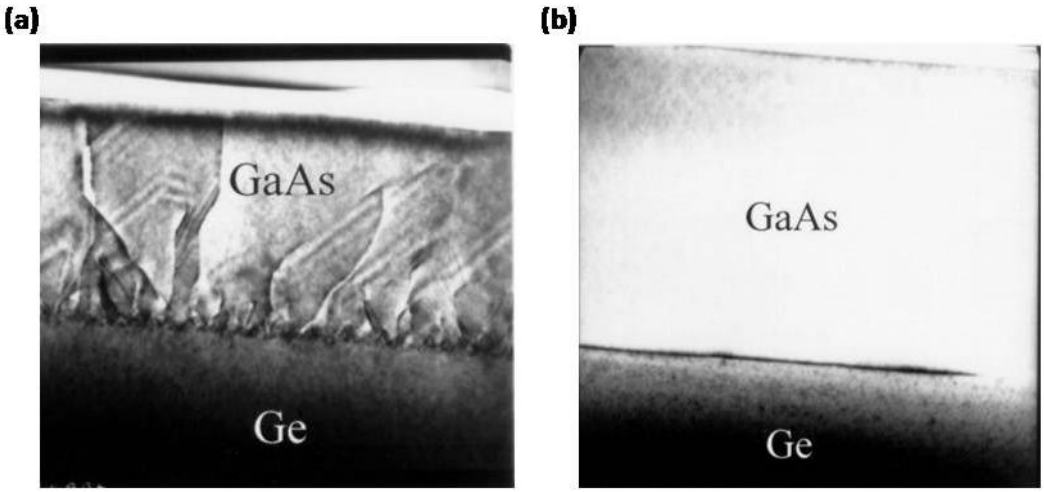

Figure 5-8 Cross-sectional TEM micrographs of two 1μm thick GaAs films grown on Ge. (a) Film with high APDs densities extending to the surface, grown on an unannealed epitaxial Ge layer. (b) APD-free film grown on an annealed epitaxial Ge layer. [14]

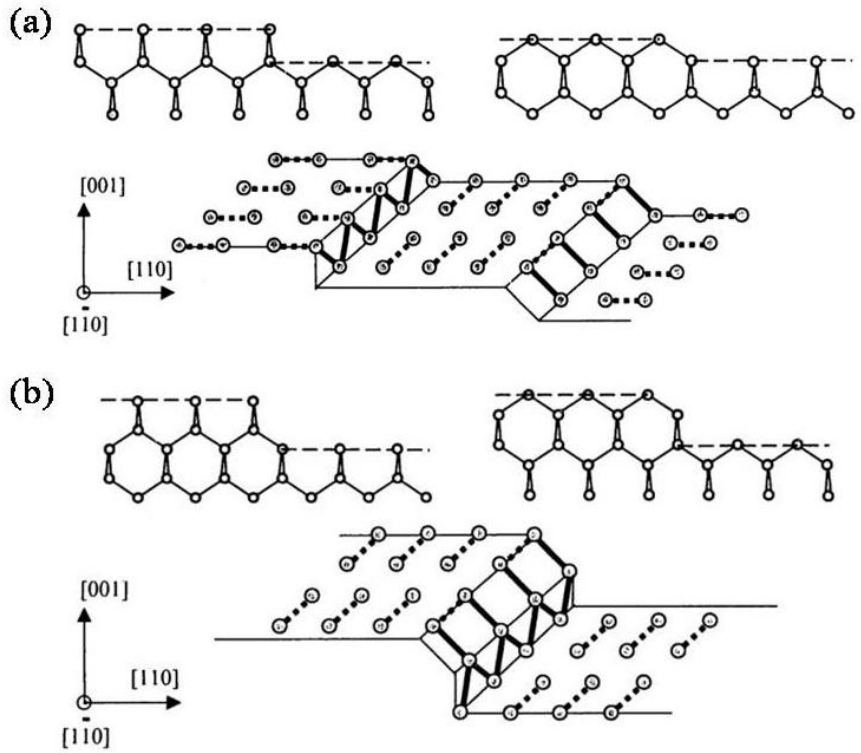

Figure 5-9 (a) S_A (upper left) and S_B (upper right) single atomic-layer steps. On a mixed domain surface (bottom) both types of single steps are evident. Note the rotation of dimerization axes and dimer rows on alternating terraces. (b) D_A (upper left) and D_B (upper right) double atomic-layer steps. Note that only D_B steps are observed experimentally, D_A steps are energetically unfavorable. On the single-domain surface (below) the dimerization axis and dimer rows are invariant across the D_B step. [15,16]

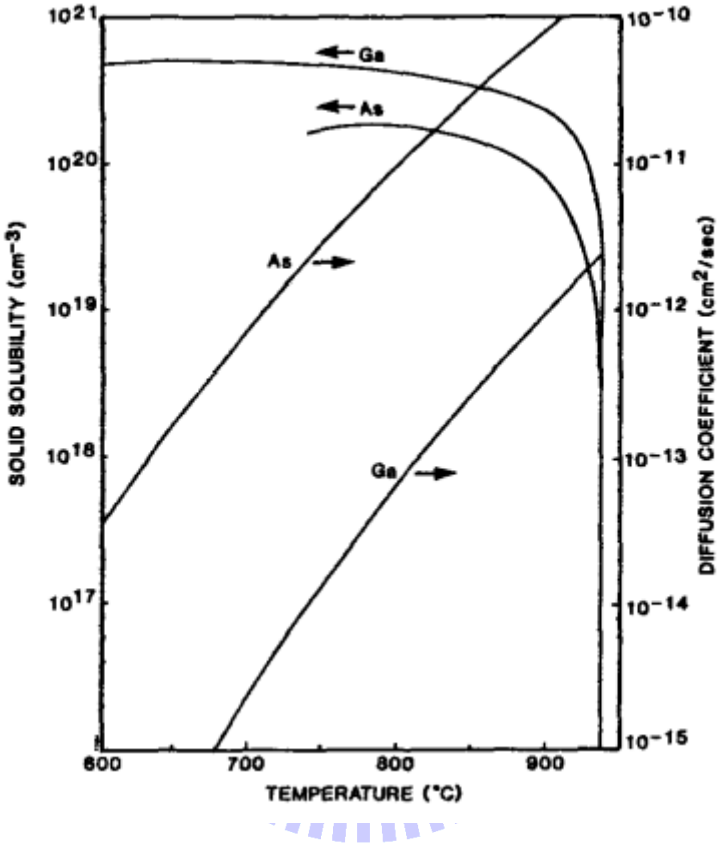

Figure 5-10 Diffusion coefficients and solid solubilities of Ga and As in Ge layer. [21]

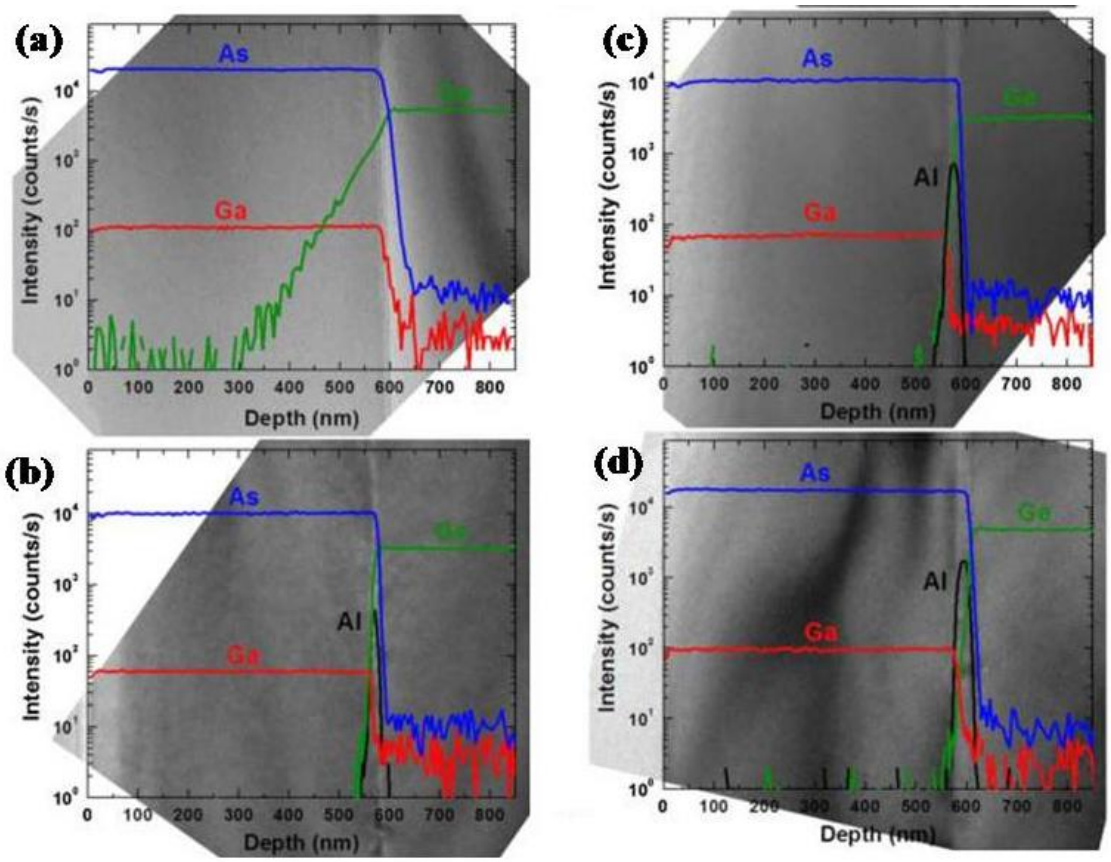

Figure 5-11 SIMS profiles for GaAs/AlAs/Ge samples with AlAs nominal thickness of (a) 0, (b) 10, (c) 20, and (d) 30 nm. The corresponding TEM image for each sample is placed behind the graph to illustrate the position of the layers. [18]

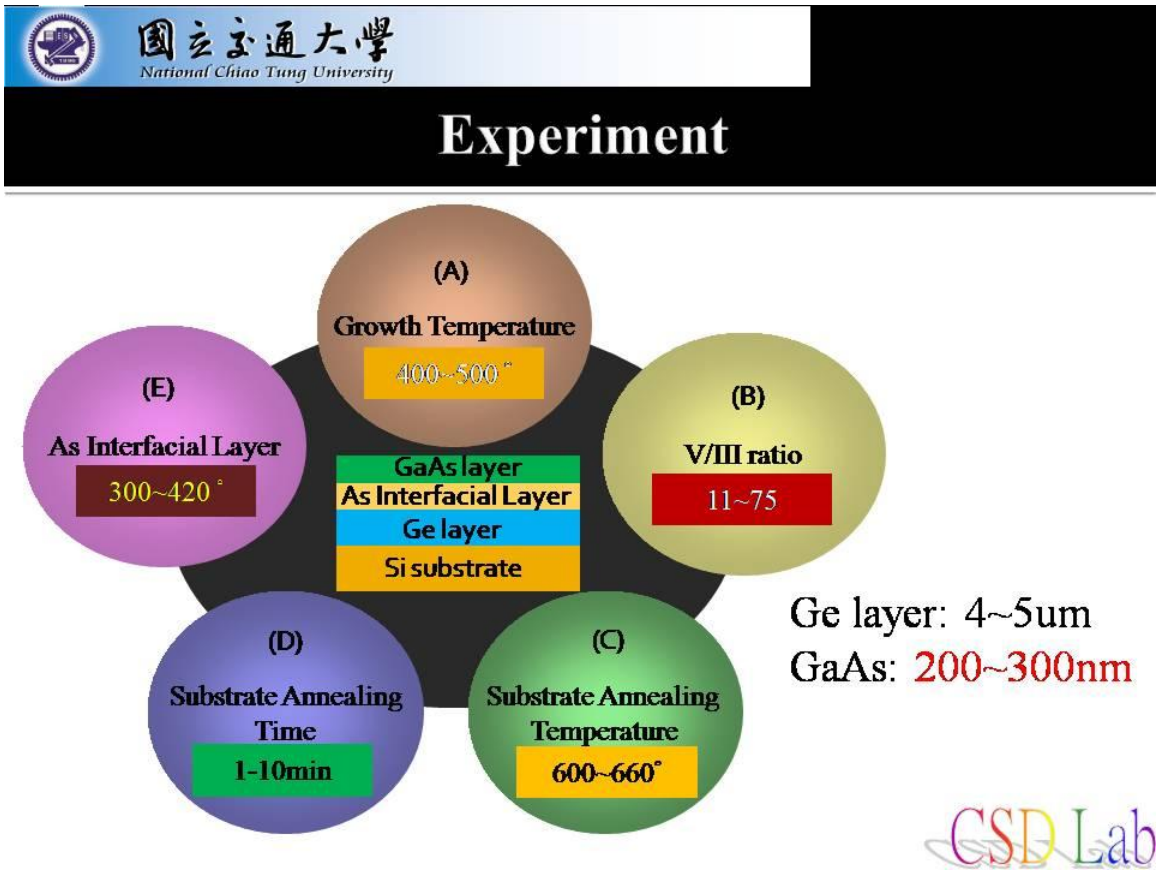

Figure 5-12 All parametrs used in the study are shown in the chart, which include growth temperature, V/III ratio, substrate annealing temperature, substrate annealing time and growth temperature of As prelayer.

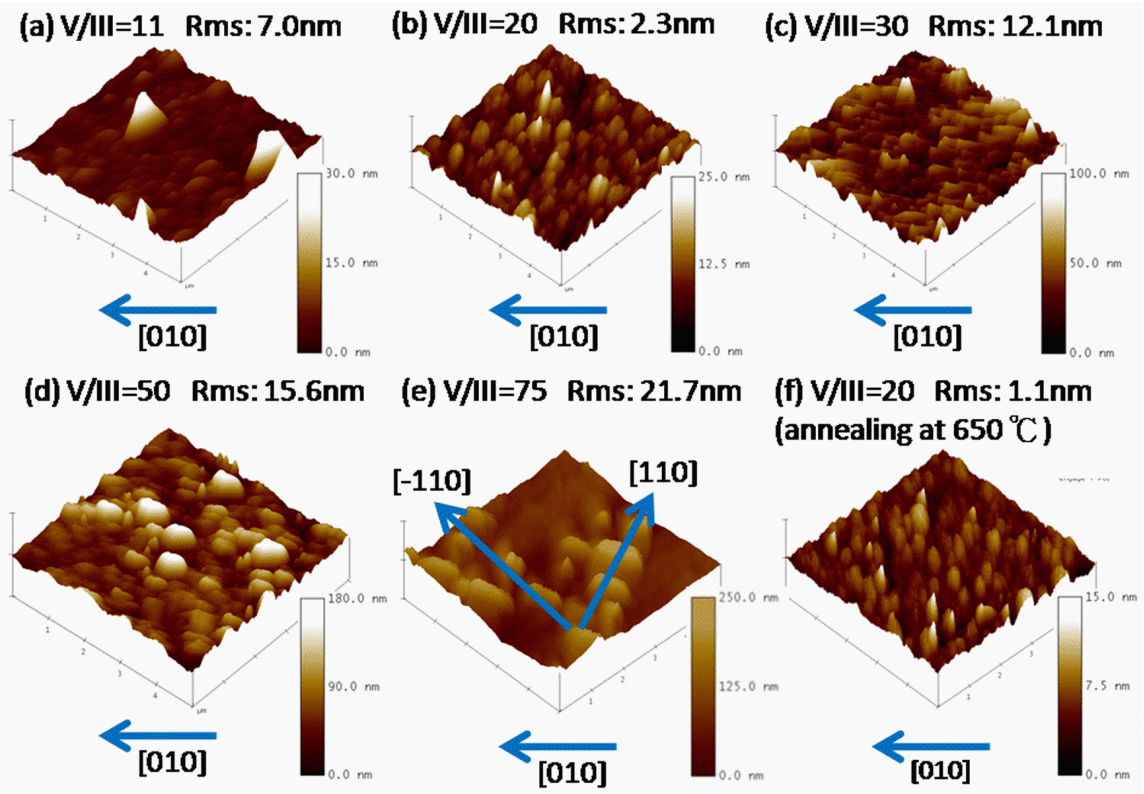

Figure 5-13 AFM images (5μm×5μm) of GaAs layer with different V/III ratios grown on a Ge/Si substrate using a graded-temperature As prelayer (a) V/III: 11, (b) V/III: 20, (c) V/III: 30, (d) V/III: 50, (e) V/III: 75, and (f) V/III: 20 and annealed at 650℃.

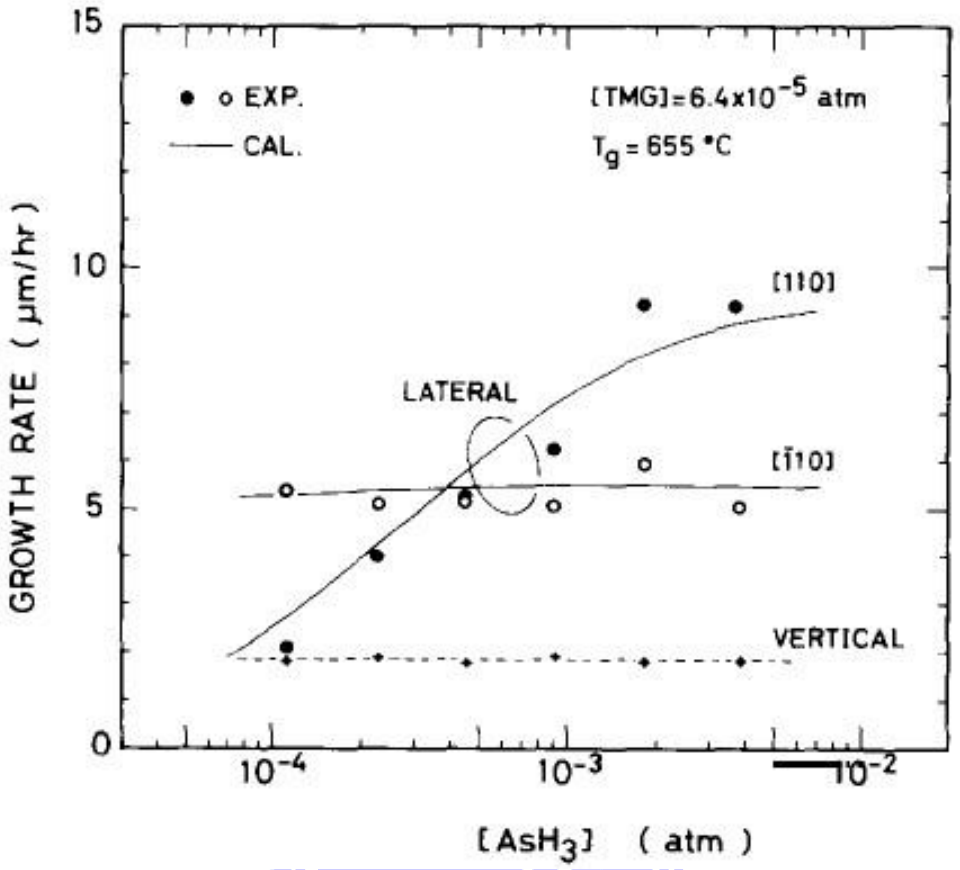

Figure 5-14 Lateral and vertical growth rates as a function of [AsH_3] [33,34]

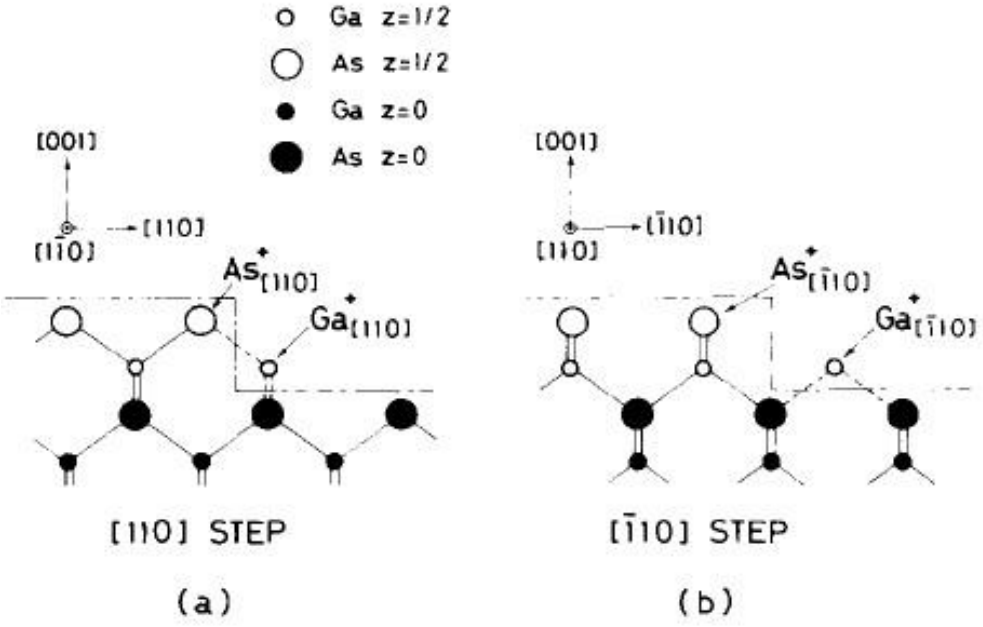

Figure 5-15 Schematic cross sections of (a) [110] and (b) [-110] steps [34]

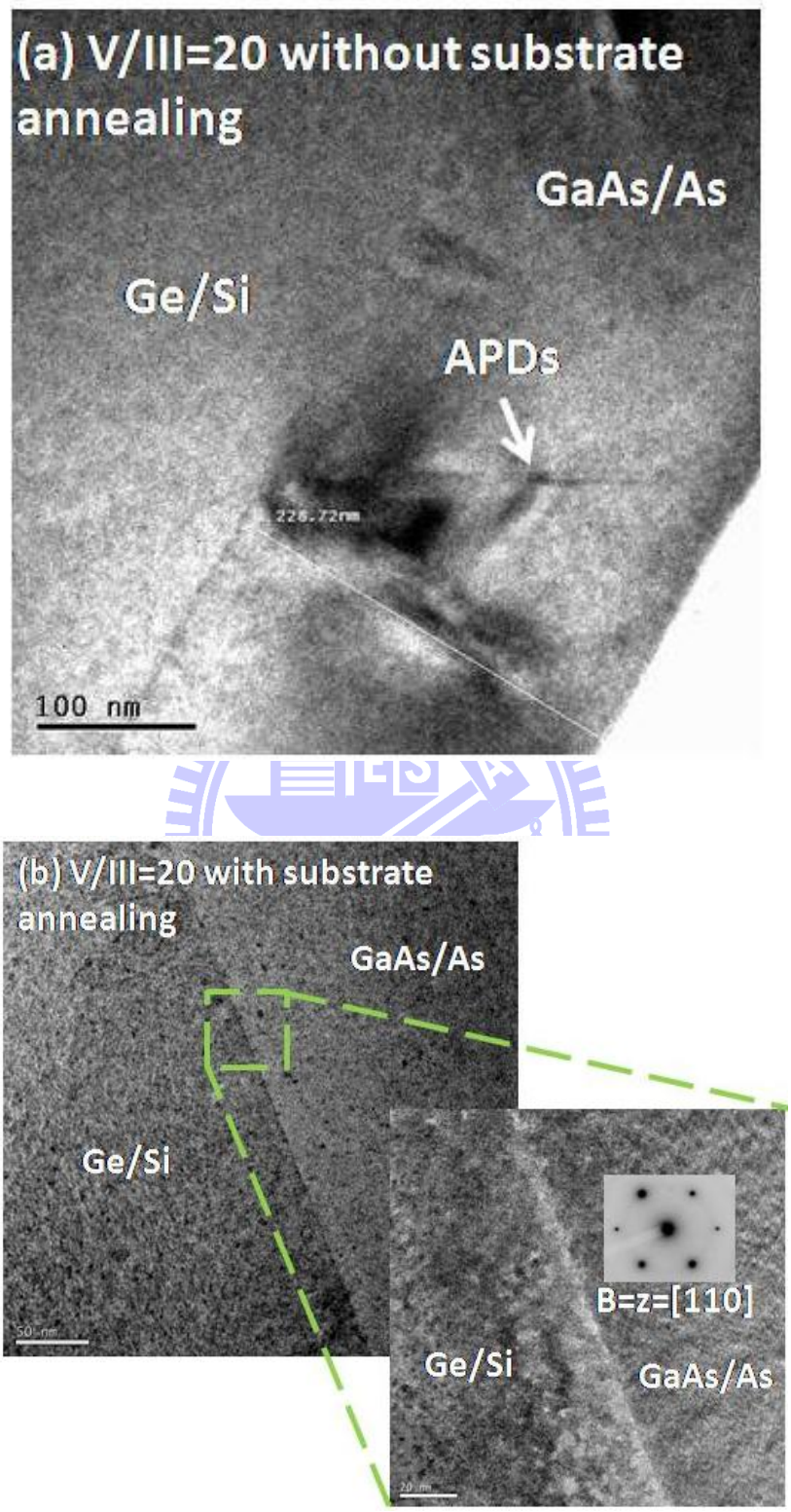

Figure 5-16 TEM cross-sectional micrograph of GaAs/As/Ge/Si heterostructure grown at a V/III ratio of 20. (a) unannealed Ge/Si substrate and (b) Ge/Si substrate annealed at 650℃

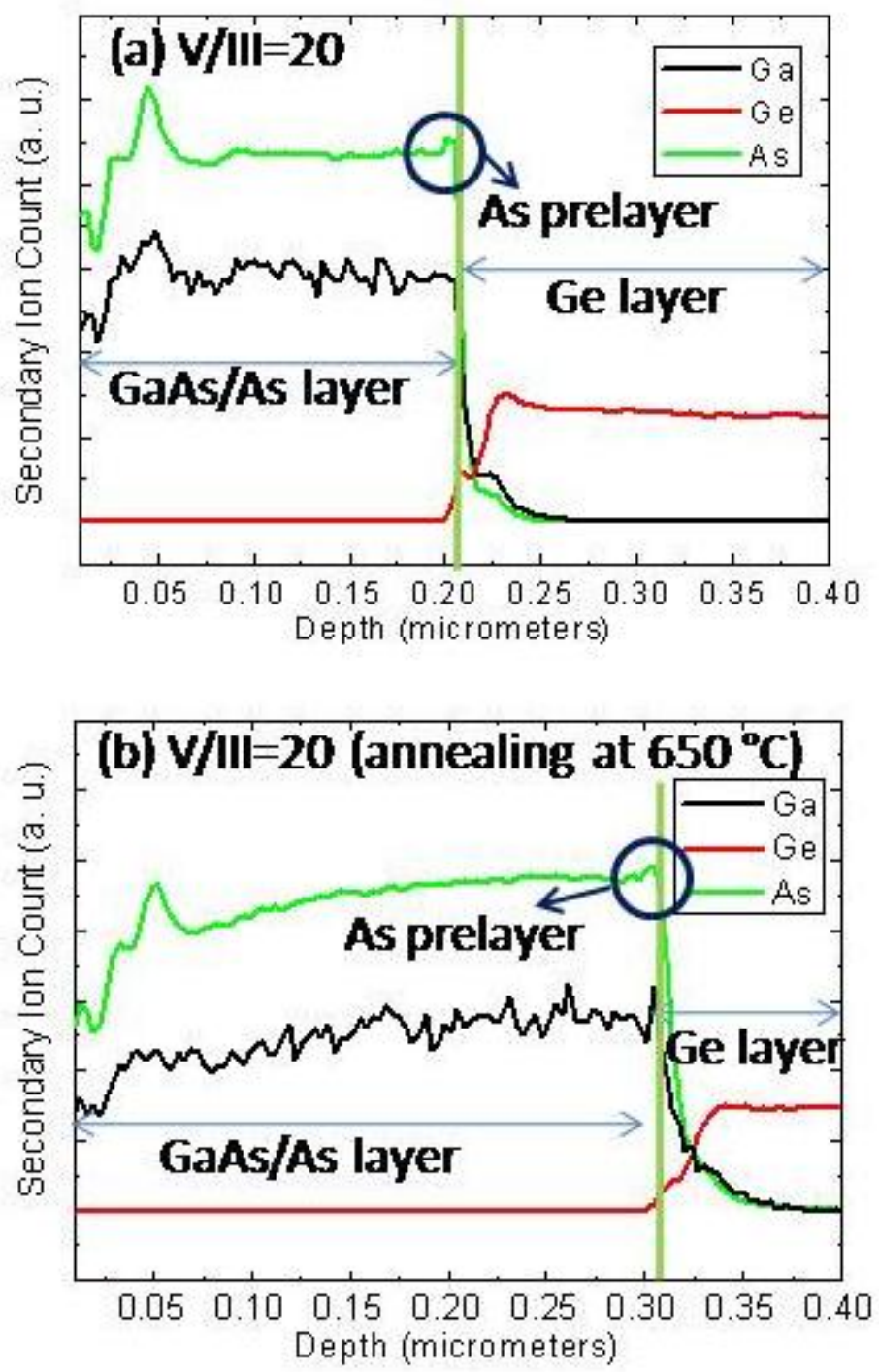

Figure 5-17 SIMS profiles for GaAs epitaxy grown at different V/III ratios on a Ge/Si substrate with a graded-temperature As prelayer (a) V/III: 20, (b) V/III: 20 and annealed at 650℃

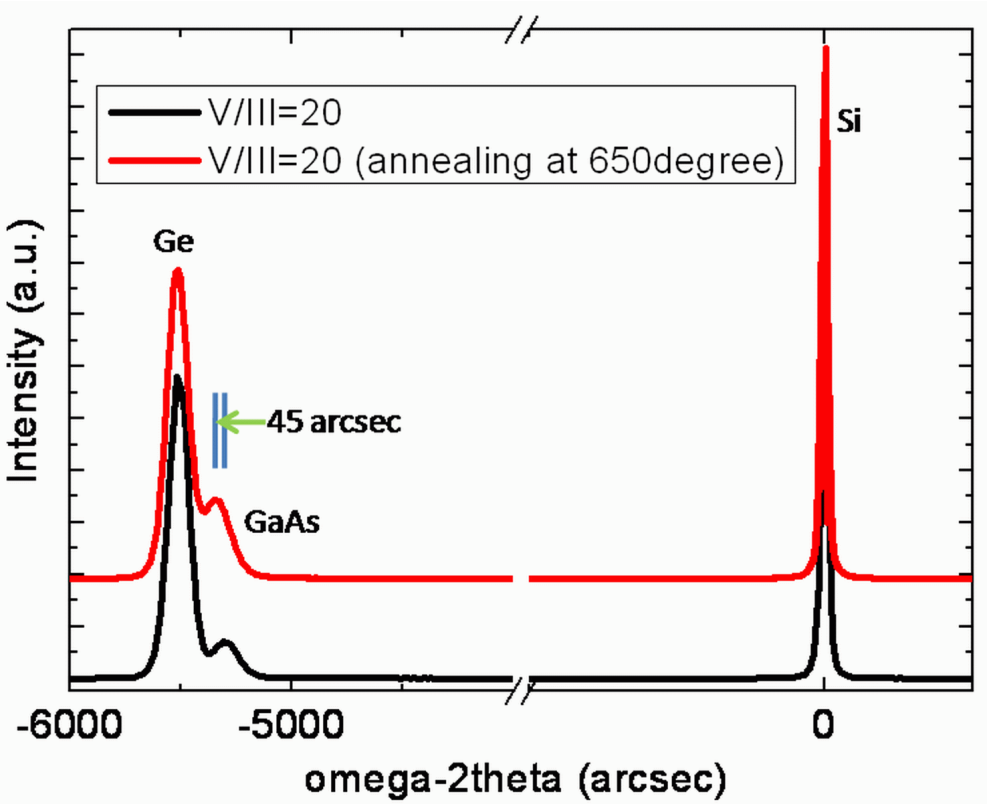

Figure 5-18 HRXRD rocking curves of the GaAs/As/Ge/Si heterostructure grown at a V/III ratio of 20. (a) unannealed Ge/Si substrate and (b) Ge/Si substrate annealed at 650℃

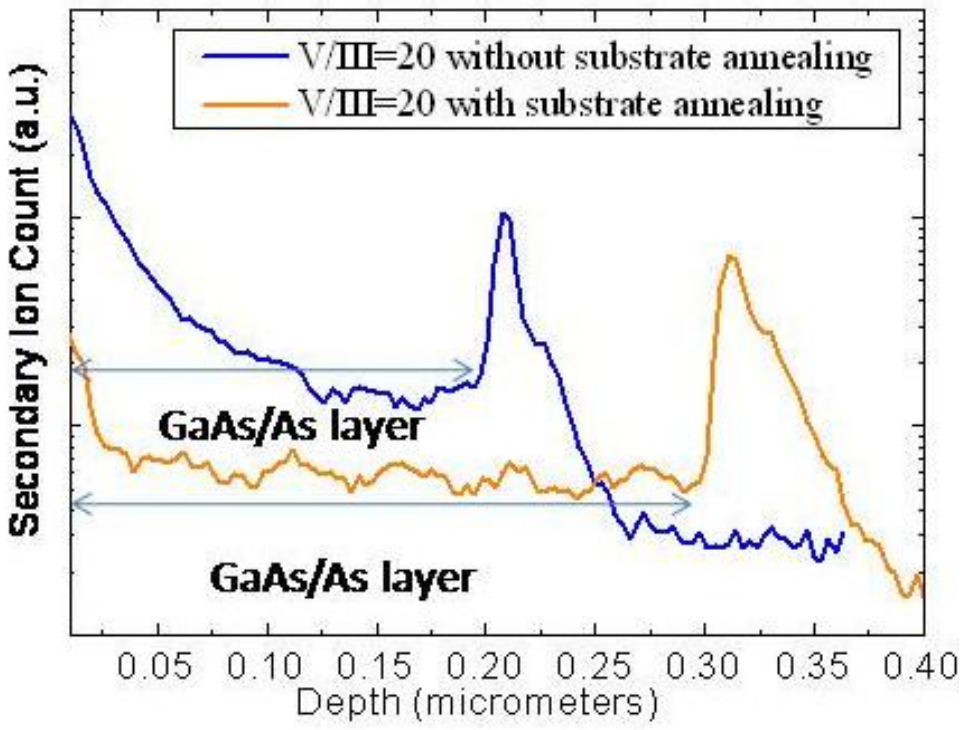

Figure 5-19 SIMS profile of carbon for the GaAs/As epitaxy grown on both the unannealed Ge/Si substrate and the Ge/Si substrate annealed at 650℃.

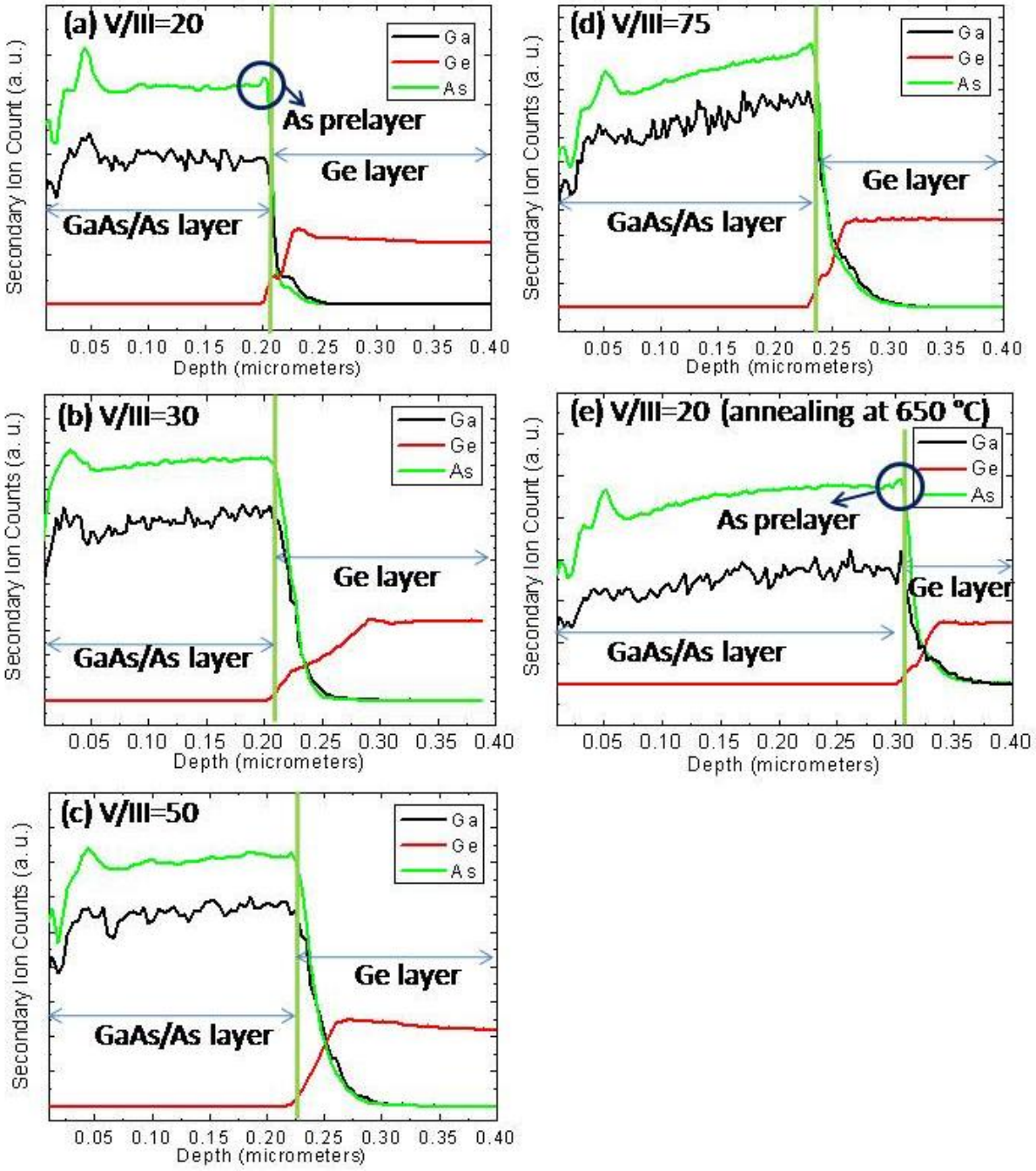

Figure 5-20 SIMS profiles for GaAs epitaxy grown at different V/III ratios on a Ge/Si substrate with a graded-temperature As prelayer (a) V/III: 20, (b) V/III: 30, (c) V/III: 50, (d) V/III: 75, (e) V/III: 20 and annealed at 650℃.

Chapter 6

Conclusion and future work

6.1 Conclusion

In conclusion, we have demonstrated that the misorientation of GaAs substrates has a direct effect on the material properties of the P^{++}-AlGaAs/N^{++}-GaAs tunnel diodes (TDs) for multijunction III-V solar cell application, as shown in chapter 3. The best surface morphology and interface sharpness for the TDs were obtained on the (100) tilted 10° off toward [111] GaAs substrate. Results show that the TD materials grown on this misoriented substrate can overcome the limitation of high surface free energy and with reduced sticking coefficient for oxygen-incorporation in the N^{++}-GaAs layers. Besides, we also found that this substrate has also reduced the anisotropic sites for oxygen-incorporation in the P^{++}-AlGaAs layers.

On the other hand, we also proved that InGaP/GaAs dual junction solar cells with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10°off GaAs substrates exhibit superior photovoltaic conversion efficiency (~20%) when operated at one sun, as shown in chapter 4. The cell design with a P^{++}-AlGaAs/N^{++}-GaAs TD grown on 10°off GaAs substrates produces higher EQE (~82% for InGaP top cell and 85% for GaAs bottom cell) as compared to the P^{++}-GaAs/N^{++}-InGaP TD. Furthermore, when these solar cell devices were operated at higher concentration ratios, they displayed superior I-V characteristics compared to the traditional dual-junction solar cell grown on 6° off misorientation GaAs substrates, as shown in chapter 4.

These results suggest that 10° off misorientation GaAs substrates for cell design with a P^{++}-AlGaAs/N^{++}-GaAs TD not only produce high light-trapping and carrier-collection efficiencies but also generate higher peak current density (J_{peak}) at higher concentration ratios (185×) than that of a P^{++}-GaAs/N^{++}-InGaP TD grown on 6° off GaAs substrate, even if the thickness of ohmic contact in the study is not sufficient.

To decrease the cost of concentrated photovoltaic solar cells (CPVSCs), we try to grow III-V materials, such as GaAs, on the Ge/Si substrate by low-pressure metal organic chemical vapor deposition to replace traditional InGaP/(In)GaAs/Ge triple-junction solar cells. We have demonstrated that the As prelayer grown using graded-temperature technique on the Ge/Si substrate annealed at 650℃ effectively improves the surface morphology of GaAs epitaxy (roughness: 1.1 nm) and avoids the need for high V/III ratios, as shown in chapter 5. The thin GaAs epitaxy grown on the Ge/Si substrate also contains lower APD density (~$2x10^7 cm^{-2}$) and lower carbon incorporation when the graded-temperature As prelayer and substrate annealing process were adopted. Furthermore, we also demonstrate that the interdiffusion of Ge and As atoms in the GaAs/Ge/Si heterostructure can be effectively suppressed by the graded-temperature As prelayer because of the difference in energies between As-Ge and Ga-Ge bonds and low As flux. These results suggest that the graded-temperature As prelayer grown on Ge/Si substrate has great potential for use in the growth of III-V nanoelectronic devices and optoelectronic devices on the Si substrate.

6.2 Future work

The purpose of the study in this thesis was to investigate some advanced techniques that can enhance the conversion efficiency and reduce production cost of III-V multijunction solar cells. Following the invesigations desrcibed in the thesis, some projects could be propose in the future.

(A) (100) tilted 10° off toward [111] GaAs substrates can be used for the growth of inverted metamorphic multijunction solar cell structures, which is built on GaAs based substrates and inverted onto other substrates.

(B) The GaAs epitaxy can be grown on Ge substrate using graded-temperature As prelayer and substrate annealing technique to replace traditional InGaP nucleation layer in InGaP/(In)GaAs/Ge triple junction solar cell. The thin GaAs epitaxy on Ge substrate using this technique is very stable, and it doesn't encroach on Spectrol-Lab's patent (US 6,380,601 B1).

(C) III-V multijunction solar cells can be grown on Ge/Si substrate using GaAs buffer layer, which decreases the cost of PVSCs and increase its competitiveness in this field.

Publication List

Journal papers

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[1] **Hung-Wei Yu**, Chen-Chen Chung, Nguyen Hong Quan, Wei-Chieh Wang , E. Y. Chang, " Investigation of $Al_xGa_{1-x}As$/GaAs Heterostructures" 2009 5th NTT-BRL School in Japan**.**

[2] **Hung-Wei Yu**, H.Q. Nguyen, J. T. Chang, C. C. Chung, W. C. Wang , C. H. Hsu, E. Y. Chang, " Investigation of Misorientation Substrates on a GaAs/$Al_{0.3}Ga_{0.7}As$ Tunnel Diode" 2010 Taiwan Int'I Photovoltaic Exhibition

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[4] Chen-Chen Chung, **Hung-Wei Yu**, Li-Han Hsu, Chien-I Kuo, Nguyen-Hong Quan, Yu-Sheng Chiu and Edward Yi Chang, "The Effect of the Pattern of Circle-grid Electrode on Concentrated GaAs Solar Cells Efficiency" 2010 218th ESC meeting, Las Vegas.

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