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具高介電常數閘極絕緣層

之低溫多晶矽薄膜電晶體可靠度研究

Investigation on Reliability of LTPS-TFTs

With High-k Gate Dielectrics

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中華民國 九十八 年

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摘要

在本論文中，我們製造了具有高性能之P型通道的高介電常數閘極絕緣層的低溫薄膜電晶體並且探討其元件特性。為了能夠提升低溫薄膜電晶體的電性，我們採用二氧化鉿（HfO_2）作為閘極絕緣層以及引進新穎的結晶技術—金屬誘發側向結晶法(MILC)—來製作高性能之元件。高載子遷移率約 215 $cm^2/V-s$、優異次臨界斜率約 107 mV/decade 以及低臨界電壓約-0.75 V 可被得到而不需要任何的缺陷鈍化處理。

我們使用傳統直流(DC)電性量測技術來有系統地研究關於閘極負偏壓高溫應力(NBTI)劣化機制，分別對於使用固相結晶法(SPC)與金屬誘發側向結晶法(MILC)之二氧化鉿（HfO_2）的低溫薄膜電晶體。在本實驗中，我們使用先前在傳統二氧化矽(SiO2)上的閘極負偏壓高溫應力之經驗公式去分析高介電常數閘極絕緣層的劣化機制。在閘極負偏壓高溫應力劣化下，實驗結果顯示閘極負偏壓高溫應力(NBTI)的劣化主要是由於表面缺陷所造成，以及使用金屬誘發側向結晶法(MILC)比起使用固相結晶法(SPC)的元件在可靠度方面有著更加穩定的性質。

最後，汲極效應在閘極負偏壓高溫應力劣化機制下亦被探討。結果顯示汲極偏壓可以降低跨在閘極絕緣層的垂直電場，並且改善閘極負偏壓高溫應力所引起的元件劣化。從實驗資料中，我們建立了汲極效應在閘極負偏壓高溫應力劣化的理論模型。此模型與臨界電壓飄移(ΔV_{TH})有良好的吻合因此能夠証實我們的理論。

Investigation on Reliability of LTPS-TFTs With High-κ Gate Dielectrics

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Abstract

In this dissertation, high performance p-channel low temperature poly-silicon thin-film transistors (LTPS-TFTs) with high-κ gate dielectrics are fabricated and investigated. In order to enhance the characteristics of LTPS-TFTs, we adopted the employment of HfO_2 gate dielectric and the novel crystallization methods, metal-induced laterally crystallization (MILC), to fabricate high performance devices. High filed effect mobility μ_{FE} ~ 215 cm^2/V-s, ultra-low subthreshold swing S.S. ~ 107 mV/decade, and low threshold voltage V_{TH} ~ -0.75 V are derived from MILC-TFT with HfO_2 gate dielectric without any defect passivation methods.

Negative bias temperature instability (NBTI) degradation mechanism in solid-phase crystallization (SPC) and MILC LTPS-TFTs with HfO_2 gate dielectric has been studied systematically with a conventional DC measurement technique. We used the previously empirical formula for traditional NBTI in SiO_2 to analyze the high-κ gate dielectric in our experiment. The results showed that NBTI degradation is more dominated by the generation of interface trap states (N_{IT}) and the MILC transistors have more stability characteristic than SPC during the NBTI stress.

Finally, the drain bias effects on NBTI degradation mechanism is also investigated. The results showed that drain bias can reduced the vertical electric field

across gate dielectric and improved the NBTI-induced degradation. From experimental data, the NBTI model with drain bias effect is established. A good fit on the threshold voltage shift (ΔV_{TH}) prediction is obtained and confirms our theory.

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Chapter 1

Introduction

1.1 Overview of Polycrystalline Silicon Thin-Film Transistors

Thin film transistors (TFTs), which employ a thin semiconductor film on an insulating substrate as the active device channel, was first demonstrated in 1961 by Dr. P. K. Wenimer in RCA. With its simplicity in structure and fabrication, it becomes more and more popular for the application of thin film transistors in image sensors and displays. In recent years, the flat display are widely used in advanced electronic products, such as cellular phone, portable computer, digital camera, etc. In all types of flat-panel displays, active-matrix liquid crystal displays (AMLCDs) are one of the most promising candidates in high quality large-area flat-panel displays due to higher refresh rate compared with the conventional passive-matrix displays [1.1]-[1.3]. Besides, TFTs also has been investigated and developed on many electric components, such as static random access memory (SRAM), dynamic random access memory (DRAM) [1.4][1.5], and 3-D ICs' applications [1.6].

It has been known that hydrogenated amorphous silicon (α-Si:H) TFTs were widely used for the pixel switching device of AMLCDs in LCD industry [1.7]. There are many advantages on α-Si:H TFTs, such as their compatibility with low processing temperature on the large-area glass substrates and high off-stated impedance which result in low leakage current. However, its driving current and electron field effect mobility μ_{EF} is very low (below 1 $cm^2V^{-1}sec^{-1}$) to limit their application for AMLCDs technology only to the switching elements. It is very desirable to integrate the switching elements with the driver circuits together on the same substrate, because it is not only to reduce the cost but also to improve circuit and system reliability.

For this goal, polycrystalline silicon (poly-Si) TFTs has been proposed and

instead of amorphous silicon for the active element of LCDS [1.8]-[1.10]. Because the field effect mobility μ_{EF} and turn-on current in poly-Si is significantly higher than that in amorphous silicon, the poly-Si TFTs has a larger aperture ratio and higher panel resolution. However, there is a new problem for poly-Si TFTs. Low temperature process is must because the switch device is required to embed on the glass substrate for application of displays. For the general display-glass, maximum processing temperature needs to be kept below 600℃. Moreover, low temperature process also limits and affects other critical process steps, such as gate insulator formation and the activation of the doped regions of the device. These reasons imply that we should develop new technologies for low temperature polycrystalline-silicon thin-film transistor (LTPS-TFTs) [1.11]-[1.15].

Generally, growing poly-Si films by low temperature chemical vapor deposition (LPCVD) will get the small grain sizes and result in poor characteristics in ploy-Si TFTs. In order to further enhance TFTs characteristics, several techniques to increase the grain size of LTPS-TFTs have been proposed and developed, such as solid-phase crystallization (SPC) , excimer laser annealing (ELA), and metal-induced lateral crystallization (MILC) [1.16]-[1.18]. In addition, the performance of poly-Si TFTs is strongly influenced by defects such as dangling bonds and strained bonds located at the grain boundaries [1.19]. Those defects would trap carriers and generate a potential barrier which degrades the electrical properties. To reduce the impact of the existing defects, a good way is passivated them. Plasma treatment or passivation by ion implantation could effectively repair week bonds and create strong bonds, which can enhance the performance and reliability of LTPS-TFTs [1.19]-[1.33].

Recently, system-on-panel (SOP) and three-dimension integration of integrated circuit (3-D ICs) technology are attracting much attention to realize on LTPS-TFTs' applications. SOP means that to integrate the switching elements with the driver

circuits together on the same substrate [1.34]. It can help to reduce the cost and improve circuit and system reliability. The 3-D ICs' technology can enhance chip area which can reduce cost of TFT devices. Therefore, the idea of system-on-panel and three-dimension integration would be a novel development of semiconductor industry.

1.2 LTPS-TFTs with High-κ Gate Dielectric

Recently, low temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs) have been widely used in active-matrix liquid crystal displays (AMLCDs) due to their better performance in polysilicon than in amorphous silicon. For realizing system-on-panel (SOP) to LTPS-TFTs [1.34], integrating driving ICs on the glass substrate are required necessarily. Therefore, high-performance TFTs with high driving current I_{Dsat}, low gate leakage current I_G, low threshold voltage V_{TH} and excellently subthreshold swing S.S. are required.

For achieving this goal, a thin gate oxide be used to increase the gate capacitance density to enhance the driving current. However, scaling down the gate oxide may induce higher gate leakage current due to the thinner thickness of gate dielectric. In order to preserve the physical dielectric thickness while increasing the gate capacitance, several high-κ dielectrics have been proposed such as Al_2O_3, Ta_2O_5, Pr_2O_3, HfO_2, etc [1.35]-[1.38]. Among above-mentioned dielectric material, HfO_2 is one of the most potential candidates recently due to its high permittivity (14-20) and thermal stability with poly-Si. However, the high I_G may be resulted by higher temperature annealing due to poly-crystalline HfO_2 [1.39]-[1.41].

In addition, low quality deposited low-temperature SiO_2 (like PECVD-SiO_2) is generally employed as the gate dielectric of the conventional LTPS-TFTs. The poor interface between the gate dielectric and silicon substrate, due to the limitation of low temperature process, has been observed [1.11]-[1.15]. Comparing with low quality

SiO_2, low temperature deposited high-κ gate could have better interface quality and electrical characteristic. Unlike in single crystal Si MOSFET, there are maybe some differences in the world of LTPS-TFTs with high-κ gate dielectric.

1.3 Overview of Metal-Induced Lateral Crystallization

Low temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs) have been attracted to use in various fields such as active-matrix liquid crystal displays (AM-LCDs), solar cells, and three-dimensional (3-D) integrated circuit [1.6]. The fabricating high-performance LTPS-TFTs enables their use in a wide range of applications. Therefore, there is great interest in improving the performance of LTPS-TFTs. To fabricate large grain sizes of poly-Si on common glass substrate, the most widely used method is to deposit α-Si film and recrystallize by post-annealing, such as solid-phase crystallization (SPC) [1.42][1.43], excimer laser annealing (ELA) [1.44][1.45], and metal-induced lateral crystallization (MILC) [1.46][1.47]. In general, poly-Si layer was not founded using to deposit directly by low temperature chemical vapor deposition (LPCVD) because the grain size is too small compared to the size of transistor.

Conventionally, SPC is a common method of crystallizing α-Si. It has many advantages, such as simplicity, low cost and batch process. But the crystallization temperature is too high (around 600℃) for commercial glass substrates. By localizing the high temperature to the silicon layer, ELA can be considered a ‘‘low’’ temperature process. While it is capable of producing poly-Si film with low defect densities, it suffers from several problems such as high initial cost and high process complexity. Recently, metal-induced lateral crystallization (MILC) phenomenon was reported for successfully producing the low temperature (around 500℃) fabrication of high quality poly-Si films and high performance TFTs. This method is simple and can be

integrated into CMOS technology. Unlike ELA, MILC is a low cost batch process; unlike SPC, better quality poly-Si film due to its large grain size and longitudinal grain boundaries.

1.3.1 Development of History

When some metal are added into α-Si, the crystallization temperature can be lowered below 600℃, and this phenomenon is known as metal-induced crystallization (MIC). This has been reported for various metal and they can be classified into two groups. One is eutectic-forming metal such as Ag, Au, Al, Sb, and In; the other is silicide-forming metal such as Pd, Ti, Cu, and Ni. Among various metal, Ni has been shown to be the best candidate due to the $NiSi_2$ has a small lattice mismatch of 0.4% with c-Si [1.48]. However, device fabricated by MIC process has poor electrical properties because of metal contamination at the channel region. Beside, the grain size of MIC is too small. It is believed that the electrical properties of TFTs can be improved if the grain size of the poly-Si can be enhanced and number of grain boundaries in the channel region can be minimized.

Recently, a new method which can solve this problem called metal-induced lateral crystallization (MILC). This method is able to produce successfully large free region of metal contamination to poly-Si thin film while have better crystallization quality. MILC-TFTs have largely longitudinal grains and their boundaries are longer ‘‘parallel’’ with the flow of carriers [1.49]. Unlike SPC with a columnar grain structure randomly, there are many grain boundaries which are transverse to I_d. The presence of potential barrier cause the additional scattering at the grain boundaries and result in μ_{FE} degradation [1.50][1.51]. In addition, the laterally long grain size is over several tens of microns which are sufficient for the size of transistor.

Unfortunately, conventional symmetric MILC-TFTs structure ‘‘must’’ result in

the continuous grain boundaries across the channel [1.47][1.52]. They exist in the three parts: source and drain (S/D) junction edge near the channel and in the central region of channel. At the S/D junction edge, which is the overlap between MIC/MILC boundaries, has high density of grain boundary trap states and crystalline defects; there is also the same large defects in the central region between MILC/MILC boundaries. It has been known that PN-junction leakage current can arise by electron-hole pairs generated via grain boundary traps in the depletion region, particularly at drain edge of the channel. In order to solve this problem, removing the MIC/MILC boundaries from junction is necessary. Ni-offset TFT structure has been fabricated for this problem [1.52][1.53]. Although Ni-offset deposition method could exclude MIC/MILC boundaries from the edges of the channel, the MILC/MILC boundary remained at the center of channel.

Finally, a novel and smart technology called metal-induced unilateral crystallization (MIUC) is presently proposed [1.47][1.54]. MIUC not only retains the essentially longitudinal MILC grain structures, it also removes all major grain boundaries — including the MILC/MILC boundary — from the edges of junction and channel. Compared to the conventional MILC TFTs, the new MIUC devices are shown to have higher field effect mobility μ_{FE}, better subthreshold swing S.S. and significantly reduced leakage current [1.55]. All of these positive characters show that MIUC is a particularly suitable technology for system on penal (SOP) applications with low-temperature process TFTs.

1.3.2 Formation Mechanism

During the MIC annealing process (around 500℃), Ni deposited onto the seed window would diffuse into the α-Si film and react with silicon to from a nickel silicide ($NiSi_2$) . The $NiSi_2$ precipitates act as a good nucleus of Si, because which has

similar crystalline structure and small lattice mismatch of 0.4% with Si. Thus, α-Si under the silicide is crystallized into polysilicon during annealing process and this is called metal-induced crystallization (MIC) [1.56][1.57]. For the SPC process, it is typically carried out by furnace annealing around 600℃ because this temperature can permit to begin forming a steady-state of nucleation enough to crystallize. For this reason, adding some Ni into a-Si layer can lower the crystallization temperature below 600℃.

In the MIC region, there are many grains and grain boundaries at MIC polysilicon layer. These grain boundaries provide good locations for trapping the atoms. Due to the fast nickel diffusion in crystalline silicon structure and good nickel trapping property at the crystalline silicon to α-Si interface, most of Ni atoms in the MIC region diffuse to and are trapped at the grain boundaries. At the MIC/α-Si interface, the nickel silicide boundaries form and exist as a continuous sandwich layer between MIC/α-Si as illustrated in Fig. 1 and Fig. 2 [1.58]. This thin nickel silicide layer is called reactive grain boundary (RGB), which is responsible for the grain growth for MILC. During the continuous annealing after MIC, some of extra nickel atoms will diffuse and reach toward the front of RGB region. The nickel atoms will lower the activation energy of α-Si crystallization and react with lateral α-Si region to form the new silicide layer. Simultaneously, the silicon atoms are dissociate at the back of nickel silicide RGB and then form crystalline silicon (c-Si) region, which is the MILC polysilicon. The dissociated nickel atoms again diffuse to the α-Si region and construct the new nickel silicide continuously, which leads the shift of nickel silicide RGB and the growth of MILC polysilicon. As a result, the α-Si is crystallized to polysilicon in the lateral direction, and this process is called metal-induced lateral crystallization (MILC). The Ni content in the MILC area is about 0.02 atomic %, and the higher concentration is observed at RGB region (0.4%) and MIC region [1.58].

Crystallites are formed randomly by the background SPC during the MILC annealing process [1.59]. Although the temperature is below 600℃, the nucleation probably occurs due to the long annealing time. Once random crystallites are formed, an additional energy is required to break the crystalline bonding structure to restore α-Si atoms which can be recrystallized by MILC. The occurrence of SPC will let lateral crystallization slow down or even stop by the random polysilicon grains resulting from the SPC. Thus, the annealing temperature is the key for the longer lateral MILC polysilicon. Although a faster MILC rate can be accomplished by using a higher annealing temperature, the shorter maximum lateral crystallization length can also be obtained [1.59]. In addition, the MILC growth not only depend on the annealing temperature but also be affected by the dopant and thickness of silicon substrate [1.60][1.61].

1.4 Negative Bias Temperature Instability in LTPS TFTs

Negative bias temperature instability (NBTI) occur mainly in p-channel MOS device, which stressed with negative gate bias and elevated temperature. In general, devices will degrade during the long-time operation, and cause the system to fail. It obviously degraded electrical characteristic like an increase in absolute threshold voltage (V_{TH}) and degradations in drive current (I_D) or channel transconductance (G_M) [1.62][1.63]. As a results, we widely used the BTI stress to accelerate testing the device lifetime on the high electric field across gate dielectric. Typical stress temperature lie in the 100℃–250℃ range with oxide electric fields below 6MV/cm.

The NBTI-induced degradation is mainly attributed to the generation of interface trap states (N_{IT}) and can be partially recoverable once the stress bias is removed. This phenomenon has been interpreted by the reaction-diffusion (R-D) model [1.64][1.65]. During the stress, inversion layer holes interact with Si–H bonds and dissociated at

Si/SiO_2 interface. Subsequently, the released hydrogen species either diffuse away from the Si/SiO_2 interface and leaves behind Si– (N_{IT} generation), or reacts back with Si- and form Si–H (N_{IT} passivation). The N_{IT} generation will cause device degradation. In addition, some reports indicated that a portion of NBTI-induced degradation is recoverable [1.66][1.67]. This partially recoverable degradation is caused by hydrogenic depassivation (recombine with Si–) when the stress removed or reduced. The relaxation characteristics can be caused by the delay time between the end of stress and the V_{TH} measurement and $I_d - V_g$ measurement time, which may result in an erroneous estimation of a device lifetime.

Low-Temperature polycrystalline silicon thin film transistors (LTPS TFTs) are attracting much research interest as potential candidates for the realization of system on panel (SOP), which indicated LTPS TFTs must be designed using the COMS inverter configuration. During the COMS operation, p-channel TFT will be subjected to negative bias stress when input is at a low voltage level and output is at a high voltage level. Besides, it must be noted that the poor thermal conductivity of the glass substrate in LTPS TFTs. From the fabrication-technology point of view and as a long-term reliability concern, the stability of poly-Si TFTs is of significant importance. That are why the NBTI is important and interested in the reliability issues of LTPS TFTs.

In MOSFET, the NBTI degradation is mainly attributed to generation of interface trap states (N_{IT}). In LTPS TFTs, however, the extra defects and grain boundaries in the poly-Si channel region , more Si-H bonds existence due to CVD deposition process, and the poor quality at SiO_2/poly-Si interface by low temperature process limitation, may be different results that in MOSFETs. The main degradations in LTPS TFTs could divide into three parts: gate dielectric film, effective interfacial layer of SiO_2/poly-Si, and poly-Si channel film. For example, the carrier injection into the gate

dielectric would result in threshold voltage V_{TH} shift; the degradation of interfacial layer of SiO_2/poly-Si and channel film may cause low field effect mobility μ_{FE}, high subthreshold swing S.S. and drain leakage current I_{min}.

Besides, in order to enhance TFTs characteristics, numerous techniques to increase the grain size of poly-Si film have been proposed and developed, such as Solid-Phase Crystallization (SPC), Excimer Laser Crystallization (ELC) and Metal-Induced Lateral Crystallization (MILC) [1.42]-[1.47], but the compared reliability effects of them are rarely explored for LTPS TFTs. Furthermore, some hydrogen-related plasma treatments have been proposed to improve the electrical characteristics of TFTs. The improvement of TFTs is due to the defects passivation of grain boundaries and interface at SiO_2/poly-Si. Nevertheless, the introduction of hydrogen would result in the reliability issue.

For reasons mentioned above, the NBTI issue in LTPS TFTs is worthwhile to discuss closely. This subject will be discussed further in later chapters.

1.5 Reliability Issue on High-κ Gate Dielectric

Recently, several high-κ gate dielectrics have been investigated as replacements for the SiO_2 gate dielectric. It allows us keeping the same EOT to increase the physical thickness of the gate stack. Hence, the gate leakage is found to be reduced by 2 to 3 orders of magnitude [1.68]. Hafnium based dielectrics have been demonstrated as promising candidates for advanced high-κ gate stacks [1.68][1.69], and it was claimed that they are finally ready to be implemented in 45nm technology and beyond.

However, those high-k materials might not be sufficiently stable under the stress. Compared to SiO_2 , hafnium-based oxide showed a large amount of V_{TH} shift due to a high density of pre-existing structural defects, which be considered that crystallization

introduces grain into the gate stack and adds extra trap states [1.68]-[1.70]. These pre-existing traps cause the V_{TH} instability due to charge trapping/de-trapping phenomenon [1.71][1.72]. Some also reported that a thinner HfO_2 film demonstrates less V_{TH} shift due to less trapping in the bulk high-κ layer [1.69]. Consequently, one of the challenges in the implementation of these high-κ dielectrics is the stress-induced instability behavior.

In addition, similar to the conventional NBTI recovery in the high-κ dielectric, the lifetime evaluation methodology for the high-κ gate dielectrics may need to be redefined because a significant portion of the charge trapping/de-trapping in high-κ gate dielectric is observed [1.70][1.73]. Since the switching time between the stress and sense measurements and the sensing time are usually on the order of a second, conventional measurements would severely underestimate V_{TH} instability in high-κ devices. As a result, the single pulse I_d-V_g measurement technique [1.73][1.74] developed to minimize trap charging/discharging during stress interruption time has previously been applied to BTI studies.

1.6 Motivation

Recently, to realize system-on-panel (SOP) for LTPS-TFTs on the glass substrate are expected. In order to achieve high function integrated circuits, high-performance TFTs with high driving current, low gate leakage current, low threshold voltage V_{TH} and low subthreshold swing S.S. are required. However, it is the difficult challenge to develop high-performance devices for both pixel TFTs and driving circuits. For resolving this problem, we adopt novel crystallization method named metal-induced lateral crystallization (MILC) to enlarge poly-Si grain size to decrease the grain boundaries and defects. MILC is superior to conventional SPC due to it have a better quality poly-Si film. In addition, we also used the high-k material, HfO_2, to replace

the conventional SiO_2 as gate dielectric. A large gate capacitance density with the same physical thickness by using high-k gate dielectric can attract more carries with a smaller voltage to turn on the LTPS TFTs. By combining the two novel technologies, we expect to develop the high-performance devices on LTPS-TFTs.

Furthermore, we also study the reliability issues on high-performance LTPS-TFTs with HfO_2 gate insulator and MILC channel. For the viewpoint of produces, the long-term stability is significantly important. It has been reported that LTPS-TFTs suffer from several degradation mechanism, such as negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), hot-carrier stress (HCS), and so on. Therefore, the degradation characteristic and mechanism of LTPS-TFTs under dc stress test must be investigated for next-generation of panel application. However, reliability issues are still not thoroughly studied in LTPS-TFTs with HfO_2 gate dielectric. In addition, many circuit applications require transistors to operate at high drain bias in addition to a high gate bias. It was found that the BTI characteristics in MOSFETs are strongly affected by the drain bias (V_{DS}) during the stress. As a result, using the BTI stress to accelerate testing the device lifetime may cause an erroneous estimation of a device lifetime. Therefore, it is critical to understand the effect of drain bias on BTI degradation mechanism, and its impact on the circuit reliability at the operation condition.

In this work, we investigate the reliability mechanism of p-channel devices with HfO_2 gate dielectric. Besides, we also discuss differences between SPC and MILC LTPS-TFTs on degradation mechanism. Based on the experimental results, we hope to clarify the degradation characteristic and their mechanisms.

1.7 Dissertation Organization

In chapter 1, some backgrounds about LTPS TFT is introduced in this section : overview of poly-Si TFTs; LTPS TFTs with high-k gate dielectric; overview of metal-induced lateral crystallization; negative bias temperature instability in LTPS TFTs; and reliability issue on high-κ gate dielectric.

In chapter 2, we describe the device fabrication and the methods to extract the typical characteristic parameters of LTPS-TFTs in our experiment.

In chapter 3, electrical characteristics of high performance SPC and MILC p-channel LTPS-TFT with HfO_2 gate dielectric are characterized, for comparison.

In chapter 4, the NBTI degradation mechanism in LTPS TFTs with HfO_2 gate dielectric has been investigated with a conventional DC measurement technique. Besides, the reliability comparisons for SPC and MILC devices have been studied systematically.

In chapter 5, the drain bias effect on negative bias temperature instability (NBTI) degradation mechanism in low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) with high-k gate stack is analyzed by the DC measurement technique. In addition, the NBTI model with drain bias effect is established.

Finally, we conclude all experiments results briefly in chapter 6.

References

[1] S. Morozumi, K. Oguchi, S. Yazawa, Y. Kodaira, H. Ohshima, T. Mano, "B/W and color LC video display addressed by poly-Si TFTs," in *SID Tech.Dig.*, pp.156, 1983.

[2] R. E. Proano, R. S. Misage, D. Jones, D. G. Ast, "Guest-host active matrix liquid-crystal display using high-voltage polysilicon thin film transistors," *IEEE Trans. Electron Devices*, vol. 38, no.8, pp. 1781-1786, Aug. 1991.

[3] Y. Oana, "Current and future technology of low-temperature poly-Si TFT-LCDs," *J. Soc. Inf. Disp.*, 9, pp. 169, 2001.

[4] H. J. Cho, F. Nemati, P. B. Griffin, and J. D. Plummer, "A novel pillar DRAM cell for 4 Gbit and beyond," in *Dig. Symp. VLSI Tech.*, 1998, pp. 38-39.

[5] F. Hayashi, H. Ohkubo, T. Takahashi, S. Horiba, K. Noda, T. Uchida, T. Shimizu, N. Sugawara, and S. Kumashiro, "A highly stable SRAM memory cell with top-gated P-N drain poly-Si TFTs for 1.5 V operation," in *IEDM Tech. Dig.*, 1996, pp. 283-286.

[6] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: a noval chip design for improving deep-submicrometer interconnect performance and system-on-chip integration," *Proceedings of the IEEE*, vol.89, pp. 602-633,2001.

[7] P. Migliorate, "Progress in Active Matrix Addressing of LCDs", in *Pro. Int Display Res.Conf.*, pp.44, 1987.

[8] A. G. Lewis, D. D. Lee and R. H. Bruce, "Ploysilicon TFT Circuit Design and performance", *IEEE J. Solid-State Circuit*, vol.27, no.12, pp.1833, 1992.

[9] T. Morita, Y. Yamamoto, M. Itoh, H. Yoneda, Y. Yamane, S. Tsuchimoto, F. Funadda and K. Awane, "VGA Driving with Low Temperature Processed Poly-Si TFTs", *IEDM Tech.Dig*. pp.841, 1995.

[10] M. J. Edwards, S. D. Brotheton, J. R. Ayres, D. J. McCulloch and J. P. Gowers, "Laser Crystallized Poly-Si Circuits for AMLCDs", *Asia Display*, pp.335, 1955.

[11] G. K. Guist and T. W. Sigmon, "High-performance thin-film transistors fabricated using excimer laser processing and grain engineering," *IEEE Trans. Electron Devices*, vol. 45 pp. 925-932, Apr. 1998.

[12] Y. W. Choi, J. N. Lee, T. W. Jang, and B. T. Ahn, " Thin-film transistors fabricated with poly-silicon films crystallized at low temperature by microwave annealing," *IEEE Electron Device Lett.*, vol. 20, no. 1, pp. 2-4, Jan, 1999.

[13] C. W. Lin, M. Z. Yang, C. C. Yeh, L. J. Cheng, T. Y. Huan, H. C. Cheng, H. C. Lin, T. S. Chao, and C. Y. Chang, "Effects of plasma treatments, substrate types, and crystallization methods on performance and reliability of low temperature polysilicon TFTs," in *IEDM Tech. Dig.*, 1999, pp. 305-308.

[14] K. M. Chang, W. C. Yang, and C. P. Tsai, "Electrical characteristics of low temperature polysilicon TFT with a novel TEOS/oxynitride stack gate dielectric," *IEEE Electron Device Lett.*, vol. 24, no. 8, pp. 512-514, Aug. 2003.

[15] J. H. Jeon, M. C. Lee, K. C. Park, S. H. Jung, and M. K. Han, "A new poly-Si TFT with selectively doped channel fabricated by novel excimer laser annealing," in *IEDM Tech. Dig.*, 2000, pp. 213-216.

[16] T. W. Little, K. I. Takahara, H. Koike, T. Nakazawa, I. Yudasaka, and H. Ohshima, "Low temperature poly-Si TFT's using solid phase crystallization of very thin films and an electron cyclotron resonance chemical vapor deposition gate insulator," *Jpn. J. Appl. Phys.*, vol. 30, no. 12B, pp. 3724, 1991.

[17] H. Kuriyama, S. Kiyama, S. Nouguchi, et al, "Enlargement of poly-Si Film Grain Size by Excimer Laser Annealing and its Application to

High-Performance Poly-Si Thin Film Transistor", *Jpn. J. Appl. Phys.*, vol.30, no.12B, pp.3700-3703, 1991.

[18] S. W. Lee and S. K. Joo, "Low Temperature Poly-Si Thin Film Transistors Fabrication by Metal-Induced Lateral Crystallization", *IEEE Electron Device Lett.*, vol.17, no.4, pp.160-162, 1996.

[19] S. Seki, O. Kogure, and B. Tsujiyama, "Effects of Crystallization on trap state Densities at Grain Boundaries in Polycrstalline Silicon", *IEEE Electron Device Lett.*, vol.18, no.8, pp.368-370, 1987.

[20] H. N. Chern, C. L. Lee, and T. F. Lei, "The effects of H_2/O_2 plasma treatment on the characteristics of polysilicon thin-film transistors," *Electron Devices, IEEE Transactions on*, vol. 40, pp. 2301-2306, 1993.

[21] N. H. Nickel, P. Mei, and J. B. Boyce, "On the nature of the defect passivation in polycrystalline silicon by hydrogen and oxygen plasma treatments," *Electron Devices, IEEE Transactions on*, vol. 42, pp. 1559-1560, 1995.

[22] Y. J. Tung, J. Boyce, J. Ho, X. Huang, and T. J. King, "A comparison of hydrogen and deuterium plasma treatment effects on polysilicon TFT performance and dc reliability," *Electron Device Letters, IEEE*, vol. 20, pp. 387-389, 1999.

[23] I. W. Wu, A. G. Lewis, T. Y. Huang, and A. Chiang, "Effects of trap-state density reduction by plasma hydrogenation in low-temperature polysilicon TFT," *Electron Device Letters, IEEE*, vol. 10, pp. 123-125, 1989.

[24] F. S. Wang, M. J. Tsai, and H. C. Cheng, "The effects of NH_3 plasma passivation on polysilicon thin-film transistors," *Electron Device Letters, IEEE*, vol. 16, pp. 503-505, 1995.

[25] C. F. Yeh, D. C. Chen, C. Y. Lu, C. Liu, S. T. Lee, C. H. Liu, and T. J. Chen, "Highly reliable liquid-phase deposited SiO_2 with nitrous oxide plasma

post-treatment for low temperature processed poly-Si TFTs," *IEDM*, 1998.

[26] C. L. Fan, H. L. Lai, and T. H. Yang, "Enhanced crystallization and improved reliability for low-temperature-processed poly-Si TFTs with NH_3-plasma pretreatment before crystallization," *Electron Device Letters, IEEE*, vol. 27, pp. 576-578, 2006.

[27] C. W. Lin, M. Z. Yang, C. C. Yeh, L. J. Cheng, T. Y. Huang, H. C. Cheng, H. C. Lin, T. S. Chao, and C. Y. Chang, "Effects of plasma treatments, substrate types, and crystallization methods on performance and reliability of low temperature polysilicon TFTs," *IEDM*, pp. 305-308, 1999.

[28] C. K. Yang, T. F. Lei, and C. L. Lee, "Improved electrical characteristics of thin-film transistors fabricated on nitrogen implanted polysilicon films," *IEDM*, pp. 505-508, 1994.

[29] C. K. Yang, T. F. Lei, and C. L. Lee, "Characteristics of top-gate thin-film transistors fabricated on nitrogen-implanted polysilicon films," *Electron Devices, IEEE Transactions on*, vol. 42, pp. 2163-2169, 1995.

[30] C. K. Yang, T. F. Lei, and C. L. Lee, "Characteristics of Top-Gate Polysilicon Thin-Film Transistors Fabricated on Fluorine-Implanted and Crystallized Amorphous Silicon Films," *Journal of The Electrochemical Society*, vol. 143, pp. 3302-3307, 1996.

[31] C. H. Tu, T. C. Chang, P. T. Liu, C. H. Chen, C. Y. Yang, Y. C. Wu, H. C. Liu, L. T. Chang, C.-C. Tsai, S. M. Sze, and C. Y. Chang, "Electrical Enhancement of Solid Phase Crystallized Poly-Si Thin-Film Transistors with Fluorine Ion Implantation," *Journal of The Electrochemical Society*, vol. 153, pp. G815-G818, 2006.

[32] S. Maegawa, T. Ipposhi, S. Maeda, H. Nishimura, T. Ichiki, M. Ashida, O. Tanina, Y. Inoue, T. Nishimura, and N. Tsubouchi, "Performance and

reliability improvements in poly-Si TFT's by fluorine implantation into gate poly-Si," *Electron Devices, IEEE Transactions on*, vol. 42, pp. 1106-1112, 1995.

[33] H. N. Chern, C. L. Lee, and T. F. Lei, "The effects of fluorine passivation on polysilicon thin-film transistors, "*Electron Devices, IEEE Transactions on*, vol. 41, pp. 698-702, 1994.

[34] Z. Meng, M. Wang, and M. Wong, **"**High Performance Low temperature Metal-Induced Unilaterally Crystallized Polycrystalline Silicon Thin Film Transistors for System-on-Panel Applications,**"** *IEEE Trans. Electron Devices*, vol. 47, pp. 404-409, 2000.

[35] Z. Jin, H. S. Kwok, and M. Wong, "High-performance polycrystalline SiGe thin-film transistors using Al_2O_3 gate insulators," *Electron Device Letters, IEEE*, vol. 19, no. 12, pp. 502-504, 1998.

[36] M. Y. Um, S.-K. Lee, and H. J. Kim, "Characterization of thin film transistor using Ta2O5 gate dielectric," in *Proc. Int. Workshop AM-LCD*, Tokyo, Japan, pp.45-46, 1998.

[37] C. W. Chang, C. K. Deng, J. J. Huang, H. R. Chang, and T. F. Lei, "High-performance Poly-Si TFTs With Pr_2O_3 Gate Dielectric," *Electron Device Letters, IEEE*, vol. 29, no. 1, pp. 96-98, 2008.

[38] C. P. Lin, B. Y. Tsui, M. J. Yang, R. H. Huang, and C. H. Chien, "High-performance Poly-Si TFTs With Using HfO_2 Gate Dielectric," *Electron Device Letters, IEEE*, vol. 27, no. 5, pp. 360-363, 2006.

[39] G. Ribes, J. Mitard, M. Denais, "Review on high-κ dielectrics reliability issues," *IEEE Trans. Electron Device and Materials Reliability*, vol. 5, no. 1, pp. 5-19, 2005.

[40] A. Neugroschel , G. Bersuker , R. Choi , "An accurate lifetime analysis

methodology incorporating governing NBTI mechanisms in high-k/SiO_2 gate stacks," *IEDM Tech. Dig.*, pp. 317, 2006

[41] R. Choi, C. Young, Y. K. Chang, D. Heh, G. Bersuker, S. Krishnan, R. P. Kirsch, A. Neugroschel, S. C. Song, B. H. Lee, R. Jammy, "Reliability Assessment on Highly Manufacturable MOSFETs with Metal Gate and Hf based Gate Dielectrics," Physical and Failure Analysis of Integrated Circuits, IPFA 2007. 14^{th}.

[42] E. Ibok and S. Garg, "A characterization of the effect of deposition temperature on polysilicon properties," *J. Electrochem. Soc.*, vol. 140, pp. 2927-2937, Oct. 1993.

[43] T. W. Little, K. I. Takahara, H. Koike, T. Nakazawa, I. Yudasaka, H. Ohshima, "Low temperature poly-Si TFT's using solid phase crystallization of very thin films and an electron cyclotron resonance chemical vapor deposition gate insulator," *Jpn. J. Appl. Phys.*, vol. 30, no. 12B, pp. 3724, 1991.

[44] N. Kubo, N. Kusumoto, T. Inushima, and S. Yamazaki, "Characterization of polycrystalline-Si thin film transistors fabricated by excimer laser annealing method," *IEEE Trans. Electron Devices*, vol. 41, pp. 1876-1879, Oct. 1994.

[45] H. Kuriyama, S. Kiyama, S. Naguchi, T. Kuwahara, S. Ishida, T. Nahda, K. Sano, K. Iwata, S. Tsuda, and S. Nakano, "High mobility poly-Si TFT by a new Excimer laser annealing method for large area electronics," in *IEDM Tech. Dig.*, 1991, pp. 563.

[46] S. W. Lee and S. K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 17, no. 4, pp. 160-162, Apr. 1996.

[47] Z. Meng, M. Wang, and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film

transistors for system-on-panel applications," *IEEE Trans. Electron Devices*, vol. 47, no. 2, pp. 404-409, 2000.

[48] T. K. Kim, G. B. Kim, B. I. Lee, S. K. Joo, "The effects of electrical stress and temperature on the properties of polycrystalline silicon thin-film transistors fabricated by metal induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 21, no. 7, pp. 347-349, 2000.

[49] M. Wang, Z. Meng, and M. Wong, "Anisotropic conduction behavior in metal-induced laterally crystallized polycrystalline silicon thin films," *Applied Physics Letter*, vol. 76, no. 4, pp. 448, 2000.

[50] G. A. Bhat, Z. Jin, H. S. Kwok, M. Wong, "Effects of longitudinal grain boundaries on the performance of MILC-TFTs," *Electron Device Letters, IEEE*, vol. 20, no. 2, pp. 97-99, 1999.

[51] V. W. C. Chan, P. C. H. Chan, Y. Chunshan, "The effects of grain boundaries in the electrical characteristics of large grain polycrystalline thin-film transistors," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1384-1391, 2002.

[52] M. Wong, Z. Jin, G. A. Bhat, P. C. Wong, H. . Kwok, "Characterization of the MIC/MILC interface and its effects on the performance of MILC thin-film transistors," *IEEE Trans. Electron Devices*, vol. 47, no. 5, pp. 1061-1067, 2000.

[53] G. B. Kim, Y. G. Yoon, M. S. Kim, J. Hunjoon, S. W. Lee, S. K. Joo, "Electrical characteristics of MILC poly-Si TFTs with long Ni-offset structure," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2344-2347, 2003.

[54] M. Wang and M. Wong, "Characterization of an individual grain boundary in metal-induced laterally crystallized polycrystalline silicon thin-film devices," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1655-1660, 2001.

[55] M. W. Ma, T. S. Chao, C. J. Su, W. C. Wu, K. H. Kao, T. F. Lei, "High-Performance Metal-Induced Laterally Crystallized Polycrystalline Silicon P-Channel Thin-Film Transistor With TaN/HfO_2 Gate Stack Structure," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 592-594, 2008.

[56] S. Y. Yoon, S. K. Kim, J. Y. Oh, Y. J. Choi, W. S. Shon, C. O. Kim, J. Jang, "A High-Performance Polycrystalline Silicon Thin-Film Transistor Using Metal-Induced Crystallization with Ni Solution," *Jpn. J. Appl. Phys.*, vol.37, pp.7193-7197, 1998.

[57] S. Y. Yoon, S. J. Park, K. Ho Kim, "Metal-induced crystallization of amorphous silicon," Thin Solid Films, Volume 383, Issues 1-2, pp. 34-38, 2001

[58] C. F. Cheng, V. M. C. Poon, C. W. Kok, M. Chan, "Modeling of Grain Growth Mechanism by Nickel Silicide Reactive Grain Boundary Effect in Metal-Induced-Lateral-Crystallization," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1467-1472, 2003.

[59] C. F. Cheng, T. C. Leung, M. C. Poon, C. W. Kok, M. Chan, "Modeling of Large-Grain Polysilicon Formation Under Retardation Effect of SPC," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2205-2210, 2004.

[60] T. Ma, M. Wong, "Dopant and thickness dependence of metal-induced lateral crystallization of amorphous silicon films," *J. Appl. Phys.*, vol.91, no. 3, pp. 1236-1241, 2002

[61] T. K. Chang, C. W. Lin, Y. H. Chang, C. H. Tseng, F. T. Chu, H. C. Cheng, L. J. Chou, "Thickness Dependence of Microstructure of Laterally Crystallized Poly-Si Thin Films and Electrical Characteristics of Low-Temperature Poly-Si TFTs," *Journal of The Electrochemical Society*, vol. 150, pp.G494-G497, 2003.

[62] C. Y. Chen, J. W. Lee, S. D. Wang, M. S. Shieh; P. H. Lee; W. C. Chen; H. Y.

Lin; K. L. Yeh; T. F. Lei, "Negative Bias Temperature Instability in Low-Temperature Polycrystalline Silicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2993-3000, 2006.

[63] C. Y. Chen, M. W. Ma, W. C. Chen, H. Y. Lin, K. L. Yeh, S. D. Wang, T. F. Lei, **"**Analysis of Negative Bias Temperature Instability in Body-Tied Low-Temperature Polycrystalline Silicon Thin-Film Transistors**,"** *IEEE Electron Device Lett.*, vol. 29, no. 2, pp. 165-167, 2008.

[64] Souvik Mahapatra, P. Bharath Kumar, and M. A. Alam "Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of pMOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 1371-1379, 2004.

[65] A. T. Krishnan, S. Chakravarthi, P. Nicollian, V. Reddy, S. Krishnan, "Negative bias temperature instability mechanism: The role of molecular hydrogen," *Applied Physics Letter*, 88, 153518, 2006.

[66] S. Rangan, N. Mielke, E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability," *IEDM*, pp. 341-344, 2003.

[67] M. A. Alam, "A critical examination of the mechanics of dynamic NBTI for PMOSFETs," *IEDM*, pp. 345-348, 2003.

[68] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, G. Ghibaudo, "Review on high k dielectrics reliability issues," *IEEE Trans. Electron Device and Materials Reliability*, vol. 5, no. 1, pp. 5-19, 2005.

[69] R. Choi, C. Young, Y. K. Chang, D. Heh, G. Bersuker, S. Krishnan, R. P. Kirsch, A. Neugroschel, S. C. Song, B. H. Lee, R. Jammy, "Reliability Assessment on Highly Manufacturable MOSFETs with Metal Gate and Hf based Gate Dielectrics," Physical and Failure Analysis of Integrated Circuits, IPFA 2007. 14th.

[70] A. Neugroschel , G. Bersuker , R. Choi, C. Cochrane, P. Lenahan, D. Heh, C. Young, C. Y. Kang, B. H. Lee, R. Jammy, "An accurate lifetime analysis methodology incorporating governing NBTI mechanisms in high-k/SiO_2 gate stacks," *IEDM Tech. Dig.*, pp. 317, 2006.

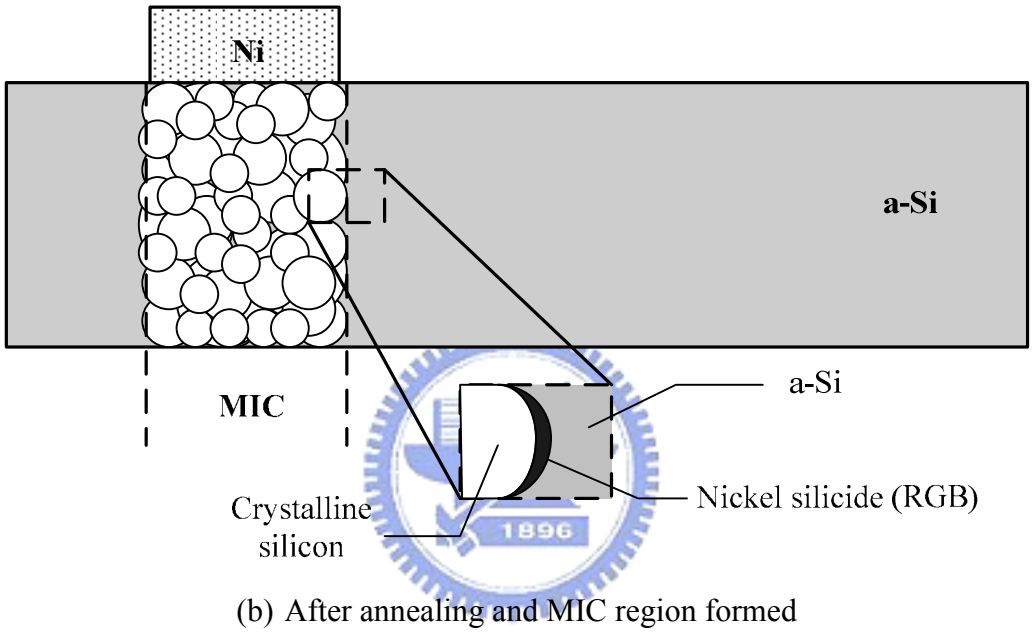
[71] D. Heh, C. D. Young, and G. Bersuker, "Experimental Evidence of the Fast and Slow Charge TrappingDetrapping Processes in High-k Dielectrics Subjected to PBTI Stress," *IEEE Trans. Electron Devices*, vol. 29, no. 2, pp. 180-182, 2008.

[72] R. Choi, S. J. Rhee, J. C. Lee, B. H. Lee, G. Bersuker, "Charge trapping and detrapping characteristics in hafnium silicate gate stack under static and dynamic stress," *IEEE Trans. Electron Devices*, vol. 26, no. 3, pp. 197-199, 2005.

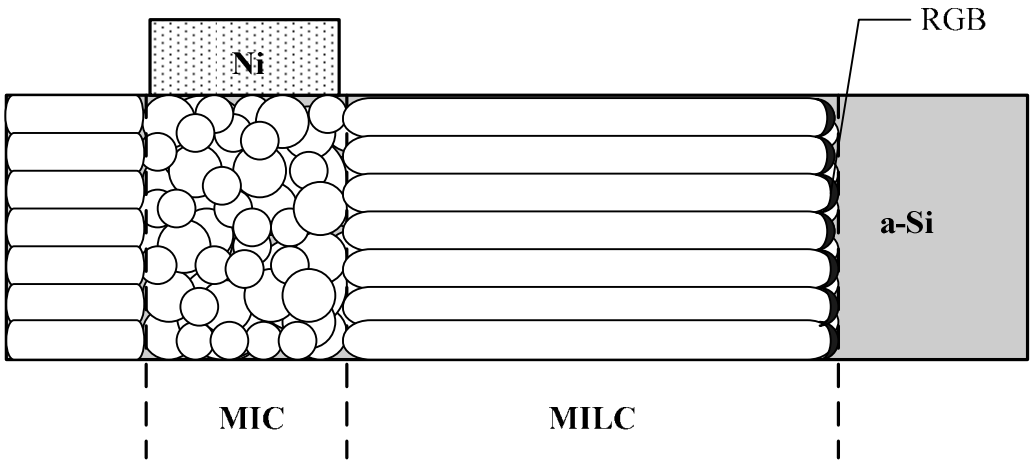
[73] D. Heh, R. Choi, C. D. Young, G. Bersuker, "Fast and slow charge trappingdetrapping processes in high-k nMOSFETs.," Integrated Reliability Workshop Final Report, 2006.

[74] R. Choi, S. C. Song, C. D. Young, G. Bersuker, "Charge trapping and detrapping characteristics in hafnium silicate gate dielectric using an inversion pulse measurement technique," *Applied Physics Letter*, 87, 122901, 2005.

(a) Before annealing



(b) After annealing and MIC region formed



(c) After annealing and MILC region formed

Fig. 1. MILC polysilicon formation during annealing process.

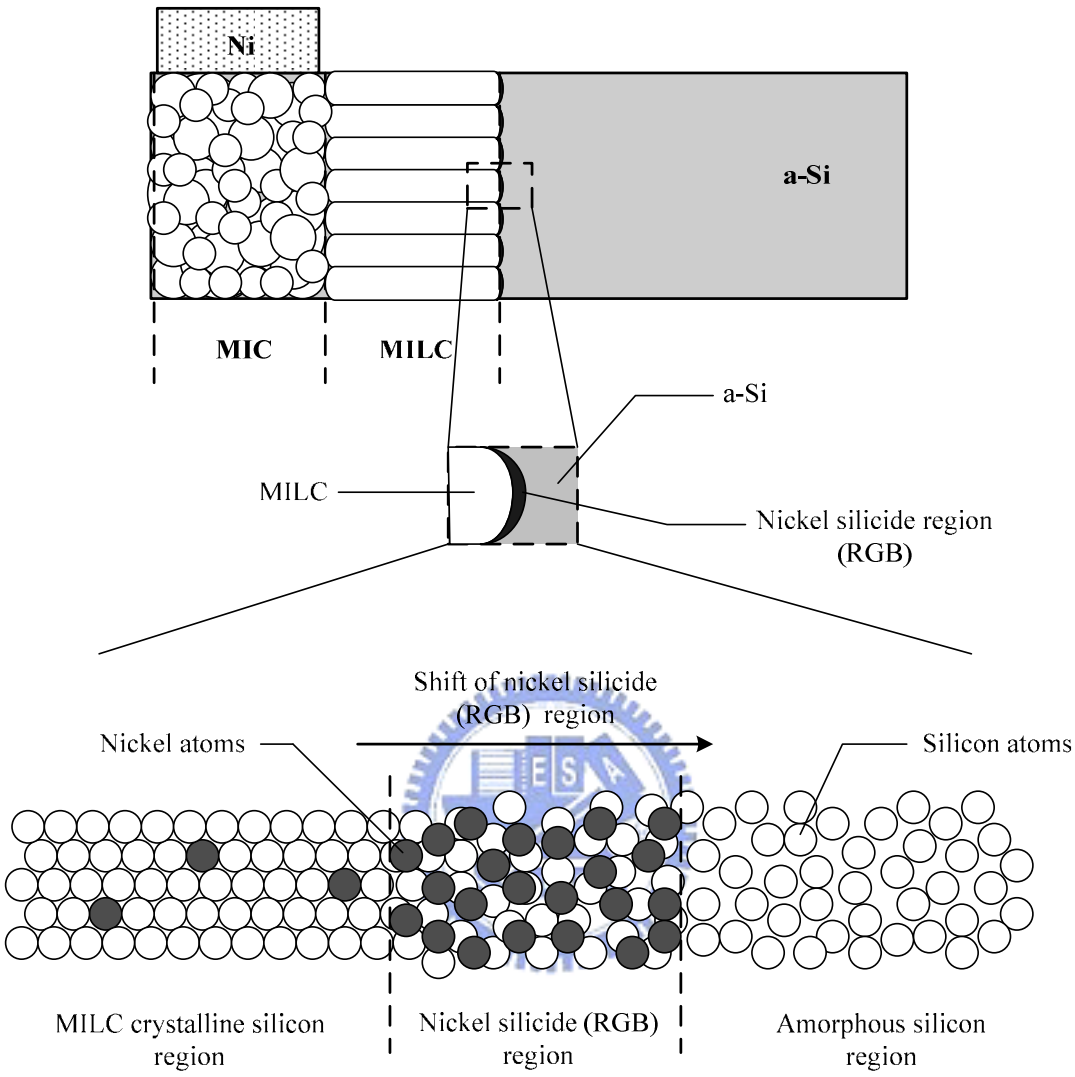


Fig. 2. MILC polysilicon formation mechanism.

Chapter 2

Device Fabrication and Method of Parameter Extraction

In this thesis, high performance p-channel low temperature poly-silicon thin-film transistors (LTPS-TFTs) are fabricated by the employment of HfO_2 gate dielectric and two crystallization methods, solid phase crystallization (SPC) and metal-induced laterally crystallization (MILC), for comparison. In addition, we will introduce the methods to extract the typical characteristic parameters of LTPS-TFTs, such as threshold voltage V_{TH}, subthreshold swing S.S., drain current *ON/OFF* ratio, field effect mobility μ_{EF}, and the trap state density N_{trap}. All the electrical characteristics were measured by Keithley 4200-SCS.

2.1 Device Fabrication

As shown in Fig.1 and Fig.2, the fabrication of devices started by depositing a 50-nm undoped amorphous Si (α-Si) layer at 550°C and 120m torr in a low-pressure chemical vapor deposition system on Si wafers capped with a 500-nm thermal oxide layer. For SPC LTPS-TFT, the 50-nm α-Si layer was crystallized by SPC process at 600°C for 24-h in a N_2 ambient. For MILC LTPS-TFT, a 5-nm Ni was deposited by electron-beam evaporation system at room temperature, 10^{-6} torr base pressure and 10^{-5} torr process pressure, and patterned by lift-off process as a seed layer to crystallize the α-Si. Then the 50-nm α-Si layer was crystallized by MILC process at 550°C for 24-h in a N_2 ambient, and the residual Ni was removed by $H_2SO_4 + H_2O_2$ solution. Here, both SPC and MILC poly-silicon channel films have been formed. Then a 500-nm plasma-enhanced chemical vapor deposition (PECVD) oxide was deposited at 300°C for device isolation. The device active region was formed by patterning and etching the isolation oxide. The source and drain regions (S/D) in the

active device region was implanted with boron (10 keV at 5 x 10^{15} cm^{-2}). The S/D was activated at 600°C for 24-h annealing in a N_2 ambient. A 50-nm HfO_2 was deposited by electron-beam evaporation system at room temperature, 10^{-6} torr base pressure and 10^{-5} torr process pressure. An O_2 annealing in furnace was applied to improve the HfO_2 at 400°C for 30-min. In order to compare the HfO_2 gate dielectric, a 50-nm PECVD SiO_2 was also deposited at 300°C in SPC poly-silicon channel film. After the patterning of S/D contact holes, aluminum was deposited by thermal evaporation system at room temperature, 10^{-6} torr base pressure and 10^{-5} torr process pressure, as the gate electrode and S/D contact pad. Finally, the TFT devices were completed by the contact pad definition. All process flow is shown in Fig. 1 and Fig.2 . Devices with gate width (W) and length (L) of 10μm /10μm are measured.

2.2 Method of Parameter Extraction

2.2.1 Determination of Threshold Voltage

Threshold voltage V_{TH} is an important parameter of semiconductor devices. However, various definitions for V_{TH} have been proposed on different types of device. In MOSFET, there are two common methods for determination of V_{TH}. One is the linear extrapolation method, which is defined in "linear-scale" I_D-V_{GS} curves at a low drain voltage (50~100mV). According to ideal I_D vs. V_{GS} equation

$$I_D = k\left[(V_{GS} - V_{TH}) - \frac{1}{2}(V_{DS} - I_D R_{SD})\right](V_{DS} - I_D R_{SD}) \quad (1)$$

$$\cong k\left[V_{GS} - V_{TH} - \frac{1}{2}V_{DS}\right](V_{DS}) \quad (2)$$

We have to note that equation (2.2) is accurate only for negligible series resistance like source and drain resistance R_{SD}, which can be generally negligible at the low drain current (or low drain voltage). V_{TH} is defined from the extrapolation of

$G_{m,max}$, which is common practice to find the point of maximum slope of the I_{DS}-V_{GS} curve ($\text{slope} = \frac{\partial I_D}{\partial V_{GS}} = G_m$) and fit a straight line to extrapolate at I_D=0. The real I_D-V_{GS} curve deviates from a straight line at gate voltage below V_{TH} due to subthreshold current, and above V_{TH} due to series resistance and mobility degradation effect. Hence the V_{TH} is determined from the extrapolated intercept of gate voltage (V_{GS}) at I_D=0 by

$$V_{TH} = V_{GS} - \frac{V_{DS}}{2} \quad (3)$$

In our thesis, V_{TH} is defined differ from above description and is defined by more simply way which called *constant drain current method*. This method can be found in almost the papers relate to poly-Si TFTs. The V_{TH} obtained from this way is close to the another extracted from linear extrapolation method. Here, constant drain current is fixed to when I = (W/L)*100 nA for p-channel at V_{DS}=|0.1|V and W, L are channel width and length respectively. In this thesis, devices were all measured by W=10 μm, L=10 μm. Thus, Ids was fixed to 10^{-7} A in all our discussion.

2.2.2 Determination of Subthreshold Swing

Subthreshold slope (S.S.) is a typical parameter to describe the control ability of gate toward channel, which reflects the turn on/off speed of a device. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude.

The S.S. should be independent of drain voltage and gate voltage. In reality, however, the S.S. increases with drain voltage due to channel shortening effect such as charge sharing, avalanche multiplication and punchthrough effect. The subthreshold slope is also related to gate voltage due to undesirable and inevitable factors such as the serial resistance and interface states. In LTPS-TFTs, the

subthreshold swing is also dependent on defects and grain boundaries in ploy-Si channel films. It has been reported that S.S. be closely related to the trap states located near the mid-gap (deep states), which originate from dangling bonds [2.1]. Besides, because of the limitation of low temperature process, the poor interface between the gate dielectric and silicon substrate has been observed. Both bulk and interface traps would make poor S.S. in LTPS-TFTs. The formula of subthreshold slope were defined as

$$S.S. = [\frac{\partial(logI_{DS})}{\partial V_{GS}}]^{-1} \quad (4)$$

In our thesis, the S.S. is defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude. In some of stress conditions, the S.S. is defined as one of the gate voltage required to decrease the threshold current by one orders due to the poor *On/Off* current ratio.

2.2.3 Determination of On/Off Current Ratio

Drain *On/Off* current ratio is another important factor of TFTs. High *On/Off* ratio represents not only large turn-on current but also small off current (or leakage current). For large-scale AMLCD Pixel-TFTs, large I_{on} is required to fast charge C_{pixel} within 1 line time (generally demanded $\geqq 10^{-6}$ A), and small I_{off} to maintain voltage on C_{pixel} for 1 frame time ($\leqq 10^{-12}$ A). As a result, we generally request that *On/Off* ratio can large than 10^6.

In our thesis, the on current is defined as the drive current when gate voltage at the maximum value and drain voltage fixed to |0.1V|. The off-current is specified as the minimum current when drain voltage equals to |0.1V|. Drain *On/Off* current ratio can be given as following

$$\frac{I_{on}}{I_{off}} = \frac{Maximum\ Drain\ Current\ at\ V_d=|0.1V|}{Minimum\ Drain\ Current\ at\ V_d=|0.1V|} \quad (5)$$

2.2.4 Determination of Field Effect Mobility

Usually, field effect mobility (μ_{eff}) is determined from the maximum value of transconductance (G_m) at low drain bias. The transfer characteristics of Poly-Silicon TFTs are similar to those of conventional MOSFETs, so that the first order of I-V relation in the bulk Si MOSFETs can be applied to Poly-Silicon TFTs. The drain current in linear region ($V_{DS} < V_{GS} - V_{TH}$) can be approximated as the following equation:

$$I_{DS} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}{V_{DS}}^2\right] \quad (6)$$

where W and L are channel width and channel length, respectively. C_{ox} is the gate oxide capacitance per unit area and V_{TH} is the threshold voltage. Thus, the transconductance is given by

$$G_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) V_{DS} \quad (7)$$

Therefore, the field-effect mobility is

$$\mu_{eff} = \frac{L}{C_{ox} W V_{DS}} G_{m(max)}\Big|_{V_{DS} \to 0} \quad (8)$$

2.2.5 Determination of The Trap Density

In LTPS-TFTs, the trap state density (N_t), which originate from dangling binds or strained bonds ,located in the grain boundaries of poly-Si film. It will trap carrier and generate barrier height V_B to degrade carriers transportation like reduction of field effect mobility (μ_{eff}). Besides, it also make higher threshold voltage V_{TH}, subthreshold swing S.S., and leakage current. Because the electrical transport properties of poly-Si films are strongly influenced by carrier trapping at the grain boundaries, we can base on this mechanisms to extract the trap state density (N_t) from the I_D-V_{GS} characteristics of poly-Si TFTs .

Many researchers have studied the electrical characteristics and carrier transport in poly-Si TFTs [2.2] [2.3]. According to the sample grain boundary trapping model, Seto et al. have successfully used this model to describe the dependence of the conductivity of poly-Si on trap density in 1975 [2.2]. They defined the barrier height V_B and developed the current transport mechanisms by thermionic emission over the barrier. Later, Levinson in 1982 based on the Seto model to propose the basic current equation of poly-Si TFTs, which assumed that scattering of carriers take place only at grain boundaries [2.4]. By modifying the mobility μ_b and replacing the doping concentration with gate induced charge density N_G, the correct expression for the I-V characteristics at low drain voltage in poly-Si TFTs is very similar to that in regular MOSFET's. It is given by

$$I_D = \mu_0 C_{ox} \frac{W}{L} (V_G - V_{TH}) V_D \, exp\left(-\frac{q^3 N_t^2 t_{ch}}{8kT\varepsilon_s C_{ox}(V_G - V_{TH})}\right) \quad (9)$$

This equation had been further corrected by Proano et al. in 1989 [2.5]. It is found that the behavior of carrier mobility under low gate bias can be expressed more correctly by using the flat-band voltage V_{FB} instead of the threshold voltage V_{TH}. The flat-band voltage V_{FB} is defined as the gate voltage at minimum leakage current occur. Furthermore, Levinson assumed that the channel thickness was constant and equal to the thickness of poly-Si film $t_{poly\text{-}Si}$. This simplifying assumption is permissible only for very thin film (t<10nm), which is not applicable to common thickness for poly-Si TFTs. A better approximation for channel thickness t_{ch} in an undoped poly-Si film is given by defining the channel thickness as the thickness at which 80% of the total charge resides. Therefore, by solving the Poisson's equation, the channel thickness is given by

$$t_{ch} = \frac{8kT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}(V_G - V_{FB})} \quad (10)$$

Substituting above modificatory terms into the (2-9), and the I_D current of poly-Si TFTs can be expressed as

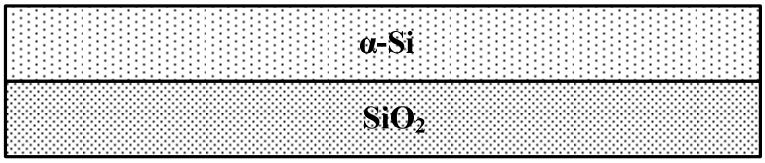
$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{FB})V_D \; exp\left(-\frac{q^2 N_t^2 \sqrt{\varepsilon_{ox}/\varepsilon_s}}{C_{ox}{}^2 (V_G - V_{FB})^2}\right) \quad (11)$$

According to equation (2-11), we can extract the trap state density (N_t) from the slope of the curve $\ln[I_D/(V_G-V_{FB})]$ versus $(V_G-V_{FB})^{-2}$. The effective grain boundary trap state density N_t can be determined from the square root of the slope

$$N_{trap} = \frac{C_{ox}}{q}\sqrt{|slope|} \quad (12)$$

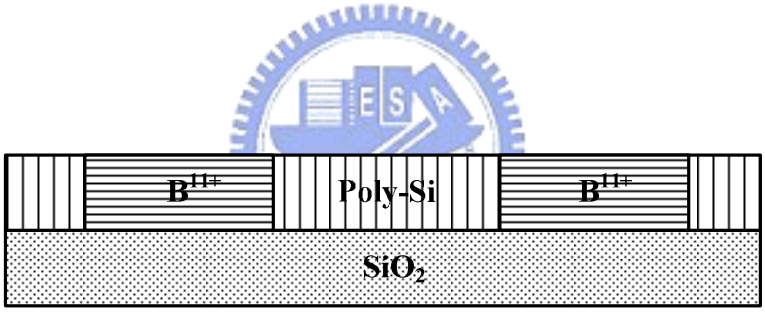
References

1. I. W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis, A. Chiang, “Passivation Kinetics of Two Types of Defects in Polysilicon TFT by Plasma Hydrogenation,” *IEEE Electron Device Lett.*, vol. 12, no. 4, pp. 181-183, 1991.
2. J. Y. W. Seto, “The electrical properties of polycrystalline silicon films,” *J. Appl. Phys.*, vol.46, no. 12, pp. 5247-5254, 1975.
3. G. Baccarani and B. Riccò, “Transport properties of polycrystalline silicon films,” *J. Appl. Phys.*, vol.49, pp. 5565, 1978.
4. J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, M. Rider, “Conductivity behavior in polycrystalline semiconductor thin film transistors,” *J. Appl. Phys.*, vol.53, pp. 1993, 1982.
5. R. E. Proano, R. S. Misage, D. G. Ast, “Development and electrical properties of undoped polycrystalline silicon thin-film transistors,” *IEEE Trans. Electron Devices,* vol. 36, no. 9, pp. 1915-1922, 1989.

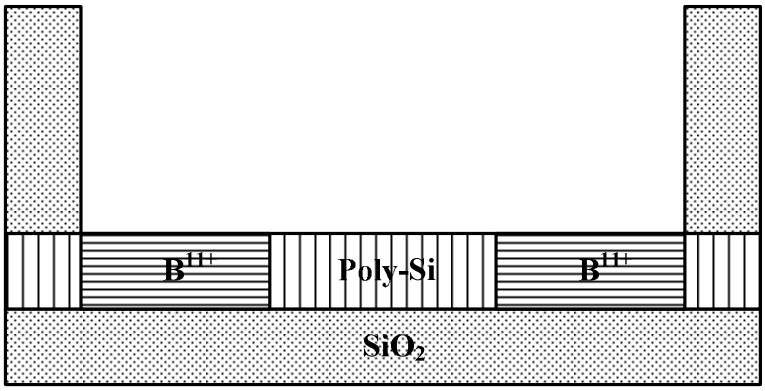


(a) Thermal oxidation and amorphous Si (α-Si) deposited by LPCVD

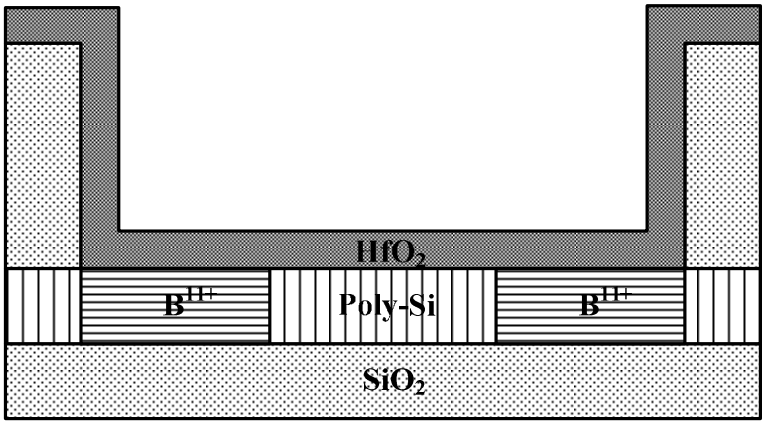
(b) Crystallization of α-Si film into poly-Si by SPC



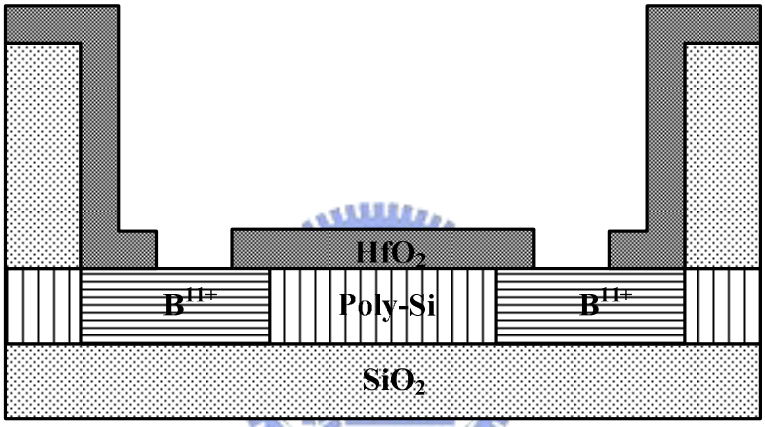
(c) The source and drain regions (S/D) was implanted with boron and activated



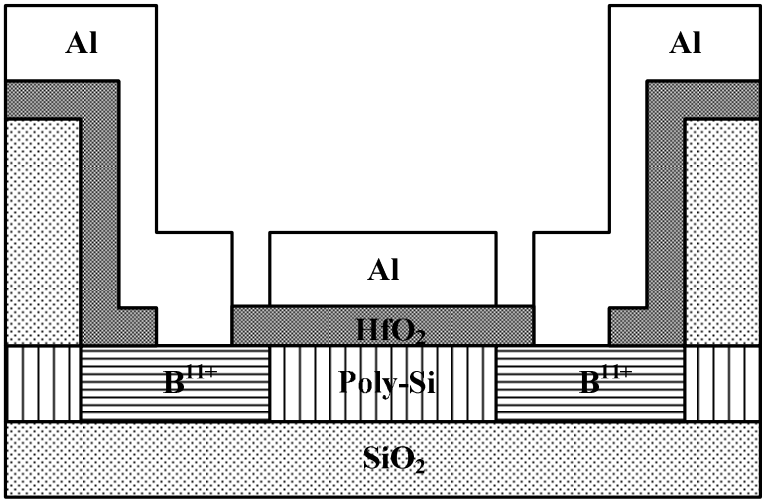
(d) SiO_2 deposited by PECVD and active region defined



(e) Deposition of HfO_2 gate dielectric and patterning



(f) Contact holes of S/D opened

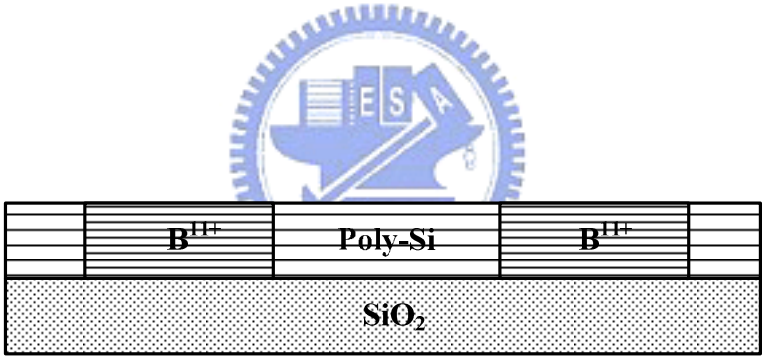


(g) Aluminum was deposited and gate electrode and S/D contact pad formed

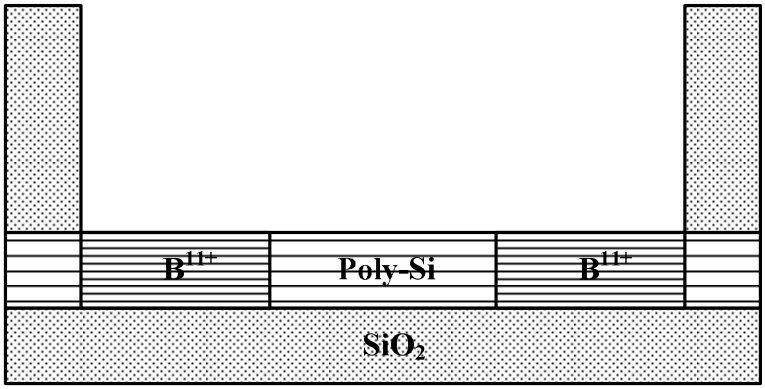
Fig. 1. The process flow of SPC LTPS-TFTs with HfO_2 gate dielectric.

(a) Thermal oxidation, amorphous Si (α-Si) and Ni deposited

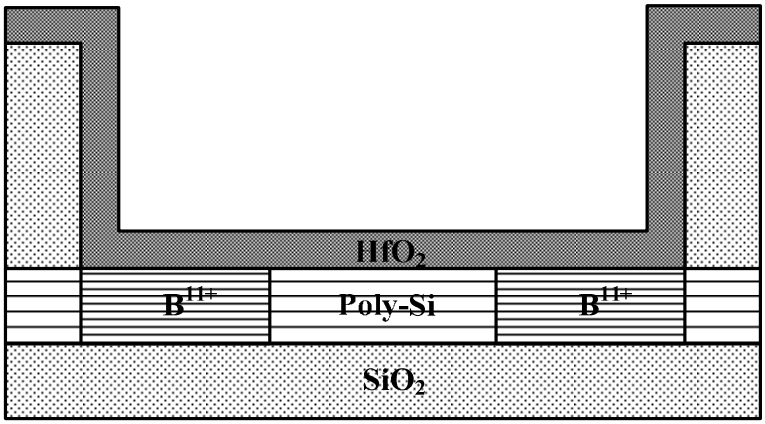
(b) Crystallization of α-Si film into poly-Si by MILC



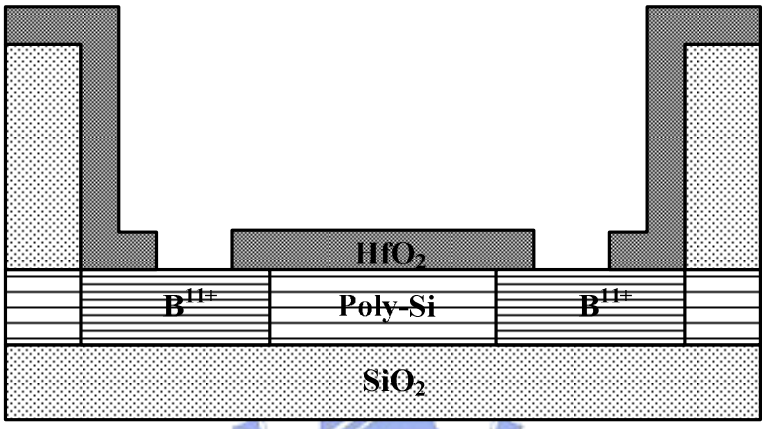
(c) Removed Ni, and S/D was implanted with boron and activated



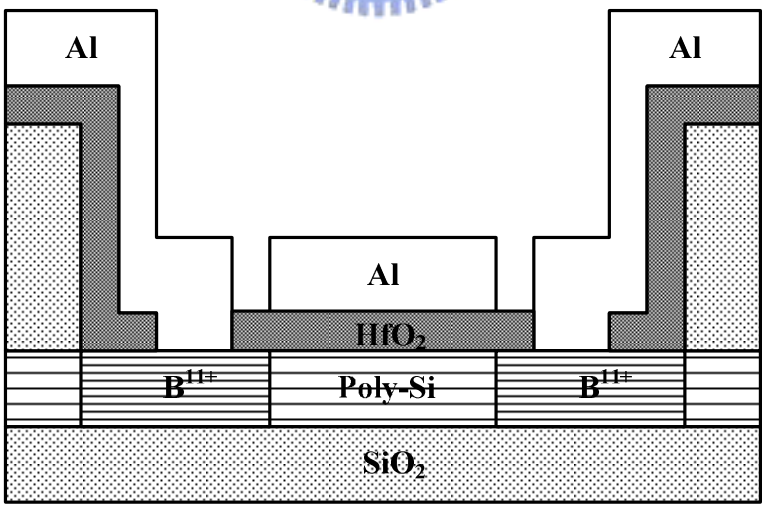
(d) SiO_2 deposited by PECVD and active region defined



(e) Deposition of HfO_2 gate dielectric and patterning



(f) Contact holes of S/D opened



(g) Aluminum was deposited and gate electrode and S/D contact pad formed

Fig. 2. The process flow of MILC LTPS-TFTs with HfO_2 gate dielectric.

Chapter 3
Electrical Characteristics of High Performance SPC and MILC P-Channel LTPS-TFT with High-κ Gate Dielectric

3.1 Introduction

High performance low temperature poly-silicon thin-film transistors (LTPS-TFTs) are mostly used as the pixel driving devices of active-matrix liquid crystal display (AMLCD) [3.1][3.2]. In order to achieve high switch speed of AMLCD, high driving current of LTPS-TFTs is required. However, there are many defects exist among the poly-silicon channel film because of many grain boundaries, resulting in much lower field effect mobility μ_{FE}, poor subthreshold swing S.S. and high threshold voltage V_{TH} [3.3]-[3.5]. Generally, two main ways are adopted to improve the performance of LTPS-TFTs. One way is the passivation of defects, such like plasma treatment or ion implantation treatment to inactive or passivate the defects of poly-silicon channel film [3.6]-[3.8]. Another way is the grain size enlargement of poly-silicon film to decrease the grain boundaries, resulting in the less defects to improve the performance of LTPS-TFTs [3.9]-[3.11]. Solid phase crystallization (SPC) method provides a low cost, good uniformity and no contamination issue of process. However, the grain size of poly-silicon which is crystallized by SPC is not large enough, resulting in poor device performance and large operation voltage. Metal-induced lateral crystallization (MILC) method can provide a larger grain size of poly-silicon than SPC method does, resulting in higher field effect mobility μ_{FE}, deeper subthreshold swing S.S. and lower threshold voltage V_{TH} [3.10]. However, the electrical characteristics of MILC-TFTs are still much poor than single crystalline metal-oxide-semiconductor field effect transistor (MOSFET). Recently, the development of LTPS-TFTs are paid much attention to the applications of system-on-panel (SOP) and three-dimension

integration of very large scale integration (VLSI) technology [3.10][3.12][3.13]. Therefore, the performance of MILC LTPS-TFT is still needed to be enhanced.

In recent years, the employment of high-κ gate dielectric is a new way to enhance the performance of LTPS-TFT without any change of device structure [3.14]-[3.17]. In addition, the performance of p-channel SPC-TFT with HfO_2 gate dielectric is much higher than n-channel SPC-TFT [3.17], which is opposite to conventional SPC-TFT with SiO_2 gate dielectric [3.18]. It shows that the p-channel LTPS-TFT with HfO_2 gate dielectric would have more potential as the pixel driving device. However, the comparison of SPC and MILC p-channel LTPS-TFT with HfO_2 gate dielectric has not been proposed. In this work, the SPC and MILC p-channel LTPS-TFT with HfO_2 gate dielectric are fabricated simultaneously for the first time. Not only the SPC p-channel LTPS-TFT shows a high performance which can be compared with conventional MILC-TFT, but also the MILC p-channel LTPS-TFT shows a much high field effect mobility μ_{FE} which can be comparable with p-channel MOSFET.

The threshold voltage V_{TH} is defined as the gate voltage at which the drain current reaches 10 nA × W/L and V_D = –0.1 V. The field effect mobility μ_{FE} is extracted from the maximum transconductance (G_m).

3.2 Results and Discussion

Figure 1 shows the transfer characteristics (I_D-V_G curve and transconductance G_m) of SPC and MILC LTPS-TFTs with HfO_2 gate dielectric. Low threshold voltage V_{TH} (about –1.05 V and –0.75 V) and ultra-sharp subthreshold swing S.S. (about 0.145 V/decade and 0.107 V/decade) are achieved for SPC and MILC LTPS-TFTs with HfO_2 gate dielectric, respectively, without any defect passivation. The interface trap state N_{it} is extracted by the equation [3.19]:

$$N_{it} = [(\frac{S.S.}{\ln 10})(\frac{KT}{q}) - 1](\frac{C_{ox}}{q}) \quad (1)$$

As shown in Fig. 2, the gate capacitance density of HfO_2 gate dielectric, C_{ox}, is extracted from Al/HfO2/p-Si capacitor that about 12.3nm of effective oxide thickness (EOT) is obtained. The grain boundary trap states N_{trap} is estimated by Levinson and Proano method [3.4][3.5], which the N_{trap} is extracted from the plot of ln $[I_D/(V_G - V_{FB})]$ versus $1/(V_G - V_{FB})^2$ curves at $V_D = -0.1$ V and high V_G as shown in Fig. 3. The flat-band voltage V_{FB} is defined as the gate voltage that yields the minimum drain-current from the transfer characteristics. These important electrical parameters of SPC and MILC LTPS-TFTs are all listed in the Table I and compared with others' work. For SPC LTPS-TFTs, high-κ gate dielectric HfO_2 device shows better threshold voltage V_{TH}, subthreshold swing S.S. and field effect mobility μ_{FE} than SiO_2 gate dielectric of device. It is mainly attributed to the less interface trap states N_{it}, grain boundary trap states N_{trap} and large gate capacitance density, corresponding to EOT ~ 12.3nm, which can attract more carriers with the same gate bias. The same results are also observed in other's work [3.14]. However, the field effect mobility μ_{FE} of SPC LTPS-TFT with $HfSiO_x$ gate dielectric is much lower than conventional MILC LTPS-TFT with SiO_2 gate dielectric even the SiO_2 thickness is as thick as 100nm [3.11]. The good performance of conventional MILC LTPS-TFT is attributed to the large grain size, resulting in less grain boundary trap states N_{trap}. The SPC LTPS-TFT with HfO_2 gate dielectric in this work exhibits good electrical characteristics as shown in Fig. 2 and Table I. SPC LTPS-TFT with HfO_2 gate dielectric shows lower threshold voltage V_{TH} and sharper subthreshold swing S.S. than conventional MILC LTPS-TFT with SiO_2 gate dielectric. It is because the EOT of HfO_2 gate dielectric is about 12.3nm which can provide gate capacitance density about 8 times higher than 100nm SiO_2 gate dielectric. In addition, the field effect mobility μ_{FE} about 114 cm^2/V-s of

SPC LTPS-TFT with HfO_2 gate dielectric is significantly higher than conventional SPC and MILC LTPS-TFT with SiO_2 gate dielectric. For the MILC LTPS-TFT with HfO_2 gate dielectric, excellent electrical characteristics can be obtained, such as low threshold voltage ~ –0.75V, excellent subthreshold swing S.S. ~ 0.107 V/decade and very high field effect mobility μ_{FE} ~ 215 cm^2/V-s, which is much better than MILC LTPS-TFT with SiO_2 gate dielectric and SPC LTPS-TFT with HfO_2 gate dielectric. The superior performance of MILC LTPS-TFT with HfO_2 gate dielectric is attributed to the small EOT and low interface trap states N_{it} and grain boundary trap states N_{trap}. Figure 4 shows the I_D-V_D curves that very high driving current about 101 μA/μm and 61 μA/μm of SPC and MILC LTPS-TFTs with HfO_2 gate dielectric, respectively, with operation voltage 2-V are achieved. It would be suitable for the application of SOP and three-dimension integration of VLSI technology.

3.3 Summary

In this paper, high performance p-channel low temperature poly-silicon thin-film transistors (LTPS-TFTs) are fabricated by the employment of HfO_2 gate dielectric and two crystallization methods, solid phase crystallization (SPC) and metal-induced laterally crystallization (MILC), for comparison. High filed effect mobility μ_{FE} ~ 114 and 215 cm^2/V-s, ultra-low subthreshold swing S.S. ~ 145 and 107 mV/decade, and low threshold voltage V_{TH} ~ -1.05 and -0.75 V are derived from SPC- and MILC-TFT with HfO_2 gate dielectric, respectively. These excellent electrical characteristics are due to low trap states and much higher gate capacitance density with equivalent oxide thickness EOT ~ 12.3nm, resulting in lower operation voltage within 2-V of LTPS-TFT without any passivation method.

The comparison of SPC and MILC p-channel LTPS-TFT with HfO_2 gate dielectric is demonstrated for the first time. Excellent performance of SPC and MILC

TFT with HfO_2 gate dielectric, such as low threshold voltage V_{TH}, subthreshold swing S.S., high field effect μ_{FE} and driving current are demonstrated for the application of SOP and three-dimension integration of VLSI technology.

References

1. W. G. Hawkins, "Polycrystalline-silicon device technology for large-area electronics," *IEEE Trans. Electron Devices,* vol. 33, no. 4, pp. 477-481, Apr. 1986.
2. R. E. Proano, R. S. Misage, D. Jones, and D. G. Ast, "Guest-host active matrix liquid-crystal display using high-voltage polysilicon thin film transistors," *IEEE Trans. Electron Devices,* vol. 38, no.8, pp. 1781-1786, Aug. 1991.
3. G. Baccarani, B. Ricco, and G. Spadini, "Transport properties of polycrystalline silicon films," *J. Appl. Phys.,* vol. 49, no. 11, pp. 5565–5570, Nov. 1978.
4. R. E. Proano, R. S. Misage, and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistor," *IEEE Trans. Electron Devices,* vol. 36, no. 9, pp. 1915–1922, Sep. 1989.
5. J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.,* vol. 53, no. 2, pp. 1193–1202, Feb. 1982.
6. S.-D. Wang, W.-H. Lo, T.-Y. Chang, and T.-F. Lei, "A novel process-compatible fluorination technique with electrical characteristic improvements of poly-Si TFTs," *IEEE Electron Device Lett.,* vol. 26, pp. 372-374, June, 2005.
7. H.-C. Cheng, F.-S. Wang, and C.-Y. Huang, "Effects of NH_3 plasma passivation on n-channel polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices,* vol. 44, no. 1, pp. 64-68, Jan. 1997.
8. C.-H. Tu, T.-C. Chang, P.-T. Liu, C.-H. Chen, C.-Y. Yang, Y.-C. Wu, H.-C. Liu, L.-T. Chang, C.-C Tsai, Simon M. Sze, and C.-Y. Chang, "Electrical enhancement of solid phase crystallized poly-Si thin-film transistors with fluorine ion implantation," *J. Electrocehm. Soc.,* vol. 153, no. 9, pp. 815-818, 2006.
9. S.-W. Lee, and S.-K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.,* vol. 17, no. 4, pp. 160-162, April, 1996.
10. G. A. Bhat, Z. Jin, H. S. Kwok, and M. Wong, "Effects of longitudinal grain boundaries on the performance of MILC-TFT's," *IEEE Electron Device Lett.,* vol. 20, no. 2, pp. 97-99, Feb., 1999.
11. Z. Meng, M. Wang, and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors

for system-on-panel applications," *IEEE Trans. Electron Devices,* vol. 47, no. 2, pp. 404-409, Feb., 2000.

12. F. Hayashi, H. Ohkubo, T. Takahashi, S. Horiba, K. Noda, T. Uchida, T. Shimizu, N. Sugawara, and S. Kumashiro, "A highly stable SRAM memory cell with top-gated P-N drain poly-Si TFTs for 1.5 V operation," in *IEDM Tech. Dig.,* 1996, pp. 283-286.
13. H. J. Cho, F. Nemati, P. B. Griffin, and J. D. Plummer, "A novel pillar DRAM cell for 4 Gbit and beyond," in *Dig. Symp. VLSI Tech.,* 1998, pp. 38-39.
14. M.-J. Yang, C.-H. Chien, Y.-H. Lu, C.-Y. Shen, and T.-Y. Huang, "Electrical properties of low-temperature-compatible p-channel polycrystalline-silicon TFTs using high-κ gate dielectrics," *IEEE Trans. Electron Devices,* vol. 55, no. 4, pp. 1027-1034, 2008.
15. C.-P. Lin, B.-Y. Tsui, M.-J. Yang, R.-H. Huang, and C. H. Chien, "High-performance poly-silicon TFTs using HfO_2 gate dielectric," *IEEE Electron Device Lett.,* vol. 27, no. 5, pp. 360-363, May, 2006.
16. M.-W. Ma, T.-S. Chao, T.-Y. Chiang, W.-C. Wu, and T.-F. Lei, "Impacts of N_2 and NH_3 plasma surface-treatment on high performance LTPS-TFT with high-κ gate dielectric," *IEEE Electron Device Lett.,* vol. 29, no. 11, pp. 1236-1238, 2008.
17. M.-W. Ma, T.-Y. Chiang, W.-C. Wu, T.-S. Chao and T.-F. Lei, "Characteristics of HfO_2/Poly-Si interfacial layer on CMOS LTPS-TFTs with HfO_2 gate dielectric and O_2 plasma surface treatment," *IEEE Trans. Electron Devices,* vol. 55, no. 12, pp. 3489-3493, 2008.
18. C.-P. Lin, Y.-H. Hsiao, and B.-Y. Tsui, "Process and characteristics of fully silicided source/drain (FSD) thin-film transistors," *IEEE Trans. Electron Devices,* vol. 53, no. 12, pp. 3086-3094, 2006.
19. C. A. Dimitriadis, P. A. Coxon, L. Dozsa, L. Papadimitrious, and N. Economou, "Performance of thin-film transistors on polysilicon films grown by low-pressure chemical vapor deposition at various pressures," *IEEE Trans. Electron Devices,* vol. 39, no. 3, pp. 598-606, 1992.

Crystallization	SPC	SPC	MILC	MILC	SPC	SPC
Ref.	This work	This work	This work	Ref.11	Ref.14	Ref.14
Gate Dielectric	SiO_2	HfO_2	HfO_2	SiO_2	SiO_2	$HfSiO_x$
W/L (μm/μm)	10/10	10/10	10/10	10/5	5/10	5/10
V_{TH} (V)	-10.3	-1.05	-0.75	-4.2	-6.90	-1.13
S.S. (V/dec.)	1.57	0.145	0.107	1.0	1.06	0.37
EOT (nm)	50	12.3	12.3	100	46.5	25.5
μ_{FE} (cm^2/V-s)	13	114	215	98	17.61	30.41
N_{it} (cm^{-2})	$1.09x10^{13}$	$2.51x10^{12}$	$1.39x10^{12}$	$3.40x10^{12}$	$7.86x10^{12}$	$4.44x10^{12}$
N_{trap} (cm^{-2})	$7.05x10^{12}$	$1.61x10^{12}$	$1.40x10^{12}$	--	$6.27x10^{12}$	$4.09x10^{12}$

Table I. Important device parameters of SPC and MILC LTPS-TFTs with HfO_2 gate dielectric. The others' works are also listed for comparison.

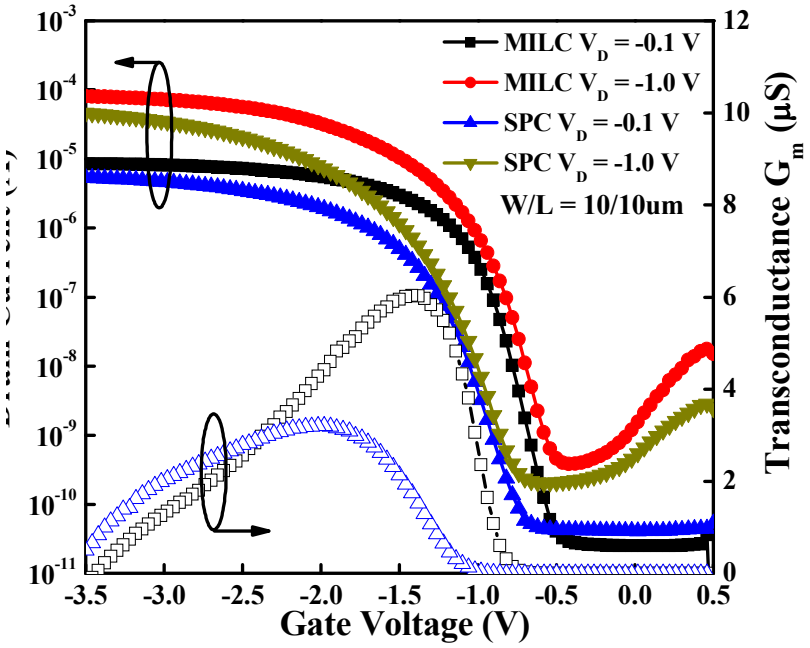


Fig. 1. The transfer characteristics (I_D-V_G and G_m) of SPC and MILC LTPS-TFTs with HfO_2 gate dielectric.

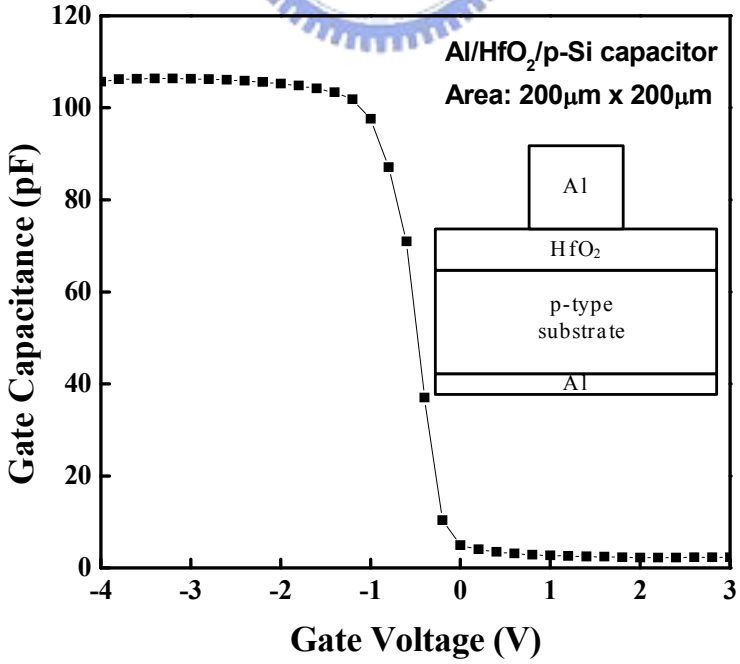


Fig. 2. The gate capacitance of Al/HfO_2/p-Si capacitor.

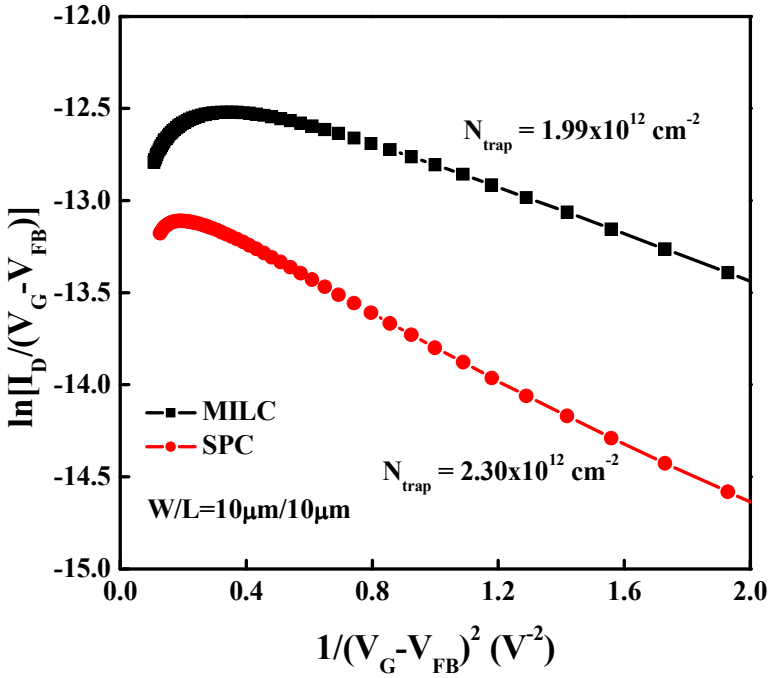


Fig. 3. The plots of ln $[I_D/(V_G - V_{FB})]$ versus $1/(V_G - V_{FB})^2$ curves at $V_D = -0.1$ V and high V_G.

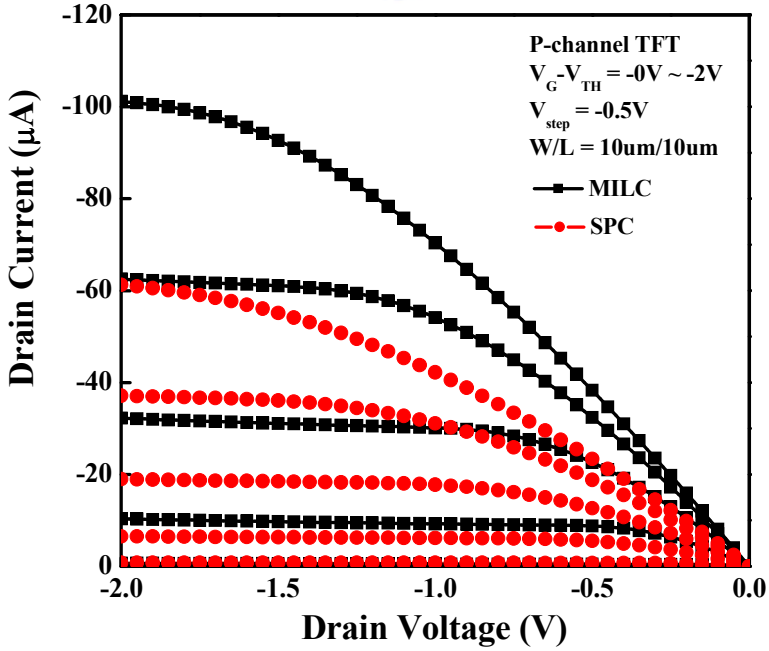


Fig. 4. The I_D-V_D curve of SPC and MILC LTPS-TFTs with HfO_2 gate dielectric.

Chapter 4

Negative Bias Temperature Instability in SPC and MILC P-Channel LTPS TFTs with HfO_2 Gate Dielectric

4.1 Introduction

Low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) are expected for the realization of system on panel (SOP) in the future [4.1]. For this target, high performance of LTPS TFTs are essential to design the CMOS inverter configuration. It has been shown that the p-channel LTPS-TFT with HfO_2 gate dielectric would have more potential as the pixel driving device than with conventional SiO_2 gate dielectric [4.2]. However, due to the poor thermal conductivity on the glass substrate and high operating voltage level, p-channel TFT will be subjected to negative bias temperature instability (NBTI) comparing with MOSFETs. Therefore, it is important to study NBTI behaviors and the related degradation mechanisms in LTPS TFTs with high-κ gate device.

In conventional MOSFETs with SiO_2 dielectric, the NBTI-induced degradation is mainly attributed to the generation of interface trap states (N_{IT}) [4.3][4.4], and it can be partially recoverable once the stress bias is removed [4.5]-[4.7]. This phenomenon has been interpreted by the reaction-diffusion (R-D) model [4.3]-[4.5]. During the stress, inversion layer holes interacted with Si–H bonds and dissociated at Si/SiO_2 interface. Subsequently, the released hydrogen species either diffuse away from the Si/SiO_2 interface and leaves behind Si– (N_{IT} generation), or reacts back with Si– and form Si–H (N_{IT} repassivation). The N_{IT} generation will cause device degradation, ie, an increase in absolute threshold voltage (V_{TH}) ,or degradations in subthreshold swing (S.S.) and field-effect mobility (μ_{FE}) [4.8][4.9].

However, this reliability issue is further complicated by the introduction of high-κ dielectrics. Compared to SiO_2 , hafnium-based oxide showed a large amount of V_{TH} shift due to a high density of pre-existing structural defects, which was considered that crystallization introduces grain into the gate stack and adds extra trap states [4.10]-[4.12]. These pre-existing traps cause the V_{TH} instability due to charge trapping/de-trapping phenomenon [4.13]-[4.16]. By the transient nature of charging behavior and N_{IT} generation, the V_{TH} shifts significant under the stress [4.11][4.17][4.18]. Although those phenomenon can affect many aspects of electrical characterization, the reliability issue in LTPS TFT with high-κ dielectric films have not yet been studied systematically

Since previous studies on LTPS TFT reliability mainly focused on solid-phase crystallization (SPC) TFTs [4.19], it is meaningful to compare SPC with MILC devices in reliability issue. In MILC TFTs, higher performance has been observed due to the larger grain sizes [4.20]; however, higher leakage current ($I_{leakage}$) is also found which is associated with channel residual Ni contamination [4.21][4.22]. As a result, the Ni-related reliability issue is more concerned. However, up to now, no such correlative comparisons for two kinds of device have been studied systematically.

In this work, the main objective is to develop a practical methodology to analyze the degradation mechanism in high-κ gate stacks under various stress bias and temperature. Use of R-D model to analyze the NBTI effect in high-κ gate dielectric TFT has not been reported. Furthermore, the comparison of NBTI effect between SPC and MILC TFT with high-κ gate stack were studied. By measuring and analyzing the NBTI characteristics, it can aid to produce highly reliable TFT circuits and realize the application of SOP and 3-D integration of VLSI technology in the future.

The NBTI stress was applied to study the degradation-dependent mechanisms by DC I_d-V_g measurement technique. It was performed at the temperature ranging from

25 ℃ to 100℃, and a gate voltage in the range of −5 to −6.5 V. Source and drain were grounded during the stress. ΔV_{TH} change was monitored by measuring the drain current–gate voltage ($I_d - V_g$) characteristics at low drain voltage (-100mV). During $I_d - V_g$ measurement, the range of the gate bias was limited to 0.5 ~ -5V to minimize an additional stress on the device.

4.2 Results and Discussion

Fig. 1 shows the transfer characteristics of the LTPS TFT with HfO_2 gate stack before and after the NBTI stress, respectively. The device shows serious degradation in the subthreshold swing (S.S.) and field-effect mobility (μ_{FE}), indicating that interface trap states (N_{IT}) were generated. Further, the threshold voltage shifts to the negative direction after the stress, it implying that a net positive charge is clearly trapped in the high-κ gate dielectric or/and at the interface states. The output characteristics also exhibit the similar degradation behavior, as can be seen in Fig.2. These show that LTPS TFT with HfO_2 devices have poor reliability problem during the long-time operation. In addition, it can be observed that stress voltage leads to a larger enhancement in ΔV_{TH} in SPC than in MILC. The results indicate that MILC transistors have more stability characteristic, compared with SPC. Detailed analysis will be discussed later.

In conventional p-MOSFETs, R-D model was proposed to describe negative bias temperature instability (NBTI) temperature/voltage dependence observed in SiO_2 gate dielectric transistors [4.3]-[4.5]. This degradation is explained by dissociation of the Si–H bond at the Si/SiO_2 interface and generation of interface trap states (N_{IT}). Compared with other electrical parameters, the threshold voltage shift (ΔV_{TH}) is the most serious during the stress. As a result, we are more concerned about V_{TH} degradation behavior for NBTI stress. Furthermore, the model has been quite

successful in predicting the voltage and temperature acceleration behavior, as well as quantitative prediction of the time dependency. The degradation of threshold-voltage shift (ΔV_{TH}) can be described by the empirical formula [4.8][4.23][4.24]

$$\Delta V_{TH} \propto t^{n} e^{(-E_a/kT)} e^{C|V_G|} \quad (1)$$

Where n is the time exponent, E_a is the activation energy, and the parameter C is the constant of V_G-dependence [4.8].

However, in the high-κ pMOSFETs, the NBTI degradation is more serious and complex than MOSFETs with traditional SiO_2 gate dielectric due to the charge trapping/detrapping phenomenon [4.13]-[4.16]. A high density of pre-existing defects in the high-κ bulk provide extra trap states (N_{OT}) and cause V_{TH} shift. Thus, stress-induced changes in the threshold voltage, ΔV_{TH}, may include contributions from both the generation of interface trap states (N_{IT}) and trap charges in gate dielectric (N_{OT}), which are expected to be controlled by different mechanisms. Originally, we cannot assure which degradation mechanisms are dominant in our experiments. It was previously reported that there are similar power-law dependence behavior in $\Delta V_{TH}(t)$ which can be obtained in charge trapping phenomenon [4.11][4.13]. Therefore, we speculate that the previous empirically formula for traditional NBTI in SiO_2 may also be able to analyze the high-κ gate dielectric in our LTPS TFTs.

Fig. 3 – Fig.6 show the time-dependence of the ΔV_{TH} at various stresses temperature with the SPC and MILC device for comparison. ΔV_{TH} shift increases with the stress time and follows a power law dependence (t^n). The time exponent n extracted here is varying from 0.14 at 25℃ to 0.34 at 100℃ for SPC, and from 0.12 at 25℃ to 0.31 at 100℃ for MILC. It is observed that the exponent n value has slightly fluctuation at low temperature (Fig. 3 and Fig.4); this is because the magnitude of the threshold-voltage shift under NBTI stress is very small (< 1 V for short stress time)

causing a larger error value.

The results indicate that behavior of n value is similar to those previously reports for conventional NBTI degradation [4.3][4.8]. That is to say, *n* value is dependent on temperature and independent on stress time and stress voltage. Moreover, the coincidence of stressed trends in SPC and MILC devices reflects the similar degradation-mechanism during NBTI stress.

It is important to note that initial ΔV_{TH} shift before the first 20 s stress, ΔV_{TH} ($t < 20s$), to extract much greater exponent *n* than the shift after the subsequent 20 s stress(ΔV_{TH} ($t > 20s$)). This is because of the measurements are performed by using the DC I_D-V_G technique. When measurement time is too long, it will lead into addition of extra stress and/or de-trapping phenomenon in the short stress-time region [4.10] [4.15]. Therefore, to obtain a correct *n* value which should be independent of the stress time, we focus on the stress data in the time range $t > 20s$, which are less affected during the stress interruption. After adjusting ΔV_{TH} (t) for the above, the different stress gate voltage produce a similar slope value.

The threshold voltage shift (ΔV_{TH}) during the stress also shows an exponential dependence on V_G and 1/T [4.8][4.24], as seen in Fig. 7 and Fig. 8. The parameter *C* extracted from plots is 0.15 ~ 0.20 for SPC and 0.12 ~ 0.21 for MILC, respectively. The activation energy (E_a) extracted from the Arrhenius relationship is between 0.04 and 0.05 eV for SPC and MILC, which is independent of stress voltage. ΔV_{TH} increases with the stress voltage or temperature, implying that ΔV_{TH} shift can be electrically and thermally activated. This experimental results also exhibit similar trend as previous NBTI-induced degradation with SiO_2 gate dielectric, as will be discussed below.

In high-κ MOSFETs, the NBTI degradation has been widely attributed to the generation of charges in gate dielectric and interface trap states (N_{IT}). However, our

experimental results indicated that the interface trap states generation must be considered to clarify the degradation behavior. The results showed that the threshold-voltage shift (ΔV_{TH}) have almost the same power law dependence on the stress time, and same exponential dependence on V_G and 1/T. Based on the results shown, we speculated that the NBTI degradation in our experiment is dominated by the generation of N_{IT}, that is, the effective quantity of N_{IT} may larger than the effective quantity of charge trapping in gate dielectric. Moreover, the electric field across the gate dielectric (below 1.5 MV/cm) was not high enough to cause hole injection [4.8], and the gate leakage current was less. It implies that the NBTI degradation may be not related to the charge trapping.

In our experiment, the all degradation behavior in MILC TFTs are similar to that in SPC TFTs. Besides, the results also indicate that MILC transistors have more stability characteristic than SPC, as shown in Fig.9 . Fig.9 represent the threshold voltage shift (ΔV_{TH}) and I_{ON} degradation on the same overdrive stress voltage (V_G-V_T = -5V) with the SPC and MILC TFTs for comparison. It can be interpreted that MILC devices have larger grain size than SPC devices in the channel region. In MILC devices, due to the grain size is large, the smaller existence of trap states in the grain boundaries and at the poly-Si/HfO_2 interface, less Si–H bonds may be found in the channel region than SPC. As a result, less N_{IT} generate (due to less Si–H bonds break) and lead better reliability than SPC device.

According to the R-D model, the NBTI-induced threshold-voltage shift occurs due to the generation of N_{IT}. It is know that N_{IT} will trap carrier and generate extra Coulomb scattering to degrade carriers transportation like reduction of field effect mobility μ_{FE} or transconductance G_M [4.25][4.26]. Besides, it also make higher enhancement of subthreshold swing (S.S.). As a result, we also observed the G_M and S.S. degradation behavior in this work. Fig.10 and Fig.11 show the dependence of the

G_M and S.S. degradation rate versus stress time under various stress bias, respectively. Compared with G_M, S.S. degradation behavior is more consistent with ΔV_{TH}. No matter in SPC or in MILC device, this phenomenon also can be obverse. In addition, Fig. 12 – Fig. 15 reveal the exponential dependence on stress voltage (V_G) and stress temperature (T) for G_M and S.S. degradation, respectively. The same results indicate that ΔV_{TH} and S.S. have analogous degradation mechanism, compared with G_M.

The subthreshold swing (S.S.) has been reported to be closely related to the trap states located near the midgap (deep states), which originate from dangling bonds [27]. During the stress, large Si-H bonds broken and left numerous trap states at the poly-Si/HfO_2 interface and grain boundaries in channel. Those trap states (N_{bulk}) will trap the inversion-carriers and cause subthreshold swing increasing [4.9]. The increasing of subthreshold swing is proportional to the generation of N_{bulk} (S.S.$\propto N_{bulk}$), which is extracted by the equation [4.28]

$$N_{bulk} = \left[\left(\frac{S.S.}{ln10}\right)\left(\frac{kT}{q}\right) - 1\right]\left(\frac{C_{OX}}{q}\right) \quad (2)$$

As same as the increasing of threshold voltage shift, the proportional relation ($\Delta V_{TH} \propto N_{bulk}$) can be observed

$$\Delta V_{TH} = -\frac{q(\Delta N_{bulk})}{C_{ox}} \quad (3)$$

However, the G_M degradation (or mobility degradation) is caused by increasing the Coulombic scattering due to trap states hold the transport charges. The mobility relation in TFTs could be modified as [4.29]

$$\mu \cong \mu_b exp\left(\frac{-q^2 N_{trap}^2}{8\varepsilon N_D kT}\right) \quad (4)$$

It is dependent on the N_{bulk} but not be proportional to N_{bulk} directly. Therefore, the ΔS.S. degradation behavior is more consistent with the ΔV_{TH} than ΔG_M.

4.3 Summary

The NBTI degradation mechanism in LTPS TFTs with HfO_2 gate dielectric has been investigated with a conventional DC measurement technique. Besides, the reliability comparisons for SPC and MILC devices have been studied systematically. We used the previously empirical formula for traditional NBTI in SiO_2 to analyze the high-κ gate dielectric in our experiment. The results showed that the threshold-voltage shift (ΔV_{TH}) have almost the same power law dependence on the stress time, and same exponential dependence on V_G and 1/T. According to the results, we demonstrated that NBTI degradation in our experiment is more dominated by the generation of interface trap states (N_{IT}).

Moreover, the coincidence of stressed trends measured in SPC and MILC reflects the similar degradation-mechanism for NBTI stress. The results can be interpreted that MILC devices have better quality than SPC devices in the channel region. In addition, the MILC transistors have more stability characteristic than SPC during the NBTI stress. Finally, we also observed the G_M and S.S. degradation behavior in this work. Compared with transconductance (G_M), the subthreshold swing (S.S.) degradation behavior is more consistent with the threshold voltage shift (ΔV_{TH}).

References

1. Z. Meng, M. Wang, and M. Wong, "High Performance Low temperature Metal-Induced Unilaterally Crystallized Polycrystalline Silicon Thin Film Transistors for System-on-Panel Applications," *IEEE Trans. Electron Devices*, vol. 47, pp. 404-409, 2000.
2. M. W. Ma, T. S. Chao, C. J. Su, W. C. Wu, K. H. Kao, T. F. Lei, **"**High-Performance Metal-Induced Laterally Crystallized Polycrystalline Silicon P-Channel Thin-Film Transistor With TaN/HfO_2 Gate Stack Structure,**"** *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 592-594, 2008.
3. S. Mahapatra, P. B. Kumar, and M. A. Alam "Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of pMOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 1371-1379, 2004.
4. A. T. Krishnan, S. Chakravarthi, P. Nicollian, V. Reddy, S. Krishnan, "Negative bias temperature instability mechanism: The role of molecular hydrogen," *Applied Physics Letter*, 88, 153518, 2006.
5. S. Rangan, N. Mielke, E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability," *IEDM*, pp. 341-344, 2003.
6. M. A. Alam, "A critical examination of the mechanics of dynamic NBTI for PMOSFETs," *IEDM*, pp. 345-348, 2003.
7. Y. Toyota, M. Matsumura, M. Hatano, T. Shiba, M. Ohkura, "Accelerated Negative-Bias Temperature Degradation in Low-Temperature Polycrystalline Silicon p-Channel TFTs Under Dynamic Stress," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2452-2459, 2007.
8. C. Y. Chen, J. W. Lee, S. D. Wang, M. S. Shieh; P. H. Lee; W. C. Chen; H. Y. Lin; K. L. Yeh; T. F. Lei, "Negative Bias Temperature Instability in Low-Temperature Polycrystalline Silicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol.

53, no. 12, pp. 2993-3000, 2006.

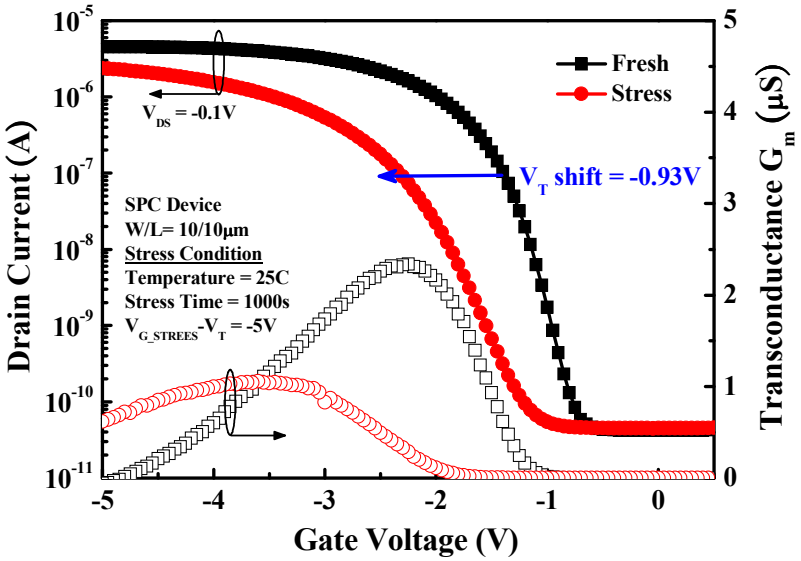
9. C. Y. Chen, M. W. Ma, W. C. Chen, H. Y. Lin, K. L. Yeh, S. D. Wang, T. F. Lei, **"**Analysis of Negative Bias Temperature Instability in Body-Tied Low-Temperature Polycrystalline Silicon Thin-Film Transistors**,"** *IEEE Electron Device Lett.*, vol. 29, no. 2, pp. 165-167, 2008.
10. G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, G. Ghibaudo, "Review on high k dielectrics reliability issues," *IEEE Trans. Electron Device and Materials Reliability*, vol. 5, no. 1, pp. 5-19, 2005.
11. A. Neugroschel , G. Bersuker , R. Choi, C. Cochrane, P. Lenahan, D. Heh, C. Young, C. Y. Kang, B. H. Lee, R. Jammy, "An accurate lifetime analysis methodology incorporating governing NBTI mechanisms in high-k/SiO_2 gate stacks," *IEDM Tech. Dig.*, pp. 317, 2006.
12. R. Choi, C. Young, Y. K. Chang, D. Heh, G. Bersuker, S. Krishnan, R. P. Kirsch, A. Neugroschel, S. C. Song, B. H. Lee, R. Jammy, "Reliability Assessment on Highly Manufacturable MOSFETs with Metal Gate and Hf based Gate Dielectrics," Physical and Failure Analysis of Integrated Circuits, IPFA 2007. 14^{th}.
13. D. Heh, R. Choi, C. D. Young, G. Bersuker, "Fast and slow charge trappingdetrapping processes in high-k nMOSFETs.," Integrated Reliability Workshop Final Report, 2006.
14. D. Heh, C. D. Young, and G. Bersuker, "Experimental Evidence of the Fast and Slow Charge TrappingDetrapping Processes in High-k Dielectrics Subjected to PBTI Stress," *IEEE Trans. Electron Devices*, vol. 29, no. 2, pp. 180-182, 2008.
15. R. Choi, S. J. Rhee, J. C. Lee, B. H. Lee, G. Bersuker, "Charge trapping and detrapping characteristics in hafnium silicate gate stack under static and dynamic stress," *IEEE Trans. Electron Devices*, vol. 26, no. 3, pp. 197-199, 2005.
16. R. Choi, S. C. Song, C. D. Young, G. Bersuker, "Charge trapping and detrapping

characteristics in hafnium silicate gate dielectric using an inversion pulse measurement technique," *Applied Physics Letter*, 87, 122901, 2005.

17. C. Shen, M. F. Li, X. P. Wang, H. Y. Yu, Y. P. Feng, A. T. L. Lim, Y. C. Yeo, D. S. H. Chan, D. L. Kwong, "Negative U traps in HfO_2 gate dielectrics and frequency dependence of dynamic BTI in MOSFETs," *IEDM*, pp. 733-736, 2004.
18. J. P. Campbell, K. P. Cheung, J. S. Suehle, A. oates, "Negative-bias temperature instability induced electron trapping," *Applied Physics Letter*, 93, 033512, 2008.
19. M. W. Ma, C. Y. Chen, W. C. Wu, C.J. Su, K.H. Kao, T.S. Chao, T. F. Lei, **"**Reliability Mechanisms of LTPS-TFT With HfO_2 Gate Dielectric: PBTI, NBTI, and Hot-Carrier Stress**,"** *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1153-1160, 2008.
20. S. W. Lee and S. K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 17, no. 4, pp. 160-162, 1996.
21. D. Zhang and M. Wong, "Effects of trace nickel on the growth kinetics and the electrical characteristics of metal-induced laterally crystallized polycrystalline silicon and devices," J. Soc. Inf. Displ., vol. 13, no. 10, pp. 815-822, 2005.
22. P. J. van der Zaag, M. A. Verheijen, S. Y. Yoon, N. D. Young, "Explanation for the leakage current in polycrystalline-silicon thin-film transistors made by Ni-silicide mediated crystallization," Appl. Phys. Lett., vol. 81, no. 18, pp. 3404-3406, Oct. 2002.
23. C. Hu, M. Wang, B. Zhang, M. Wong, "Negative Bias Temperature Instability Dominated Degradation of Metal-Induced Laterally Crystallized p-Type Polycrystalline Silicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 4, pp. 587-594, 2009.
24. C. Y. Chen, J. W. Lee, P. H. Lee, W. C. Chen, H. Y. Lin, K. L. Yeh, M. W. Ma, S.

D. Wang, T. F. Lei, “A Reliability Model for Low-Temperature Polycrystalline Silicon Thin-Film Transistors,” *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 392-394, 2007.

25. S. C. Sun, J. D. Plummer, “Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces,” *IEEE Trans. Electron Devices*, vol. 27, no. 8, pp. 1497-1508, 1980.
26. S. Takagi, A. Toriumi, M. Iwase, H. Tango, “On the Universality of Inversion Layer Mobility in Si MOSFET’s: Part I —Effects of Substrate Impurity Concentration,” *IEEE Electron Device Lett.*, vol. 41, no. 12, pp. 2357-2362, 1994.
27. I. W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis, A. Chiang, “Passivation Kinetics of Two Types of Defects in Polysilicon TFT by Plasma Hydrogenation,” *IEEE Electron Device Lett.*, vol. 12, no. 4, pp. 181-183, 1991.
28. C. A. Dimitriadis, P. A. Coxon, L. Dozsa, L. Papadimitrious, N. Economou, “Performance of thin-film transistors on polysilicon films grown by low-pressure chemical vapor deposition at various pressures,” *IEEE Trans. Electron Devices,* vol. 39, no. 3, pp. 598-606, 1992.
29. J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, M. Rider, “Conductivity behavior in polycrystalline semiconductor thin film transistors,” *J. Appl. Phys.*, vol.53, 1993, 1982.



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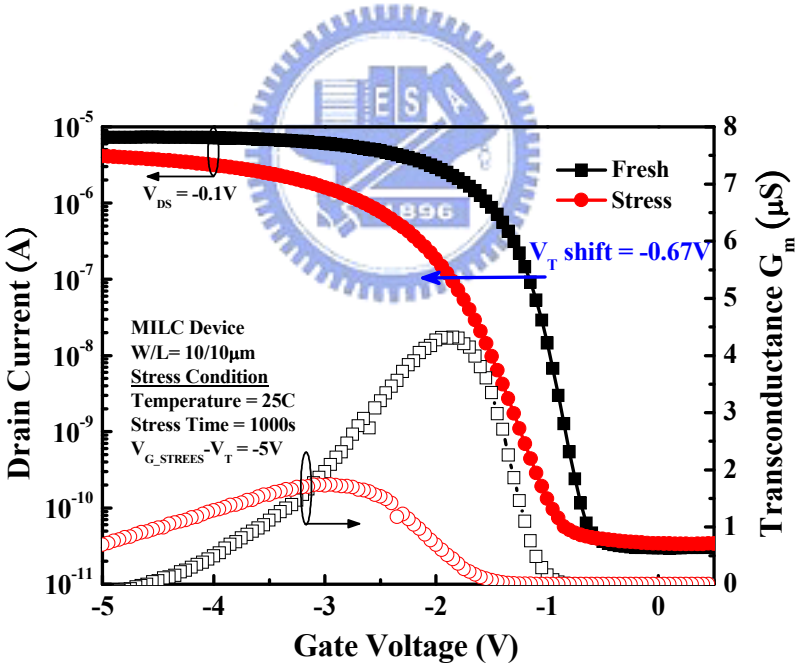
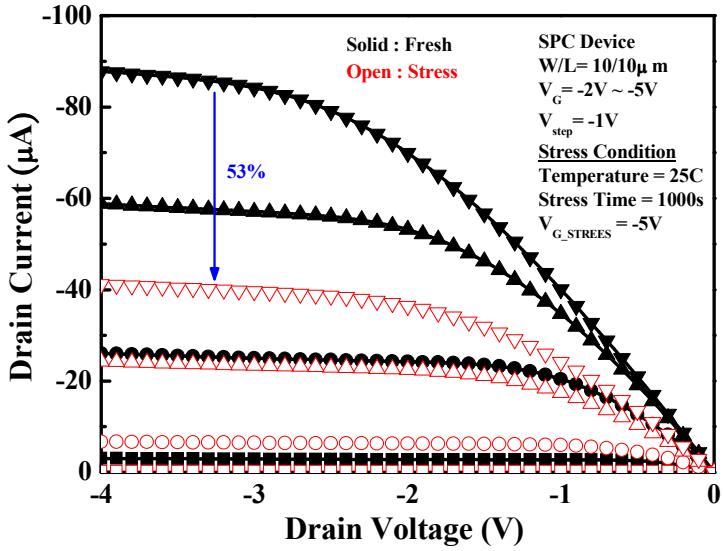


(b)

Fig. 1. Transfer characteristics of (a) SPC and (b) MILC LTPS-TFTs with HfO_2 gate dielectric before and after NBTI stress.



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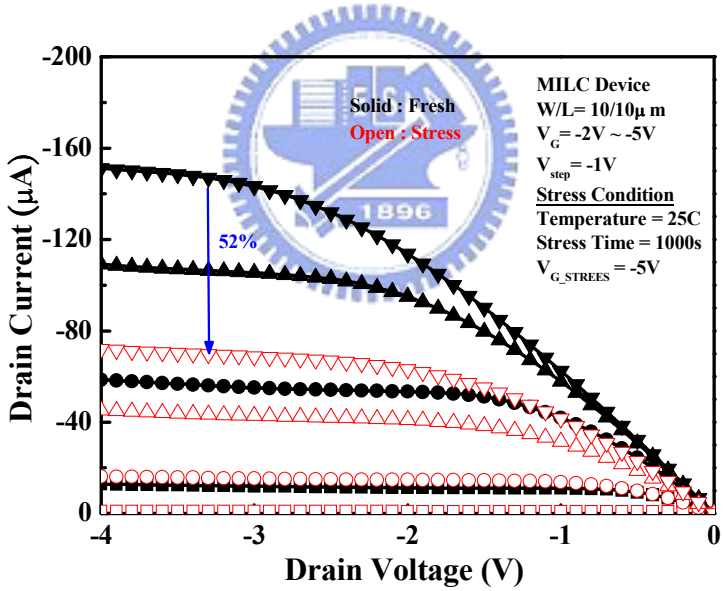
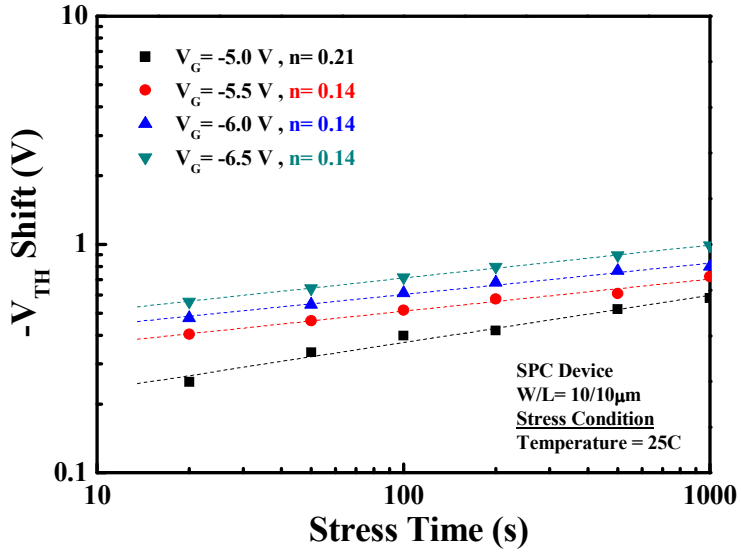


(b)

Fig. 2. Output characteristics of (a) SPC and (b) MILC LTPS-TFTs with HfO_2 gate dielectric before and after NBTI stress.



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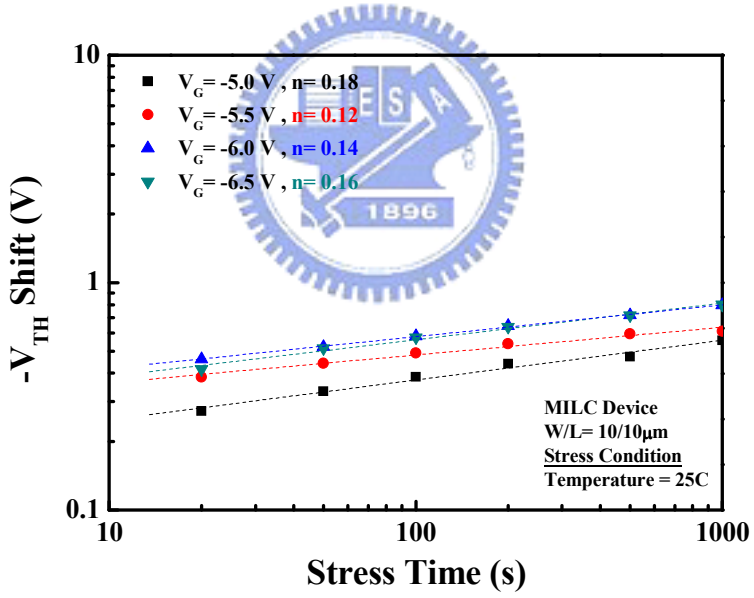

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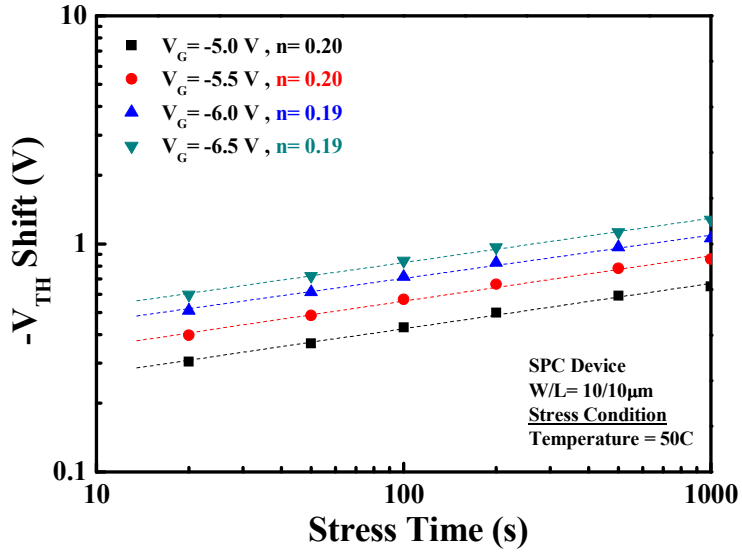
Fig. 3. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress time at 25℃ with the (a) SPC and (b) MILC device.



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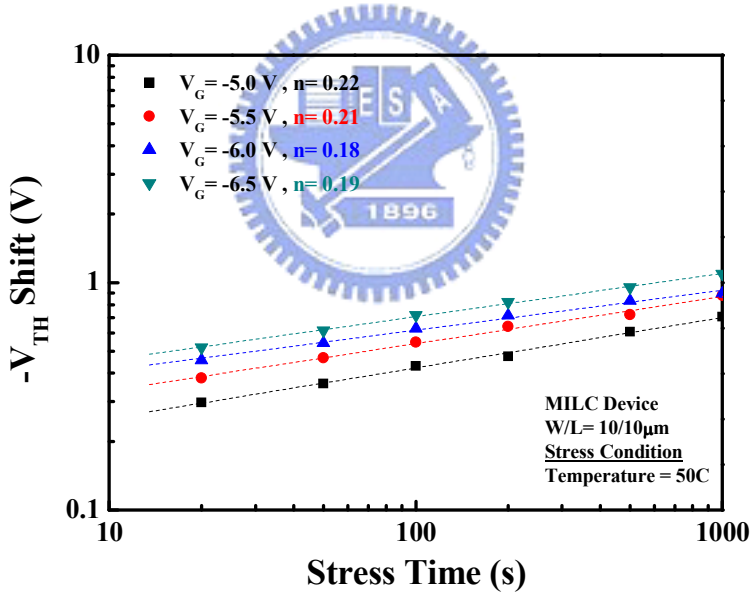
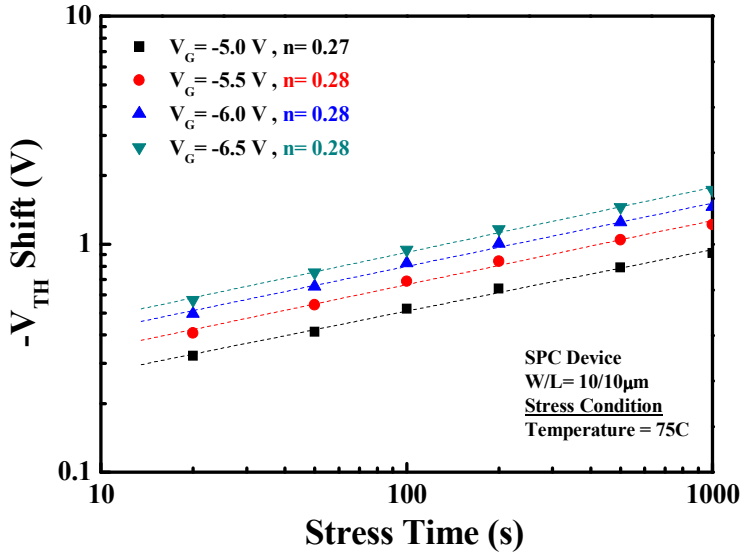


(b)

Fig. 4. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress time at 50℃ with the (a) SPC and (b) MILC device.



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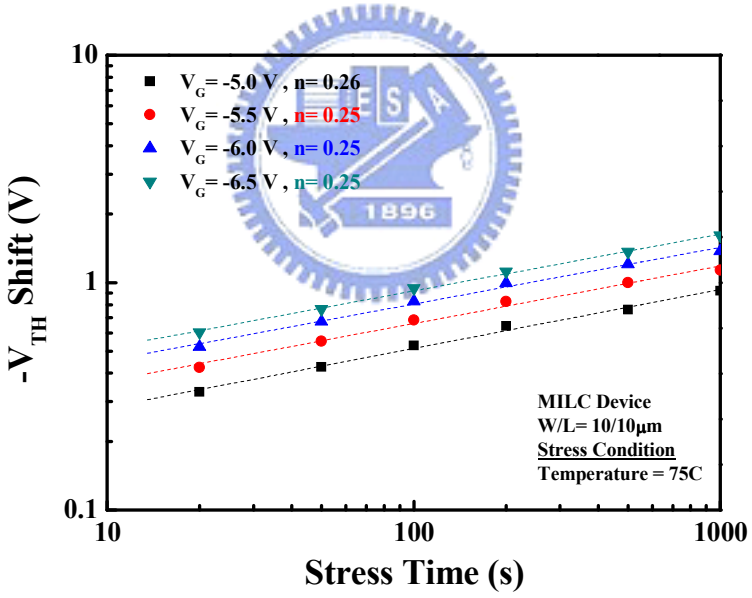
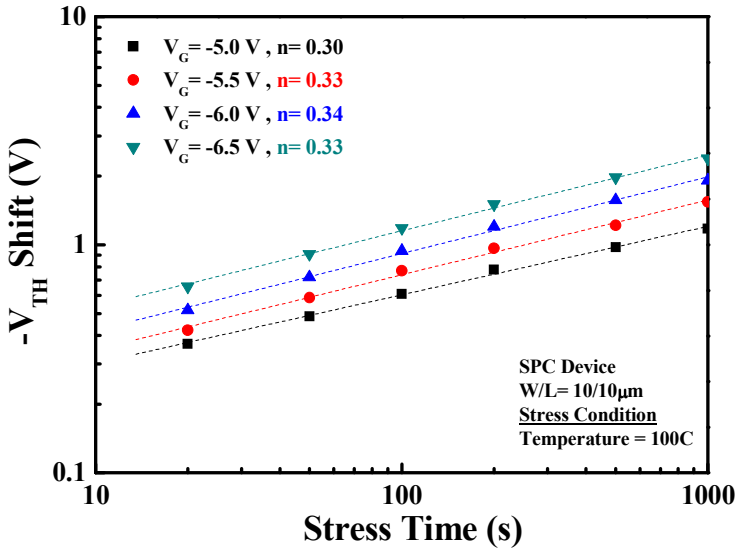


(b)

Fig. 5. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress time at 75℃ with the (a) SPC and (b) MILC device.



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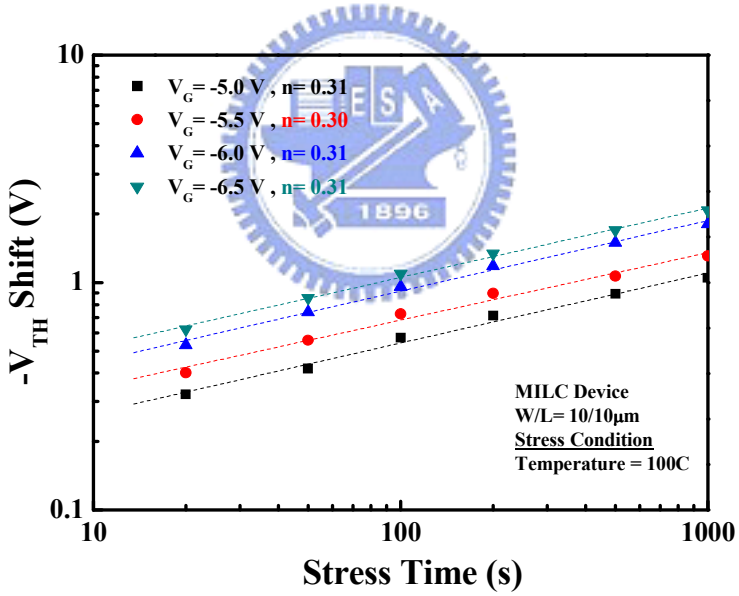
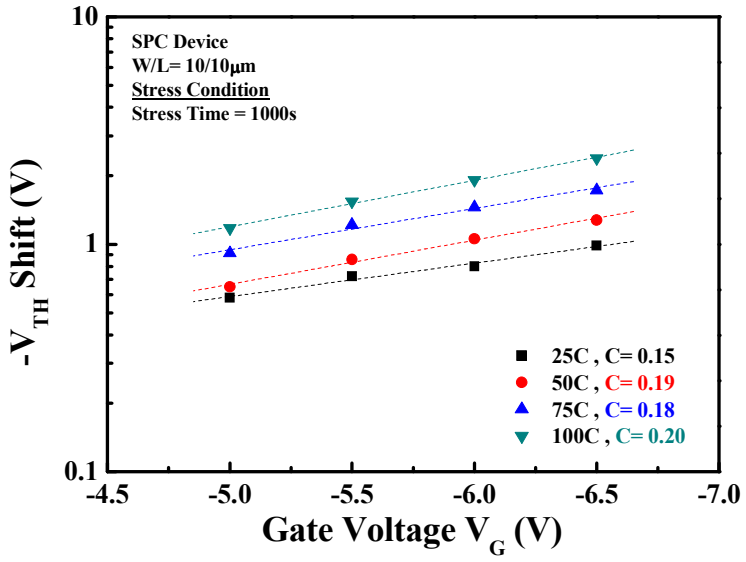


(b)

Fig. 6. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress time at 100℃ with the (a) SPC and (b) MILC device.



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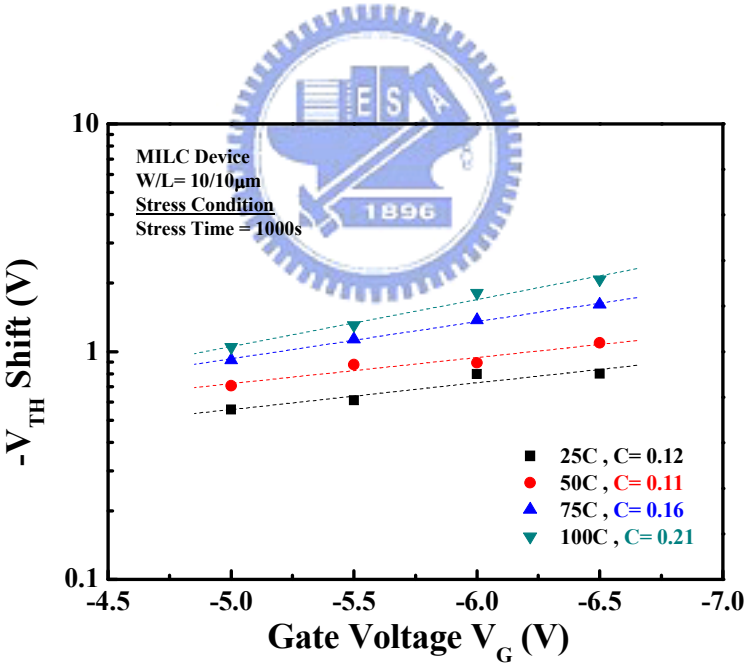
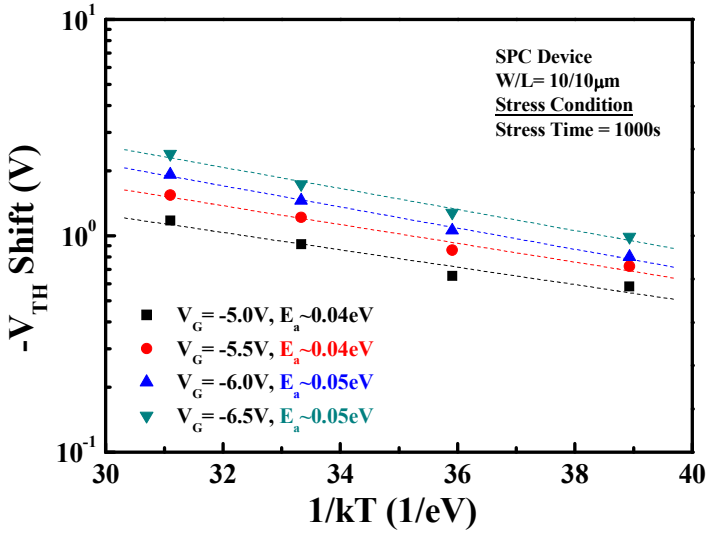


(b)

Fig. 7. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress voltage at various temperature with the (a) SPC and (b) MILC device.



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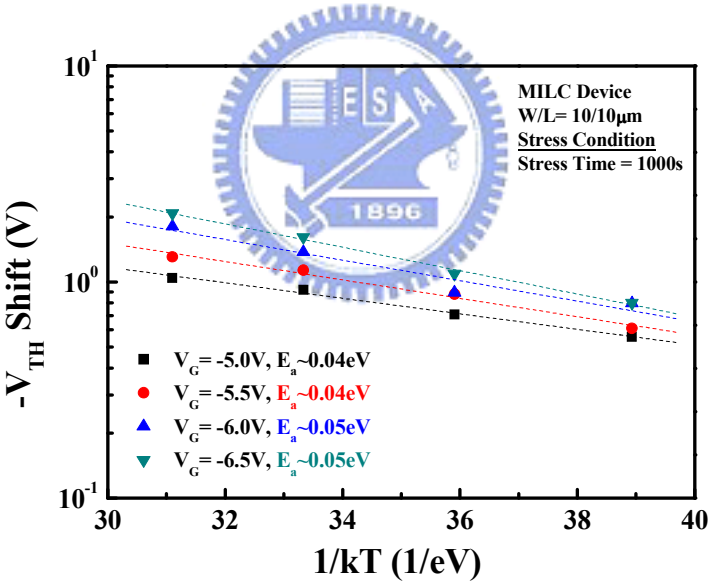

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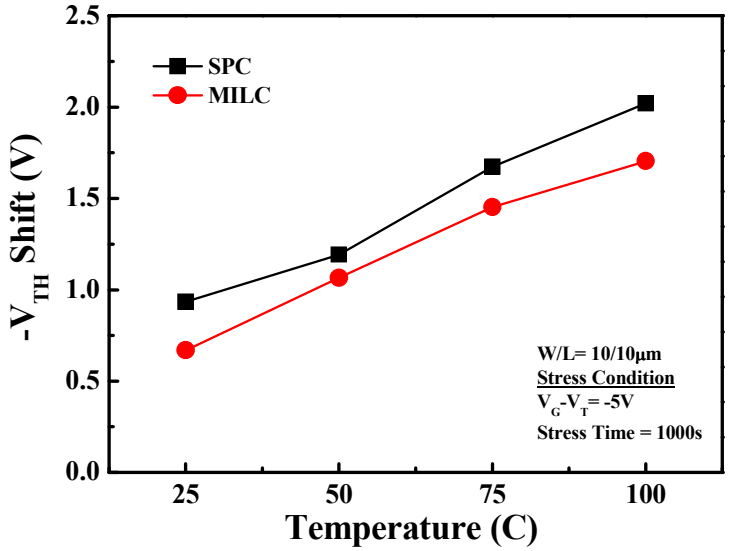
Fig. 8. Dependence of the threshold voltage shift (ΔV_{TH}) versus temperature at various stress voltage with the (a) SPC and (b) MILC device.



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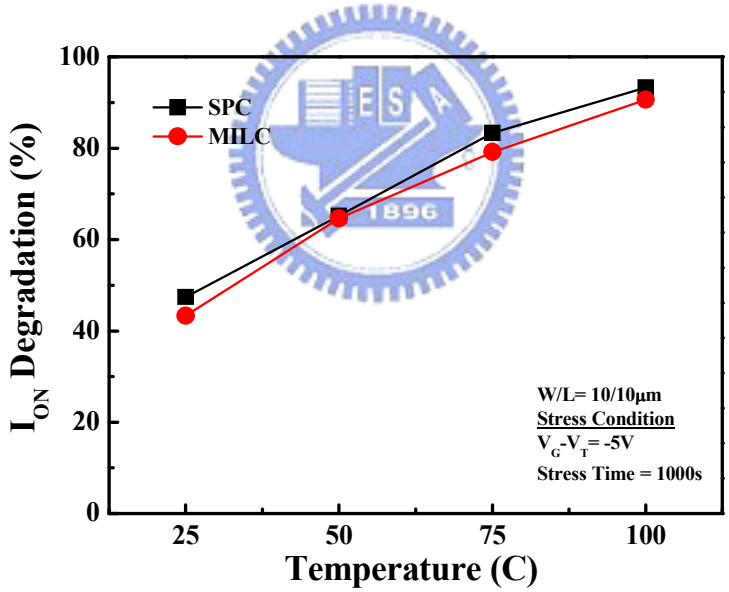
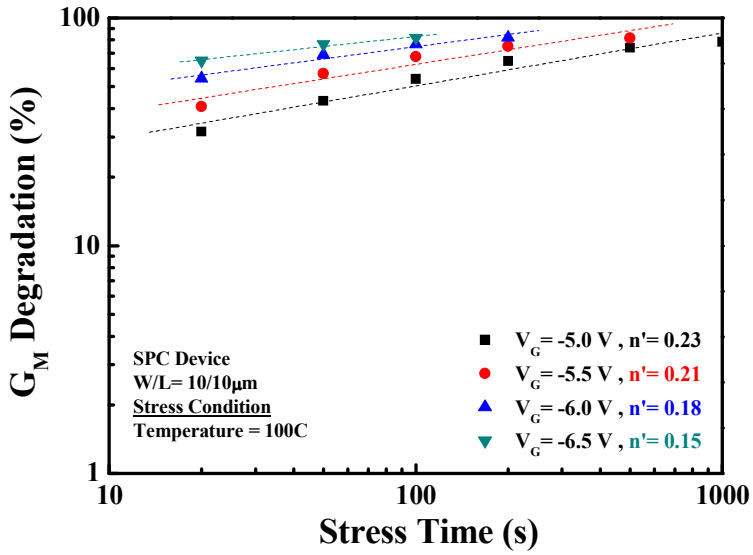


(b)

Fig. 9. Dependence of the (a) threshold voltage shift (ΔV_{TH}) and (b) I_{ON} degradation versus temperature on the same overdrive stress voltage with the SPC and MILC device.



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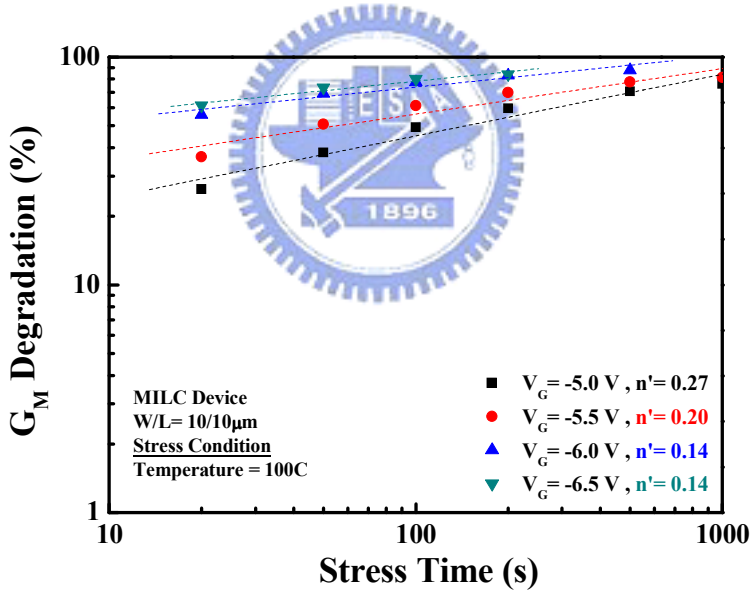
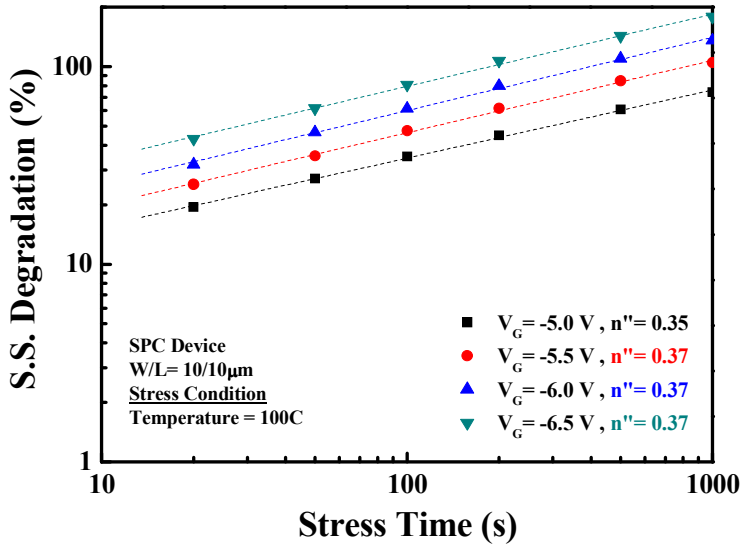


(b)

Fig. 10. Dependence of the transconductance degradation (%G_M) versus stress time at 100℃ with the (a) SPC and (b) MILC device.



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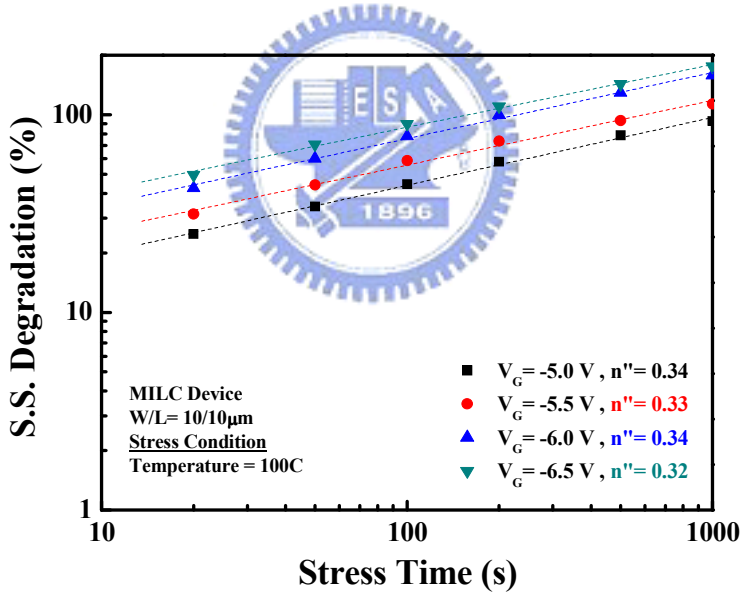
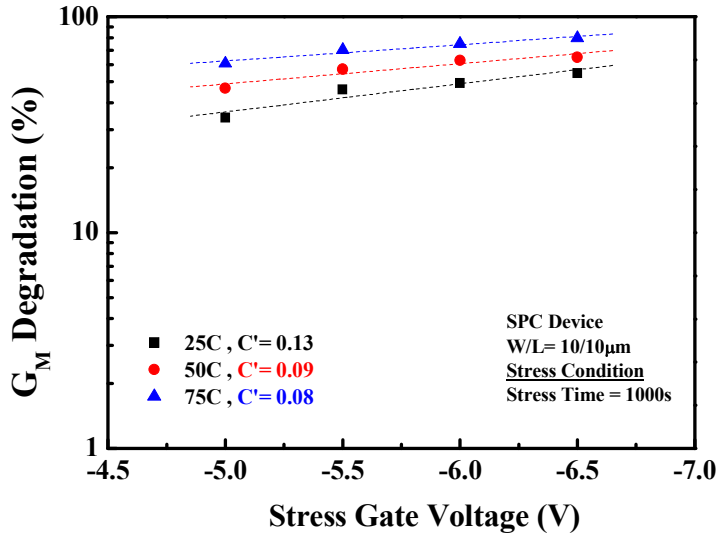


(b)

Fig. 11. Dependence of the subthreshold swing degradation (%S.S.) versus stress time at 100℃ with the (a) SPC and (b) MILC device.



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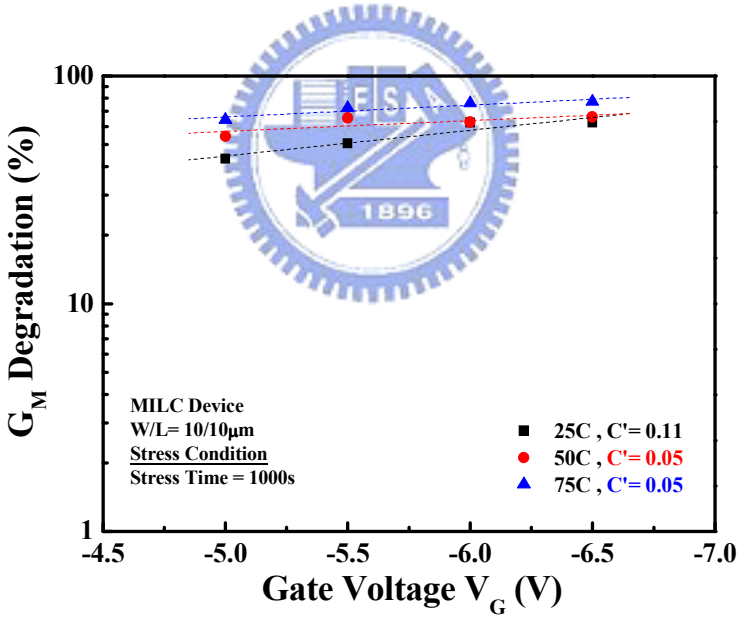
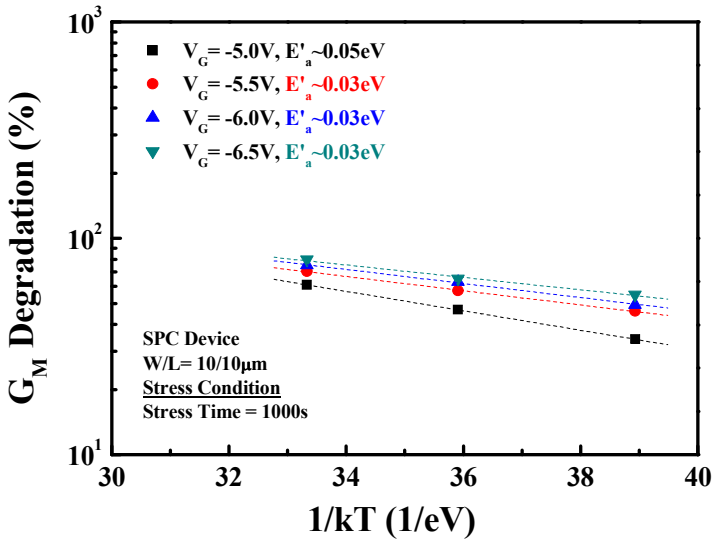


(b)

Fig. 12. Dependence of the transconductance degradation (%G_M) versus stress voltage at various temperature with the (a) SPC and (b) MILC device.



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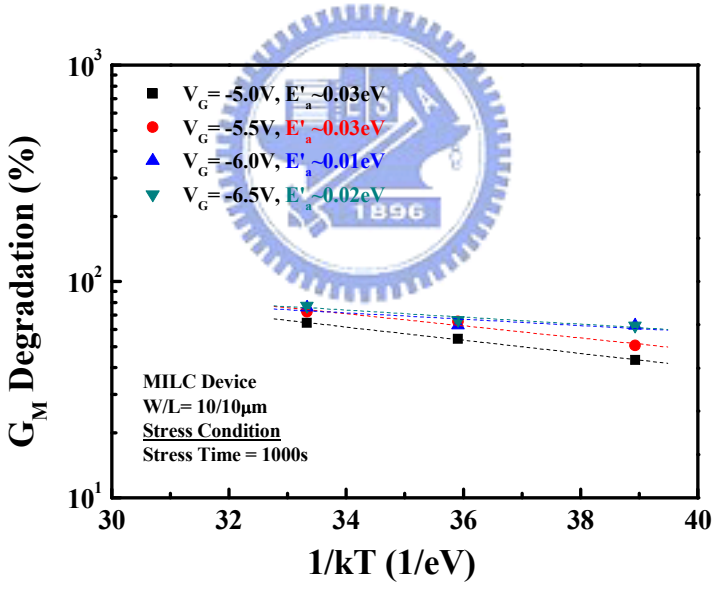
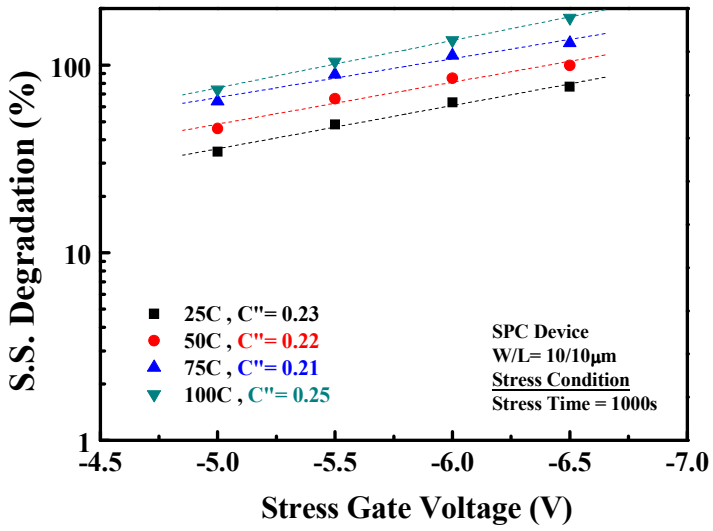


(b)

Fig. 13. Dependence of the transconductance degradation (%G_M) versus temperature at various stress voltage with the (a) SPC and (b) MILC device.



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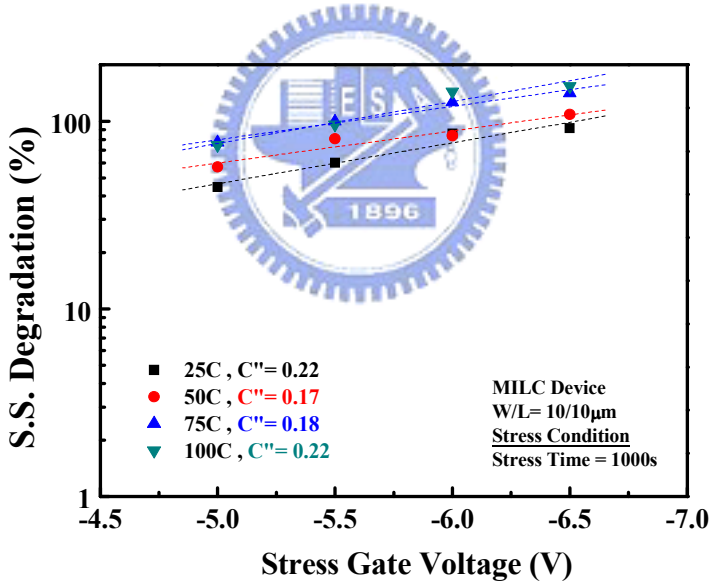
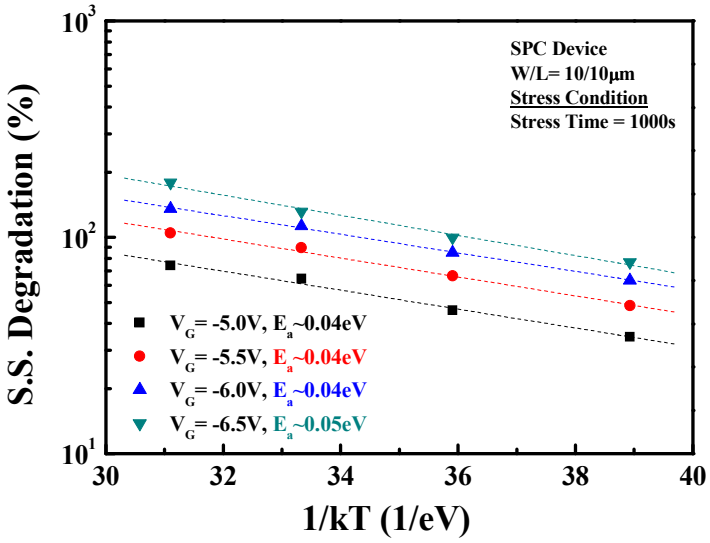


(b)

Fig. 14. Dependence of the subthreshold swing degradation (%S.S.) versus stress voltage at various temperature with the (a) SPC and (b) MILC device.



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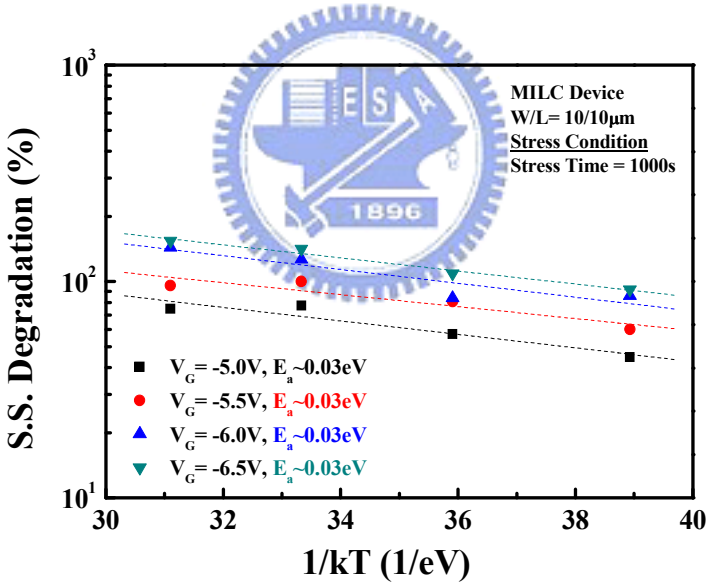


(b)

Fig. 15. Dependence of the subthreshold swing degradation (%S.S.) versus temperature at various stress voltage with the (a) SPC and (b) MILC device.

Chapter 5

Drain Bias Effects on Negative Bias Temperature Instability in LTPS TFTs With HfO_2 Gate Dielectric for SPC and MILC Devices

5.1 Introduction

Negative-bias temperature instability (NBTI) is one of the most important reliability issues in advanced p-channel metal-oxide-silicon field-effect transistors (pMOSFETs). During the stress, large Si–H bonds broken and left numerous trap states at the poly-Si/HfO_2 interface and grain boundaries in channel [5.1]-[5.3]. Those defects could trap the inversion-carriers to degrade carriers transportation. It was observed obviously that electrical characteristic degraded like an increase of threshold voltage (V_{TH}) and degradations in drive current (I_D) or in transconductance (G_M) [5.4][5.5]. Recently, for digital circuits, due to the scaling of gate oxide below 2 nm without corresponding scaling of their supply voltages, this problem become more serious and notable. After a long time of operation, some critical device parameters may be change. The device is said to be fail when this changes of the critical parameter exceed certain threshold. This may cause the circuit to fail such as fail to meet the speed requirement.

On the other hand, low temperature polycrystalline silicon thin-film transistors (LTPS TFTs) are known as attractive candidates for system-on-panel applications [5.6]. For this target, high performance of p-channel LTPS TFTs with HfO_2 gate dielectric are capable of designing the CMOS inverter configuration [5.7]. However, the reliability issue is more serious due to operating at high voltage level. Compared with the pixel switching devices, the driving circuits have to control their output current precisely, which require devices with good electrical stability during

long-time operation [5.4][5.8][5.9]. In general, we widely used the NBTI stress to accelerate testing the device lifetime under the high electric field across gate dielectric.

However, the predictions based on the alone BTI tests, may lead to underestimation of the real lifetime. Under the normal test methodology, devices are stressed under stress gate bias with other electrodes grounded. However, many circuit applications require transistors to operate at high drain bias in addition to a high gate bias, especially for analog and RF circuits. It was found that the BTI characteristics in MOSFETs are strongly affected by the drain bias (V_{DS}) during the stress [5.10][5.11], which may suggest in an erroneous estimation of a device lifetime. Unfortunately, the mixed effects of NBTI and drain bias (V_{DS}) are rarely explored for the LTPS TFTs with high-κ gate dielectric, and the mechanism is not well known. Therefore, it is critical to understand the effect of drain bias on BTI degradation mechanism, and its impact on the circuit reliability at the operation condition.

In this work, by the comprehensive study of device degradation behavior with time, temperature and voltage, we investigated here a degradation behavior for p-channel HfO_2 TFTs that considers both the effects of NBTI and V_{DS}. Based on the results, an empirical model is presented that matches well with the experimental data. Furthermore, the comparison of the effects between SPC and MILC TFT with high-κ gate stack were studied. By analyzing the NBTI characteristics with drain bias V_{DS}, it can aid us to predict real lifetime, accurately.

The NBTI stress was applied to study the degradation-dependent mechanisms by DC I_d-V_g measurement technique. It was performed at the temperature ranging from 25 ℃ to 100℃, and a gate voltage in the range of −5 to −6.5 V. During the stress, source were grounded and drain with bias from 0V to -10V. ΔV_{TH} change was monitored by measuring the drain current–gate voltage ($I_d - V_g$) characteristics at low

drain voltage (-100mV). During $I_d - V_g$ measurement, the range of the gate bias was limited to 0.5 ~ -5V to minimize an additional stress on the device.

5.2 Results and Discussion

Fig.1 and Fig.2 shows the transfer characteristics and output characteristics of the LTPS TFT under constant stress gate voltage (V_{G_STRESS}) and various stress drain voltage (V_{DS_STRESS}), respectively. Obviously, typical NBTI degradation occurs. The threshold voltage shift (ΔV_{TH}), increase of subthreshold swing (S.S.) and degradation of transconductance (G_M) was observed after the stress. It is interesting to note that stress-induced degradation alleviated when stress drain voltage enhanced. The results indicated that considered the effect of drain voltage, NBTI-induced degradation may be overpessimistic. Moreover, the same stressed trends in SPC and MILC reflects the similar degradation-mechanism during the stress.

To investigate the degradation behavior particularly, we try to use the methodology which is performing in conventional NBTI to analyze experimental results, although the effects of drain voltage is not well known. The behavior of threshold-voltage shift (ΔV_{TH}) can be described by the empirically formula [5.4][5.11][5.12]

$$\Delta V_{TH} \propto t^n e^{(-E_a/kT)} e^{B|V_G|} \quad (1)$$

Where n is the time exponent, E_a is the activation energy, and the parameter C is the constant of V_G-dependence [5.4]. ΔV_{TH} have the power law dependence on the stress time, and exponential dependence on V_G and 1/T, respectively.

As shown in Fig.3 – Fig.6, degradation of the threshold-voltage shift versus stress time at various stress drain voltage under different temperature are observed. There are several interesting phenomenon can be note: 1) The shift in the ΔV_{TH} are increases with the stress time and follows a power law dependence (t^n), which is

clearly consistent with the conventional NBTI stress. 2) The ΔV_{TH} decreases rapidly with increasing the V_{DS} first, and then trend to saturation when V_{DS} greater than -6V. 3) The extraction of time-dependence n value exhibited two behavior. When V_{DS} less than -6V, the n value can be deemed almost unvarying constant under any temperature; when V_{DS} greater than -6V, the n value is reduced or enhanced. 4) No matter in SPC or in MILC devices, the same phenomenon can be also obverse after the stress.

Furthermore, it is observed that the exponent *n* value are slightly fluctuation (Fig.3 – Fig.6); this is because, the magnitude of the threshold-voltage shift under NBTI stress is very small (< 1 V for short stress time) causing a larger error value.

From these results, a reliability model was proposed to explain the NBTI degradation with drain bias effect in our experiment. In considering the mechanism of NBTI, the ΔV_{TH} can be expressed as the equation (1). The empirical formula for traditional NBTI indicated threshold-voltage shift (ΔV_{TH}) have the power law dependence on the stress time, and exponential dependence on V_G and 1/T, respectively. According to the previous work [5.13], it can be found that *n* value is independent of stress voltage under the same temperature, and ΔV_{TH} is reduced when the gate stress decreased, as seen in Fig.7. The same behavior only when V_{DS} less than -6V (in Fig.3 – Fig.6) can be also observed clearly. The results suggested that addition of drain voltage (V_{DS}) during the stress could reduce the degree of degradation as same as the degree of stress gate voltage (V_G). When a V_{DS} bias applied to the drain, the voltage drop on the gate dielectric near the drain side decreases and improves the partial NBTI-degradation, as illustrated in Fig.8 .

This phenomenon can be described by a mathematical expression as follows. We assume that the channel potential under V_{DS} effect is expressed by a linear approximation along the channel at low $|V_{DS}|$ (Fig.8), which can be simply expressed

as [5.10][5.11]

$$V(y) = V_{DS} \times (c\frac{y}{L}) \tag{2}$$

Furthermore, the vertical electric field becomes a function of V(y) through the channel, and it is

$$\left|V_{G\_NEW}(y)\right| = |V_G| - |V(y)| \tag{3}$$

By combining Eqs.(1) with Eqs.(3), the new NBTI model with V_{DS} effect is established and rewritten as

$$\Delta V_{TH\_NEW}(y) = \Delta V_{TH} \times e^{-C|V_{DS}|\times(\frac{y}{L})} \tag{4}$$

With the integral along the channel from 0 to L, we can obtain the ΔV_{TH_NEW} as given by [5.10][5.11]

$$\Delta V_{TH\_NEW} = \Delta V_{TH} \times \frac{A(1-e^{-C|V_{DS}|})}{C|V_{DS}|} \tag{5}$$

Where *A* and *C* is the fitting parameter. It is important to note above result which is only applicable when V_{DS} less than the saturation voltage V_{Dsat} (i.e. $V_{Dsat} = V_G - V_T$). In general, it is agreed that holes play critical role in NBTI degradation since they are attracted to channel interface and break the Si-H bond [5.1]-[5.3]. As the drain voltage increases beyond the V_{Dsat}, the channel near the drain is not in inversion, or the pinch-off region (velocity saturation region) generated. The hole concentration in this region almost approach to zero. It also indicated that the potential in all channel is not a linear function ,and Eqs(3) is not appropriate. As a result, the NBTI-induced degradation in this region can be neglected, and other damage mechanism may occur. This simple model can interpret that drain bias effect is equal to decrease of stress gate voltage, and *n* value is independent of drain voltage. In addition, when V_{DS} stress is much higher than V_G stress ($V_{DS} \gg V_G$), it may cause different extra degradation mechanisms, such as hot carrier effect (HCE) [5.14][5.15], electron injection (EI)

[5.8], and channel-hot-hole (CHH) [5.10][5.16]. However, those degradation mechanisms were not discussed in this work.

Fig.9 show the dependence of the threshold voltage shift (ΔV_{TH}) on the stress drain bias at various temperature. The stress was performed with a fixed V_G = -6V and the stress time is 1000s. Based on the above model, the threshold voltage shift (ΔV_{TH}) prediction matches with the experimental curve at low drain bias. In our experiment, the threshold voltage on SPC device is about -1.4V and the saturation voltage is -4.6V. On MILC device, the threshold voltage and the saturation voltage are about -1.1V and -4.9V, respectively. The results also accord with our experiment, that is, a good fit is obtained when $V_{DS} \leqq V_{Dsat}$. From Fig.9, the data exhibits three degradation regions. When V_{DS} was applied initially, the threshold voltage shift (ΔV_{TH}) reduced rapidly. At the low V_{DS} stress condition ($V_{DS} \leqq V_{Dsat}$), ΔV_{TH} decreased with the increase of the V_{DS}, gradually. Once V_{DS} greater than V_{Dsat}, the degradation-behavior turn to saturated. Based on the results shown, the drain bias effects are strongly affected the NBTI-induced stress indeed, which may lead to underestimation of the real device lifetime.

Fig. 10 represent the degradations of the maximum transconductance (G_M) and subthreshold swing (S.S.) under various drain bias. The degradation can be attributed that the generation of deep interface states and tail interface states, during the stress [5.17]. It is know that N_{IT} will trap carriers and generate extra Coulomb scattering to degrade carriers transportation [5.18][5.19], such as enhancement of threshold voltage V_{TH} and subthreshold swing S.S., or reduction of transconductance G_M. We can found that the degradations-behavior show similar trend with the degradations of the ΔV_{TH}. It means that the drain bias effect can improve the generation of N_{IT} by releasing the vertical electric field across gate dielectric, as the same behavior of ΔV_{TH} improvement.

5.3 Summary

The drain bias effect on negative bias temperature instability (NBTI) degradation mechanism in low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) with high-k gate stack is analyzed by the DC measurement technique. Instead of the grounded drain, V_{DS} was applied to reduced the vertical electric field across gate dielectric and improved the NBTI-induced degradation. The results showed the same power law dependence on the stress time and *n* value is independent of stress voltage at any stress temperature, when V_D less than V_{Dsat}. From those data, the NBTI model with drain bias effect is established. A good fit on the threshold voltage shift (ΔV_{TH}) prediction is obtained and confirms our theory.

Finally, we also observed the degradation of the subthreshold swing (S.S.) and maximum transconductance (G_M) under various drain bias. The similar behavior indicated that drain bias effect can improve the generation of N_{IT} by releasing the vertical electric field across gate dielectric, as the same behavior of ΔV_{TH} improvement.

References

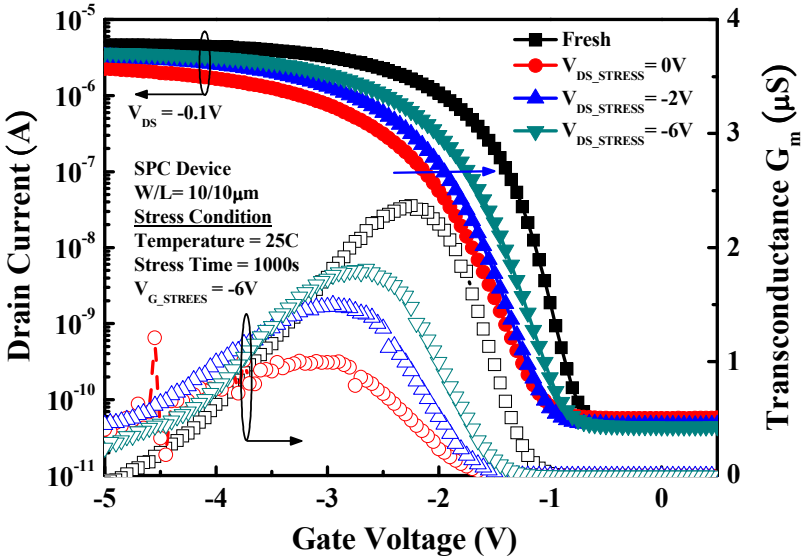
1. S. Mahapatra, P. B. Kumar, M. A. Alam, “Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of pMOSFETs,” *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 1371-1379, 2004.
2. A. T. Krishnan, S. Chakravarthi, P. Nicollian, V. Reddy, S. Krishnan, “Negative bias temperature instability mechanism: The role of molecular hydrogen,” *Applied Physics Letter*, 88, 153518, 2006.
3. S. Rangan, N. Mielke, E. C. C. Yeh, “Universal recovery behavior of negative bias temperature instability,” *IEDM*, pp. 341-344, 2003.
4. C. Y. Chen, J. W. Lee, S. D. Wang, M. S. Shieh; P. H. Lee; W. C. Chen; H. Y. Lin; K. L. Yeh; T. F. Lei, “Negative Bias Temperature Instability in Low-Temperature Polycrystalline Silicon Thin-Film Transistors,” *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2993-3000, 2006.
5. C. Y. Chen, M. W. Ma, W. C. Chen, H. Y. Lin, K. L. Yeh, S. D. Wang, T. F. Lei, **“**Analysis of Negative Bias Temperature Instability in Body-Tied Low-Temperature Polycrystalline Silicon Thin-Film Transistors**,”** *IEEE Electron Device Lett.*, vol. 29, no. 2, pp. 165-167, 2008.
6. Z. Meng, M. Wang, and M. Wong, **“**High Performance Low temperature Metal-Induced Unilaterally Crystallized Polycrystalline Silicon Thin Film Transistors for System-on-Panel Applications,**”** *IEEE Trans. Electron Devices*, vol. 47, pp. 404-409, 2000.
7. M. W. Ma, T. S. Chao, C. J. Su, W. C. Wu, K. H. Kao, T. F. Lei, **“**High-Performance Metal-Induced Laterally Crystallized Polycrystalline Silicon P-Channel Thin-Film Transistor With TaN/HfO_2 Gate Stack Structure,**”** *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 592-594, 2008.
8. C. Hu, M. Wang, B. Zhang, M. Wong, “Negative Bias Temperature Instability

Dominated Degradation of Metal-Induced Laterally Crystallized p-Type Polycrystalline Silicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 4, pp. 587-594, 2009..

9. M. W. Ma, C. Y. Chen, W. C. Wu, C.J. Su, K.H. Kao, T.S. Chao, T. F. Lei, **"**Reliability Mechanisms of LTPS-TFT With HfO_2 Gate Dielectric: PBTI, NBTI, and Hot-Carrier Stress**,"** *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1153-1160, 2008.
10. L. Yuhao, J. Orona, D. Nayak, D. Gitlin, "Mechanism and Modeling of PMOS NBTI Degradation with Drain Bias," IEEE Reliability physics symposium, 2007.
11. C. Y. Chen, J. W. Lee, P. H. Lee, W. C. Chen, H. Y. Lin, K. L. Yeh, M. W. Ma, S. D. Wang, T. F. Lei, "A Reliability Model for Low-Temperature Polycrystalline Silicon Thin-Film Transistors," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 392-394, 2007.
12. C. Hu, M. Wang, B. Zhang, M. Wong, "Negative Bias Temperature Instability Dominated Degradation of Metal-Induced Laterally Crystallized p-Type Polycrystalline Silicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 4, pp. 587-594, 2009.
13. "Negative Bias Temperature Instability in SPC and MILC P-Channel LTPS TFTs with HfO_2 Gate Dielectric," Chapter 4
14. N. A. Hastas, C. A. Dimitriadis, J. Brini, G. Kamarinos, "Hot-carrier-induced degradation in short p-channel nonhydrogenated polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 49, no. 9, pp. 1552-1557, 2002.
15. U. Yukiharu, H. Tomoaki, F. Takashi, K. Tetsuya, T. Yuji, "Hot carrier effects in low-temperature polysilicon thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 40, pp. 2833-2836, 2001.
16. T. Kawamura, M. Matsumura, T. Kaitoh, T. Noda, M. Hatano, T. Miyazawa, M.

Ohkura, “A Model for Predicting On-Current Degradation Caused by Drain-Avalanche Hot Carriers in Low-Temperature Polysilicon Thin-Film Transistors,” *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 109-115, 2009.

17. I I. W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis, A. Chiang, “Passivation Kinetics of Two Types of Defects in Polysilicon TFT by Plasma Hydrogenation,” *IEEE Electron Device Lett.*, vol. 12, no. 4, pp. 181-183, 1991.
18. S. C. Sun, J. D. Plummer, “Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces,” *IEEE Trans. Electron Devices*, vol. 27, no. 8, pp. 1497-1508, 1980.
19. S. Takagi, A. Toriumi, M. Iwase, H. Tango, “On the Universality of Inversion Layer Mobility in Si MOSFET’s: Part I —Effects of Substrate Impurity Concentration,” *IEEE Electron Device Lett.*, vol. 41, no. 12, pp. 2357-2362, 1994



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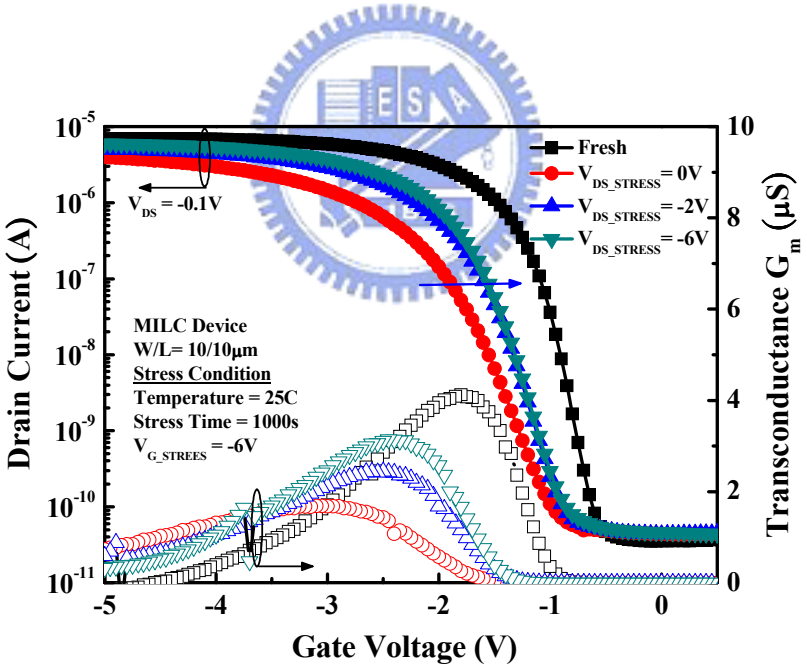
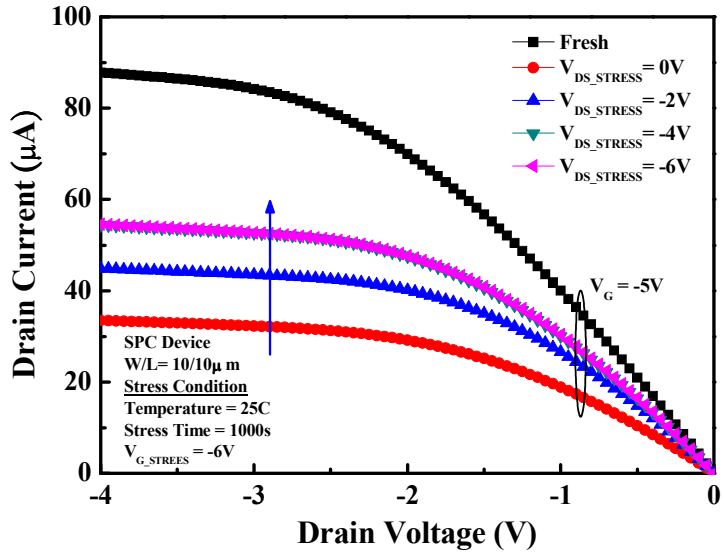


(b)

Fig. 1. Transfer characteristics of (a) SPC and (b) MILC LTPS-TFTs with HfO_2 gate dielectric under constant stress gate voltage (V_{G_STRESS}) and various stress drain voltage (V_{DS_STRESS}).



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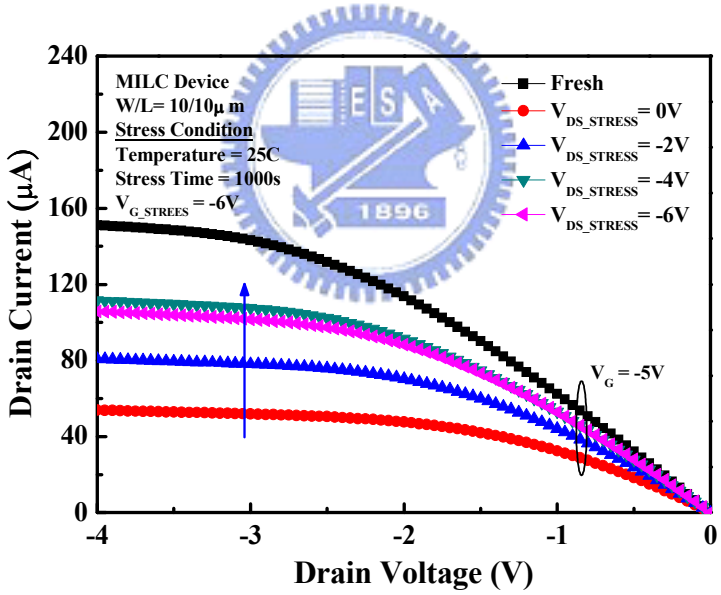
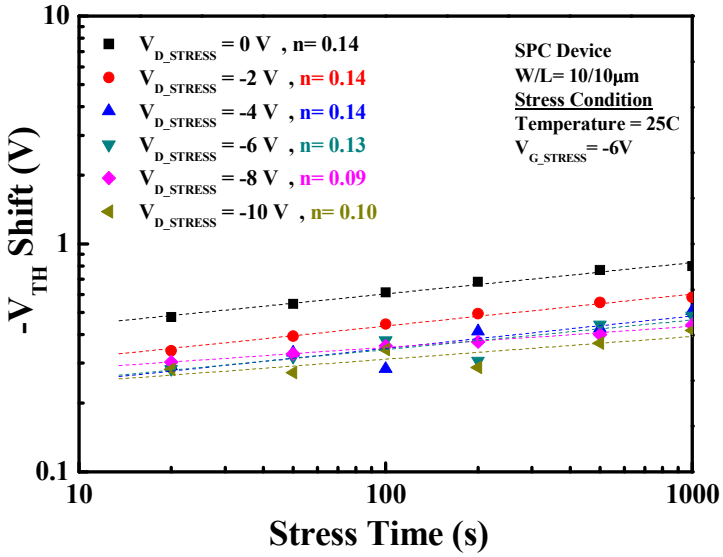


(b)

Fig. 2. Output characteristics of (a) SPC and (b) MILC LTPS-TFTs with HfO_2 gate dielectric under constant stress gate voltage (V_{G_STRESS}) and various stress drain voltage (V_{DS_STRESS}).



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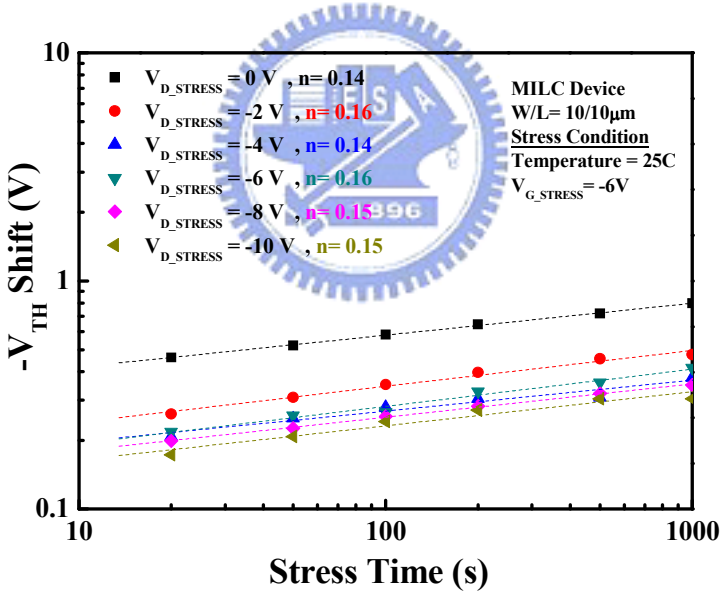
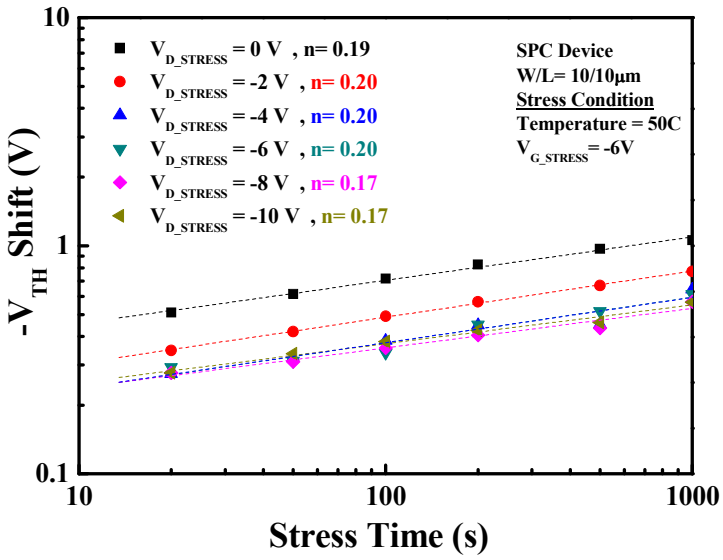


(b)

Fig. 3. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress time at 25℃ under various V_{DS_STRESS} with the (a) SPC and (b) MILC device.



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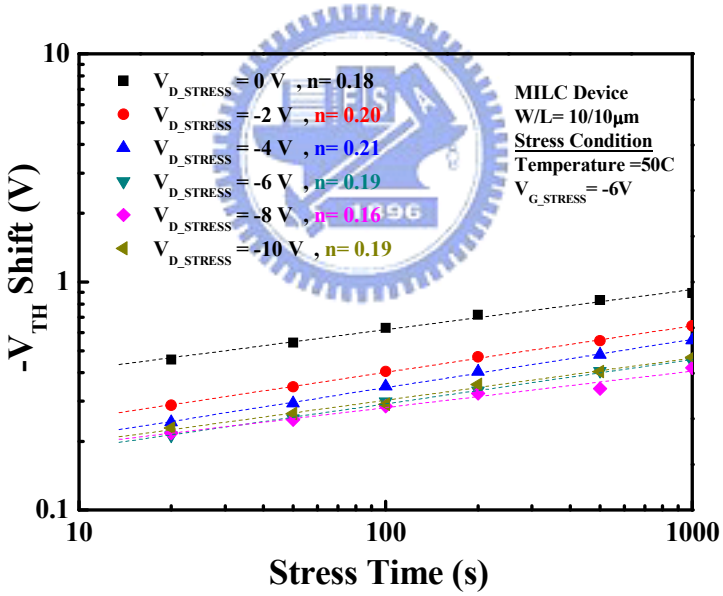
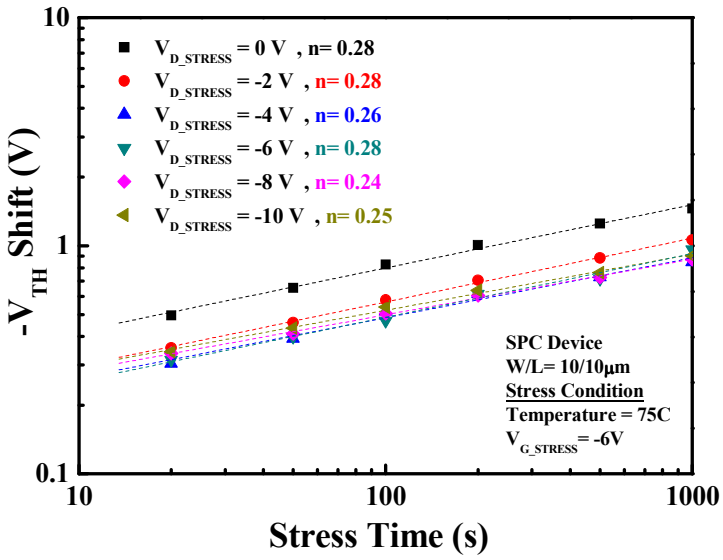


(b)

Fig. 4. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress time at 50℃ under various V_{DS_STRESS} with the (a) SPC and (b) MILC device.



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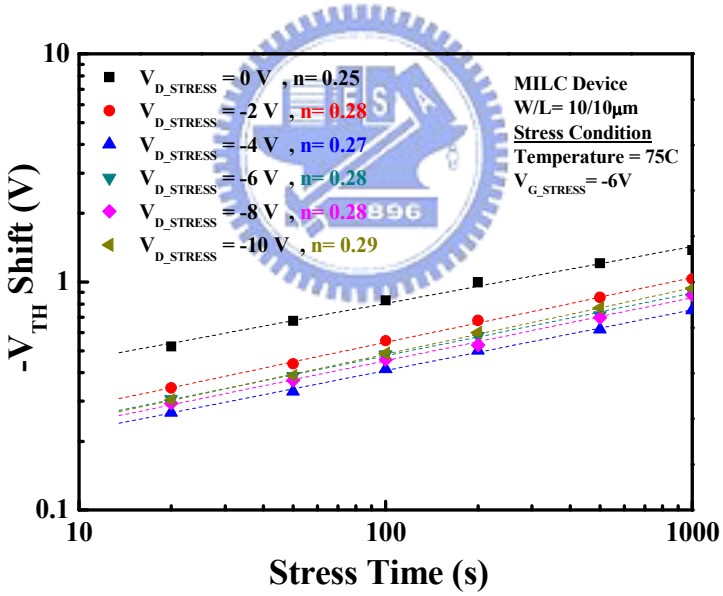

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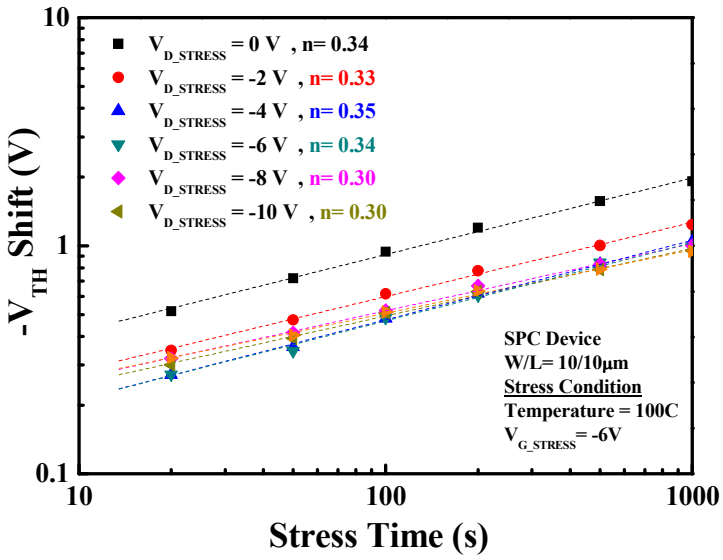
Fig. 5. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress time at 75℃ under various V_{DS_STRESS} with the (a) SPC and (b) MILC device.



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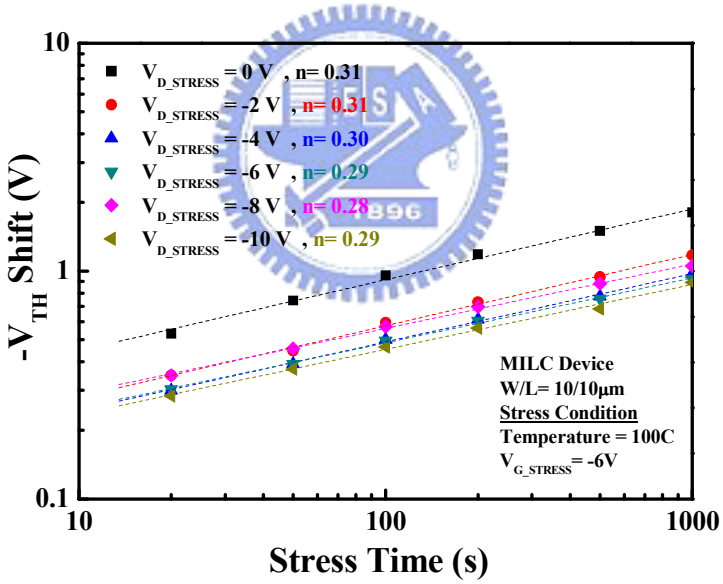

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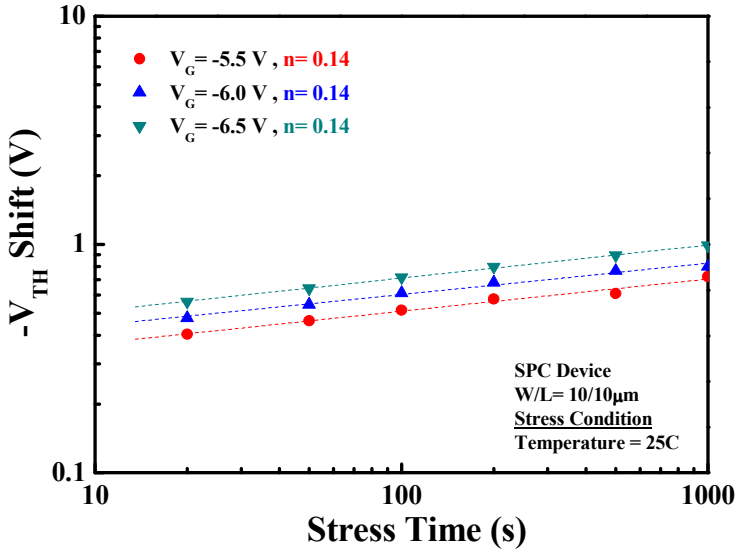
Fig. 6. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress time at 100℃ under various V_{DS_STRESS} with the (a) SPC and (b) MILC device.



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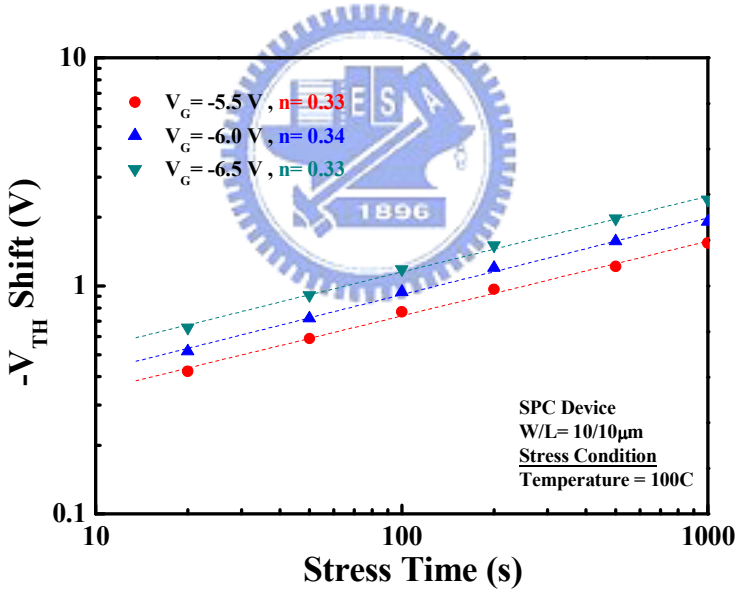

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Fig. 7. Dependence of the threshold voltage shift (ΔV_{TH}) versus stress time at (a)25℃ and (b)100℃ on the SPC device.

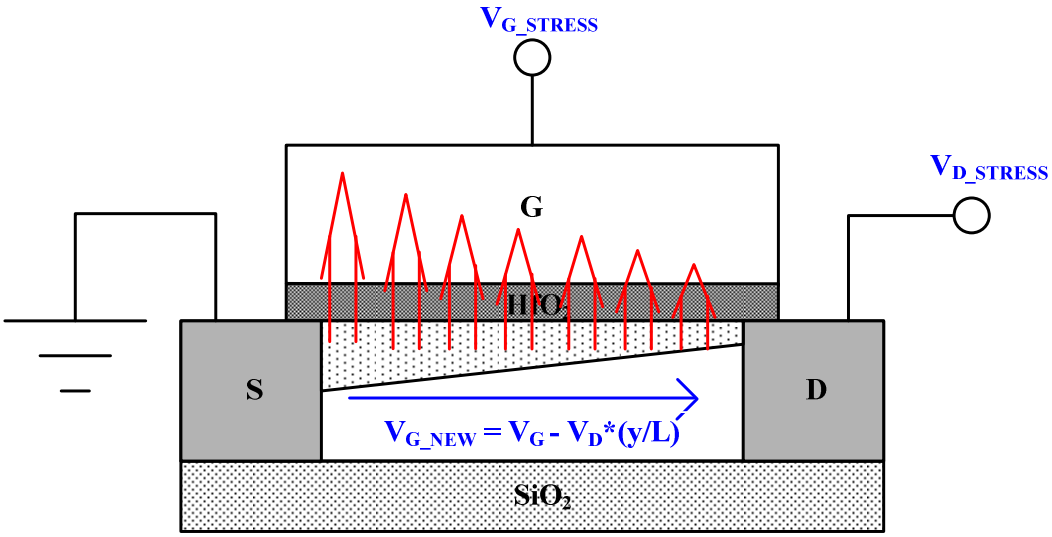
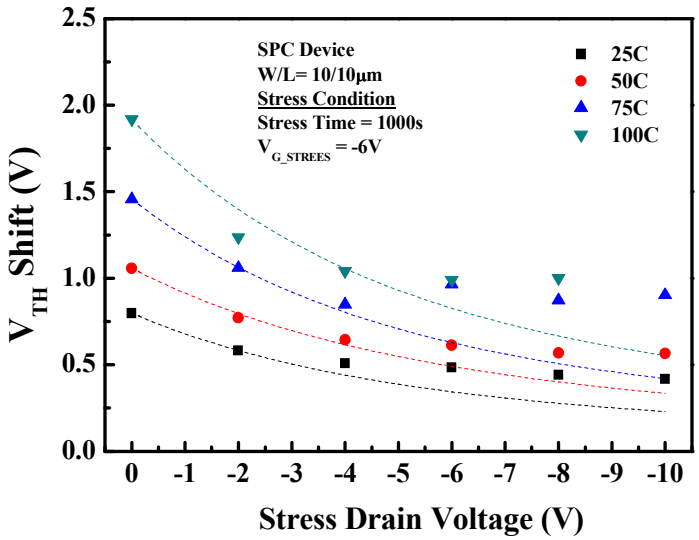


Fig. 8. Schematic of the NBTI stress with drain bias, showing the reduction of gate oxide electrical field along the channel.



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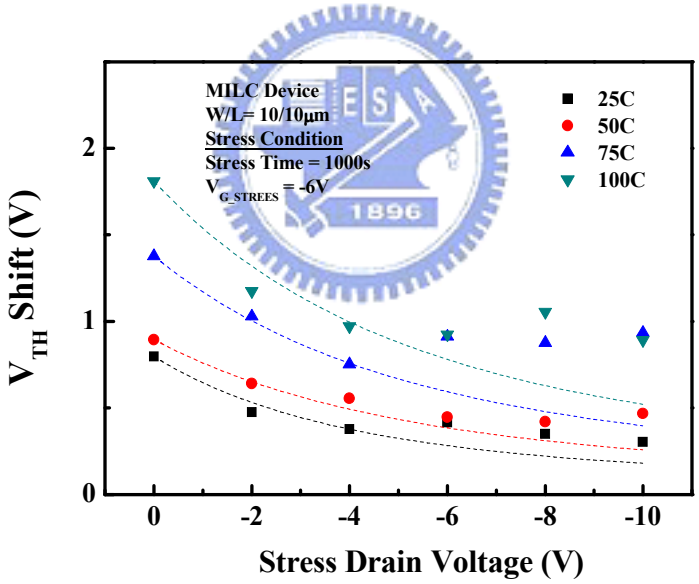

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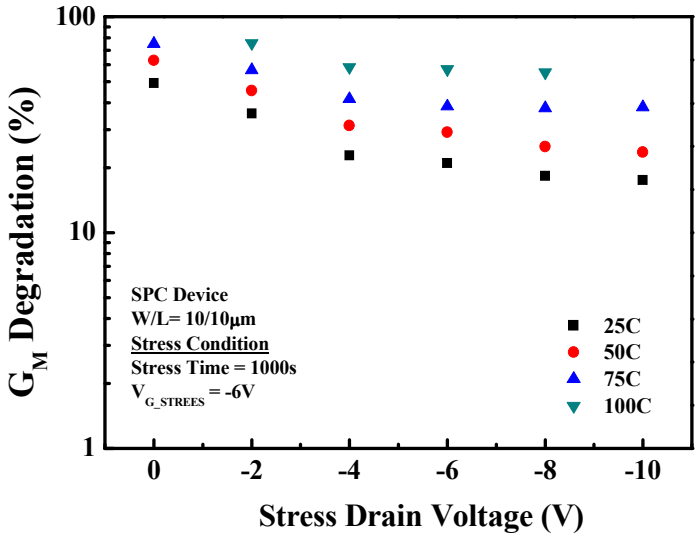
Fig. 9. Measured (solid dot) and predicted (dotted line) threshold voltage shift (ΔV_{TH}) as a function of drain bias at various temperature.



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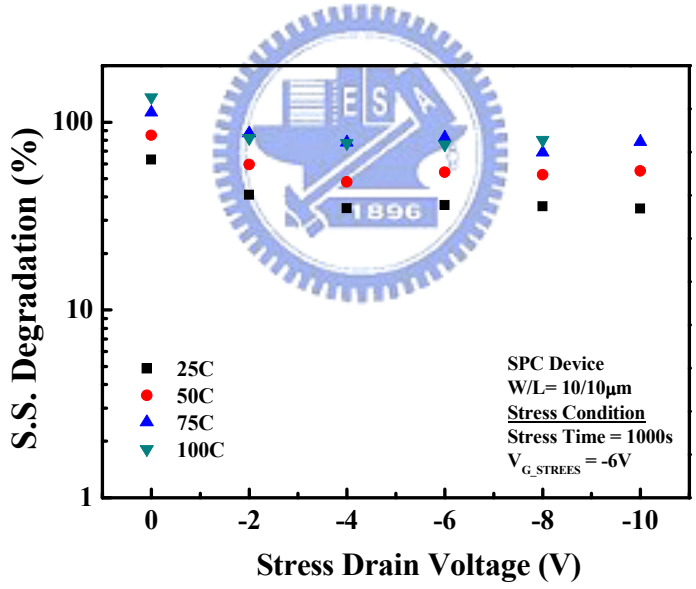

(b)

Fig. 10. Dependence of the (a) transconductance degradation (%G_M) and (b) subthreshold swing degradation (%S.S.) versus drain bias at various temperature with the SPC device.

Chapter 6

Conclusions

In this work, high performance p-channel low temperature poly-silicon thin-film transistors (LTPS-TFTs) are fabricated by the employment of HfO_2 gate dielectric and two crystallization methods, solid phase crystallization (SPC) and metal-induced laterally crystallization (MILC), for comparison. High filed effect mobility μ_{FE} ~ 114 and 215 cm^2/V-s, ultra-low subthreshold swing S.S. ~ 145 and 107 mV/decade, and low threshold voltage V_{TH} ~ -1.05 and -0.75 V are derived from SPC- and MILC-TFT with HfO_2 gate dielectric, respectively. These excellent electrical characteristics are due to low trap states and much higher gate capacitance density with equivalent oxide thickness EOT ~ 12.3nm, resulting in lower operation voltage within 2-V of LTPS-TFT without any passivation method. Excellent performance of SPC and MILC TFT with HfO_2 gate dielectric are demonstrated for the application of SOP and three-dimension integration of VLSI technology.

The negative bias temperature instability (NBTI) degradation mechanism in LTPS TFTs with HfO_2 gate dielectric has been investigated with a conventional DC measurement technique. Besides, the reliability comparisons for SPC and MILC devices have been studied systematically. We used the previously empirical formula for traditional NBTI in SiO_2 to analyze the high-κ gate dielectric in our experiment. The results showed that the threshold-voltage shift (ΔV_{TH}) have almost the same power law dependence on the stress time, and same exponential dependence on V_G and 1/T. According to the results, we demonstrated that NBTI degradation in our experiment is more dominated by the generation of interface trap states (N_{IT}). The coincidence of stressed trends measured in SPC and MILC reflects the similar degradation-mechanism for NBTI stress. Moreover, the results exhibited that MILC

devices have more stability characteristic than SPC during the NBTI stress. Compared with transconductance (G_M), the subthreshold swing (S.S.) degradation behavior is more consistent with the threshold voltage shift (ΔV_{TH}).

Finally, the drain bias effect on NBTI degradation mechanism in this work is analyzed. Instead of the grounded drain, V_{DS} was applied to reduced the vertical electric field across gate dielectric and released the NBTI-induced degradation. When V_D less than V_{Dsat}, it showed the same power law dependence on the stress time and *n* value is independent of stress voltage at any stress temperature. The results suggested that addition of drain voltage (V_{DS}) during the stress could reduce the degree of degradation as same as the degree of stress gate voltage (V_G). From those data, the NBTI model with drain bias effect is established. A good fit on the threshold voltage shift (ΔV_{TH}) prediction is obtained and confirms our theory. The similar behavior indicated that drain bias effect can improve the generation of N_{IT} by releasing the vertical electric field across gate dielectric, as the same behavior of ΔV_{TH} improvement.

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具高介電常數閘極絕緣層之低溫多晶矽薄膜電晶體可靠度研究

Investigation on Reliability of LTPS-TFTs With High-κ Gate Dielectrics