

# Chapter 2

## Wireless LAN Radio Receiver

Wireless LANs allow for easy portable communications and eliminate the installation cost associated with wired LANs. Laptop computers nowadays are attached with WLAN as fundamental connectivity interfaces to increase the value of the product and the affordability of wireless data access together with highly developed internet environment make the success of WLAN markets more fruitful. Behind the market, the standardization allowing seamless interoperation between various wireless devices plays an important role to make WLAN available worldwide. Therefore, understanding the requirements for WLAN is necessary for the design of a WLAN receiver. The overview of various WLAN standards is introduced in Section 2.1. After that, Section 2.2 describes the radio specifications of WLAN standards, and the specifications for receivers intended for WLAN are then derived in Section 2.3. Section 2.4 and Section 2.5 are devoted to discussing the architecture of the receiver and the requirements of the building blocks of the receiver in detail.

### 2.1 Overview of Wireless LAN Standards

IEEE adopted the first standard for WLANs (IEEE Std 802.11-1997 [1]) in 1997 and revised in 1999 (802.11a [2] and 802.11b [3]) and 2003 (802.11g [4]). IEEE

Table 2.1: Wireless LAN Standards.

Designation	Frequency (GHz)	Modulation	Max. Data Rate (Mbps)
802.11	2.4	DSSS, FHSS	2
802.11b	2.4	CCK, PBCC	11, 22
802.11g	2.4	OFDM	54
802.11a	5	OFDM	54
HIPERLAN/2	5	OFDM	54

Std 802.11-1997 defines three physical (PHY) layers including an infrared (IR) baseband PHY, a frequency hopping spread spectrum (FHSS) radio and a direct sequence spread spectrum (DSSS) radio in the 2.4-GHz ISM band. All three PHY layers specifies 1 and 2 Mbps of data rate. IEEE Std 802.11b enhances the highest data rate to 11 Mbps with complimentary code keying (CCK) or 22 Mbps with packet binary convolutional coding (PBCC) modulation schemes while 802.11a and 802.11g extends the highest data rate to 54 Mbps with orthogonal frequency division multiplexing (OFDM) in 5-GHz UNII band and 2.4-GHz, respectively. There are hopes that next-generation wireless LAN will deliver throughputs of over 100 Mbps. The IEEE802.11n Task Group (TGn) will begin accepting standard proposals from March 2004, but informal negotiations have been underway for some time [5].

European Telecommunications Standards Institute (ETSI) also revised a wireless LAN standard for High Performance Radio Local Area Network type 2 (HIPERLAN/2) [6]. The physical layer specifications are quite similar to that of IEEE 802.11a with only a little differences. Table 2.1 summarizes various WLAN specifications.

## 2.2 Wireless LAN Radio Specifications

The radio specifications of WLAN standards include both receive and transmit parts, however, the main focus of the work is on receiver design and therefore the transmit radio specifications are omitted hereafter.

Table 2.2: Frequency Bands of various WLAN standards.

Designation	Frequency Bands (GHz)	Channel spacing (MHz)
802.11b/g	2.4-2.483	5/20
802.11a	5.15-5.35, 5.725-5.825	20
HIPERLAN/2	5.15-5.35, 5.47-5.725	20

### 2.2.1 Frequency Bands

Table 2.2 shows the frequency bands and channel spacings of 802.11 and HIPERLAN/2 standards. Although 802.11a and HIPERLAN/2 both adopt OFDM as the modulation scheme and operate at 5-GHz band, the frequency channels are not the same at the upper bands.

### 2.2.2 Sensitivity

The sensitivity specifications for WLAN standards depend on the data rate and modulation schemes. The packet error rate (PER) shall be less than 10% at a PSDU (PHY sublayer service data units) length of 1000 bytes for rate-dependent input levels shall be the numbers listed in Table 2.3. Note that IEEE mandates 802.11g to be back compatible to 802.11b, and therefore the sensitivity for 802.11g are the same as that of 802.11b and 802.11a.

### 2.2.3 Maximum Input Level

The maximum input signal level as well as the sensitivity determines the dynamic range of a wireless LAN receiver. The PER shall be less than 10% at a PSDU length of 1000 bytes for the maximum input levels measured at the antenna for any baseband modulation as shown in Table 2.4.

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Table 2.3: Rate-dependent sensitivity specifications for various WLAN standards.

Designation	802.11b/g	802.11a/g	HIPERLAN/2
Data rate (Mbps)	Sensitivity (dBm)	Sensitivity (dBm)	Sensitivity (dBm)
1	-83		
2	-80		
5.5	-79		
11	-76		
6		-82	-85
9		-81	-83
12		-79	-81
18		-77	-79
24		-74	
27			-75
36		-70	-73
48		-66	
54		-65	-68

Table 2.4: Maximum input signal levels.

Designation	Maximum Input Level (dBm)
802.11b	-10 (CCK-11Mbps)
802.11a	-30
802.11g	-20 (Extended Rate PHY)
HIPERLAN/2	-20 (Class 1), -30 (Class 2)

Table 2.5: Adjacent/Non-adjacent channel rejection specifications.

Data Rate (Mbps)	802.11b/g	802.11a/g		HIPERLAN/2	
	Adj. (dB)	Adj. (dB)	Non-adj. (dB)	Adj. (dB)	Non-adj.(dB)
11	35				
6		16	32	21	40
9		15	31	19	38
12		13	29	17	36
18		11	27	15	34
24		8	24		
27				11	30
36		4	20	9	28
48		0	16		
54		-1	15	4	23

### 2.2.4 Adjacent and Non-adjacent Channel Rejection

The adjacent or non-adjacent(alternative) channel rejection is measured by setting the desired signal's strength 3 dB (6 dB for 802.11b) above the mode-dependent sensitivity and raising the power of the interfering signal until 10% PER is caused for a PSDU length of 1000 bytes. The required adjacent and non-adjacent channel rejection ratios for various WLAN standards are shown in Table 2.5

### 2.2.5 Receiver Input Blocking

Receiver blocking specifies that the sensitivity of the receiver is degraded in the presence of strong interfering signals due to overloading of receiver stages. The blocking level defines the maximum input power level for an interferer the receiver should be able to operate with. IEEE 802.11a/b/g standards do not define receiver input blocking levels, however, HIPERLAN/2 does. The blocking characteristics of the receiver for HIPERLAN/2 are specified for different frequency ranges as identified in Table 2.6.

Table 2.6: Receiver input blocking levels for HIPERLAN/2.

Frequency of the interference	Blocking level	Spurious response level
100 kHz ... 2,5 GHz	0 dBm	-20 dBm
4,5 ... 5,15 GHz	-30 dBm	-40 dBm
5,15 GHz ... $f_c-50$ MHz	-30 dBm	-40 dBm
$f_c+50$ MHz ... 5,35 GHz	-30 dBm	-40 dBm
5,35 ... 5,47 GHz	-30 dBm	-40 dBm
5,47 GHz ... $f_c-50$ MHz	-30 dBm	-40 dBm
$f_c+50$ MHz ... 5,725 GHz	-30 dBm	-40 dBm
5,725 GHz ... 7 GHz	-30 dBm	-40 dBm
7 GHz ... 13 GHz	-20 dBm	-40 dBm

## 2.3 Receiver Specification Calculation

The required radio receiver specifications such as noise figure, input-referred third-order intermodulation intercept point (IIP3) and so on can be calculated with the radio specifications defined by WLAN standards. The calculation equations are described as follows. With these equations in hand, the receiver specifications can be estimated and the calculation can be easily achieved with a spread sheet created in Excel. The specifications for IEEE 802.11b, 802.11a/g and HIPERLAN/2 are summarized in Table 2.7, 2.8 and 2.9, respectively.

### 2.3.1 Noise Figure

The required noise figure of a receiver ( $F_{\text{overall}}$ ) and integrated part of the receiver ( $F_{\text{integrated}}$ ) can be determined from the sensitivity specification ( $P_{\text{in,min}}$ ) and the required signal to noise ratio ( $SNR_{\text{required}}$ ). Considering the loss ( $L_{\text{filter,switch}}$ ) of a passive filter and a switch precedent to the low noise amplifier and design margin ( $DM$ ), the noise figure can be determined by the following equations where

## 2.3. RECEIVER SPECIFICATION CALCULATION

Table 2.7: Radio receiver specifications for IEEE 802.11b WLAN.

Radio Standards Specifications						
Data Rate	1	2	5.5	11	Mbps	
Bandwidth	22	22	22	22	MHz	
Sensitivity	-83	-80	-79	-76	dBm	
Bit Error Rate	1E-5	1E-5	1E-5	1E-5		
Modulation	DBPSK	DQPSK	CCK	CCK		
SNR required	1.0	5.0	4.5	8.5	dB	
Adjacent Channel Rejection	35	35	35	35	dB	
Receiver Noise Figure						
$P_{in,min}$	-83	-80	-79	-76	dBm	
$kTB$	-100.3	-100.3	-100.3	-100.3	dBm	
Loss precedent to LNA	3	3	3	3	dB	
Design Margin	5.3	4.3	5.8	4.8	dB	
Overall NF	11	11	11	11	dB	
Integrated NF	8	8	8	8	dB	
System Noise Floor	-89.5	-89.5	-89.5	-89.5	dBm	
Third-order IM Intercept Point						
$P_{desired}$	-77	-74	-73	-70	dBm	
$P_{blocker}$	-42	-39	-38	-35	dBm	
Input IP3	-24	-19	-18.3	-13.3	dBm	
Input $P_{-1dB}$	-34	-29	-28.3	-23.3	dBm	
SFDR,3rd	43.3	47.3	46.8	50.8	dBm	
Second-order IM Intercept Point						
$P_{desired}$	-77	-74	-73	-70	dBm	
$P_{blocker}$	-42	-39	-38	-35	dBm	
Input IP2	-6	1	1.5	8.5	dBm	
Image Rejection Ratio						
In-band $P_{image}$	-42	-39	-38	-35	dBm	
Out-of-band $P_{image}$	-27	-27	-27	-27	dBm	
$P_{desired}$	-83	-80	-79	-76	dBm	
In-band Image Rejection Ratio	42	46	45.5	49.5	dB	
Out-of-band Image Rejection Ratio	57	58	56.5	57.5	dB	

the dimensions of variables are in logarithm scale.

$$P_{in,min} \equiv 10 \log(kTB) + F_{overall} + SNR_{required} + DM \quad (2.1)$$

$$F_{overall} \leq P_{in,min} - 10 \log(kTB) - SNR_{required} - DM \quad (2.2)$$

$$F_{overall} = L_{filter,switch} + F_{integrated} \quad (2.3)$$

Examine the tables, the design margin for HIPERLAN/2 is 2-3 dB less than that for IEEE 802.11a/g, because of the sensitivity specifications of the former standard is 2-3 dB more stringent than the later.

### 2.3.2 Third Order Intermodulation

The third order intermodulation characteristic of the receiver is specified by the third order intermodulation intercept point (IP3). The required IP3 referred to the receiver input can be determined from the adjacent and non-adjacent channel rejection specifications as shown in Eq. (2.4).

$$IIP3 = \frac{3 \cdot P_{\text{blocker}} - P_{\text{desired}} + SNR_{\text{required}}}{2} \quad (2.4)$$

where  $P_{\text{blocker}}$  is the adjacent or non-adjacent channel blocker level. IIP3 specifications are usually limited by non-adjacent channel rejection specifications because large blockers are allowed to present in non-adjacent channels.

### 2.3.3 Second Order Intermodulation

The second order nonlinear effect is critical for direct conversion receivers because the second order intermodulation produces low frequency terms that may directly leak to baseband and corrupt the signal. The specification to characterize the second order effect is IP2. The required input IP2 for the receiver can also be calculated from the adjacent and non-adjacent channel rejection specifications as shown in Eq. (2.5).

$$IIP2 = 2 \cdot P_{\text{blocker}} - P_{\text{desired}} + SNR_{\text{required}} \quad (2.5)$$

The IP2 and IP3 specifications for HIPERLAN/2 are more rigorous than that for IEEE 802.11a/g since the receivers for HIPERLAN/2 should resist larger non-adjacent channel interferer than IEEE 802.11a/g.

### 2.3.4 Image Rejection Ratio

The image rejection specification is necessary for those receivers with intermediate frequencies such as heterodyne and low-IF architectures. The required image



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Table 2.8: Radio receiver specifications for IEEE 802.11a/g WLAN.

Radio Standards Specifications									
Data Rate	6	9	12	18	24	36	48	54	Mbps
Bandwidth	20	20	20	20	20	20	20	20	MHz
Sensitivity	-82	-81	-79	-77	-74	-70	-66	-65	dBm
Bit Error Rate	1E-5	1E-5	1E-5	1E-5	1E-5	1E-5	1E-5	1E-5	
Modulation	BPSK	BPSK	QPSK	QPSK	16QAM	16QAM	64QAM	64QAM	OFDM
SNR required	3.0	4.0	6.0	8.0	11.0	15.0	19.0	20.0	dB
Adjacent Channel Rej.	16	15	13	11	8	4	0	-1	dB
Non-adjacent Channel Rej.	32	31	29	27	24	20	16	15	dB
Receiver Noise Figure									
$P_{in,min}$	-82	-81	-79	-77	-74	-70	-66	-65	dBm
kTB	-100.7	-100.7	-100.7	-100.7	-100.7	-100.7	-100.7	-100.7	dBm
Loss precedent to LNA	3	3	3	3	3	3	3	3	dB
Design Margin	4.7	4.7	4.7	4.7	4.7	4.7	4.7	4.7	dB
Overall NF	11	11	11	11	11	11	11	11	dB
Integrated NF	8	8	8	8	8	8	8	8	dB
System Noise Floor	-90	-90	-90	-90	-90	-90	-90	-90	dBm
Third-order IM Intercept Point									
$P_{desired}$	-79	-78	-77	-74	-71	-67	-63	-62	dBm
$P_{blocker}$	-47	-47	-47	-47	-47	-47	-47	-47	dBm
Input IP3	-29.5	-29.5	-29.5	-29.5	-29.5	-29.5	-29.5	-29.5	dBm
Input $P_{-1dB}$	-39.5	-39.5	-39.5	-39.5	-39.5	-39.5	-39.5	-39.5	dBm
SFDR,3rd	40.3	40.3	40.3	40.3	40.3	40.3	40.3	40.3	dBm
Second-order IM Intercept Point									
$P_{desired}$	-79	-78	-77	-74	-71	-67	-63	-62	dBm
$P_{blocker}$	-47	-47	-47	-47	-47	-47	-47	-47	dBm
Input IP2	-12	-12	-12	-12	-12	-12	-12	-12	dBm
Image Rejection Ratio (IRR)									
In-band $P_{image}$	-47	-47	-47	-47	-47	-47	-47	-47	dBm
Out-of-band $P_{image}$	-27	-27	-27	-27	-27	-27	-27	-27	dBm
$P_{desired}$	-82	-81	-79	-77	-74	-70	-66	-65	dBm
In-band IRR	38	38	38	38	38	38	38	38	dB
Out-of-band IRR	58	58	58	58	58	58	58	58	dB

rejection ratio (IRR) is determined with Eq. (2.6).

$$IRR_{required} = P_{image} - P_{desired} + SNR_{required} \quad (2.6)$$

For in-band images, the required image reject ratio is determined with receiver blocking specifications of WLAN standards. Since IEEE 802.11a/b/g do not specify the receiver blocking levels, the in-band image rejection ratio is calculated with the non-adjacent channel interferers. The in-band image rejection ratio is important for receivers designed in low-IF architecture, since the performance of low-IF architecture is very sensitive to the image rejection ratio. The image rejection ratio of a low-IF receiver is limited by the mismatch in the in-phase and

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Table 2.9: Radio receiver specifications for HIPERLAN/2.

Radio Standards Specifications								
Data Rate	6	9	12	18	27	36	54	Mbps
Bandwidth	20	20	20	20	20	20	20	MHz
Sensitivity	-85	-83	-81	-79	-75	-73	-68	dBm
Bit Error Rate	1E-5	1E-5	1E-5	1E-5	1E-5	1E-5	1E-5	
Modulation	BPSK	BPSK	QPSK	QPSK	16QAM	16QAM	64QAM	OFDM
SNR required	3.0	4.0	6.0	8.0	12.0	15.0	20.0	dB
Adjacent Channel Rej.	21	19	17	15	11	9	4	dB
Non-adjacent Channel Rej.	40	38	36	34	30	28	23	dB
Receiver Noise Figure								
$P_{in,min}$	-85	-83	-81	-79	-75	-73	-68	dBm
kTB	-100.7	-100.7	-100.7	-100.7	-100.7	-100.7	-100.7	dBm
Loss precedent to LNA	3	3	3	3	3	3	3	dB
Design Margin	1.7	2.7	2.7	2.7	2.7	1.7	1.7	dB
Overall NF	11	11	11	11	11	11	11	dB
Integrated NF	8	8	8	8	8	8	8	dB
System Noise Floor	-90	-90	-90	-90	-90	-90	-90	dBm
Third-order IM Intercept Point								
$P_{desired}$	-82	-80	-78	-76	-72	-70	-65	dBm
$P_{blocker}$	-42	-42	-42	-42	-42	-42	-42	dBm
Input IP3	-20.5	-21	-21	-21	-21	-20.5	-20.5	dBm
Input $P_{-1dB}$	-30.5	-31	-31	-31	-31	-30.5	-30.5	dBm
SFDR,3rd	46.3	46	46	46	46	46.3	46.3	dBm
Second-order IM Intercept Point								
$P_{desired}$	-82	-80	-78	-76	-72	-70	-65	dBm
$P_{blocker}$	-42	-42	-42	-42	-42	-42	-42	dBm
Input IP2	1	0	0	0	0	1	1	dBm
Image Rejection Ratio (IRR)								
In-band $P_{image}$	-30	-30	-30	-30	-30	-30	-30	dBm
Out-of-band $P_{image}$	-30	-30	-30	-30	-30	-30	-30	dBm
$P_{desired}$	-85	-83	-81	-79	-75	-73	-68	dBm
In-band IRR	58	57	57	57	57	58	58	dB
Out-of-band IRR	58	57	57	57	57	58	58	dB

quadrature-phase signal paths (I/Q mismatch). Typically, the image rejection ratio for 1 % amplitude error and 1° phase error is about 40 dB. Obviously, for IEEE 802.11b and HIPERLAN/2 there is almost no design tolerance for I/Q mismatch and for IEEE 802.11a/g the mismatch of 1 % amplitude error and 1° phase error is tolerable.

## 2.4 Receiver Architecture

The capability of CMOS technology on wireless radio transceiver in the microwave and RF frequency has been presented in many literatures. The trend of the current CMOS wireless transceiver is to achieve a higher integration level, lower power

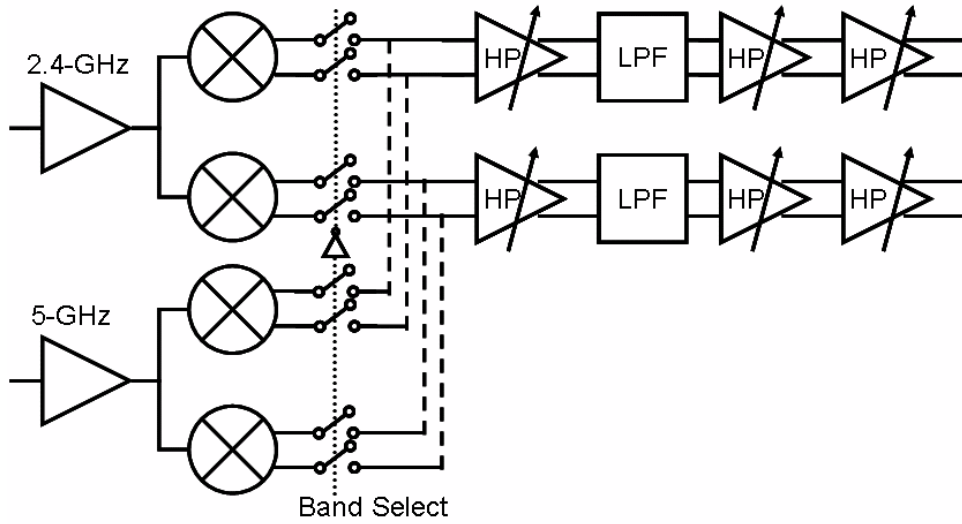


Figure 2.1: Dual-band direct conversion receiver architecture.

consumption and multi-mode and multi-band applications. Two of the attractive architectures for CMOS wireless receivers are low-IF and zero-IF (direct conversion). From the previous section, low-IF receivers are sensitive to I/Q mismatch and cause the image problem very thorny and requires delicacy digital algorithm to calibrate. Therefore the main focus of the work is on direct conversion.

The proposed dual-band direct conversion receiver architecture is shown in Figure 2.1. Sharing the RF front-end in dual frequency bands may reduce the components required, however, the low noise amplifier and the down-conversion mixers of the shared RF front-end need to cope with both 2.4 and 5 GHz signals. Typically, dual-band design requires at least two resonant tanks that resonates at the two desired frequency bands. Since the available quality factors of spiral inductors are not high enough, one of the resonant tank causes degradation to the other and thus affects the available noise and gain performance. Therefore, the receiver adopts two direct conversion RF front-ends and one shared analog baseband circuitry. The direct conversion architecture accompanies several issues such as DC offset, I/Q mismatch, even-order intermodulation, flicker noise disturbance and injection locking in local oscillators, which should be carefully addressed.

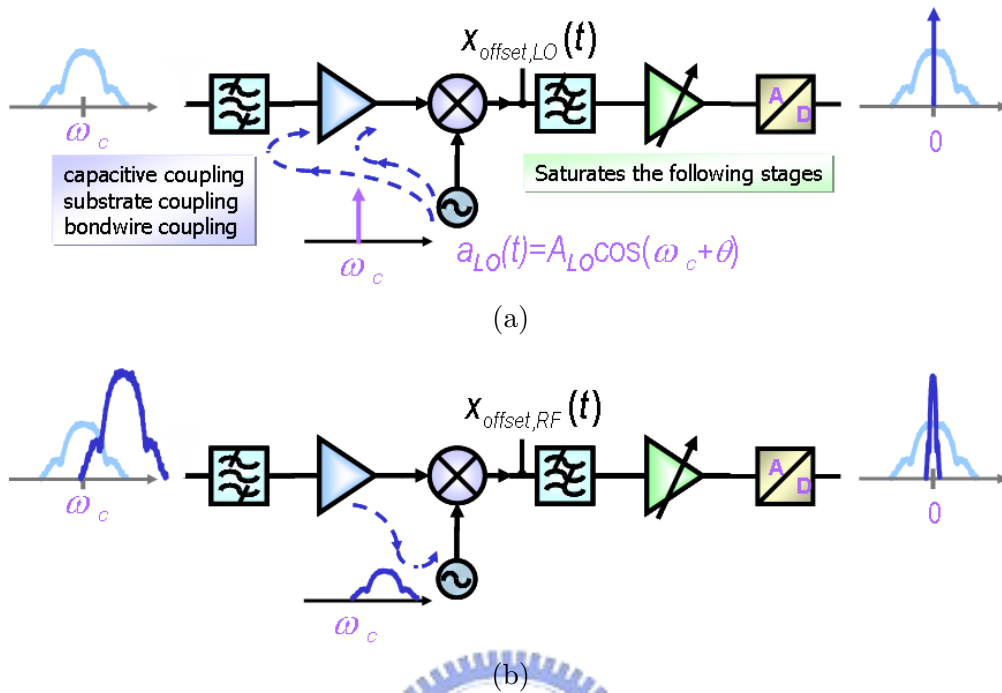


Figure 2.2: DC offset results from self-mixing of (a) LO and the leaked LO (b) RF interferer and the leaked RF interferer.

### 2.4.1 DC Offset

When the RF input signal is down converted to baseband, the signal of interest at the output is zero frequency and extraneous offset voltages can not only corrupt the desired output but also possibly saturate the subsequent stages and thereby desensitize the wanted analog baseband signal. The major sources of DC offset come from the self-mixing of leaked LO signal at RF port and LO signal at LO port of the down conversion mixer as shown in Figure 2.2(a). In addition, the strong interferer at the RF input may leak to LO port and create self-mixing of the interferers as shown in Figure 2.2(b). In the worst case, the DC offset is dynamic due to dynamic LO leakage or RF interference level and not easy to be calibrated by digital offset cancellation algorithms.

There are various ways to combat the DC offset problems [35]. The easiest way to eliminate the DC offset is capacitive coupling as shown in Figure 2.3(a). Since the signal may contain information at very low frequencies, a very low corner frequency

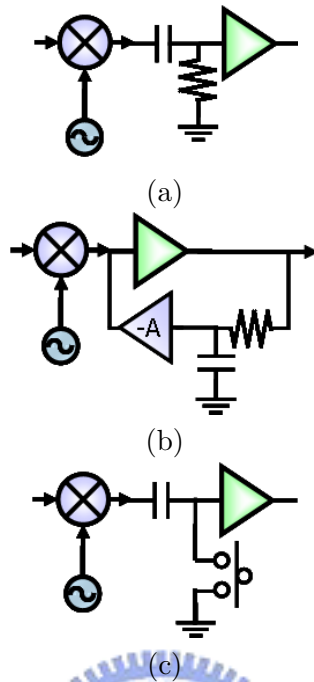


Figure 2.3: DC offset cancellation techniques.

is required to minimize the effects of capacitive coupling, as a result, the capacitors are usually implemented with off chip discrete components.

Negative feedback is another approach to cancel the DC offset as depicted in Figure 2.3(b). The advantage of the negative feedback is that grounded capacitors can be used and therefore MOS capacitors can be used to reduce die area.

The third approach uses the idle time intervals in the receiving as shown in Figure 2.3(c). During the idle time intervals, the switch is turned on and the offset voltage is measured and stored on the capacitor. When receiving, the switch is turned off and the measured voltage is carried out and cancels the offset voltage. However, the thermal noise of the switch mandates large values for the capacitor.

## 2.4.2 Even-Order Intermodulation

If two strong interferers appear at the LNA input, the second order intermodulation distortion of the LNA will induce low frequency tones at the LNA output. If the

subsequent mixer intermixes the low frequency tones, the even order distortion will not be a significant issue. However, the mismatch of differential switching transistor pair causes direct feed through the low frequency at the mixer output and thus corrupts the baseband signal. The RF port of the mixer also suffers from the same even order distortion effect. To eliminate the even order distortion, the LNA and mixer should present good second-order nonlinearity performance characterized by IP2 and good matching in the LO switching pair of the mixer.

### 2.4.3 I/Q Mismatch

I/Q mismatch results from the amplitude and phase error of quadrature LO signals as well as the gain and phase error of the I and Q analog baseband circuits. Any I/Q mismatch directly introduces an error vector to the original signal vector. Therefore I/Q should be accurately matched to improve the BER performance. Suppose the received signal is

$$x_{in}(t) = a \cos \omega_c t + b \sin \omega_c t \quad (2.7)$$

If the quadrature LO signals are

$$x_{LO,I}(t) = 2 \cos \omega_c t \quad (2.8)$$

$$x_{LO,Q}(t) = 2(1 + \epsilon) \sin(\omega_c t + \theta)$$

where  $\epsilon$  represents the I/Q amplitude error in percentage and  $\theta$  is the I/Q phase error. Therefore the obtained down converted baseband I/Q signals can be expressed as

$$x_{BB,I}(t) = a \quad (2.9)$$

$$x_{BB,Q}(t) = (1 + \epsilon)(b \cos \theta + a \sin \theta)$$

The original vector magnitude of the baseband signal is  $\sqrt{a^2 + b^2}$ , now the I/Q mismatched vector magnitude is

$$\sqrt{a^2 + (1 + \epsilon)^2 (b \cos \theta + a \sin \theta)^2}, \quad (2.10)$$

and the error vector magnitude is

$$|\mathbf{e}| = (1 + \epsilon) (b \cos \theta + a \sin \theta) - b. \quad (2.11)$$

The normalized error vector magnitude (EVM) can be expressed as

$$EVM = \frac{(1 + \epsilon) (b \cos \theta + a \sin \theta) - b}{\sqrt{a^2 + b^2}} \quad (2.12)$$

and can be used as the performance index for the receiver and can be regarded as the inversed signal-to-noise ratio if we take noise as error vectors (see Appendix A). Therefore the phase and gain error in the quadrature LO signals cause the degradation of SNR, which in turns degrades the BER performance. The major I/Q mismatch results more from the I/Q LO signal imbalance than from the I/Q baseband signal paths. To overcome the I/Q mismatch, it requires a careful design on the quadrature LO signal generation. Figure 2.4 depicts the degradation of EVM with regard to quadrature phase and amplitude errors. The I/Q mismatch degrades the SNR is not as worse as DC offset does since 5 degrees of phase error and 2 % of amplitude error would results in EVM of  $-25$  dB, which is roughly 25 dB of SNR. However, the same I/Q errors is not tolerable for low-IF receivers.

### 2.4.4 Flicker Noise

Since the RF spectrum is directly down-converted to the baseband frequency, the baseband signal is strongly affected by the flicker noise of the device. The flicker noise is more problematic in MOSFET than in BJT. The flicker noise raises the noise

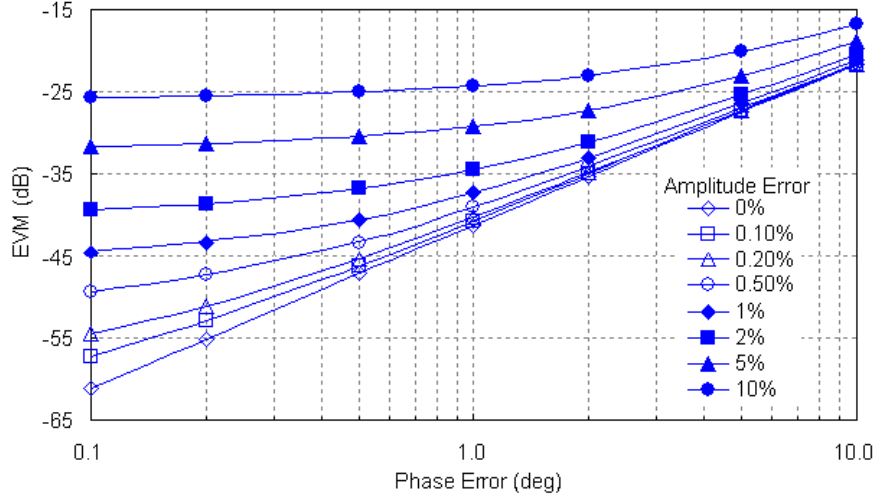


Figure 2.4: EVM versus amplitude and phase errors.

figure of the baseband circuits. The input referred noise voltage power spectrum density of a MOS transistor is

$$\overline{v_n^2} = \frac{K_f}{WLC_{ox}f} \quad (2.13)$$

and the thermal noise is

$$\overline{v_n^2} = \frac{4kT\gamma}{g_m}, \quad (2.14)$$

therefore the corner frequency of the flicker noise and thermal noise intersect is

$$f_c = \frac{K_f}{WLC_{ox}} \frac{g_m}{4kT\gamma} = 2\pi \frac{K_f}{4kT\gamma} f_T \quad (2.15)$$

To eliminate the flicker noise effect, the device dimension of the baseband circuit should be scaled up ( $f_T$  should be scaled down), in such case, the flicker noise may become a minor problem. In addition, PMOS devices should be used wherever possible in the baseband circuit because their flicker noise is lower than NMOS.



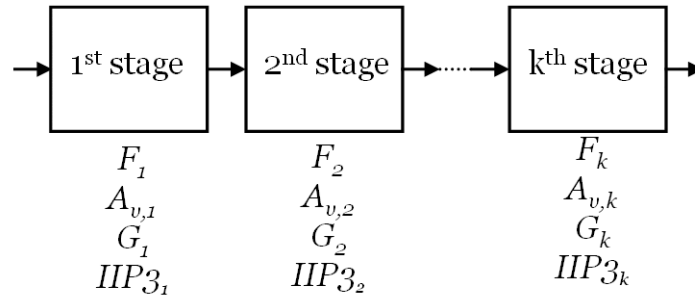


Figure 2.5: Cascaded radio receiver.

## 2.5 Receiver Link Budget Plan

The receiver link budget planning deals with the specifications for each building block of the radio receiver. A typical radio receiver consists of multiple stages in cascade as shown in Figure 2.5. The overall noise figure of the receiver due to the noise contribution of different blocks is given by Friis' formula [7]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_k - 1}{G_1 G_2 \dots G_k} \quad (2.16)$$

where  $F_i$  is the noise figure of the  $i$ -th stage and  $G_i$  is the power gain of the  $i$ -th stage. From Eq. (2.16), it is clear that the system noise figure is dominated by the noise performance of the first stage, since the noise contribution of each block is divided by the preceding gain.

### 2.5.1 Noise Figure Calculation in Integrated Receivers

Since the Friis' formula is based on the definition of available signal and noise powers, Eq. (2.16) is only valid if available power gain is used. Since the available power gain is defined as the available output power divided by the available power from the source, that is at the input and output reference planes of each stage, the impedance must be conjugated power matched, otherwise Friis' equations is not applicable. However, for integrated radio receivers designed at low microwave and

RF frequencies, the power-matched interfaces are often not necessary, since the wavelength at 2-5 GHz frequency range is quite long compared to the on-chip circuit blocks. The power-matched condition is practically required only in the external connections. For instance, the low noise amplifier input is required to match to the output impedance of off-chip filter in order to maintain the shape of the transfer function.

In addition, the signal and noise are often referred to voltage mode in integrated radio receiver designs. In ideal case, the zero-impedance signal source drives infinite input impedance of the following circuit stage. As a result, the Friis' formula must be revised to adapt the integrated radio receiver design. The each individual block of a integrated radio receiver can be modeled as a voltage-controlled voltage source with arbitrary input and output impedances as depicted in Figure 2.6. The unloaded voltage gain of each individual stage is



$$A_{v,k} = \frac{v_{o,k}}{v_{i,k}} \quad (2.17)$$

and the impedance mismatched voltage gain in the interface between the  $k$ -th and  $(k + 1)$ -th stages can be expressed as

$$A_{k,k+1} = \frac{R_{i,k+1}}{R_{i,k+1}R_{o,k}} \quad (2.18)$$

where  $R_{i,k+1}$  and  $R_{o,k}$  represent the input impedance of the  $(k + 1)$ -th stage and the output impedance of the  $k$ -th stage. The noise figure  $F_k$  of an individual stage can

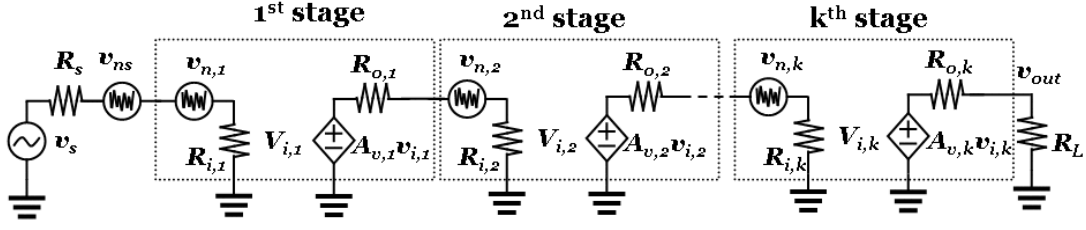


Figure 2.6: Cascaded receiver stages with arbitrary input and output impedances.

be expressed as

$$\begin{aligned}
 F_k &\equiv \frac{\text{Total output noise}}{\text{Total output noise due to the source}} \\
 &= \frac{\left(\overline{v_{ns}^2} + \overline{v_{n,k}^2}\right) A_{s,k}^2 A_{v,k}^2}{\overline{v_{ns}^2} A_{s,k}^2 A_{v,k}^2} \\
 &= 1 + \frac{\overline{v_{n,k}^2}}{\overline{v_{ns}^2}} \quad (2.19)
 \end{aligned}$$

In the impedance matched condition,  $A_{s,k} = 0.5$ . Equation. (2.19) shows no dependency on the matching condition and it is valid as long as the impedance mismatch does not change the internal (input-referred) noise properties  $\overline{v_{n,k}^2}$  of the block.

Consider a receiver consists of three individual blocks in cascade, i.e.,  $k = 3$ , and

the total output voltage of the three-stage cascaded receiver can be derived as

$$\begin{aligned}
 v_{out} &= A_{v,3}v_{i,3}\frac{R_L}{R_L + R_{o,3}} \\
 &= A_{v,3}A_{3,L}\left((A_{v,2}v_{i,2} + v_{n,3})\frac{R_{i,3}}{R_{i,3} + R_{o,2}}\right) \\
 &= A_{v,3}A_{3,L}\left(A_{2,3}\left(v_{n,3} + A_{v,2}\left((A_{v,1}v_{i,1} + v_{n,2})\frac{R_{i,2}}{R_{i,2}R_{o,1}}\right)\right)\right) \\
 &= A_{v,3}A_{3,L}\left(A_{2,3}\left(v_{n,3} + A_{v,2}\left(A_{1,2}\left(v_{n,2} + A_{v,1}(v_s + v_{n,1} + v_{ns})\frac{R_{i,1}}{R_{i,1}R_s}\right)\right)\right)\right) \\
 &= A_{v,3}A_{3,L}(A_{2,3}(v_{n,3} + A_{v,2}(A_{1,2}(v_{n,2} + A_{v,1}A_{s,1}(v_s + v_{n,1} + v_{ns})))))) \\
 &= A_{v,3}A_{3,L}A_{2,3}v_{n,3} + A_{v,3}A_{3,L}A_{2,3}A_{v,2}A_{1,2}v_{n,2} \\
 &\quad + A_{v,3}A_{3,L}A_{2,3}A_{v,2}A_{1,2}A_{v,1}A_{s,1}(v_s + v_{n,1} + v_{ns}) \\
 &= A_{v,tot}\left(v_s + v_{n,1} + v_{ns} + \frac{v_{n,2}}{A_{v,1}A_{s,1}} + \frac{v_{n,3}}{A_{v,2}A_{1,2}A_{v,1}A_{s,1}}\right) \tag{2.20}
 \end{aligned}$$

$$= A_{v,tot}(v_s + v_{n,in}) \tag{2.21}$$

where  $A_{v,tot}$  is the cascaded voltage gain and  $v_{n,in}$  is the input-referred noise voltage of the cascade receiver. The cascade noise figure can then be derived as

$$\begin{aligned}
 F_{tot} &= \frac{A_{v,tot}^2 \overline{v_{n,in}^2}}{A_{v,tot}^2 \overline{v_{ns}^2}} = \frac{\overline{v_{n,in}^2}}{\overline{v_{ns}^2}} \\
 &= \frac{\overline{v_{ns}^2} + \overline{v_{n,1}^2} + \frac{\overline{v_{n,2}^2}}{A_{v,1}^2 A_{s,1}^2} + \frac{\overline{v_{n,3}^2}}{A_{v,2}^2 A_{1,2}^2 A_{v,1}^2 A_{s,1}^2}}{\overline{v_{ns}^2}} \\
 &= 1 + \frac{\overline{v_{n,1}^2}}{\overline{v_{ns}^2}} + \frac{\overline{v_{n,2}^2}}{A_{v,1}^2 A_{s,1}^2 \overline{v_{ns}^2}} + \frac{\overline{v_{n,3}^2}}{A_{v,2}^2 A_{1,2}^2 A_{v,1}^2 A_{s,1}^2 \overline{v_{ns}^2}} \\
 &= F_1 + \frac{F_2 - 1}{A_{v,1}^2 A_{s,1}^2} + \frac{F_3 - 1}{A_{v,2}^2 A_{1,2}^2 A_{v,1}^2 A_{s,1}^2} \tag{2.22}
 \end{aligned}$$

## 2.5.2 Intercept Point Calculation

The cascade third order intermodulation intercept point (IP3) can be given by

$$\frac{1}{V_{iIP3,cas}^2} = \frac{1}{V_{iIP3,1}^2} + \frac{A_{v,1}^2}{V_{iIP3,2}^2} + \frac{(A_{v,1}A_{v,2})^2}{V_{iIP3,3}^2} \tag{2.23}$$

where  $V_{IP3i,k}$  represents the input referred IP3 voltage of the  $k$ -th stage. When calculating the cascade IP3, the passive elements such as external filters and switches exhibit high linearity, that is the IP3 specifications for the passive components is almost extremely infinite.

For the second order intermodulation, the IP2 products do not resident directly at the desired signal band; they are down converted to the baseband, instead. Therefore the cascade gain of IP2 products is not the same as the signal path. Ideally, fully balanced circuits do not present any IP2 products, however, the IP2 products may leak to the output via the mismatch (offset) of the differential circuits in practice [8]. The second order distortion due to offset voltage  $v_{os}$  of a balanced circuit arises from third order terms [9] and the input IP2 can be given by

$$V_{iIP2} = \frac{\alpha_1 + 3\alpha_3 v_{os}^2}{3\alpha_3 v_{os}} = \frac{V_{iIP3}^2}{4v_{os}} + v_{os} \simeq \frac{V_{iIP3}^2}{4v_{os}} \quad (2.24)$$

The mismatch is mainly results from the process variation and as a result, prediction of the second order distortions is difficult. In order to characterize the IP2 of RF receivers to some extent, assuming the stages after the down conversion mixers are all fully balanced and without any second order distortions, the IP2 products major come from the front-end (LNA and mixers), and therefore the overall receiver IP2 specification is dominated by the RF front-end, especially in the mixers.

### 2.5.3 Dual-band Specifications Revisited

The overall specifications for the proposed dual-band direct conversion receiver can be summarized from Table 2.7, 2.8 and 2.9 as shown in Table 2.10. Since the cascade gain of the integrated receiver is quite large, the IP3 specification and hence the SFDR are typically not easy to meet, which is usually limited by the power gain of the receiver front-end. By employing a dual-gain mode operation of the receiver front-end, the linearity can be relaxed if the blocking effect can be eliminated at low

Table 2.10: Specification for integrated dual-band direct conversion receivers.

Parameters	IEEE 802.11b	IEEE 802.11a/g	HIPERLAN/2	Units
NF	8	8	8	dB
IIP3	-13.3	-29.5	-20.5	dBm
IIP2	8.5	-12	1	dBm
High-gain IIP3	-27.75	-34	-29	dBm

input signal levels.

The IP3 specifications previously calculated with Eq. (2.4) is based on the situation that two equal-level interferers locate in adjacent and alternate adjacent channels, creating a third-order intermodulation distortion product in the desired channel. The situation is more rigorous compared with the adjacent channel rejection measurement condition specified by IEEE 802.11 standards. If the receiver front-end has two gain modes, the IP3 specification for the high gain mode should be carefully determined for not introducing blocking effects. The analysis is addressed as follows.

Assume the input desired signal  $A_1 \cos \omega_1 t$  is accompanied by an interferer  $A_2 \cos \omega_2 t$ . The output is

$$y(t) = \left( \alpha_1 A_1 + \frac{3}{4} \alpha_3 A_1^3 + \frac{3}{2} \alpha_3 A_1 A_2^2 \right) \cos \omega_1 t + \dots \quad (2.25)$$

which, for  $A_1 \ll A_2$ , reduces to

$$y(t) = \left( \alpha_1 + \frac{3}{2} \alpha_3 A_2^2 \right) A_1 \cos \omega_1 t + \dots \quad (2.26)$$

Assume the signal and the interferer see the same resistive load, the condition for no blocking effect is that  $C/I \geq S/N \equiv \kappa$ , that is

$$\frac{(\alpha_1 A_1)^2}{\left( \frac{3}{2} |\alpha_3| A_2^2 A_1 \right)^2} \geq \kappa. \quad (2.27)$$

Provided that

$$A_{IIP3} = \sqrt{\frac{4\alpha_1}{3|\alpha_3|}} \quad (2.28)$$

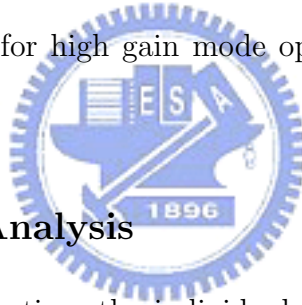
and the mandated adjacent channel rejection ratio (ACRR),  $\rho \equiv A_2^2/A_1^2$ , the inequality can be transferred to

$$\frac{A_{IIP3}^2}{A_1^2} \geq 2\sqrt{\kappa\rho}. \quad (2.29)$$

Represent Eq. (2.29) in logarithm, the minimum input IP3 allowed should be

$$IIP3 \geq P_{\text{desired}} + ACRR + \frac{SNR}{2} + 3. \quad (2.30)$$

Hence the IIP3 specification for high gain mode operation is relaxed as shown in Table 2.10.



### 2.5.4 Link Budget Analysis

Based on the receiver specification, the individual specifications for each building block of the integrated receiver can be planned via a spread sheet. Table 2.11 shows the spread sheet for link budget plan. Specify the values of gain, noise figure, 1-dB compression point, and the input/output impedance of each stage to see if the overall receiver specifications are met. Within a few trials, the specifications for each building block can be determined and represent the goals of circuit designs. However, the analysis in a spread sheet is merely a one-dimension estimation of the receiver performance, for more reasonable prediction, these specifications should be verified with budget simulation as well as system simulation in behavioral level, which will be discussed in detail Chapter 6.

Table 2.11: Dual-band receiver link budget plan.

Parameters	BPF	T/R	LNA	Mixer	HPF	LPF	VGA	Unit
Gain,high	-1.5	-1.5	17.0	8.0	10.0	-3.0	50.0	dB
Gain,low			8.0	8.0	0.0	-3.0	13.0	dB
NF	1.5	1.5	3.5	15.1	17.9	21.0	21.0	dB
V <sub>n,in,HG</sub>			0.67	5.0	7.0	10	10	nV/ $\sqrt{\text{Hz}}$
V <sub>n,in,LG</sub>			13.4	5.0	7.0	10	10	nV/ $\sqrt{\text{Hz}}$
iP-1dB,HG	$\infty$	$\infty$	-18					dBm
iIP3,HG	$\infty$	$\infty$	-7.5					dBm
V1-dB,in,HG			0.04	0.25	0.31	0.50	0.35	V
Vip3,in,HG			0.13	0.84	1.04	1.67	1.17	V
iP-1dB,LG			-8					dBm
iIP3,LG			2.5					dBm
V1-dB,in,LG			0.13	0.25	0.31	0.50	0.35	V
Vip3,in,LG			0.42	0.84	1.04	1.67	1.17	V
R <sub>,in</sub>	50	50	50	5K	1M	1M	500K	Ohm
R <sub>,out</sub>	50	50	50	1K	1K	1K	100	Ohm
A <sub>v,k,k+1</sub>	0.50	0.50	0.50	0.99	1.00	1.00	1.00	
NF,cas	10.26	8.76	7.26					dB
SFDR,HG			53.89	45.62	41.84	35.27	35.04	dB
SFDR,LG			49.90	45.48	42.13	37.15	37.68	dB
iIP3,cas,high			-24.54					dBm
iIP3,cas,low			-8.88					dBm

## 2.6 Summary

This chapter gives an overview of various wireless LAN applications. The specifications of the WLAN standards have been described, and the requirements have been mapped into receiver parameters such as noise figure and linearity requirements to give brief sketch of the receiver performance. The chapter also describes the requirements for a dual-band receiver for WLAN and the link budget has been analyzed.