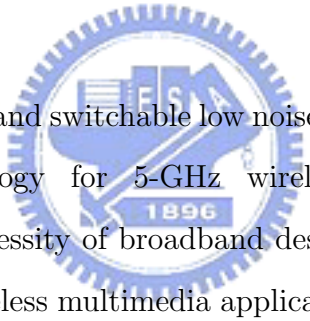
Chapter 3

Dual-Band Switchable Low Noise Amplifier Design



The chapter presents a dual-band switchable low noise amplifier (LNA) implemented in 0.25-μm CMOS technology for 5-GHz wireless multimedia applications. Section 3.1 overviews the necessity of broadband design techniques for RF circuits to the need of high-speed wireless multimedia applications and the design targets of the LNA. A brief summary of the intended radio receiver architecture for the LNA is given in Section 3.2. Section 3.3 reviews the recent researches of CMOS LNAs and the considerations of LNA designs. Instead of using conventional broadband techniques not well suitable for CMOS implementation, a dual-band switchable load is proposed for broadband LNA design. The proposed dual-band load design technique is discussed in Section 3.4. The complete LNA circuit design is described in Section 3.5 and the experimental results is given in Section 3.6.

3.1 Introduction

The demands on broadband wireless multimedia access have driven wireless standards toward higher frequency bands and higher transmission rates. About

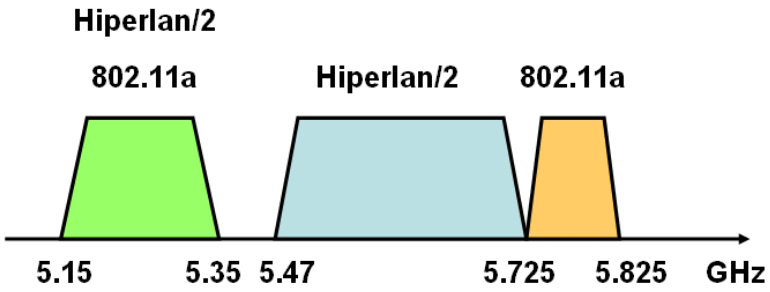


Figure 3.1: Frequency band allocation of 5-GHz wireless LAN standards.

300 MHz spectrum in 5-6 GHz band are allocated for unlicensed high-speed wireless network connectivity such as IEEE 802.16, 802.11a and HIPERLAN/2 in Europe [2][10][11]. By utilizing orthogonal frequency division multiplexing modulation technology, 802.11a and HIPERLAN/2 standards promise 54 Mbit/s transmission capability, occupying about 20 MHz band per channel. Each specification has two distinct frequency bands as shown in Figure 3.1. IEEE 802.11a specifies a lower frequency band from 5.15 GHz to 5.35 GHz and an upper band between 5.725 GHz and 5.825 GHz; HIPERLAN/2 allocates the same lower frequency band and an upper frequency band from 5.47 GHz to 5.725 GHz. In order to utilize the two frequency bands, radio receivers must be able to receive both frequency bands and not to pick up the unwanted interferers. A broadband receiver [34] might be able to receive both lower and upper bands, but wideband receiving is prone to pick up the interferers and also the implementation cost will be high. To achieve a low cost, higher data rate and wider bandwidth radio receiver, a tunable CMOS low noise amplifier operating both in the lower and upper frequency bands for the radio receiver is proposed which is implemented in 0.25-μm CMOS technology equipped with thick top metal. The LNA can be operated at two frequency bands of 5-GHz suitable for broadband wireless multimedia applications.

Table 3.1: Receiver noise figure specifications for IEEE 802.11a and HIPERLAN/2.

Parameters	IEEE 802.11a	Hiperlan/2	Unit
Data Rate	54	54	Mbit/s
Sensitivity	−65	−68	dBm
Bit Error Rate	10^{-5}	10^{-5}	
SNR	20	20	dB
System NF	11	11	dB
Integrated NF	8	8	dB
Design Margin	4.7	1.7	dB

3.2 Radio Receiver

Direct conversion is adopted as the target receiver architecture because of the highly integration feature. The design specification of the receiver was determined through receiver link budget analysis. The signal to noise ratio for 54 Mbit/s required to keep the BER less than 10^{-5} is set to be 20 dB. Assuming that the overall receiver noise figure is 11 dB, and the loss introduced by external components is estimated to be 3 dB, the noise figure of integrated receiver must be less than 8 dB. For HIPERLAN/2, the sensitivity specification is 3 dB lower than IEEE 802.11a, hence the design margin of HIPERLAN/2 is 3 dB less than IEEE 802.11a (Table 3.1).

The radio receiver consists of a low noise amplifier, a pair of down conversion mixers, lowpass filters and variable gain amplifiers as shown in Figure 3.2. The receiver employs capacitors to eliminate DC offset caused by self-mixing of LO signals. The receiver budget simulation shows that the cascade noise figure is smaller than 8 dB with LNA noise figure of 3.5 dB and power gain of 16 dB as shown in Figure 3.3.

3.3 Recent LNA Researches

The low noise amplifier determines with the receiver sensitivity to detect weak input signals. The most important design considerations include

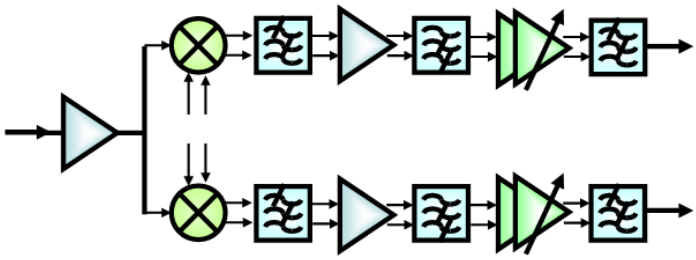


Figure 3.2: Direct conversion receiver architecture for 5-GHz wireless LAN.

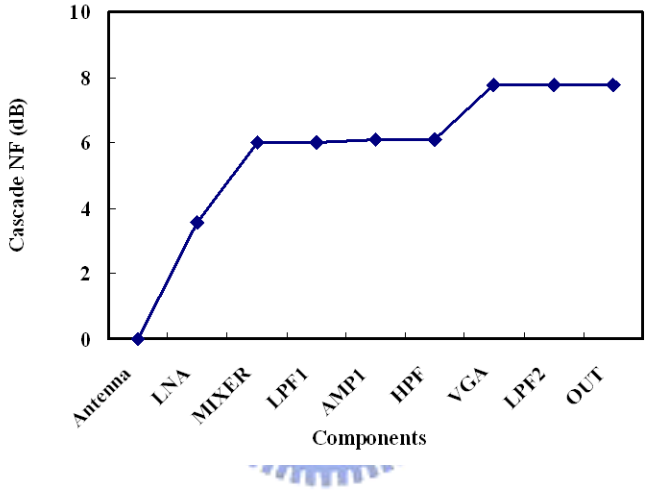


Figure 3.3: Receiver noise figure degradation.

- Minimize the noise figure of the amplifier as low as possible.
- Provide sufficient gain so as to minimize the noise contribution from the building blocks after the LNA.
- Match the input/output impedance of LNA to 50 Ω if it follows a RF pre-select filter or precedes the image-reject filter in a heterodyne receiver.
- Perform sufficient linearity to minimize the spurious entering the following mixer.
- Consume low power for portable wireless communication system.

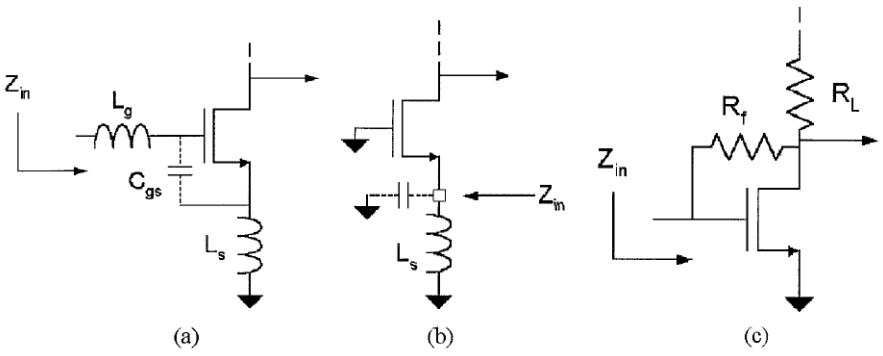


Figure 3.4: Common low noise amplifier topologies.

Figure 3.4 depicts the common architectures of LNA circuits. The typical configurations of the input transistor of LNA are common source and common gate. The latter is seldom applied since it has a theoretical limit on noise figure as $F = 1 + \gamma$, where $\gamma = 2/3$ for long channel device and thus $F = 2.2$ dB [12]. If parasitic resistance adds other noise contribution, the noise figure is degraded more than 3 dB [13]. Therefore it is not suitable for high-tier communication systems. However, for low-power and low-tier communication systems such as paging applications, the common-gate topology can be employed with external high quality factor inductors to achieve ultra low power LNA [14].

The common source configuration is widely used in the input stage of LNA. The input impedance matching usually employs an inductive degeneration at the source of the MOSFET and another inductor at the gate together with source inductor to resonate the gate to source capacitor C_{gs}. The input impedance of Figure 3.4(a) would be

$$Z_{in} = s\left(L_s + L_g\right) + \frac{1}{sC_{gs}} + \frac{g_{m1}}{C_{gs}}L_s \tag{3.1}$$

By choosing the L_s and bias g_{m1} to achieve the real part of Eq. (3.1) to be 50 Ω and the image part will be zero at resonant frequency ω_0. Simplify Eq. (3.1) at resonance, the impedance will approximate to $\omega_T L_s$. Hence the degenerative inductance is limited by the process parameter ω_T in the perspective of this tuned

matching method. In addition, the value of L_s should be small to ensure the gain not degraded at high frequency due to the inductive degeneration. Otherwise, the power dissipation would be increased to compensate the gain degradation. Typically, the inductance is ranged around in 1 nH and can be implemented by bonding wire or package lead inductance.

The output load of LNA typically employs an inductor to increase high frequency power gain. These inductive loading may be implemented by on-chip spiral inductors or active inductors. Though active inductors occupy less chip area and perform band-pass characteristics, they degrade the noise performance very much [15]-[17]. Since the impedance is tuned to 50 Ω at the narrow band resonate frequency, it might differs from 50 Ω at the desired frequency if other parasitic capacitive or inductive effects have not been carefully considered. For wideband input impedance matching, one might employ the $1/g_m$ termination or shunt series feedback as shown in Figure 3.4(b) and (c). However, both of them add noise power at the output and should not be taken in the input stage in high-tier applications. The output impedance matching to 50 Ω is very critical if LNA needs to drive a external image-reject filter in heterodyne receivers. This can be easily performed with the shunt-series feedback structure [18].

Most of the architectures of LNAs in literatures are cascode structure no matter single-ended or differential input [15]-[27]. The cascode amplifiers are often applied in high-frequency circuits because the effective capacitance at the input is reduced [28]. Besides, it provides a high reverse isolation and thus ensuring stability. A high reverse isolation of LNA is important for the sake of avoiding LO power leakage through the LNA to the antenna thus causing interference. In addition, in direct conversion receiver, the LO leakage causes notorious DC offset [17] difficult to overcome.

The low power requirement is very important in portable wireless applications. Though the minimum noise of a device can be achieved by biasing it at optimum

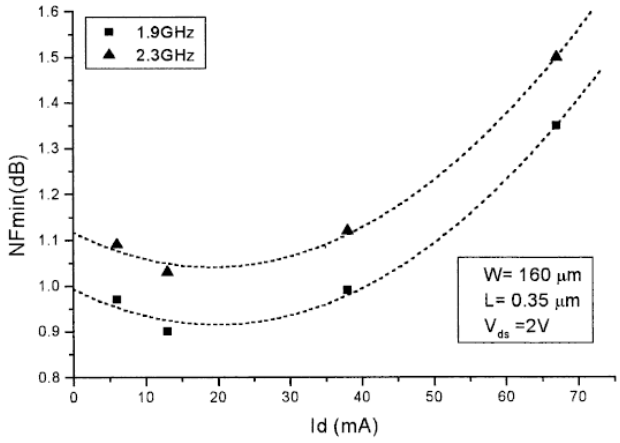


Figure 3.5: Minimum noise figure versus drain current of a MOSFET.

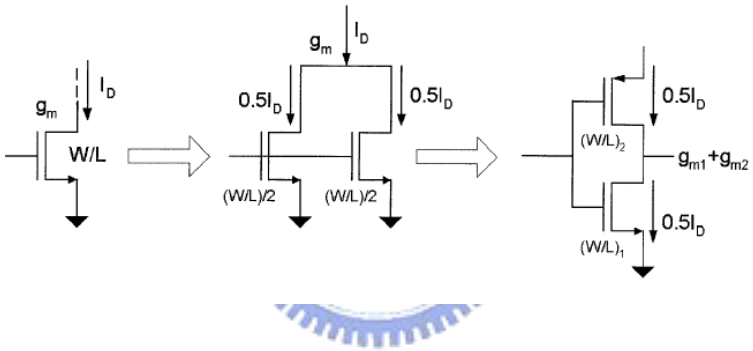


Figure 3.6: Current reuse transconductance.

drain current [29], the optimum drain current is not low enough for the intention of low-power RF integrated circuits as shown in Figure 3.5 [30]. Therefore the performance must tradeoff between low-power and optimum low noise. Nevertheless, some circuit design techniques can be employed to reuse the bias currents [21][31][32] or reduce the supply voltage by LC folded loading [23]. The main ideal of [31] is to achieve a transconductance g_m of a single device with less current and obtain an equivalent $g_{m,tot} = g_{m1} + g_{m2}$ as shown in Figure 3.6. Figure 3.7 employs the stacked second stage transistor to reuse bias current of cascode stage for the second stage bias [21][32]. However, these techniques introduce noise contribution and impedance design at input port and inter-stage should be carefully considered.

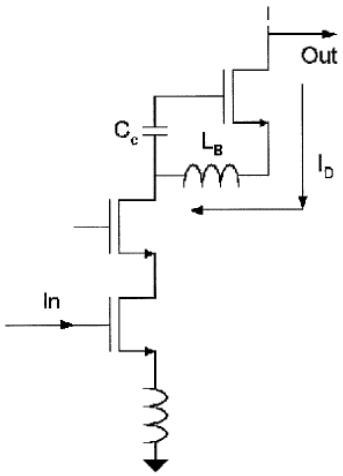


Figure 3.7: The stack cascode for current reuse.

Though the design of LNA involves many tradeoffs for various design requirements, [33] provides a design methodology for simultaneously input match at a specific gain or power constraint with the selection of best device size to achieve near-optimum noise performance. The noise figure is expressed as

$$F = 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha}\frac{\chi}{Q_s}\left(\frac{\omega_0}{\omega_T}\right) \tag{3.2}$$

where R_l, R_g and R_S are the inductor series resistance, gate resistance of input MOSFET and source resistance, respectively. α is defined as g_m/g_{d0}. χ and Q_s can be expressed as

$$\chi = 1 + 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1 + Q_s^2\right) \tag{3.3}$$

$$Q_s = \frac{\omega_0\left(L_s + L_g\right)}{R_s} = \frac{1}{\omega_0 R_S C_{gs}} \tag{3.4}$$

where δ is the coefficient of gate noise, classically equal to 4/3 for long-channel devices and c stands for complex correlation coefficient of gate noise $\overline{i_g^2}$ and drain

noise $\overline{i_d^2}$. The optimum Q_s at a specific gain and power constraint are

$$Q_{s,opt,gain} = \sqrt{1+2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}}+\frac{5\gamma}{\delta\alpha^2}} \tag{3.5}$$

$$Q_{s,opt,power} = \sqrt{3}\sqrt{1+2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}}+\frac{5\gamma}{\delta\alpha^2}} = \sqrt{3}Q_{s,opt,gain} \tag{3.6}$$

The minimum noise factors are

$$F_{min,gain} = 1+\sqrt{\frac{4}{5}\delta\gamma}\left(\frac{\omega_0}{\omega_T}\right)\sqrt{1+2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}}+\frac{5\gamma}{\delta\alpha^2}} \tag{3.7}$$

$$F_{min,power} = 1+\sqrt{\frac{16}{15}\delta\gamma}\left(\frac{\omega_0}{\omega_T}\right)\sqrt{1+2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}}+\frac{5\gamma}{\delta\alpha^2}} \tag{3.8}$$

Typically, the low noise amplifier does not consume very large power and limiting the power consumption is not the first priority of LNA design but minimizing the noise figure is. Therefore the low noise design of the proposed LNA is based on the optimum noise method which requires conjugate match of the input impedance of the LNA to Γ_{opt} of the optimum noise.

Though the advanced CMOS process exhibits higher cutoff frequency and equips with thick-metal spiral inductors, one may need to use external components to match the input impedance and reduce noise figure lower. Though the noise figure may be reduced low enough, other parasitic effects such as substrate loss due to bonding pads and electrostatic discharge protection circuit hinder the noise performance.

3.4 Broadband Load Design

To meet the broadband requirement of 5-GHz wireless LAN specifications, the power gain and noise figure of the LNA must be flat for equal sensitivity performance for each channel. Hence, the impedance matching will be the critical issue for wideband design. It is well known that Tee or Ell networks of inductors and capacitors can be

used for impedance matching network in narrow-band LNA design. For broadband impedance matching, multi-section of Tee or Ell matching networks can still be applied. However, on-chip spiral inductors usually occupies large die area and using more impedance matching networks results in larger die area and thus increases costs. With external passive elements the wideband impedance matching may be achieved [34].

In addition to input impedance match, the loading should also be broadband.

3.4.1 Broadband Continuous-Tuned Load

For a cascode LNA, the gain can be expressed as $A_v = G_m Z_{load}$. The load can be implemented by using a parallel LC tank and the impedance Z_{load} is given by

$$Z_{load}(\omega) = R_{load} \parallel j\omega L \parallel \frac{1}{j\omega C} \tag{3.9}$$

$$R_{load} = \left(Q_{ind}^2 + 1\right) R_p \tag{3.10}$$

$$\omega_c = \frac{1}{\sqrt{LC}} \tag{3.11}$$

where Q_{ind} and R_p are the quality factor and series parasitic resistor of the inductor, respectively. By varying the capacitance or inductance, the resonant frequency ω_c can be tuned to the desired frequency band and thus the broad bandwidth design can be achieved. Figure 3.8(a) depicts a resonant tank by shunting a variable capacitor (varactor) with an inductor. The varactor can be implemented by a p-n junction diode or an accumulation-mode varactor whose capacitance can be continuously controlled by digital bits through a D/A converter. Assume ω_L and ω_H as the lower and upper resonant frequencies, the tuning frequency range $\Delta\omega = \omega_H - \omega_L$ can be given by

$$\Delta\omega = \omega_L \left(\sqrt{\frac{C_{max}}{C_{min}}} - 1 \right) \tag{3.12}$$

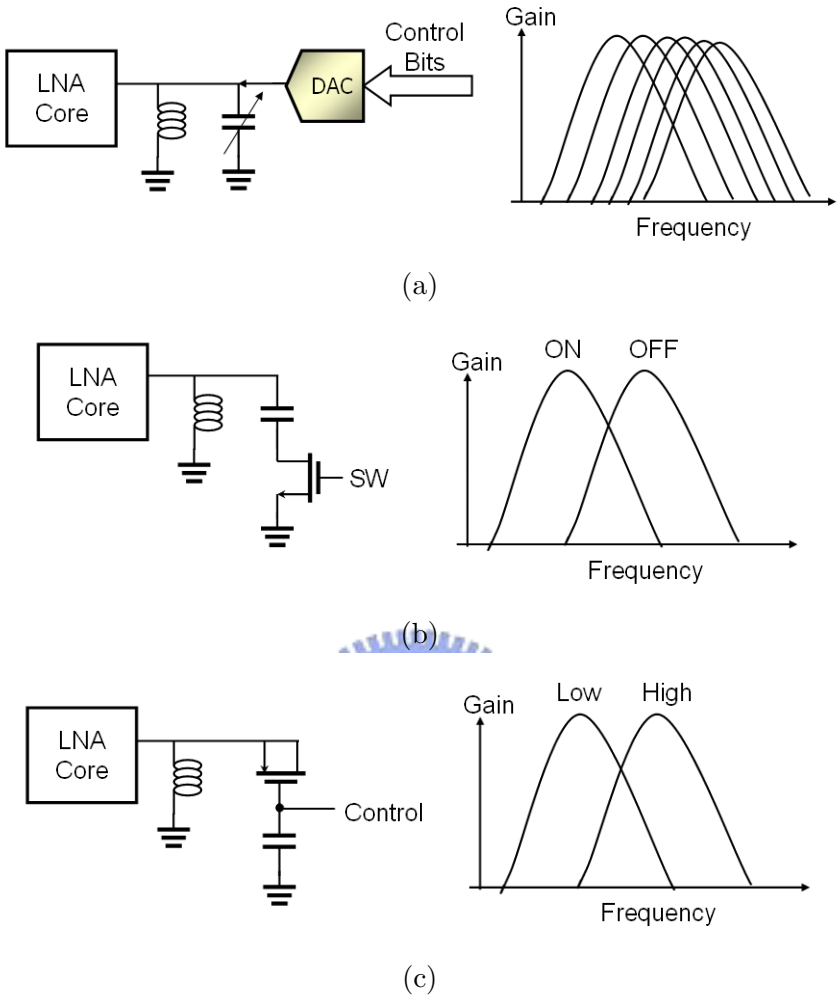


Figure 3.8: Broadband load design: (a) tuned load; (b) dual-band load; (c) proposed dual-band switchable load.

where C_{max} and C_{min} are the maximum and minimum capacitance of the varactor. The C_{max}/C_{min} ratio is

$$\frac{C_{max}}{C_{min}} = \left(1 + \frac{\Delta\omega}{\omega_L}\right)^2 \equiv \eta. \tag{3.13}$$

The ratio η is about 1.28 for IEEE 802.11a and 1.24 for HIPERLAN/2, which can be implemented by a p^+ to-n-well junction varactor [36]. If we consider the parasitic capacitance C_{ind} of the inductor, and assume the varactor capacitance

ratio is $\nu \equiv C_{var,max}/C_{var,min}$, then

$$\frac{C_{var,max} + C_{ind}}{C_{var,min} + C_{ind}} = \eta \tag{3.14}$$

$$\frac{C_{ind}}{C_{var,min}} = \frac{\nu - \eta}{\eta - 1} \geq 0, \tag{3.15}$$

that is $\nu \geq \eta$. In other words, with the parasitic capacitance of the inductor, the varactor capacitance ratio must be larger than η, resulting in a more stringent requirement of varactors. In addition, the nonlinear C-V characteristic of p^+ to n-well junction varactor leads to a small linear control range and thus a high resolution D/A is needed or a sophisticated algorithm is required to linearize. To eliminate the design expenses for the continuous-tuned band, an efficient design on dual-band load is proposed.

3.4.2 Dual-band Load

To omit the D/A converter and simplify the design, the loading can be replaced by a capacitor in series of a switch (Figure 3.8(b)). Therefore the broadband load becomes dual-band load. When the switch is off, the resonant frequency is determined by the inductor and its parasitic capacitor. However, when the switch is on, the turn-on resistance R_{on} of the switch degrades the quality factor of the resonant load. The turn-on resistance can be lowered by a larger size MOSFET which results in larger parasitic capacitance and hence decreases the resonant frequency of the load.

3.4.3 Proposed Dual-band Switchable Load

To deal with the turn-on resistance problem, the variable capacitor in Figure 3.8(a) is replaced with a PMOS transistor in connection as a two-terminal MOS capacitor.

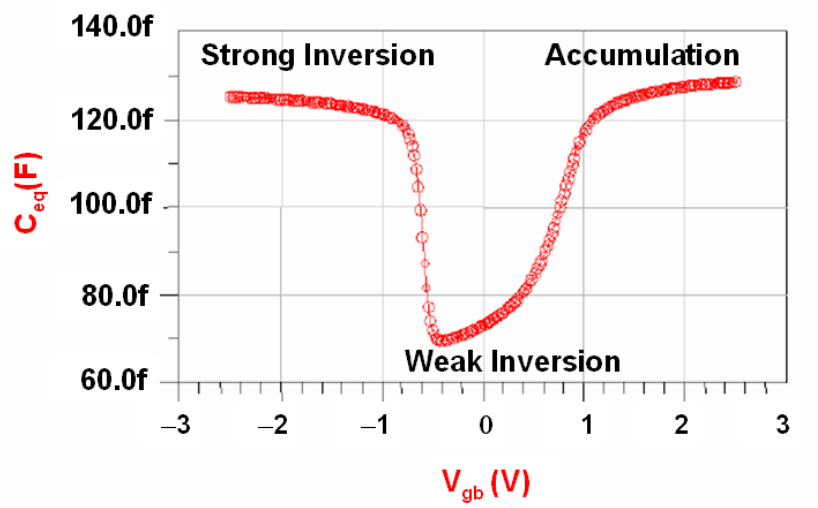


Figure 3.9: Gate capacitance of the PMOS capacitor.

The equivalent capacitance of PMOS capacitor is

$$\begin{aligned} C_{eq} &= C_{ovs} + C_{ovd} + C_{gb} \\ &= 2nL_D C'_{ox} W + WLC'_{gb} \end{aligned} \tag{3.16}$$

where $1 \leq n \leq 2$ is for fringing effect, L_D is the source/drain lateral diffusion and C'_{ox} and C'_{gb} are the unit area gate oxide and gate-to-bulk capacitance, respectively. By biasing the PMOS in strong inversion region and weak inversion region, the unit-area gate-to-bulk capacitance C'_{gb} varies between C'_{ox} and the series combination of C'_{ox} and C'_{dep} [37]. Therefore the capacitance ratio can be expressed as

$$\frac{C_{eq,max}}{C_{eq,min}} = \frac{2nL_D C'_{ox} W + WLC'_{ox}}{2nL_D C'_{ox} W + WL\frac{C'_{ox}C'_{dep}}{C'_{ox}+C'_{dep}}} \tag{3.17}$$

$$= \frac{2nL_D/L + 1}{2nL_D/L + \zeta/(1+\zeta)} \tag{3.18}$$

where $\zeta \equiv C'_{dep}/C'_{ox}$. With the assumption of $2nL_D/L \ll 1$, the capacitance ratio becomes $1+1/\zeta$. For $\zeta \simeq 0.5$, the capacitance ratio would be three and thus suitable

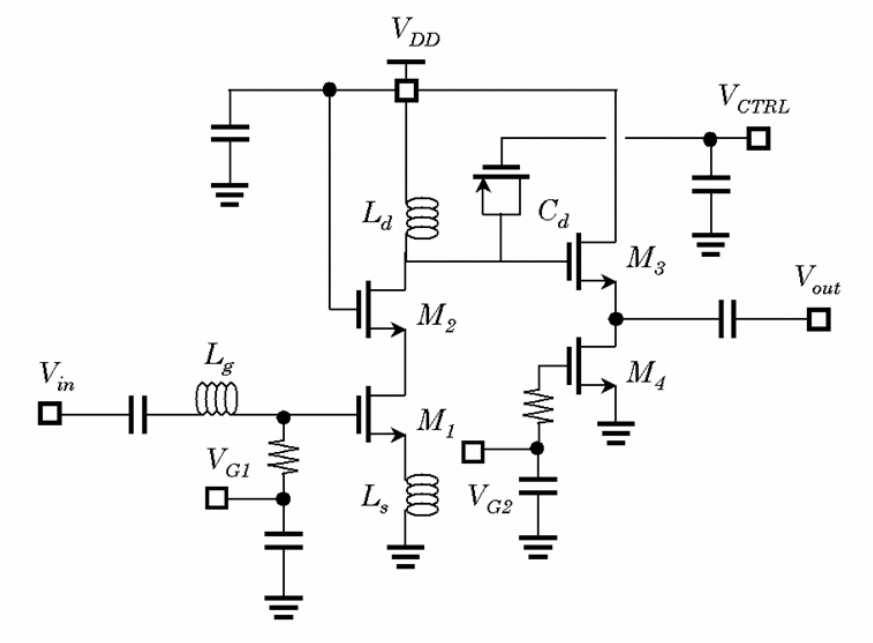
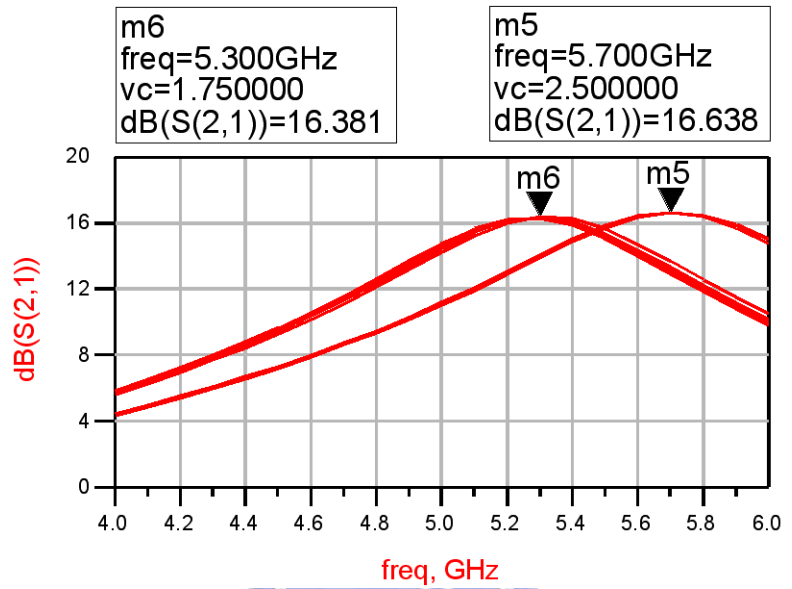


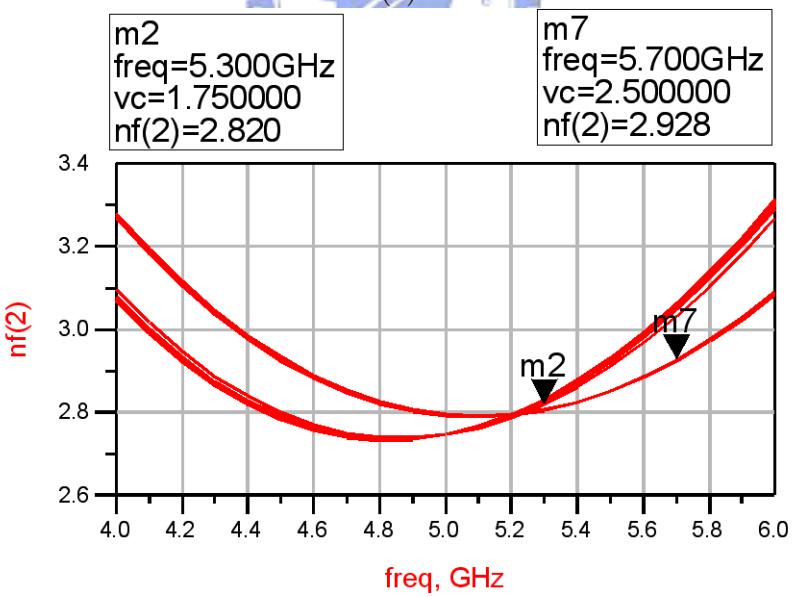
Figure 3.10: Dual-band switchable LNA schematic.

for broadband applications. Figure 3.9 depicts the two distinct capacitance values with respect to gate control voltage of a PMOS with 70μm/0.24μm. Because of the distinct capacitance values of MOS capacitor as the gate voltage changes, by properly choosing inductance and PMOS dimension, the resonant frequency can be designed to the desired frequency bands.

As for impedance matching, the loaded quality factor of the impedance matching network to cover the entire 5-GHz band is about 8. For inductor degenerated common-source LNA, the quality factor of the input matching network is typically below 3 to avoid the necessity of tuning and trimming for high Q networks [18]. Therefore, the broadband input impedance matching in the design can be mitigated with one section low Q network.



(a)



(b)

Figure 3.11: Simulated power gain and noise figure of the LNA.

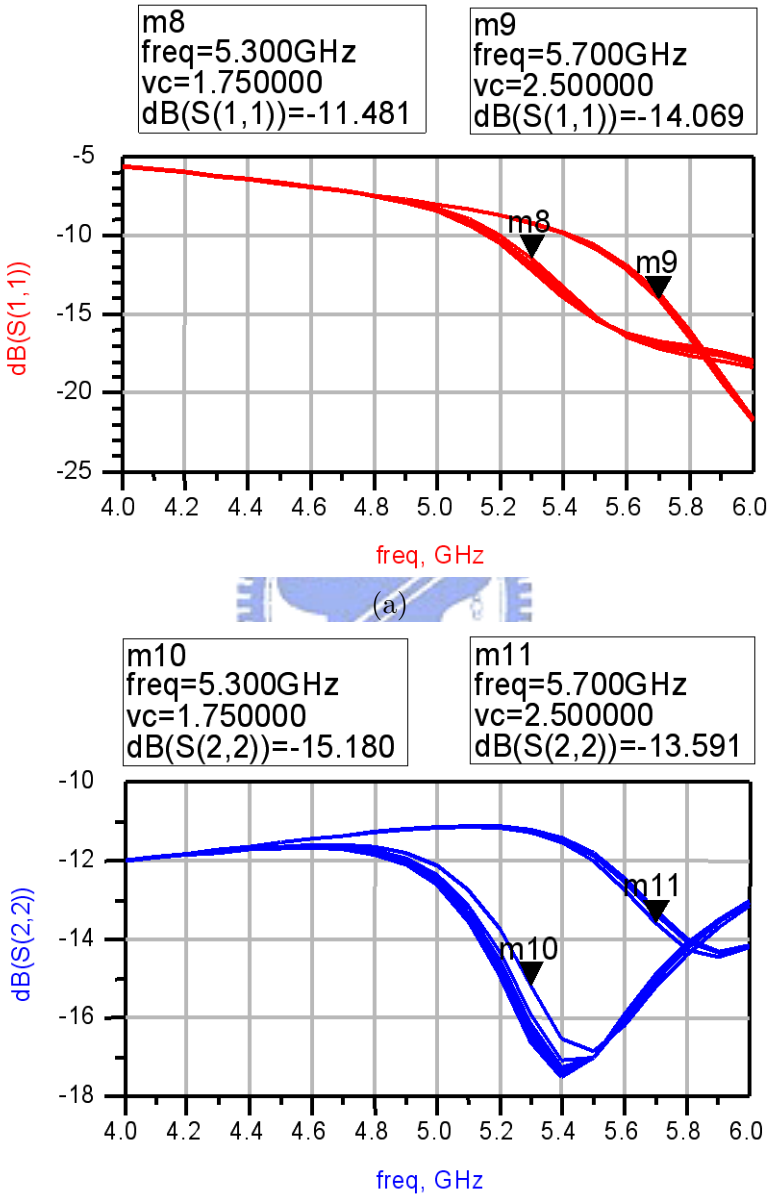


Figure 3.12: Simulated input and output return losses of LNA.

3.5 Circuit Design

The low noise amplifier is composed of a cascode input stage and a source follower output stage as depicted in Figure 3.10. The component values are listed in Table 3.2. The input impedance matching employs inductive degeneration approach to make the noise circles closer to the gain circles and as a result simultaneously noise and power gain matching is obtained [38]. The source follower translates the high output impedance of previous stage to low impedance for matching the LNA output to 50 Ω. The output impedance matching is easily achieved by properly biasing the transistor M3 at $1/g_{m3} = 50\ \Omega$. The drain inductor L_d together with PMOS capacitor C_{eq} forms a resonant load of the cascode stage. By varying the gate bias voltage V_{ctrl} of the PMOS capacitor, the resonant frequency can be switched to the desired upper and lower bands.

Simulation results show that the frequency band of the LNA is switchable because of the switchable distinct capacitance values of the PMOS varactor. The simulated power gain of the LNA is shown in Figure 3.11. The switching of the capacitance puts a slight effect on the input impedance matching as shown in Figure 3.12. The reverse isolation of the LNA is more than 35 dB. The simulated input IP3 is about −16.5 dBm and the 1-dB compression point is −31.5 dBm. The

Table 3.2: LNA component list

Device	Value	Device	Value
M_1	210/0.24	C_1	6pF
M_2	90/0.24	C_2	6pF
M_3	90/0.24	C_B	6pF
M_4	110/0.24	V_{dd}	2.5V
L_g	1.55nH	V_{G1}	0.7V
L_s	0.54nH	V_{G2}	0.65V
R_B	10k	V_{ctrl}	0/2.5V
L_d	2.46nH	I_d	5.5mA
C_d	70/0.24		

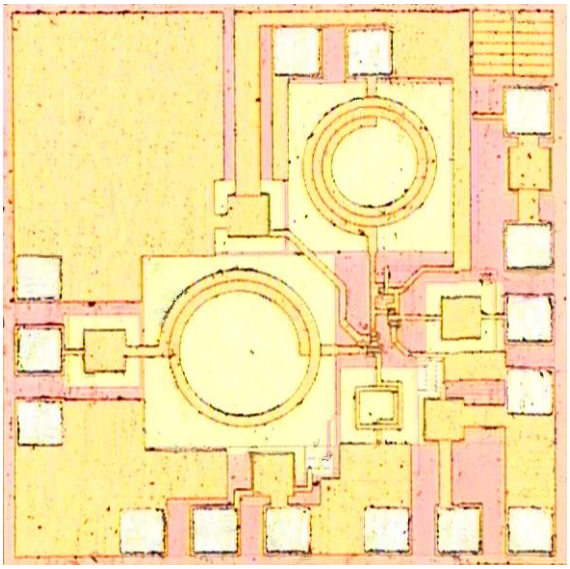


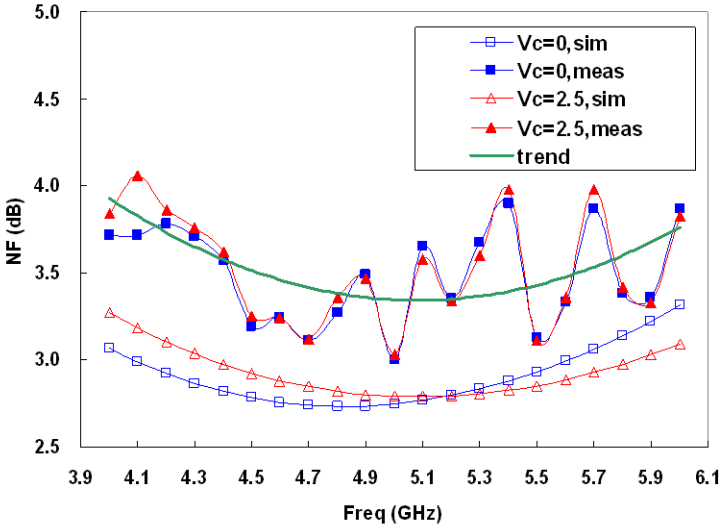
Figure 3.13: LNA chip photo.

LNA drains about 5.5 mA from 2.5 V power supply.

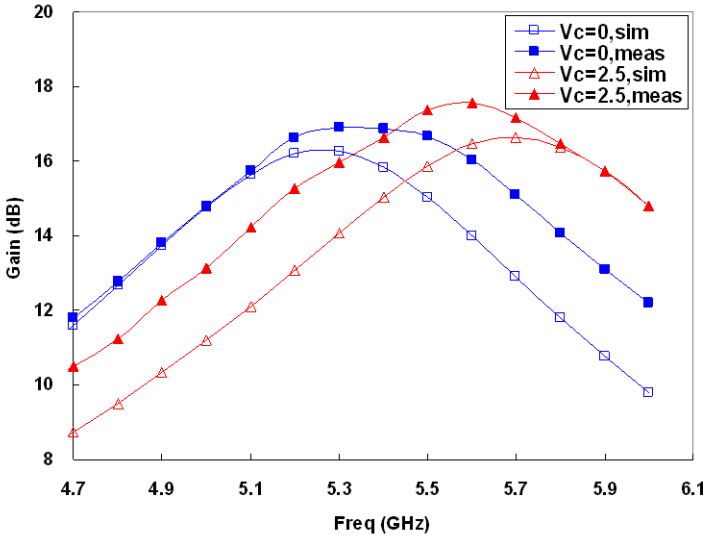
The chip photo of the LNA is depicted in Figure 3.13. The die area is 1110.83μm×1112.90μm. Using device layout cells ensures the RF performance of each inductors and transistors. Metal 1 is adopted as ground layer to shield the LNA from the substrate loss and substrate noise, which is very essential at the input of the LNA. Each element is surrounded by a substrate guard ring for shielding unintended coupling from the substrate. In addition, each DC bias pad is companied by a MIM capacitor to bypass any high frequency disturbing received from DC probe antenna effects.

3.6 Experimental Results

The circuit is measured on wafer using RF probes and an HP8510C network analyzer. The gate control voltage of the PMOS varactor is switched from 0 to 2.5 V. The measurement results are illustrated in the following figures. The noise figure in the 5-GHz band in around 3.5-3.7 dB is shown in Figure 3.14(a). The difference between simulated and measured noise figure is due to the uncounted substrate loss of the



(a)



(b)

Figure 3.14: LNA measurement results at $V_{ctrl} = 0$ and 2.5 V: (a) noise figure; (b) power gain.

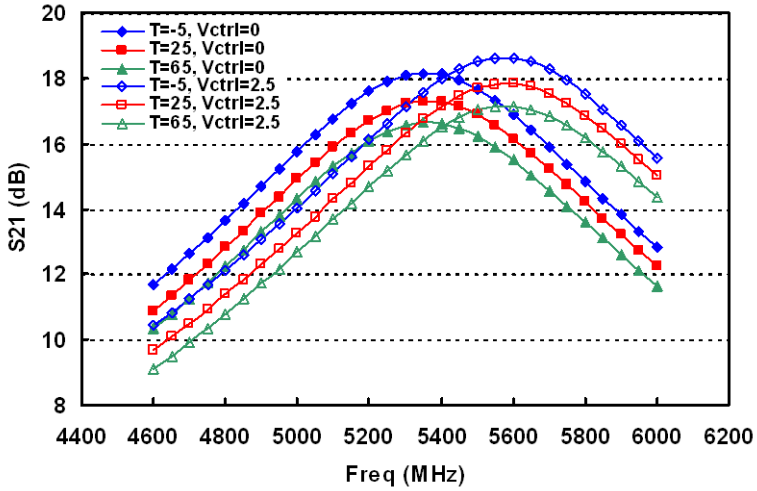


Figure 3.15: Power gain measurement at three different temperatures ($-5, 25$ and 65°C).

bias resistor at the input of the LNA. The power gain is around 16.5-17.8 dB and switchable in the lower and upper frequency bands at 5 GHz (Figure 3.14(b)). The LNA is in lower band as V_{ctrl} is zero and in upper band when V_{ctrl} is 2.5 V.

The power gain at various temperatures is also measured as depicted in Figure 3.15. Though the power gain varies from 16.5 dB to 18 dB as the temperature changes from -5 to 65°C, the peak frequency of the power gain does not change much. The reason is that the temperature dependence of the PMOS capacitor C_{eq} is due to the thermal expansion of the device, the variation in ϵ_{ox} and the change in the depth of the depletion region. The frequency variation due to temperature dependence of the capacitance can be given by

$$\frac{\Delta\omega}{\omega} = \sqrt{\frac{\Delta C/C}{1+\Delta C/C}} \simeq \sqrt{\frac{\Delta C}{C}}. \tag{3.19}$$

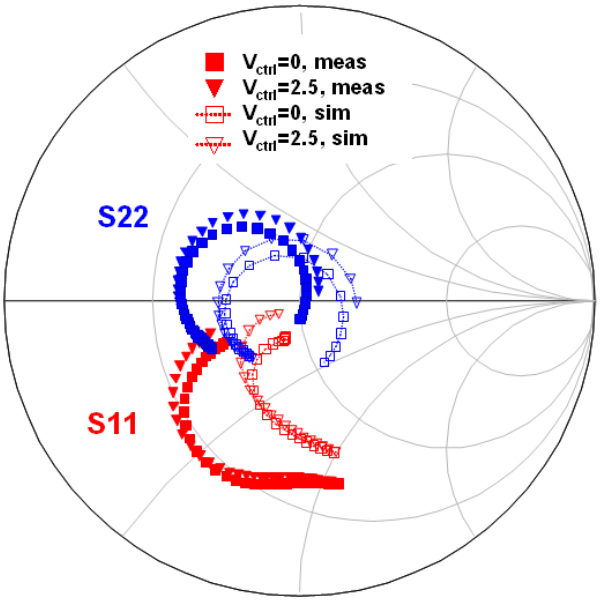
Typically, the temperature dependence is 20-50 ppm/°C [39] and thus the frequency variation is about 20-35 MHz at 5-GHz. Since the quality factor of the resonator is not very high, therefore the gain variation due to the peak frequency variation is acceptable.

Table 3.3: Summary of the LNA measured performance.

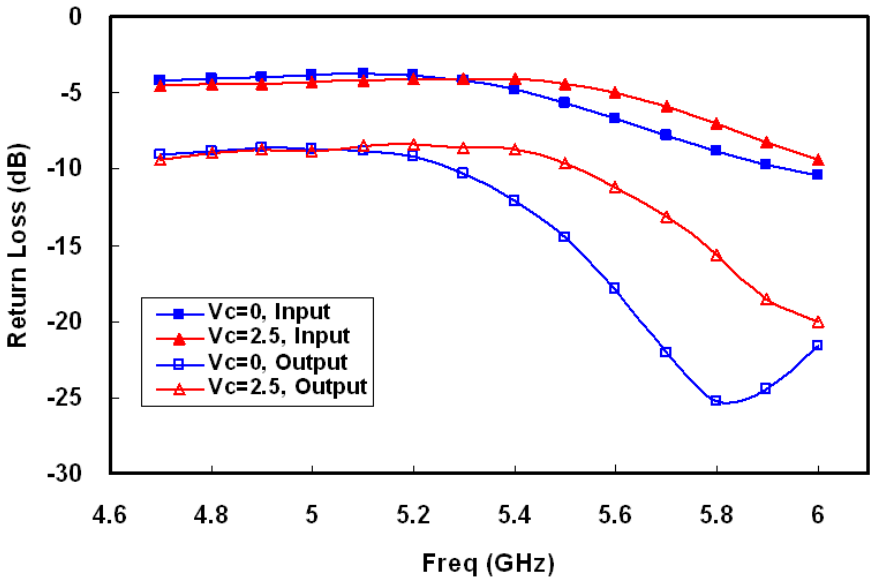
Parameter	Performance
Frequency Range	5.1-5.9 GHz
Noise Figure	3.5-3.7 dB
Gain	16.5-17.8 dB
Input Return Loss	> 4 dB
Output Return Loss	> 8 dB
Reverse Isolation	> 33 dB
Input IP3	-14.5 dBm
Current Consumption	9.5 mA
Power Supply	2.5 V

The input impedance matching $s11$ measured is less than -4 dB in the bands and the output impedance matching $s22$ is better than -8.5 dB in both bands as shown in Figure 3.16. With a low loaded-Q input matching network to cover the dual bands, the need for multi-section matching network at the input is eliminated in the design. The best input return loss frequency is shifted to a higher frequency due to the smaller inductance of L_g than the predicted one. This can be improved by adding a bonding wire to increase the inductance without further degradation of noise figure. The best output return loss frequency is also shifted to a higher frequency resulting from the change of g_{m3} of the source follower due to process variation. This can be adjusted by fine tuning the bias point of the source follower.

The measured reverse isolation is better than 33 dB. In order to test the linearity of the LNA in the two switching frequency bands, two tones with 1 MHz offset reside both around 5.3 and 5.7 GHz are injected as the input signal for IP3 measurement. The PMOS varactor does not affect the linearity of the LNA. The measured result shows that the LNA exhibits input IP3 of -14.5 dBm and input referred 1-dB compression point of -23.2 dBm in 5.3 GHz, and respectively, -14.6 dBm and -23.1 dBm in 5.7 GHz (Figure 3.17). For better noise performance, the LNA consumes 4 mA more than simulated 5.5 mA at a 2.5 V power supply. The



(a)



(b)

Figure 3.16: Measurement results: (a) s11 and s22 in Smith chart; (b)input and output return losses.

performance measured is summarized in Table 3.3.

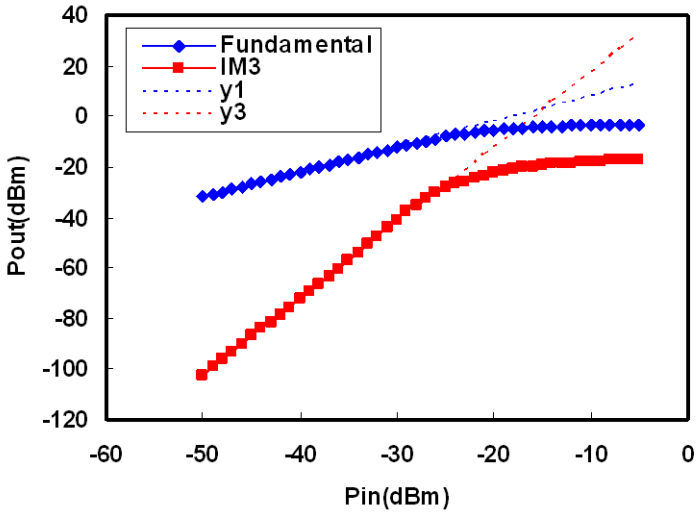


Figure 3.17: LNA IP3 measurement results at $V_{ctrl} = 0\ V$.

3.7 Summary

A dual-band switchable low noise amplifier for 5-GHz wireless multimedia systems has been presented. With a PMOS varactor together with the inductor as a dual-band switchable load, the LNA can be operated at the lower band or the upper band at 5-GHz by 1-bit control signal at the PMOS gate. The design avoids the need of large chip area for broadband design, D/A converter for tuning p-n junction diodes as well as sophisticated linearization algorithm. The dual-band switchable LNA is suitable for broadband wireless multimedia applications.