Chapter 6

Case Study: 2.4-GHz Direct Conversion Receiver

The chapter presents a 0.25-μm CMOS receiver front-end designed for 2.4-GHz direct conversion RF transceiver and demonstrates the necessity and feasibility of the RF and baseband co-verification methodology. The design covers from front-end schematic design to back-end layout design in Section 6.1. The RF/Baseband co-verfication for the direct conversi receiver is described in Section 6.2. The measurement result discussed in Section 6.3 shows agreement with the co-simulation result. Dissipating 10.5 mA at 2.5 V power supply, the receiver exhibits an EVM of -9.18 dB stimulated by a -76 dbm 11M symbol/sec QPSK modualtion input signal, which is suitable for IEEE 802.11b wireless LAN applications.

6.1 Receiver Front-End Design

The target transceiver architecture is direct conversion and the block diagram is illustrated in Figure 6.1. The direct conversion architecture eliminates the need of bulky image rejection filter and increases the integration capability. The transceiver is composed of five circuit modules. Module 1 integrates a RF band-pass filter, a

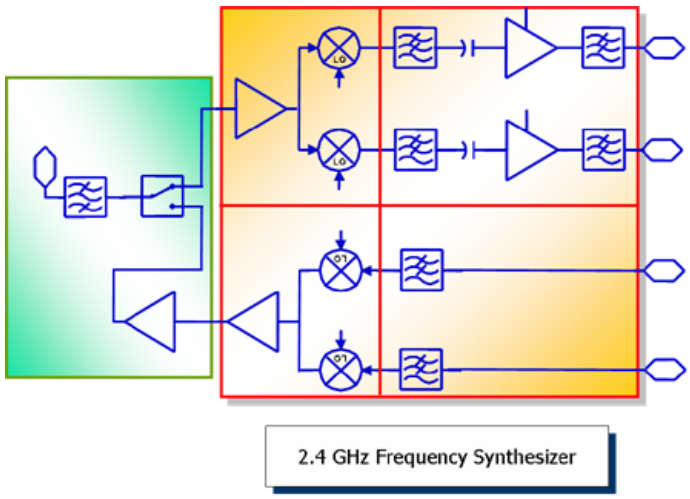


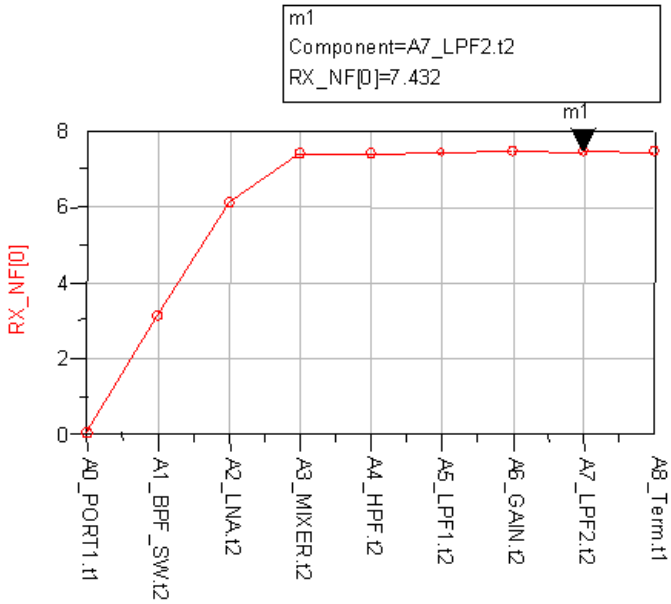
Figure 6.1: The wireless LAN transcevier architecture.

transmit/receive switch and a power amplifier. Module 2 is the receiver front-end. Module 3 is the transmitter front-end. Module 4 is for analog baseband signal processing, including variable gain amplifiers and transmit and receive low-pass filters. Module 5 is the frequency synthesizer for 2.4-GHz LO frequency.

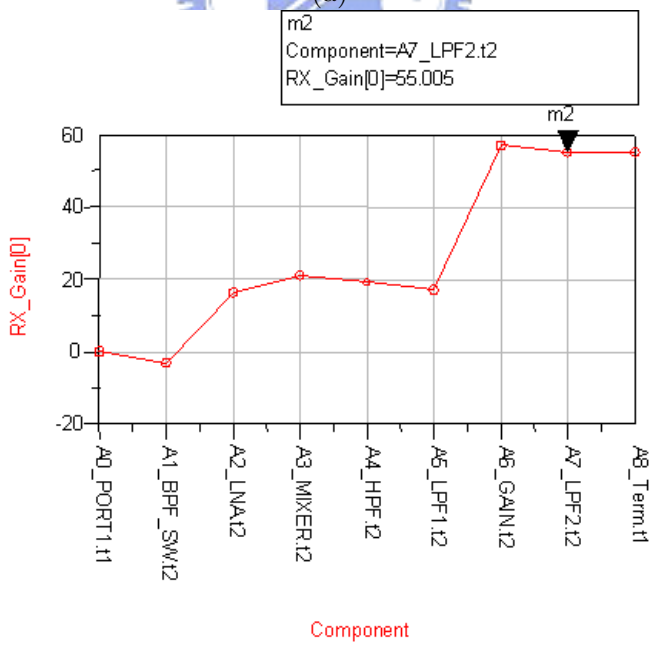
6.1.1 Behavior Design

Behavior simulation is necessary to determine the specifications for each building block such that the overall performance of the receiver meets the requirement of IEEE802.11b standard. IEEE 802.11b mandates the sensitivity of receivers to receive signal level as low as -76 dBm for 11 Mbps mode [3]. Therefore the integrated receiver noise figure should be lower than 8 dB, assuming 3 dB of loss for filter and switch precedent to the low noise amplifier. The input 1-dB compression point and IP3 point should be no less than -23 dBm and -13 dBm, respectively.

The receiver front-end consists of a low noise amplifier and a pair of I/Q direct down conversion mixers. The low noise amplifier has two operation modes, high-gain and low-gain mode in order to reduce the linearity requirement of the receiver mixers. The link budget analysis is performed in ADS using AC budget simulation.



(a)



(b)

Figure 6.2: Receiver noise and gain budget analysis at high gain mode.

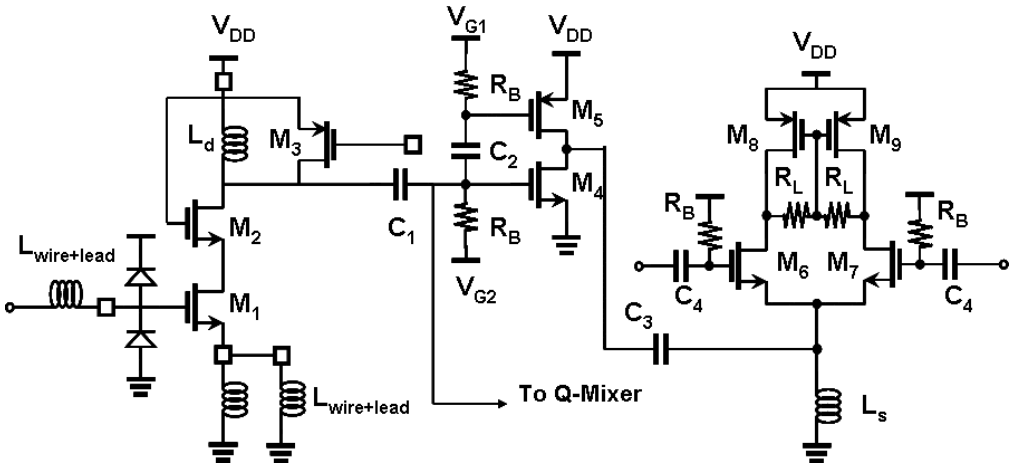


Figure 6.3: The receiver front-end schematic.

Figure 6.2 shows the noise and gain budget analysis results at high gain mode.

6.1.2 Circuit Design

The low noise amplifier (LNA) employs cascode architecture to increase the isolation from mixer input to LNA input to eliminate the LO leakage back to antenna. The LNA has an ESD protection circuit at the input which degrades the noise performance and requires careful design. To prevent further degradation of noise performance by input matching network, the input inductor is implemented by bonding wire and package lead instead of on-chip spiral inductors. The source degenerate inductor is implemented by two parallel of bonding wires and package leads. The input inductor together with the source degenerate inductor resonate the input gate capacitor of M_1 to perform 50 Ω impedance matching. To achieve two-gain mode operations, a PMOS transistor M_3 is shunt with the inductive load L_d. When a high voltage applies to the gate of M_3, the PMOS is off so that the load of the LNA is the impedance of L_d resonating the parasitic capacitor of M_3. When a low voltage applies to the gate of M_3, inductive load is shorted by M_3 so as to lower the LNA gain.

Conventional Gilbert-cell topology shares the same current of driver stage

Table 6.1: Element List

Device	Value	Device	Value
M_1	170/0.24	L_d	4 nH
M_2	170/0.24	L_s	7.6 nH
M_3	90/0.24	C_1	0.63 pF
M_4	110/0.24	C_2	1.6 pF
M_5	230/0.24	C_3	1.6 pF
M_6	150/0.5	C_4	2.5 pF
M_7	150/0.5	R_B	4.7 KΩ
M_8	410/0.65	R_L	1.7 KΩ
M_9	410/0.65	V_{DD}	2.5 V
V_{G1}	1.75 V	I_{DD}	10.5 mA
V_{G2}	0.75 V		

and switching stage and sets a noise figure and conversion gain design trade off for its application on direct conversion mixers. The driver stage has higher conversion gain with larger current drained while switching stage has lower 1/f noise contribution with lower current drawn. By separating the driver stage and the switching stage, the bias current of the differential switching pair does not have to be constrained by the driver stage as conventional single-balanced mixers [42]. Though current-injection mixers help to decouple the design tradeoff [43], the intermodulation performance is still limited due to further lowering the biasing current of switching stage. Since direction conversion receivers are prone to 1/f noise at the output stage, the mixer adopts the AC-coupled current-folded topology as discussed in Chapter 4. Capacitor C_2 couples the RF signal of the driver stage and also blocks the 1/f noise contributed by the driver stage into the switching stage. The bias point of the differential switching pair can be lowered to eliminate 1/f noise contribution of the switching pair without degrading the linearity performance.

The overall receiver front-end is depicted in Figure 6.3 and device parameters are list in Table 6.1. The simulation results of noise figure and conversion gain as RF input power sweep at high gain mode is shown in Figure 6.4. The simulation takes into account the parasitic of ESD circuit as well as bonding wires and package

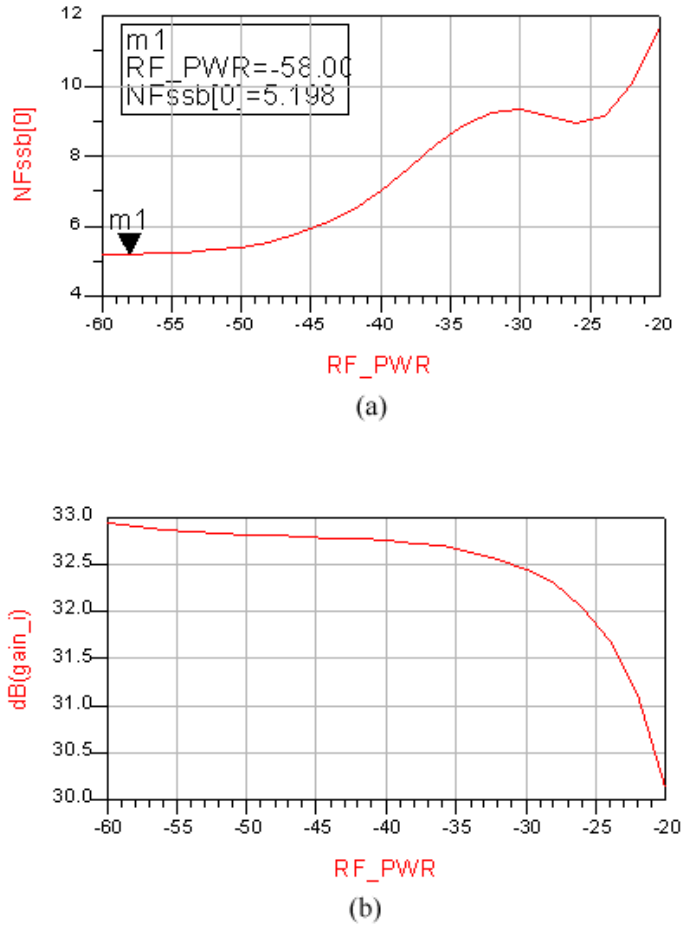


Figure 6.4: The receiver front-end simulation results: (a) noise figure; (b) conversion gain.

leads. The QFN package model is depicted in Figure 6.5. The simulation is base on harmonic-balance simulation at IF of 330 kHz to demonstrate the 1/f noise contribution to noise figure. The receiver front-end shows a conversion gain of 32 dB and a single-sideband noise figure of 5.2 dB.

6.2 RF/Baseband Co-verification and Co-design

The DC offset of the direct conversion receiver can be mitigated by an external AC coupling capacitor, however the highpass effect of the capacitor also blocks

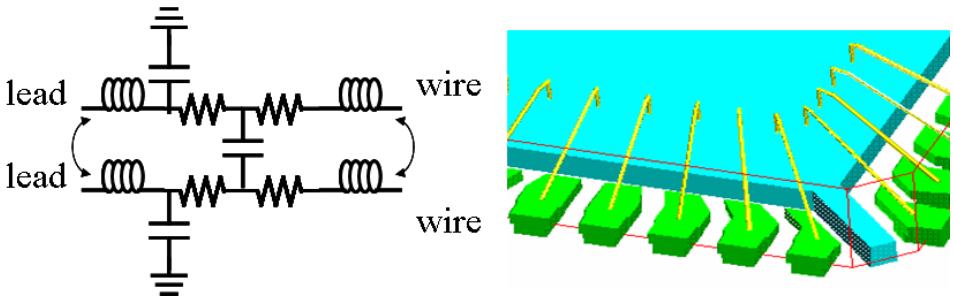


Figure 6.5: QFN package equivalent circuit model.

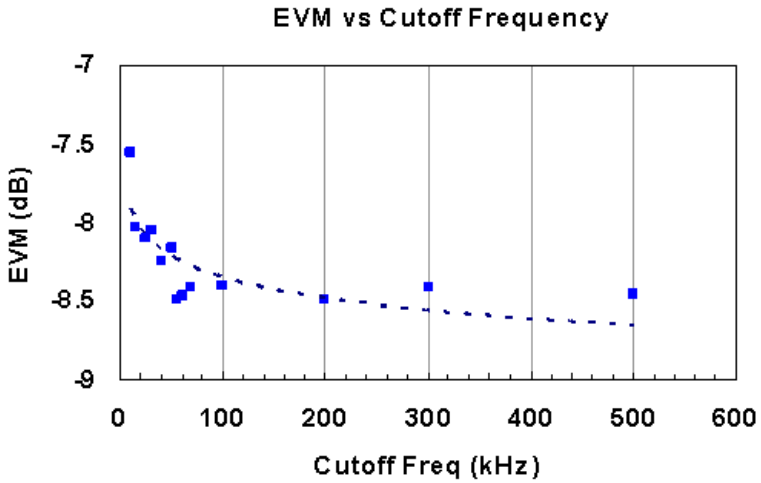


Figure 6.6: Effects of the highpass cutoff frequency on EVM.

the baseband signals. Hence the highpass cutoff frequency must be determined with actual modulated signals to evaluate the effects on EVM. The co-simulation of circuit-level RF with algorithm-level baseband can be applied to determine the cutoff frequency.

The co-verification platform is fulfilled in the DSP environment of ADS. The data flow simulator and circuit envelope simulator enables co-simulation of algorithm-level baseband with circuit-level RF front-end. An algorithm-level of 11 M symbol/sec QPSK modulation baseband transceiver has been established to co-simulate with the RF front-end circuit designed with UMC 0.25-μm RFCMOS

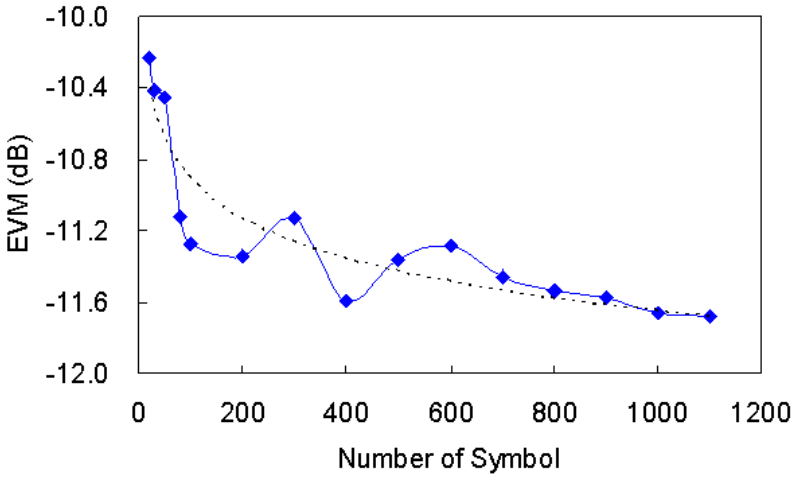


Figure 6.7: EVM converges when number of symbol is larger than 1000.

design kit.

Figure 6.6 shows the circuit-level co-simulation of EVM with various highpass cutoff frequencies of the AC coupling capacitor. The EVM goes higher as cutoff frequency decreases because of less DC offset can be removed. As the cutoff frequency increases, the EVM decreases and saturates when highpass cutoff frequency is larger than 60 kHz.

The RF/Baseband co-simulation considers 1000 symbols to obtain reasonable simulation results, since the EVM simulation result converges when the number of symbols considered is larger than 1000 as shown in Figure 6.7. Table 6.2 shows the RF/Baseband co-verification results at various abstraction levels from behavior to post-layout extraction level. The ideal required SNR as well as Intersil baseband required SNR are also given as a comparison to the co-simulation results. Even though the receiver front-end circuit simulation shows about 5 dB noise figure which meets the behavior specification, the EVM has 4 dB degradation from behavior level to circuit level co-simulation. This is because there are some other impairments not well modeled by the behavior. The receiver front-end exhibits -11 dB of EVM when

Table 6.2: RF/Baseband Co-verification Results

Input Power	−83	−80	−79	−76	dBm
Input SNR	17.4	20.4	21.4	24.4	dB
Ideal required SNR	−0.25	3.25	2.0	5.0	dB
Intersil required SNR	1.0	5.0	4.5	8.5	dB
Behavior-level EVM	−9.02	−11.93	−12.54	−15.01	dB
Circuit-level EVM	−5.59	−8.49	−9.33	−11.73	dB
Layout-level EVM	−5.39	−8.25	−9.01	−11.66	dB

input power is −76 dBm.

6.3 Experimental Results

To verify the design methodology, the receiver front-end is implemented with UMC 0.25-μm 1P5M RFCMOS process equipped with thick top metal and the circuit layout is shown in Figure 6.8. The die area is about 1800×1800 μm^2, but the core circuit occupies only one-sixth of the whole area. This is because the pad coordinates must be fixed prior to obtain the package models. The receiver front-end circuit is encapsulated with QFN5x5-20L package and mounted on a FR-4 printed circuit board as shown in Figure 6.9. The schematic of the printed circuit board is depicted in Figure 6.10.

Instead of measuring the low frequency noise figure of the receiver, an error vector magnitude measurement is employed to verify the performance. The measurement setup is shown in Figure 6.12. The RF front-end circuit module down converts a 2.4-GHz 11M symbol/sec QPSK modulation input signal generated by a signal generator (Agilent E4438C ESG). The 2.4-GHz quadrature LO signals are generated by another ESG and passed through a quadrature phase shifter composed of a rat-race coupler and two branch-line couples on a FR-4 circuit board (Figure 6.11(a)). The down-converted I/Q differential analog baseband signals are amplified by a dual-channel variable gain amplifier by Analog Device (AD605) and

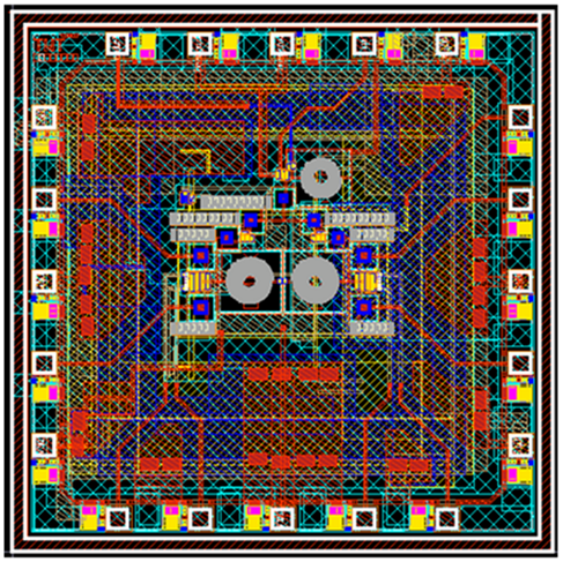


Figure 6.8: The RF receiver front-end circuit layout.

converted to single-end I/Q signals (Figure 6.11(b)).

The single-end I/Q signals are fed into the two-channel inputs of a vector signal analyzer (Agilent 89441, VSA). The VSA plays a role as a baseband demodulator. Though the RF and LO frequencies are the same in a direct conversion receiver, there is a frequency offset between the RF and LO signals because they are generated by two unlocked signal generators. The equalizer of the VSA is enabled to compensate the frequency offset and to simulate the frequency compensation in practical baseband demodulators. Figure 6.13 shows the EVM of the receiver front-end is 34.76% or −9.18 dB at −76 dBm input signal. The receiver front-end consumes 10.5 mA at 2.5 V power supply. There is about 2 dB implementation loss due to the uncounted the quadrature LO phase shift errors in the co-verification.

6.4 Summary

A 2.4-GHz CMOS direct conversion receiver front-end has been presented. Implemented in 0.25-μm CMOS technology, the RF front-end exhibits a EVM of −9.18 dB at −76 dBm 11M symbol/sec QPSK modulation. The receiver

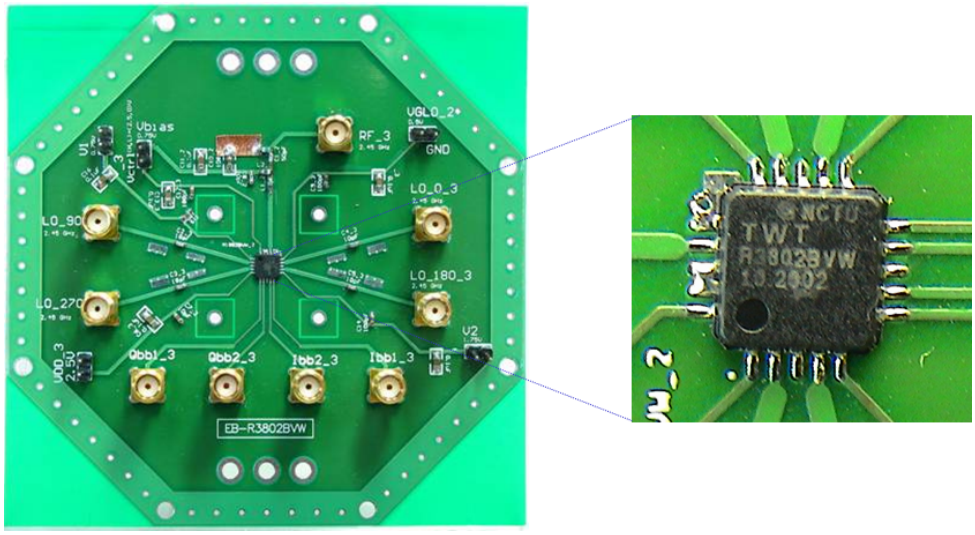


Figure 6.9: The RF receiver front-end circuit board.

front-end design is based on RF/Baseband co-verification methodology to assure the performance before the chip fabrication. The measurement result shows the prediction capability of the co-verification approach. It will be helpful to assure design freeze before fabrications.

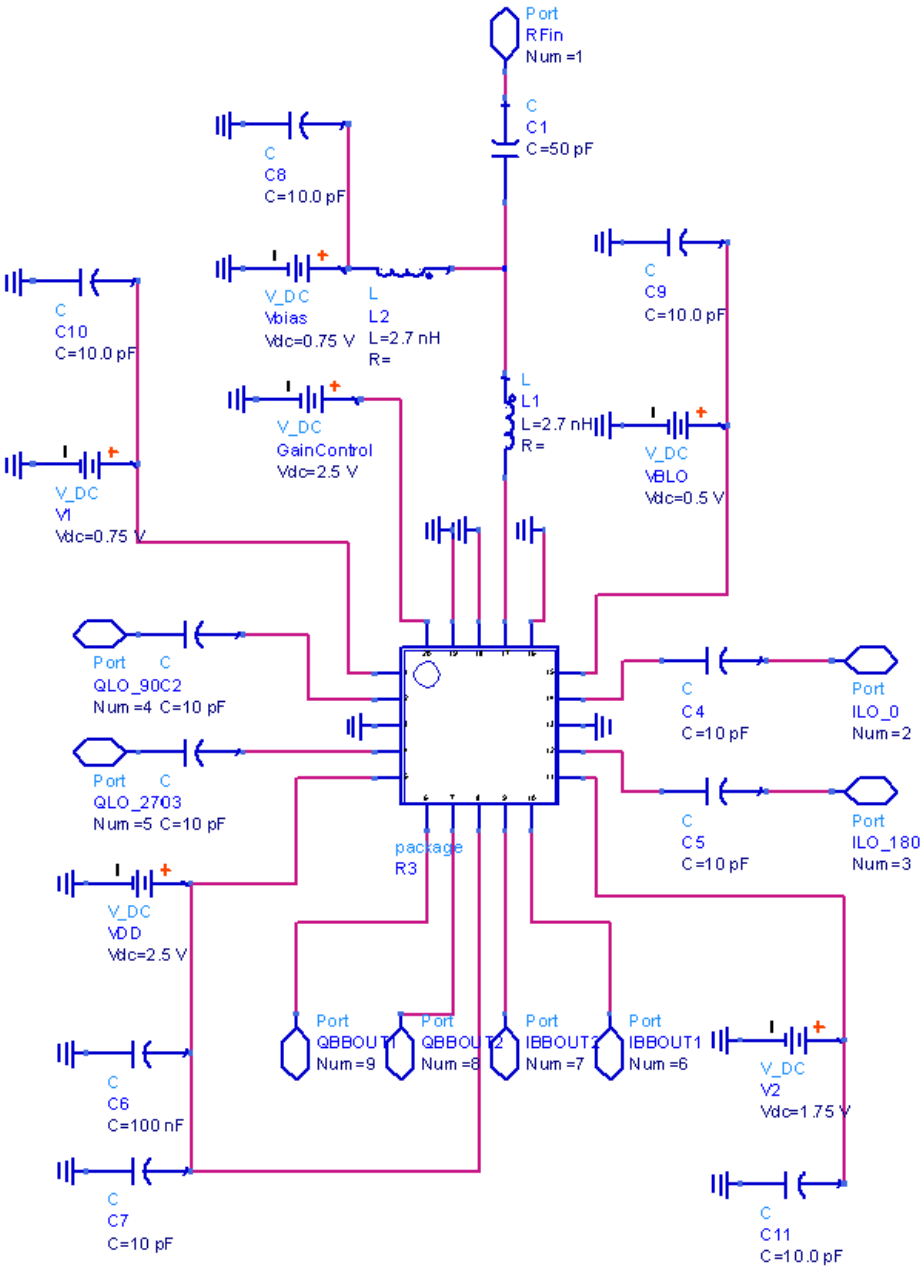
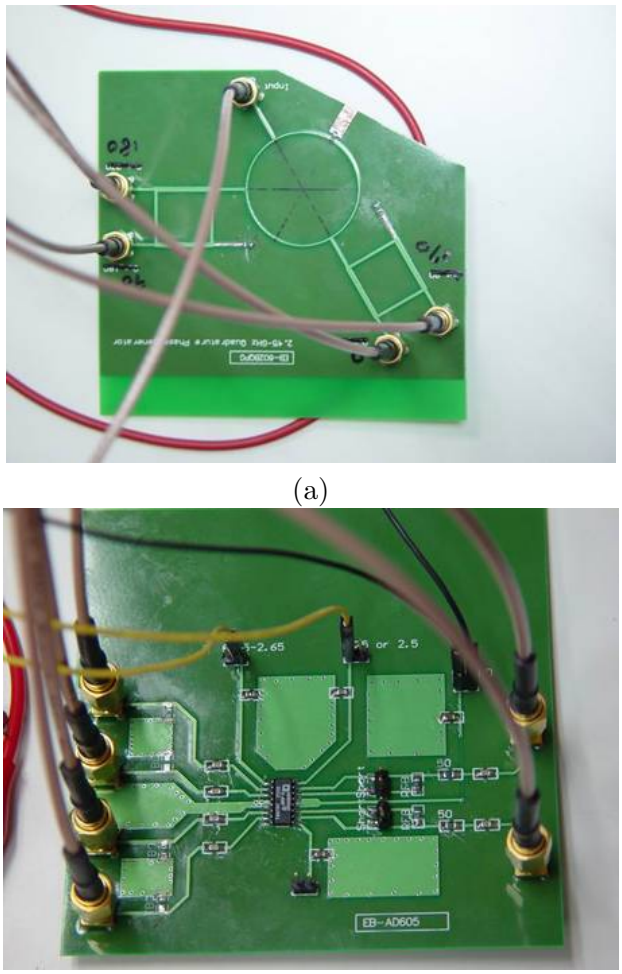


Figure 6.10: The RF receiver front-end circuit board schematic.



(a)

(b)

Figure 6.11: Other circuit board: (a) the quadrature phase shifter; (b) the variable gain amplifier.

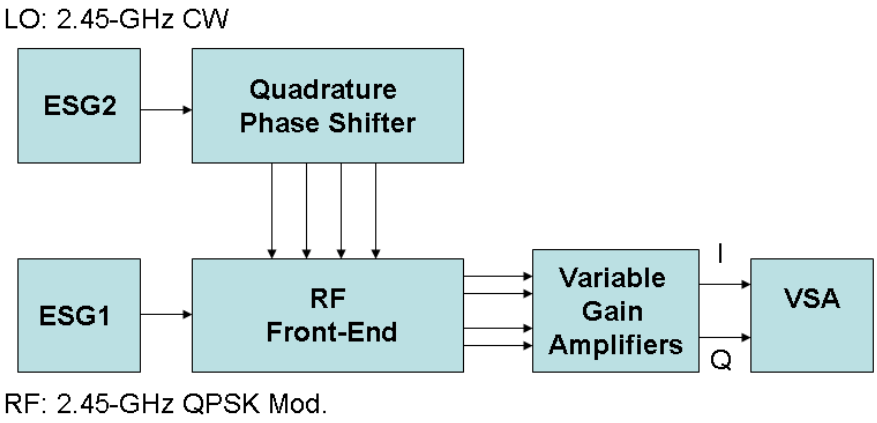


Figure 6.12: EVM measurement setup.

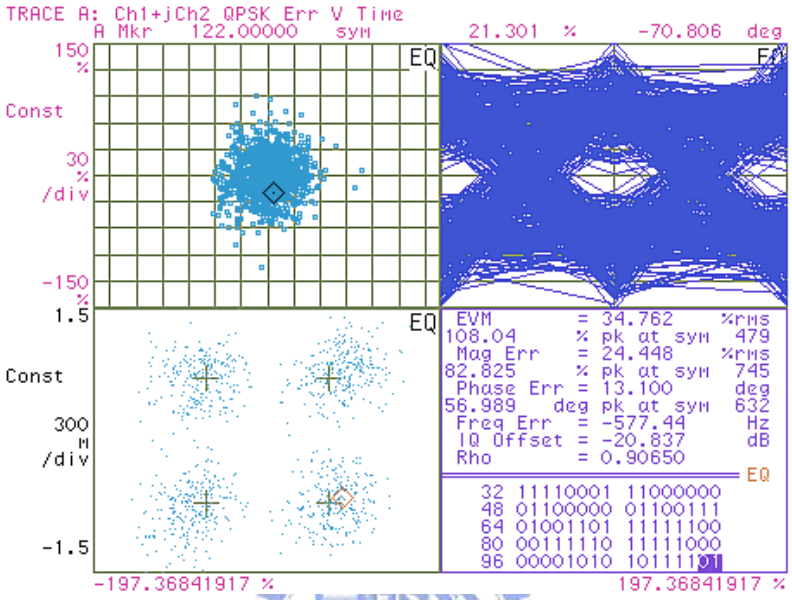


Figure 6.13: EVM measurement result of the receiver front-end.

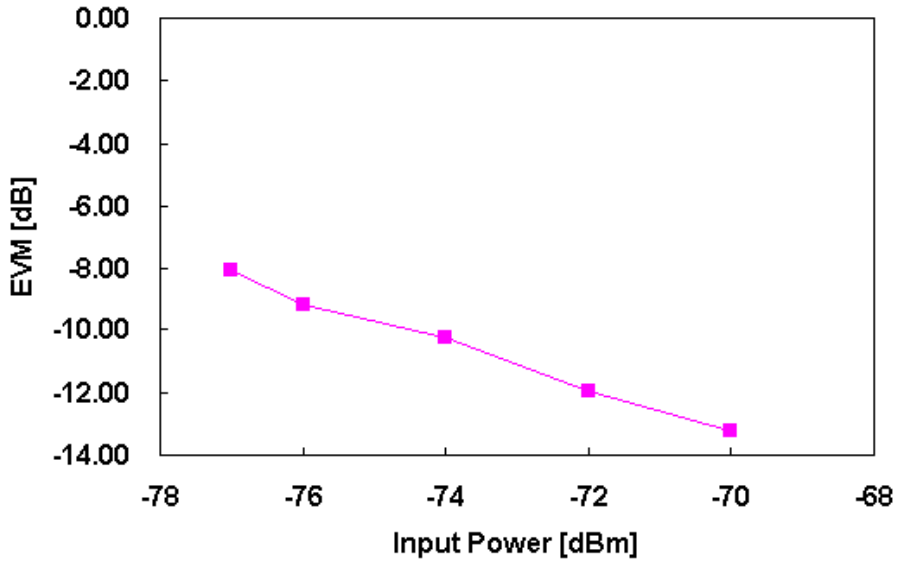


Figure 6.14: EVM versus input power.