V_{in} is copied to the scaled differential pair M_{N3}–M_{N4}, yielding the required weighted voltage.

Since the differential pair structure offers an extremely high input impedance, the loading effect on the controlled transistor (M_{N7}) is much reduced,[5] and resistance values in the MΩ range are readily available.

It may also be noted that the extension of this technique to floating resistors, involving the feedback of V_D and V_S, would increase the quiescent power consumption and complexity, but is entirely straightforward.

Simulation results: SPICE simulations of the basic GVCR and its application as the resistive elements in the familiar two-integrator-loop biquadratic filter section have been performed. The results were obtained using realistic level 3 models (with gate-voltage-dependent mobility) for all MOS devices. However, auxiliary devices, including capacitors and operational amplifiers, were assumed to be ideal.

The DC current/voltage characteristics for the GVCR of Fig. 1 are shown in Fig. 2 for a range of control voltages. This family of curves shows that the resistor offers good linearity for terminal voltage swings up to 5 V_{pp}, combined with a wide tuning range (from 60 kΩ to over 200 kΩ for this example). It may be noted that the operational range for the gate control voltage V_C is limited by the saturation conditions on M_{N5}–M_{N6} and M_{P1}–M_{P2}. With the bias supplies set at ±5 V it was found that V_C could be varied between 2·8 and 3·9 V.

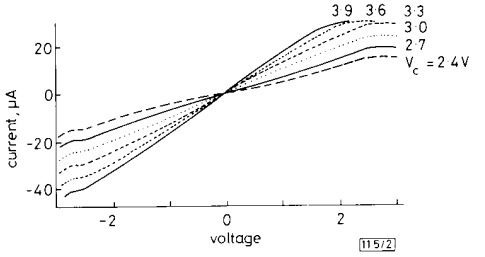

Fig. 2 *Variation of GVCR static v/i characteristics with control voltage V_C*

As previously shown, the values for m are dependent on V_B, ϕ_B and γ and could range from 1·05 to 1·3. In the process considered, the model parameters employed in the n-channel transistors were $\gamma = 0{\cdot}65\ V^{1/2}$, $\phi_B = 0{\cdot}677$ V and $V_B = -5$ V. This, it may be noted, sets $m = 1{\cdot}13$ and requires the optimum K_3/K_1, K_4/K_2 ratios to be 3·1. However, simulation revealed that distortion was actually minimised with K_3/K_1 and K_4/K_2 at the lower value of 2·6. The discrepancies appear to be due to imperfections in the current-mirror (M_{P1}–M_{P2}) and the nonlinear nature of the differential pairs.

Frequency response evaluations predict a 3 dB bandwidth for the control circuitry of 3 MHz at $I_0 = 6\ \mu$A, a larger bandwidth being possible, but at the cost of increased power consumption and distortion. For example, doubling I_0 to 12 μA gives a 3 dB bandwidth of 4·3 MHz, but increases distortion by 0·5% ($V_{in} = 1$ V_{pp} and $V_C = 3{\cdot}2$ V).

The aspect ratios resulting in minimum distortion were 5/50 for M_{N1}–M_{N2}, 13/50 for M_{N3}–M_{N4}, 70/10 for M_{N5}–M_{N6}, 10/50 for M_{N7} and 80/10 for M_{P1}–M_{P2}; V_{bias} was −3·8 V.

Fig. 3 shows the schematic diagram for a 'biquad'-type implementation of a second-order Chebyshev lowpass function with a passband ripple of 0·5 dB and a 4·7 kHz cutoff frequency. Although this example contains six GVCRs, the presence of common inputs reduces the number of (identical) control circuits required (as embodied in Fig. 1) to only four.

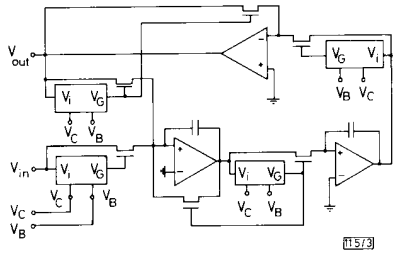

Fig. 3 *GVCR-based implementation of two-integrator-loop second-order lowpass filter structure*

Amplitude/frequency response simulations show good agreement with the design specification, and indicate that stopband attenuations in excess of 100 dB should be attainable at frequencies in the MHz range. Distortion analyses also show THD levels would typically be lower than 1% for input signals up to 4 V_{pp}.

Conclusions: A tunable grounded MOSFET resistor has been described in which linearisation is achieved via terminal-voltage feedback. Simulation results have shown that resistance values in the MΩ region can be realised, and that a biquadratic filter section based on the proposed device would maintain reasonably low levels of distortion with relatively large input signals.

These unbalanced structures could provide an economic alternative to the balanced arrangements previously advocated for use in fully integrated continuous-time MOSFET-C filters.

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References

1 TSIDIVIS, Y., BANU, M., and KHOURY, J.: 'Continuous-time MOSFET-C filters', *IEEE J. Solid-State Circ.*, 1986, **SC-21**, pp. 15–29
2 BANU, M., and TSIVIDIS, Y.: 'Floating voltage-controlled resistors in CMOS technology', *Electron. Lett.*, 1982, **18**, pp. 678–679
3 HAN, I. S., and PARK, S. B.: 'Voltage-controlled linear resistor by two MOS transistors and its application to active *RC* filter MOS integration', *Proc. IEEE*, 1984, **72**, pp. 1655–1657
4 BABANEZHAD, J. N., and TEMES, G. C.: 'A linear NMOS depletion resistor and its application in an integrated amplifier', *IEEE J. Solid-State Circ.*, 1984, **SC-19**, pp. 932–938
5 BILOTTI, A.: 'Operation of a MOS transistor as a variable transistor', *Proc. IEEE*, 1966, **54**, pp. 1093–1094
6 BANU, M., and TSIVIDIS, Y.: 'Detailed analysis of nonidealities in MOS fully integrated active *RC* filters based on balanced networks', *IEE Proc. G*, 1984, **131**, pp. 190–196
7 TORRANCE, R. R., VISWANATHAN, T. T., and HANSON, J. V.: 'CMOS voltage to current transducers', *IEEE Trans.*, 1985, **CAS-32**, pp. 1097–1104

CIRCUIT EXAMPLE TO DEMONSTRATE THAT FAN-OUT STEMS OF PRIMARY INPUTS MUST BE CHECKPOINTS

Indexing terms: Logic and logic design, Logic circuits, Combinatorial circuits

A simple circuit example is presented to demonstrate that the set of checkpoints should include the fan-out stems of primary inputs for irredundant combinational circuits. It is shown that transistor faults are not sufficient to constitute a complete set of checkpoints for combinational MOS circuits.

To reduce the time for test generation and fault simulation, the fault collapsing technique is used to reduce the number of faults to be considered. Faults are combined into classes based on a geometric structure for which the circuit is effectively divided into fan-out regions. The checkpoint theory has been presented by Bossen *et al.*[1] and Breuer *et al.*[2] to collapse faults. The set of primary inputs and the fan-out branches are sufficient to constitute a complete set of checkpoints for a

combinational circuit. However, no circuit example, either in the above References or in any published literature, has been given to demonstrate that it should be necessary. As a result, many researchers, like Shih *et al.*,[3] who dealt with this problem for MOS circuits, and Miczo,[4] did not include the fan-out stems of primary inputs in the set of checkpoints.

In this letter we give a simple circuit example which contains only six NAND gates to demonstrate that the fan-out stems of primary inputs should be included in the set of checkpoints for irredundant combinational circuits. The logic diagram of the circuit and the circuit diagram implemented in NMOS technology are shown in Fig. 1*a* and *b*, respectively. Tables 1*a* and *b* list the stuck-at-1 and stuck-at-0 line faults of the circuit of Fig. 1*a* and the stuck-on and stuck-open transistor faults of the circuit of Fig. 1*b*, respectively. For this circuit, the set of tests, $T = \{011, 101, 110, 111\}$, detects all single stuck-at line faults and all single transistor stuck faults of all the fan-out branches, but does not detect the primary input fanout stem fault, ***b*** stuck-at-1. To detect the ***b*** stuck-at-1 line fault, an extra pattern {001} or {100} is needed. This is because that the reconvergent fan-out of the fan-out stem ***b***,

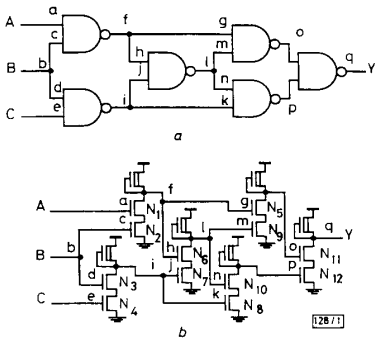

Fig. 1 *Example circuit of six NAND gates*
a Logic diagram
b Circuit diagram which is implemented in NMOS technology

Table 1 FAULT TABLE FOR CIRCUIT OF FIG. 1

		Line stuck-at-1 fault															
ABC	Y	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q
000	0												1	1	1			1
001	0		1		1								1	1	1			1
010	0	1				1							1	1	1			1
011	1	0								0	0					0		
100	0		1	1									1	1	1			1
101	0			1	1								1	1	1			1
110	1					0	0		0								0	
111	0						1	1		1		1						1

		Line stuck-at-0 fault																
ABC	Y	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q
000	0						1		1	1	1					1	1	
001	0						1		1	1	1					1	1	
010	0						1		1	1	1					1	1	
011	1		0		0	0	0	0					0	0				0
100	0						1		1	1	1					1	1	
101	0						1		1	1	1					1	1	
110	1	0	0	0						0		0	0		0			0
111	0	1		1	1	1										1	1	

a

		Transistor stuck-on fault											
ABC	Y	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12
000	0									1	1		
001	0			1						1	1		
010	0	1			1					1	1		
011	1	0						0				0	
100	0		1							1	1		
101	0		1	1						1	1		
110	1				0		0						0
111	0					1			1				

		Transistor stuck-open fault											
ABC	Y	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12
000	0						1	1				1	1
001	0						1	1				1	1
010	0						1	1				1	1
011	1			0	0	0				0			
100	0						1	1				1	1
101	0						1	1				1	1
110	1	0	0						0		0		
111	0	1	1	1	1							1	1

b

(*a*) Lists of line faults for circuit of Fig. 1*a*; and (*b*) lists of transistor faults for circuit of Fig. 1*b*. Note that only detectable faults are listed

which is a primary input, masks this fault for T. Hence, the complete set of checkpoints must include the fan-out stem of primary inputs. It should be mentioned that this circuit is irredundant. For each fault, there exists at least one test pattern to detect it.

Fig. 1*a* can also be implemented in the CMOS version. The same analysis can be applied.

In conclusion, this letter, for the first time, gives a circuit example to demonstrate that the fan-out stems of primary inputs are necessary checkpoints for 'irredundant' combinational circuits. Breuer's checkpoint theorem,[2] therefore, should be restated as the following: 'In an irredundant combinational circuit, any test, which detects all single stuck faults on all primary inputs and all branches of fan-out points, detects all single faults'.

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References

1 BOSSEN, D. C., and HONG, S. J.: 'Cause-effect analysis for multiple fault detection in combinational networks', *IEEE Trans.*, 1971, **C-20**, pp. 1252–1275
2 BREUER, M. A., and FRIEDMAN, A. D.: 'Diagnosis and reliable design of digital systems' (Computer Science Press, Woodland Hills, CA, 1976)
3 SHIH, H. C., and ABRAHAM, J. A.: 'Fault collapsing techniques for MOS VLSI circuits'. Proc. 16th int. symp. on fault tolerant comput., Vienna, Austria, July 1986, pp. 370–375
4 MICZO, A.: 'Digital logic testing and simulation' (Harper & Row, 1986), pp. 192–193

CONTROL OF GATE LEAKAGE IN AlInAs-INSULATOR HIGFETs

Indexing terms: Semiconductor devices and materials, FETs, Semiconductor doping

By proper optimisation of the channel, the gate leakage of 1 μm gate-length GaInAs HIGFETs has been reduced to below 10 nA/mm. This has been achieved in a delta-doped structure in which Zener tunnelling is inoperative.

$Ga_{0.47}In_{0.53}As$ (hereafter GaInAs) has many advantages when used in the conducting channel of field-effect transistors (FETs). However, one of the problems hindering the development of GaInAs-based FETs has been the low Schottky barrier height, which causes unacceptably high gate leakage. Oxidation treatments have been proposed;[1] however, work on GaInAs FETs has concentrated on junction FETs,[2] high electron mobility transistors and heterojunction insulated gate FETs (HIGFETs).[3,4]

For low noise applications, the reduction of reverse bias gate leakage is of great importance. In this letter it is demonstrated that a dramatic decrease in gate leakage can be obtained by suitable design of the FET conducting channel, so that the channel is totally depleted before Zener tunnelling can become operative. This effect is observed in HIGFET devices, in which a layer of undoped high-bandgap $Al_{0.48}In_{0.52}As$ (hereafter AlInAs) separates the gate from the channel.

Zener tunnelling of electrons from the valence band to an empty conduction band state is much stronger in low-bandgap semiconductors like GaInAs than in GaAs. It is only operative if the voltage dropped across the channel is in excess of the bandgap. This implies that if the channel can be pinched-off by a voltage of less than its bandgap, Zener tunnelling should be eliminated. Thus, if

$$E_g > V_{dep} (= V_p - V_{ins} - V_{bi}) \quad (1)$$

where V_{bi} is the built-in voltage (equal to the difference in Schottky barrier height ϕ_m and conduction bandgap discontinuity ΔE_c), V_p the pinch-off voltage, V_{dep} the voltage dropped in the channel at pinch-off, V_{ins} the voltage dropped across the insulator at pinch-off and E_g is the bandgap of the channel.

This suggests that in a suitable high-transconductance structure it should be possible to suppress Zener tunnelling, giving reduced gate leakage. The delta-doped HIGFET,[3] in which doping consists of a thin spike, has a small V_{dep} and thus the inequality in expr. 1 should be satisfied.

The samples used in this work were grown by MBE on Fe-doped InP substrates. Results from two structures are discussed below; these had identical insulating top layers to ensure that gate leakage associated with the insulator was the same for both wafers.

The first structure (A) consisted of a 1·2 μm-thick GaInAs channel ($n = 1{\cdot}5 \times 10^{17}\,cm^{-3}$) capped with an insulating layer of 55 nm of lattice-matched AlInAs with a 5 nm-thick layer of *i*-InP. The second, 'delta-doped', wafer (B) used a 0·1 μm buffer of *i*-InP, followed by 20 nm of *i*-GaInAs, 6 nm of *n*-GaInAs ($n = 2 \times 10^{18}\,cm^{-3}$) and 2 nm of *i*-GaInAs. The insulating top layers were identical to those on structure A. Then NiAuGe ohmic contacts were annealed at 400°C, and TiPtAu gate metal was deposited onto the *i*-InP antioxidation layer. FETs were mesa isolated using standard etchants.

The forward bias current is dominated by thermionic emission over the channel/insulator interface. Formation of an accumulation layer leads to nonsaturating behaviour.[5]

Figs. 1*a* and *b* plot the gate currents for typical 1 μm gate-length FETs from wafers A and B, respectively. The forward bias gate current of both devices shows similar, i.e. non-Schottky, behaviour characterised by a sharp initial rise followed by a more gradual increase. The behaviour agrees with that predicted above.

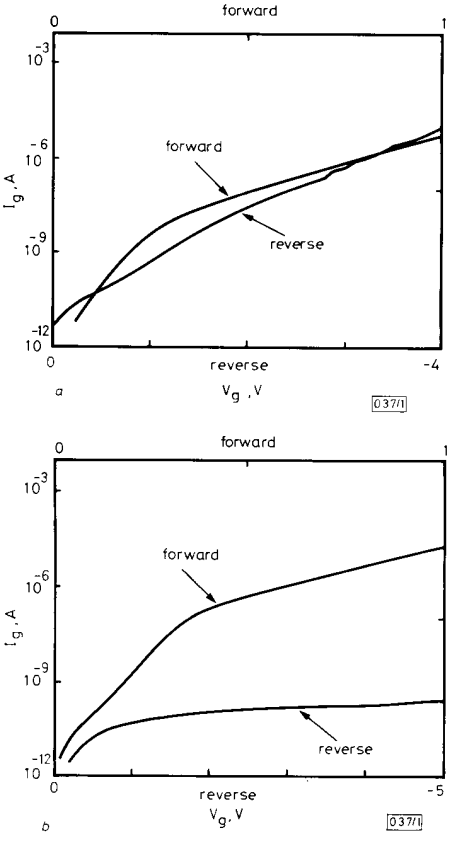

Fig. 1 *Forward- and reverse-bias gate current for 1 × 100 μm^2 FET at 300 K and $V_{ds} = 0$*
a Wafer A *b* Wafer B