國 立 交 通 大 學

電子物理學系

博士論文

氮化矽的氫與其應力對電晶體之影響

Impacts of Hydrogen and Stress Of the Silicon Nitride on the Transistors

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摘要

首先，此研究確認了利用壓縮應力的氮化矽覆蓋層相較於伸張應力的氮化矽覆蓋層具有較高於 N 型金氧半場效電晶體耦合應力記憶技術的潛力。我們提出選用覆蓋層的方法應該被調整為使用應力改變量最大而非傳統挑選的初始應力最大的覆蓋層。並且，我們也發現到初始覆蓋層內的氫含量與隨後於退火時釋放的氫含量都會影響介面處懸浮鍵的鈍化。另一方面，退火後的應力而非應力改變量主導了閘極氧化層的劣化，進而導致劣化的閘極漏電流，在熱載子的加壓測試下顯現較高的臨限電壓位移，以及較差的閃爍雜訊。隨後，我們有系統的研究了不同反應氣體流量所沉積的氮化矽對複晶矽薄膜電晶體的鈍化效應。覆蓋了氮化矽的複晶矽薄膜電晶體能夠展現更佳的性能表現，壓抑電流突增效應(Kink effect)與改善閘極漏電流與閘極導致的汲極漏電流(DIBL)。由於不同的鈍化效應，覆蓋不同製程製備的氮化矽的原件會展現不同的效應。一物理機制被提出以解釋不完整的缺陷鈍化所導致的雙駝(double hump)現象。根據不同寬度的元件比較，不只是自由基在複晶矽內的缺陷鈍化作用會改善原件傳輸特性，閘極氧化層內的缺陷鈍化也會造成元件特性的改善。此外，覆蓋了氮化矽的原件，會提升對於正閘極電壓加壓測試，負閘極電壓加壓測試，與熱載子的加壓測試的免疫力。再者，此製程非常的簡單(不需要面臨電漿處理需要長時間問題)並且與傳統薄膜電晶體有很高的相容性。

隨後，此研究根據不同氮化矽厚度與不同的四乙氧基矽烷氧化層厚度討論了富含氫的氮化矽對於氫鈍化效率的議題，並得到了利用氮化矽是十分有效率的鈍化方法結論。氫會遭受隨後的退火製程導致的不穩定性也被詳細討論。結果顯示使用氮化矽覆蓋層可以避免氫從複晶矽通道中釋放。然而，移除氮化矽會使得氫在隨後的熱製程中釋放，而使得原件特性與對照樣本的特性相似。移除了氮化矽的樣本可以減緩對於熱載子的加壓測試的劣化。然而，氫釋放會劣化對於正偏壓

溫度不穩定性加壓測試與負偏壓溫度不穩定性加壓測試的免疫力。兩種可能的機制被提出以解釋源自於氫釋放所導致的缺陷密度上升。此種不理想效應會影響熱載子的加壓測試，正偏壓溫度不穩定性加壓測試與負偏壓溫度不穩定性加壓測試。

最後，此研究討論了鄰近的薄膜對固相結晶與金屬側向結晶的影響。對於利用固相結晶的原件來說，將元件製備在氮化矽薄膜上會改變臨限電壓對溫度的相依性，其歸因於氫導致的成核點形成與氫或氮鈍化缺陷的行為。我們也發現在結晶前移除晶背後的非晶矽會影響原件的表現，其歸因於應力的影響。對於利用金屬側向結晶的原件來說，這些鄰近的薄膜不單會改變金屬側向結晶的速率，其也會改變電特性，故硬遮罩，緩衝氧化層，與絕緣墊片會因為不同的結晶特性而影響電特性。我們提出了三種可能的機制，包含了鎳捕捉，本質應力，與氫的參與，以釐清臨近薄膜的影響。

Impacts of Hydrogen and Stress Of the Silicon Nitride on the Transistors

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Abstract

First, this dissertation certified that the compressive SiN capping layer has more potential than the tensile layer for fabrication using the stress memorization technique to enhance NMOS mobility. The mechanism that we have proposed implies that the conventional choice of the capping layer should be modulated from the point of view of the stress shift rather than using the highest tensile film. We also found that both the initial component of the deposited capping layer and the H released during annealing affected interface-state passivation. On the other hand, the annealed stress rather than the stress shift are responsible for degraded gate oxide quality, leading to the degraded gate leakage, higher threshold voltage shift under hot carrier stressing, and degraded flicker noise. Then, the effect of the flow rate of different reactant gases on the deposition of the SiN layer for passivation of poly-Si TFTs had systematically investigated. SiN passivation layers were found to yield better performance, suppress the kink effect, and improve the gate leakage current and gate induce drain leakage (GIDL) of polysilicon thin film transistors (poly-Si TFTs). The SiN passivation layers deposited under different deposition conditions possess different characteristics, due to their varying passivation effect. A physical mechanism is proposed to explain the double hump phenomenon induced by incomplete trap passivation. Based on the analysis of width dependence, the better performance of the samples with SiN passivation layers was attributed to not only the radical passivation of the defect states, but also the radical passivation of pre-existing defects in the gate oxide. Furthermore, using SiN passivation layers improves the immunity to positive gate bias stress, negative gate bias stress, and hot carrier stressing. Moreover, the manufacturing processes are simple (without the long processing time plasma treatment requires) and compatible with TFT processes.

Then, this dissertation investigates the passivation efficiency of hydrogen by

hydrogen-containing nitride, based on a comparison of different thicknesses of SiN or inserted TEOS oxide, indicating that hydrogen diffusion is efficient. Hydrogen instability induced by post annealing is also reviewed in detail. Results show that using a SiN capping layer can prevent the release of hydrogen from a poly-Si channel. However, removing this SiN capping layer allows the hydrogen release during post annealing, and the resulting device performance becomes comparable to the control sample. Samples with SiN capping layers removed can alleviate degradation by hot carrier stressing. However, hydrogen release reduces the immunity of PBTI and NBTI. Two possible mechanisms can explain the increased pre-existing defects associated with hydrogen release, which affects the hot carrier stressing, NBTI, and PBTI.

Finally, this dissertation presented the impacts of the proximity layer on the SPC and MILC. For samples crystallized by SPC, the temperature dependence of threshold voltage are different for samples fabricated on the SiN proximity layer, and the formation of seed nuclei by hydrogen or traps passivated by hydrogen and nitrogen are responsible for this temperature dependence. Also, we found that removal of the backside a-Si before the crystallization would alter the performance originating from the stress viewpoint. For samples crystallized by MILC, The proximity layers not only affect the MILC growth rate, but also the electrical characteristics, meaning that the materials of the hard mask, the buffered layer, and the spacer affect the electrical characteristics due to the different crystallization conditions. Based on the comparison among the proximity layers, the SiN proximity layer is not suitable to be a hard mask or a spacer, due to the concern of crystallization condition. We proposed three reasonable mechanisms, including the gettering of Ni, the intrinsic stress, and the involvement of hydrogen, to make the deep understanding of the impacts of proximity layers.

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Chapter 1

Introduction

1.1 Background

SiN is one of the promising materials for sealing substrate against the process chemical, the outstanding adhesion, and the application of the gate dielectric or FinFET fabrication [1.1]-[1.3]. Recently, the interest in studying the capabilities of devices capped silicon nitride has been rapidly growing, including the potential of the strain coupling for metal-oxide-semiconductor field-effect transistors (MOSFETs) and the trap passivation by hydrogen radicals for poly-Si thin film transistors.

1.1.1 Strained Channel Technology

Strain techniques has emerged as one of the most promising remedies for boosting the drive current in scaled devices since 1980s [1.4]-[1.5]. When the band structure of material is changed by strain, the band gap, mobility, effective mass, diffusivity of dopants, and oxidation rate is altered simultaneously. The stress induced by local oxidation of silicon and shallow trench isolation was investigated about the impact on electron and hole mobility since 1997. However, the strain from a localized source decays rapidly away from the booster, it was not until deep submicrometer technologies were developed that these effects were observed experimentally [1.6]. For no significant processing cost, the mobility advantage offered by strain technology is a promising technique to meet transistor target as Fig.1-1 [1.7]. The strained thin film Si or Ge capped on strain-relaxed $SiGe_x$ buffer (SRB) as Fig. 1-2 (a) can create bi-axial tensile or compressive stress, and the mobility of carrier could be enhanced significantly. Whether or not SRB layer is used underneath will make influence on both misfit and threading dislocations [1.8]. Both electron and hole mobility are enhanced by tensile strain induced in the thin epitaxial Si layer grown on

a relaxed SiGe virtual substrate [1.9]. It is noted that the capping film should be optimized to control the underlying relaxed SiGe layer dislocation penetration and Ge out-diffusion during annealing, or the damaged interface state, gate oxide quality, and even bulk substrate trap would severely degrade device performance, reliability and flick noise characteristics [1.10]-[1.11]. Besides, the high wafer cost and enhancement loss at high vertical field possess significant concern [1.12]. In the 1990s, anther strained channel technology was proposes, uni-axial strain, which is induced by process and free from the aforementioned concerns of bi-axial strain. Compared to biaxial technique, uni-axial strain provides larger enhancement at both low strain and high vertical electric field due to difference in the warping of the valence band.

Uni-axial strain was thoroughly investigated by a large number researcher. Contact etching stop layer (CESL) was employed to generate uni-axial strain as Fig. 1-2(b) [1.13]-[1.16]. This technique can be easily incorporated into conventional process. Depending on the SiN fabrication process, the SiN could possess tensile stress or compressive stress. Dual-SiN stressor could both enhance NMOS and PMOS performance with appropriate CESL adoption, respectively.

The embedded SiGe source drain was adopted for PMOS, and the channel region would meet compressive strain by SiGe S/D stress as Fig. 1-3(a) [1.17]-[1.18]. Thus, the mobility of hole and drive current would enhance. Subsequently, the $Si_{1-y}C_y$ (y=1~2%) was proposed to fabricate tensile strain to promote NMOS performance as Fig. 1-3(b) [1.19]-[1.20]. Although the Ge-outdiffusion is avoided, C precipitation and C-related interface state are a crucial issue.

Recently, stress memorization technique (SMT) was introduced as a promising technique [1-21]-[1.25]. By the capping layer such as SiN or TEOS oxide and spacer confinement, the expanded volume of poly silicon gate would release its volume downward during annealing, and make the channel become vertical compressive as

Fig. 1-3(c). It is noted that the vertically compressive could significantly enhance electron mobility. Since the strain would enter plastic regime, the strain would remain after the capping layer was removed. Besides, the phenomenon of material expansion also plays a critical role in the SMT process. For poly-Si implantation, the deeper the R_p projection range using the same dosage, the more obvious the stress memorization. More effective recrystallization would thus occur and the volume swelling could be enhanced significantly.

1.1.2 Polysilicon TFT

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been studied because of their potential application in high performance active matrix thin-film displays on glass substrates and high density vertically components [1.26]. The polysilicon layer is a disordered material with a significant number of defect states. This high density of defects would degrade threshold voltage, subthreshold swing, mobility, and leakage current.

Because the grain boundaries in poly-Si TFTs have a profound influence on device characteristics and degrade carrier transport, developing promising techniques to reduce the trap density is important. Poly-Si has been formed using a variety of techniques, such as direct growth by low-pressure chemical vapor deposition (LPCVD) [1.27], and annealing of amorphous silicon (a-Si) by rapid thermal annealing (RTA) [1.28], laser crystallization (LC) [1.29], and solid-phase crystallization (SPC) [1.30]. Also, Nickel (Ni) based metal-induced lateral crystallization (MILC) of a-Si has been proposed to obtain high performance TFTs. RTA is a high temperature (>600^{o}C) process, resulting in films with a high defect density [1.31]. By localizing the high temperature to the silicon film, LC can be

considered a “low-T” process. Although it is capable of producing poly-Si films with low defect density, is suffers from high initial setup cost, high process complexity, and unacceptable uniformity. Conventional SPC possesses a relatively inexpensive batch process and a superior uniformity, the process temperature is still high. Moreover, MILC process would encounter the issue of metal residue, leading to unacceptable leakage current [1.32].

Previous research shows that hydrogen plasma treatment and hydrogen-containing nitride film deposition are promising approaches for improving performance [1.33]- [1.35], because hydrogen radicals can effectively passivate the defects of intra-grain, grain boundary, and the gate dielectric [1.33]- [1.34]. Also, O_2, N_2 and CF_4 plasma have also been found to be effective to enhance the poly-Si TFTs performance [1.35]- [1.37].

Using the non-hydrostatic stress is another approach for improving the poly-Si TFT performance. A lot of works have been done for clarifying the influence of the mechanical stress, including the stress applied before the crystallization [1.38] or after the crystallization [1.39]. For the stress applied before the crystallization, the tensile stress increases the growth rate of the crystallization, but the compressive stress retards the growth rate of the crystallization. For the stress applied after the crystallization, the tensile stress would increase the electron mobility, but degrade the hole mobility.

1.1.3 Mobility Enhancement Physics

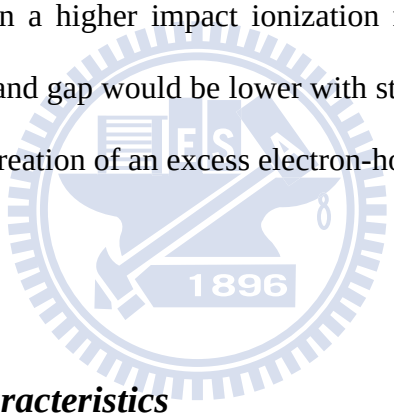
The carrier mobility is given by $\mu = \frac{q\tau}{m^*}$, where τ is the mean free time and m^* is the conductivity effective mass. With the strain coupling, the changed band

structure of Silicon modulates inter-valley scattering probability as well as effective mass. For NMOS, electron distribute in the six degenerate valleys as the same energy as Fig. 1-4. Compared to four-fold valley, the two-fold valley on (100) wafer along Si/SiO_2 interface (transport direction k_x) have lower effective mass [1.40]. With the SiGe biaxial strain coupling, the subband energy difference between four-fold Δ_4 valley and two-fold Δ_2 valley would increase, meaning that Δ_4 valley would lose electron to Δ_2 valley as Fig. 1-5. The curvature of conduction band near the Brillouin Zone is relatively insensitive to strain [1.41]. Thus, strain-induced mobility enhancement origin from the valley-splitting, and the carrier would almost redistribute in the Δ_2 valley possessed lower effective mass. Thus, the mobility would be enhanced by lowering the effective mass generally. Additionally, the inter-valley scattering would also be suppressed by the increased valley splitting between Δ_4 valley and Δ_2 valley [1.42]- [1.43].

For the uni-axial strain, the sensitivity of band structure to strain is different according to the Si channel direction and orientation the transistor fabricated on. For example, devices along <100> compared to the <110> as Fig. 1-6 possesses higher sensitivity for uniaxial strain, where uniaxial strain is parallel to transport direction [1.42]-[1.43]. From the band structure, strained device along <100> as Fig. 1-7 possesses an anisotropic occupation of four fold valley. Therefore, the anisotropic occupation is responsible for the lower conductivity mass compared to <110> strained device. For the same strain coupling, the bi-axial strain induces largest band splitting and uniaxial <110> strain induces smallest one. For uniaxial strain, the curvature of conduction band near the Brillouin Zone is also relatively insensitive to strain, meaning that the carrier repopulation is the dominant mobility enhancement mechanism.

1.1.4 Hot Carrier Effects

Hot carrier, which was produced by the high lateral electric field near the drain, can generate electron-hole pairs via impact ionization. Subsequently, the hot carrier with high energy would inject into the gate oxide, and the oxide quality and interface state would be degraded [1.44]- [1.45]. Thus, the hot carrier effect would cause threshold voltage shift and degraded subthreshold swing. As the strain technique application, the altered band structure also makes influence on the hot carrier effects [1.46]- [1.48]. The higher carrier mobility in strained channels implies a lower electric field at velocity saturation. Carrier heating in the maximum field near the drain becomes easier, resulting in a higher impact ionization rate and a higher substrate current. Additionally, the band gap would be lower with strain coupling, meaning that lower energy is lost in the creation of an excess electron-hole pair.



1.1.5 Flicker Noise characteristics

The origin of the 1/f noise in MOSFET has been debated for several decades, whether mobility fluctuation noise due to the phonon scattering [1.49]- [1.50] or number fluctuation noise due to traps in the gate oxide [1.51]-[1.52]. McWorther proposed a 1/f noise model based on quantum mechanical tunneling transitions of electron the channel and traps in the gate oxide [1.53]. Since the tunneling time depends on the distance from the channel to trap, the distribution of time constants would produce 1/f noise as Eq. (1-1).

$$S_{I_D} = \frac{q^2 kT\lambda N_t}{f^{\gamma} WLC_{ox}^2} \frac{I_D^2}{(V_g - V_t)^2} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1-1)$$

The frequency component γ deviates from 1 if the trap density is not uniform in depth ; $\gamma < 1$ is observed when the trap density is higher close to the gate oxide/channel interface than that in the interior of the gate oxide and $\gamma > 1$ for the opposite condition. The model possesses excellent agreement with experiments for NMOS than PMOS. In addition to inversion charge density fluctuation, it was later proposed that a trapped carrier also affects the surface mobility through coulomb interaction, called as correlated mobility fluctuation as Eq. (1-2). However, the correction factor as constant was criticized for being unphysically, since screening was not accounted for [1.54]- [1.55]. Instead, α should be expected to decrease with increasing inversion charge density due to the screening effect.

$$S_{I_D} = \frac{q^2 kT\lambda N_t}{f^{\gamma} WLC_{ox}^2} (1 + \frac{\alpha \mu_{eff} C_{ox} I_D}{g_m})^2 g_m^2 \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1-2)$$

On the other hand, the mobility fluctuation theory considers flicker noise as a result of fluctuation in bulk mobility, due to phonon scattering as Eq. (1-3).

$$\frac{S_{Id}}{I_D^2} = \frac{q\alpha_H \mu_{eff} V_{DS}}{fL^2 I_D} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1-3)$$

It is noted that both number fluctuation and mobility fluctuation may fail to accurately describe the LF noise data over the entire bias range. The mobility fluctuation model is often fitting in strong inversion, and the number fluctuation is more useful below and around threshold.

1.2 Motivation

Recently, using SiN to improve device performance has drawn a lot of attention for a number of applications. For single crystal devices, using strain technique is a promising approach. Although using the contact etching stop layer (CESL) to couple strain into the channel is a mature technique, the SiN intrinsic-stress impact on the SMT technique and its mechanism still need clarifications. As the poly-Si pitch shrinks in high-density static random access memory circuits, the thickness of the capping layer that we can use is reduced, meaning that the mobility enhancement would be lowered with each successive generation. Therefore, choosing the appropriate material and taking advantage of the limits to the thickness of the capping layer to create the highest mobility are important issues.

On the other hand, because the grain boundaries in poly-Si TFTs have a profound influence on device characteristics and degrade carrier transport, developing promising techniques to reduce the trap density is important. Besides the involvement of strain, using a plasma deposited SiN layer as a high concentration diffusion source of atomic hydrogen is a promising approach for improving the performance of poly-Si TFTs [1.56]. These hydrogen and nitrogen radicals originating from SiN layer are effective to improve the mobility, threshold voltage, and leakage current. However, the effect of the flow rate of different reactant gases on the deposition of the SiN layer for passivation of poly-Si TFTs has yet to be systematically investigated.

Moreover, post annealing decreases the benefits of using hydrogen radicals by plasma treatment to passivate these defects, indicating that there are limits to thermal cycling after the hydrogenation process. The effects of the post annealing temperature on the poly-Si TFT performance have also been studied experimentally [1.57]. However, the effects of the hydrogen instability induced by post annealing on the passivation of tail states, the passivation of deep states, and the additional defect generation in poly-Si TFTs must be clarified.

Furthermore, the stress originating from SiN not only affects the carrier transportation, but also the crystallization. Thus, besides the hydrogen induced retardation of the crystallization, the influence of stress originating from proximity layer on device performance is very important.

1.3 Organization of the Dissertation

The organization of the thesis is separated into six chapters and organized as follows.

In chapter 1, we presented the introduction of strain techniques related to single-crystal MOSFETs and the trap reduction associated to poly-Si TFTs.

In the chapter 2, we explore a variety of SiN as the capping layer to execute SMT. Based on the material and electrical analysis, a reasonable mechanism connecting the property of SiN to the improvement of mobility would be proposed. In addition to the enhancement of performance, the impacts of SMT on the interface state, gate leakage, hot carrier stressing, and flicker noise were thoroughly studied.

In the chapter 3, this chapter presented the effect of the flow rate of different reactant gases on the deposition of the SiN layer for passivation of poly-Si. Poly-Si TFTs capped with different SiN passivation layers show differences in their performance improvements, since different mechanisms are involved. Additionally, a mechanism to explain the double hump phenomenon induced by incomplete trap passivation was proposed. Also, the immunity to positive gate bias stress, negative gate bias stress, and hot carrier stressing was reviewed in detail.

In the chapter 4, this chapter focused on the passivation efficiency of hydrogen by hydrogen-containing nitride, based on the comparison of different thicknesses of SiN or inserted TEOS oxide. Also, the impacts of hydrogen release on the threshold

voltage, mobility, and leakage were studied. Moreover, the degradation of hot carrier stressing, NBTI, and PBTI for all samples were systematically investigated. The hydrogen release make the poly-Si TFTs exhibit different characteristics of reliability, and two possible mechanisms were proposed to explain the increased pre-existing defects.

In the chapter 5, the impacts of the SiN proximity layer on the poly-Si TFT crystallized by SPC or MILC would be clarified. As a result, SPC exhibits the strong dependence on the stress, the proximity layer, and the crystallization temperature. For MILC, the SiN proximity layer not only retards the MILC growth rate, but also degrades the electrical characteristics. Three possible mechanisms can be used to explain the dependence of MILC on the proximity layer.

In the chapter 6, the results are summarized and organized. Future works will be presented based on the result of the thesis..

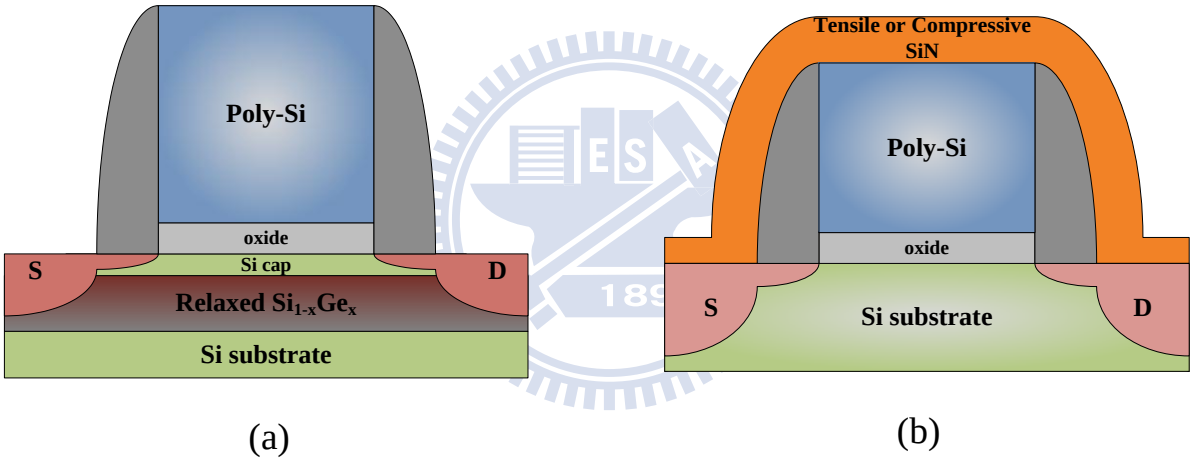
	2010	2011	2012	2013	2014	2015	2016	2017
Mobility enhancement factor due to strain								
Bulk/UTB FD/MG	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
Effective Ballistic Enhancement Factor								
Bulk/UTB FD/MG	1	1	1	1.03	1.12	1.19	1.26	1.34

Manufacturable solution exist, and are being optimized

Manufacturable soultions are known

Manufacturable solutions are NOT known

Fig. 1.1 2010 ITRS Process integration Devices and structures Logic potential solution



(a) (b)

Fig. 1.2 (a) Si capped on SiGe substrate can possess biaxial strain property. (b) Contact etch stop layer induce uni-axial stain.

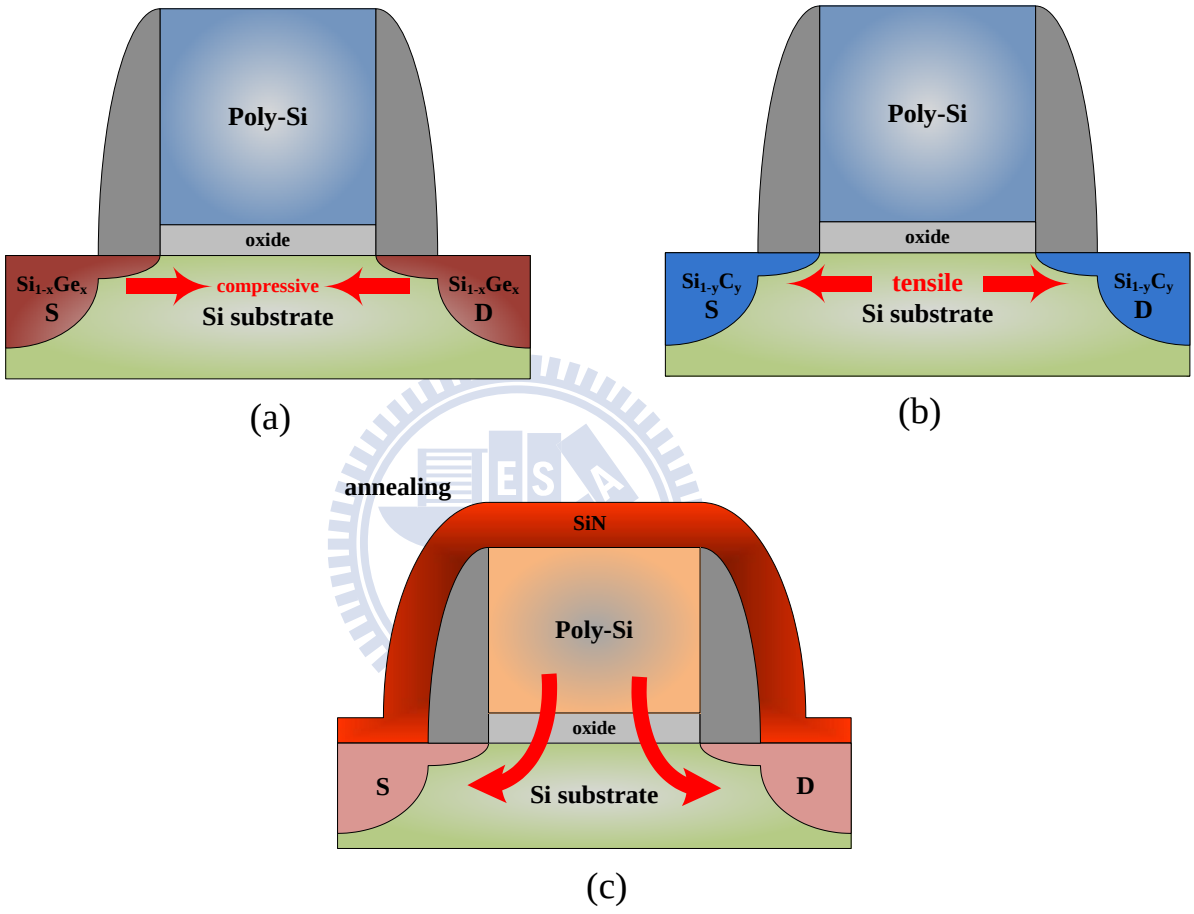


Fig. 1.3 (a) SiGe S/D possessed larger lattice constant induces compressive uni-axial strain laterally into the channel (b) SiC S/D possessed smaller lattice constant induces tensile uni-axial strain laterally into the channel. (c) The poly gate thermal volume expansion induces strain memorization for SMT application.

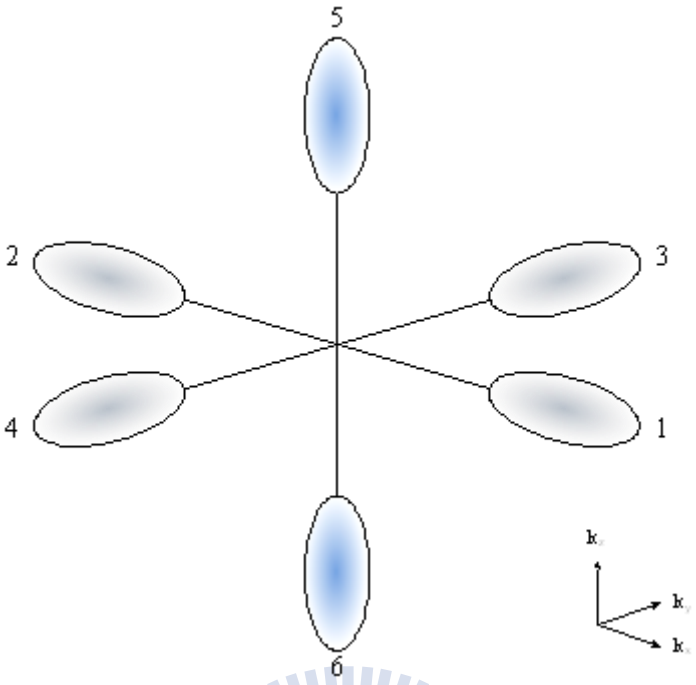


Fig. 1.4 Silicon without strain coupling possesses six- fold degenerate valley.

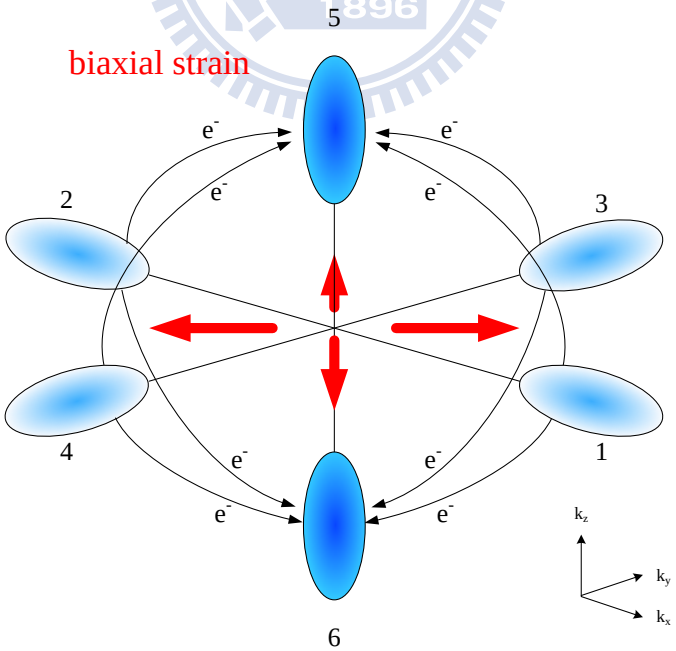


Fig. 1.5 With biaxial strain coupling, the carrier would redistribute into Δ_2 valley.

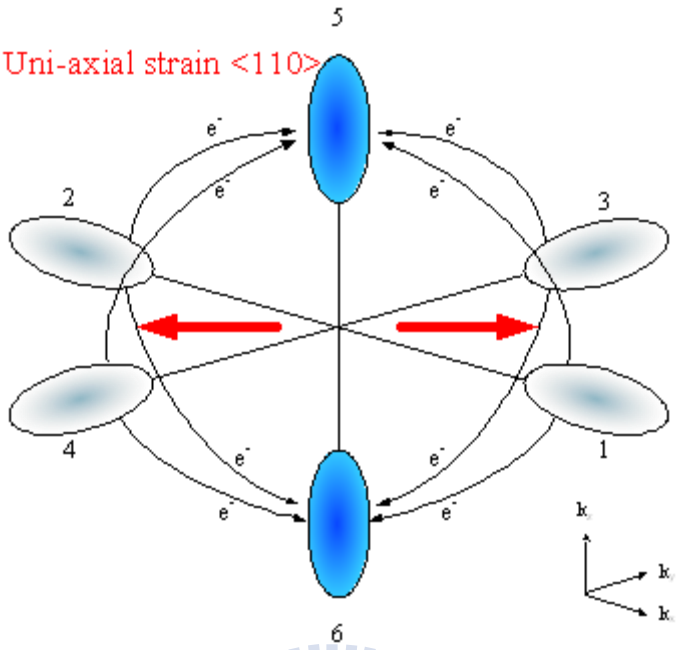


Fig. 1.6 With <110> uni-axial strain coupling , the carrier would redistribute into Δ_2 valley.

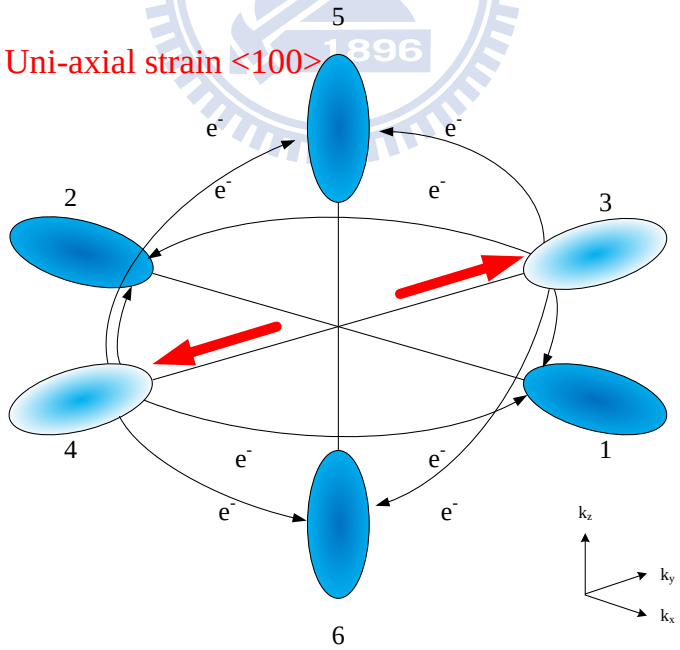


Fig. 1.7 With <100> uni-axial strain coupling, the E-k relation would transfer into an anisotropic occupation of four fold valley

Chapter 2

Stress of SiN and Stress Memorization in Devices.

2.1 Introduction

Channel-strain engineering is one of the most effective remedies to boost the drive current in scaled devices [2.1]. Using biaxial strain, it introduces a relaxed SiGe buffer layer using a complex process with the Ge out-diffusion issue [2.2]- [2.3]. For uniaxial strain, including SiGe source/drain, [2.4] research has invented a contact etch stop layer and stress-memorization technique (SMT) [2.5]-[2.6]. Among these techniques, SMT is simpler to fabricate, compatible with conventional processes, and has the potential to combine other strain-technique advantages, owing to its memorization technique.

In recent approaches, several investigations have focused on optimization of the SMT technique by manipulating the geometrical structure and material features to obtain higher mobility. For example, SiN_x offers a higher Young's modulus than SiO_x. Hence, using SiN_x as spacer or capping layer could confine an expanded poly-Si gate firmly and sufficiently suppress lateral expansion to attain higher tensile strain coupling. The phenomenon of material expansion also plays a critical role in the SMT process. For poly-Si implantation, the deeper the *Rp* projection range using the same dosage, the more obvious the stress memorization [2.7], [2.8]. With a heavier implant source and the amount of dose aid, the poly-gate condition would be more amorphized [2.9]. More effective recrystallization would thus occur, and volume swelling could be enhanced significantly.

However, the SiN intrinsic-stress impact on the SMT technique and its mechanism still need clarifications. As the poly-Si pitch shrinks in high-density static random access memory circuits, the thickness of the capping layer that we can use is reduced, meaning that the mobility enhancement would be lowered with each successive generation [2.10]. Therefore, choosing the appropriate material and taking advantage of the limits to the thickness of the capping layer to create the highest mobility are important issues.

In this chapter, we explore a variety of SiN as the capping layer to execute SMT. We find that the material with the greatest potential is a compressive SiN layer rather than the tensile SiN layer that is typical of the conventional process for CESL and

SMT. Among the intrinsic characteristics of the SiN layer, the key factor is the amount of stress shift rather than the initial or final stress. The corresponding mechanism is also clarified. SMT would degrade gate leakage, but its mechanism did not clarify clearly [2.11]. To our knowledge, a few research reports the impact of initial compressive nitride on gate leakage and interface-state. This chapter also investigates interface-state passivation and the connection between gate-leakage and intrinsic stress characteristics in the SMT process. A previous work adopted Fourier-transform-infrared-spectroscopy (FTIR) for evaluating the hydrogen concentration in different kinds of nitride for SMT application. However, Ortolland presented hydrogen as an interface-state creator [2.12]. In contrast, we found that hydrogen passivation improved the interface-state. Besides performance advantage, the SMT with compressive nitride is superior for interface condition, gate-leakage concern, hot carrier stressing, and flicker noise.

2.2 Experiment

2.2.1 Material Analysis

X-ray photoelectron spectroscopy (XPS) was employed to investigate the SiN_x films as 150nm by PECVD (Plasma Enhanced chemical vapor deposition) with different deposition condition. The detail of deposition condition split was list as table 1 with RF power 100W in 137Pa. For investigating the impact of thermal annealing, all conditions execute nitrogen annealing for 30s at 900℃. The N/Si atomic ratios was obtained from the area of the N 1s peaks and that of the SiN parts of the Si 2p peaks as table 1. We found that N/Si would be higher with the higher diluent gas N_2 in the deposition process. For increasing SiH_4 flux, the N/Si would increase first, and then the ratio would decrease to Si rich SiN_x as Fig. 2-1. After RTA process, SiH_4 high and N_2 high would release nitrogen in the high temperature, and the N/Si atomic ratios would decrease consequently. For the density analysis, all samples possess comparable etching rate, except Si high SiN_x samples cannot be etch by phosphoric acid. As sketched in Fig. 2-2, the chemical shifted component was analyzed by XPS. Starting with the a-Si network in which each Si is connected by four other Si atoms as nearest neighbors. As nitrogen couple into the network, an increasing number of homopolar Si-Si bonds are replaced by heteropolar Si-N bonds, meaning that the charge would transfer from Si to the more electronegative N leaves a positive charge

on the Si atom. Therefore, the Si core level would shift from 99.6eV in a-Si toward the higher binding energy, such as 102.8 as $SiN_{1.5}$ [2.13]. By modulating the diluent gas N_2, composition of the peaks in the as-deposited films do not change substantially. However, after the RTA process, the peak of lower binding energy Si 2p formed, meaning that the lower x of SiN_x would form in the process with nitrogen loss.

Moreover, Fourier transform infrared spectrometer (FTIR) was adopted for investigating differences among all conditions as Fig. 2-3 and Fig. 2-4. From the area of Si-N bonding comparison, no significant difference can be detected by FTIR. After annealing, Si-N detected by FTIR would increase, and the FWHM (full width at half maximum) would get higher for all N_2 modulation samples. It is noted that the FWHM of the band reflect the overall disorder of the network topology [2.14]. Therefore, the higher FWHM reveals that the range of bond angle distortion and the absorption band would be broader. However, the FWHM of SiH_4 sample would decrease after annealing, and it is consistent with a previous report [2.14], indicating that a thermally activated reordering of the network for the nitrogen rich composition. Additionally, modulation of diluent gas makes impact on the Si-H and N-H bonding as Fig. 2-5 and Fig. 2-6. The higher the diluents gas, the lower Si-H bonding as-deposited possesses. Besides, the film deposited by lower diluent gas would break higher quantity of Si-H during annealing. However, the N-H bonding doesn't reveal a clear dependence on the flux of diluents gas. Additionally, the SiH_4 high as deposited has the highest Si-H band among all samples and largest broken Si-H after annealing process.

Furthermore, the characteristics of intrinsic stress are very important for device application, such as CESL and SMT process [2.15]- [2.16]. By modulating diluent gas and RF power in 137Pa, different SiN_x samples deposited on 4-inch wafer were investigated. The stress measurement was performed on a Tencor FLX-2320 system. This system evaluates the stress by measuring the change in curvature of the silicon substrate before and after process. The lower RF power performs in the deposition process, the higher tensile quantity the film possesses as demonstrated in Fig. 2-7. Besides, it is quite obvious that deposition with higher diluent gas can create higher tensile film. It is well know that the quantity of hydrogen in nitride makes influence on the intrinsic stress properties [2.17]-[2.18]. We found that nitride with lower hydrogen quantity could become more tensile in our experiment. Recently, both the intrinsic stress after annealing and intrinsic stress shift are extremely important in the

SMT fabrication process as Fig. 2-8. We observed that all samples become more tensile after RTA process. Nitride Deposited with lower RF power can achieve higher stress after RTA 900℃ for 30s；However, the film deposited by lower diluent gas with lower initial intrinsic stress achieves higher annealed stress shift as Fig. 8. In other word, the lower diluents gas N_2 in the deposition process labeled as N_2 low can achieve higher stress shift potential after RTA as Fig.2-9. The H component in nitride film may play a significant role in determining the stress shift quantity, since the film with higher stress shift always possesses higher H quantity in our experiment. Finally, the impact of implantation and multi-deposition on the stress process are investigated as Fig. 2-10 and Fig. 2-11. With the RF power as 100W in 137Pa the N_2 low and SiH_4 high were deposited by PECVD on highly doping 4-inch wafer. Multi-deposition samples with deposition of 500Å SiN and cooling process executed three times are fabricated to compare to Once-deposition as 1500Å. For investigating implant impact, some of Once-deposition samples would also execute implantation treatment with As^+(80keV with 1E15/cm^2), which labeled as Implant-treatment. As a previous report [2.19], if the deposition process divides into several times, the final intrinsic stress would get higher, due to relaxation effect of the nitride. However, the Multi-deposition does not present a high intrinsic stress compared to Once-deposition in this experiment. Multiple depositions would decrease initial stress, annealed stress, and stress shift quantity for N_2 low comparison；However, the stress characteristics of SiH_4 high possess slight difference. For the implantation treatment investigation, the stress as deposited film would decrease, whether the initial stress is tensile or not. It's consistent with the previous report, which proposed that implantation is a promising method to minimize the impact of tensile SiN on PMOS performance. Additionally, with the implantation treatment, the potential of stress shift of SiH_4 could be enhanced.

2.2.2 Device Fabrication

After RCA cleaning process, 3nm gate oxide was thermally grown on 6-in wafers in a vertical furnace. Undoped poly-Si gate (2000 Å) was deposited, and As^+(50keV with 5E15/cm^2) was adopted to enable the maximum Poly Amorphorization Implantation (PAI) effect. After extension and spacer formation, four different silicon nitride (SiN) capping layers (1500 Å) were deposited by PECVD, modulating the

flow-rate of N_2 or SiH_4 to confine the poly-Si gates. The power was set at 100W, pressure was 137 Pa, and temperature was 300℃. To obtain a different intrinsic stress of SiN, the flow-rates of the N_2 were set to 50, 100, and 1000 sccm with NH_3 = 6 sccm and SiH_4 = 50 sccm across all three. The samples were labeled N_2-low, N_2-med, and N_2-high, respectively. In addition, a SiH_4-high sample in which the flow-rate of SiH_4 was 100 sccm, but the NH_3 and N_2 were 6 and 50 sccm, respectively, was prepared for comparison. For investigating the impact of poly grain size on SMT, poly gate would deposit in different temperature effect as 550℃, 580℃, and 600℃, respectively. Later, after PAI treatment and spacer formation, the samples with silicon gate deposited by different temperature would cap by N_2-med nitride. After RTA at 900℃ for 30s, the source/drain and poly-Si gate were activated and the channel strain induces simultaneously. Subsequently the capping layers were removed, leaving residual strain in the channel, and standard MOSFET fabricating steps were followed to complete the final devices with channel lengths of 0.4μm and 0.35μm.

2.3 Results and Discussions

2.3.1 Device Performance

Figure 2-12 illustrates the value of transconductance divided by capacitance, to make the strain contribution to mobility clearer. We found that the N_2-low split shows the highest enhancement, 27%, while the N_2-high split exhibits the lowest enhancement, 10%. In addition, the SiH_4-high sample also shows a 23% improvement. Figure 2-13 demonstrates the stress characteristics of all capping layers on 6-inch wafer for comparison as initial-stress, final-stress, and stress shifts (defined as final-stress – initial-stress). The different SiN splits have a comparable etching rate in hot H_3PO_4 solution, and thus the films have analogous density.

This investigation was focused on a compressive SiN layer rather than TEOS oxide or tensile SiN layer was used to execute SMT. After the annealing process, all SiN splits became more tensile. As shown in Figure 2-12, the compressive SiN, N_2-low, that we used offered the greatest enhancement of mobility, instead of the highest tensile capping layer as is conventionally used. This result is contradictory to the usual practice of optimizing the tensile capping layer to enhance NMOS mobility.

Based on the experimental results, we postulate a model to clarify the mechanism.

Previous research shows that we should use a material with a higher Young's Modulus as a spacer to confine the expanded poly gate, and use the PAI technique to make the grain recrystallize effectively. In this experiment, we thoroughly investigate the capping layer and postulate another mechanism for enhancing mobility. N_2-high and N_2-low possesses Young's modulus as 166.562Gpa and 149.386Gpa, respectively. In conventional SMT as shown in Figure 2-14, the poly-Si gate in the RTA process expands its volume by an abrupt increase in temperature, and tends to be more compressive due to confinement of volume by the spacer and capping layer wrapping. Subsequently, the poly Si gate expands its volume into the channel region during annealing process. The channel eventually becomes vertically compressive and subsequently tends to be tensile. However, N_2-high doesn't show a higher mobility than that of N_2- low one, which is not consistent when Young's modulus considered solely. Our experiment results show that the capping layer also plays an obvious role, in addition to the poly-Si thermal expansion condition. Since N_2-low and SiH_4-high splits possessing higher stress shift have higher mobility, the benefit of mobility enhancement is the split with the highest stress shift instead of the original or final, most tensile, capping layer. It is found that the film with the highest stress shift tends to compress the channel more during the annealing process as shown in Figure 2-15. This is consistent to the model that the larger the shift of stress, the higher the vertical stress shift [2-5]. The highest stress shift in vertically results in the largest compressive strain gain vertically, making the channel become more tensile horizontally, and enhancing the electron mobility in return. Consequently, not only the volume confinement during annealing as traditional viewpoint, but also the intrinsic stress shift of capping layer make influence on the SMT technique.

The mechanisms we explore, along with the results we have obtained, indicate the existence of a greater variety of choice for the optimization of SMT. Since the compressive SiN layer we use possesses the greatest stress shift potential, the choice of materials for optimization is now broader. Figure 2-16 shows the I_{DS}-V_{GS} characteristics. All devices display a similar subthreshold swing in the V_g=0.05V condition, which implies an identical interface at the oxide/substrate for capping layer optimization.

Figure 2-17 shows the measured charge-pumping current of different samples. All samples made using the SMT process show a more reduced interface-state than the control sample. To investigate the interface-state passivation as shown in Figure

2-17, we measured initial and annealed samples using FTIR (Figure 2-5 and 2-6). The initial FTIR spectrum (Fig. 2-5) shows that the SiH4-high sample exhibits a high Si–H bond, while the N2-low, -med, and -high samples show a high N–H bond. The higher the N2 flow-rate during deposition, the lower the amount of H coupled into the capping layer. The initial quantity of hydrogen in the deposited capping layer plays an important role for passivating the interface-state;[2-20]-[2-21] However, Ortolland proposed that hydrogen is an interface-state creator for SMT investigation [2-12]. Stathis investigated the impact of hydrogen diffusion on different oxide condition and proposed that hydrogen would either induce interface-state or passivate the interface-state, depending on the initial interface property. At oxide interface, there is a single variety of silicon dangling bond defect, the Pb center. Pb centers are generated by Ho in a sample with initial low Pb density and reduced (passivated) if the initial Pb density is high [2-22]. We investigated the impact of hydrogen on silicon dioxide rather than the impact of hydrogen on oxynitride and high-k materials as Ortolland's work [2-12]. As a result, the impact of hydrogen diffusion in SMT on interface-state condition depends on the initial oxide condition. Figure 2-6, which shows decreased concentrations of Si–H and N–H compared to initial composition, reveals that the annealing process had significant impact on the H-component. Higher N_2 flow also affects the quantity of hydrogen release during annealing. We believe that the Si–H and N–H break release hydrogen into the channel during the annealing process. The released hydrogen passivates the dangling bonds in the annealing process, in addition to passivation by hydrogen coupling during the deposition process. For the standard SMT process, the device with a capping layer undergoes high temperature annealing during strain memorization, and the released hydrogen of this capping layer further passivates the interface-state. Consequently, the amount of passivated dangling bonds depends not only on the initial capping layer component but also on the amount of hydrogen released during the annealing process.

Besides, we found that the intrinsic stress shift of nitride also has strong dependence on the ability of passivating dangling bonds as Fig. 2-18. The film with higher hydrogen released, which always possesses higher intrinsic stress shift, could further passivate the interface states. Thus, the passivation ability is partly responsible for clarifying the connection between the intrinsic stress shift and mobility gain.

Beside the mechanism of different capping layer, the composition of poly gate also play a key role for determining the strain coupling based on different

recrystallization property, such as Poly Amorphorization Implantation (PAI) and dopant confinement layer (DCL). For both the poly depletion and SMT strain coupling concern, the MIPS (metal inserted poly silicon) structure with SMT application is the promising technique. Thus, we investigate the impact as different deposition temperature, include 550℃(amorphous Si), 580℃, and 600℃(poly Si). The lower deposition temperature could make higher gm/C_{inv}, which represent the improvement of mobility as Fig. 2-19. However, with the lower deposition temperature, the poly depletion would be more significant, and the threshold voltage would also become larger consequently. For further analyzing the mechanism, the charge pumping was adopted as Fig. 2-20. We observed that the interface state would be lower with lower silicon deposition for gate application, beside the different poly gate volume expansion of different silicon grain shape during annealing process. However, from a previous research as CESL, the author proposed that hydrogen diffusion through silicon gate possesses lowest diffusion speed, due to the dangling bond in grain boundary would trap hydrogen [2-20]-[2-21]. Thus, nitrogen would tend to diffuse through S/D and laterally diffusion into the channel region rather than diffusion through poly gate. However, we deduce that hydrogen diffusion path in poly gate act as an important role in SMT process beside diffusion through S/D junction from our result. We deduced that amorphous silicon would recrystallize into higher grain diameter compared to poly silicon in the high temperature as 680℃ for spacer formation. Thus, hydrogen possesses higher diffusion speed for larger silicon grain size of poly silicon [2-21]. Beside the thermal expansion properties of different silicon gate, the silicon gate deposited in lower temperature has better interface. Thus, we proposed that the amorphous silicon possesses higher potential for SMT process in MIPS.

The gate-leakage was investigated in Fig. 2-21. Devices fabricated using SMT show a higher leakage in low electric fields than control devices. This increased leakage is strongly related to the bulk oxide traps, and oxide-trap-assisted Poole-Frenkel conduction in low electric fields [2-23]. Further, N_2-med and SiH_4-high show a higher leakage current than their counterparts, even exhibiting soft breakdown (SBD), owing to damaged oxide quality [2-24]-[2-25].The stress shift during annealing is proportional to the strain memorized in the channel [2-26]. To clarify the mechanism of leakage, stress before and after annealing was measured and is shown in Fig.2-22. The capping layers all become more tensile after the annealing process. It

is noted that the N_2-low split exhibits the highest stress-shift (stress of annealed minus initial stress). However, this high stress-shift does not cause oxide degradation. Hence, the amount of stress-shift, which is proportional to SMT coupling strain, is weakly dependent on the gate leakage, meaning that the memorized strain is not the dominant mechanism for generating bulk oxide trap. The annealed SiH_4-high sample has the greatest stress, followed by the N_2-med, which shows the same trend as the leakage characteristics shown in Fig. 2-21. Based on these observations, we believe that the stress of the capping layer after annealing rather than the memorized strain is the origin of the degradation of gate-oxide quality. As the capping layer is removed, capping layer stress is relaxed, but the damaged caused by the stress remains. Thus, the stress after annealing, rather than the initial stress, appears to be the dominant factor in the degradation of gate-oxide.

The N_2-low sample shows an initial compressive stress which then changes into a lower tensile stress, giving lower gate leakage than the initial tensile sample. We thus infer that the initial compressive capping layer (N_2-low for our case) possesses a greater potential than the initial tensile layer for executing SMT for low gate-leakage.

2.3.2 Hot Carrier Stress

Recently, the hot carrier effect for core device alleviates gradually as the operation voltage scaling low；However, the I/O device with higher operation voltage still possesses hot carrier concern. The impact of SMT on the characteristic of hot carrier would be specified as follow. With the strain coupling by SMT process, the substrate current would be enhanced as Fig. 2-23. The hot carrier characteristics would be reviewed. Devices with W/L=10/0.35μm were stressed at $V_{DS} = 3.5V$ and V_G at maximum substrate current. Fig. 2-24 demonstrates threshold voltage shift ($\Delta V_{th} = V_{th}(t) - V_{th}(0)$) as a function of time for different SiN_x conditions. The N_2-med and SiH_4 high reveal the worst degradation in terms of the largest ΔV_{th}, meaning that the damaged oxide quality induced by stress of capping layer is the dominant mechanism rather than the strain couping. Charge pumping current as initial and after 5000 sec hot carrier stress among all samples was demonstrated in Fig. 2-25. The film with better interface condition still could remain its superiority compared to counterparts. Fig. 2-26 demonstrates charge pumping current shift ($\Delta I_{cp} = I_{cp}(t) - I_{cp}(0)$) as a function of time for different SiN_x conditions. We observe that N_2-low,

N_2-med, and SiH_4 high, which possess lower dangling bond as initial, have higher charge pumping current shift than control and N_2 high after hot carrier stress. We believe that the higher substrate current and higher initial Si-H are responsible for the difference of charge pumping current shift. The degradations of transconductance and interface state induced by hot carrier stress as a function of time was sketched respectively as Fig. 2-27 and 2-28, and the device with higher strain coupling would remain its superiority after the hot carrier stress test. From the investigation of charge pumping current and transconductance, we found that N_2 med and SiH_4 high possessed terrible interface state and higher electron trapped in the oxide would remain its transconductance superiority due to the strain coupling.

2.3.3 Flicker Noise

In addition to DC influence, low frequency noise has become a critical concern in scaling down device sizes, and its properties are useful in identifying the gate dielectric properties of devices fabricated using SMT. In previous work, we demonstrated that initial compressive nitride yields better performance than initial tensile nitride. However, the dependence of the strain coupling using SMT on low frequency noise, and the effect of initial compressive and tensile nitride on low frequency noise, require clarification. For NMOS transistor analysis, the carrier number fluctuation theory is more appropriate than mobility fluctuation theory[2-27]-[2-31]. According to the carrier number fluctuation theory, the carriers would move in the defect in oxide, and move out from the defect for duration as Fig. 2-29. The duration of carrier traps in the defect depends on the distance from defects to Si/SiO_2 interface. From the time distribution of different trapping duration, the characteristics of noise would reveal $1/f^{\gamma}$ form. Thus, the quality of oxide and the distribution of traps are very important for defining the feature of flicker noise. Next, the impact of SMT on flicker noise would be specified as follow. The experimental setup for measuring low frequency flicker noise is shown in Fig. 2-30. The output of the pre-amplifier is connected to the dynamic signal analyzer, which performs sampling and fast Fourier transform of the incoming signal and calculates the density spectrum at the frequency of interest. The corresponding setups of measurement parameters, including the voltage for four terminals and the range of frequency, are controlled by a personal computer. The noise measurement in this experiment was performed in a range of 4Hz to 102400Hz. In table II, γ value of different device

were specified, which could reveal the distribution of defects in gate oxide. According to the number fluctuation model, the frequency component γ deviates from 1 when the trap density is not uniform in depth. $\gamma < 1$ is expected when the trap density is higher close to the gate oxide/channel interface than that in the interior of the gate oxide, and $\gamma > 1$ for the opposite case. However, the values of γ approach 1 for all samples, meaning that the SMT has no significant influence on trap distribution in the oxide.

Figure 2-31 shows the comparison of S_{VG} characteristics of different samples at 25Hz. For the carrier number fluctuation model including correlated mobility fluctuation[2-32], the noise is given by

$$S_{V_g} = \frac{q^2 kT\lambda N_t}{f^{\gamma} WLC_{ox}^2}(1 + \alpha\mu_o C_{ox}(V_g - V_{th}))^2$$

We observed that S_{Vg} is independent of V_g until $V_g - V_{th} = 0.47V$, indicating that the carrier number fluctuation model is the dominant mechanism in determining the characteristics of low frequency noise in weak inversion for all samples. On the other hand, S_{Vg} reveals a strong dependence on V_g and gradually increases as $V_g - V_{th} > 0.47V$. Thus, at this operating voltage, the correlated mobility fluctuation should also be taken into account, meaning that the effect of carriers scattering in the channel through the coulomb potential interaction by trapped carrier has become significant [2-32]-[2-33].

The characteristics of S_{Vg} at $V_g - V_{th} = 0.97V$ and $f = 25Hz$ were demonstrated as shown in Figure 2-32. We found that SiH_4-high and N_2-med possess higher S_{Vg} than the control, but N_2-low and N_2-high have improved S_{Vg}. Thus, we believe it is not the intrinsic effect of the SMT strain coupling mechanism that determines the low frequency noise behavior, but the extrinsic effect as Figure 2-33.

The N_2 med and SiH_4 high sample have higher oxide defect density, which was damaged by capping layer stress. It is consistent with gate leakage characteristics. Thus, the damaged oxide is responsible for the degraded flicker noise. The mechanism of improved oxide quality as N_2 low and N_2 high was demonstrated as Fig. 2-34. The band diagram describe the tunneling transitions, (a) tunneling into trap directly [2-34] or (b) using interface traps [2-35] as stepping stones from the silicon substrate into the trap. Thus, the passivated dangling bond by hydrogen in the SMT

process would decrease the possibility tunneling via interface state indirectly, and the flicker noise of the device would improve in the SMT process consequently.

2.4 Summary

In this chapter, the impact of power and diluents gas on the properties of nitride was clarified clearly. We find that the stress shift quantity rather than initial or final stress amount should be considered in stress memorization techniques. The initial compressive SiN capping layer has a higher stress shift potential than all tensile SiN capping layers split in SMT adoption, and the largest enhancement in mobility is achieved. This implies the traditional choice of capping layer should be widened to include the stress shift with the highest split. Besides, both the initial component of deposited capping layer, and the H released during annealing, affect the interface state passivation. The mechanism for the degraded gate-leakage and immunity of hot carrier stressing is ascribed to the stress induced during annealing. Based on the performance and gate-leakage, the initial compressive layer of SiN offers better performance than an initial tensile layer when using SMT. Additionally, the flicker noise would be degraded by stress induced during annealing, and would be alleviated by further passivated dangling bond. On the whole, the initial compressive layer performs better characteristic as performance, gate leakage, hot carrier, and flick noise.

	N_2 high	N_2 med	N_2 low	SiH_4 high	Si rich
SiH_4 (sccm)	50	50	50	100	500
NH_3 (sccm)	6	6	6	6	6
N_2 (sccm)	1000	100	50	100	100
Initial N/Si ratio	0.665	0.637	0.559	0.763	0.223
Anneal N/Si ratio	0.589	0.633	0.550	0.520	0.239
initial stress [Mpa]	477	148	-215	227	19
annealed stress [Mpa]	525	910	877	1165	523
initial Young's modulus [Gpa]	166.562	161.905	149.386	169.246	
annealed Young's modulus [Gpa]	162.498	169.989	177.433	195.28	
shrinkage	2%	4.80%	7.20%	4.50%	
initial hardness	15.063	19.147	19.651	14.662	
Annealed hardness	16.476	17.805	19.225	16.36	

Table 2.1 Properties of all nitride samples.

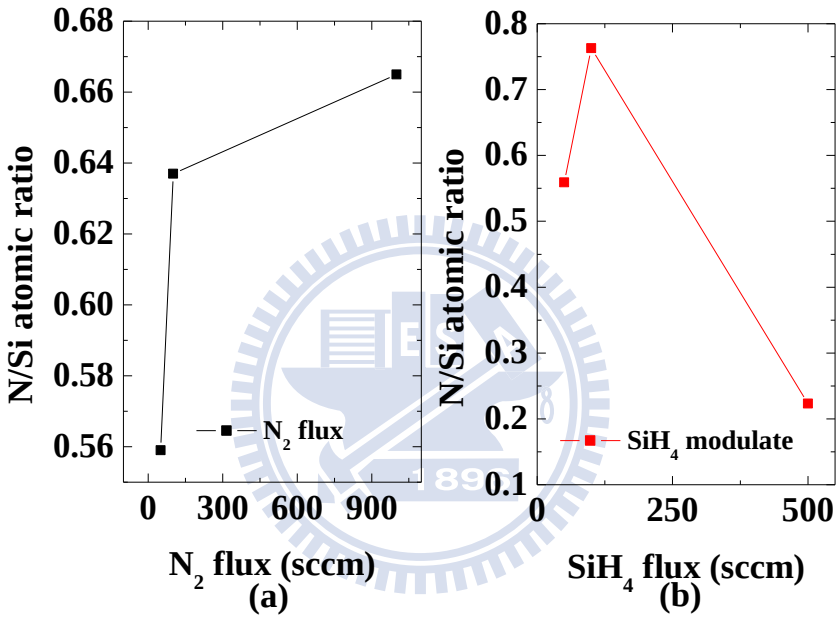


Fig. 2-1 (a) Influence of N_2 flux on N/Si atomic ratio. (b) Influence of SiH_4 flux on N/Si atomic ratio.

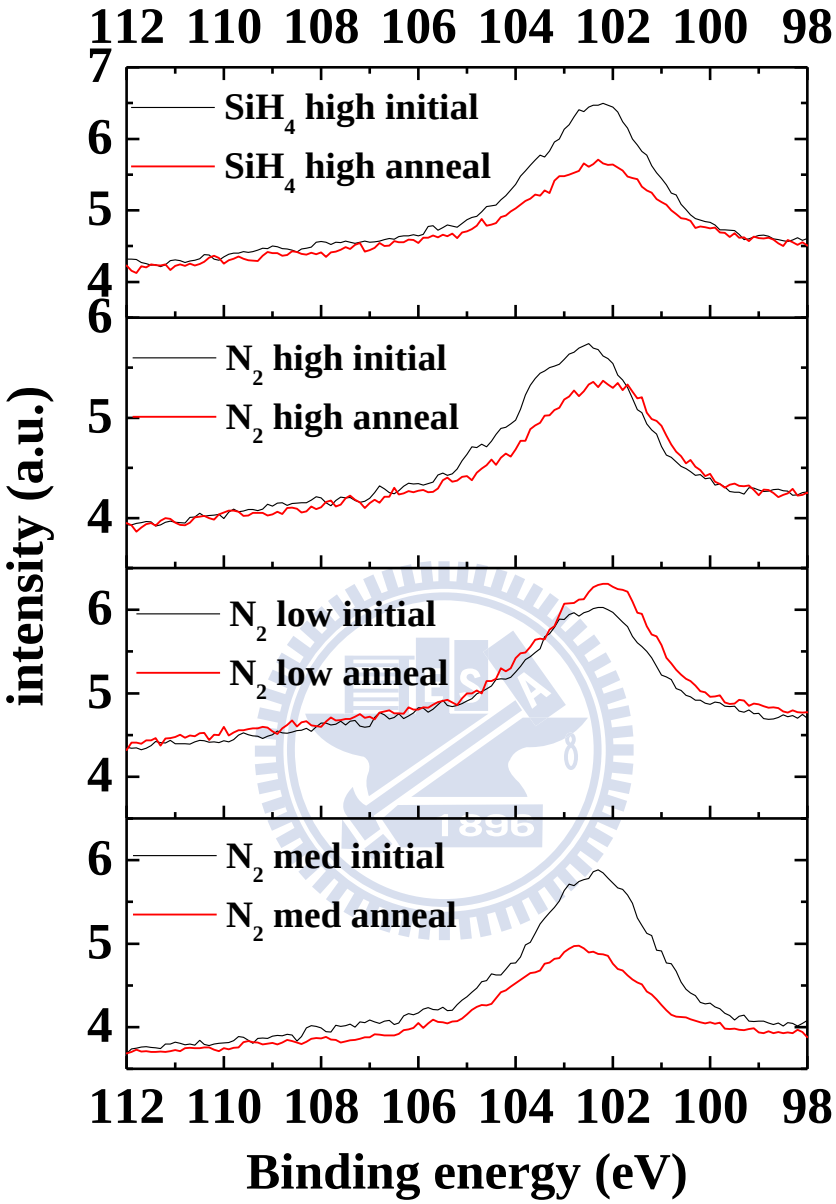


Fig. 2-2

Fig. 2.2 Characteristics of XPS for all initial and annealed SiN_x.

]

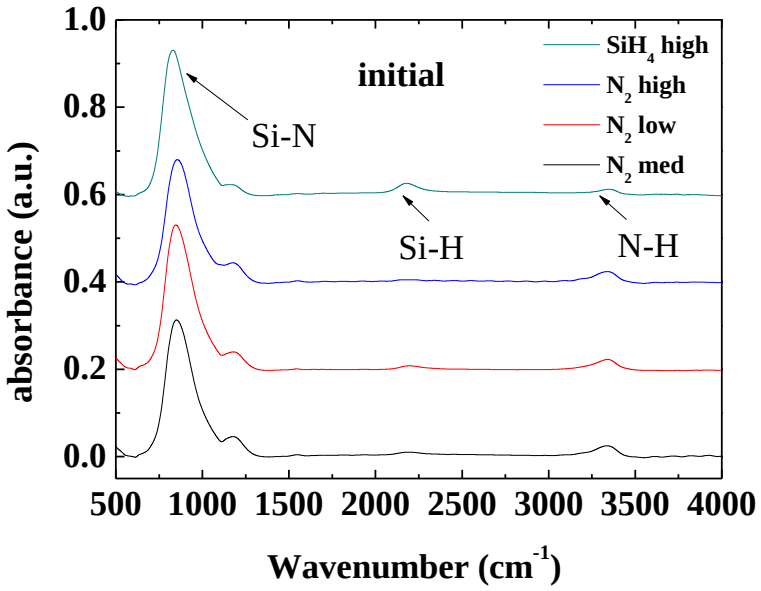


Fig. 2-3 The Si-N Characteristics of FTIR for all samples before annealing.

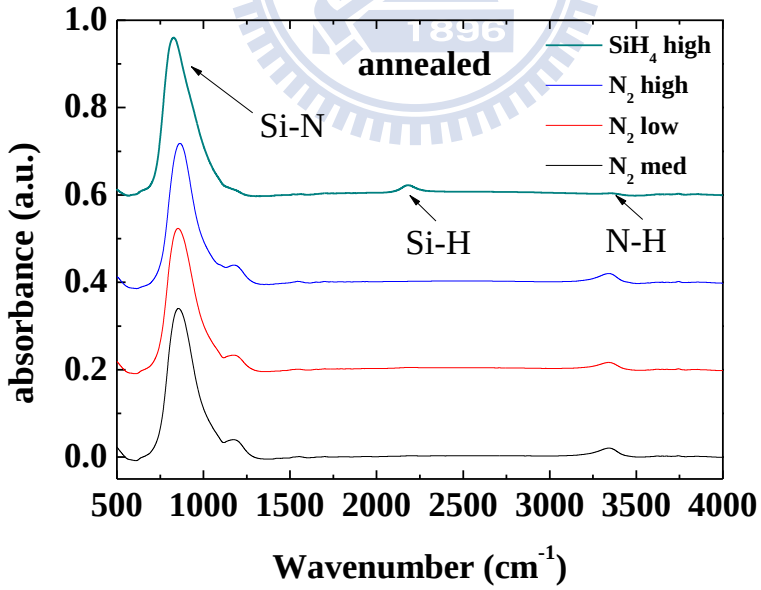


Fig.2-4 The Si-N Characteristics of FTIR for all samples after annealing.

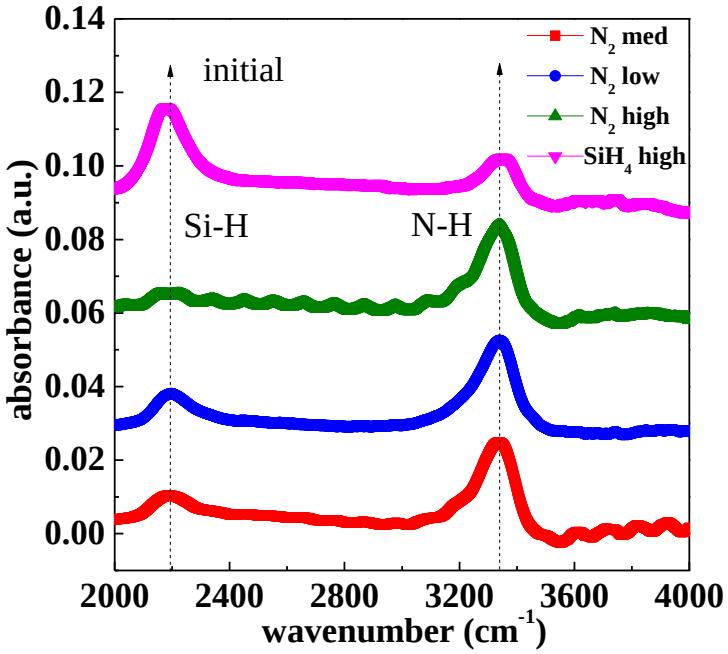


Fig. 2-5. Initial FTIR of N_2 rich, N_2 med, N_2 low, SiH_4 rich, and control sample for analyzing the H content.

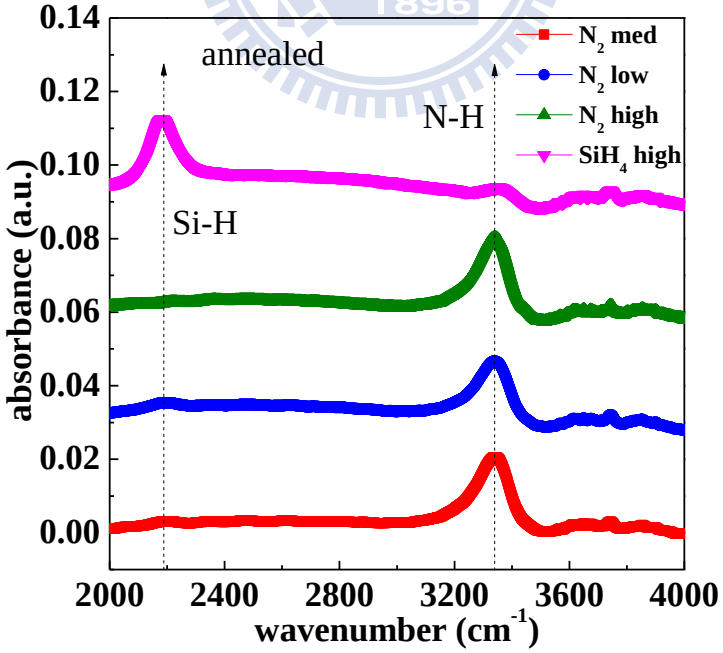


Fig. 2-6 Annealed FTIR of N_2 rich, N_2 med, N_2 low, SiH_4 rich, and control sample for analyzing the H content.

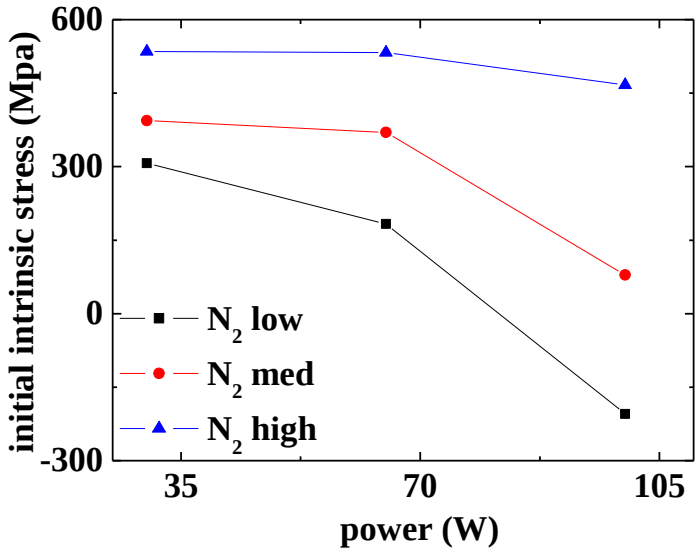


Fig. 2-7 The connection between initial intrinsic stress and power for N_2 low, N_2 med, and N_2 high.

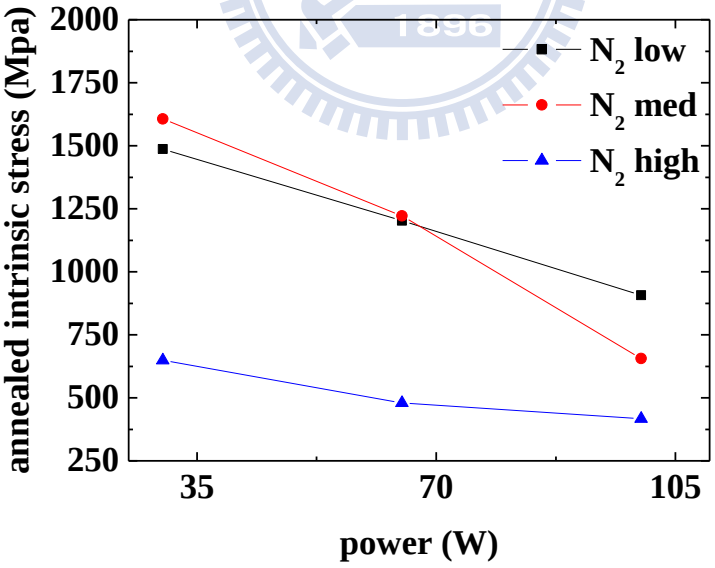


Fig. 2-8 The connection between intrinsic stress after annealing and power for N_2 low, N_2 med, and N_2 high

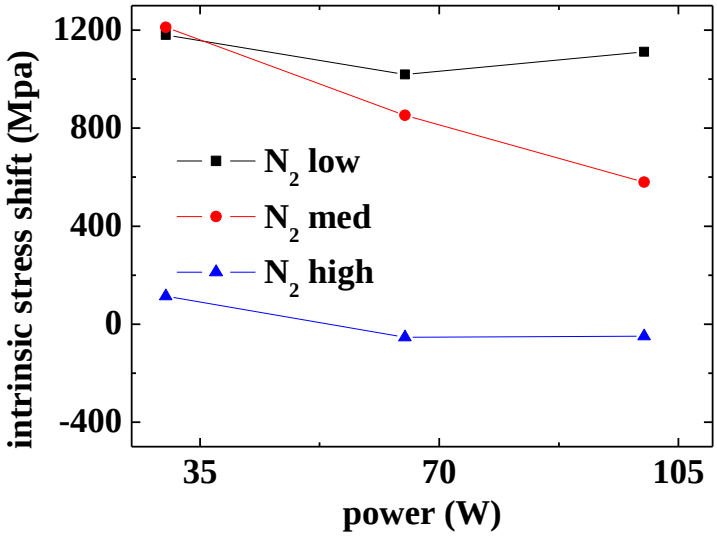


Fig. 2-9 The connection between intrinsic stress shift after annealing and power for N_2 low, N_2 med, and N_2 high

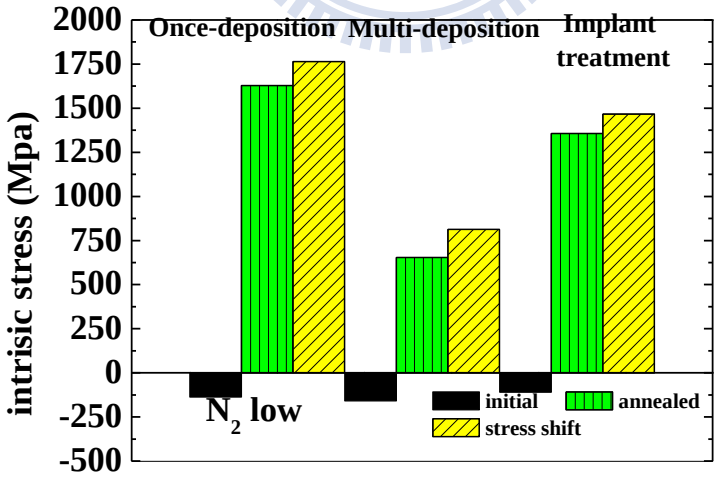


Fig. 2-10 Intrinsic stress characteristics as N_2 low for Once-deposition, Multi-deposition, and Implant treatment.

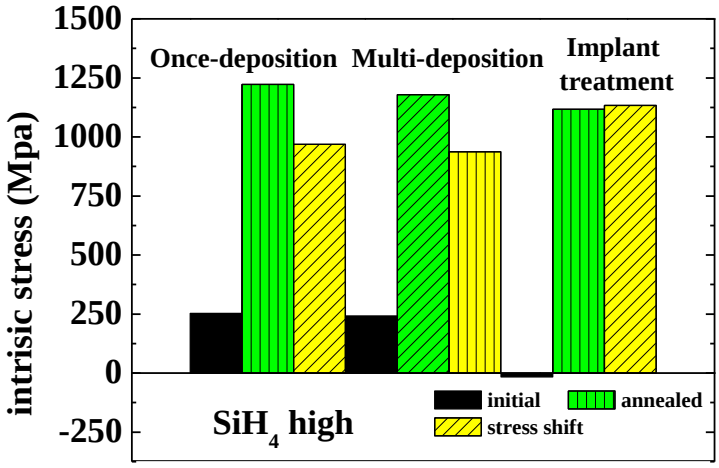


Fig. 2-11 Intrinsic stress characteristics as SiH_4 low for Once-deposition, Multi-deposition, and Implant treatment.

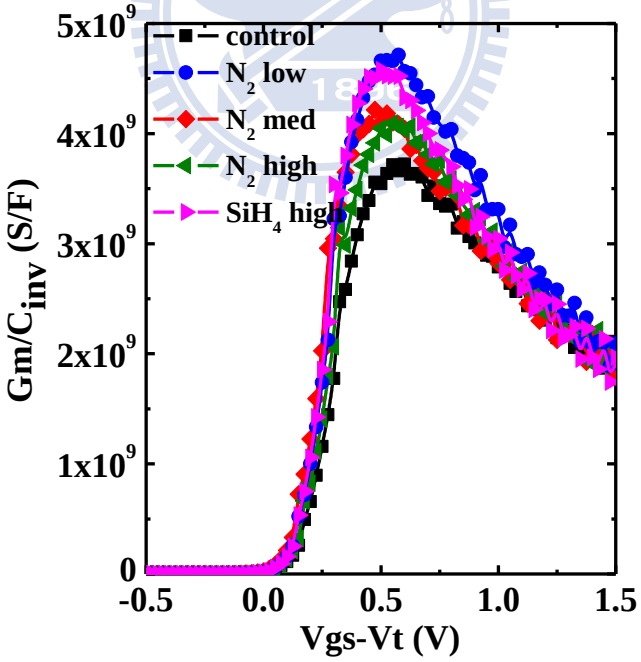


Fig. 2-12 Gm/C_{inv} for NMOSFET with different capping layer SiN (1500Å) in linear region with channel length equal to 0.4μm.

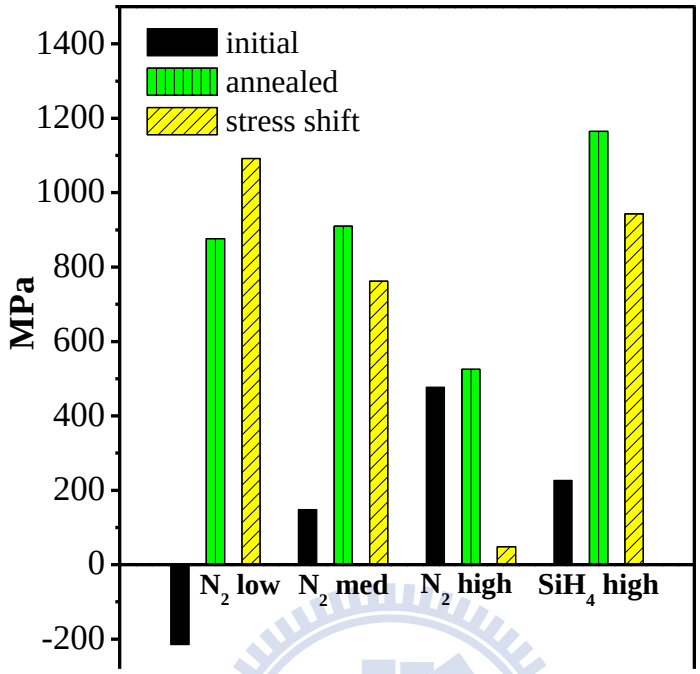


Fig. 2.-13 Initial strain, after annealing strain, and the strain shift by annealing process of different N_2 and SiH_4 flux.

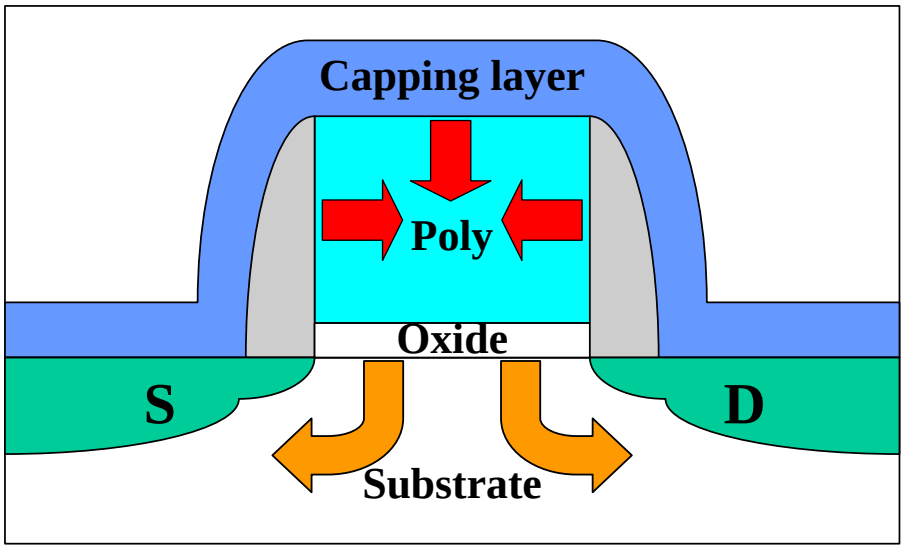


Fig. 2-14 The traditional thermal poly-Si expansion mechanism.

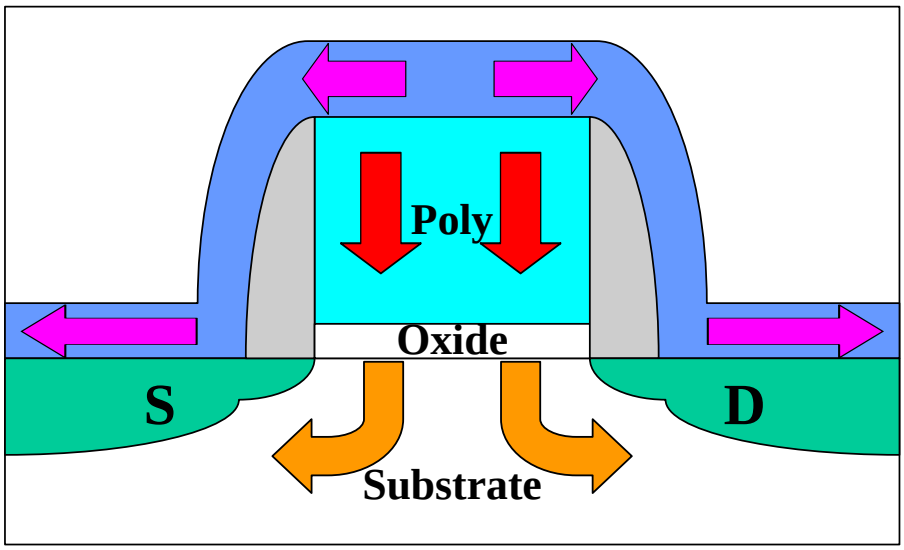


Fig. 2-15 The new model with the mechanically induced strain mechanism for the capping layer.

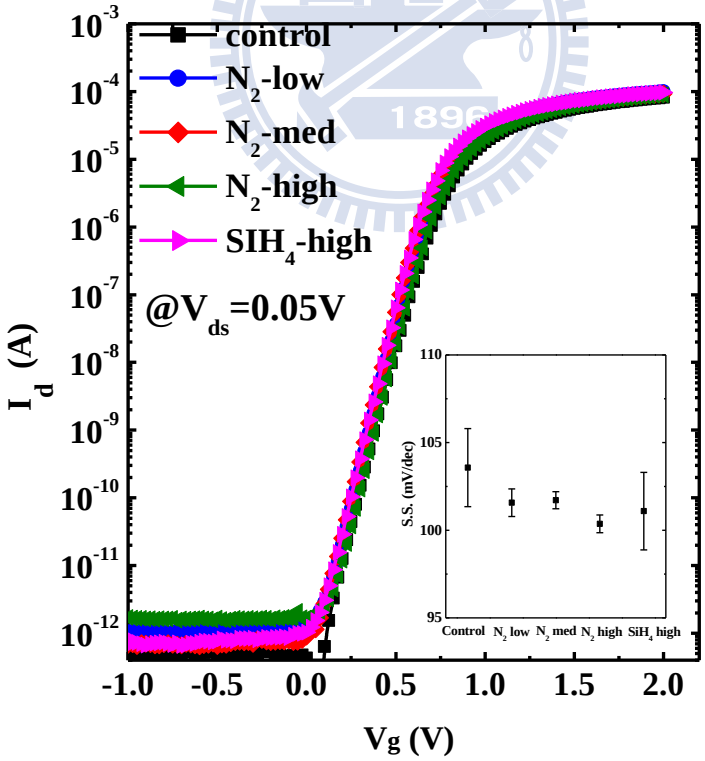


Fig. 2-16 I_d-V_g for different SiN at V_g=0.05V characteristics. The inset shows the subthreshold swing for different SiN.

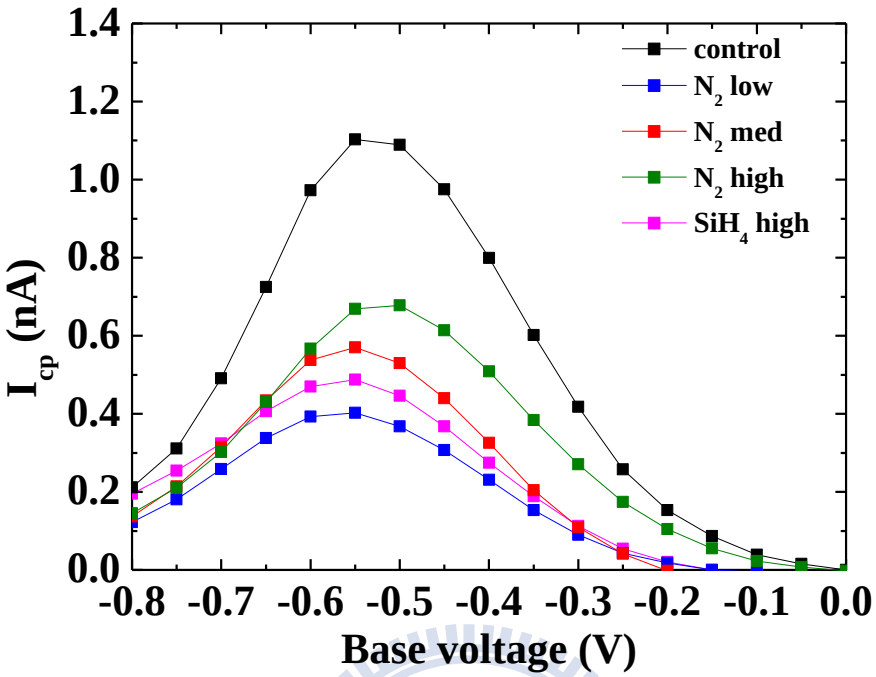


Fig. 2-17 Charge pumping analysis of all strain samples and the control sample with frequency of 2 MHz and voltage amplitude 1V.

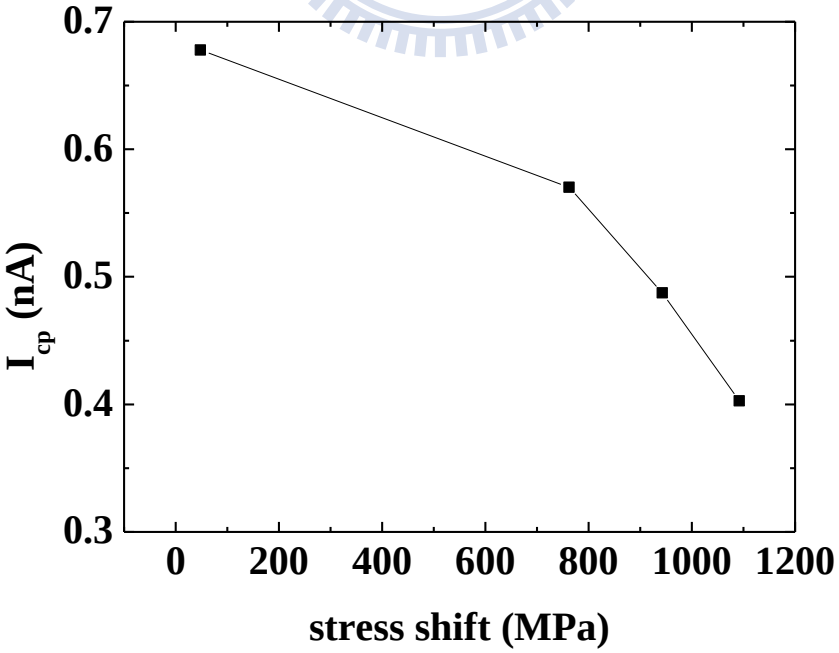


Fig. 2-18 The connection between intrinsic stress shift and charge pumping current.

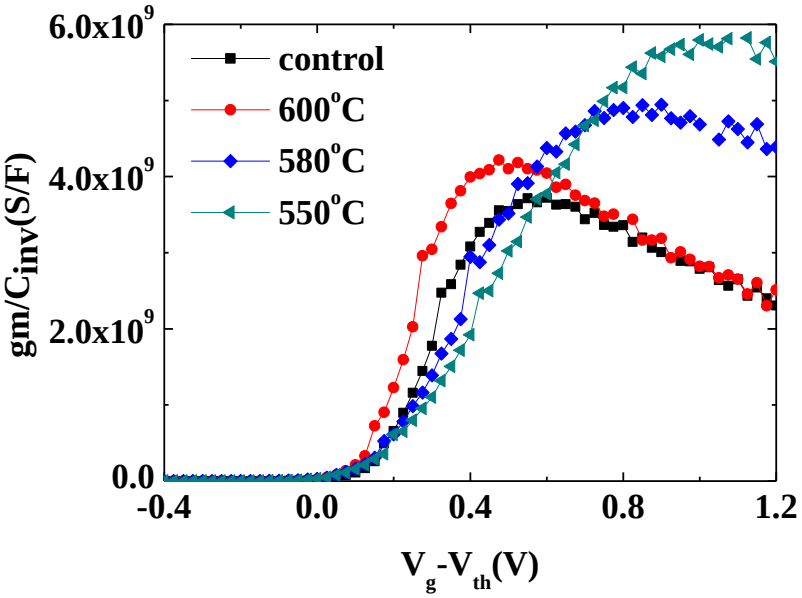


Fig. 2-19 Gm/C_{inv} for NMOSFET with silicon gate (2000Å) with different deposition temperature in linear region with channel length equal to 0.4μm.

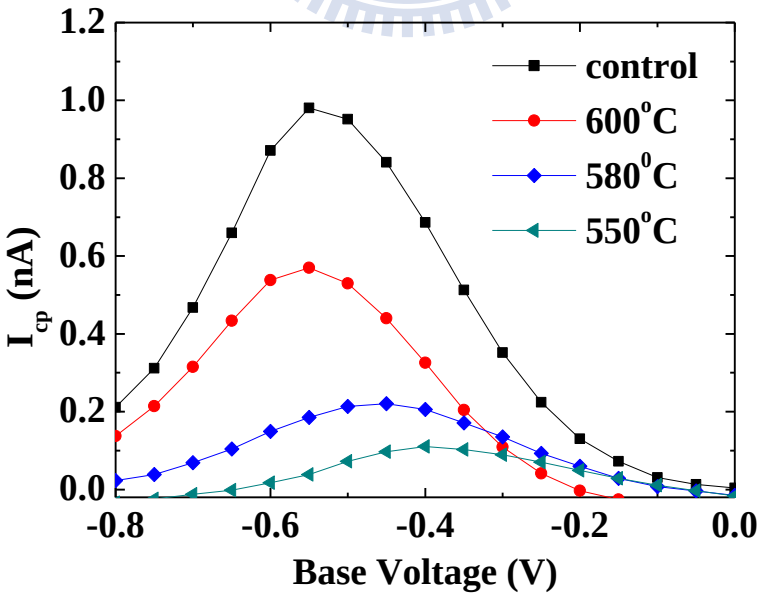


Fig. 2-20 Charge pumping analysis of strain samples by different deposition temperature with frequency of 2 MHz and voltage amplitude 1V.

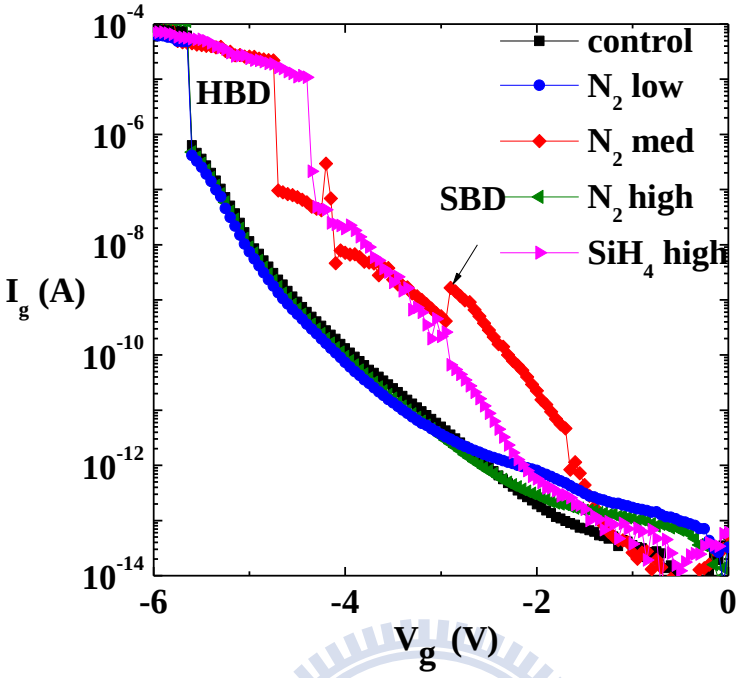


Fig. 2-21 Characteristics of gate leakage were investigated. All strain samples possess higher leakage, and SiH_4 and N_2 med sample display soft breakdown.

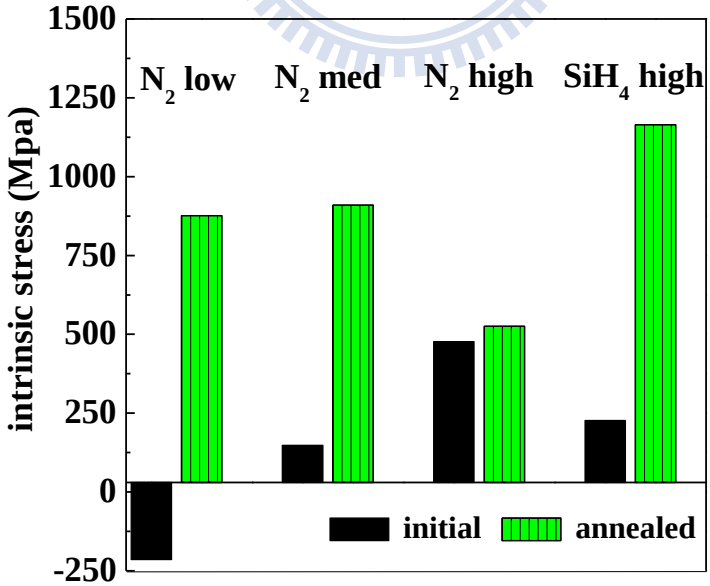


Fig. 2-22 Stress of all capping layers sketched as initial stress and annealed stress in order of magnitude.

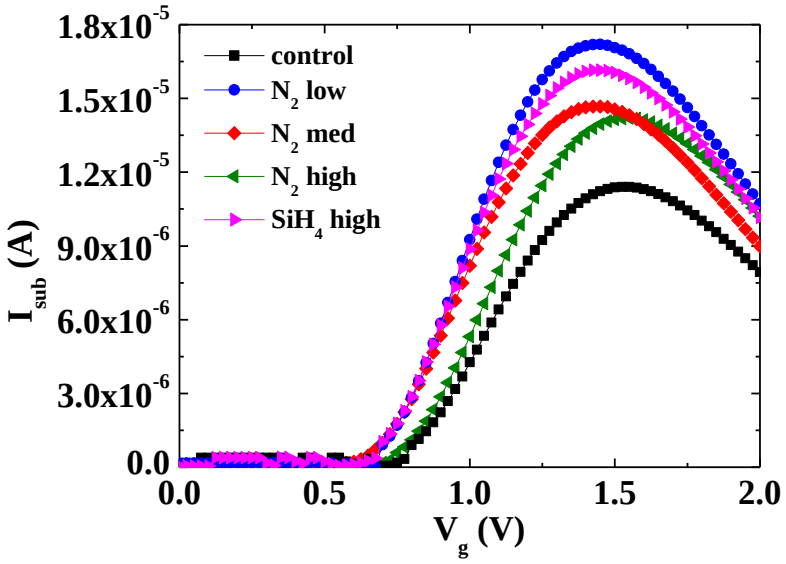


Fig. 2-23 Substrate current versus gate voltage for all samples with device size W/L=10μm/0.35μm.

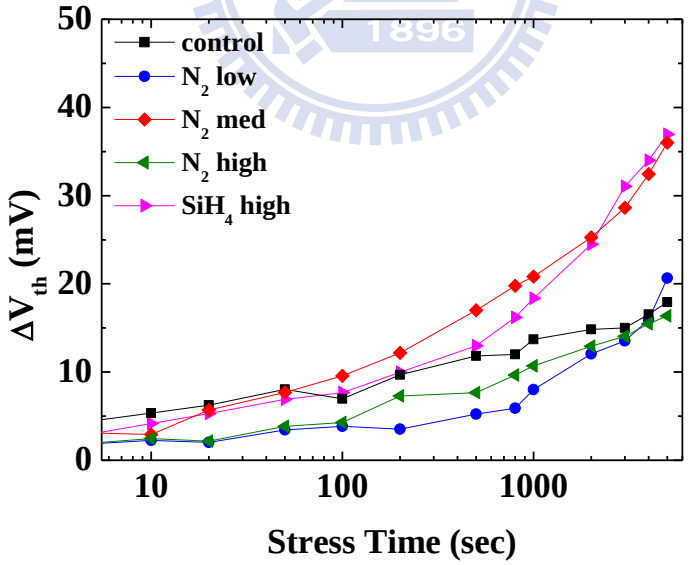


Fig. 2-24 Threshold Voltage shift as a function of stress time. Devices with W/L=10μm/0.35μm were stressed at V_{DS} = 3.5V, and V_G of maximum substrate current.

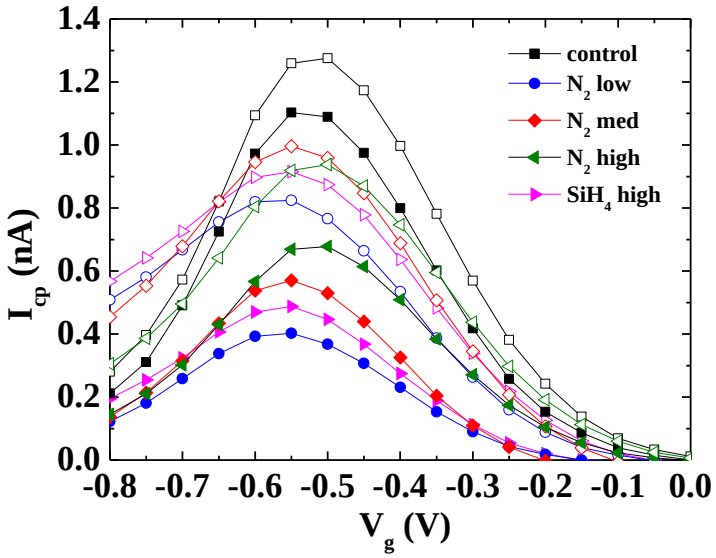


Fig. 2-25 Charge pumping current with W/L=10μm/0.35μm before and after 5000sec hot carrier stressing for all samples.

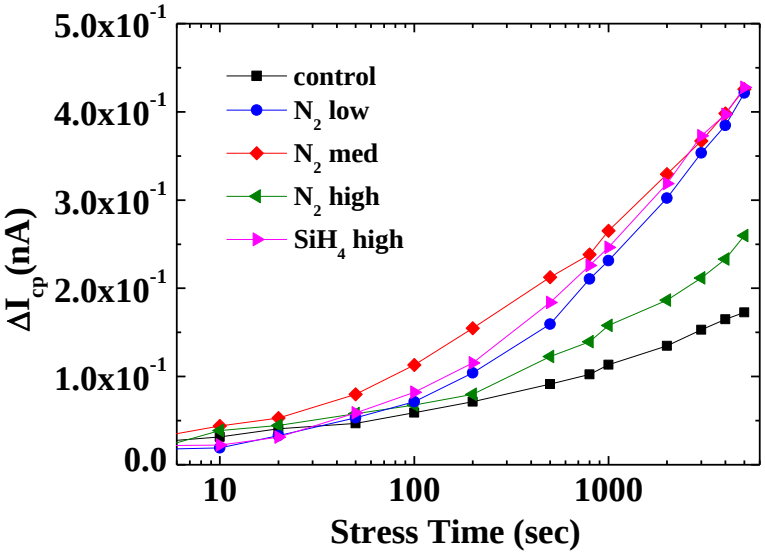


Fig. 2-26 Charge pumping current shift as a function of stress time. Devices with W/L=10μm/0.35μm were stressed at V_{DS} = 3.5V, and V_G of maximum substrate current.

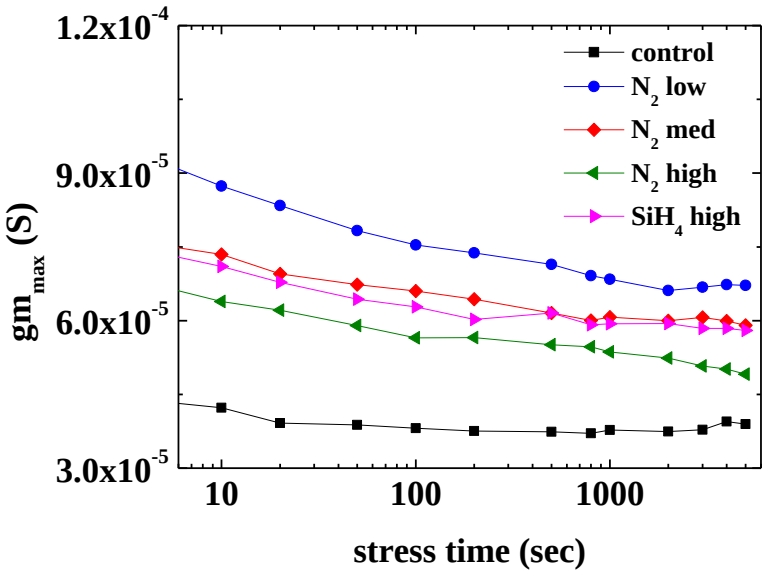


Fig. 2-27 Transconductance degradation as a function of stress time. Devices with W/L=10μm/0.35μm were stressed at V_{DS} = 3.5V, and V_G of maximum substrate current.

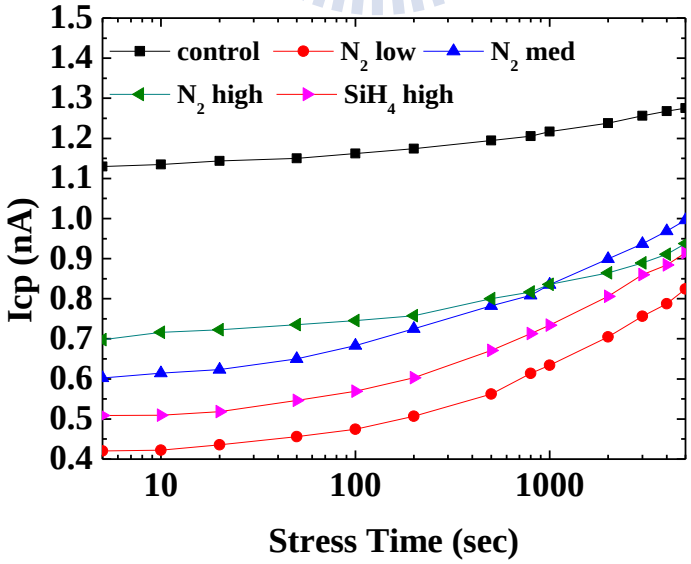


Fig. 2-28 Charge pumping current characteristics as a function of stress time. Devices with W/L=10μm/0.35μm were stressed at V_{DS} = 3.5V, and V_G of maximum substrate current.

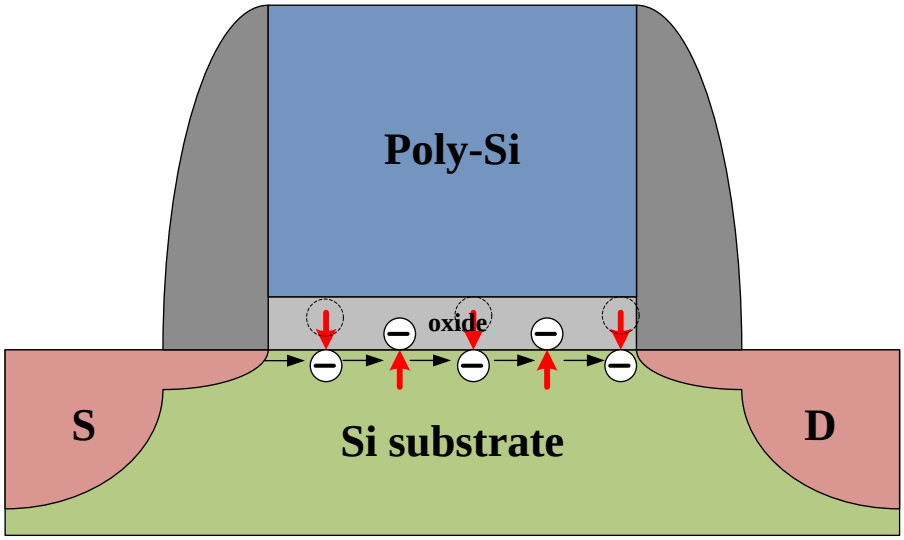


Fig. 2-29 Schematic illustration of electrons in the channel of NMOS moving in and out of traps, giving rise to fluctuations in the inversion charge density and drain current consequently.

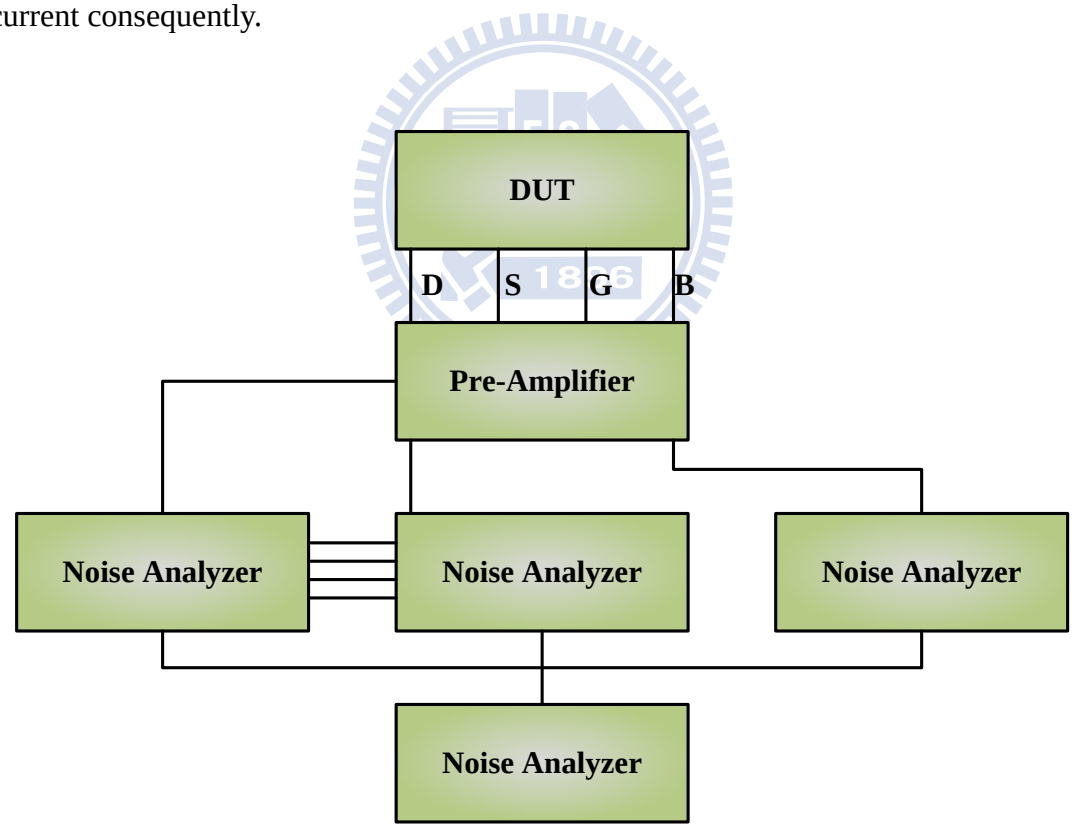


Fig. 2-30 Schematic setup for flicker noise measurement.

	0.8 V	1 V	1.2 V	1.4 V	1.6V
control	0.90576	0.92151	0.99105	0.99576	0.97286
N2 low	0.88801	0.93901	0.90855	0.92135	0.91846
N2 med	0.99949	0.98276	0.99827	0.97939	0.95814
N2 high	0.93528	0.92436	0.96475	0.96506	0.94139
SiH4 high	0.89079	0.90098	0.96002	0.97018	0.95147

Table 2 Characteristics of γ value with different gate voltage for all samples.

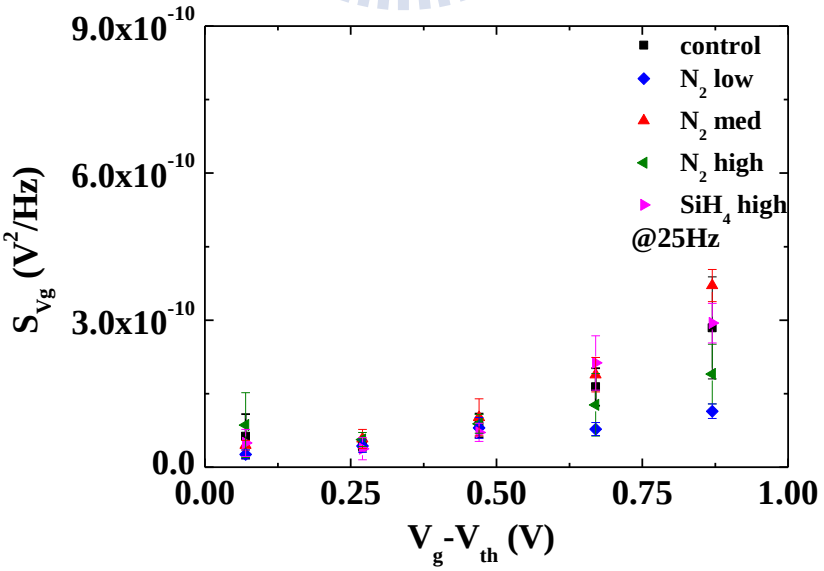


Fig. 2-31Input-referred gate voltage noise spectral density (S_{Vg}) as a function of gate voltage at V_d=0.05V and f=25Hz.

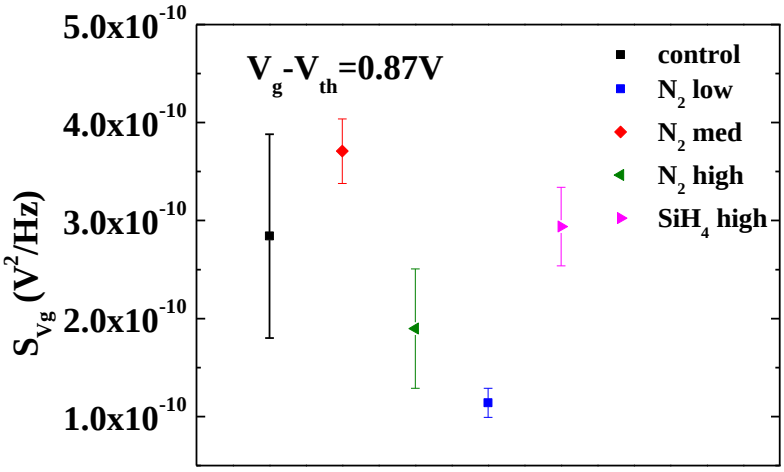


Fig. 2-32 S_{Vg}@25 Hz for all samples under V_g-V_{th}=0.87V and V_d=0.05V

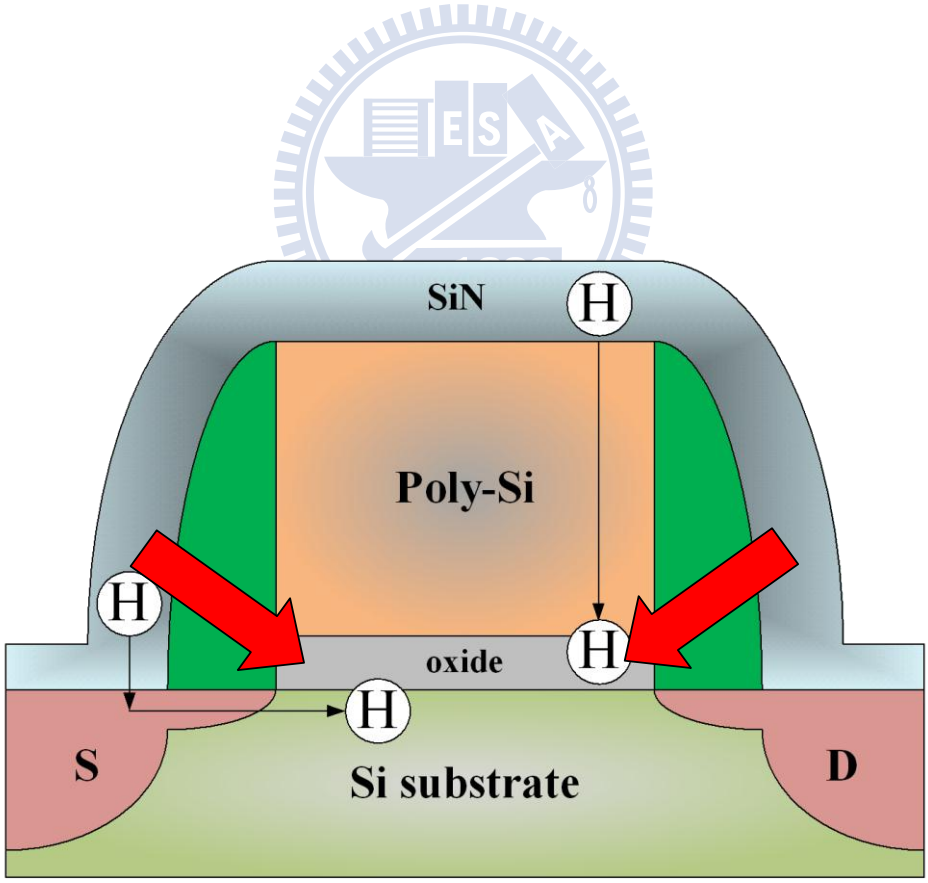


Fig. 2-33 Hydrogen diffuses and passivates the interface state, improving low frequency noise. However, if nitride stress reaches a detrimental level during annealing, it degrades oxide quality and flicker noise behavior.

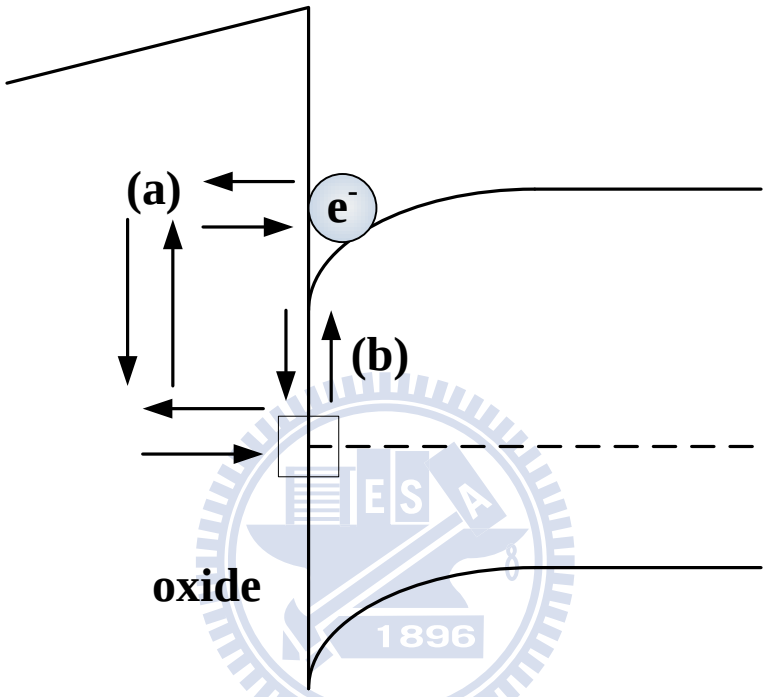


Fig. 2-34 Band diagram indicating the tunneling transitions of electrons between conduction band and traps in the gate oxide, (a) direct tunneling and (b) indirect tunneling via interface traps

Chapter 3

Effects of Channel Width and Nitride Passivation Layer on Electrical Characteristics of Polysilicon Thin-Film Transistors

3.1 Introduction

Recently, polycrystalline silicon (poly-Si) thin film transistors (TFTs) have attracted much attention, due to their application in active-matrix liquid crystal displays (AMLCDs). Further, there has been increasing interest in developing techniques for optimizing poly-Si TFTs, because such devices are promising for high vertical density components, in applications where the high mobility of single-crystal MOSFETs is not mandatory. The transfer characteristics of poly-Si TFTs depend strongly on defects in the intra-grain, grain boundary, and the gate dielectric. The deep states, which originate from the dangling bonds in grain boundaries, influence the threshold voltage and the subthreshold swing; while tail states, which originate from the intra-grain defects, affect the field-effect mobility and the minimum leakage current [3.1]-[3.2]. In order to achieve superior characteristics for poly-Si TFTs, many techniques to optimize the device performance by reducing the trap density or increasing the grain size of poly silicon have been proposed [3.3]. Therefore, passivation of these defects may improve the threshold voltage, subthreshold swing, and mobility characteristics.

Hydrogen passivation by hydrogen plasma treatment has been proposed as an effective way to improve TFT performance. However, poly-Si TFTs with hydrogen plasma treatment suffer a severe hot carrier issue, due to weak Si-H bonds. Therefore, NH_3, F, and N_2 have been proposed to improve the immunity of the hot carrier, by creating strong bonds, which are more difficult to break than Si-H bonds during hot carrier stressing [3.4]-[3.8]. Nevertheless, the additional time necessary for plasma treatment is an important issue to overcome.

Silicon nitride film is one of the most promising materials for coating and passivation films used in electronic devices and mechanical parts [3.9]. It has been reported that SiN layer can improve the performance of bulk-silicon MOSFETs [3.10], fully depleted silicon-on-insulator (SOI) MOSFETs [3.11], and a-Si thin film transistors [3.12]. Further, using a silicon nitride passivation layer is effective for suppression of the I-V kink in heterojunction field-effect transistors (HFET), since the

radicals can passivate defects, leading to a reduction in the trapping/detrapping process [3.13]. It has been reported that using a plasma deposited SiN layer as a high concentration diffusion source of atomic hydrogen is a promising approach for improving the performance of poly-Si TFTs [3.14]. However, few complete investigations of poly-Si TFTs with SiN passivation layers have been reported.

On the other hand, an appropriate choice of molecular fraction of the nitrogen mixed with the hydrogen is known to be effective in further enhancing the improvement in the plasma discharge [3.15]. However, the effect of the flow rate of different reactant gases on the deposition of the SiN layer for passivation of poly-Si TFTs has yet to be systematically investigated. In studying the impact of SiN deposition conditions on single-crystal MOSFETs, C. S. Lu et al. proposed that reducing the flow rate of the diluent gas as nitrogen results in better improvement in the interface-state due to passivation by hydrogen radicals [3.16]. In this work, we find the deposition conditions of the SiN passivation layers affect the characteristics of the poly-Si TFT.

Plasma passivation requires a very long hydrogenation-time (>4 hr) to passivate the strain-bond-related tail state [3.2]. To enable fabrication of useful transistors without additional processing time, this paper investigates the effects of an SiN passivation layer on the electrical characteristics of TFTs. The deposition time of the nitride passivation layer is less than 10 minutes, enabling significant passivation of the tail state, deep state, and trap inside the gate dielectric. As a result, TFTs with SiN passivation layers not only exhibit improved initial TFT performance, but also enhanced immunity to positive gate bias stress, negative gate bias stress, and hot carrier stressing.

3.2 Experiment

The poly-Si TFTs studied in this work were prepared as follows: an amorphous silicon film of 500 Å was deposited at 500℃ by low-pressure chemical vapor deposition (LPCVD) on thermally oxidized wafers. The wafers were annealed at 600^{o}C for 24 hours to transform the amorphous film into poly-Si, and the poly-Si films were patterned into active islands. After removal of the surface oxide, the 30-nm thick tetraethyl orthosilicate (TEOS) oxide was deposited at 680^{o}C. A 2000 Å thick poly-Si layer was deposited and patterned as the gate electrode, which also serves as

the mask for self-aligned implantation. The source/drain and gate regions were then implanted by phosphorous (15 keV at 5 x 10^{15} cm^{-2}) and activated at 600℃ for 24-h annealing in N_2 ambient. The SiN layers were deposited under four different deposition conditions by plasma-enhanced chemical vapor deposition with the same thickness of 3000Å . The control sample was skipped in this step. The power, pressure, and temperature were set at 100-W, 137-Pa, and 300℃, respectively. Table 1 shows the reactant and diluent gas flow rates used to investigate the effect of the nitride passivation layer. The samples were labeled N_2-low, N_2-med, N_2-high, and SiH_4-high. A 2000Å PECVD oxide was then deposited at 300℃ in 2.5 minutes for all TFTs capped with a nitride passivation layer. For comparison, a PECVD oxide (5000 Å) passivation layer was deposited at 300℃ in 6.3 minutes on the control sample. Hence, all samples have passivation layers of identical thickness. After patterning of the contact holes, aluminum was deposited by PVD and patterned as the probe pads to complete the TFT devices. For comparison, some devices underwent Post-SiN-deposition thermal annealing in nitrogen at 350℃ for 60min.

3.3 Results and Discussions

3.3.1 Performance

Figure 3-1 shows the I_d-V_g curves of n-channel TFT for the control sample and the samples with the SiN passivation layer. The channel length and width are both 10 μm. It is evident that n-channel TFTs exhibit improved performance with the capped SiN layer, compared to control samples. The threshold voltage and subthreshold swing are improved compared to the control sample, meaning that using SiN passivation appears to effectively terminate the dangling bonds in the poly-Si and SiO_2/poly-Si interface. Further, the gate induce drain leakage (GIDL) is suppressed for the poly-Si TFTs with SiN capping compared to the control sample, which is attributed to trap passivation. The N_2-high sample possesses the highest subthreshold swing, while the SiH_4-high sample possesses the lowest peak transconductance, as shown in Fig. 3-2. In contrast, the control sample possesses no peak transconductance, due to the hole trapping. The N_2-med and N_2-low possess better transfer characteristics.

The above results indicate that the deposition conditions of SiN passivation

layers affect the characteristics of poly-Si TFTs. Both the NH_3 and N_2 plasma passivation effectively improve TFT transfer characteristics by plasma discharge. However, NH_3 plasma treatment is more effective than N_2 plasma treatment, because the hydrogen radicals are most effective for passivating the grain boundary and trap states [3.6]-[3.8]. In our work, during the deposition of SiN, the hydrogen and nitrogen radicals diffuse and passivate intra-grain and grain boundary trap state in the poly-Si by forming Si-H and Si-N bonds. The reactant gas of NH_3 can generate the hydrogen and nitrogen radicals, and the reactant gas of N_2 plasma can generate only the nitrogen radicals. As a result, the deposition-condition of SiN has a significant influence on the generation of radicals as well as on poly-Si TFT device performance.

Figure 3-3 shows the drain-current-vs-drain voltage (I_d-V_d) characteristics of all n-channel poly-Si TFTs. There are three distinct features of these characteristics. At low overdrive voltage, all samples capped with SiN exhibit better performance than the control sample, due to passivation of the tail state. As the overdrive voltage is further increased, however, the control sample has better performance than the SiH_4-high sample, due to hole trapping at higher gate voltage (discussed later). At higher drain biases the “kink” effect is much more pronounced for the control sample than its counterparts. We believe that trap passivation is responsible for the suppressed kink effect. There are several models for the explanation of pronounced kink effect by trap. B. Kim et al. demonstrated that the kink effect depends on the nature of surface states [3.17]. M. Hack et al. proposed that the presence of grain boundaries or traps in poly-Si TFT’s significantly enhanced the kink effects in poly-Si TFT’s, compared to single-crystal counterparts [3.18]. A. K. K.P. et al. predicted that the local electric field near the irregular surface due to grain boundaries can be appreciably greater than the average electric field, which can initiate additional impact ionization [3.19]. Thus, the reduced trap induced by the radicals is a reasonable explanation for the suppression of the kink effect.

A high quality gate oxide and interface between gate oxide and the poly-Si channel are critical for transfer characteristics. Due to the nature of TEOS oxide, there are more dangling bonds and weak Si-O and Si-Si bonds in the bulk oxide and in the interface between the gate oxide and the poly-Si channel. Figure 3-4 shows the gate-leakage characteristics for all samples. The TFTs capped with SiN layers possess lower leakage than the control sample, indicating that using SiN passivation layers is an effective way to improve gate oxide quality. It has been reported that large

amounts of nitrogen exist in oxynitride film. This enables formation of strong Si ≡ N bonds in the oxynitride/poly-Si interface that can improve gate leakage and charge trapping [3.20]. Further, NH_3 and H_2 plasma treatments are effective in improving gate leakage [3.21].Thus, passivation of defects in the bulk oxide, nitrogen pile-up at the oxide-poly silicon interface, and improved interface state condition by nitrogen radicals are responsible for improving gate leakage during SiN deposition. As a result, using SiN passivation layers enables termination of both traps in the poly-Si channel and pre-existing traps in the gate oxide by radicals.

3.3.2 Width Dependence of TFT Capped Nitride Passivation Layers

The transfer characteristics of N_2-high sample exhibits a double hump as shown in Fig. 3-1, implying that hydrogen and nitrogen radical propagation is less effective. In order to clarify the double hump phenomenon of the N_2-high sample, we compared the transfer characteristics of the N_2-high samples of different channel widths as shown in Fig. 3-5. The double hump in the subthreshold region indicates the secondary conduction path for the device with a width of 10 μm. As the width is scaled down, the double hump phenomenon is suppressed. A physical mechanism is proposed to explain the early turn-on phenomenon for device with a width of 10 μm. It is noted that the number of defects and available radicals affects the efficiency of passivating defects [3.1]. The trap passivation is not complete for the entire poly-Si channel for devices with wider channel width, as shown in Fig. 3-6a. A portion of the poly Si channel, which was passivated by nitrogen or hydrogen radicals, has a lower local threshold voltage than unpassivated portions of the channel, resulting in a nonuniform threshold voltage. Moreover, the nonuniform threshold voltage exhibits the early turn-on phenomenon. As the channel width is scaled down, the portion of the poly-Si channel without passivation by radicals is minimized, as shown in Fig. 3-6b, and the double hump phenomenon is suppressed, since the radicals can diffuse and passivate the trap effectively.

In order to clarify the width effect on the devices' electrical characteristics, a detailed investigation of the parameters of the poly-Si TFTs is necessary. Again, the threshold voltage, subthreshold swing, and maximum mobility strongly depend on the grain, grain boundaries, and interface properties. As shown in Fig. 3-7a, TFTs capped with SiN passivation layers possess better subthreshold swing than the control sample

for all dimensions, and the N_2-low and SiH_4-high have the lowest subthreshold swing. All samples with SiN passivation layers possess saturated features. These results indicate that the passivation of the deep state in the grain boundary is efficient, so the decrease of subthreshold swing is less dependent on the variation in channel width. Figure. 3-7(b) demonstrates the threshold voltage as a function of width. The threshold voltage (V_{th}) is defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L) \times 100nA$ at $V_{DS} = 0.1V$. The threshold voltage of the control sample decreases as the width is scaled down, which is attributed to the grain boundary effect. In contrast, the improvement in the threshold voltage increases as the width shrinks for TFTs with capped SiN passivation layers. I. W. Wu et al. found that the subthreshold swing decreases monotonically with hydrogenation, similar to the response of the threshold voltage [3.2]. However, the improvement in the subthreshold swing does not display a strong dependence on channel width in this work. Thus, we believe that not only increased passivation of the deep state, but the increased passivation of pre-existing defects in the gate oxide are the mechanisms by which the threshold voltage improves as the width is scaled down. It has been reported that the dominant pathway for hydrogen diffusion into the active poly-Si film may be through the gate oxide where the diffusivity of hydrogen is much higher than in the poly-Si layer [3.1][3.22]. Thus, passivation of the pre-existing traps by hydrogen or nitrogen radicals is reasonable. Passivation of pre-existing traps in the gate oxide becomes more efficient as channel width narrows, which is responsible for the improvement in the threshold voltage. The increase of mobility along with the channel width decrease is observed in Fig. 3-7(c). Two mechanisms may explain the mobility's dependence on the channel width. The first mechanism is the improvement in the interface state condition and the enhanced passivation of the tail state in poly-Si channel film at narrow channel widths. The second possible cause is the lower impact of the grain boundaries. At wider channel width, the SiH_4-high sample has the lowest mobility, meaning that the SiH_4-high has the lowest tail state passivation among all samples. The mobility for all TFTs capped with the SiN passivation layer becomes comparable at narrow channel widths. We believe that the passivation of the tail state by the SiN passivation layer increases as the width falls, becoming similar for all nitride conditions at narrow channel widths, because the defects can be passivated effectively when a sufficient number of radicals is supplied.

In general, the improvements in threshold voltage and mobility by nitride

passivation become more significant as channel width is scaled down, because hydrogen or nitrogen radicals can terminate the strain bonds, and more efficiently passivate the pre-existing defects in the bulk oxide and interface. Moreover, the H_2-plasma easily passivates dangling bonds in the grain boundaries to reduce the midgap deep states, while a very long hydrogenation-time (>4 hr) is required to passivate the strain-bond-related tail state [3.2]. This theory is consistent with the effect of using a SiN passivation layer. In this work, using an SiN passivation layer passivates the deep states and the strain-related tail state. Passivation of deep states is rapidly saturated, since the improvement in the subthreshold swing stays almost constant for all channel widths. On the other hand, the difference in mobility decreases for TFTs with different SiN passivation layers as the width is scaled down, meaning that passivation of tail state is slow compared to passivation of the deep state.

3.3.3 PGBS, NGBS, and Hot Carrier Stressing

Another important issue in poly-Si TFT is reliability. The positive gate bias stress (PGBS), negative gate bias stress (NGBS), and the hot carrier stressing often degrade the reliability of TFT devices. Positive gate bias stress was carried out at $V_{DS} = 0V$ and $V_{GS} = 10V$ for 3000s to examine the device reliability, as shown in Fig.3-8. The tunneling of hot holes from the gate into the substrate may be responsible for the positive charge trapping in the control sample during the initial stressing period, and the electron trapping would then become the dominant trapping mechanism [3.23]. By contrast, samples capped with SiN passivation layers have smaller shift in threshold voltage than the control sample. Negative gate bias stress was carried out at $V_{DS} = 0V$ and $V_{GS} = -10V$ for 1000s to examine the device reliability, as shown in Fig. 3-9. The control sample exhibits a significant electron trapping, while TFTs capped with SiN passivation layers show improved electron trapping. These results show that using SiN passivation layers can improve the immunity of PGBS and NGBS.

Fig. 3-10(a) shows the dependence of dc hot-carrier degradation at a drain voltage (V_D) of 18 V on overdrive voltage (V_G-V_{th}) for all samples, where I_{on} is a drain current (I_D) at V_g of 9 V and V_D=0.1 V, I_{ono} is the initial value of I_{on}, and ΔI_{on} is the decrease in I_{on} after 1000s of stress. For bulk-silicon, the worst dc hot carrier

degradation occurs when the stress condition, V_g, is about half of V_d. However, the worst case stress condition of the thin film transistor is lower than that of the bulk-silicon. Y. Toyota found that the worst stress condition is $V_{GS} = 2V$ at $V_{DS} = 10V$ [3.24]. In this work, we found the lowest degradation at $V_{GS} - V_{th} = 5V$. Thus, we believe that the significant degradation of drain current below $V_{GS} - V_{th} = 5V$ Vis attributable to hot carrier induced damage, and the degradation of drain current above $V_{GS} - V_{th} = 5V_g$ is attributable to positive gate bias stress induced damage. In contrast, samples capped with SiN passivation layers show slight variation in the drain current (below 5%). Threshold voltage shift and the relative variation of transconductance of TFTs with and without SiN passivation layers are shown in Figs.3-10(b)(c). Samples capped with SiN passivation layers exhibit improved threshold voltage shift and mobility degradation. The improved immunity of hot carrier stressing for samples with SiN passivation layers is comparable to that of samples with plasma treatment in the literature [3.25]-[3.26].

We found that TFTs capped with SiN passivation layers show improved immunity to positive gate bias stress, negative gate bias stress, and hot carrier stressing. We believe this improvement is due to the passivation of traps in the grain boundaries, intra-grain, and TEOS oxide with strong Si ≡ N bonds during the deposition of SiN passivation layer [3.27].

3.3.4 Post-SiN-deposition Thermal Annealing

It has been reported that the improvement by using hydrogen radicals to passivate the defects would degrade during the post annealing, indicating the limits on thermal cycling after the hydrogenation process[3.28]. Figure 3-11 shows the I_d-V_g curves of n-channel TFT for the control sample and the samples with the SiN passivation layers after Post-SiN-deposition Thermal Annealing. The channel length and width are both 10 μm. The threshold voltage would decrease after post-annealing for samples with the SiN passivation layers；However, the threshold voltage of the control sample is comparable to the original value. And the characteristics of subthreshold swing are relatively insensitive to the post annealing. Figure 3-12 shows the characteristics of transconductance after Post-SiN-deposition Thermal Annealing. For TFTs with the SiN passivation layers, the treatment of post annealing would degrade the transconductance as well as the passivation of tail states, indicating that

using SiN passivation layers also suffers the limits on thermal cycling after the deposition of SiN. A physical mechanism is proposed to explain the hydrogen instability induced by post annealing as Figure 3-13. We believe that the post annealing would break the passivation of tail states created by hydrogen, compared to deep states, due to hydrogen bonding in dangling bonds is far stronger than the tail states (about 2eV) [3.2]. The break of passivation of tail states would induce the degradation of transconductance. The hydrogen may diffuse into the gate oxide, and decrease the threshold voltage subsequently.

3.4 Summary

Using an SiN passivation layer was found to yield better performance, suppress the kink effect, and improve gate induce drain leakage (GIDL) for polysilicon thin film transistors (poly-Si TFTs) without the long hydrogenation time required by plasma-treatment. TFTs capped with different SiN passivation layers show differences in their performance improvements, since different mechanisms are involved. Additionally, a mechanism to explain the double hump phenomenon induced by incomplete trap passivation for SiN deposited with high flow rates of nitrogen was proposed.

All samples with SiN passivation layers exhibit saturated improvement of the subthreshold swing. However, the characteristics of mobility become comparable across all samples at narrow channel widths. This shows that the subthreshold swing improvement, which is affected by the deep states, has a more rapid response to radical diffusion than the mobility improvement induced by tail state passivation.

Furthermore, using SiN passivation layers exhibits excellent reliability characteristics. We believe that the passivation of traps in the grain boundaries, intra-grain, and TEOS oxide with strong $Si \equiv N$ bonds is responsible for the improved gate leakage and reliability.

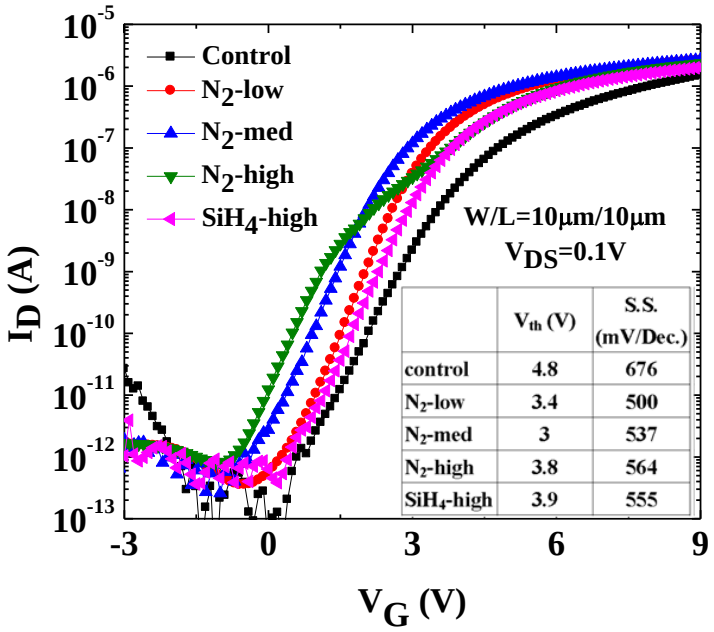


Fig. 3-1 Transfer characteristics (I_D-V_G) of n-channel TFTs with different passivation layers.

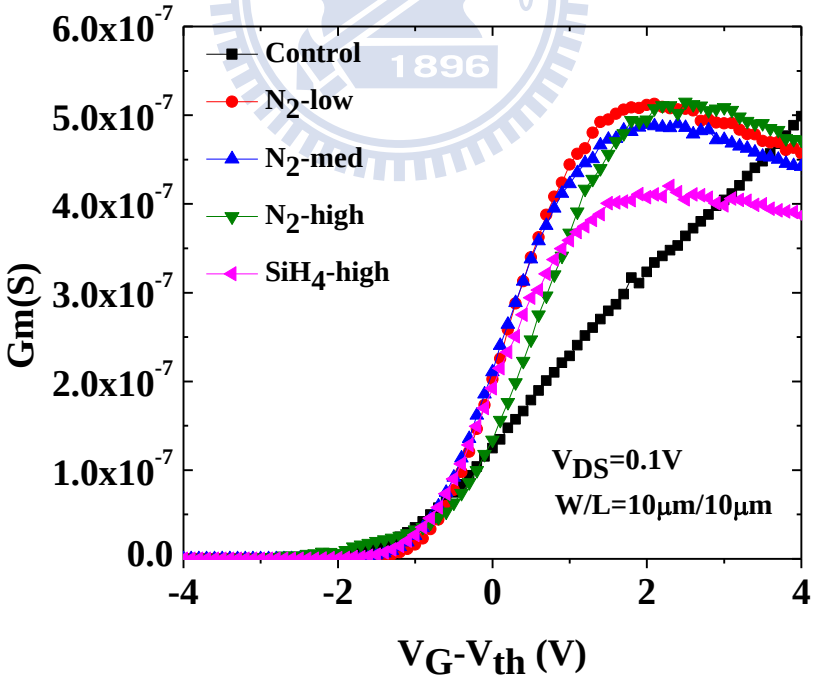


Fig. 3-2 Transconductance of n-channel TFTs with different passivation layers.

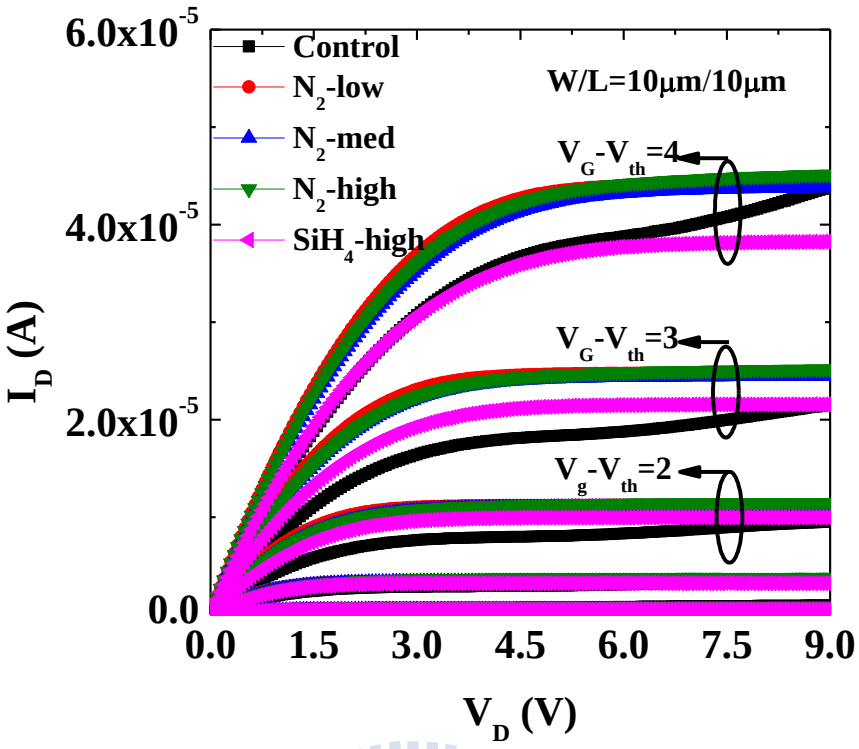


Fig. 3-3 Output characteristics (the I_D-V_D curve) of n-channel TFTs with different passivation layers.

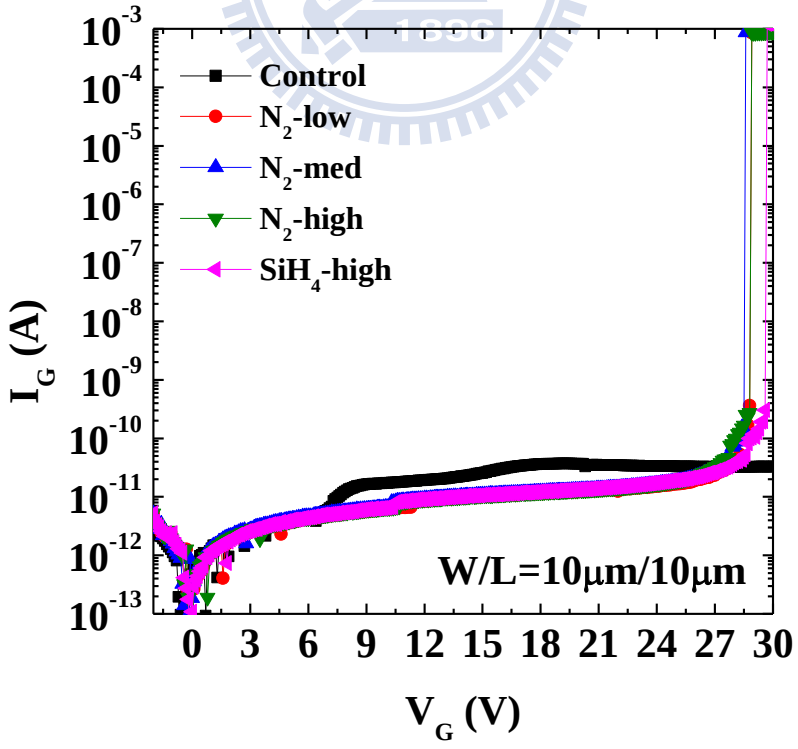


Fig. 3-4 Gate leakage current of n-channel TFTs for all samples.

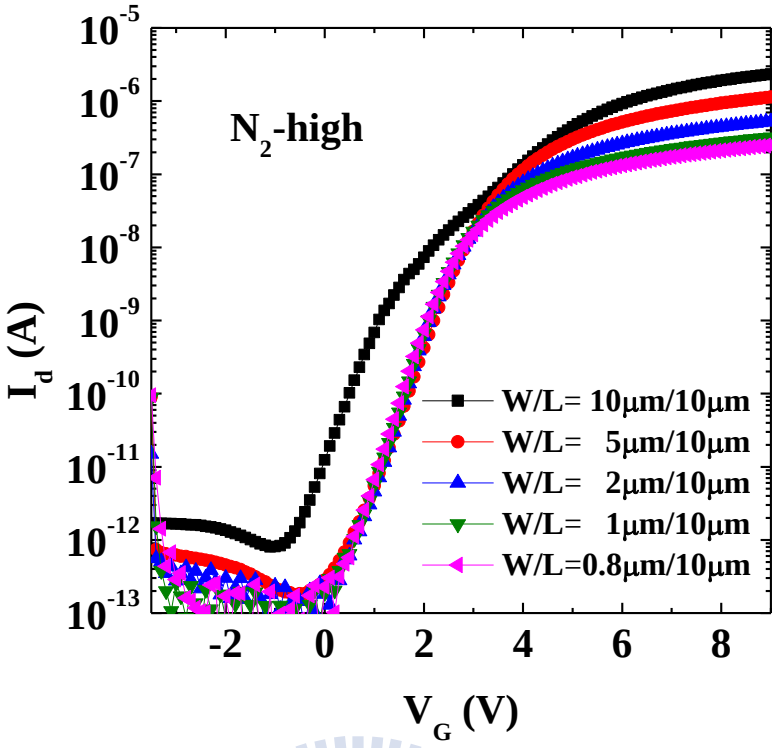


Fig. 3-5 Transfer characteristics (I_D-V_G) for N_2-high sample with different channel width.

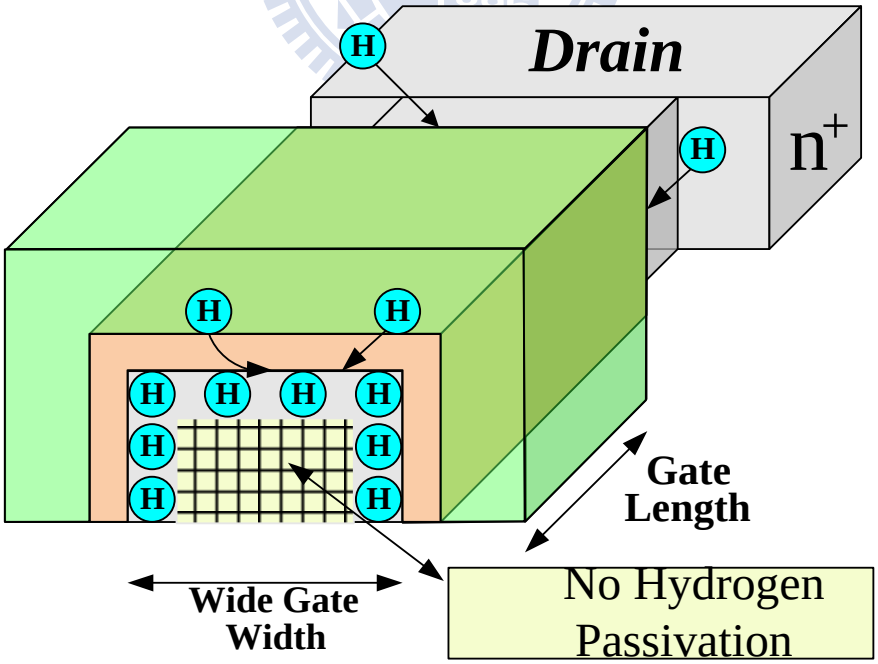


Fig. 3-6(a) Cross-section of n-channel TFTs with wider channel widths. The incomplete trap passivation is also indicated, and is responsible for the double hump phenomenon.

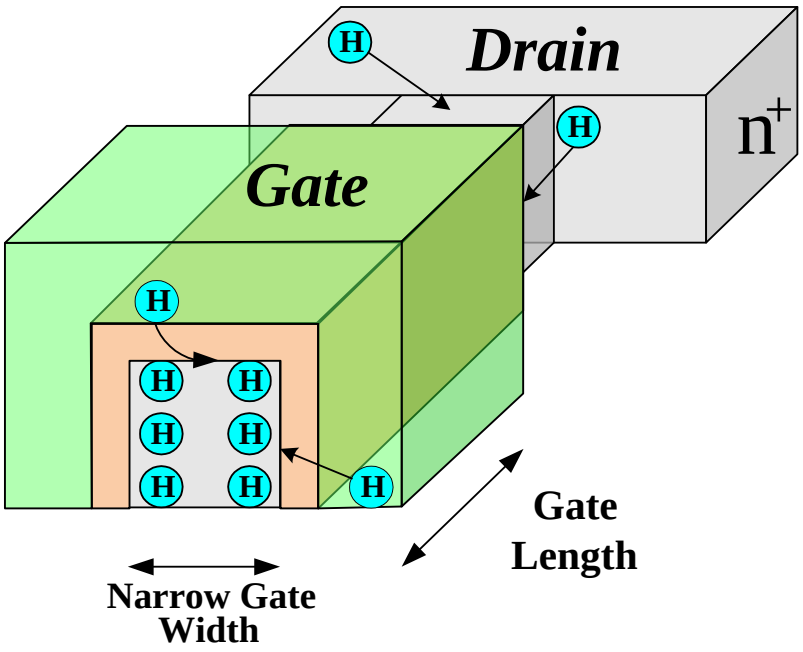


Fig. 3-6(b) Cross-section of n-channel TFTs with narrower channel widths. The complete trap passivation appears to suppress the double hump phenomenon.

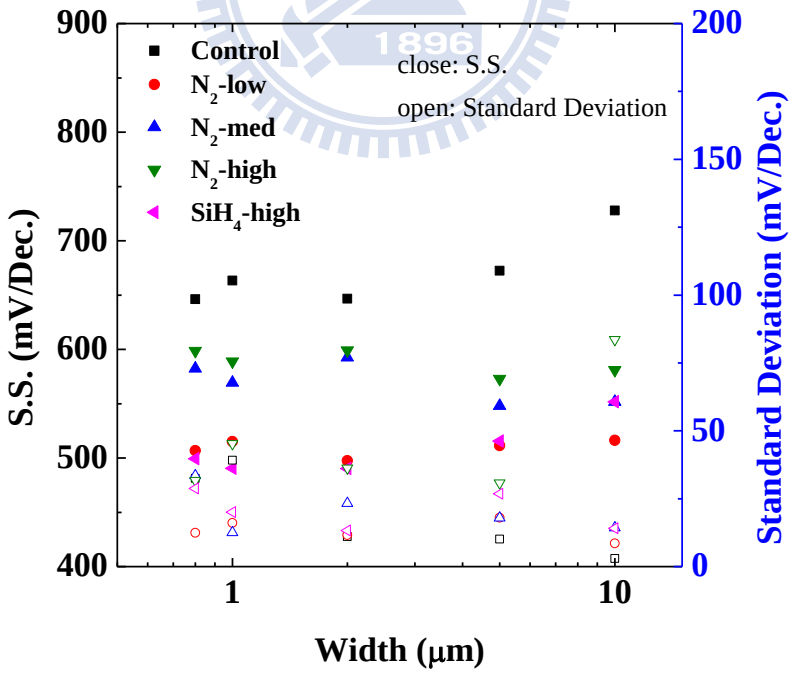


Fig. 3-7(a) Variation of subthreshold swing as a function of channel width for L = 10μm with different passivation layers.

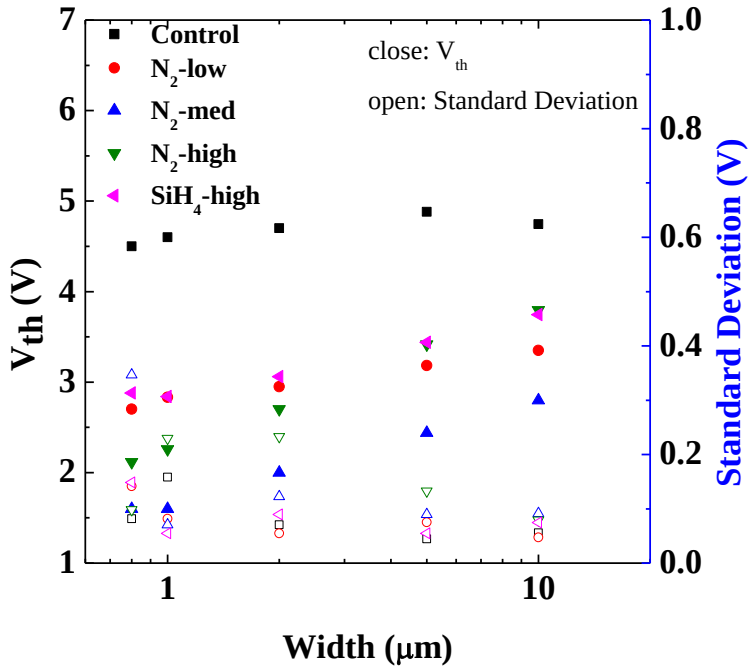


Fig. 3-7(b) Variation of threshold voltage as a function of channel width for L = 10μm with different passivation layers.

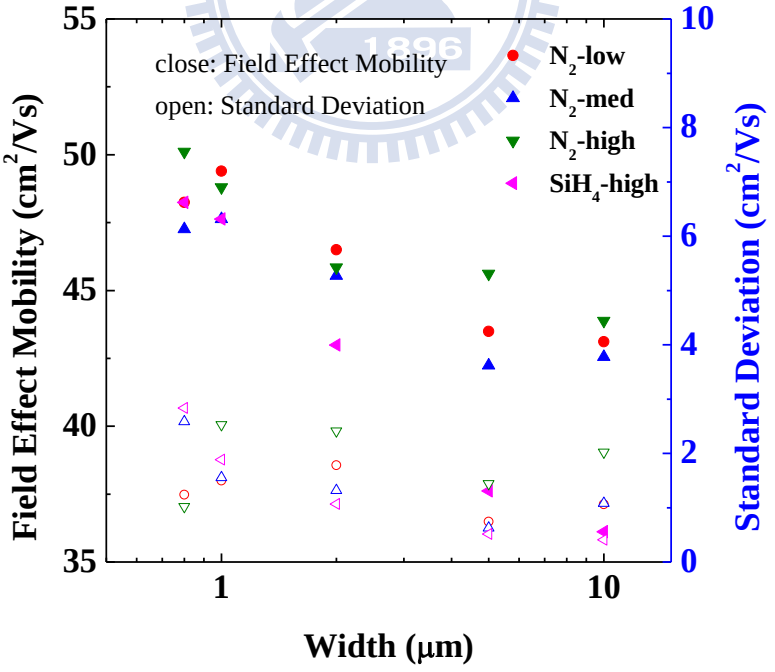


Fig. 3-7(c) Variation of field mobility as a function of channel width for L = 10μm with different passivation layers.

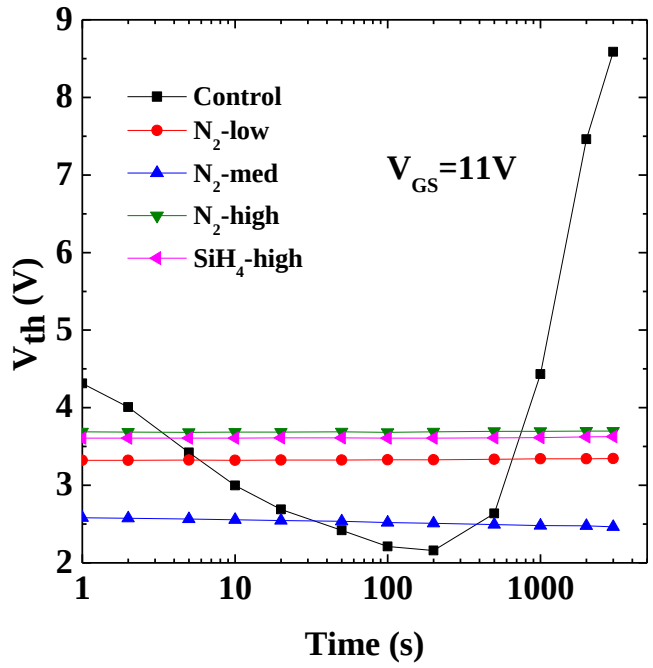


Fig. 3-8 Threshold voltage shift as a function of stress time for n-channel TFTs under positive gate bias stress as V_{GS} =11V .

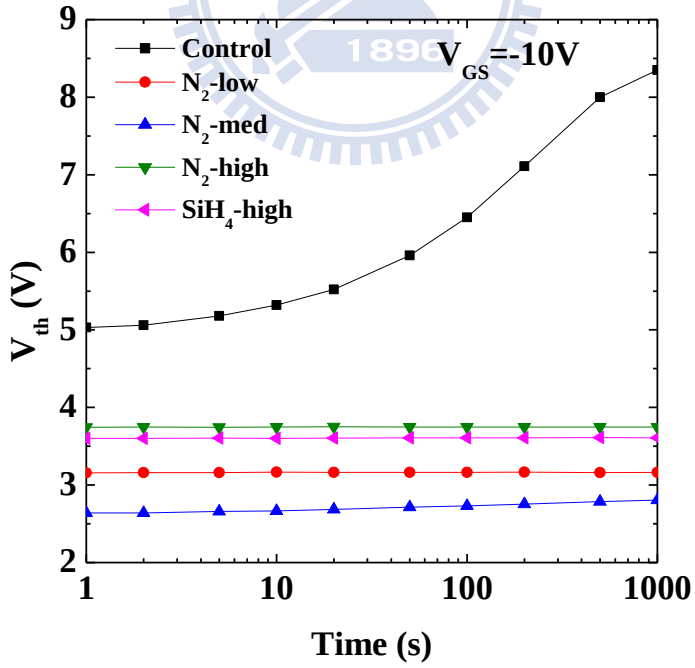


Fig. 3-9 Threshold voltage shift as a function of stress time for n-channel TFTs under negative gate bias stress as V_{GS}= -10V.

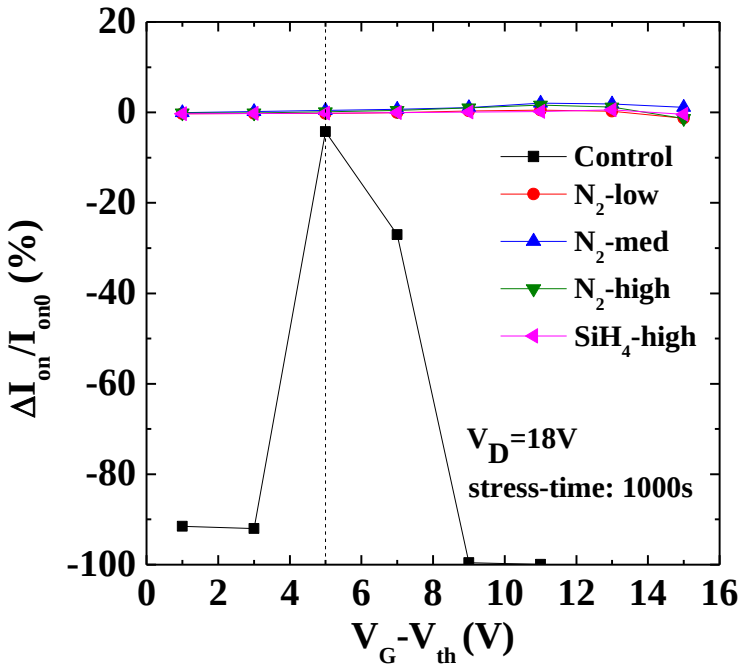


Fig. 3-10(a) Dependence of I_{on} degradation under dc stress on gate voltage for all samples.

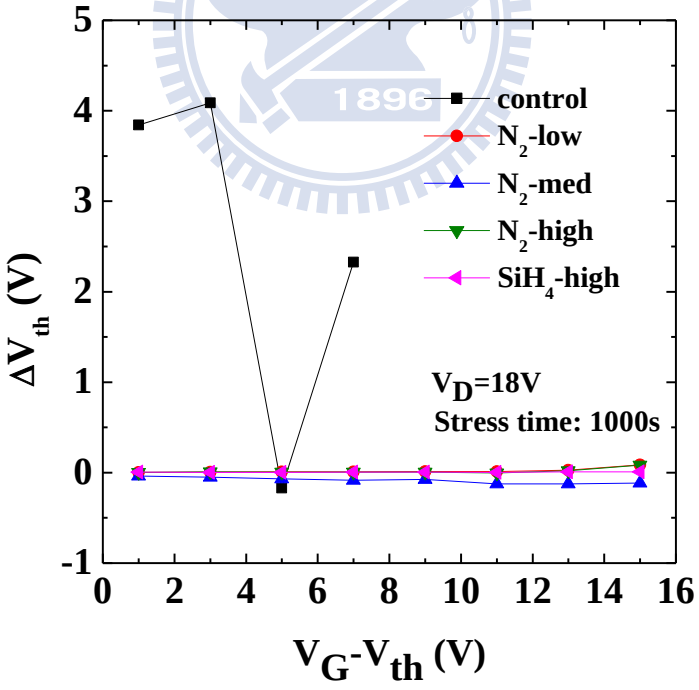


Fig. 3-10(b) Dependence of V_{th} degradation under dc stress on gate voltage for all samples.

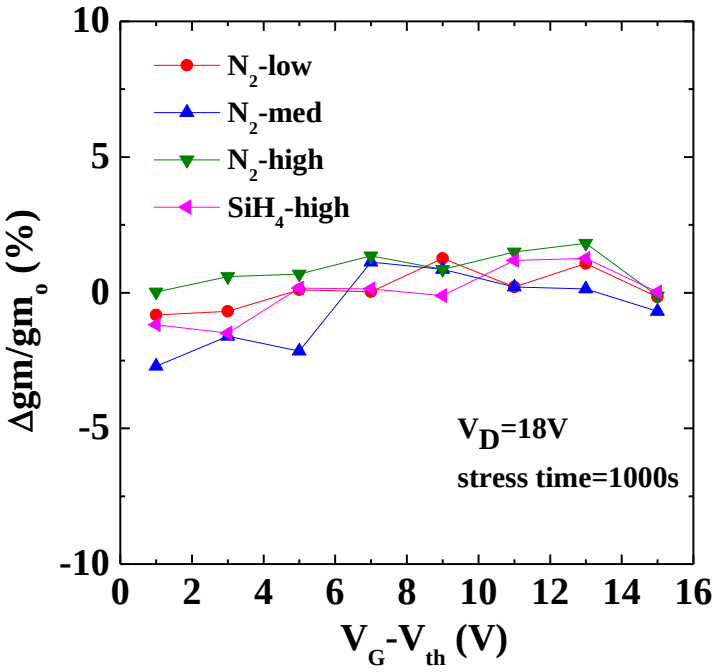


Fig. 3-10(c) Dependence of transconductance degradation under dc stress on gate voltage for all samples.

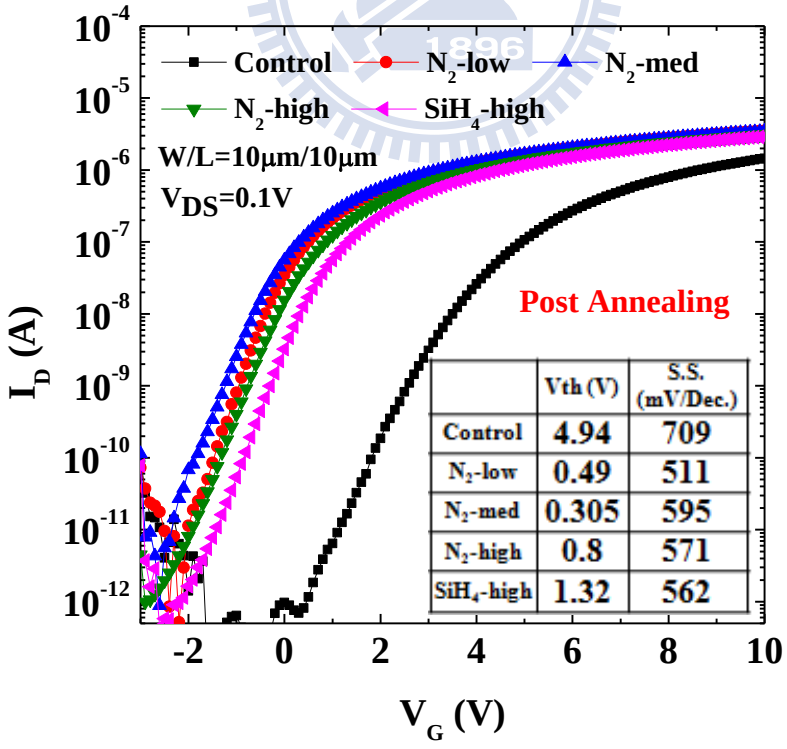


Fig. 3-11 Transfer characteristics (I_D-V_G) of n-channel TFTs with different passivation layers after the post annealing.

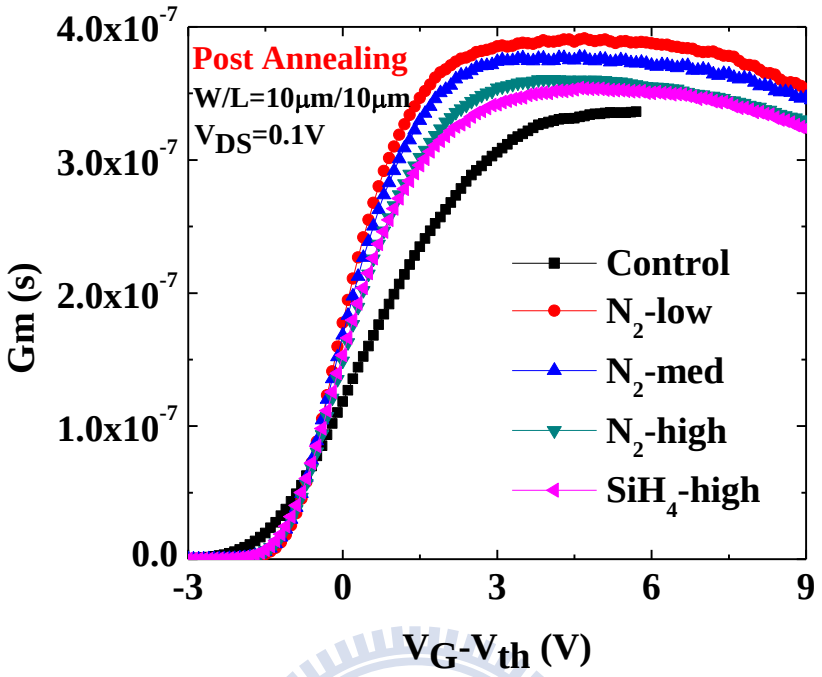


Fig. 3-12 Transconductance of n-channel TFTs with different passivation layers after the post annealing.

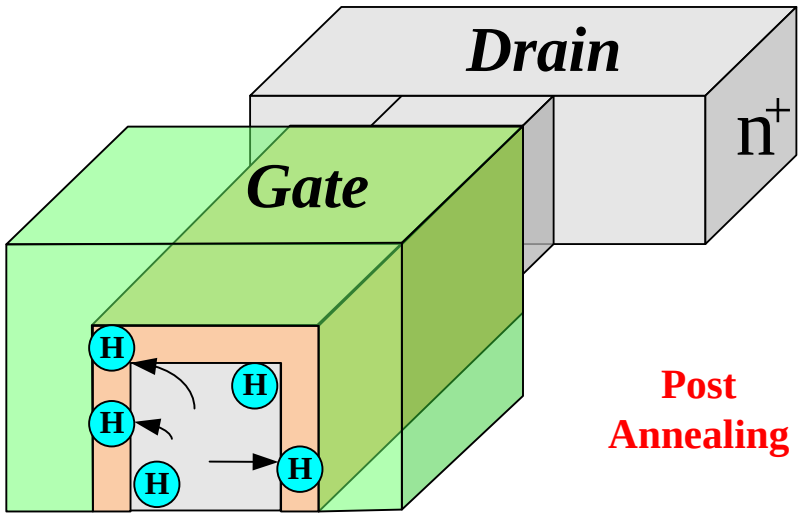


Fig. 3-13 A mechanism of hydrogen instability induced by post annealing.

	N_2-low	N_2-med	N_2-high	SiH_4-high
N_2 (sccm)	50	100	1000	100
NH_3 (sccm)	6	6	6	6
SiH_4 (sccm)	50	50	50	100

Table 4.1

Chapter 4

Hydrogen Instability Induced by Post Annealing on Poly-Si TFTs

4.1 Introduction

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) have attracted attention recently, due to their potential applications in active-matrix liquid crystal displays (AMLCDs) and high density vertically components [4.1]-[4.2].Because the grain boundaries in poly-Si TFTs have a profound influence on device characteristics and degrade carrier transport, developing promising techniques to reduce the trap density is important. Previous research shows that hydrogen plasma treatment and hydrogen-containing nitride film deposition are promising approaches for improving performance [4.3]-[4.5], because hydrogen radicals can effectively passivate the defects of intra-grain, grain boundary, and the gate dielectric [4.3]-[4.4].

In addition to using hydrogen plasma or hydrogen-containing nitride to passivate the traps deliberately, the hydrogen diffuses into the polysilicon during the fabrication process, in areas such as the buffered layer, the gate dielectric, and the hard mask of nanowires [4.6]-[4.9]. However, this hydrogen diffusion into the polysilicon easily suffers from subsequent thermal processes such as solid phase crystallization, the deposition of gate dielectric, and the dopant activation, resulting in unavoidable hydrogen instability.

Post annealing decreases the benefits of using hydrogen radicals by plasma treatment to passivate these defects, indicating that there are limits to thermal cycling after the hydrogenation process. The effects of the post annealing temperature on the poly-Si TFT performance have also been studied experimentally [4.10]. However, the effects of the hydrogen instability induced by post annealing on the passivation of tail states, the passivation of deep states, and the additional defect generation in poly-Si TFTs must be clarified. To investigate the effects of hydrogen instability, it is necessary to eliminate the Si-H bonds completely by post annealing, and avoid the issue of plasma damage.

We investigate the passivation efficiency of hydrogen using hydrogen-containing nitride, based on the comparison of different thicknesses of SiN or inserted TEOS

oxide. Although the issue of hydrogen has been thoroughly investigated for single-crystal MOSFETs [11][12], to our knowledge, this is the first time the issue of hydrogen release for poly-Si TFTs capped SiN has been demonstrated. These results indicate two types of defects: the original type of defect affected by passivation/depassivation and a second type generated by hydrogen release during subsequent annealing. Further, the characteristics of n-channel TFTs under a negative bias stress, positive bias stress, and hot carrier stressing are studied for a comprehensive reliability investigation.

4.2 Experiment

The entire process for device fabrication is shown schematically in Figure 4-1. Amorphous silicon film measuring 500 Å thick was deposited on thermally oxidized wafers at 500°C by a low-pressure chemical vapor deposition (LPCVD). The wafers were annealed at 600℃ for 24 hours to transform the amorphous film into poly-Si, and the poly-Si films were patterned into active islands. After removing the surface oxide, a 30-nm thick tetraethyl orthosilicate (TEOS) oxide was deposited on the wafers. A 2000 Å thick poly-Si was deposited and patterned to form the gate electrode, which also served as a mask for self-aligned implantation. The source/drain and gate regions were then implanted with phosphorous (15 keV at 5 x 10^{15} cm^{-2}) and activated at 600℃ for 24-h annealing in the N_2 ambient. In order to investigate the buffered oxide thickness effects on passivation efficiency, 10-nm or 20-nm thick tetraethyl orthosilicate (TEOS) oxide was deposited. Further, in order to investigate the nitride thickness effects on passivation efficiency, 100-nm or 200-nm SiN was deposited by LPCVD at 780℃ for coupling hydrogen without plasma damage. During the deposition process, the hydrogen radicals diffused and passivated the defects in the channel. Under the same pressure, all samples received the same thermal budget by annealing in the nitrogen as shown in Fig. 4-2. The sample, denoted as SiN-removed, was capped by 10-nm TEOS oxide and 100-nm SiN layer originally. The capping SiN was then removed by a carefully selective wet etching process. A 500-nm thick tetraethyl orthosilicate (TEOS) oxide formed at 680℃ was adopted as the passivation layer as well as post annealing for all samples. After patterning the contact holes, aluminum was deposited by PVD and patterned as the probe pads to complete the TFT devices. Poly-Si TFTs of different channel widths from 10 to 0.8-μm and gate

lengths from 10 to 1-μm were fabricated to analyze the passivation effects.

4.3 Results and Discussions

4.3.1 Thickness Control of Deposited Inserted TEOS oxide and SiN films

Figures 4-3(a) and 4-3(b) demonstrate the threshold voltage as a function of width and length, respectively. The threshold voltage (V_{th}) is defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L) \times 100nA$ at $V_{DS} = 0.1V$. Figures 4-4(a) and 4-4(b) show the mobility as a function of width and length, respectively. The field-effect mobility μ_{FE} is extracted from the maximum transconductance. The calculated mobility decreases as the channel length shortens, due to the influence of the S/D series resistance on the transconductance. The threshold voltage of the control sample decreases as the channel widths fall from 10-μm down to 0.8-μm, since the gate control is further increased with decreasing of the channel width due to corner portion domination [4.2]. It is noted that the passivation effect by PECVD SiN passivation layer or plasma discharge exhibits the strong width dependence, since the portion of the poly-Si channel without passivation by radicals is minimized as the channel width is scaled down [4.13]. The improvements in threshold voltage and mobility by capping LPCVD SiN are significant for all width dimensions, implying that LPCVD SiN passivation layer exhibits higher passivation efficiency. The improvements are relatively insensitive to the channel length dimension, since the decreasing quantity of traps counteracts the effects of available radicals as the channel dimension is scaled down. It is noted that the deep states, which originate from the dangling bonds in the grain boundaries, influence the threshold voltage and the subthreshold swing. However, tail states, which originate from the intra-grain defects, affect the field-effect mobility and the minimum leakage current [4.14]. The SiN-100nm exhibits significant improvements in threshold voltage and mobility compared to the control sample, implying a successful reduction in the trap densities of both deep states and tail states. On the other hand, the SiN-200nm exhibits comparable performance to the SiN-100nm, implying comparable improvements in threshold voltage and mobility. Thus, the trap passivation by hydrogen-containing nitride becomes saturated beyond a critical thickness, since it is difficult for the hydrogen located in the additional thickness of the nitride to diffuse into the poly-Si channel.

In order to investigate the effect of LPCVD-TEOS buffer layer on the efficiency of trap passivation, a thin TEOS buffer layer (denoted as TEOS-10nm or TEOS-20nm) was deposited prior to the SiN deposition. Figures 4-5(a) and 4-5(b) display the threshold voltage as a function of width and length, respectively. Figures 4-6(a) and 4-6(b) show the mobility as a function of width and length, respectively. It can be seen that the TEOS-10nm, TEOS-20nm, and SiN-200nm exhibit comparable performance. These results indicate that a thin TEOS buffer layer cannot retard the hydrogen diffusion, resulting in a comparable improvement in the threshold voltage and mobility. However, T. I. Tsai et al. proposed that a thin TEOS-7nm is effective in blocking hydrogen into channel during LPCVD deposition in single-crystal MOSFETs [4-15]. A possible cause is the significant impact of the grain boundaries, in addition to the interface states. Both the available radicals and the number of defects affects the efficiency of passivating defects. Due to the higher defect density of poly-Si, hydrogen passivation becomes more efficient than in single crystal devices, leading to the ineffective retardation of hydrogen diffusion.

4.3.2 Hydrogen Instability Induced by Post Annealing

For some TEOS-10nm wafers, the capping SiN were deliberately stripped after SiN deposition (denoted as SiN-removed split). This is used to evaluate the impacts of the sequential thermal process on the passivation of the dangling bonds and the intra-grain defects with/without the capping SiN. This study presents the characteristics of threshold voltage, mobility, I_{Dmin} leakage, and activation energy to systematically investigate the hydrogen instability induced by post annealing. Figures 4-7(a) and 4-7(b) demonstrate the threshold voltage as a function of width and length, respectively. Figures 4-8(a) and 4-8(b) show the mobility as a function of width and length, respectively. The SiN-removed reveals threshold voltage and mobility characteristics comparable to those of the control sample. This implies that post annealing breaks both the passivation of the dangling bonds and the intra-grain defects by hydrogen, which in turn decreases the improvement in threshold voltage and mobility. By the same token, the comparison shows that the SiN capping layers can strengthen the immunity against the post annealing, due to the suppression of hydrogen outgassing during post annealing.

Figure 4-9 shows the drain-current-vs-drain voltage (I_D-V_D) characteristics of all

n-channel poly-Si TFTs. The TEOS-10nm exhibits significantly better performance than the control sample due to a reduction in the tail state density. The SiN-removed exhibits a performance comparable to that of the control sample, indicating that the Si-H bonds, which affect the electrical properties, break completely.

Figure 4-10(a) and 4-10(b) show the characteristics of minimum current. The strong dependence of minimum leakage observed on V_G vs. V_D indicates that trap-to-trap tunneling dominates, which depends on the deep state density and local electric field [4-16]. Although all samples exhibit comparable I_{Dmin}, the gate voltage corresponding to minimum current at fixed drain bias for the SiN-removed sample is different from the TEOS-10nm sample, since the post annealing process also breaks the passivation of traps, which is associated with the leakage current. On the other hand, the V_{GD} dependence for the SiN-removed sample and the control sample are comparable, meaning the same quantity of traps associated with the leakage current.

The temperature dependences of the drain current of the control sample, the TEOS-10nm, and the SiN-removed were also measured in the temperature ranges from 25℃ to 125℃. At V_D=0.1V, using the linear fitting of the ln(I_D) versus the 1/KT plot, where K is the Boltzmann constant and T is the absolute temperature, the activation energy E_a of the drain current at different gate biases is deduced as shown in Fig. 4-11 [4.17]. It can be seen that the TEOS-10nm have lower E_a than the SiN-removed and the control sample. It also confirms that trap states in the channel are passivated by hydrogen for the sample capped SiN. However, post annealing breaks the passivation of traps for the samples without SiN capping. The calculated conductance activation energy correlates well with corresponding measurements of threshold voltage, mobility, and leakage current. Thus, we believe that post annealing makes the SiN-removed sample suffer from hydrogen instability, resulting in the performance comparable to that of the control sample.

4.3.3 Hot Carrier Stressing, PBTI, and NBTI

As mentioned previously, hydrogen release occurs in the SiN-removed sample during post annealing, resulting in a performance comparable to the control sample. Within this observation, one may assume that the SiN-removed sample will exhibit the reliability comparable to that of the control or TEOS-10nm samples. This section presents the hot carrier stressing, PBTI, and NBTI results in detail. We found that

reality is completely different from our expectations.

Figure 4-12 shows the dependence of dc hot-carrier degradation at a drain voltage (V_D) of 23-V on gate voltage V_G after 1000s for all samples, where I_{on} is a drain current (I_D) at V_g of 18V and V_D=0.1 V, and the degradation rate is defined as $\Delta I_{on}= (I_f - I_i) /I_i$. As expected, the TEOS-10nm sample exhibits the worst degradation of I_{on} at V_G=4V of all samples. This is attributed to the break of Si-H during hot carrier stressing, although trap passivation by hydrogen makes the poly-Si TFTs exhibit better performance initially [4-18]. Moreover, it can be seen that removing the SiN before post annealing can alleviate the degradation at lower V_G, since the post annealing breaks the Si-H.

Figure 4-13 shows the time dependence of threshold voltage shift ΔV_{th} of the n-channel TFTs after the PBTI stress with $V_G = 19V$ and $V_D = V_S = 0V$ for 30000s at $T = 25^oC$. BTI degradation was evaluated by the conventional method in which I_D-V_G curves are measured during stress interruption. It can be seen that the increase in the ΔV_{th} of the SiN-removed is higher than that of the TEOS-10nm and the control sample, implying a raised defect density.

Figure 4-14 shows the time dependence of the threshold voltage shift ΔV_{th} of the n-channel TFTs after the NBTI stress with $V_G = -19V$ and $V_D = V_S = 0V$ for 30000s at $T = 25^oC$. The control sample and TEOS-10nm sample exhibit increasing threshold voltage after NBTI stressing, but the SiN-removed sample exhibits decreasing threshold voltage. Further,, the insignificant degradation of the subthreshold swing indicates insignificant negatively-charged ΔQ_{it}(not shown here) [4-19]. Thus, the different dominant charge trappings are responsible for the different immunities of the NBTI, implying different oxide quality and channel conditions [4-20]. As a result, the control sample and the SiN-removed sample exhibit different immunity to NBTI stressing, although their original performances are comparable. It is known from the literature that the interface between the poly Si channel/gate oxide exhibits better quality than the interface between the poly Si gate/gate oxide [4-21]. The non-ideal interface between poly-Si gate/gate oxide results in the significant electron injection from poly-Si gate under negative bias stressing. On the other hand, the hydrogen release degrades the interface between poly-Si channel/gate oxide, and the hole injection from the poly-Si channel becomes higher than the electron injection from poly-Si gate, as a result.

At constant gate voltage, an elevated temperature can create a build-up of positive charges in the oxide layer, which in turn decreases device performance. Figure 4-15 shows the degradation rate at elevated temperature for 1000s. This figure shows that the shift of threshold voltage becomes more negative at elevated temperatures, and the temperature dependence is significant for the SiN-removed sample.

The data from the hot carrier stressing, PBTI and NBTI shows a good reproducibility from the devices of the same batch. Whether or not buffered TEOS oxide is used, the capping SiN samples exhibit comparable characteristics of reliability (not shown here), but hydrogen release significantly affects the reliability of the SiN-removed samples. Impurities or strain relaxation can induce defects that affect the trapping charge efficiency and degrade the threshold voltage[4-22]. This study shows that hydrogen release has an effect on the charge trapping efficiency.

Based on our results, there are two possible mechanisms for the increase in pre-existing defects in the SiN-removed sample. The first mechanism is the hydrogen or hydroxide group, which does not affect the original performance as strongly as the control sample, inducing traps, preexistent to the stress or created during the stress in the gate oxide[4-22][4-23]. The second possible cause is the out-diffusion of hydrogen released from the intra-grain or grain boundary, since such hydrogen migration may generate defects, such as platelets, H_2-defects, and vacancies in poly-Si channel [4-24][4-25].

As a result, capping SiN for applications such as hard mask, spacer, and gate dielectric, would suffer from hot carrier stressing, although the capping SiN makes significant improvement in mobility and threshold voltage. Moreover, samples with the SiN capping layer removed subsequently can alleviate the degradation by hot carrier stressing, but hydrogen release would reduce the immunity of PBTI and NBTI.

4.4 Summary

This chapter investigates the passivation efficiency of hydrogen by hydrogen-containing nitride, based on the comparison of different thicknesses of SiN or inserted TEOS oxide. As a result, the trap passivation by hydrogen-containing nitride becomes saturated beyond a critical thickness of SiN, and inserting TEOS oxide cannot retard the hydrogen diffusion. Moreover, we investigate the effects of hydrogen instability induced by post annealing on device performance and reliability.

For the SiN-removed sample, post annealing decreases the improvements of defect passivation. Devices with a SiN capping layer can suppress outgas of hydrogen while retaining the improvement in mobility and threshold voltage.

Furthermore, samples with capping SiN suffer from hot carrier stressing, although capping SiN offers significant improvement in mobility and threshold voltage. Samples with SiN capping layers removed subsequently can alleviate the degradation by hot carrier stressing. However, hydrogen release reduces the immunity of PBTI and NBTI. Samples experiencing hydrogen release exhibit the worst degradation of PBTI. For NBTI concerns, the dominant degradation mechanism of the threshold voltage of the SiN-removed sample is the hole trapping rather than the electron trapping, which is the mechanism the control sample and the capped SiN sample suffer. Two possible mechanisms can explain the increased pre-existing defects that affect the hot carrier stressing, NBTI, and PBTI.

- **500-nm thermal oxide**
- **50-nm undoped amorphous Si layer**
- **Crystallization at 600^{o} C for 24hr**
- **Active Region patterning**
- **30nm TEOS oxide**
- **200nm poly-Si gate**
- **Gate patterning**
- **The S/D regions were implanted with phosphorous and activated at 600 ˚C for 24 h.**
- **10nm or 20nm TEOS oxide deposition**
- **100nm or 200nm SiN deposition at 780^{o} C**
- **Removed 200nm SiN**
- **500nm TEOS oxide deposition**

split / process	control	SiN-100nm	SiN-200nm	TEOS-10nm	TEOS-20nm	SiN removed
SiN 100nm		O				
SiN 200nm			O	O	O	O
TEOS oxide 10nm				O		O
TEOS oxide 20nm					O	
Removed SiN 200nm						O

Fig. 4-1 Process flow and split table

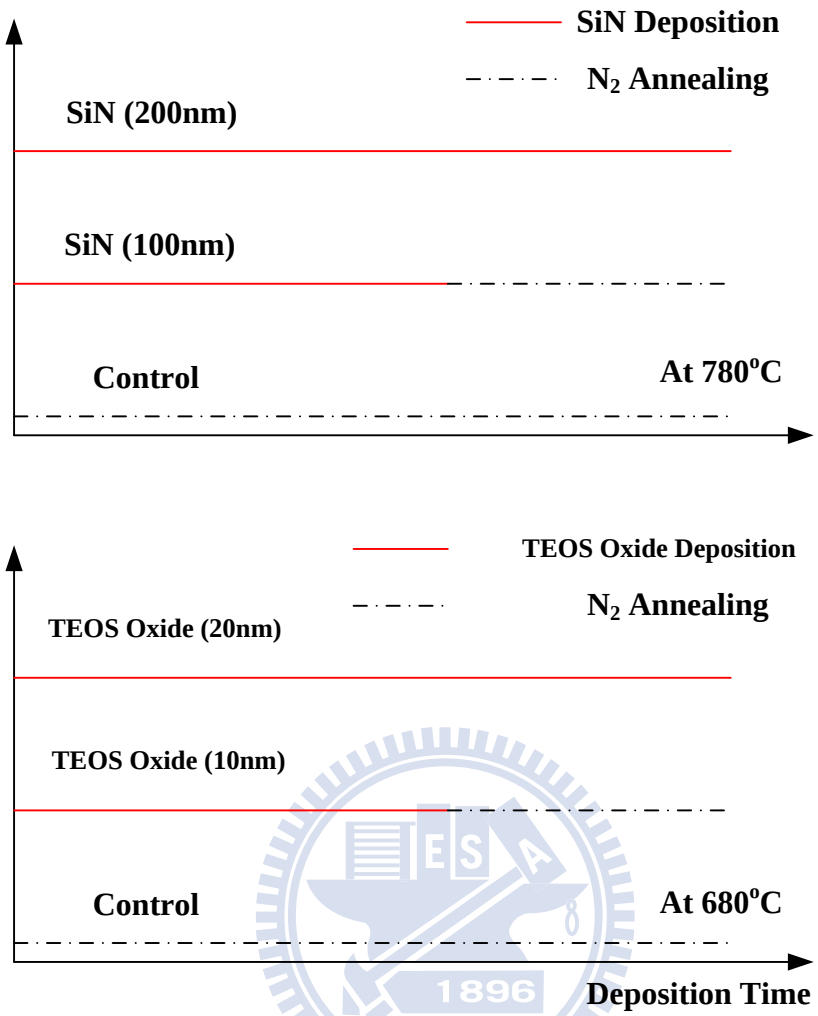
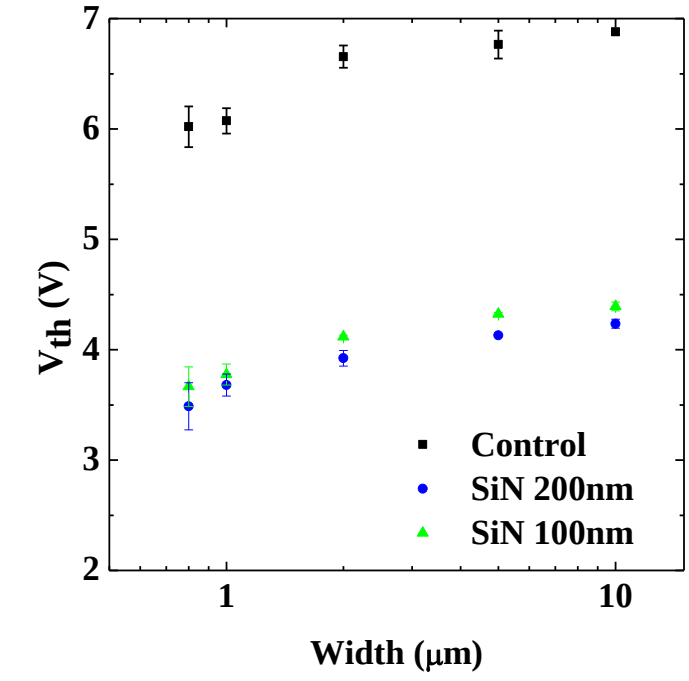
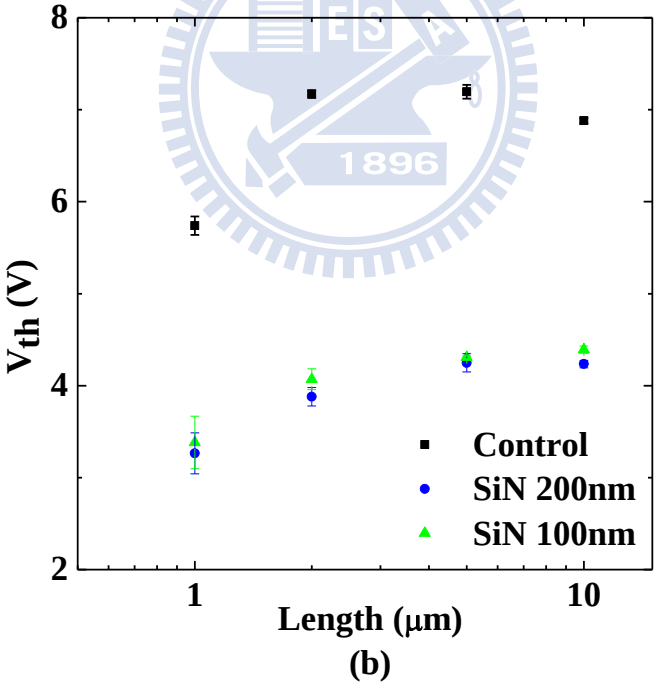


Fig. 4-2 Schematic diagram of three types of deposition process for TEOS oxide or SiN based on the same thermal budget.



(a)



(b)

Fig. 4-3(a) Variation of threshold voltage as a function of channel width for sample with $L = 10\mu m$ capped thickness of SiN capping. Fig. 4-3(b) Variation of threshold voltage as a function of channel length for sample with $W = 10\mu m$ capped different thickness of SiN capping.

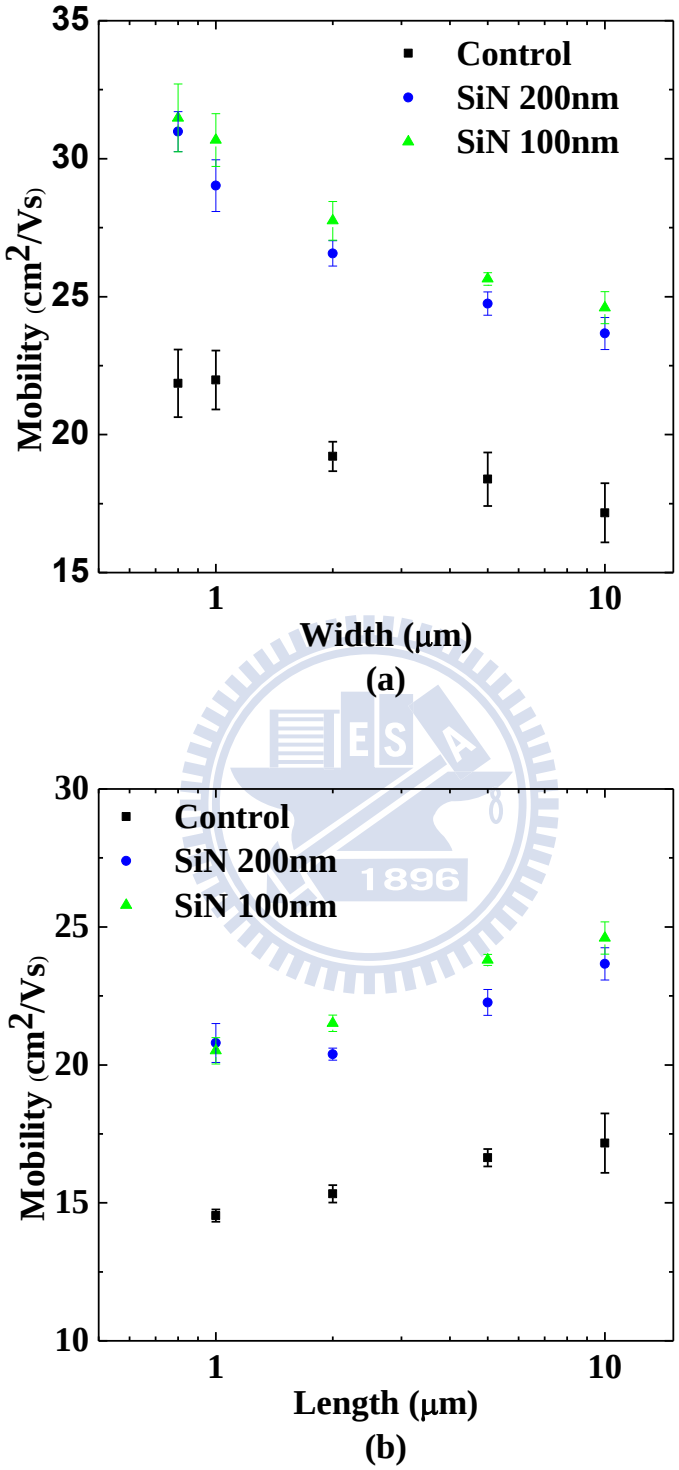
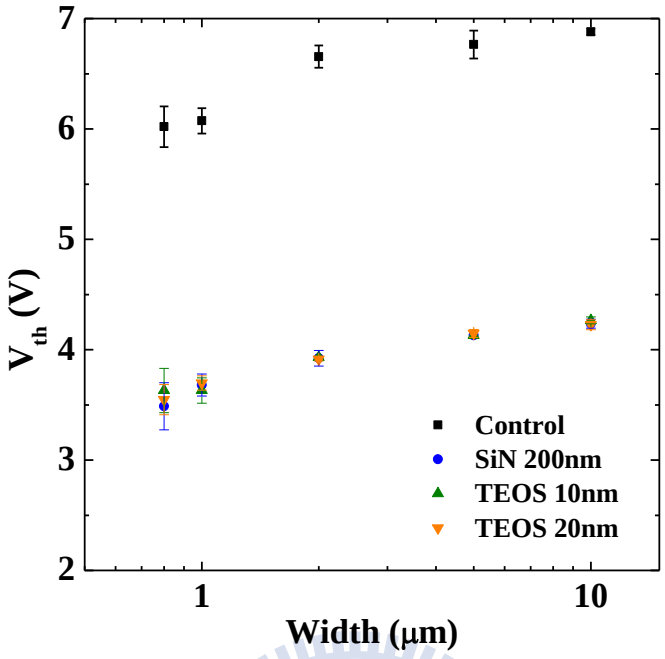
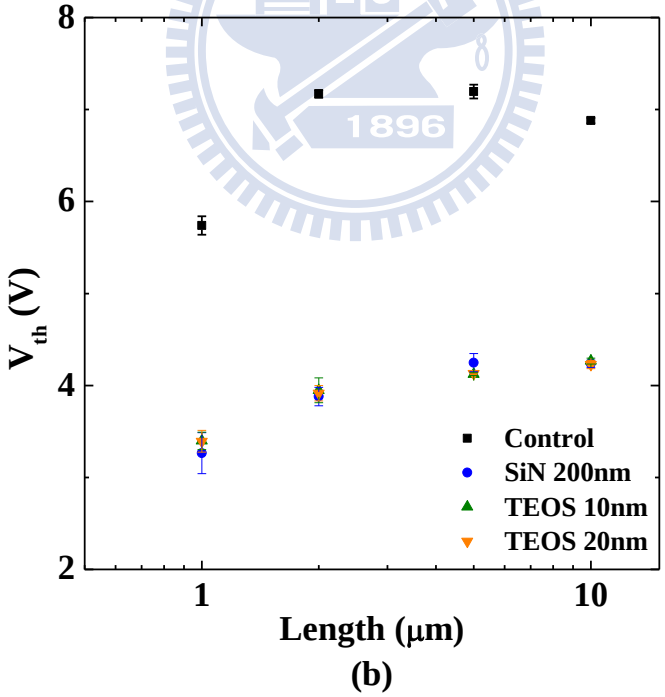


Fig. 4-4(a) Variation of mobility as a function of channel width for sample with L = 10μm capped different thickness of SiN capping. Fig. 4-4(b) Variation of mobility as a function of channel length for sample with W = 10μm capped different thickness of SiN capping.

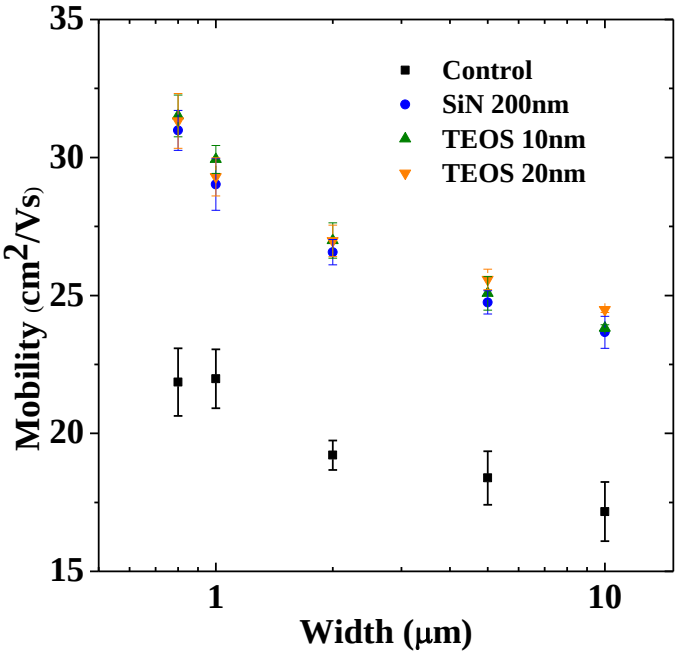


(a)

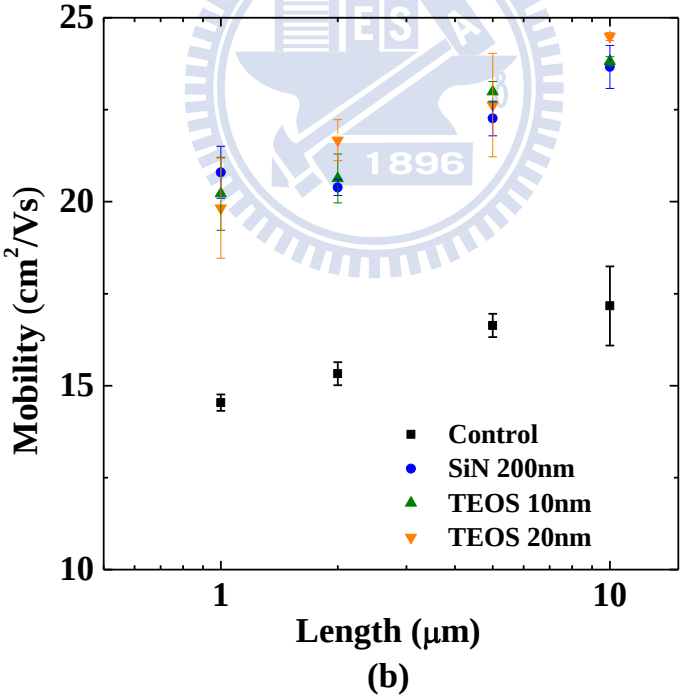


(b)

Fig. 4-5(a) Variation of threshold voltage as a function of channel width for sample with $L = 10\mu m$ capped different thickness of TEOS oxide capping. Fig. 4-5(b) Variation of threshold voltage as a function of channel length for sample with $W = 10\mu m$ capped different thickness of TEOS oxide capping.



(a)



(b)

Fig. 4-6(a) Variation of mobility as a function of channel width for sample with L = 10μm capped different thickness of TEOS oxide capping. Fig. 4-6(b) Variation of mobility as a function of channel length for sample with W = 10μm capped different thickness of TEOS oxide capping.

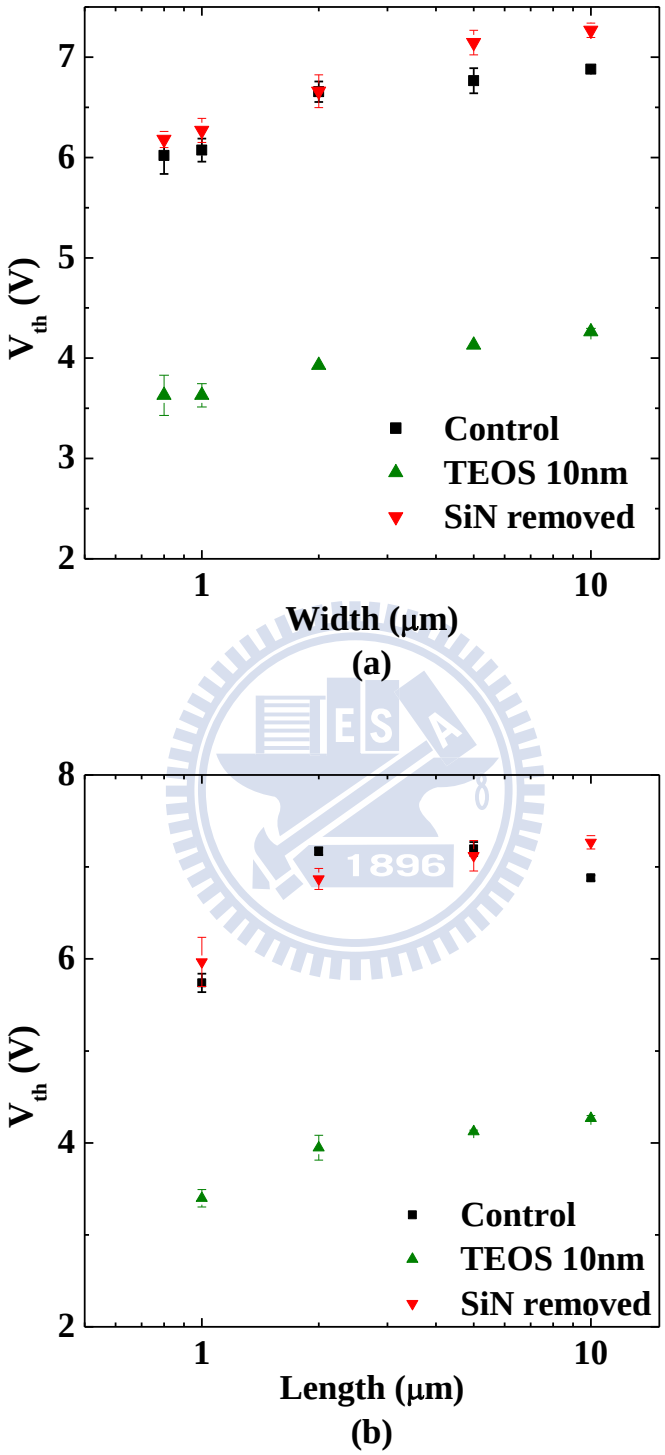
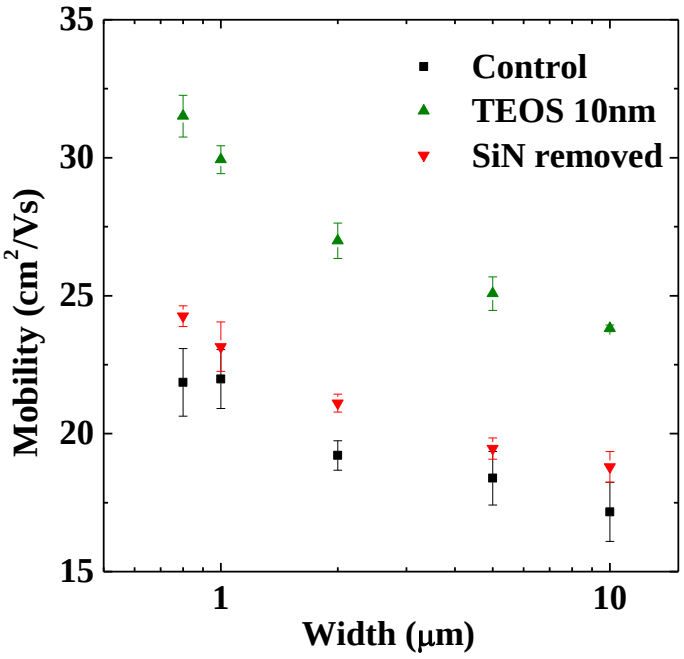


Fig. 4-7(a) Variation of threshold voltage as a function of channel width with L = 10μm for the control sample, the nitride capped sample, and the nitride removed sample. Fig. 4-7(b) Variation of threshold voltage as a function of channel length with W = 10μm for the control sample, the nitride capped sample, and the nitride removed sample.



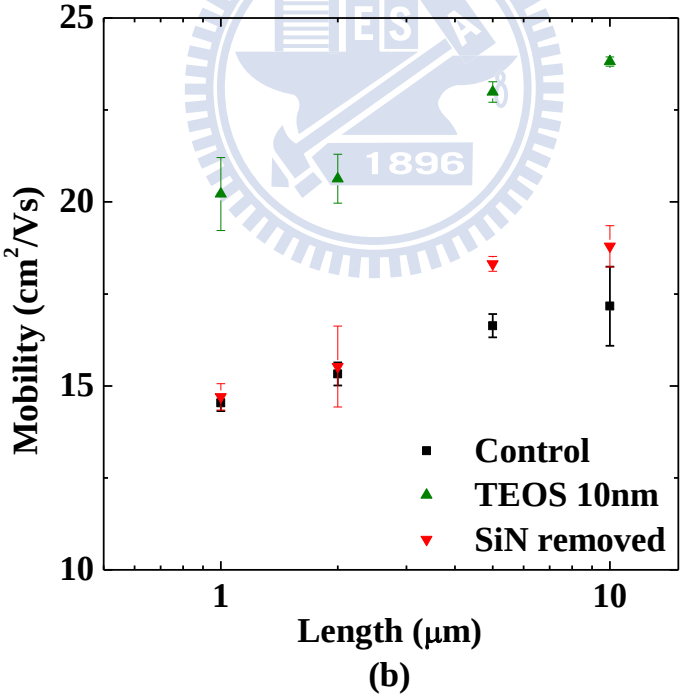


Fig. 4-8(a) Variation of mobility as a function of channel width with $L = 10\mu m$ for the control sample, the nitride capped sample, and the nitride removed sample.

Fig. 4-8(b) Variation of mobility as a function of channel length with $W = 10\mu m$ for the control sample, the nitride capped sample, and the nitride removed sample.

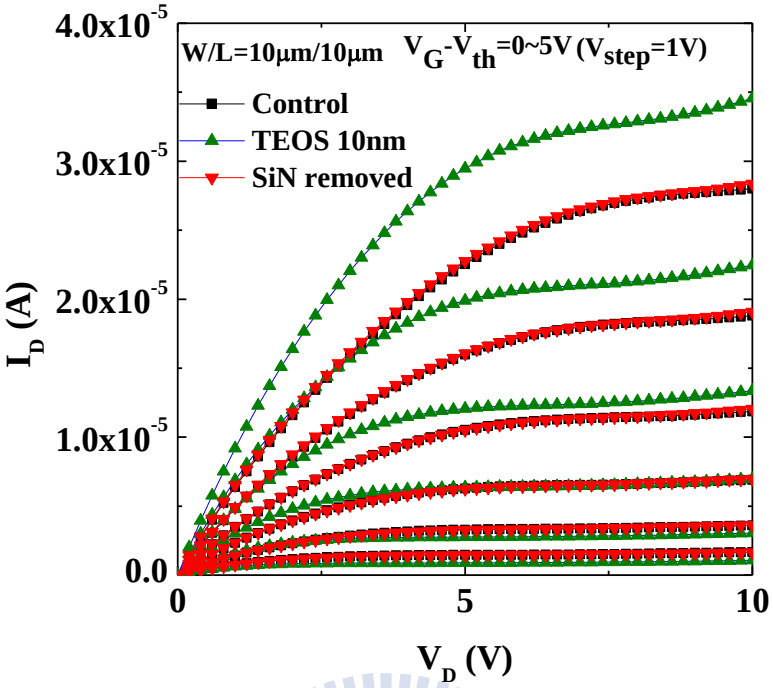
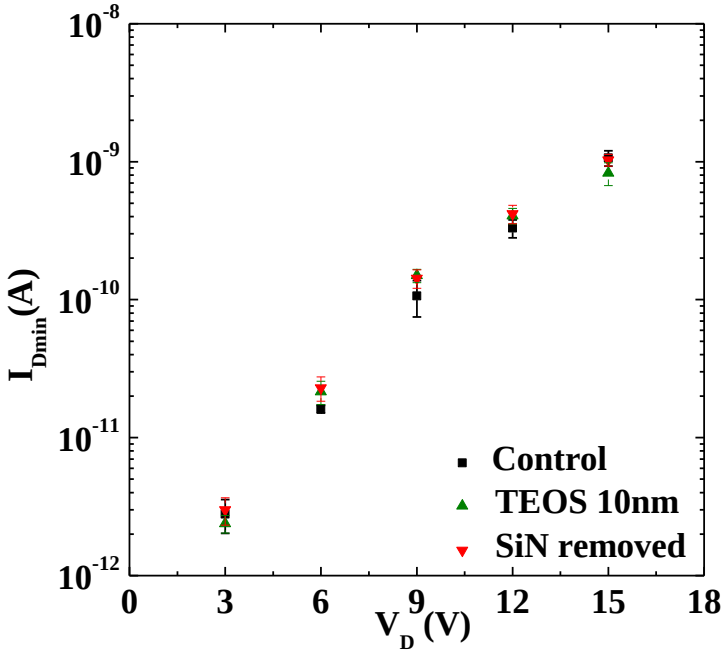
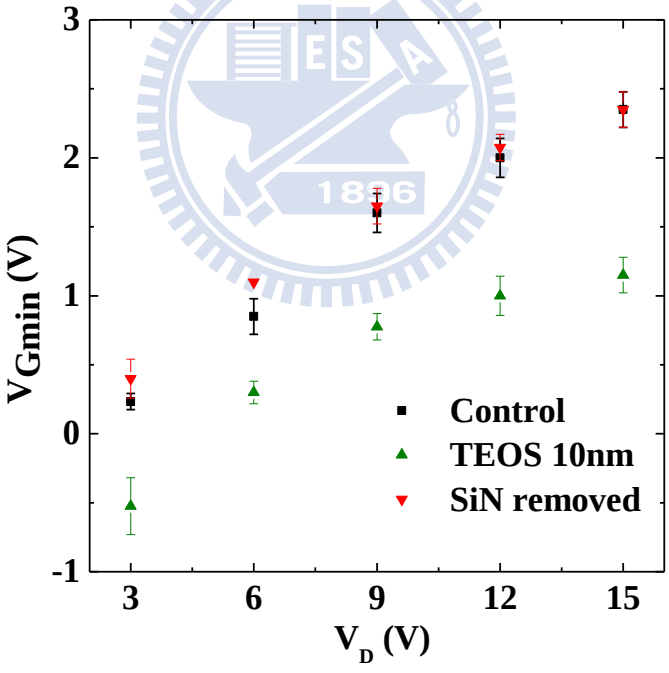


Fig. 9

Fig. 4-9 Output characteristics (the I_D-V_D curve) of n-channel TFTs with $W/L = 10\mu m/10\mu m$ for the control sample, the nitride capped sample, and the nitride removed sample.



(a)



(b)

Fig. 4-10(a) The minimum current for the control sample, the nitride capped sample, and the nitride removed sample. Fig. 4-10(b) The gate voltage corresponding to minimum leakage current at fixed drain bias for the control sample, the nitride capped sample, and the nitride removed sample.

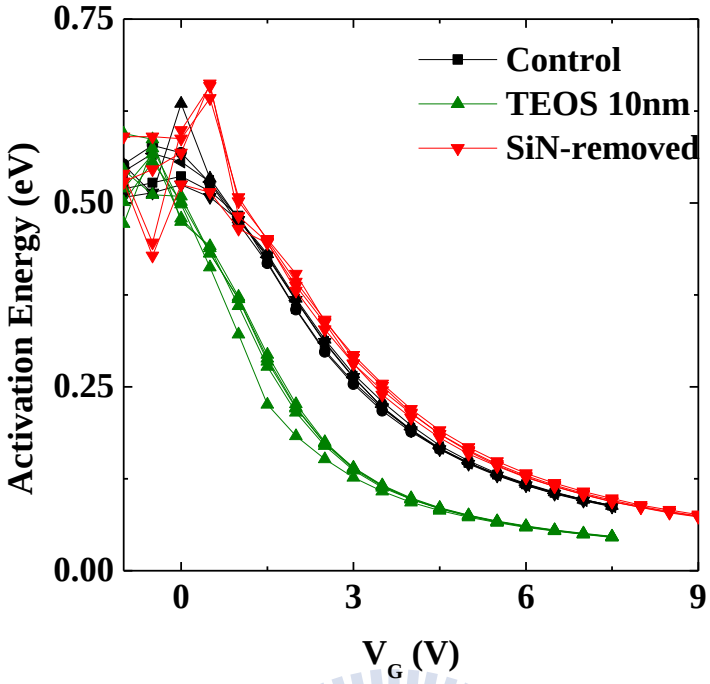


Fig. 4-11 The activation energies of the drain current for the control sample, the nitride capped sample, and the nitride removed sample.

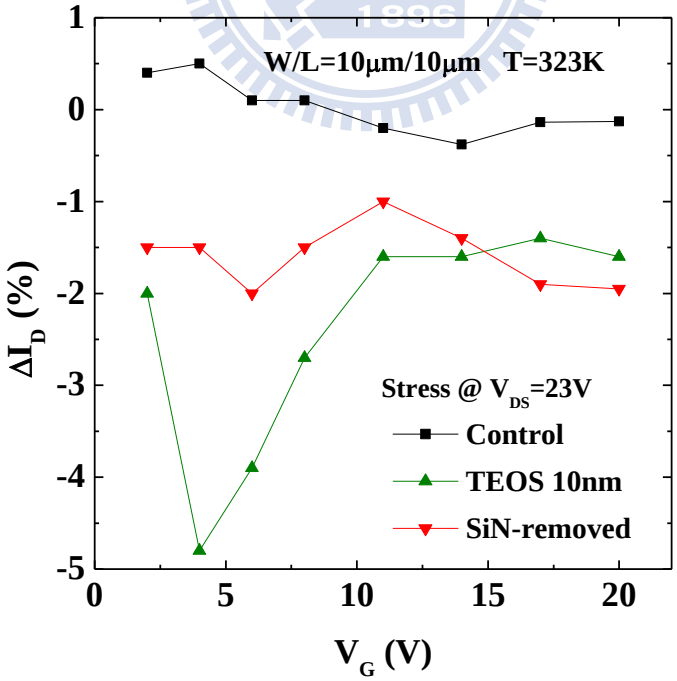


Fig. 4-12 Dependence of I_{on} and Gm degradation under dc stress on gate voltage for the control sample, the nitride capped sample, and the nitride removed sample.

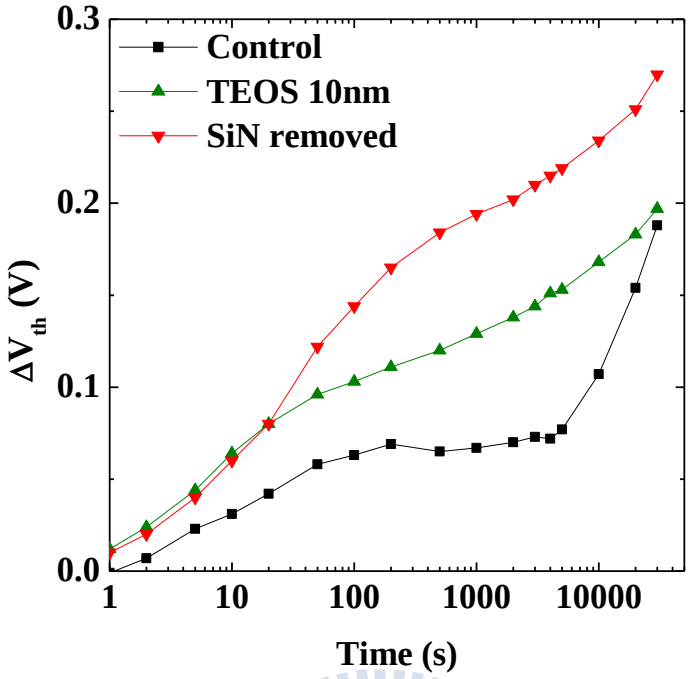


Fig. 4-13 Threshold voltage shift as a function of stress time for the control sample, the nitride capped sample, and the nitride removed sample with $W/L = 10\mu m/10\mu m$ under positive gate bias stress as $V_{GS} = 19V$.

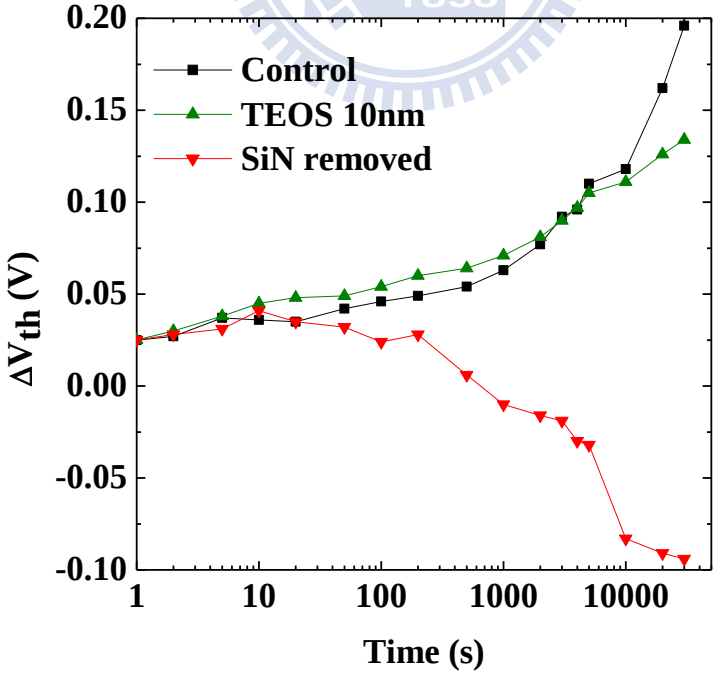


Fig.4-14 Threshold voltage shift as a function of stress time for the control sample, the nitride capped sample, and the nitride removed sample with $W/L = 10\mu m/10\mu m$ under negative gate bias stress as $V_{GS} = -19V$.

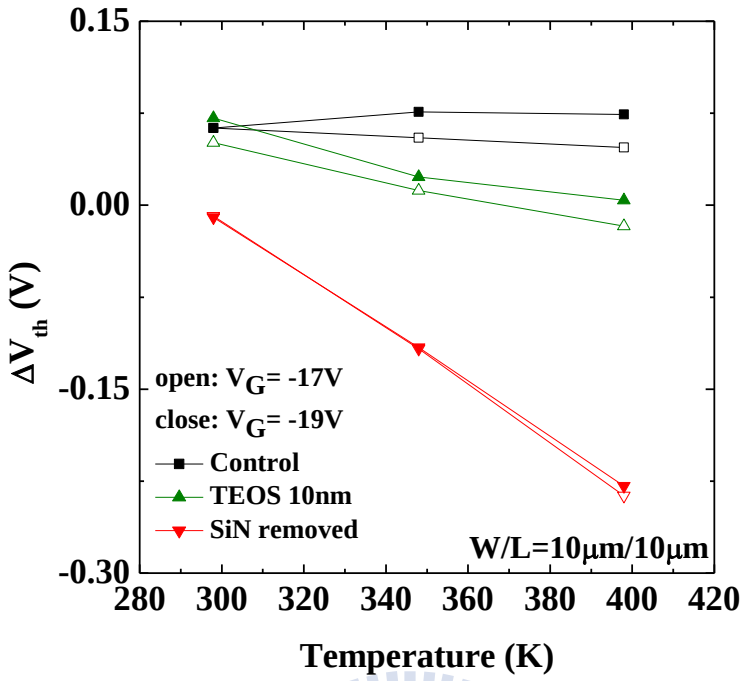


Fig. 4-15 Measurement of NBTI degradation at different temperatures for the control sample, the nitride capped sample, and the nitride removed sample with $W/L = 10\mu m/10\mu m$.

Chapter 5

Impacts of the Underlying Insulating Layer on the SPC and MILC.

5.1 Introduction

Recently, polycrystalline silicon (poly-Si) thin film transistors (TFTs) have attracted attention, due to their potential applications in active-matrix liquid crystal displays (AMLCDs) and high density vertically components [5.1]-[5.2]. SiN is one of the promising materials for sealing substrate against the process chemical, the outstanding adhesion, and the application of the gate dielectric or FinFET fabrication [5.3]-[5.5]. However, its hydrogen release and inherent non-hydrostatic stress may result in some influence on properties of poly-Si TFTs crystallized by SPC. A lot of works have been done for clarifying the influence of the mechanical stress, including the stress applied before the crystallization [5.6] or after the crystallization [5.7]. For the stress applied before the crystallization, the tensile stress increases the growth rate of the crystallization, but the compressive stress retards the growth rate of the crystallization. For the stress applied after the crystallization, the tensile stress would increase the electron mobility, but degrade the hole mobility. Removing the back side layer makes influence on the amorphous silicon transistors, due to the different stress sensitivity [5.8]. This chapter confirms that using the SiN would affect the electrical characteristic and exhibit different temperature dependence on TFTs crystallized by SPC. Also, this chapter presents the influence of removing the back side layer on the electrical characteristics of thin film transistors and provides guidance for further explorations of stress theory for TFT applications.

On the other hand, Metal-induced-lateral-crystallization (MILC) has been studied as a lower temperature alternative to solid-phase crystallization (SPC) of amorphous silicon or amorphous SiGe, due to its high quality poly-Si layer with higher carrier mobility, larger grain size, and lower defect density [5.9].

Although MILC has been a subject of numerous researches, its detailed mechanism still provokes many questions, including the metal sources, the temperature, and the dopant species [5.9]-[5.10]. M. Wong et al. reported that the proximity layer makes influence on the MILC growth rate [5.11]-[5.12]. Although this study proposed a reasonable mechanism (the gettering of Ni take place at the interface between a-Si and buffered layer), M. Wong et al. found this mechanism is not enough

to bridge to the MILC growth rate as the dopant species involves, implying the involvement of another mechanism [5.12].

Moreover, FinFETs, nanowires, and double-gated TFTs crystallized by MILC have also drawn a lot of attention for a number of applications [5.13]-[5.14]. With the advantage of these structures, MILC poly-Si can achieve better performance. Basically, the fabrication flow of these novel structures needs SiN, thermally grown oxide, or TEOS oxide, to serve as the hard mask, the buffered layer, or the spacer before MILC, respectively [5.13]-[5.15]. Thus, clarifying the influences of these proximity layers on the crystallization besides the advantage of the structures of poly-Si TFTs becomes very important.

This chapter presents three commonly used proximity layers for clarifying the impacts of proximity layers on MILC rate and electrical characteristics of p-channel TFTs. Again, in order to avoid other mechanisms involves in the carrier transportation (e.g., different mechanisms of scattering and charge trapping based on different gate oxide or spacer), which are not the scope of this chapter, only different buffered layer are studied for clarifying the impact of proximity layer.

5.2 Experiment

5.2.1 Device Fabricated by SPC

The polysilicon TFT studied in this work were prepared as shown in Fig. 5-1: wafers with 500nm-thick thermally grown oxides were used as the substrate. Silicon nitride of a thickness approximately 100 Å or 1500 Å was deposited by low-pressure chemical vapor deposition (LPCVD) on some wafers (samples C, D, E, and F). A 500Å amorphous silicon (a-Si) film was deposition at 500℃ by LPCVD for all samples. The backside layer of amorphous silicon was removed from part of the samples (samples G and H). In order to examine the influence of annealing temperature, 580℃ and 600℃ for 24 hours were adopted to transform the a-Si film into poly-Si. Poly-Si films were patterned into active islands. In this chapter, all devices investigated have a gate width/length dimension of 10/10 (μm/μm).

5.2.2 Device Fabricated by MILC

Fabrication of the underlying insulating layers (proximity layer) was started by capping a 500-nm-thick thermal oxide layer or the TEOS oxide layer on 6-in silicon

wafers. A number of wafers with thermal oxides, namely inserted SiN, were deposited as 150nm SiN by low-pressure chemical vapor deposition (LPCVD) as a stacked double layer for investigating the impact of the SiN proximity layer. Then, a 50-nm-thick a-Si thin film was deposited by LPCVD on all wafers. A 5-nm-thick Ni thin film was selectively deposited using an electron gun evaporator on a-Si film using the lift-off process as shown in Fig. 5-2. The wafers were heat-treated at 550℃ in an N_2 ambiance for 24h to laterally crystallize the channel region where the nickel thin film was not deposited. All unreacted Ni was subsequently removed in an H_2SO_4 solution. A 500-nm-thick plasma-enhanced chemical vapor deposition (PECVD) oxide was deposited at 300℃ for device isolation. The oxide was then patterned and etched to define the active region of the device. The source and drain region were implanted with BF_2 (15keV at 5E15cm^{-2}) and activated at 600℃ for 24-h annealing in an N_2 ambiance. A 30-nm-thick oxide was deposited at 300℃ by PECVD as the gate oxide. After patterning of contact holes, aluminum was deposited by PVD and patterned as the probe pads to complete the TFT devices.

The devices were annealed at 350℃ for 1h. Other than post-annealing, no other hydrogenation process was performed for investigating the intrinsic behavior of the devices.

5.3 Results and Discussions

5.3.1 Impacts of SiN and Backside Amorphous Silicon on Poly-Si TFTs

Fig. 5-3 shows the stress characteristics of sample G and sample H, those backside a-Si films were removed before crystallization, and re-crystallized at temperature of 580℃ for G-sample and 600℃ for H-sample, respectively. Stress induced by a-Si film was calculated from wafer's curvature. The a-Si film, as deposited near 500℃, induces compressive stress for both samples. After the crystallization of the a-Si film during 580℃ (G-sample) and 600℃ (H-sample) for 24 hours, the residual stress changes into tensile stress. Thus, the crystallization process alters the residual stress, meaning that removing the backside a-Si as well as its stress before crystallization may influence the electrical characteristics of poly-Si TFTs fabricated on the front side of the wafer. Fig. 5-4 and Fig. 5-6 show the characteristics of threshold voltage, which was defined as the gate voltage to achieve a normalized

drain current of $I_D = (W/L) \times 100nA$ at $V_{DS} = 0.1V$. Fig. 5-4 shows the threshold voltage for samples deposited on the thermally oxidized silicon wafer (samples A, B, G, and H), and samples possess larger grain size crystallized at 580℃ with lower deep state density [5.4], is responsible for lower threshold voltage compared to the samples crystallized by 600^{o}C [5.16]. Removal of the back side layer, samples G and H, as well as the tensile stress before crystallization would retard the growth rate of the crystallization and generate a higher deep state density Fig. 5-5, consequently resulting in a higher threshold voltage than samples A and B.

On the other hand, the temperature dependence of threshold voltage is different for samples fabricated on the SiN proximity layer for samples C, D, E, and F. Not only the different stress interactions, but also the formation of seed nuclei by hydrogen or traps passivated by hydrogen and nitrogen are responsible for this different temperature dependence [5.17], which reported that the hydrogen can promote of the nuclei formation, resulting in a smaller grain size of the channel poly-Si as well as a higher threshold voltage. However, the releasing hydrogen would passivate the trap states in the grain boundary, leading to smaller threshold voltage. These mechanisms, which are sensitive to the annealing temperature, are reasonable to affect the temperature dependence. The Fig. 5-7 shows the I_D-V_D characteristics, and using 600℃ annealing achieves higher performance than 580℃ annealing, meaning that higher annealing temperature is more effective in reducing density of tail state (originated from strain bonds). We believe that strain bonds which are associated with dislocation and microtwins would decrease after higher temperature annealing, resulting in lower tail state as well as higher mobility. Fig. 5-8 and Fig. 5-9 demonstrate the immunity of positive gate bias stress (PGBS), and the initial formation of positive charge followed by a gradual negative charge buildup is consistent with previous result [5.18]. Also, the increasing deep state induced by removing backside layer would increase the formation of positive charge. Thus, not only oxide quality, but the poly-Si affects the immunity of PGBS [5.2].

Moreover, we investigated the minimum current as shown in Fig. 5-10 and Fig. 5-11. The strong observed dependence of the leakage on V_{Gmin} and V_D implies that trap assisted GIDL dominates, which depends on the deep state density and the local electric field. For the sample deposited on the oxidized silicon wafer, which was crystallized by lower temperature, exhibits lower leakage. Removal of the backside a-Si exhibits a lower I_{Dmin} leakage at higher V_D compared to the control sample, this

observation can be possibly ascribed to the following explanations. The higher trap state inducing peak electric field lowering maybe responsible for suppressing trap-to-trap tunneling for samples without the backside a-Si [5.19]. (Advanced studies are planned). Fig 5-12 shows the leakage of samples with inserted SiN. The density of the deep state is dominant to explain the features of leakage at lower V_D；However, samples crystallized by higher temperature possess higher minimum leakage at higher V_D. We believe that this observation can be possibly ascribed to the decreasing electric field induced by higher trap density.

5.3.2 Impacts of Proximity layer on the MILC Growth Rate and Electrical Characteristics

Ni-Induced MIC of a-Si occurs through a three-step process: silicide formation, breakup of the silicide layer into small nodules, and transport of the silicide nodules through the a-Si film. At the edge of an Ni-covered region, a certain number of the breakaway $NiSi_2$ nodules move laterally into the a-Si region not originally covered by Ni. As the nodules move laterally, any a-Si along the path of the moving nodules are crystallized during the MILC process [5.9]. According to this theory, the growth model of MILC does not reveal the dependence of MILC growth length on the proximity layer.

Fig.5-13 shows the relation between MILC growth length and different underlying insulating layers. The region crystallized by MILC was identified with optical microscopy, as shown in the inset. Using TEOS oxide achieves the fastest growth length (~52.5 μm), and using inserted SiN exhibits the slowest growth length (~42 μm). Three possible mechanisms could be responsible for the dependence of MILC growth length on the underlying insulating layers. The first mechanism proposed by Wong et al. is that Ni gettering occurs at the interface between a-Si and a buffered layer, meaning that the different interface between a-Si and a buffered layer would generate different gettering sites of Ni [5.1].The second mechanism is the effect of stress on lateral growth behavior during MILC. Tensile stress enhances the breakage of Si-Si bonding, and increases the number of absorbing Si atoms at the front of the $NiSi_2$/a-Si interface. This tensile stress also generates more vacancies in the $NiSi_2$ precipitates, and these vacancies raise the diffusion rate of Ni atoms through

$NiSi_2$. Consequently, the tensile stress enhances MILC growth length, whereas the compressive stress retards it[5.20]. Thus, the stress of the underlying insulating layer is reasonable to affect MILC growth length. This stress may originate from the different coefficients of thermal expansion between the a-Si and proximity layer, the different lattice constants of various films, and intrinsic stress caused by film shrinkage, though the realistic stress interaction is difficult to gauge[5.21]. We believe that the higher compressive stress (-312Mpa) of the wet oxide could explain the lower MILC growth length, compared to the growth length of the TEOS oxide (-52Mpa). The third possible cause is the out-diffusion of the released hydrogen from the underlying insulating layer, such as SiN, because the MILC growth length of the H_2-doped sample was retarded[5.10]. The higher H content signifies a film with less dangling bonds in amorphous Si, leading to a lower MILC growth length. We believe that the released hydrogen from SiN as shown in figure 5-14 would counteract the effects of tensile stress(1.2Gpa), resulting in the slowest growth length.

Fig.5-15 displays the I_D-V_G curves of a p-channel TFT, and shows that using different underlying insulating materials results in a substantial impact on the electrical characteristics because of the different crystallization conditions and channel/bottom oxide interface. Fig.5-16 demonstrates the threshold voltage and subthreshold swing. The threshold voltage (V_{th}) is defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L) \times 100nA$ at $V_{DS} = 0.1V$. Figs. Fig.5-17 and 5-18 demonstrate the field-effect mobility and output characteristics (the I_D-V_D curve).The deep states that originate from the dangling bonds in grain boundaries influence the threshold voltage and subthreshold swing, whereas tail states, which originate from intra-grain defects, affect field-effect mobility [5.22]. Kim et al. proposed that a higher MILC growth rate may generate lower trap density in the poly-Si channel [5.10]. However, they did not catalogue the types of defects or verify this theory with any electrical characteristics of transistors. The inserted SiN sample exhibits the lowest mobility, the worst output characteristics, and the highest threshold voltage, correlating well with the slowest MILC growth length. In contrast, the TEOS oxide sample exhibits superior mobility, though with a slightly higher threshold voltage and subthreshold swing, compared to the wet oxide sample. Therefore, the underlying insulating layers affect not only MILC growth length, but also the electrical characteristics.

5.4 Summary

In this chapter, we investigated the impacts of SiN and removal of back side layer on the deep state, the tail state, and the minimum leakage current on TFTs. As a result, the sample without a-Si on the back side exhibits higher V_{th} and lower I_{Dmin}. On the other hand, TFTs with poly-Si on the SiN exhibit different temperature dependence, due to the releasing hydrogen from SiN. Furthermore, the samples with higher trap density may exhibit lower I_{Dmin} at higher V_{DS}, because the decreasing peak electric field would counteract the contribution of trap density.

Moreover, this chapter clarified the effects of underlying insulating layers on MILC growth length and electrical characteristics. Three possible mechanisms can be used to explain the dependence of MILC growth length on the proximity layer. In addition, other than the difference in MILC growth length, the underlying insulating layers affect threshold voltage and mobility. Based on the comparison among underlying insulating layers, using SiN not only retards MILC growth length the most, but also exhibits the worst threshold voltage and mobility. Therefore, we believe that the three probable mechanisms, which can be affected by the dopant, annealing, and different fabrication processes, can provide guidance for further examinations on the effects of the proximity layer.

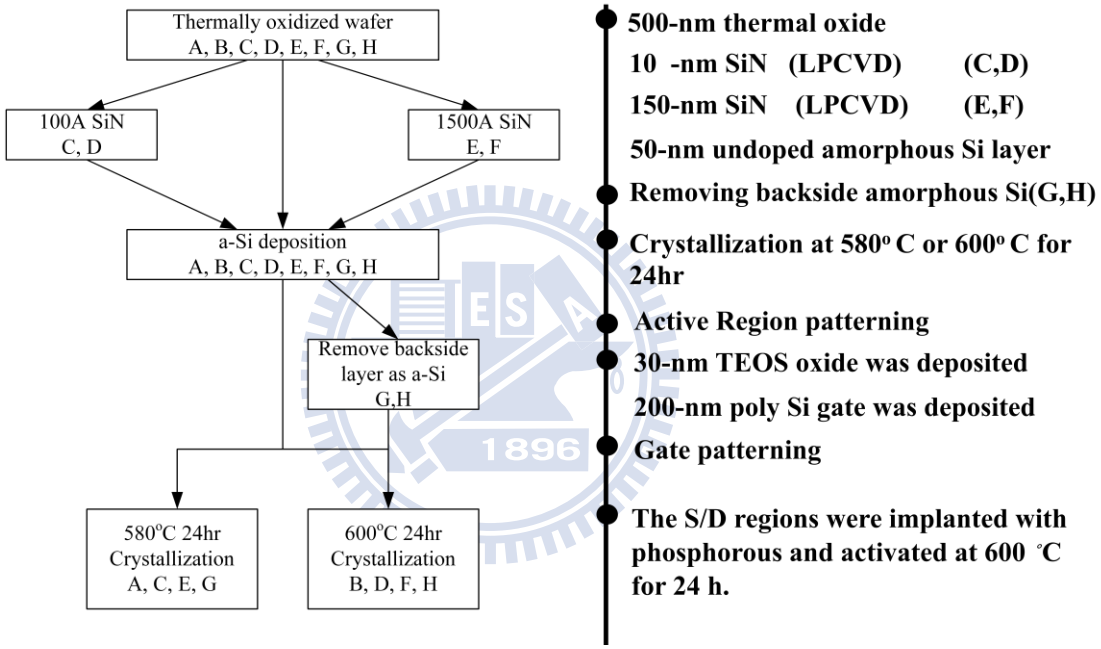


Fig. 5-1 Schematic of the proposed process.

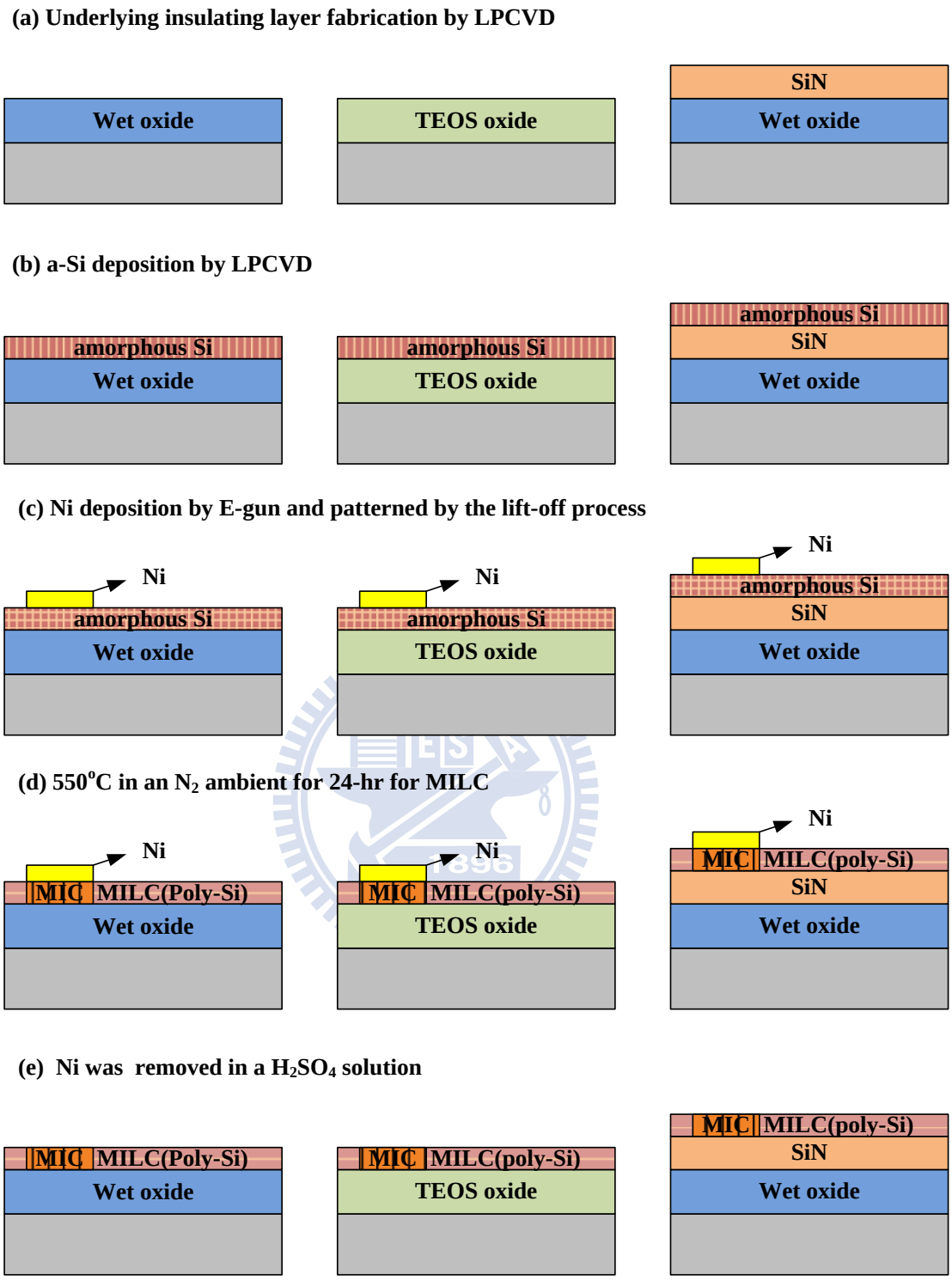


Fig. 5-2 Schematic diagram of MILC process.

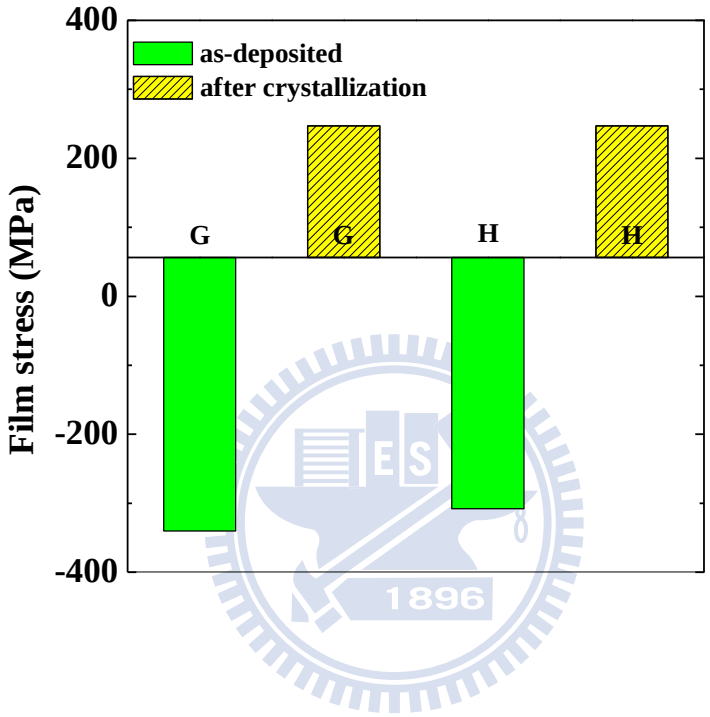


Fig. 5-3 Residual stress change in amorphous silicon thin film.

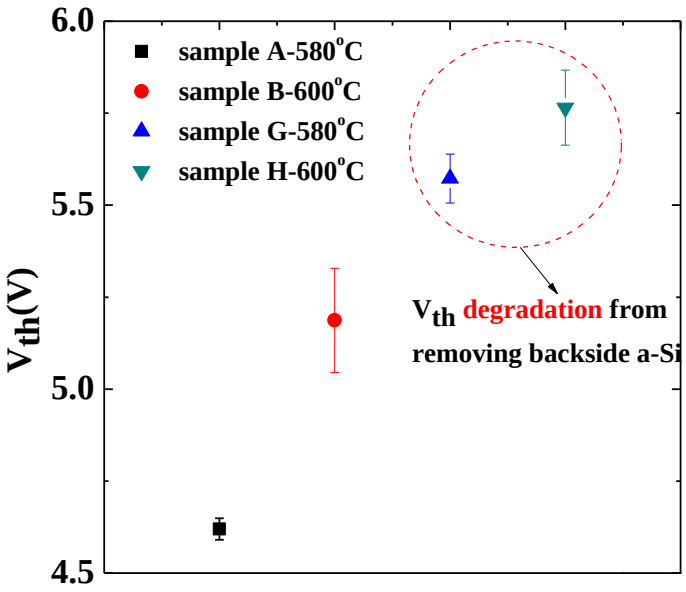


Fig. 5-4 Threshold voltage for samples deposited on oxidized wafers.

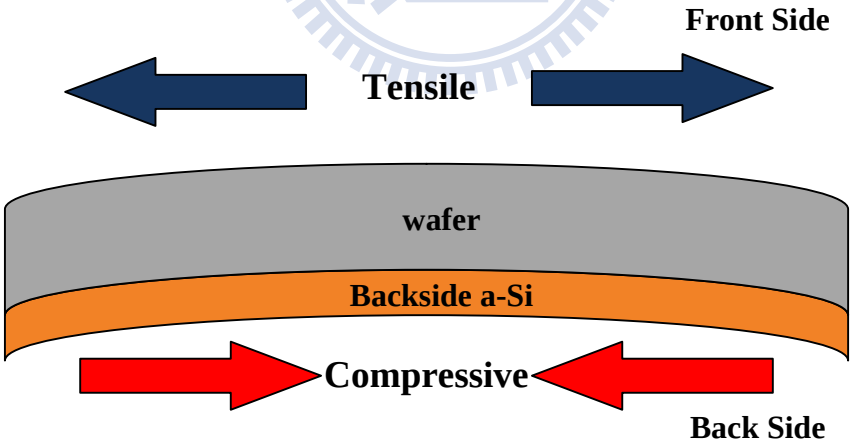


Fig. 5-5 The mechanism of the stress impacts induced by backside amorphous silicon.

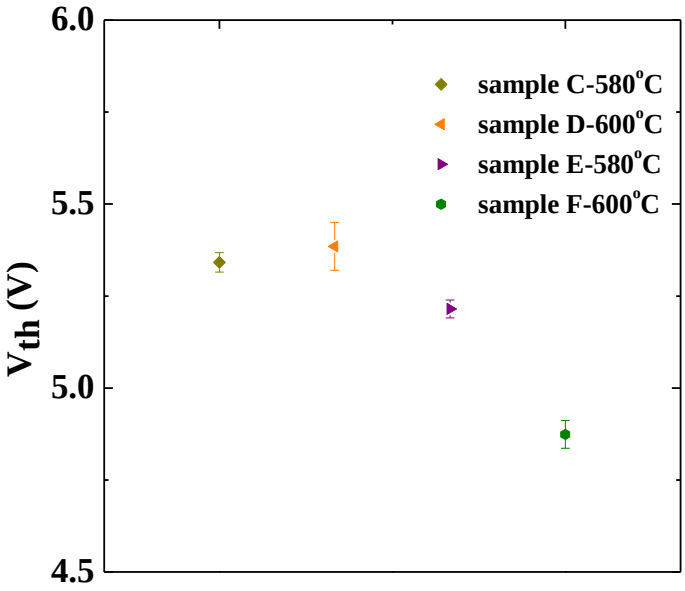


Fig. 5-6 Threshold voltage for samples deposited on oxidized wafers with inserted SiN.

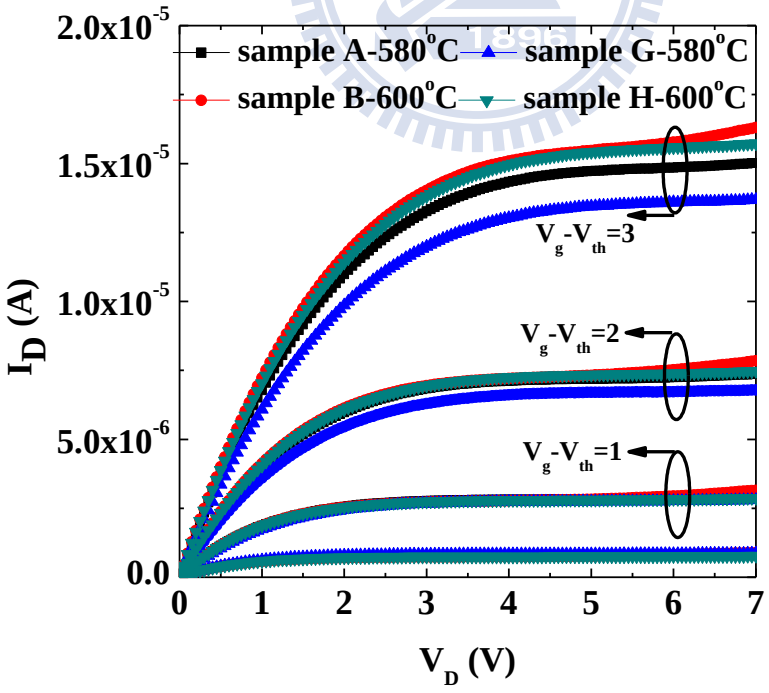


Fig. 5-7 Output characteristics of samples deposited on on oxidized wafers.

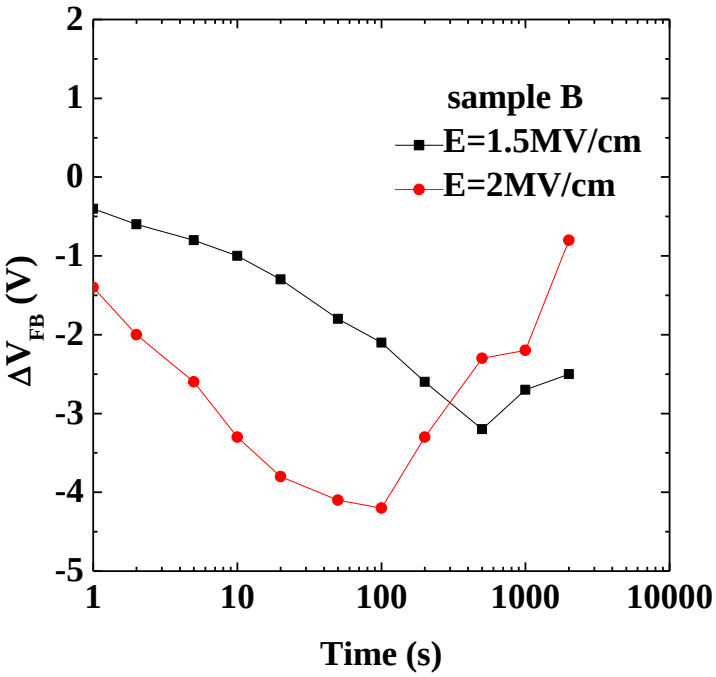


Fig. 5-8 ΔV_{FB} as a function of time for control sample stressed by different electric field.

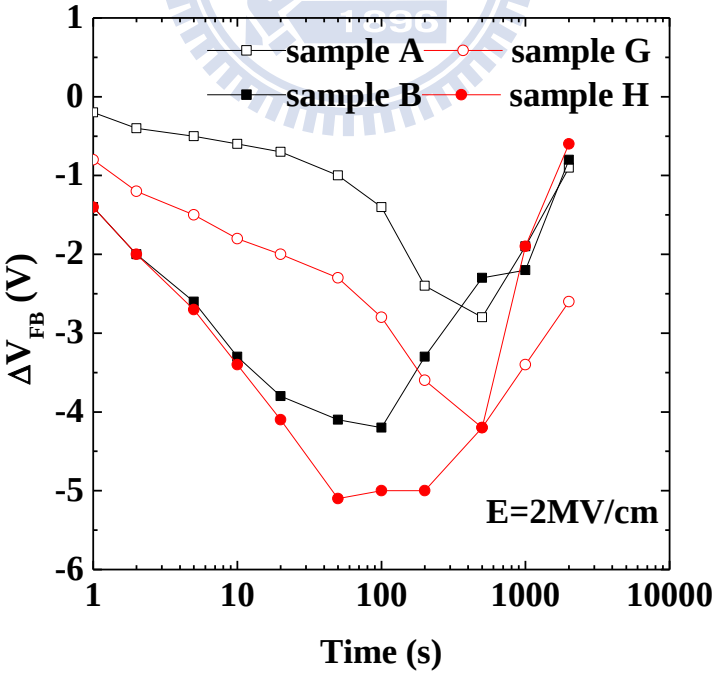


Fig. 5-9 ΔV_{FB} as a function of time for samples with and without removing back side layer.

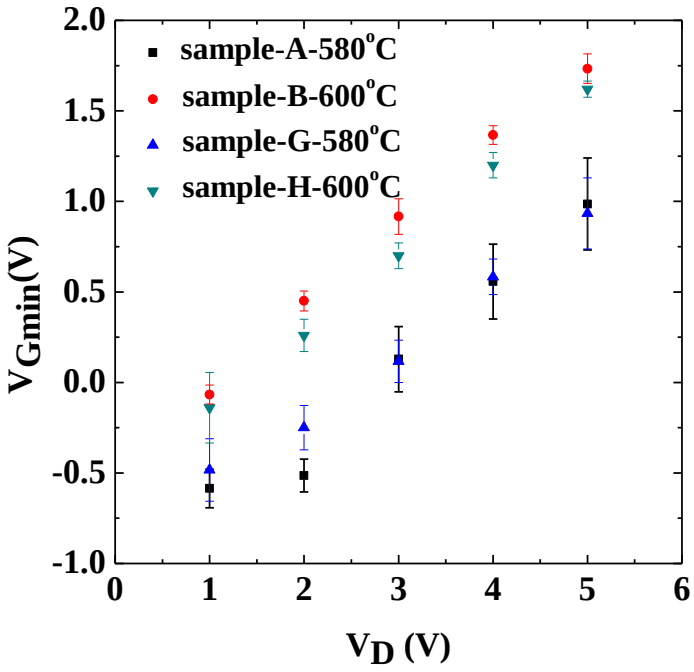


Fig. 5-10 The gate voltage corresponding to minimum leakage current at fixed drain bias for samples deposited on oxidized wafers.

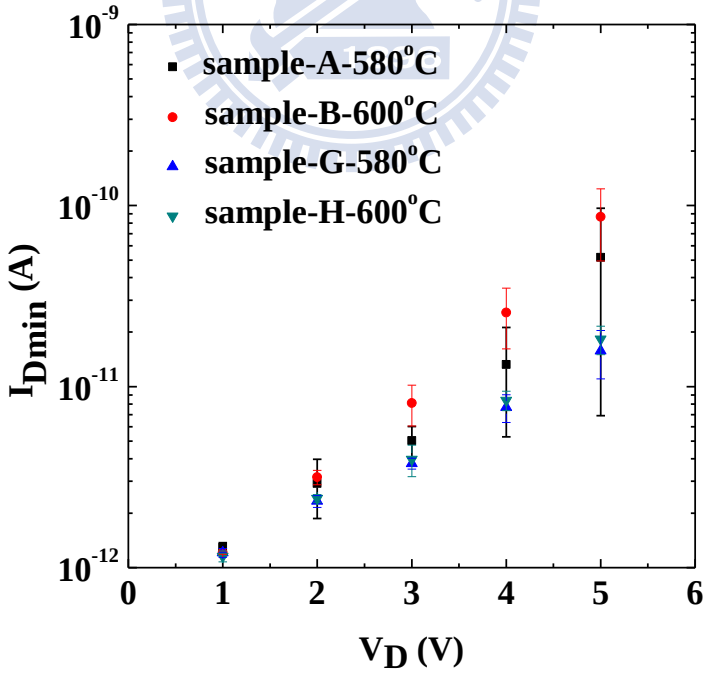


Fig. 5-11 The minimum current of samples deposited on oxidized wafers at different $V_{D.}$

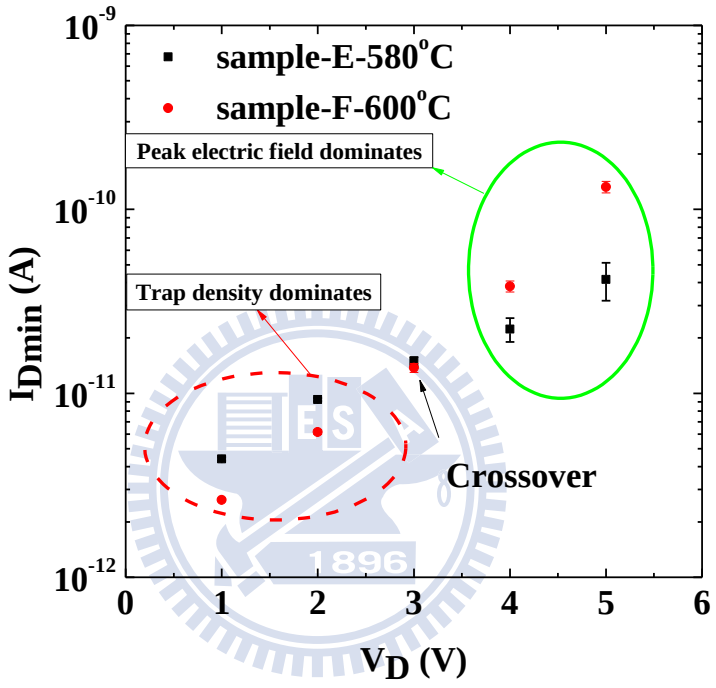


Fig. 5-12 The minimum current of samples deposited on oxidized wafers with inserted SiN at different $V_{D.}$

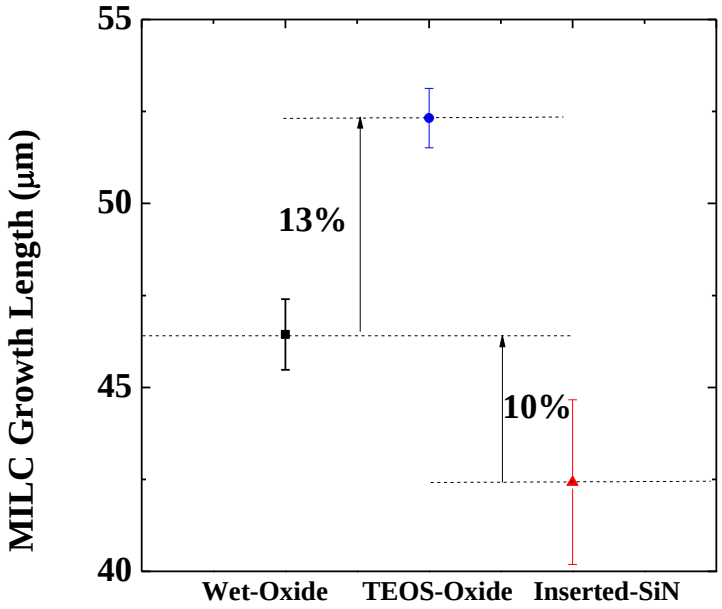


Fig. 5-13 The dependence of the MILC length on the underlying insulating layers.

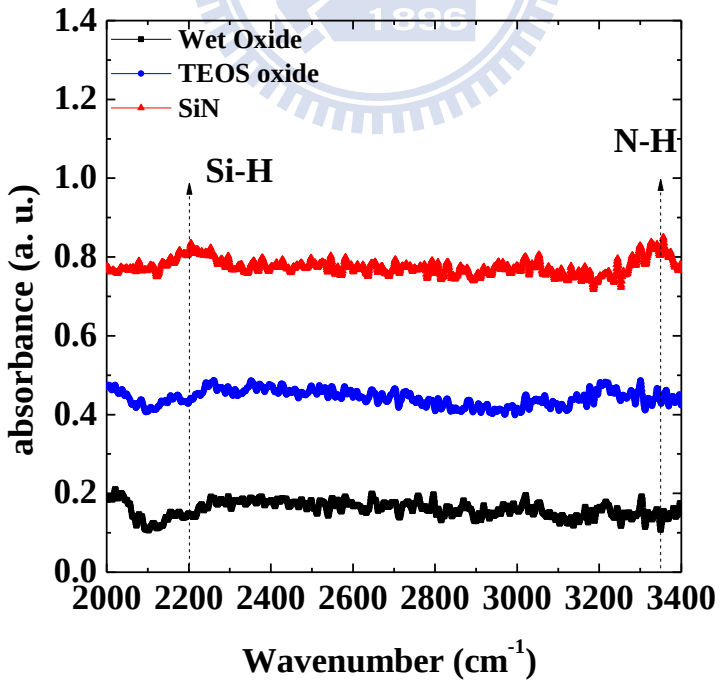


Fig. 5-14 The FTIR of Wet Oxide, TEOS oxide, and SiN for analyzing the H content.

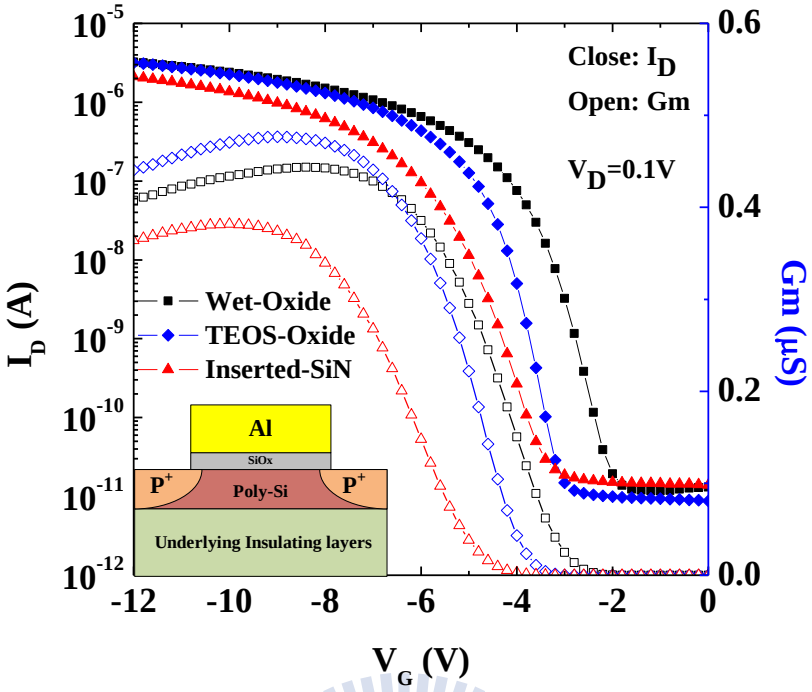


Fig. 5-15 Transfer characteristics (I_D-V_G) of p-channel TFTs with different underlying insulating layers.

	Wet oxide (500nm)	TEOS oxide (500nm)	SiN (150nm)
Intrinsic stress	-312Mpa	-52Mpa	1.2Gpa
Thermal expansion coefficient(單位)	0.4 (10^{-6} °C)	0.5 (10^{-6} °C)	3 (10^{-6} °C)

Table 5.1 Properties of underlying insulating layers.

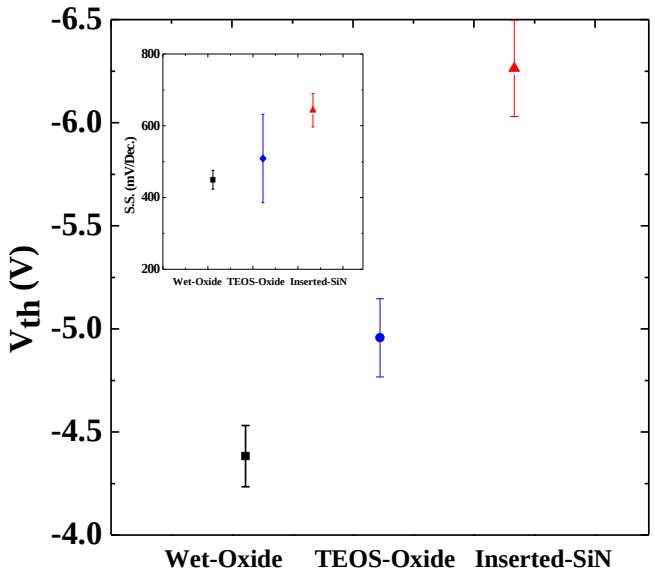


Fig. 5-16 Variation of threshold voltage as a function of channel width for $W/L = 10\mu m/10\mu m$. The inset shows the Variation of subthreshold swing as a function of channel width for $W/L = 10\mu m/10\mu m$.

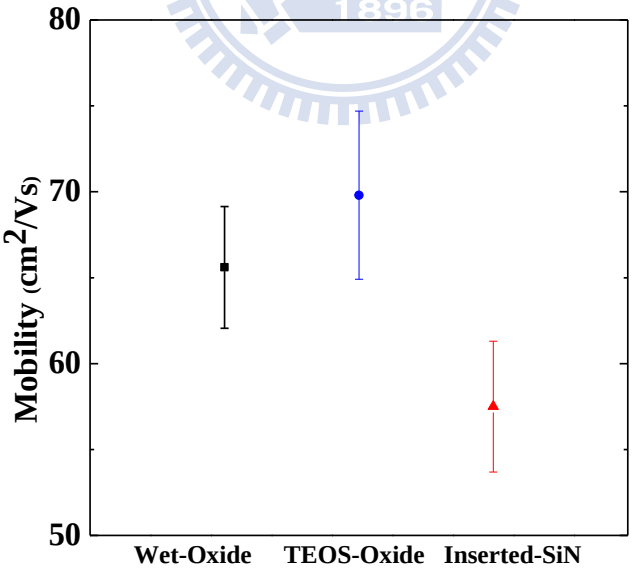


Fig. 5-17 Variation of mobility as a function of channel width for $W/L = 10\mu m/10\mu m$.

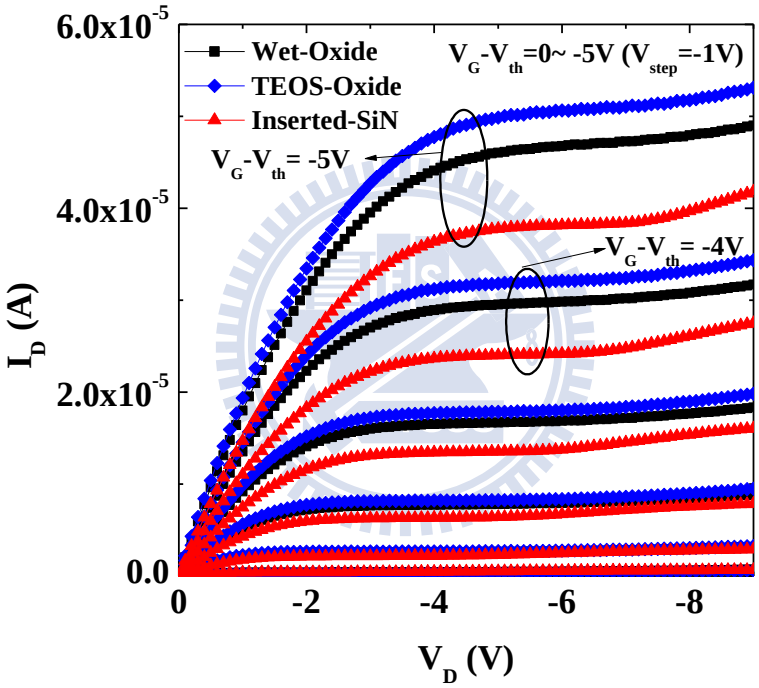


Fig. 5-18 Output characteristics (the I_D-V_D curve) of n-channel TFTs with $W/L = 10\mu m/10\mu m$ for all samples.

Chapter 6

Conclusions and Recommendations for Future Research

6.1 Conclusions

In this dissertation, the impacts of SiN on single crystal devices and poly-Si thin film transistors would be investigated in detail.

First, this dissertation presented the impacts of SiN on single crystal devices fabricated by Stress-Memorization technique in the chapter 2. The stress shift quantity rather than initial or final stress amount should be considered in stress memorization techniques. The initial compressive SiN capping layer has a higher stress shift potential than all tensile SiN capping layers split in SMT adoption, and the largest enhancement in mobility is achieved. This implies the traditional choice of capping layer should be widened to include the stress shift with the highest split. Besides, both the initial component of deposited capping layer, and the H released during annealing, affect the interface state passivation. The mechanism for the degraded gate-leakage and immunity of hot carrier stressing is ascribed to the stress induced during annealing. Based on the performance and gate-leakage, the initial compressive layer of SiN is a promising candidate compared to the initial tensile layer. Additionally, the flicker noise would be degraded by stress induced during annealing, and would be alleviated by further passivated dangling bond. On the whole, the initial compressive layer performs better characteristic as performance, gate leakage, hot carrier stressing, and flick noise.

In the chapter 3, we investigated the impacts of SiN on poly-Si TFT. As a result, using an SiN passivation layer was found to yield better performance, suppress the kink effect, and improve gate induce drain leakage (GIDL) for polysilicon thin film

transistors (poly-Si TFTs) without the long hydrogenation time required by plasma-treatment. TFTs capped with different SiN passivation layers show differences in their performance improvements, since different mechanisms are involved. Additionally, a mechanism to explain the double hump phenomenon induced by incomplete trap passivation for SiN deposited with high flow rates of nitrogen was proposed. Then, the width dependence of threshold voltage, subthrehold swing would be reviewed thoroughly. Furthermore, using the passivation layer is effective to alleviate the reliability issue.

In the chapter 4, we investigates the passivation efficiency of hydrogen by hydrogen-containing nitride, based on the comparison of different thicknesses of SiN or inserted TEOS oxide. As a result, the trap passivation by hydrogen-containing nitride becomes saturated beyond a critical thickness of SiN, and inserting TEOS oxide cannot retard the hydrogen diffusion. Moreover, we investigate the effects of hydrogen instability induced by post annealing on device performance and reliability. For the SiN-removed sample, post annealing decreases the improvements of defect passivation. Devices with a SiN capping layer can suppress outgas of hydrogen while retaining the improvement in mobility and threshold voltage. Besides, samples with capping SiN suffer from hot carrier stressing, although capping SiN offers significant improvement in mobility and threshold voltage. Samples with SiN capping layers removed subsequently can alleviate the degradation by hot carrier stressing. However, hydrogen release reduces the immunity of PBTI and NBTI. Samples experiencing hydrogen release exhibit the worst degradation of PBTI. For NBTI concerns, the dominant degradation mechanism of the threshold voltage of the SiN-removed sample is the positively-charged ΔQ_{ot} rather than the negatively-charged ΔQ_{it}, which is the mechanism the control sample and the capped SiN sample suffer. Two possible

mechanisms can explain the increased pre-existing defects that affect the hot carrier stressing, NBTI, and PBTI.

In the chapter 5, we investigated the impacts of SiN and removal of back side layer on the deep state, the tail state, and the minimum leakage current on TFTs crystallized by SPC. The sample without a-Si on the back side exhibits higher V_{th} and lower I_{Dmin}. On the other hand, TFTs with poly-Si on the SiN exhibit different temperature dependence, due to the releasing hydrogen from SiN. Furthermore, the samples with higher trap density may exhibit lower I_{Dmin} at higher V_{DS}, because the decreasing peak electric field would counteract the contribution of trap density. Then, the impacts of underlying insulating layers on the MILC growth rate and electrical characteristics are clarified. Three possible mechanisms can be used to explain the dependence of MILC growth rate on the proximity layer. Also, besides the difference in MILC growth rate, the proximity layers affect the threshold voltage and mobility. Based on the comparison among proximity layers, the SiN proximity layer not only retards the MILC growth rate most, but also exhibits the worst threshold voltage and mobility. As a result, we believe the three probable mechanisms, which can be affected by the dopant, the annealing, and the different fabrication process, can provides guidance for further exploration of the impact of the proximity layer.

6.2 Recommendation for Future Research

There are some still unknown physical insights to be studied for future work. Here are some suggestions as shown as following:

So far, the determining factor of mobility enhancement for conventional planar bulk devices has been thoroughly studied. This planar device is difficult to scale

effectively, since the challenge in the control of short-channel effects. A FinFET has been regarded as a promising candidate for future high-performance and low-power CMOS, due to the superior immunity against short-channel effects. S.C.Takagi et al. proposed that uniaxial strain is effective to enhance mobility on the (110) fin sidewall. For the first time, M. Saitoh et al. proposed that the stress memorization technique improves the I_{on} in FinFET as a result of both improvements in mobility and parasitic resistance. Also, the improvement of for <110> FinFET in I_{dlin} is higher than planar devices, meaning that SMT is a promising approach for improving FinFET performance. However, a conclusive understanding of the stress distribution inside the silicon fin produced by such techniques is still missing. Therefore, in order to further optimize the FinFET performance, understanding the SMT mechanism related to FinFET is necessary, such as the channel dimension dependence, the impacts of gate fabrication process, and the impacts of pre-amorphorization in S/D region.

Besides, we have demonstrated the effect of the flow rate of dilute gas on the deposition of the SiN layer for passivation of poly-Si TFTs. It would be interesting to investigate the impacts of *decreasing* N_2 flow rate, increasing NH_3 flow rate, and the temperature during SiN deposition. We will systematically relate the SiN deposition process to specific performance enhancements and physically mechanisms.

Moreover, we predicted that the SiN-effect would be saturated beyond a critical SiN thickness, and the TEOS buffer oxide as 20nm can’t retard the hydrogen diffusion in chapter 4. Thus, investigating the critical thickness of SiN and TEOS oxide that can alter the passivation efficiency is interesting.

Furthermore, we proposed the backside amorphous silicon and underlying insulating layers affect the poly-Si TFT crystallized by SPC and MILC. It’s interesting to investigate the impacts of backside amorphous silicon on MILC. Also,

the complete research of different fabrication process of underlying insulating layers, such as the morphology, process temperature, and the dopant effect, related to poly-Si TFT crystallized by SPC and MILC is meaningful.

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Chapter 1

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[1] **Chia-Chun Liao**, Min-Chen Lin, Tsung-Yu Chiang, and Tien-Sheng Chao, "Effects of Channel Width and Nitride Passivation Layer on Electrical Characteristics of Polysilicon Thin-Film Transistors," *IEEE Transactions on Electron Devices*, Vol. 58, No. 11, pp. 3812-3819, September 2011.

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氮化矽的氫與其應力對電晶體之影響

Impacts of Hydrogen and Stress of the SiN on the Transistors