國 立 交 通 大 學

光電工程研究所碩士班

碩 士 論 文

導電性高分子聚合物/有機材料及自我組裝單分子層在空間電荷限制電晶體中的應用

The application of conduction polymer/organic materials and self-assembly monolayer in space-charge-limited transistors

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中華民國 九十八 年 七 月

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摘 要

軟性電子與顯示技術是新世代電子技術領域之重要方向，有機電晶體更是因為低製作成本、易於大面積製作等優點而被許多專家學者廣泛研究討論。傳統之有機場效電晶體具有在同一平面的源極與汲極，屬於水平結構，因其難以縮短通道長度及受限於高分子材料之低載子遷移率等原因，導致高操作電壓及低輸出電流等缺點。所以有人提出以膜厚控制通道長度，但是卻因為製程因素，大部分提高了輸出電流卻犧牲了開關比。有鑒於此，本論文將介紹一種具有製程簡單、低操作電壓、輸出電流大特性之垂直式有機電晶體。

本論文首先討論具有不同主動層有機材料的空間電荷限制電晶體，並探討其工作原理與元件特性。目前高分子空間電荷限制電晶體當操作電壓是1伏特的時候最大輸出電流密度是0.136mA/cm^2，開關比為24310，電流增益約為10^4。在比較不同主動層的元件時發現到主動層的形態會造成漏電現象。接著將介紹一些自我組裝單分子層的化學結構還有操作原理。最後將討論自我組裝單分子層應用在製作元件中減少製作時間或是增加輸出電流的成果。

The application of conduction polymer/organic materials and self-assembly monolayer in space-charge-limited transistors

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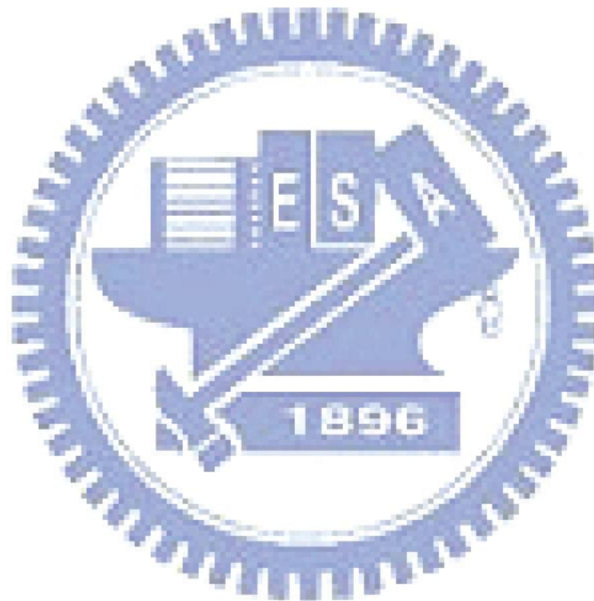
Abstract

Polymer transistors have been studied extensively due to their applications on low-cost large area transistors arrays or on flexible electrons. Conventional polymer filed-effect transistor (FET) is a horizontal device with source and drain electrodes in the same plane. Low mobility conjugated polymers and long channel length limit the characteristics of polymer FET, and thus polymer FET usually exhibits high operation voltage and low operation frequency. In view of these limitations, this paper will introduce various vertical organic transistors; the channel length is determined by the total thickness of the organic semiconductor layer between source and drain. Even high turn-on current has been obtained low on/off ratio and sophisticated vertical fabrication procedures limit its following development. Specifically, on/off ratio of most vertical transistors are as low as a few hundreds.

In this thesis we will discuss with different active layer materials of organic space-charge-limited transistors, then introduce operating mechanism and of characteristics the devices. So far, output current density of space-charge-limited

transistor is about 0.136 mA/cm^2 at operating voltage 1V, on/off ratio is 24310, and current gain is around 10^4. In comparing the device of different active layer was found that the morphology of active layer will cause leakage phenomenon. Then it will introduce self-assembled monolayer's chemical structure and the principle of operation. Finally, discussion of self-assembled monolayer used to reduce the production time or increase output current for the devices.



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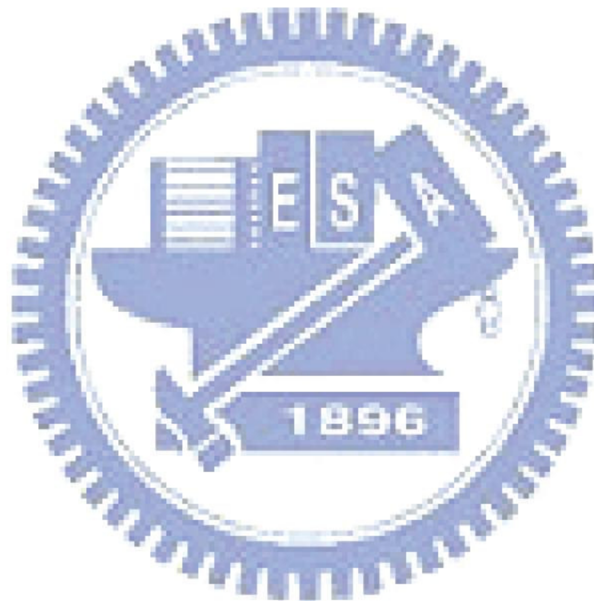

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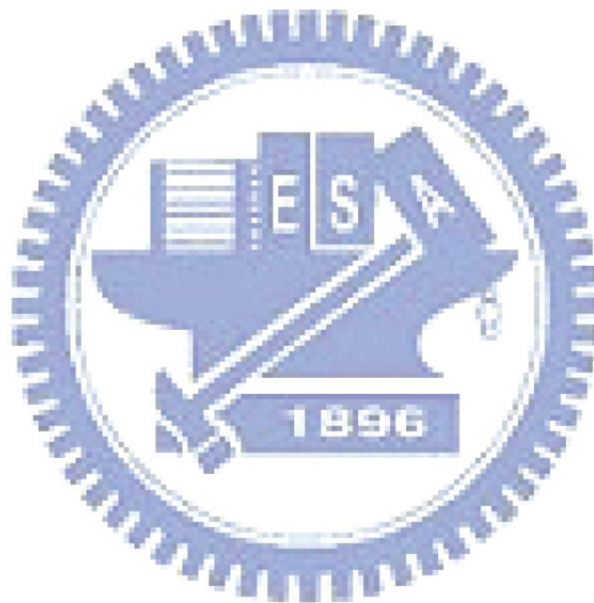


Chapter 1

Introduction

1-1 Introduction

Electronic devices based on organic semiconductors provide attractive alternatives to inorganic devices due to their lower cost as well as the compatibility with flexible substrates. One of the key components in the organic electronic circuits is the polymer field-effect transistor (FET). [1, 2] Many researches on polymer FET have demonstrated reasonable performance [3, 7] and the possibility of integration with organic light-emitting diodes. [3-6] The characteristics of polymer FETs can be strengthened by increasing the mobility [10], utilizing a self-assemble monolayer as gate dielectrics [11] and reducing the channel lengths to the submicron [8]. Horizontal organic FETs with submicron channel lengths made by electron-beam lithography [13], nanoimprint lithography [14] and soft contact lamination [15] have been demonstrated. Vertical organic FETs, whose channel length was determined by the thickness of an insulating layer between source and drain, have been made by solid-state embossing [16], excimer laser [17] and photolithography [18]. However, the inherently low mobility as well as the incompatibility between conventional submicron lithography and organic materials poses great limitation on the device performance and the fabrication process for polymer FET. The unique advantages of organic materials such as low-cost and large-area solution process are so far not fully explored for high-performance FET. Vertical non-field-effect transistors with multilayer structures give another route to circumvent the limits of both horizontal and vertical field-effect transistors. In vertical

no-field-effect transistors, the channel length can be easily defined by the total

thickness of the organic layers, and the current is modulated by a conductive layer embedded in the organic materials. Various device operating principles were proposed with different types of conductive layers such as a thin metal film [19, 20, 27, 28], a strip-type metal film [21, 22], a mesh gate electrode [23-25], and a porous conducting polymer network [26]. The remaining problems are the low current density, low on/off ratio as well as the complex fabrication process. Take the organic static-induced transistor (SIT) as an example, it have a striped metal layer embedded in the thermally evaporated organic layer. [22, 38] It has a similar structure with the vacuum tube triode, which consists of the cathode for electron emissions by heating, the anode for electron collection, and the grid for current modulation. In a vacuum tube triode both the grid and anode electrodes are able to control the potential within the device but the grid is much more effective in controlling the gradient near the cathode. When the grid is in large and negative bias, the electrons experience a negative gradient of potential after they are emitted from cathode. Effectively the electrons encounter a large energy barrier between cathode and anode, and consequently very few of them can be collected by the anode. On the contrary, if the grid is slightly negative biased or positively biased, it is possible for the electrons to find a passage through the potential minimum between two grid wires. Despite similar structure, in SIT the current is modulated by a junction potential barrier while in vacuum tube triode the space-charge-limited current (SCLC) is modulated. [39] Another example is the “analog transistors” proposed by Shockley in 1952. It is the first solid-state device whose operation resembles that in the vacuum tube triode with current limited by the SCLC. [40]

1.2 Motivation

One of the key components of the flexible electronics is FET, a horizontal device with source and drain electrodes on the same plane. The current ratio in the on and off

states (on/off ratio) and the field-effect mobility are two parameters to characterize the organic field-effect transistors. So far the organic FET shows low current output because of the intrinsically low carrier mobility due to the weak wave function overlaps between the molecules and the disorder in the thin film. The low mobility also strongly limits the operation speed to be under 100 kHz. Furthermore, the organic FET is unstable because the conduction channel is confined to a few monolayer at the semiconductor-dielectric interface where the adsorbed oxygen, moisture, and other chemicals have huge effect on the transistor characteristics. To obtain a desired current output, its operating voltage usually exceeds 20 volts. A great deal of effort was made in to improve the performance of the field-effect transistors by increasing the mobility, reducing the gate dielectrics thickness, and reducing the channel lengths. For new material developments, many new organic molecules have been designed and synthesized. [31-37] Pentacene represents one of the most studied molecules for FET application. Under favorable fabrication conditions, motility as high as 5 $cm^2V^{-1}s^{-1}$ have been reported. [31] Much progress has also been made in polymeric materials. [9, 10] So far the highest mobility for polymer is about 1 $cm^2V^{-1}s^{-1}$. [9] While these values are still far below that offered by inorganic semiconductors, some are appropriate for some low-end applications. One way to reduce the operating voltage is utilizing a self-assembled monolayer (SAM) as gate dielectric with gate current densities as low as 10^{-9} Acm^{-2}. [11, 12] With these dielectrics, the transistor can be operated with voltages of 2 V. The devices is however sensitive to the pin-holes in SAM and not highly reproducible. Lithography upon SAM is also difficult. Organic field-effect transistors with submicron channel lengths made by electron-beam lithography [13], Nan imprint lithography [14] and soft contact lamination [15] have been demonstrated. Vertical organic field - effect transistors, whose channel length was determined by the thickness of an insulating layer between source and drain, have

been made by solid-state embossing [16], excimer laser [17] and photolithography [18]. However, these procedures to reduce the channel length are complicated and expensive. So far the organic FET still suffers from low mobility, high voltage and low speed. The unique promises of organic materials such as low-cost and large-area solution process not yet realized by high-performance field-effect transistors.

Vertical non-field-effect transistors with multilayer sandwich structures give another route to circumvent the limits of organic field-effect transistors. In vertical non-field-effect transistors, the channel length can be made small easily because of it is defined by the thickness of the organic layers. The current is modulated by a conductive metal layer embedded in the organic materials. Various device operating principles were proposed with different types of conductive layers such as a thin metal film [19, 20], a strip-type metal film [21, 22], a mesh gate electrode [23], and a porous conducting polymer network. [26] The remaining problems are the low current density, low on/off ratio as well as the complex fabrication process. In order to tackle the major challenge for organic transistors, that is, low mobility of most organic materials, molecular or polymeric, we have invented two new metal-base organic transistors with vertical structure. One is based on the concept of hot carrier ballistic transport in the base [27, 28], and another one is a solid-state analogy of vacuum tube which we call space-charge-limited transistor [29, 30]. Operation principles and device structures of vertical metal-based organic transistors are discussed below. They show good performance including low voltage, high current output and high speed with easy fabrication.

1.3 Theoretical background

Organic semiconductor device inherited the functions of inorganic semiconductor device, and it could be used to produce each work of that inorganic semiconductor can be reached. However organic semiconductor properties can be

produced products which are different from past products on a soft substrate, such as thin flexible display panel, soft-type transistors, solar cells and optoelectronic devices. The characteristics of organic matter will make products of organic semiconductor more extensive use and more diversified. By simple process, spin coating solution or technology of ink-jet, polymer semiconductors products can make production costs down. So high-tech products become more common, scientific and technological development brings infinite potential in the future.

However, organic semiconductors are non-crystalline materials, molecular distribution is non-random order. The nature of most materials did not be doped by electrons or holes materials so that the mobility of materials s is very low. Furthermore, HOMO and LUMO of the organic semiconductor will make where the valence band and conduction band are. Therefore, the metal electrode work function and the difference between HOMO and LUMO will have a great impact for different injection.

In the inorganic semiconductor materials, space charges may be received from cations and anions after the free charges counteraction in the interface of PN junction. But there is no PN junction in Organic semiconductor, so do not have the space charges which like depletion region. It was from the injection charge which can not transport or recombine immediately, and accumulate in the metal-semi interface. As a result, it contains high carrier concentration in interface and charge back into the electrode, the formation of the loss. (Figure 1.1)

SCLC easily occur in the following conditions, low-carrier injection barrier (<0.25eV), the interface between electrode and semiconductor is ohmic contact, the injection electrode provides a large number of carrier and fill all the traps up, and the semiconductor material itself mobility is too low. Using the following modified Child's Law (Square-power Law) mathematical model of SCLC, trap-free and

trap-trapped, respectively. $J = \frac{9}{8}\varepsilon_0\varepsilon_r\mu\frac{V^2}{L^3}$

Trap-free case: The assumption is that thermal free carriers and trapping states do not exist in organic semiconductor materials.

L: is the specimen thickness, which is the drift space between electrodes

μ: injected carrier drift mobility

V: the voltage applied across the electrodes

ε_0: the permittivity of free space

ε_r: the relative dielectric constant

Trapped case：(The assumption is that there are no thermal free carriers in organic semiconductor materials. Under the conditions of shallow trap, the first deep trap has been filled.)

$$J = \frac{9}{8}\theta\varepsilon_0\varepsilon_r\mu\frac{V^2}{L^3}$$ θ=free carriers / trapped carriers

Trap states in materials are from their own defects and impure materials. According to the relative position between e-holes of the trap states and the e-hole quasi-Fermi level can be divided into deep traps and shallow traps as in the Figure 1.2.

J-V^2 shows a linear relationship no matter traps exist or not. In fact, the mobility of semiconductor materials is a function contained temperature and electric field. As follow: (with holes for example).

$$\mu_p(E,T) = \mu_0(T)Exp(\gamma\sqrt{E})$$ μ_p : Mobility of holes

$$\mu_0(T) = \mu_0 Exp(\frac{-\Delta}{K_B T})$$ μ_0 : Intrinsic mobility

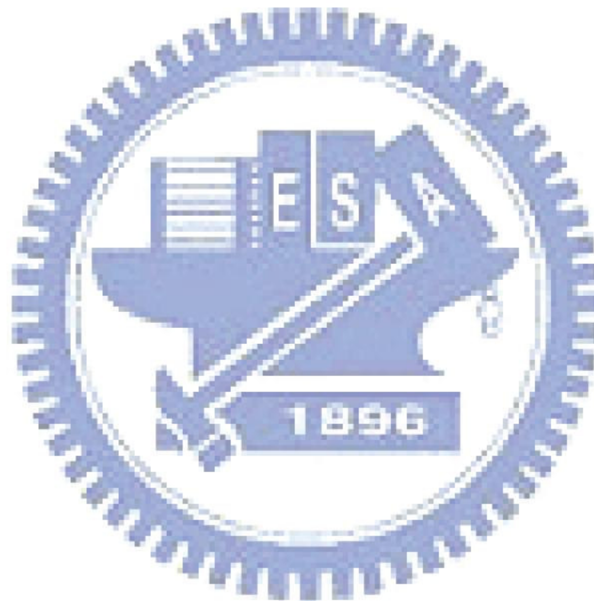
$$\gamma = B(\frac{1}{K_0 T} - \frac{1}{K_0 T_0})$$ Δ: Potential difference

B: Poole-Frenkel constant

In the above results, electrical devices are controlled by SCLC, the current density will enhance by high temperature and applied voltage.

1.4 Thesis Organization

After introduction of Chapter 1, the device fabrication will be discussed in Chapter 2. Then characteristic of space-charged-limited transistors will be described in chapter 3. The self-assembled-monolayer will be analyzed in Chapter 4. Finally, conclusions will be given in Chapter 5. The section organization of this thesis is listed below:



Chapter 1

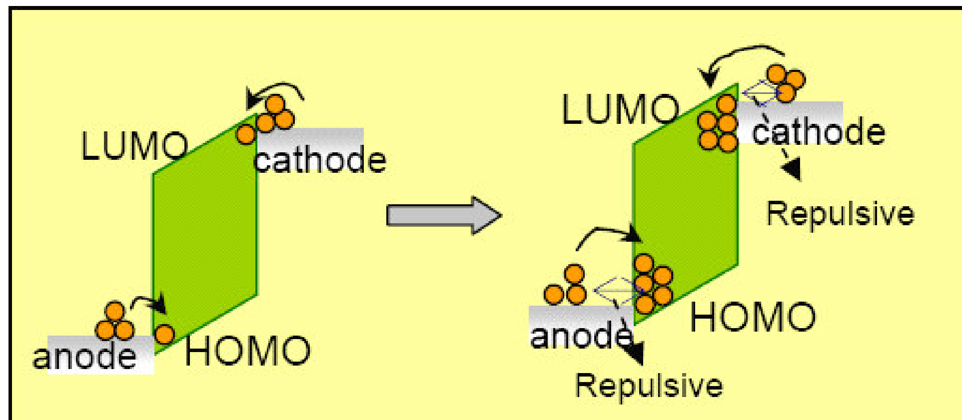


Figure 1.1 The injection charge which can not transport or recombine immediately, and accumulate in the metal-semi interface.

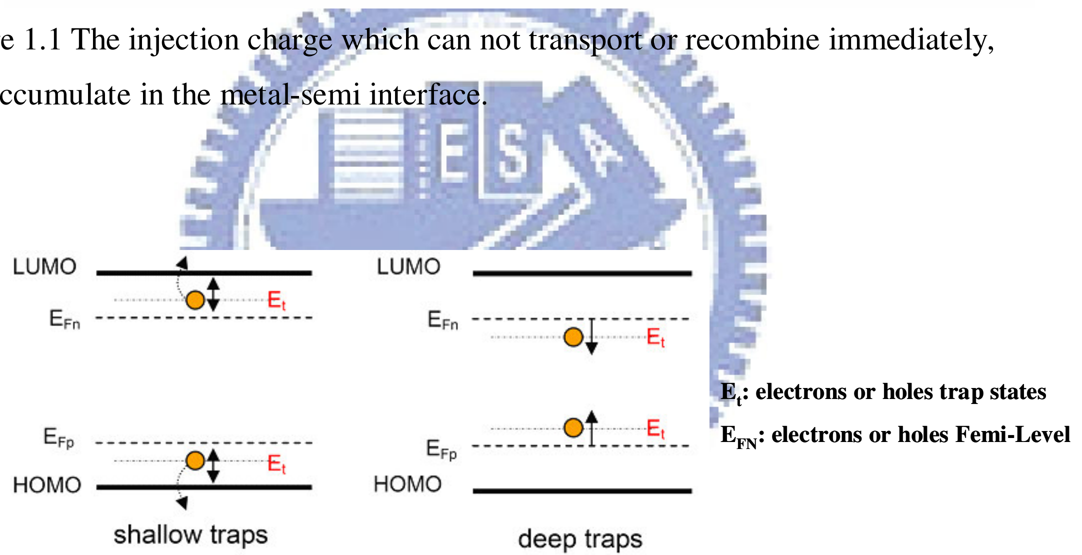


Figure 1.2 Band diagrams of deep traps and shallow traps.

Chapter 2

Device Fabrication

2.1 Device Structure and Fabrication

2.1.1 Device structure and cross-section

Figure 2.1 shows the structure of space-charge-limited transistors. Bottom silicon oxide is used to block the leakage current between Al and Au, and the top silicon oxide is used to block the leakage current between Al and Al. There are three organic materials will be discussed such as poly [3-hexylthiophene] (P3HT), pentacene and fullerene (C60). The cross-section of device and the device dimension is 1mm^2. Figure 2.2 shows the process flow of the vertical transistor proposed in this work.

2.1.2 Glass substrate clean

Glass substrate (CORNING Eagle 2000) must keep clean or films may become rough. The rough surface would cause point discharge between the insulator and metal. The steps of clean glass substrate are shown as.

Steps:

(1) De Ion (DI) water current flows for 5 minutes in order to remove the particles.

(2) The substrates should be placed under the in the acetone and ultrasonic resonance for 5 minutes in order to remove the organic pollution. Then, the substrates have to put under the DI water current flow for 5 minutes in order to remove the solvent.

(4) The substrates were put in the KG detergent bath with ultrasonic resonance for 5 minutes in order to remove the particles, fingerprint, and ionic.

(5) The substrates were put under the DI water current flow for 5 minutes in order to remove the solvent.

(6) Finally, the substrates would be fried with dry N_2 flow to blow off the water on the substrates.

2.1.3 Bottom metals deposition

Before deposition metal on the substrate, the glass substrates were exposed to the UV-light by UVO_3 clean machine that keep the substrate surface clean. Nickel(99.99 %) was deposited to increase the adhesion of the Gold by thermal evaporator. The deposition rate was controlled at 1Å/sec and the thickness of nickel was about 100Å. After deposition of adhesion layer, Gold (99.99%) was deposited by thermal evaporator. Both of two processes the deposition pressure was started at $5x10^{-6}$torr and the substrates temperature fixed at 50°C. The metal region was defined through shadow mask.

2.1.4 High Density Polystyrene Spheres as Shadow Mask

It could fabricate a microstructure in the lateral direction within a large scale organic device using non-photolithographic processes according to Spontaneous Patterning of Higher Order Structures' (SPHOS) [41–43]. Colloidal lithography [44], one of the techniques adopted in the SPHOS forms porous films by removing particles after the film deposition. Positively charged polystyrene particles shown in Figure 2.3(a) (200 nm, tetramethylammonium latex) were adsorbed onto the substrates from dispersion by electrostatic interactions. Particles concentration diluted with ethanol to 0.6 wt%. Immersion time was 3 minutes to allow the adsorption to reach saturation. Excess particles were rinsed off in a beaker with ethanol and then transferred to a beaker with boiling isopropanol solution for ten seconds. Figure 2.3(b) shows polystyrene spheres are absorbed on the Au film surface. After the SiO/Al/SiO

deposition, the polystyrene spheres are removed by an adhesive tape (Scotch, 3M) without damage to the metal. The images of the Al grid with 2000 Å opening diameter are shown in Figure 2.3(c). The key procedure in this fabrication is that the substrate is then transferred to a beaker with boiling isopropanol solution for ten seconds. Similar to the method of Fujimoto et al [24], the substrate is finally blown dry immediately in a unidirectional nitrogen flow. The boiling isopropanol treatment is a critical step to achieve a high density yet separated array of holes, required for vacuum tube triode as well as SCLT. When the substrate is submerged in polystyrene solution, the charged polystyrene spheres are absorbed on the Au surface without aggregation due to the electrostatic repulsion force. The polystyrene spheres without the boiling isopropanol treatment shown in Figure 2.3(d) are easy to aggregate during the drying process and cause unwanted non-uniform and connected distribution. This may be attributed to the capillary force which pulls spheres into aggregates before the spheres are immobile during the period of vaporized solvent. The importance of the boiling isopropanol treatment is presumed to increase the evaporation rate of the solvent during the nitrogen blow dry such that the spheres do not have enough time to move to one another and form aggregate during evaporation. By tuning the solution concentration and submerging time, the condition to prepare Al grid with maximum opening density with minimum unwanted openings can be found in spite of some occurrence of the unwanted irregular openings The benefit of this method is the possibility to process large areas in a short processing time without photolithography.

2.1.5 Dielectric and grid fabrication

After immersed polystyrene spheres as shadow mask, the deposition is started at the pressure around 3×10^{-6}torr. Slower deposition rate is expected to result in smoother and better ordering of the insulator than fast one. The 50-nm-thick silicon oxide was deposited by thermal evaporation at a deposition rate of 0.1Å/s. It is

evaporated to prevent large leakage current from Al to Au. The insulator region was defined through shadow mask. Then we deposited aluminum as base metal. The deposition is started at the pressure around 5×10^{-6}torr. The 30-nm-thick Al was deposited by thermal evaporation at a deposition rate of 1Å/s.

2.1.6 Organic active layer fabrication

In the section, introduce each of the organic layer deposition respectively:

1. P3HT:

The substrate was exposed under the ultra-violate light for 15min to keep surface clean. P3HT was spin coated from chlorobenzene solution (2.5 wt% 1000rpm) on the Au layer, and baked at 200 °C for 10min in vacuum. After we spin coated the P3HT film, we use acetone to clean the unnecessary area. Then, a thin P3HT layer of about 1338 Å was obtained.

2. Pentacene

The substrate was exposed under the ultra-violate light for 15min to keep surface clean. The pentacene material obtained from Aldrich without any purification was directly placed in the thermal coater for the deposition. The deposition was started at the pressure around 3×10^{-6}torr. The 180-nm-thick pentacene was deposited by thermal evaporation at a deposition rate of 1Å/s. The active region was defined by shadow mask.

3. C60

The substrate was exposed under the ultra-violate light for 15min to keep surface clean. The C60 was directly placed in the thermal coater for the deposition. The deposition was started at the pressure around 3×10^{-6}torr. The 200-nm-thick C60 was deposited by thermal evaporation at a deposition rate of 1Å/s. The active region was defined by shadow mask.

2.1.7 Top metal deposition and Package

We deposited Al as the top metal. The deposition was started at the pressure around 5×10^{-6}torr. The 50-nm-thick Al was deposited by thermal evaporation at a deposition rate of 1Å/s.

If life time of device becomes longer, the sample should be packaged to avoid the oxygen and moisture. The device were packaged in the glove box filled with the N2 gas and sealed the cap for sample protection. We sealed the cap by the glue which crosses link as it exposed under the ultra-violate light for proper time where the wave length is 356nm. The process flow of the vertical transistor was proposed in this work.

2.2 Dielectric characteristics

From Figure 2.4(a), we can get the different breakdown voltage corresponding to different thickness of silicon oxide. When the operating voltage is 1V with thickness of bottom dielectric is 50 nm, the leakage current level is 10^{-3}mA/cm^2. When the operating voltage is 1V the leakage with thickness of top dielectric is 30 nm, the leakage current level is 10^{-2} to 10^{-3}mA/cm^2. The current of transistor can be low off depending on these measurement results.

Figure 2.4(b) shows comparison the characteristics of silicon oxide with/without Polystyrene Spheres. From Figure 2.4(b), the leakage current of silicon oxide significantly increase after used Polystyrene spheres as mask. The reason is Polystyrene Spheres occupied the location of silicon oxide (SIO). It is inevitable in the process of Polystyrene Spheres.

Chapter 2

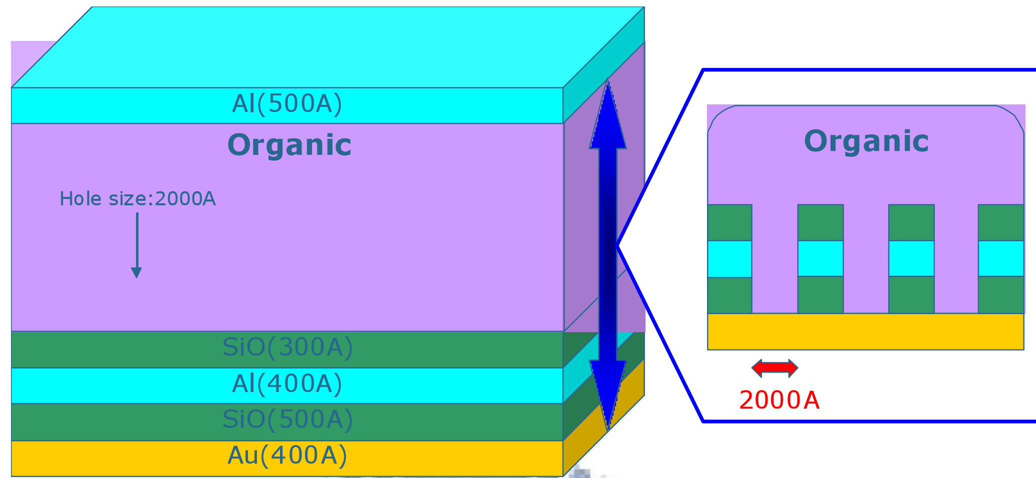


Figure 2.1 The structure of space-charge-limited transistor.

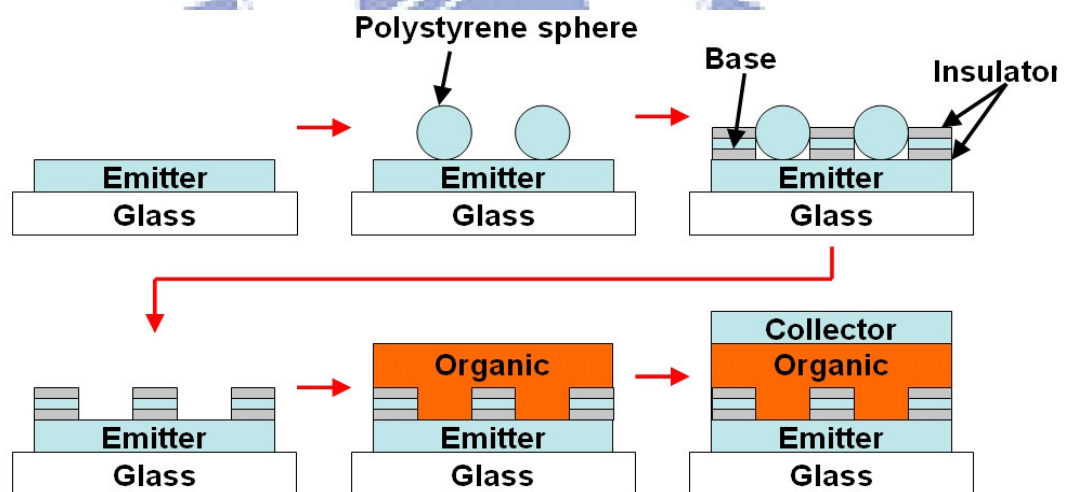


Figure 2.2 The process flow of the vertical transistor proposed in this work.

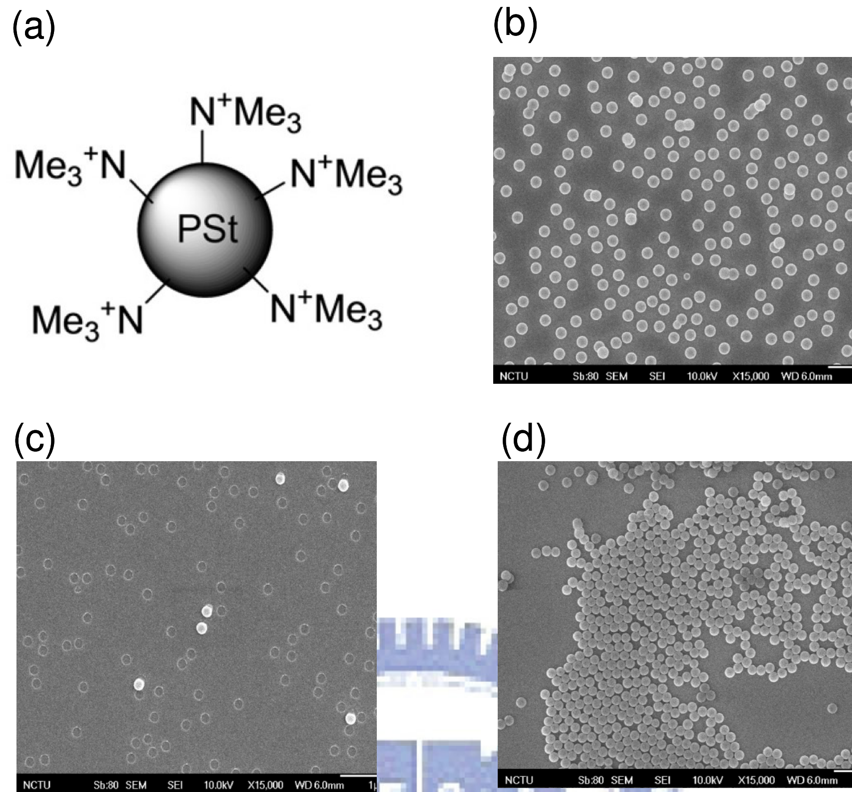
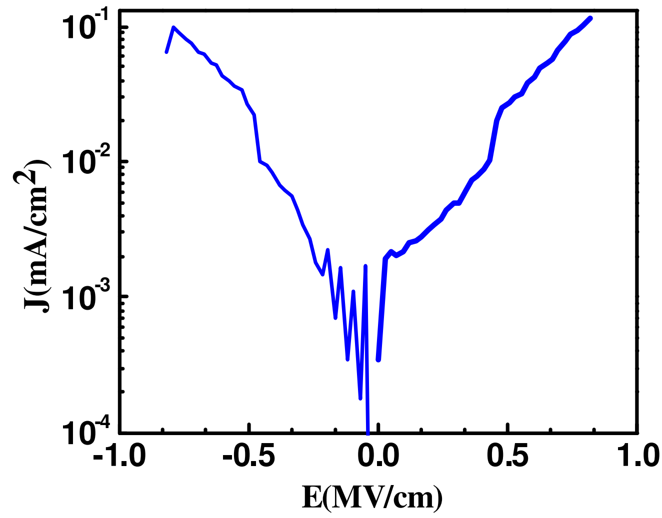
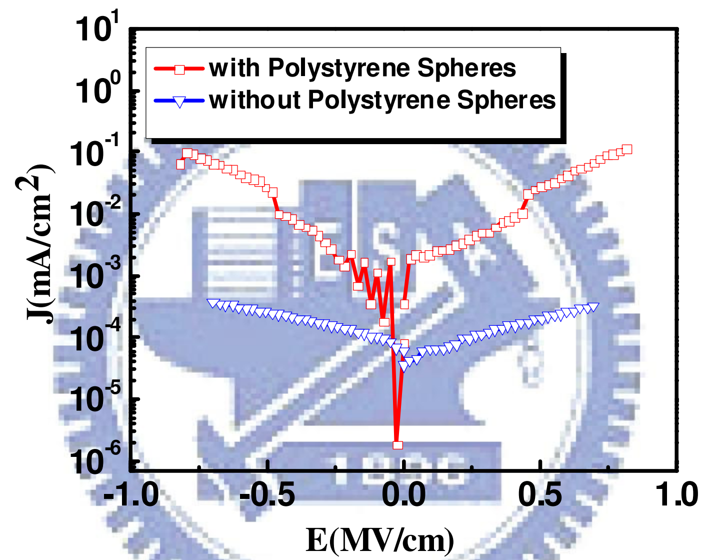


Figure 2.3(a) The structure of polystyrene spheres.(b) The polystyrene spheres on the Au film surface.(c) The polystyrene spheres are removed by an adhesive tape (Scotch, 3M) without damage to the metal. (d) The gold surface without the boiling IPA treatment.



(a)



(b)

Figure 2.4(a) The characteristics of silicon oxide with Polystyrene Spheres. (b) Comparison the characteristics of silicon oxide with/without Polystyrene Spheres.

Chapter 3

Result and Discussion

3.1 Transfer characteristic of SCLT

3.1.1 P3HT-based space-charge-limited transistor

P3HT-based SCLT was fabricated based on chapter 2. The characteristics of P3HT-based SCLT with opening diameters of 2000 Å on the top insulator (SIO) are shown in Figure 3.1 (a). In P3HT-based SCLT the carriers in the Al grid are blocked by the 30-nm silicon oxide and 14-nm P3HT between Al (base) and Al (collector). The grid current is the reverse current of the Al/SIO/P3HT/Al diode which is almost zero. The current gain is an important value to be maximized. As shown in Figure 3.1 (a) and Figure 3.1 (b), the grid current density (J_G) of P3HT-based devices is in the order of 10^{-5} mA/cm^2 which is much smaller than J_C. The current gain which is defined J_C/J_G is as large as 10^4. The collector current (J_C) for fixed collector voltage is modulated by the grid voltage (V_G) and the Au (emitter) is the common ground. The positive grid voltage V_G, is used to introduce energy barrier for holes at the openings, and the off current can be reduced by increasing V_G until a large leakage current between the grid and collector occurs. Figure 3.1(a) shows the on/off ratio of J_C is 24310 at $V_C = -1$ V for transistors with opening diameters of 2000 Å on the top insulator and the highest J_C output is 1.331mA/cm^2 in for device dimension is 1 mm^2. The total output current can be scaled up by using a larger area in the same condition. The device characteristics in double logarithmic scale with fixed V_G are shown in Figure 3.2 for tracing the signature of SCLC. Three regions belonging to ohmic, trap filling and SCLC can be distinguished [45]. The slope of $\log I - \log V$ is equal to 1 for ohmic conduction, while the slope is equal to 2 for SCLC. The dashed lines with slope equal to 1 and 2 are drawn in the Figure.3.2 for indication. Indeed, the current

follows the SCLC once the barrier at the opening is suppressed by a sufficiently negative V_C. There is always a small ohmic current at the low voltage. The polymer diode has a turn-on voltage where the current varies from a small leakage ohmic current to a quadratic SCLC current. The turn-on voltage is determined by both the level of the leakage and the difference between the work functions of the cathode and anode. Figure3.2 is shown the P3HT-based emitter-collector diode and the SCLC is about 3V.

3.1.2 Pentacene-based space-charge-limited transistor

Pentacene-based SCLT was fabricated based on chapter 2. The characteristics of Pentacene-based SCLT with opening diameters of 2000 Å on the top insulator are shown in Figure 3.3(a). In Pentacene-based SCLT the carriers in the Al grid are blocked by the 30-nm silicon oxide and 60-nm Pentacene between Al (base) and Al (collector). The grid current is the reverse current of the Al/SIO/Pentacene/Al diode which is small but not zero. The current gain is therefore an important value to be maximized. As shown in Figure 3.3(a) and Figure 3.3(b), the grid current density J_G of Pentacene-based devices is in the order of 10^{-3} mA/cm^2 which is much smaller than J_C. The current gain which is defined J_C/J_G is as large as 10^3. The collector current (J_C) for fixed collector voltage is modulated by the grid voltage (V_G) and the Au (emitter) is the common ground. The positive V_G is used to introduce energy barrier for holes at the openings, and the off current can be reduced by increasing V_G until a large leakage current between the grid and collector occurs. Figure 3.3(a) shows the on/off ratio of J_C is 390 at $V_C = -1$ V for transistors with opening diameters of 2000 Å on the top insulator and the highest J_C output is 0.2693mA/cm^2 for device dimension of 1 mm^2. The device characteristics in double logarithmic scale with fixed V_G are shown in Figure 3.4 for tracing the signature of SCLC. The dashed lines with slope equal to 1 and 2 are drawn in Figure 3.4 for indication. Indeed, the current follows the SCLC

once the barrier at the opening is suppressed by a sufficient negative V_C. There is always a small ohmic current at low voltage. The polymer diode has a turn-on voltage where the current varies from a small leakage ohmic current to a quadratic SCLC current. The turn-on voltage is determined by both the level of the leakage and the difference between the work functions of the cathode and anode. Figure3.4 is shown the P3HT-based emitter-collector diode and the SCLC is about 4V.

3.1.3 C60-based space-charge-limited transistor

C60-based SCLT was fabricated based on chapter 2. The characteristics of C60-based SCLT with opening diameters of 2000 Å on the top insulator are shown in the Figure 3.5(a). In C60-based SCLT the carriers in the Al grid are blocked by the 30-nm silicon oxide and 80-nm C60 between Al (base) and Al (emitter). The grid current of Al/SIO/C60/Al diode is almost zero. Therefore, the current gain is an important value to be maximized. As shown in Figure 3.5(a) and Figure 3.5(b), the grid current density (J_G) of C60-based devices is in the order of 10^{-3} which is smaller than J_C. The current gain J_C/J_G is as 10^2. The collector current (J_C) for fixed collector voltage is modulated by the grid voltage (V_G) and the Al (emitter) is the common ground. The negative V_G is used to introduce energy barrier for electrons at the openings, and the off current can be reduced by decreasing V_G. Figure 3.5(a) shows the on/off ratio of J_C is 589 at $V_C = 1$ V for transistors with opening diameters of 2000 Å on the top insulator and the highest J_C output is 0.411mA/cm^2 for device dimension area of 1 mm^2. The total output current can be scaled up by using a larger area. The device characteristics in double logarithmic scale with fixed V_G are shown in the Figure 3.6 for tracing the signature of SCLC. The dashed lines with slope equal to 1 and 2 are drawn in the Figure 3.6 for indication. Indeed, the current follows the SCLC once the barrier at the opening is suppressed by a positive enough V_C. At low voltage there is always a small ohmic current. The polymer diode has a turn-on voltage where

the current switches from a small leakage ohmic current into a quadratic SCLC current. The turn-on voltage is determined by both the level of the leakage and the difference between the work functions of the cathode and anode. Figure3.6 is shown the P3HT-based emitter-collector diode and the SCLC is about 2V.

3.2 Operation mechanism

The operation mechanism of the polymer SCLT can be understood as the quadratic space-charge-limited current between the emitter and the opening modulated by the grid potential. The potential at the center of the opening is a linear combination of grid and collector potential $\mu V_G + V_C$ in vacuum tube. The factor μ depends on the device geometry and increases with the ratio between the opening diameter and the grid-collector distance. The SCLC between the emitter and the opening is therefore approximately $C\varepsilon\mu\left(\lambda V_G + V_C\right)^2 / L^3$, where ε is the polymer dielectric constant and L is the emitter-top insulator distance. If the potential across the opening were uniform, the factor C would be the standard SCLC value of 9/8. The overall effect of non-uniform potential in our case can be absorbed into a numerical factor C. Because of the higher electric field, the space between the grid and the collector does not limit the collector current. Therefore the emitter-opening current given above is actually the output current. In this section, P-type (P3HT and Pentacene) and N-type (C60) are introduced respectively.

1. P3HT and Pentacene (P-type)：

The grid control of the current can be further illustrated by looking at the spatial distribution of the current across the opening. For P3HT and Pentacene, some region near the center of the opening has negative potential for holes to pass through. The effect of the grid near the edge is so significant that a potential barrier forms despite of the negative potential of the collector. The current is therefore confined in an area

controlled by the grid potential. As the transistor is in the on state, there is no barrier in all the area. The emitter-collector path through A position at the center and the path through B position (Figure 3.7(a)) near the edge of the opening have the potential profiles as the curves (x) and (y) in the Figure 3.7(b), respectively. Assuming that the collector current is roughly a superposition of the currents of many small diodes given by the paths through different positions, the small diodes at position A contributing to a high current (A_{ON}) and those at position B are just about to be turned on (B_{ON}), shown in the Figure 3.7(c). On the other hand, as the device is in the off state, the grid potential is positive and there is a potential barrier at the B position as the curve (z) in Figure 3.7(b), and the small diodes there is reverse biased (B_{OFF}). As for A position, if it also has the potential profile like curve (z) in Figure 3.7(b), the off current comes from small diodes at position A will be small. However, if the potential profile is as the curve (y), there would be an undesirable leakage current from the barely-on small diode at A (A_{OFF}). Theoretically an even more positive grid potential can drive it into curve (z). However in practice breakdown of the base/SIO/organic/collector diode may happen first.

2. C60 (N-type)：

The grid control of the current can be further illustrated by looking at the spatial distribution of the current across the opening. For C60, some region near the center of the opening has positive potential for electrons to pass through. The effect of the grid near the edge is so significant that a potential barrier forms despite of the positive potential of the collector. The current is therefore confined in an area controlled by the grid potential. As the transistor is in the on state, there is no barrier in all the area. The emitter-collector path through A position at the center and the path through B position (Figure 3.8(a)) near the edge of the opening have the potential profiles as the curves (x) and (y) in Figure 3.8(b), respectively. Assuming that the collector current is

roughly a superposition of the currents of many small diodes given by the paths through different positions, the small diodes at position A contributing to a high current (A_{ON}) and those at position B are just about to be turned on (B_{ON}), as indicated in Figure 3.8(c). On the other hand as the device is in the off state, the grid potential is negative and there is a potential barrier at the B position as the curve (z) in Figure 3.8(b), and the small diodes there is reverse biased (B_{OFF}). As for A position, if it also has the potential profile like curve (z) in Figure 3.8(b), the off current comes from small diodes at position A will be small. However, if the potential profile is as the curve (y), there will be an undesirable leakage current from the barely-on small diode at A (A_{OFF}). Theoretically an even more negative grid potential can always drive it into curve (z). However, in practice breakdown of the base/SIO/C60/emitter diode may happen first.

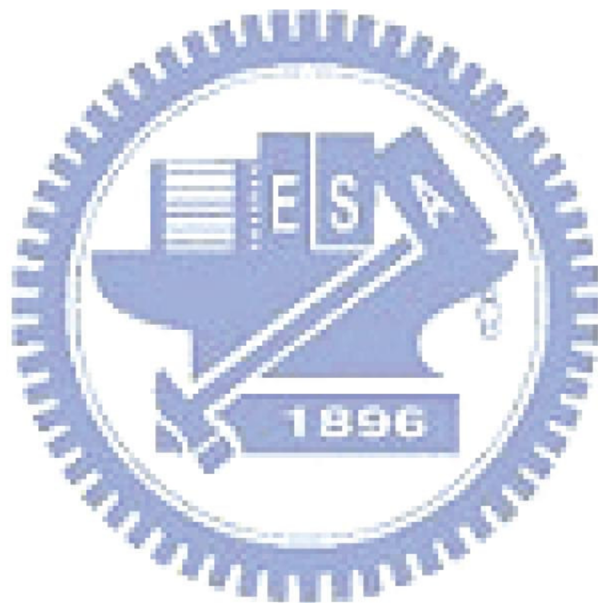
3.3 Discussion

To improve output current, pentacene and fullerene (C60) are used to fabricate as SCLTs. The J-V curves for emitter-collector diodes with different organic materials are compared in the Figure 3.9. Typical parameters are listed in Table I. Pentacene and C60 provide higher output current than P3HT for SCLTs from Table I. However, pentacene SCLTs and C60 SCLTs suffer from high leakage current even as base leakage is as low as in P3HT SCLTs. New leakage phenomena are proposed and discussed.

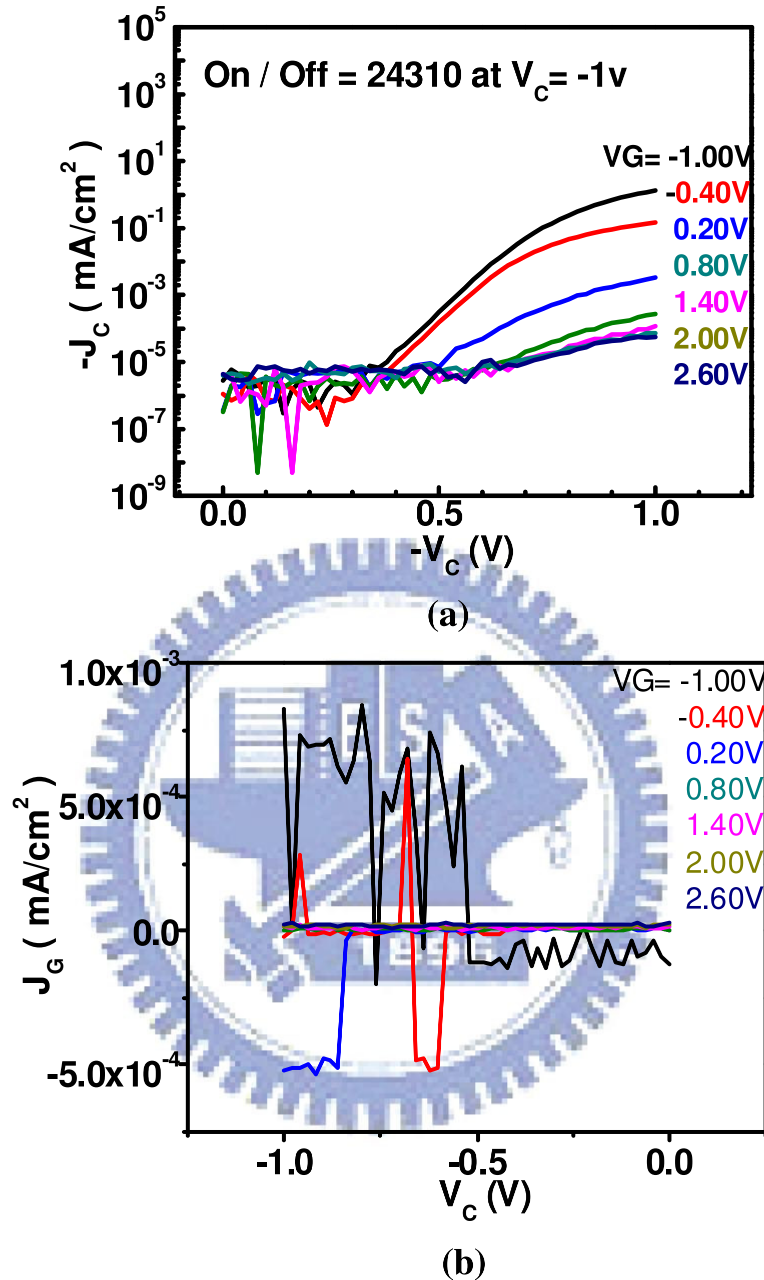
Morphology effect:

Leakage phenomenon is the morphology effect. AFM images of pentacene, C60, and P3HT above grid structure are compared in Figure 3.10(a), 3.10 (b) and 3.10(c). Surface profile reveals that the grain structure in pentacene and C60 produce holes while P3HT have rather smooth and dense morphology. Holes in pentacene/C60 make the top collector metal penetrates into pentacene/C60 film and shield the base electric

field. As a result, base metal looses ability to turn off the channel.



Chapter 3



(b)

Figure 3.1 The electric characteristics of the P3HT-based SCLT with various grid voltages applied. The Au electrode is commonly grounded and the Al collector is negatively biased at V_C with respect to Au. The negative collector current IC means the holes are collected by the Al collector and flows out from the transistor. The gate current I_G is no more than a few nA for all measurements. (a) The collector current as a function of the collector voltage various by step V_G. (b) The grid current as a function of the collector voltage of the transistor with same fabrication procedure described in (a).

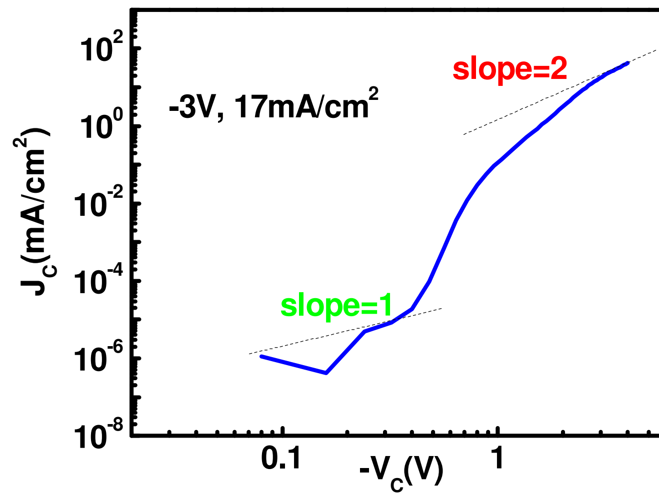
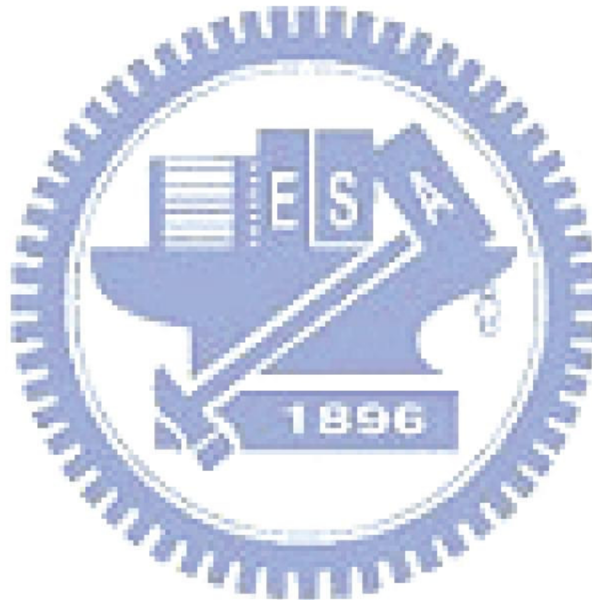
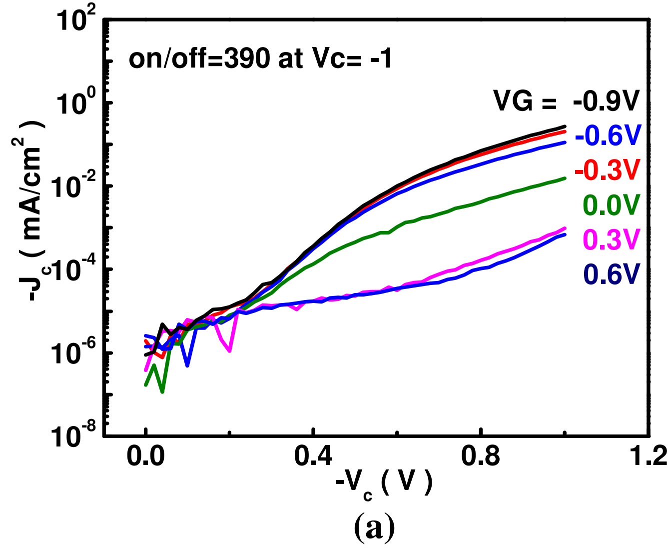
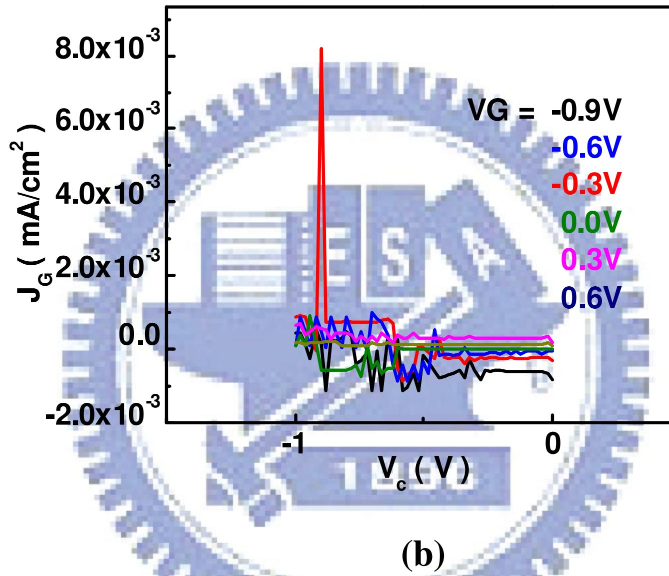


Figure 3.2 The electric characteristics of the P3HT-based SCLT in double logarithmic scale with fixed V_G.





(a)



(b)

Figure 3.3 The electric characteristics of the Pentacene-based SCLT with various grid voltages applied. The Au electrode is commonly grounded and the Al collector is negatively biased at V_C with respect to Au. The negative collector current IC means the holes are collected by the Al collector and flows out from the transistor. (a) The collector current as a function of the collector voltage various by step V_G. (b) The grid current as a function of the collector voltage of the transistor with same fabrication procedure described in (a).

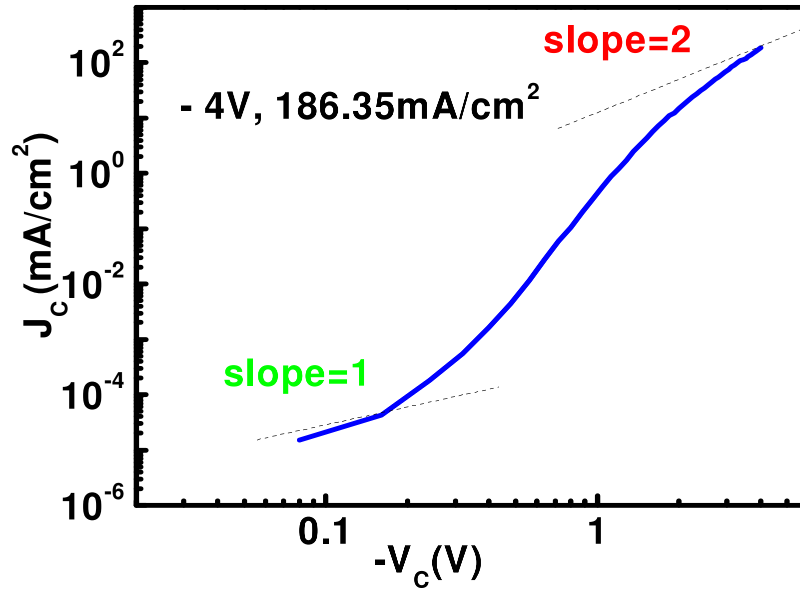
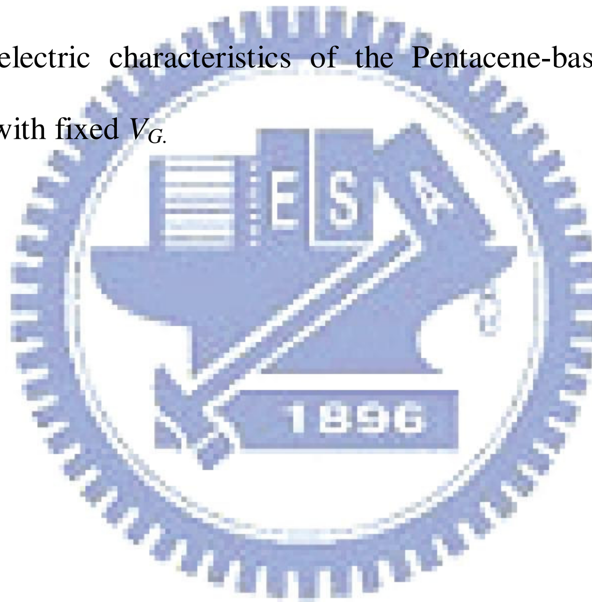
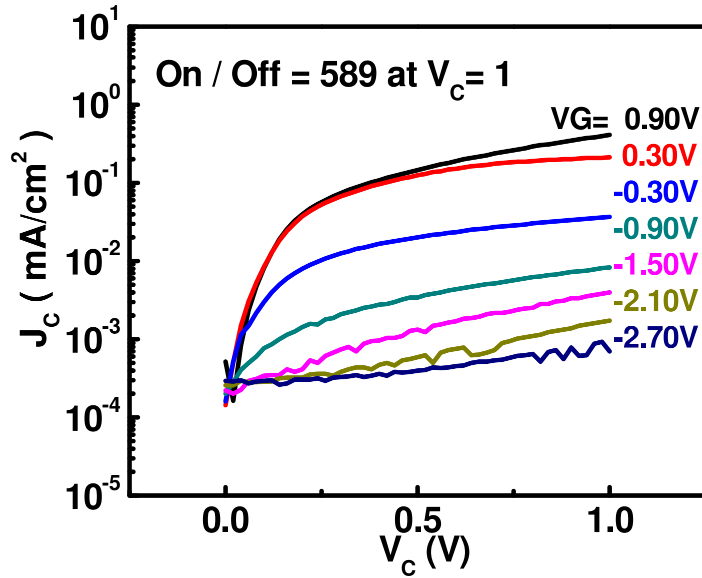
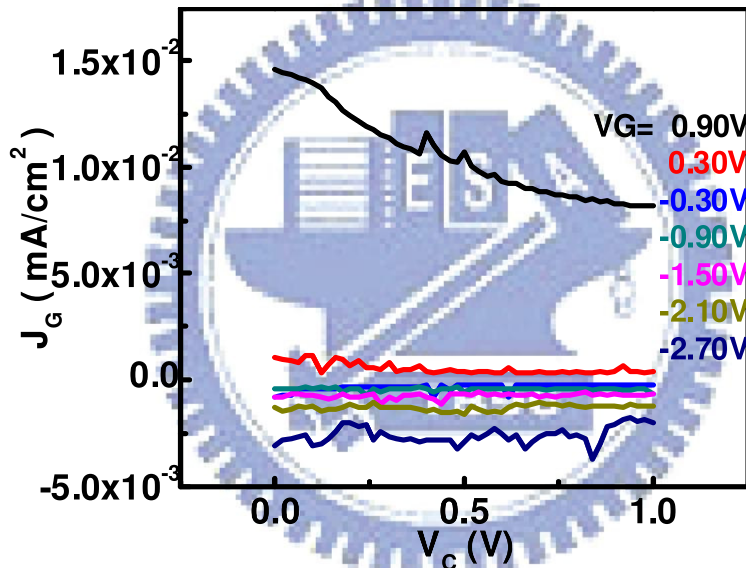


Figure 3.4 The electric characteristics of the Pentacene-based SCLT in double logarithmic scale with fixed $V_{G.}$





(a)



(b)

Figure 3.5 The electric characteristics of the C60-based SCLT with various grid voltages applied. The Al electrode is commonly grounded and the Au collector is positive biased at V_C with respect to Au. The collector current IC means the electrons are collected by the Au collector. (a) The collector current as a function of the collector voltage various by step V_G. (b) The grid current as a function of the collector voltage of the transistor with same fabrication procedure described in (a).

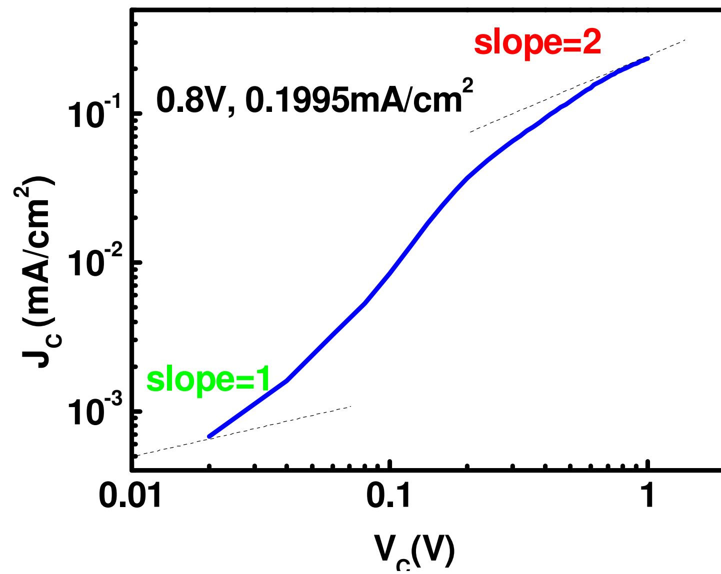
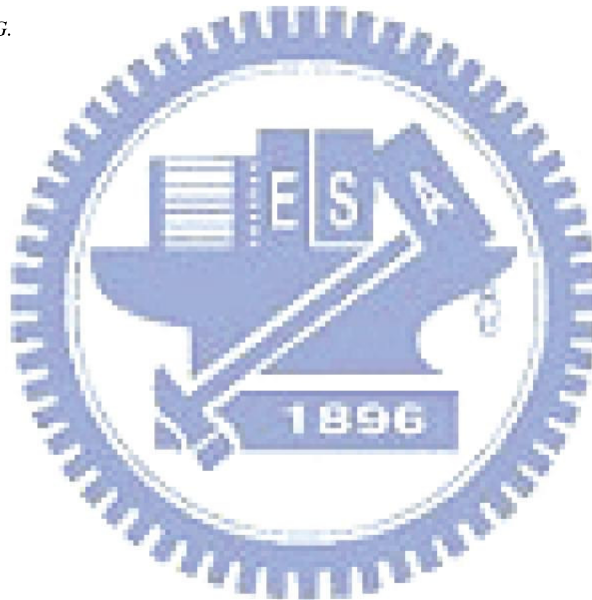


Figure 3.6 The electric characteristics of the C60-based SCLT in double logarithmic scale with fixed V_{G}.



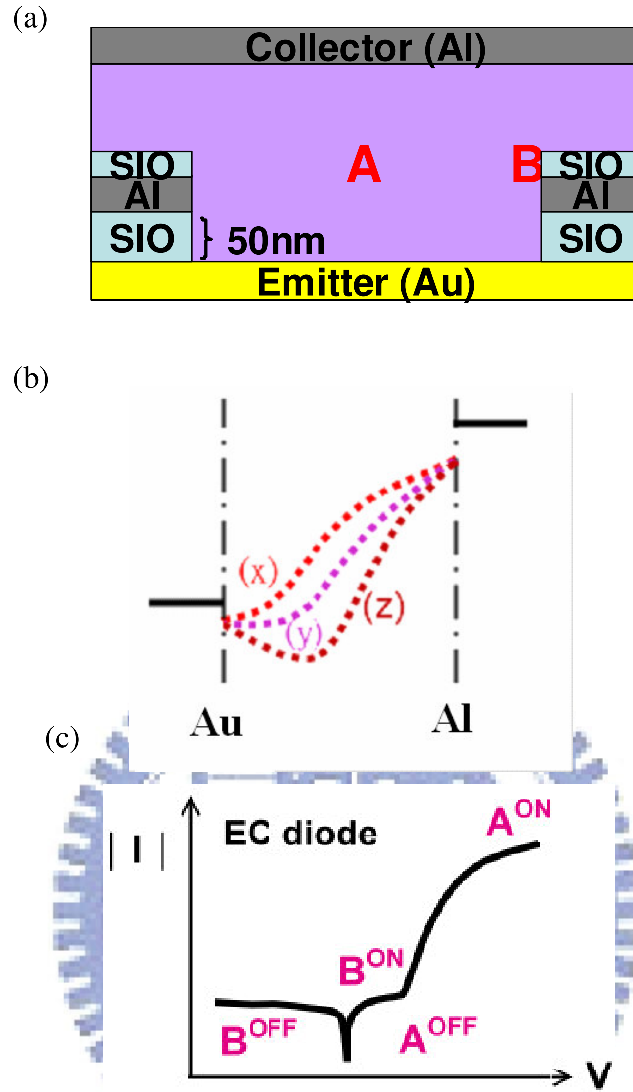


Figure 3.7 (a) The device structure near one opening of polymer SCLT. Position A is at the center of the opening, while position B is near the grid. (b) The potential profile along the emitter–collector path through the opening when VC is fixed at a negative value.(x), (y), (z) are the potential profile along the path for various conditions. (c) The schematic current–voltage curve of EC diode with the structure Au/P-type/Al. The path through position A in on or off state are denote as A^{ON} or A^{OFF} in the diode IV curve. The state of the path through B is also shown. Because of the proximity to the positive biased grid B path can never be fully turned on as A.

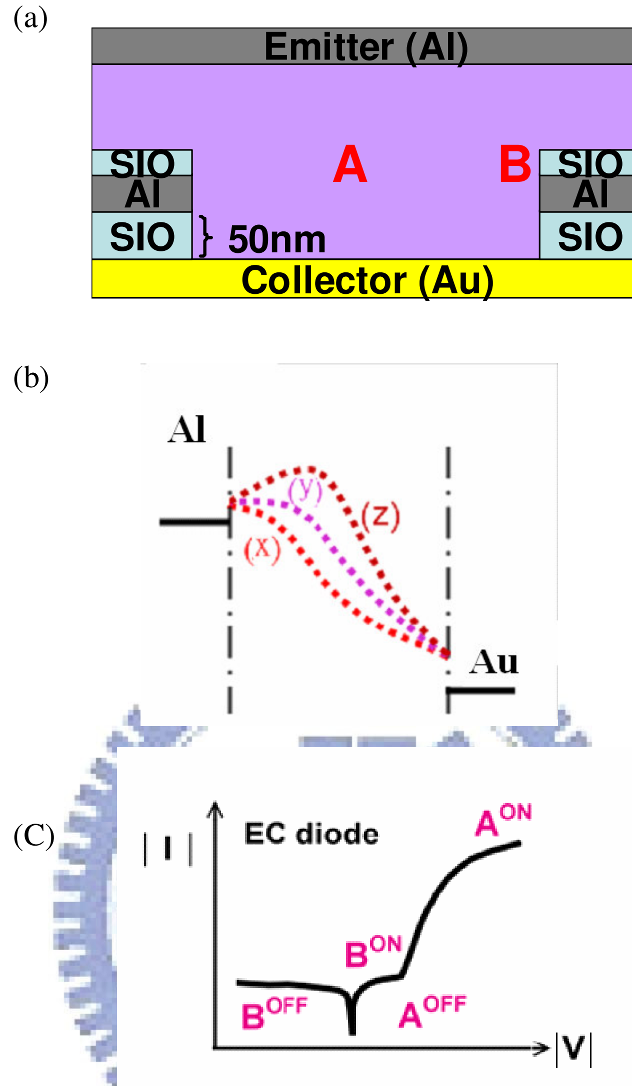


Figure 3.8 (a) The device structure near one opening of polymer SCLT. Position A is at the center of the opening, while position B is near the grid. (b) The potential profile along the emitter–collector path through the opening when VC is fixed at a positive value. (x), (y), (z) are the potential profile along the path for various conditions. (c) The schematic current–voltage curve of EC diode with the structure Au/C60/Al. The path through position A in on or off state are denote as A^{ON} or A^{OFF} in the diode IV curve. The state of the path through B is also shown. Because of the proximity to the negative biased grid B path can never be fully turned on as A.

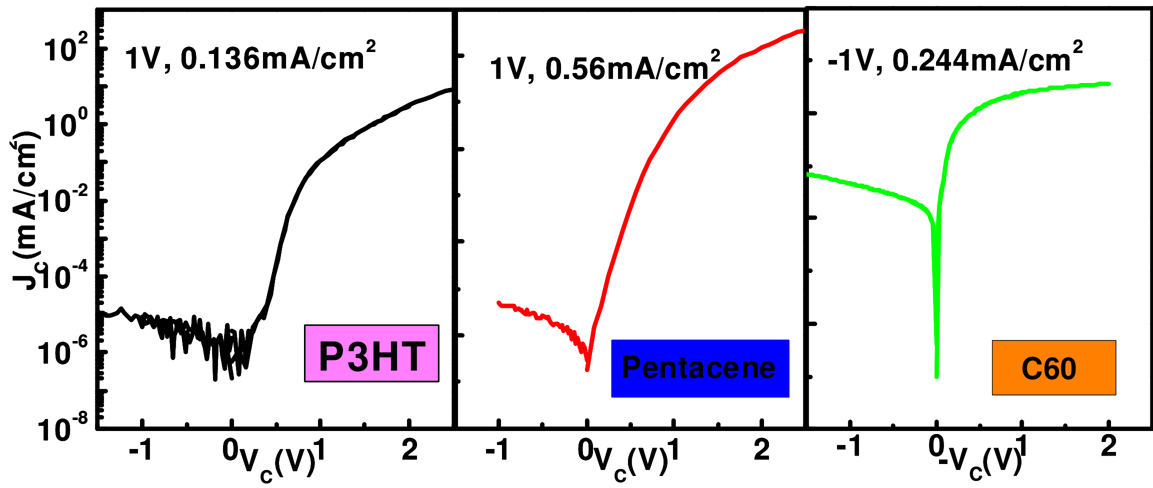


Figure 3.9 Current density – voltage curves for emitter–collector diodes made by P3HT, pentacene, and C60.

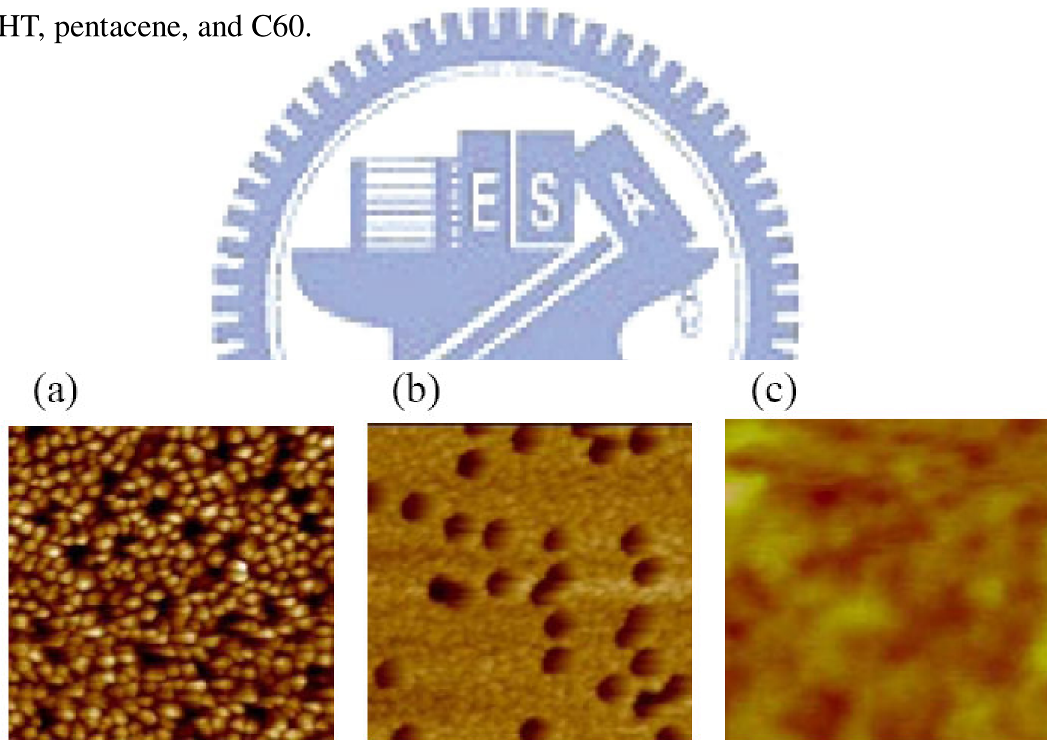


Figure 3.10 AFM images of (a) pentacene, (b) C60, and (c) P3HT above grid structure. The dimension of these images is 3um×3um.

Chapter 4

Self-Assembled Monolayer

4.1 Motivation

Structure of two-tier silicon oxide provides low leakage current, however the deposition of silicon oxide is very time-consuming. Section 4.2.1 will introduce two kinds self-assembled-monolayer (SAM) to replace the top silicon oxide. The benefits of SAM are fast fabrication, good coverage, and can reach the ideal order of leakage current. The metal (base) in chapter 3 is Aluminum (Al), therefore the binding force between Al and SAM is the key point to achieve good coverage. There is a thin film of alumina on Al surface, and alumina has good interaction with acid-based groups. Therefore, compound I, 4-hexadecyloxybenzoic acid, and Compound Ⅱ, n-octadecylphosphonic acid, are chosen in this chapter.

The metal (emitter) in chapter 3 is Gold (Au), but Indium Tin Oxide (ITO) is the most widely used as a transparent anode in organic electroluminescent (EL) devices due to its high conductivity, work function, and transparency in the visible spectral range. Therefore, in this chapter ITO is used as the follow-up study. Because the work function of ITO is generally not sufficiently large for the contact to be ohmic, there is a barrier to holes injection. Thus, various surface treatments of ITO have been attempted to change the work function of ITO in order to reduce the holes injection barrier height. The work function controlled by chemical modification has recently been applied to enhance holes injection at ITO. The compound Ⅲ, p-chlorobenzoyl chloride dichloride with –COCl binding groups are chosen in this work.

4.2 Materials

4.2.1 SAM as Dielectric

Compound Ⅰ:

Figure 4.1(a) is the chemical structure of compound I, 4-hexadecyloxybenzoic acid. The series of compound I was prepared from 4-hexadecyloxybenzoic acid (obtained from Tokyo Chemical Inc.) via alkylation of the hydroxy group with alkyl bromides according to a literature procedure. Compound I was dissolved in a mixture of n-hexadecane and THF (1:1, v/v) at a concentration of 0.25 mM and kept at 25 ℃.

Compound Ⅱ:

Figure 4.1 (b) shows the chemical structure of n-octadecylphosphonic acid. SAMs were prepared in a solution of 2-propanol at room temperature. Compound Ⅱ was dissolved in isopropanol at a concentration of 5 mM.

4.2.2 SAM as improving holes injection of Indium Tin Oxide

As we know, the work function of ITO is generally not sufficiently large for the contact to be ohmic and so there is a barrier for holes injection. Thus, various surface treatments of ITO have been attempted to change the work function of ITO to reduce the holes injection barrier height. The work function controlled by chemical modification has recently been applied to enhance holes injection at ITO. Figure 4.1 (c) shows the chemical structure of Compound Ⅲ, p-chlorobenzoyl chloride dichloride. It was dissolved in absolute alcohol at a concentration of 5 mM in this work. Figure 4.2 shows the schematic energy diagrams for ITO-treated/Pentacene/Al hole-only single-carrier devices.

4.3 Diode Fabrication

4.3.1 Metal (Al)/Insulator (SAM)/Metal (Al)

Figure 4.3 shows the structure of the diode (Al/SAM/Al) and diode.

Glass substrate clean

Glass substrate (CORNING Eagle 2000) must keep clean or films may become rough. The rough surface would cause point discharge between the insulator and

metal. The steps of clean glass substrate are shown as.

Steps:

(1) De Ion (DI) water current flows for 5 minutes in order to remove the particles.

(2) The substrates should be placed into the in the acetone and under the ultrasonic resonance for 5 minutes in order to remove the organic pollution. Then, the substrates have to put under the DI water current flow for 5 minutes in order to remove the solvent.

(4) The substrates were put in the KG detergent bath with ultrasonic resonance for 5 minutes in order to remove the particles, fingerprint, and ionic.

(5) The substrates were put under the DI water current flow for 5 minutes in order to remove the solvent.

(6) Finally, the substrates would be fried with dry N_2 flow to blow off the water on the substrates.

Bottom and Top metal deposition:

The deposition was started at the pressure around 5×10^{-6} torr. The 50-nm-thick Al was deposited by thermal evaporation at a deposition rate of 5Å/s. The region was defined by shadow mask.

Compound Ⅰ:

The substrate was exposed under the ultra-violate light for 15 mins to keep surface clean first. It was immersed in the solution containing compound I for four minutes. Then, it was cleaned surface by hexane-soaked tissue.

Compound Ⅱ:

The substrate was exposed under the ultra-violate light for 15 mins to keep

surface clean first. It was immersed in the solution containing compound Ⅱ for four minutes. Then, it was cleaned surface by isopropanol.

4.3.2 Al/SAM/Organic/Al

Figure 4.4 shows the structure of the diode (Al/SAM/organic/Al) in this work. This section just introduced the organic layer deposition and other processes were same as section 4.2.1. From the result of section 4.3 compound Ⅱ was be used in this section.

Organic active layer fabrication:

4. **P3HT:**

P3HT was spin coated from chlorobenzene solution (2.5 wt% 1000rpm) on the Au layer, and baked at 200 °C for 10min in vacuum. After we spin coated the P3HT film, we use acetone to clean the unnecessary area. Then, a thin P3HT layer of about 1338 Å was obtained.

5. **Pentacene**

The pentacene material obtained from Aldrich without any purification was directly placed in the thermal coater for the deposition. The deposition was started at the pressure around 3×10^{-6}torr. The 500Å -thick pentacene was deposited by thermal evaporation at a deposition rate of 1Å/s. The active region was defined by shadow mask.

6. **C60**

The substrate was exposed under the ultra-violate light for 15min to keep surface clean. The C60 was directly placed in the thermal coater for the deposition. The deposition was started at the pressure around 3×10^{-6}torr. The 200-nm-thick C60 was deposited by thermal evaporation at a deposition rate of 1Å/s. The active region was defined by shadow mask.

4.3.3 ITO/SAM/Organic/Al

Figure 4.5 shows structure of the diode (ITO/SAM/pentacene/Al) and the diode in this work. ITO glass was cleaned with acetone and isopropanol first. The sample was immersed in the solution containing compound Ⅲ for forty minutes. Then it was cleaned surface by absolute alcohol.

Organic active layer fabrication:

Pentacene

The pentacene material obtained from Aldrich without any purification was directly placed in the thermal coater for the deposition. The deposition was started at the pressure around 3×10^{-6}torr. The 180-nm-thick pentacene was deposited by thermal evaporation at a deposition rate of 1Å/s. The active region was defined by shadow mask.

Top metal deposition

The deposition was started at the pressure around 5×10^{-6}torr. The 50-nm-thick Al was deposited by thermal evaporation at a deposition rate of 5Å/s. The region was defined by shadow mask.

4.4 Diode characteristics

4.4.1 SAM as Dielectric

Figure 4.6 shows the insulator characteristic of different SAM. Figure 4.7 shows the insulator characteristics of Al/SAM/organic/Al diodes. According to the structures of SAMs, the number of OH groups of compound Ⅱ is more than that of compound Ⅰ. Therefore, compound Ⅱ has better binding with Aluminum than compound Ⅰ. From the difference, the characteristic of compound Ⅱ is better than that of compound Ⅰ. Compound Ⅱ is chosen as insulator in this work.

4.4.2 SAM as improving holes injection of Indium Tin Oxide

Figure 4.8 shows the *J-V* characteristics of diode with ITO chemically modified with –COCl binding groups of *p*-chlorobenzene derivatives. In Figure 4.8, *J-V*

characteristics of hole-only single-layer devices with ITO modified with *p*-chlorobenzene derivatives with –COCl binding groups are compared with those of the device with as-cleaned ITO. While ITO treated with –COCl gave the intermediate *J*-*V* characteristics that are much better than those of as-cleaned ITO. These results suggest that the efficient hole injection into Pentacene. It is because that the increase in the work function of ITO covered with the two dipole layers introduced by the surface modification. Therefore, the device characteristics are strongly correlated with the change in the observed work functions of various modified ITO.

4.5 Discussion

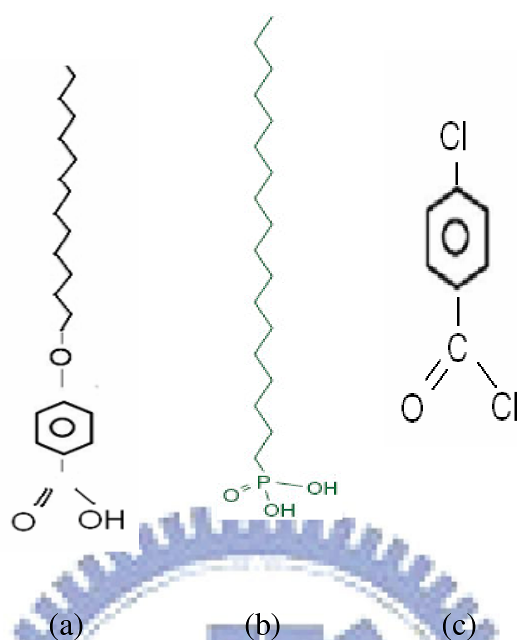
1. The characteristics of Al/SAM/Al and Al/SIO/Al.

Figure 4.9 shows the characteristics of Al/SAM/Al and Al/SIO/Al. When the operating voltage is 1V the leakage with thickness of SIO is 30-nm, the leakage current level is 10^{-2} to 10^{-3}mA/cm^2. When the operating voltage is 1V the leakage with n-octadecylphosphonic acid, the leakage current level is 10^{-3} to 10^{-4}mA/cm^2. The result of the insulating properties of n-octadecylphosphonic acid is superior to SIO. It is because that n-octadecylphosphonic acid uses functional groups to attach with alumina on aluminum surface. It can reduce the leakage current from the side of aluminum. Therefore, the benefits of n-octadecylphosphonic acid are fast fabrication, good coverage, and can reach the lower leakage current than SIO.

2. The difference of Au/pentacene/Al and ITO/pentacene/Al

Figure 4.10 shows the diode characteristics of different bottom metal. When the operating voltage is 1V the characteristic of ITO-based diode is better than Au-based diode. For our device operating voltage is no more than 1V, therefore under the condition ITO-based is better than Au-based for Pentacene SCLT.

Chapter 4



(a) (b) (c)

Figure 4.1 Self-assembled monolayer dielectrics (a) Chemical structure of 4-hexadecyloxybenzoic acid. (b) Chemical structure of n-octadecylphosphonic acid. (C) Chemical structure of p-chlorobenzoyl chloride dichloride.

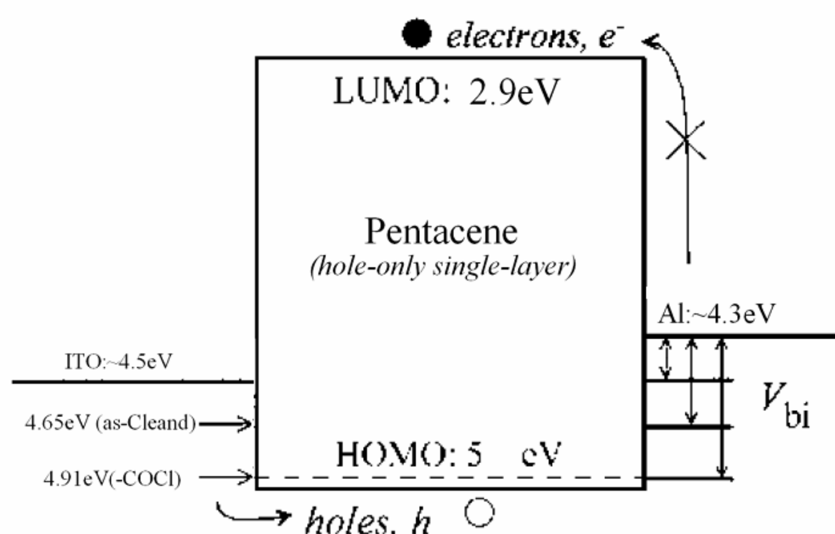


Figure 4.2 Schematic of energy diagrams for ITO treated/Pentacene/Al hole-only single-carrier devices.

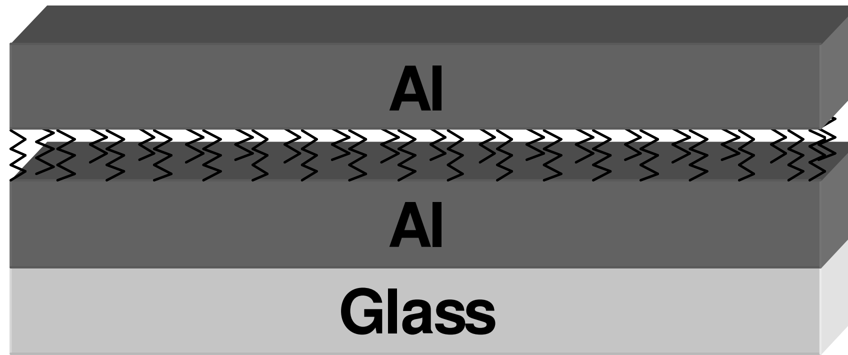


Figure 4.3 Structure of the diode (Al/SAM/Al) and diode.

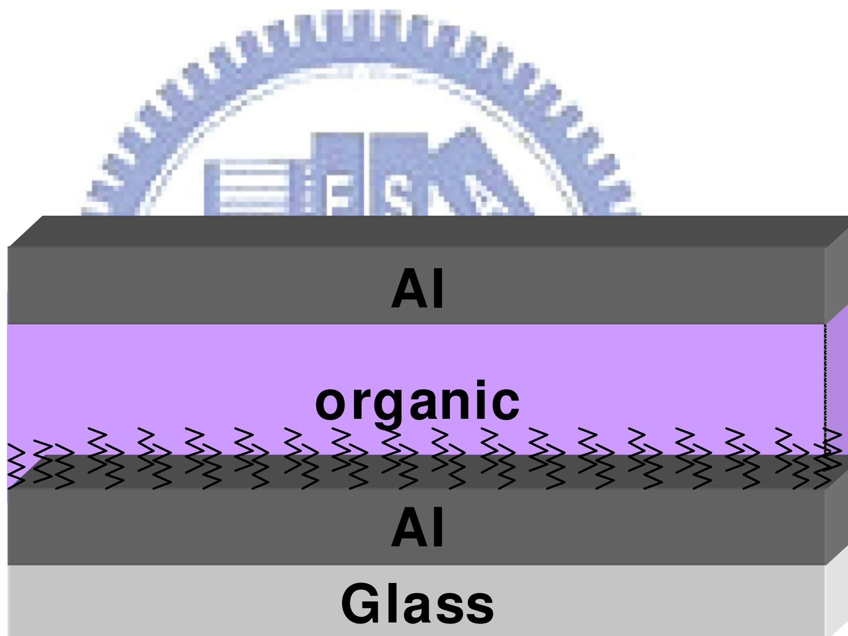


Figure 4.4 Structure of the diode (Al/SAM/organic/Al) in this work.

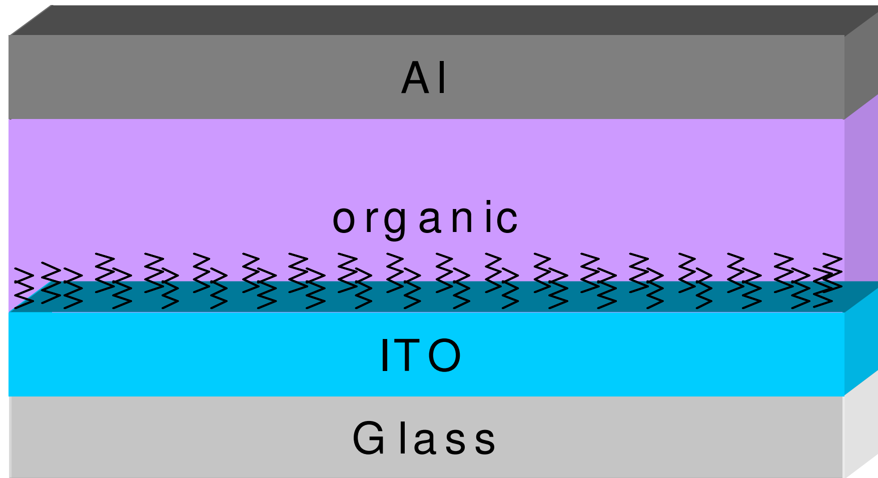
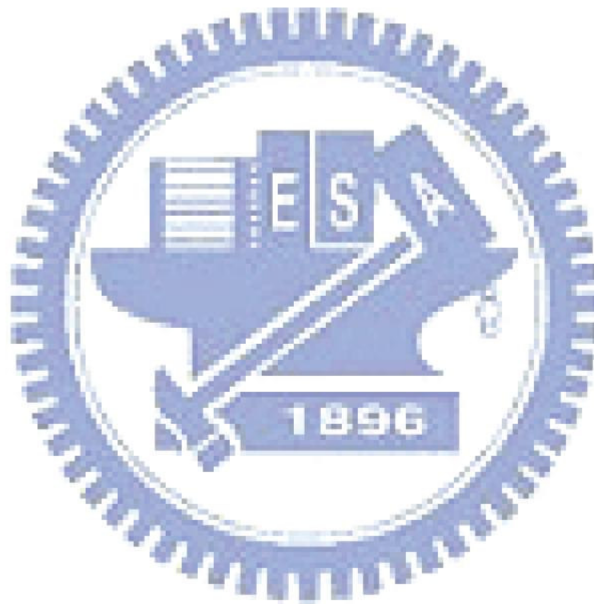
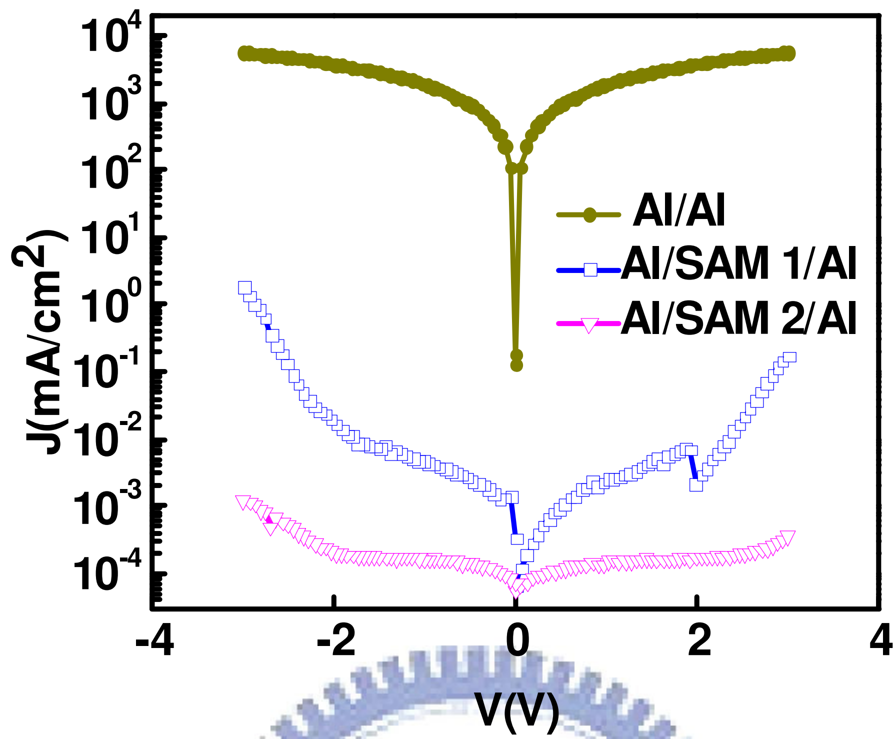


Figure 4.5 Structure of the diode (ITO/SAM /Al) and the diode in this work.





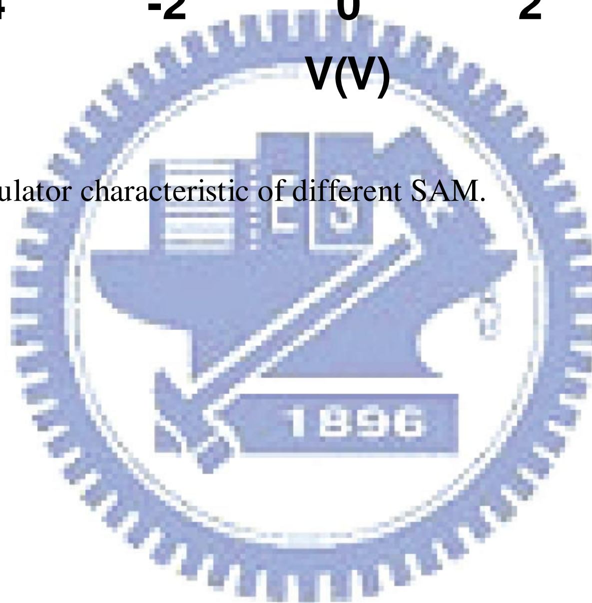
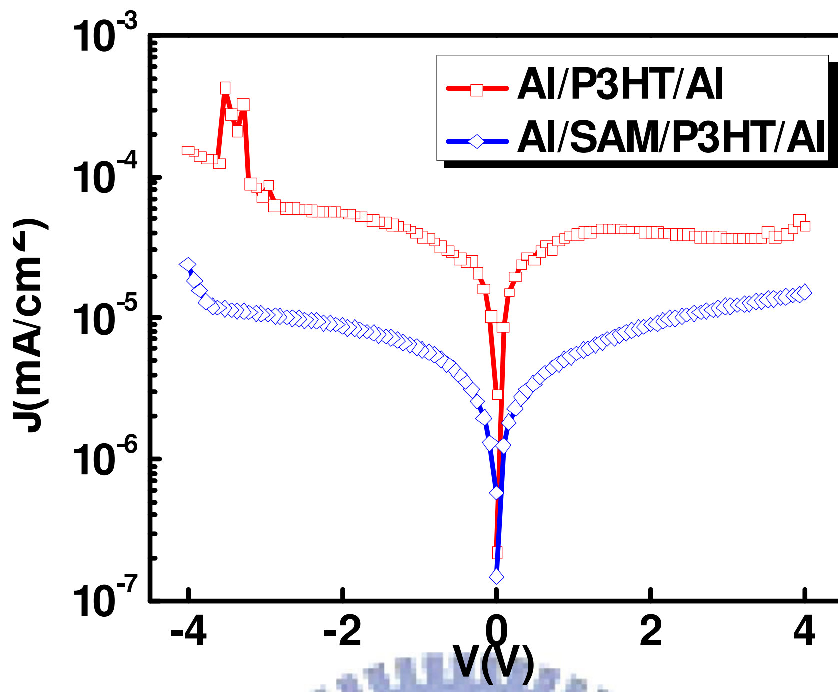
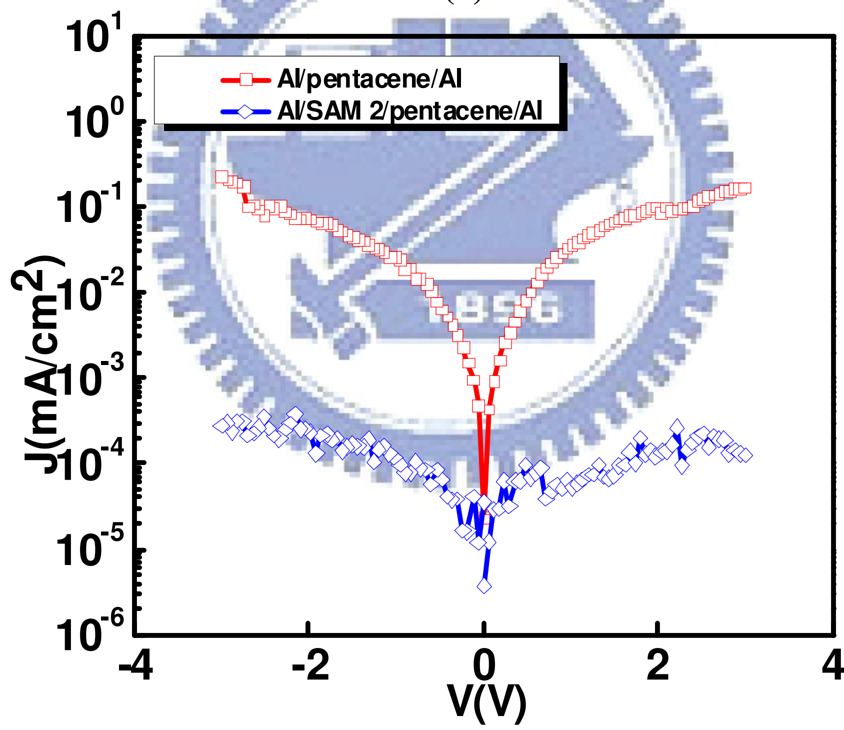


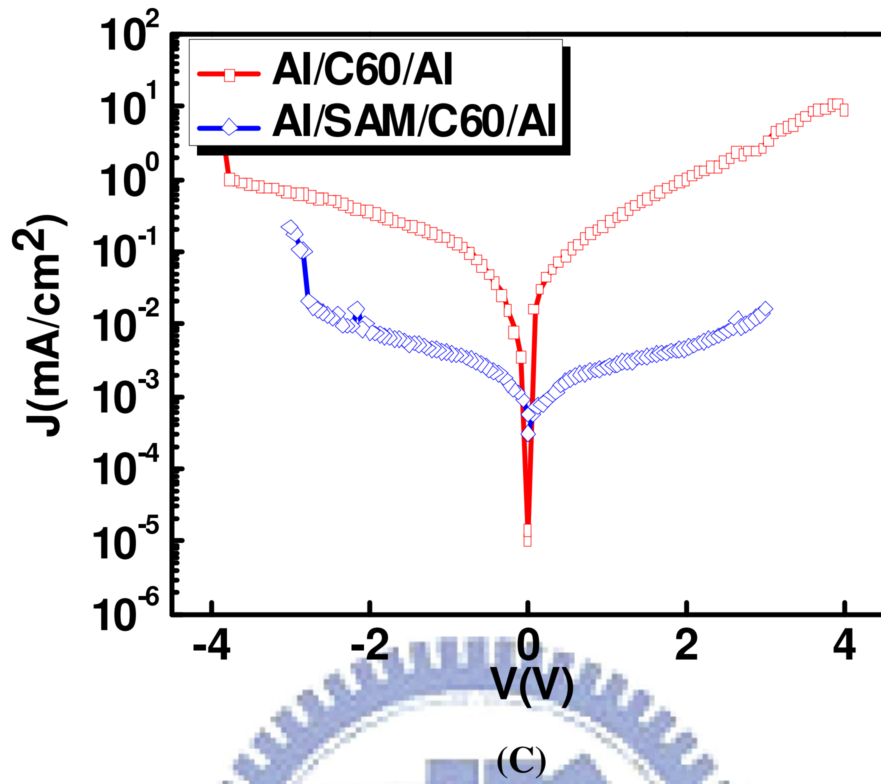
Figure 4.6 The insulator characteristic of different SAM.



(a)



(b)



(C)

Figure 4.7 The insulator characteristics of Al/SAM/organic/Al diodes. (a) Comparison of Al/P3HT/Al and Al/SAM/P3HT/Al, (b) Comparison of Al/Pentacene/Al and Al/SAM/Pentacene/Al and (c) Comparison of Al/C60/Al and Al/SAM/C60/Al

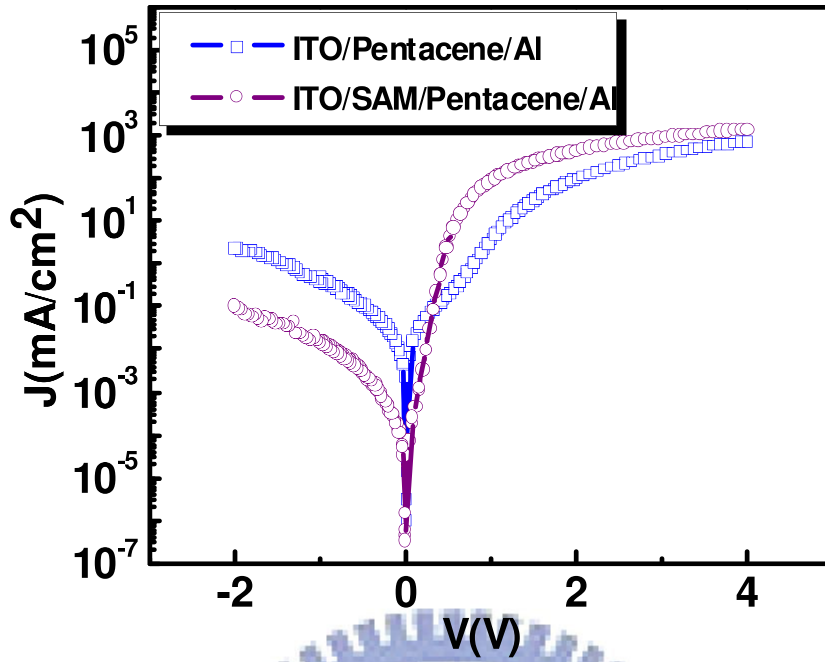


Figure 4.8 The *J-V* characteristics of diode with ITO chemically modified with –COCl binding groups of *p*-chlorobenzene derivatives

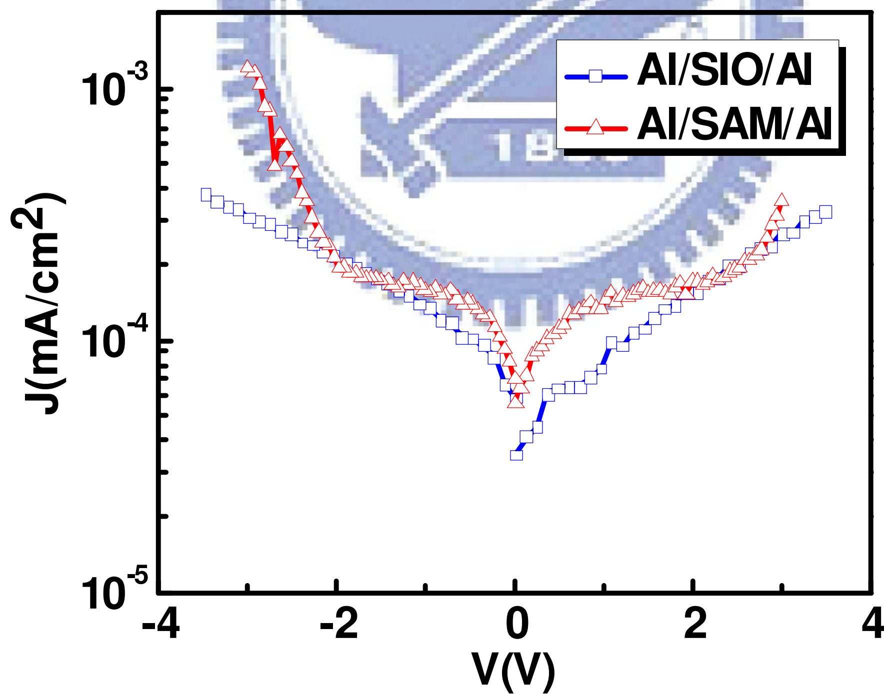


Figure 4.9 shows the characteristics of Al/SAM/Al and Al/SIO/Al.

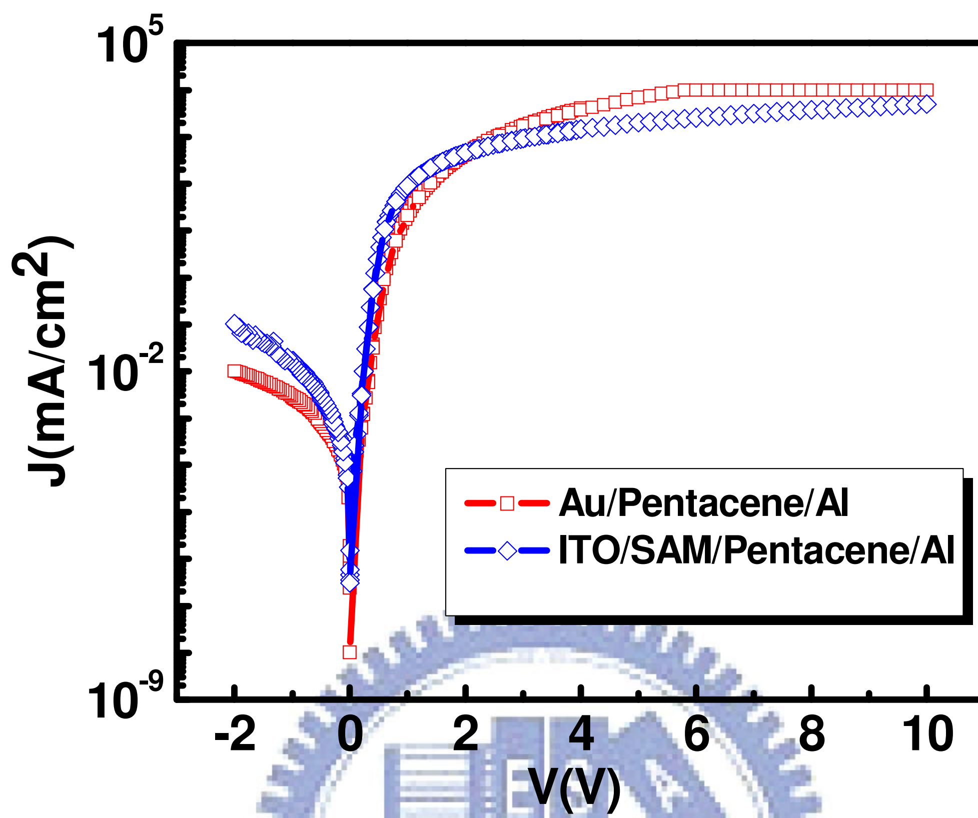


Figure 4.10 shows the diode characteristics of different bottom metal.

Chapter 5

Conclusions

We try to fabricate the low operation voltage space-charge-limited transistor (SCLT) with new structure and investigate the effects of self-assembled-monolayer (SAM) on Al or ITO surface. A 1-V P3HT-based SCLT with on/off current ratio 24310 is firstly demonstrated. Significant impacts of thin film morphology on the leakage current of organic SCLTs are firstly observed and recognized as new leakage phenomena. Surface profile reveals that the grain structure in pentacene/C60 produces holes make the top metal penetrates into pentacene/C60 film and shield the base electric field while P3HT have rather smooth and dense morphology. Therefore, pentacene SCLTs and C60 SCLTs suffer from high leakage current even when base leakage is as low as in P3HT SCLTs.

We tried to reduce the production time and increase output current by using SAMs. N-octadecylphosphonic acid using OH groups to attach with alumina on Al surface to reduce the leakage current from the side of Al. Therefore, it is faster fabrication, better coverage, and lower leakage current than SIO. P-chlorobenzene derivative with –COCl binding groups is used to increase the work function of ITO. For our device operating voltage is no more than 1V, therefore under the condition ITO-based is better than Au-based for Pentacene SCLT.

In future work, we will try to solve the morphology effect by spin solution-processed polymer on pentacene. We will fabricate SCLTs with various bottom metal based on this thesis results.

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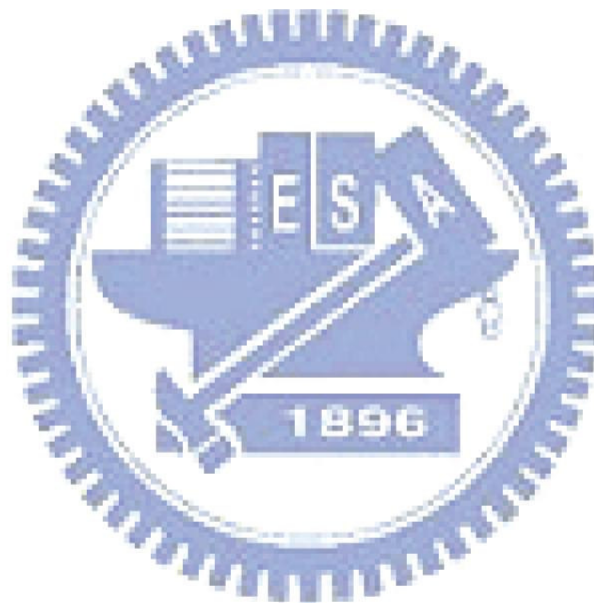

Table 3.1 Typical parameters of vertical transistors.

The characteristic of Space-Charge-Limited Transistors			
	V(V)	$J(mA/cm^2)$	$\mu_{SCLC}(cm^2V^{-1}S^{-1})$
P3HT	-3	17	1.51E-5
Pentacene	-4	186.35	2.27E-4
C60	0.8	0.1995	8.35E-6