應用於低暗電流和高光譜反應之互補式金氧半影像感測器分析與設計

THE ANALYSIS AND DESIGN OF CMOS IMAGERS FOR LOW-DARK-CURRENT AND HIGH-SPECTRAL-RESPONSE APPLICATIONS

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事由：推薦電子研究所博士班研究生施育全提出論文並參加國立交通大學博士論文口試。

說明：本校電子研究所博士班研究生施育全已完成電子研究所規定之學科及論文研究訓練。

有關學科部分，施君已修畢 18 學分(請查閱學籍資料)，通過資格考試及英文語文能力測驗；有關論文研究部分，施君已完成『應用於低暗電流和高光譜反應之互補式金氧半影像感測器分析與設計』論文初稿，並已有數篇相關之論文與專利發表或送審，茲列舉如下：

(A) JOURNAL PAPERS

[1] Ude Lu, Ben C.-P. Hu, **Yu-Chuan Shih**, Yuh-Shyong Yang, Chung-Yu Wu, Chiun-Jye Yuan, Ming-Dou Ker, Tung-Kung Wu, Yaw-Kuen Li, You-Zung Hsieh, Wensyang Hsu, and Chin-Teng Lin, “CMOS chip as luminescent sensor for biochemical reactions,” ***IEEE Sensors Journal***, vol. 3, pp. 310-316, June 2003.

[2] Chung-Yu Wu, **Yu-Chuan Shih**, Jeng-Feng Lan, Chih-Cheng Hsieh, Chien-Chang Huang, and Jr-Houng Lu, “Design, optimization, and performance analysis of new photodiode structures for CMOS active-pixel-sensor (APS) imager applications,” ***IEEE Sensors Journal***, vol. 4, pp. 135-144, Feb. 2004.

[3] **Yu-Chuan Shih** and Chung-Yu Wu, “A new CMOS pixel structure for low-dark-current and large-array-size imager applications,” accepted by ***IEEE Transactions on Circuits and Systems I***, Feb. 2004.

[4] **Yu-Chuan Shih** and Chung-Yu Wu, “Optimal design of CMOS pseudo-active-pixel-sensor (PAPS) structure for low-dark-current and large-array-size imager applications,” accepted by ***IEEE Sensors Journal***, Mar. 2004.

(B) CONFERENCE PAPERS

[1] **Yu-Chuan Shih** and Chung-Yu Wu, “The design of high-performance 128 x 128 CMOS image sensors using new current-readout techniques,” in *Proc.* ***IEEE***

International Symposium on Circuits and Systems, May 1999, vol. 5, pp. 168-171.

[2] **Yu-Chuan Shih** and Chung-Yu Wu, “A new CMOS imager using the pseudo-active-pixel-sensor (PAPS) circuit for high resolution applications,” in *Proc.* ***Enropean Conference on Circuit Theory and Design***, Aug. 2001, vol. 2, pp. 57-60.

[3] **Yu-Chuan Shih** and Chung-Yu Wu, “An optimized CMOS pseudo-active-pixel-sensor structure for low-dark-current imager applications,” in *Proc.* ***IEEE International Symposium on Circuits and Systems***, May 2003, vol. 1, pp. 809-812.

(C) PATENTS

[1] Chung-Yu Wu, **Yu-Chuan Shih**, Jeng-Feng Lan, Chih-Cheng Hsieh, Chien-Chang Huang, and Jr-Houng Lu, “The photodiode with the characteristics of low-leakage-current effects (可減少漏電流影響之光電二極體),” R.O.C. Patent No. 575969, Feb. 11, 2004.

總言之，施君已具備國立交通大學電子研究所應有的訓練水準。因此推薦施君參加國立交通大學電子研究所博士論文口試。

國立交通大學電子研究所教授　　　吳重雨　博士

應用於低暗電流與高光譜反應之互補式
金氧半影像感測器分析與設計

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摘要

本論文提出、分析並設計應用於互補式金氧半(CMOS)主動式像素影像感測器(Active Pixel Sensor imager)之新型光二極體架構和應用於低暗電流和大陣列數目影像感測器之新型互補式金氧半像素架構。論文中主要包含下列三個主要部份：(1)應用於互補式金氧半主動式像素影像感測器之新型光二極體架構設計、最佳化與成果分析；(2)應用於低暗電流與大陣列數目靜態影像感測器之新型互補式金氧半像素架構；(3) 應用於低暗電流與大陣列數目影像感測器之互補式金氧半虛擬主動式像素感測器(Pseudo Active Pixel Sensor)的最佳化設計。

首先，由於暗電流在互補式金氧半影像感測器的主動式像素感測單元中主要產生於經過局部氧化矽(LOCOS)過程後的鳥嘴區和高摻雜濃度沉積引起的表面損害。此外，淺和深的 pn 接面分別可以改善短波長光和長波長光的光感應度。為了減少暗電流和增加整體的光譜反應，吾人提出並分析利用 p 型基體和輕微摻雜濃度的感測器佈植 SN−當 pn 接面光二極體與其鳥嘴區分別被 SN−和 p-field 佈植包圍住的兩種新型光二極體架構。在 5 µm x 5 µm 的主動式像素感測單元中，採用了提出的光二極體架構並經過 0.35 µm 1P3M N-well 互補式金氧半技術的製造。從量測結果顯示，在 5 µm x 5 µm 主動式像素感測單元中，兩種吾人提出的光二極體架構與傳統架構及別的光二極體架構比較下，在 2 V 反相偏壓時有 30.6 mV/sec 和 35.2 mV/sec 的較低暗電流和較高的光譜反應。

其次，根據傳統的主動式像素感應器的像素架構，吾人提出一稱之為『虛擬主動式像素感應器』(Pseudo Active Pixel Sensor)的新型像素架構

並應用於靜態互補式金氧半影像感測器中。這個新型的像素架構和傳統被動式像素影像感測器(Passive Pixel Sensor imager)及主動式像素影像感測器相比，具有低漏電流、高訊號雜訊比例和高填充係數等優點。一種稱之為『行零偏壓緩衝直接注入式』(Zero-bias Column Buffer-Direct-Injection)的讀出電路架構也被提出，此種讀出電路偏壓光二極體和位於行匯流排的雜散pn接面於0 V或接近0 V來減少光二極體的暗電流和列開關的漏電流。改良式的雙重三角取樣(Double Delta Sampling)電路也被使用來減少固定樣式雜訊(fixed pattern noise)、時脈回饋雜訊和通道電荷注入。352 x 288(CIF)格式的互補式金氧半虛擬主動式像素影像感測器實驗晶片是經由0.25 μm 1P5M N-well互補式金氧半技術製造。像素的大小是5.8 μm x 5.8 μm。像素讀出速率從100 kHz到10 MHz，相當於最大的畫面速率(frame rate)超過30 frames/sec。這個提出的靜態互補式金氧半影像感測器還具有58%的填充係數、3110 μm x 2760 μm的晶片面積和操作在3.3 V電源供應時產生的24 mW功率消耗。這個實驗性的晶片已經成功地證明了新提出的虛擬主動式像素感測器架構並且可以應用在低暗電流和高解析度的大陣列數目靜態互補式金氧半影像感測器系統設計。

最後，根據吾人提出的虛擬主動式像素感測器的像素架構，一應用於互補式金氧半影像感測器的像素架構稱為『最佳化虛擬主動式像素感測器』(Optimal Pseudo Active Pixel Sensor)亦被提出、分析和設計。在像素中被共享的零偏壓緩衝器可保持光二極體和位於像素匯流排的雜散pn接面偏壓於0 V或接近0 V來減少光二極體的暗電流和像素開關的漏電流。每單位像素面積的光電流與暗電流比例(PDRPA)這個係數可以定義用來描述最佳化虛擬主動式像素感測器的性能特徵。當零偏壓緩衝器被四個像素共用時被發現具有最大的PDRPA。此外、行取樣電路和輸出相關雙重取樣電路也被用來減少固定樣式雜訊、時脈回饋雜訊和通道電荷注入。352 x 288(CIF)格式的互補式金氧半最佳化虛擬主動式像素影像感測器實驗晶片是經由0.25 μm 1P5M N-well互補式金氧半技術設計和製造。在這個製造的互補式金氧半影像感測器當中，每四個像素共用一個零偏壓緩衝器下的PDRPA值等於37.7 μm^{-2}。它也具有8.2 μm x 8.2 μm的像素大小、42%的填充係數和3630 μm x 3390 μm的晶片面積。量測到的最大畫面速率是30 frames/sec、暗電流為82 pA/cm^{2}。量測到的光動態範圍是65dB。與主動式像素感測器架構和傳統的被動式像素感測器架構相比較時，吾人所提出的最佳化虛擬主動式像素感測器架構具有較小的暗電

流、較高的填充係數和較高的光動態範圍。

根據以上的結果，我們深信吾人所提出新型光二極體架構可以被應用在具有小像素面積、高解析度和高品質的互補式金氧半影像感測系統中。此外，具有小像素面積、高填充係數和低暗電流等優點特徵之吾人所提出的新型互補式金氧半虛擬主動式像素影像感測器架構，將可以被應用在大陣列數目靜態互補式金氧半影像感測器設計中。吾人所提出之互補式金氧半最佳化虛擬主動式像素影像感測器和虛擬主動式像素感測器、主動式像素感測器、被動式像素感測器等互補式金氧半影像感測器相比較下有較低的暗電流，同時也比互補式金氧半主動式像素影像感測器有較高的填充係數。因此，吾人所提出之最佳化虛擬主動式像素感測器架構應用在高品質的互補式金氧半影像感測器時會具有較高的潛力。

THE ANALYSIS AND DESIGN OF CMOS IMAGERS FOR LOW-DARK-CURRENT AND HIGH-SPECTRAL-RESPONSE APPLICATIONS

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ABSTRACT

In this thesis, new photodiode structures for CMOS active pixel sensor (APS) imagers and new CMOS pixel structures for low-dark-current and large-array-size imager applications are proposed, analyzed, and designed. The main parts of this thesis include: (1) design, optimization, and performance analysis of new photodiode structures for CMOS APS imager applications; (2) a new CMOS pixel structure for low-dark-current and large-array-size still imager applications; (3) optimal design of CMOS pseudo active pixel sensor (PAPS) structure for low-dark-current and large-array-size imager applications.

Firstly, it is known that the dark current in the APS cell of a CMOS imager is mainly generated in the regions of bird's beak after the LOCOS (local oxidation of silicon) process as well as the surface damage caused by the implantation of high doping concentration. Furthermore, shallow and deep pn junctions can improve the photo-sensitivity for light of short and long wavelengths, respectively. Two new photodiode structures using p-substrate and lightly-doped sensor implant SN− as pn junction photodiode with the regions of bird's

beak embraced by SN− and p-field implant, respectively, are proposed and analyzed to reduce dark current and enhance the overall spectral response. 5 μm x 5 μm APS cells fabricated in a 0.35 μm single-poly-triple-metal (1P3M) N-well CMOS process are designed by using the proposed photodiode structures. As shown from the experimental results, the two proposed photodiode structures of 5 μm x 5 μm APS cells have lower dark currents of 30.6 mV/sec and 35.2 mV/sec at the reverse-biased voltage of 2 V and higher spectral response, as compared to the conventional structure and other photodiode structures.

Secondly, based on the conventional APS pixel structure, a new pixel structure for still CMOS imager application called the pseudo active pixel sensor (PAPS) is proposed and analyzed. It has the advantages of low dark current, high signal-to-noise ratio (SNR), and high fill factor over the conventional passive pixel sensor (PPS) imager or APS imager. The readout circuit called the zero-bias column buffer-direct-injection (ZCBDI) structure is also proposed to suppress both dark current of photodiode and leakage current of row switches by keeping both biases of photodiode and parasitic pn junction in the column bus at or near zero voltage. The improved double delta sampling (DDS) circuits are also used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. An experimental chip of the proposed PAPS CMOS imager with the format of 352 x 288 (CIF) has been fabricated by using 0.25 μm single-poly-five-level-metal (1P5M) N-well CMOS process. The pixel size is 5.8 μm x 5.8 μm. The pixel readout speed is from 100 kHz to 10 MHz, corresponding to the maximum frame rate above 30 frames/sec. The proposed still CMOS imager has a fill factor of 58%, chip size of 3110 μm x 2760 μm, and power dissipation of 24 mW under the power supply of 3.3 V. The experimental chip has successfully demonstrated the function of the proposed new PAPS structure. It can be applied in the design of large-array-size still CMOS imager systems with low dark current and high resolution.

Finally, based on the proposed PAPS pixel structure, a pixel structure called the optimal pseudo active pixel sensor (OPAPS) is proposed, analyzed, and designed for the applications of CMOS imagers. The shared zero-biased-buffer in the pixel is used to suppress both dark current of photodiode and leakage current of pixel switches by keeping both biases of photodiode and parasitic pn junctions in the pixel bus at zero voltage or near zero voltage. The factor of photocurrent-to-dark-current ratio per pixel area (PDRPA) is defined to characterize the performance of the OPAPS structure. It is found that a zero-biased-buffer shared by four pixels can achieve the highest PDRPA. In addition, the column sampling circuits and output correlated double sampling (CDS) circuits are also used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. An experimental chip of the proposed OPAPS CMOS imager with the format of 352 x 288 (CIF) has been designed and fabricated by using 0.25 μm single-poly-five-level-metal (1P5M) N-well CMOS process. In the fabricated CMOS imager, one shared zero-biased-buffer is used for four pixels where the PDRPA is equal to 37.7 μm^{-2}. The fabricated OPAPS CMOS imager has a pixel size of 8.2 μm x 8.2 μm, fill factor of 42%, and chip size of 3630 μm x 3390 μm. The measured maximum frame rate is 30 frames/sec and the dark current is 82 pA/cm^{2}. The measured optical dynamic range is 65dB. It is found that the proposed OPAPS structure has lower dark current, higher fill factor, and higher optical dynamic range as compared with the APS structure and the conventional PPS structure.

From the above results, it is believed that the proposed new photodiode structures can be applied to CMOS imager systems with small pixel size, high resolution, and high quality. Moreover, with the advantageous characteristics of small pixel area, high fill factor, and low dark current, it is expected that the proposed new PAPS CMOS imager structure can be applied to the design of large-array-size still CMOS imagers. The proposed OPAPS CMOS imager has the smaller dark current than those of PAPS, APS, and PPS CMOS imagers and higher fill factor than that of APS CMOS imager. Thus the proposed OPAPS structure has high potential for the applications of high-quality CMOS imagers.

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施育全
誌於 風城交大
九十三年秋

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Nowadays, the imaging system technology has been applied in various fields including camera [1]-[6], medical examination [7]-[9], surveillance systems [10]-[12], astronomy [13]-[15], military systems [16]-[18], and other strategic equipments [19]-[21]. The integration of commercial and military imaging systems has been recently developed and analyzed. Electronic imagers are one kind of popular imaging systems that have experienced continuing improvements over the past 10 years. The image quality is now approaching that of film.

Electronic imagers have come to dominate a wide range of markets. At the commercial end, electronic imagers are universally used for camcorders, scanners, digital still cameras, videophones, and recognition systems. At the high end, these devices are used in robotics, teleconferencing systems, and scientific applications. In addition, the medical industry often uses them for a variety of image scanning systems and applications.

Digital electronic cameras are the widest applications of electronic imagers, especially in computer peripherals for document capture and visual communications. The cost of the camera has been made sufficiently low, so that most personal computers almost have at least one camera peripheral. Even less expensive cameras will find entertainment applications. Wireless applications of cameras will require ultra-low-power operation. Very small cameras will also permit new markets.

Due to the wide applications in our daily life, all digital electronic cameras have the same basic functions. These are 1) optical collection of photons, i.e., a lens; 2) wavelength discrimination of photons, i.e., filters; 3) detector for conversion of photons to electrons, e.g., a photodiode; 4) a method to readout the detectors, e.g., a CCD; 5) timing, control, and drive electronics for the sensor; 6) signal processing electronics for correlated double sampling, color processing, etc.; 7) analog-to-digital conversion; and 8) interface electronics [22]. In a CCD-based system, these functions often consume several watts of power and are therefore a major drain on a battery. The volume and mass of the electronics and power supply constraints the level of miniaturization of the system [22].

In imaging systems, integration of the image sensor with circuit for both driving the image sensor and performing on-chip signal processing is becoming increasingly important [23]. A high degree of electronics integration on the focal-plane can enable miniaturization of instrument systems and simplify system interfaces. In addition to good imaging performance with low noise, no lag, no smear, and good blooming control, it is desirable to have random access, simple clocks, and fast readout rates. The development of a CMOS-compatible image sensor technology is an important step for highly integrated imaging systems since CMOS technology is well suited for implementing on-chip signal processing circuits. CMOS technology is also a widely accessible and well-understood technology.

The main factor contributing to the recent activity in CMOS image sensors [24]-[30] is the steady, exponential improvement in CMOS technology. The rate of minimum feature size decrease has exceeded the similar improvements in CCD technology [22]. Over the past ten years, there has been a growing interest in CMOS image sensors. The major reason for this interest is customer demand for miniaturized, low-power, and cost-effective imaging systems. CMOS-based image sensors offer the potential opportunity to integrate a significant amount of VLSI electronics on chip and reduce component and package costs. It is now straightforward to envision a single-chip camera that has integrated timing and control electronics, sensor array, signal processing electronics, analog-to-digital converter (ADC), and full digital interfaces. Such a camera-on-a-chip will operate with standard logic supply voltages and consume power measured in the tens of milliwatts [31]-[32].

With the rapid scaling down of CMOS technology, the design of multi-million-pixel high-resolution CMOS imagers [33]-[34] has become more and more challenging. Generally, small pixel size, low dark current, high fill factor, and high spectral response are required in the high-resolution CMOS imagers. The rate of pixel size decrease in CMOS imagers is shown in Fig.1.1. To achieve the optimal overall performance of CMOS imagers, a number of photodiode structures, pixel structures, and readout structures are developed for different system applications.

In this chapter, the background of CMOS image sensor is introduced first in Section 1.1. In Section 1.2, the design motivation of this thesis is described. Finally, the organization of this thesis is given in Section 1.3.

1.2 MOTIVATION

The photodiode is a key component of CMOS imagers. To achieve a high-performance CMOS imager, the photodiode should be designed and optimized carefully. The two critical parameters in the design of photodiodes for imager applications are the dark current and the spectral response. Large dark current in the photodiode array of CMOS imagers can lead to non-uniformity, low scalability, and reduced dynamic range. The first source of dark current depends on doping concentrations, bandgap, and temperature of the reverse-biased photodiode [35]. The second source is the defect-generated dark current determined by the shape of photodiode layout, the cross-sectional structure of the photodiode, and the fill factor [35]. The shape of photodiode layout can be designed to reduce the dark current [35]. Generally, the second source of dark current is mainly generated from the pn junction depletion region under bird's beak in LOCOS process [36] or in the interface isolation of STI (shallow trench isolation) as well as the surface damage caused by the implantation of high doping concentration. In addition, higher (lower) reverse-biased voltage of photodiode and parasitic pn junctions in the pixel leads to larger (smaller) dark current.

The spectral response is another important parameter considered in the design of photodiodes. The high spectral response of photodiodes can be generated by using shallow and deep depth of the pn junctions to absorb photons for light of short and long wavelengths, respectively.

In this thesis, both the operational requirements and structures of photodiode and pixel circuits are well studied and considered in detail. Two new photodiode structures for CMOS active pixel sensor (APS) imager applications are proposed and analyzed to reduce dark current and enhance the overall spectral response. In addition, a new pixel structure for still CMOS imager applications and its optimization is also proposed to have the advantages of lower dark current and higher fill factor over the conventional passive pixel sensor (PPS) imager or active pixel sensor (APS) imager. The proposed photodiode structures and pixel circuits can improve the overall performance of CMOS imager systems with innovative techniques and developments and can be applied to CMOS imagers with small pixel size, high resolution, and high quality. It is believed that the function and performance of CMOS imagers are well improved under our work.

1.3 ORGANIZATION OF THIS THESIS

This thesis contains six chapters, which include design, optimization, and performance analysis of new photodiode structures for CMOS active pixel sensor (APS) imager applications, a new CMOS pixel structure called pseudo active pixel sensor (PAPS) for low-dark-current and large-array-size still imager applications, and optimization design of CMOS pseudo active pixel sensor (PAPS) structure.

Chapter 1 introduces the background, describes the research motivation, and explains the main topics of this thesis.

In Chapter 2, a brief description of photodetectors in CMOS image sensors is outlined and their developments are reported. Then, the structures and operational requirements of CMOS image sensor are discussed. Finally, we will discuss and review the pixel circuits in CMOS image sensors including the state-of-the-art structures.

In Chapter 3, two new photodiode structures with low dark current and high spectral response are proposed. The pn junction of p-substrate and the lightly-doped sensor implant SN– is used as a photodiode in both structures. The regions of bird's beak in the two proposed structures are completely embraced by the SN– implant and the p-field implant, thus not located in the pn junction depletion region. Both pn junction depletion located under the bird's beak and surface damage due to high doping concentration can be avoided and the generation of dark current can be suppressed. Furthermore, the use of shallow and deep pn junctions can increase the photo-sensitivity for light of short and long wavelengths, respectively. Thus the spectral response can be improved. Systematic comparisons on measurement results of dark currents and spectral responses among the proposed photodiode structures and other structures in CMOS technology with reasonable process modifications are presented. From the experimental results, it has been verified that the two proposed structures in the 5 μm x 5 μm APS cell of the CMOS imager have low dark currents of 30.6 mV/sec and 35.2 mV/sec at the reverse-biased voltage of 2 V as well as good spectral response. The two proposed photodiode structures have lower dark current and higher spectral response as compared to the conventional structure and other photodiode structures.

In Chapter 4, a new pixel structure called the pseudo active pixel sensor (PAPS) for the large-array-size still CMOS imagers with low dark current and high fill factor is proposed. A new readout circuit is also proposed to readout the sensor current to the column bus and performs the outside-pixel integration using the APS-like structure. The new readout circuit keeps the biases of both photodiode and parasitic pn junctions in the column bus at or near zero bias to achieve low dark current, low column leakage current, and high linearity. The improved double delta sampling (DDS) circuit is used to reduce fixed pattern noise, clock feedthrough noise, and the noise from the effect of channel charge injection. An experimental chip of the proposed PAPS CMOS imager with the format of 352 x 288 (CIF) has been fabricated by using 0.25 μm single-poly-five-level-metal (1P5M) N-well CMOS process. The pixel size is 5.8 μm x 5.8 μm. The pixel readout speed is from 100 kHz to 10 MHz, corresponding to the maximum frame rate above 30 frames/sec. The proposed still CMOS imager has a fill factor of 58%, chip size of 3110 μm x 2760 μm, and power dissipation of 24 mW under the power supply of 3.3 V. The experimental chip has successfully demonstrated the function of the proposed new PAPS structure. It can be applied in the design of large-array-size still CMOS imager systems with low dark current and high resolution.

In Chapter 5, the optimal design of the structure of PAPS for the large-array-size

CMOS imagers with low dark current is presented and analyzed. In the proposed optimal PAPS (OPAPS) structure, a buffer circuit called the zero-biased buffer direct injection (ZBBDI) is shared by limited number of pixels to keep the photodiodes at zero or near zero bias and readout the selected pixel current [37]. Then the integration of readout current is performed by using an APS-like circuit. A new factor called the photocurrent-to-dark-current ratio per pixel area (PDRPA) is defined and optimized for the OPAPS structure. In the OPAPS design, both column sampling circuit and output correlated double sampling (CDS) circuit are used to reduce fixed pattern noise, clock feedthrough noise, and the noise from the effect of channel charge injection. An experimental chip of the proposed OPAPS CMOS imager with the format of 352 x 288 (CIF) has been designed and fabricated by using 0.25 μm single-poly-five-level-metal (1P5M) N-well CMOS process. In the fabricated CMOS imager, one shared zero-biased-buffer is used for four pixels where the PDRPA is equal to 47.29 μm^{-2}. The fabricated OPAPS CMOS imager has a pixel size of 8.2 μm x 8.2 μm, fill factor of 42%, and chip size of 3630 μm x 3390 μm. Moreover, the measured maximum frame rate is 30 frames/sec and the dark current is 82 pA/cm^2. Additionally, the measured optical dynamic range is 6 5dB. It is found that the proposed OPAPS structure has lower dark current, higher fill factor, and higher optical dynamic range as compared with the active pixel sensor (APS) and the conventional passive pixel sensor (PPS). Thus the proposed OPAPS structure has high potential for the applications of high-quality and large-array-size CMOS imagers.

Finally, the main results and conclusions of this thesis are summarized in Chapter 6. Some suggestions for the future works about the implementations of photodiode structure, pixel circuits, and readout circuits are also addressed in this chapter.

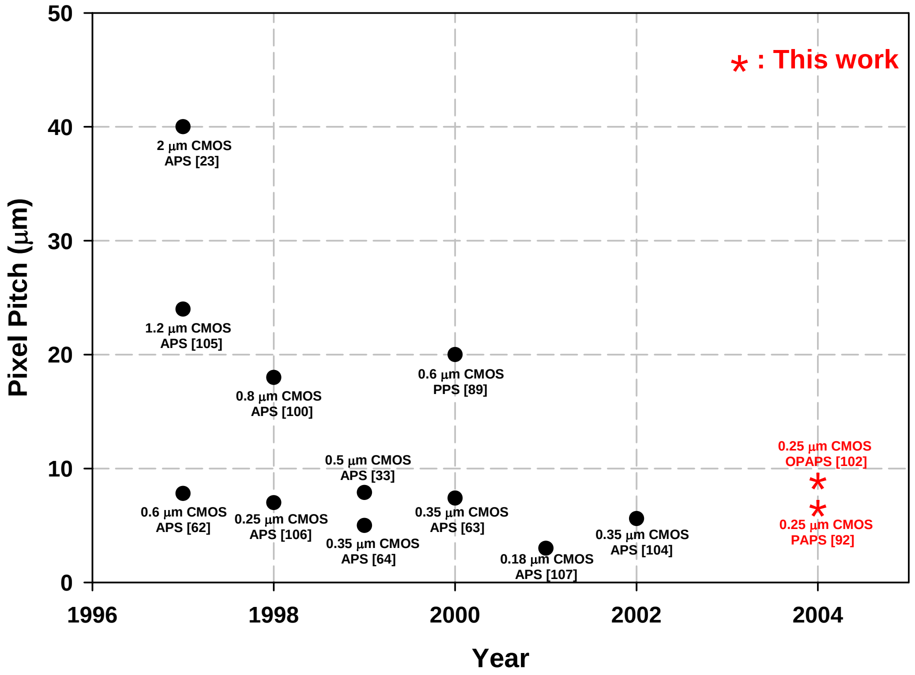


Fig. 1.1 The rate of pixel size decrease in CMOS imagers.

CHAPTER 2

REVIEW OF PHOTODETECTORS, PIXEL CIRCUITS, AND READOUT CIRCUITS IN CMOS IMAGE SENSORS

2.1 INTRODUCTION

In this chapter, the photodetectors and pixel circuits in CMOS image sensors are reviewed and discussed. The photodetectors for use in CMOS imaging systems are described in Section 2.2. In Section 2.3, the overall architectures and operational requirements of CMOS image sensors are discussed. In Section 2.4, the pixel circuits in CMOS image sensors are reviewed including the state-of-the-art structures. Finally, a summary is given in Section 2.5.

2.2 PHOTODETECTORS CMOS IMAGING SYSTEMS

In Imaging systems, a pixel array transduces light to an electrical quantity (charge, current, or voltage) over a two-dimensional scene. Nearly all visible-light solit-state imagers are based on the principle of carrier photogeneration. Photons entering a semiconductor generate electron-hole pairs if the photon energy exceeds the bandgap energy. An electric field separates the holes and electrons typically and then they are collected in a potential well and the holes are discarded. The major differences between imager types are related to how the electrons are converted to an output signal and how the array is scanned out.

Considerable researches have been devoted to use silicon as a material for photodetection. The interest in silicon for such applications derives almost from its dominant position in the semiconductor industry, where its properties are well understood and its manufacturing processes well established. Furthermore, because of its relatively large bandgap, silicon has low leakage current at room temperature.

In the electromagnetic spectrum [38], visible light is one of many subsets of electromagnetic radiation that also include radio waves, microwave, infrared radiation, X-rays, and γ-rays. The different forms of radiations are distinguished by their wavelengths, which for visible light ranges from about 0.4 μm (violet) to about 0.8 μm (red). A variety of interactions can be occurred between visible light photons and silicon [39]. Some of these interactions result in the conversion of photons into electrical charges, while others convert impinging photons into entity without electronic charges and other photons.

Photodetectors is a very important component in OEIC (OptoElectronic integrated Circuit) [40]. The possible applications range from artificial retina (neuro-vision), pattern recognition, alert and control [41], CCD/CMOS imager [42]-[45], and front end receiver in optical communication [46], [47]. There are many kinds of photodetectors available, and each of them has its own merits and weaknesses for a given applications.

There are several commonly used photodetectors in CMOS imaging systems, namely, charge injection device (CID) [48], static induction transistor (SIT) [49], [50], base-store image sensor (BASIS) [51], and floating gate array device (FGA) [52]-[54]. Moreover, two most commonly used structures of photodetector, namely, photogate (PG) [22], [55]-[57] and photodiode (PD) [58]-[61], are often used in CMOS imagers. Some comparisons among these photodetectors in CMOS imagers are summarized in Table 2.1. As can be shown in Table 2.1, photodiode is chosen as the photodetector in this thesis due to its good compatible with CMOS technology, high quantum efficiency, small pixel size, and random access. The medium fill factor can be improved by using microlens. In addition, the influence of noise can be improved by careful design of readout circuit.

There are many photodiode structures such as pinned photodiode [62], hole-accumulated photodiode [63], mixed P/N+ and P/N-well photodiode [64], and hollow photodiode [65]. The pinned photodiodes have small dark current, but the complex process may reduce yield and increase cost. It includes two junctions optimized independently of CMOS devices to improve the spectral response. Due to the same principle of the pinned photodiode and the distance of the sensor junction from the isolation region (LOCOS or STI region), the hole-accumulated photodiode structure has low dark current. It requires the same complex process as the pinned photodiode. The mixed P/N+ and P/N-well photodiode can absorb photons for light of short and long wavelengths by using P/N+ and P/N-well junctions, respectively. However, the structure is not scalable due to the large N-well width and space. The spectral response and quantum efficiency of the hollow photodiode are improved because of its extended depletion region. Controlling the uniformity of the hollow photodiode array is difficult due to the hollow shape of the photodiode.

2.3 OVERALL ARCHITECTURES AND OPERATIONAL REQUIREMENTS OF CMOS IMAGE SENSORS

2.3.1 Overall Architectures

The overall architecture of a CMOS image sensor is shown in Fig. 2.1. The image sensor consists of an array of pixels that are typically selected a row at a time by row select logic. This can be either a shift register or a decoder. The pixels are readout to vertical column busses that connect the selected row of pixels to a bank of analog readout circuits. These analog readout circuits perform functions such as charge integration, gain, sample and hold, correlated double sampling (CDS), and noise reduction.

More advanced CMOS image sensors contain on-chip ADC. The ADC can be column-parallel ADCs; that is, each column of pixels has its own ADC or a single ADC; that is, a single ADC is used in the overall CMOS imager sensor. The digital output of the ADC is readout to perform the off-chip digital signal processing. A timing and control logic block is also integrated on the same chip.

The CMOS image sensor architecture of Fig. 2.1 permits several modes of image readout. Progressive-scan readout of the entire array is the common readout mode. A window readout mode is implemented where only a smaller region of pixels is selected for readout. This increases access rates to windows of interest. A skip readout mode is also possible where every second (or third, etc.) pixel is readout, This mode allows for downsampling of the image to increase readout speed at the cost of resolution. Combinations of skip and window modes allow electronic pan, tilt, and room to be implemented.

2.3.2 Operational Requirements of CMOS Image Sensors

In different applications of CMOS imaging systems, there exist certain specific requirements for the design of CMOS image sensors. In general, the requirements involve quantum efficiency, conversion gain, saturation level, image lag, smear, crosstalk, anti-blooming, noise, dynamic range, readout rate, array size, and pixel pitch. Some general discussions of these requirements are summarized below.

1) *Quantum Efficiency* : Quantum efficiency is the probability that a photon incident on the pixel creates a hole or electron that is collected in the pixel’s potential well. Quantum efficiency depends on several parameters, including the reflection coefficient of the optical stack on the pixel, the fraction of the pixel area which is light-shielded, the fraction of the pixel area where photocharge goes elsewhere than the photosite, the photon wavelength, the bulk and surface carrier lifetimes, the depth of the potential well, and the volume and shape of the depletion regions. It is useful to think of quantum efficiency as the product of optical aperture, which is the fraction of pixel area which is optically active, optical stack transmission, which is the fraction of photons incident on optically active areas which reach the silicon surface, and collection efficiency, which is the fraction of photogenerated electrons that get collected.

2) *Conversion Gain* : The image data starts as charge and is usually converted to voltage. For an imager with a linear charge-to-voltage characteristic, the ratio of output signal to collected charge is a constant, referred to as the conversion gain. It is usually expressed in units of $\mu V/e^-$ and is equal to the reciprocal of the charge sense capacitance, times any system gain.

3) *Saturation Level* : Pixel saturation occurs when the pixel stores the maximum amount of charge. If more charge is added, it simply spills into the substrate or adjacent pixels. It is usually expressed in terms of electrons, although it is sometimes referred to the output as a voltage. It can also be stated in terms of illumination required to produce the saturation charge. Depending on design, the output circuit can saturate before the pixel saturates. In this case, the saturation level is set by the output circuit.

4) *Image Lag* : Image lag refers to the persistence of one frame in successive frames. An imager demonstrates lag when, for example, a strong light is suddenly

turned off but the imager output does not immediately return to the black level. Lag is usually caused by incomplete charge reset. It is informally characterized by whether or not it is visible on a video display.

5) Smear : In a CMOS imager, a charge packet passing by a region of high illumination accumulates additional charge due to optical crosstalk, creating vertical stripes in the reconstructed image. A column line can easily collect stray charge from a highly illuminated pixel, corrupting the readout of all pixels in that column.

6) Crosstalk : Crosstalk is any contamination of one pixel’s signal by another pixel’s signal. Smear is an example of optical crosstalk. Examples of electrical crosstalk include ground bounce and capacitive coupling.

7) Anti-Blooming : Blooming is the spread of charge from saturated pixels into surrounding potential wells. It differs from optical crosstalk in that all photogenerated charge, not just a small fraction, spreads out into the surrounding pixels/shift registers. Most pixels contain some means for shunting excess charge to a drain in order to preserve the information in nearby non-saturated pixels. Anti-blooming characterizes the effectiveness of the technique used to drain excess charge. It is expressed as the ratio of the illumination required to produce blooming to the illumination required to saturate the pixel.

8) Noise : Noise in the imager sensor can be separated typically into two categories, random noise and pattern noise. Random noise varied temporally and is not constant from frame to frame in the imager. Pattern noise is divided into two components, one is fixed pattern noise (FPN) and the other is the photo-response nonuniformity (PRNU). The FPN comes from dimensions, doping concentration, and contamination of photo-detectors and the characteristics of threshold voltage, width, and length in MOSFETS. The PRNU noise comes from the thickness of layers on the top of photo-detectors and wavelength of illumination. These noise in the CMOS imager sensor are briefly discussed below.

(i) Random Noise

An imager with a constant scene should produce identical output from frame to frame. In practice, the output from a given pixel will vary over time due to thermal noise, charge trapping, and 1/f noise in the devices which comprise the imager. Photonic shot noise is usually not included in this quantity, although this also contributes to noise at the output. Random noise is typically stated in terms of input-referred equivalent electrons, i.e., the root mean square (rms) output voltage noise divided by the conversion gain.

(ii) Fixed-Pattern Noise

Fixed-pattern noise (FPN) is the fixed (constant in time) variation between pixel outputs under spatially uniform illumination. Fixed-pattern noise is typically due to random or mask-induced mismatches in device parameters such as threshold voltage, trap density, and parasitic capacitance. FPN is usually a function of illumination, and can be written as the sum of a gain term and an offset term for an imager with a linear response characteristic. Offset FPN is constant over illumination, and gain FPN is proportional to illumination.

FPN consists of components that describe variation between columns, and variation between pixels in a single column. Column FPN is the standard deviation of the column-average pixel output values in a time-average, uniformly illuminated frame. The column FPN is expressed as

$$\text{FPN (column)} = \sqrt{\frac{\sum_{j}(\overline{P}_j - \overline{P})^2}{j-1}} \tag{2.1}$$

where $\overline{P}_j$ is the average pixel value in column j and $\overline{P}$ is the average pixel value in the frame. Since a column FPN calculation requires multiple columns, $j > 1$. Pixel FPN is the standard deviation of pixel output values after column FPN has been removed. In order to calculate pixel FPN, multiple pixels are required. The pixel FPN is expressed as

$$\text{FPN (pixel)} = \sqrt{\frac{\sum_{i,j}(\overline{P}_{i,j} - \overline{P}_j)^2}{i \bullet j-1}} \tag{2.2}$$

where $i \bullet j > 1$.

(iii) Reset Noise

If the diffusion of the photodiode is reset through a MOSFET, this is equivalent to a capacitance being charged through the resistance of the MOSFET channel. The rms (root-mean-square) noise voltage can be expressed as

$$\langle V_{rms} \rangle = \sqrt{\frac{kT}{C}} \tag{2.3}$$

where k is the Boltzmann constant, T is temperature, and C is the capacitance of photodiode. The reset noise is generally called “KTC” noise. KTC noise can only be canceled by using the photogate-type active pixel sensor (APS). Currently, reset noise limits the read noise in photodiode-type APS [22].

(iv) Thermal Noise

Thermal noise is a white noise which means the noise power is constant over all frequencies. For a resistor, the thermal noise rms voltage can be expressed as

$$\langle V_{rms} \rangle = \sqrt{4kTBR} \tag{2.4}$$

where B is the noise bandwidth and R is the resistor. Since the thermal noise covers the entire frequency range, the bandwidth determines the actual amount measured.

(v) Shot Noise

Shot noise is another white noise that arises from the discrete nature of the electrons, for example, the random arrival of particles of charge. This is the result of the random generation of carriers such as thermal generation within a depletion region (i.e. shot noise of dark current) or the random generation of photon-electrons.

(vi) Flicker (1/f) Noise

The flicker noise occurs at any junction, including metal-to-metal, metal-to-semiconductor, semiconductor-to-semiconductor, and conductivity fluctuations. The flicker noise arises mainly in amplifier circuits where there are numerous such contacts. At low frequency, flicker noise can be the dominant component, but it drops below thermal noise at higher frequency.

9) Dynamic Range : The dynamic range is defined as the ratio of maximum charge capacity to noise floor. The required dynamic range of CMOS imagers is determined by the ratio of the brightest signal level to the weakest. Larger dynamic range is preferred but limited by storage capacitance, linearity, and noise level.

10) Readout Rate : The readout rate is chosen according to the specific imaging system requirements and limited by the allowable chip power dissipation as well as the circuit operation speed. Usually a higher readout rate is needed for multiple sampling applications in image compensation function. Higher readout rate is also needed to avoid the saturation of the signal after integration.

11) Array Size and Pixel Pitch : Higher image resolution requires larger array size and smaller pixel pitch. However, a larger pixel size is needed to increase the fill factor, photo-senstivity, and dynamic range. Thus the optimal design trade-off should be made between the application flexibility and resolution performance.

It is important to determine the operational requirements in the design of CMOS imager for specific applications. A complete analysis of operational parameters like noise, spectral response, sensitivity, and resolution should be set before the design trade-off. Therefore, all the operational requirements discussed above have unique optimized orientations for CMOS imagers in different applications.

2.4 PIXEL CIRCUITS OF CMOS IMAGE SENSORS

In the development of CMOS imagers, the pixel circuit is the second major part next to the photodetectors. Pixel circuit is designed to support a good interface between photodetectors and the following signal processing stage. Different pixel circuit techniques have been developed for CMOS imagers with different applications.

Generally, the pixel pitch of CMOS imagers is reduced with the increasing array size and resolution. Moreover, the total power and noise of pixels are limited by the imaging system. These three major factors often put constraints on pixel circuit design space and complexity. Thus the design of pixel circuits requires a trade-off between circuit performance and complexity.

Some conventional pixel circuits such as passive pixel circuit [66], [67], active pixel circuit [68]-[74], and logarithmic pixel circuit [22] are still commonly used in CMOS imagers. More complex pixel circuits have been developed to provide excellent bias control, high injection efficiency, high linearity, and low noise performance based on these conventional pixel circuits. In the following, these conventional pixel circuits used in CMOS imagers will be reviewed. The noise performance and dynamic range of these pixel circuits are also discussed.

2.4.1 Passive Pixel Circuit [66], [67]

The photodiode-type passive pixel circuit consists of one photodiode PD and a pass transistor Mpt as shown in Fig. 2.2. When the pass transistor Mpt is on, the photodiode is connected to a column bus. A charge integrating amplifier (CIA) readout circuit at the bottom of the column bus keeps the voltage on the column bus constant and reduces KTC noise [68]. When the photodiode is accessed, the voltage on the photodiode is reset to the column bus voltage, and the charge proportional to the photosignal, is converted to a voltage by the CIA. This single-transistor pixel circuit allows the highest fill factor for a particular CMOS process. The quantum efficiency of the passive pixel can be quite high due to the large fill factor.

The disadvantages of the passive pixel circuit are its readout noise level and scalability. Readout noise of a passive pixel is typically of the order of 250 electrons r.m.s. [22]. The passive pixel also does not scale well to larger array sizes and faster pixel readout rates. This is because increased bus capacitance and faster readout speed both result in higher readout noise.

2.4.2 Active Pixel Circuit [68]-[74]

After the invention of passive pixel circuit, the insertion of a buffer or an amplifier into the pixel can potentially improve the performance of pixel. A sensor with an active amplifier within each pixel is referred as an active pixel sensor (APS). Each amplifier is only activated during readout, so power dissipation can be kept low. The photodiode-type APS consists of one photodiode and three transistor as shown in Fig. 2.3. The CMOS APS trades pixel fill factor for improved performance compared to passive pixels. Microlenses are commonly used to compensate the loss in optical signal [75], [76].

The read noise of photodiode-type APS pixel is limited by the reset noise on the photodiode, and is thus typically 75-100 electrons r.m.s [22]. The reset noise scales as $1/C^{1/2}$ [22], where C is the photodiode capacitance. A trade-off can be made in pixel fill factor, dynamic range, and conversion gain. The photodiode APS is suitable for most mid to low performance applications.

2.4.3 Logarithmic Pixel Circuit [22]

In some cases, nonlinear output of the sensor is required [77]-[81]. The logarithmic pixel circuit is shown in Fig. 2.4. As shown in Fig. 2.4, the photodiode voltage self-adjusts to a level such that the load transistor current is equal to the photocurrent collected by the photodiode. This results in a logarithmic transformation of the photosignal for typical light levels and wide dynamic range. The disadvantages of this logarithmic approach are slow response time due to low light levels, large fixed pattern noise (FPN), and small signal-to-noise ratio (SNR) due to FPN, temporal noise, and small voltage swings [22].

2.5 READOUT CIRCUITS OF CMOS IMAGE SENSORS

2.5.1 Double Delta Sampling (DDS) Circuit [99]

The most commonly used readout circuit in CMOS imagers is double delta sampling (DDS) circuit [99] as shown in Fig. 2.5. The DDS circuit is composed of column sampling circuit and output correlated double sampling circuit. The two branches in column sampling circuit are used to store the reset and signal voltage. Each branch consists of a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and the first source follower with a column-selection switch (csel). The clamp switches, the coupling capacitors (COS and COR), and the output drivers are common to an entire column of pixels. The load transistors of the first set of source follower and the subsequent clamp circuits and output source followers are common to the entire array. The DDS circuit can be used to suppress fixed pattern noise (FPN) and clock feedthrough noise. The disadvantages of DDS circuit is the high noise due to channel charge injection.

2.6 SUMMARY

In this chapter, the photodetectors and pixel circuits in CMOS image sensors are reviewed and discussed. All the structures and circuits discussed above have their uniqueness and features for different applications. Based on the developments of photodetectors and the fast advancement of CMOS technologies, high-performance and low-cost CMOS imagers will be developed through the inventions of new photodiode structures and pixel circuits. This will be driven by rapid developments and wide applications of multimedia systems. In the following chapters, the advanced developments of photodiode structures and pixel circuits are proposed. Under our work in this thesis, a new generation of CMOS imaging systems is highly expected.

Table 2.1 Comparisons of characteristics among photodetectors in CMOS imagers

DEVICE PARAMETERS	CID	SIT	BASIS	FGA	PG	PD
CMOS Compatible	Poor	Medium	Medium	Medium	Medium	Good
Fill Factor	High	Medium	Medium	High	Medium	Medium
Quantum Efficiency	Medium	Medium	Medium	Low	Medium	High
Noise	Large	Medium	Medium	Medium	Small	Medium
Pixel Size	Small	Medium	Medium	Small	Medium	Small
Random Access	Yes	Yes	Yes	Yes	Yes	Yes

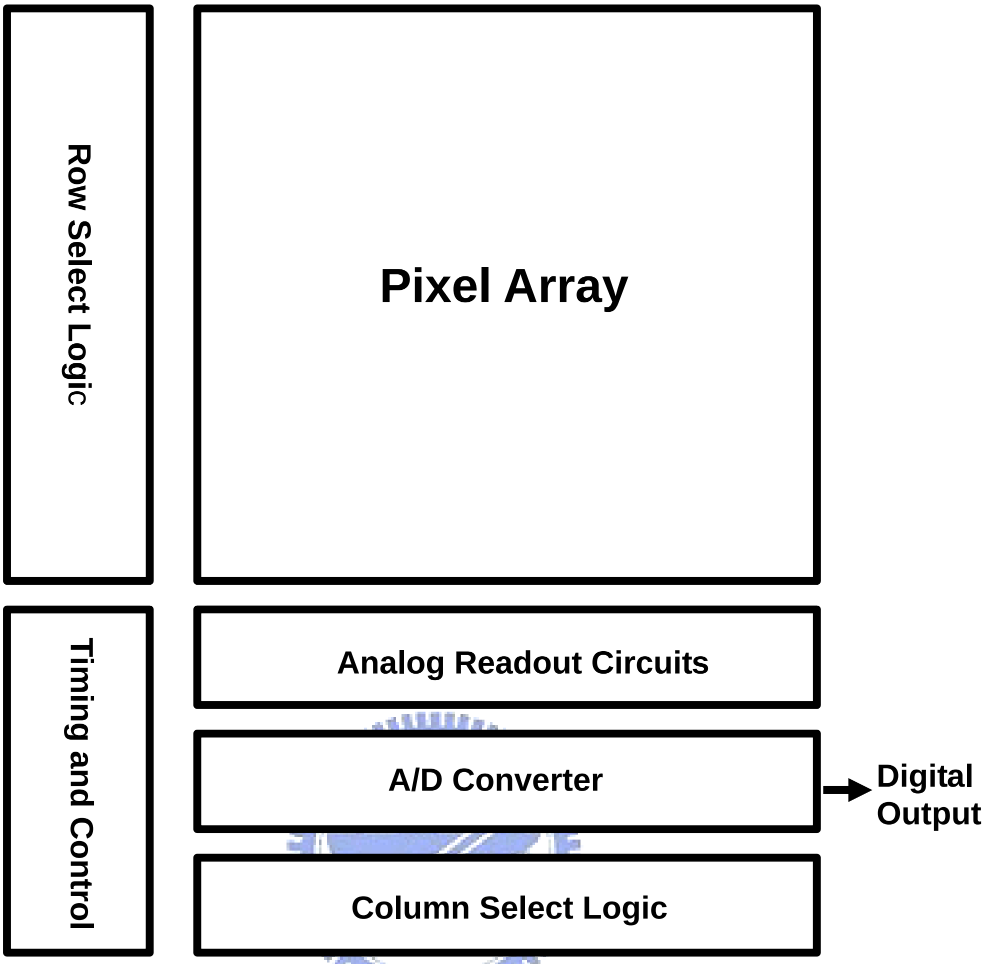


Fig. 2.1 The overall architecture of a CMOS image sensor.

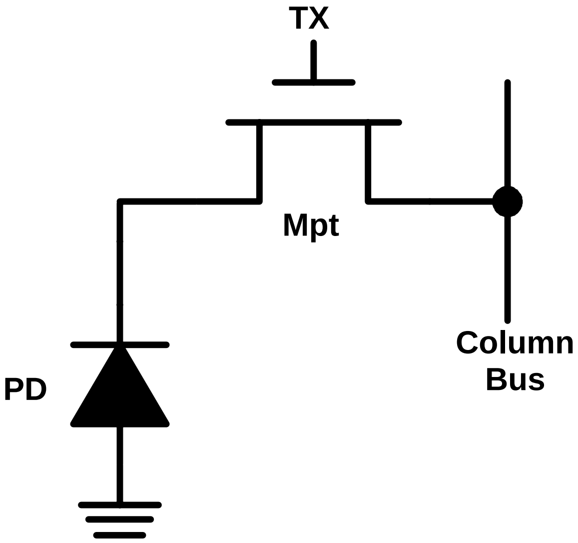


Fig. 2.2 Passive pixel circuit.

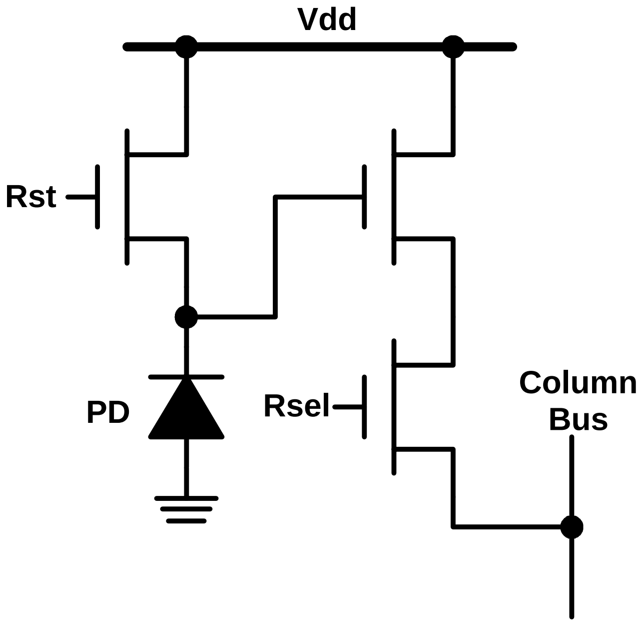


Fig. 2.3 Active pixel circuit.

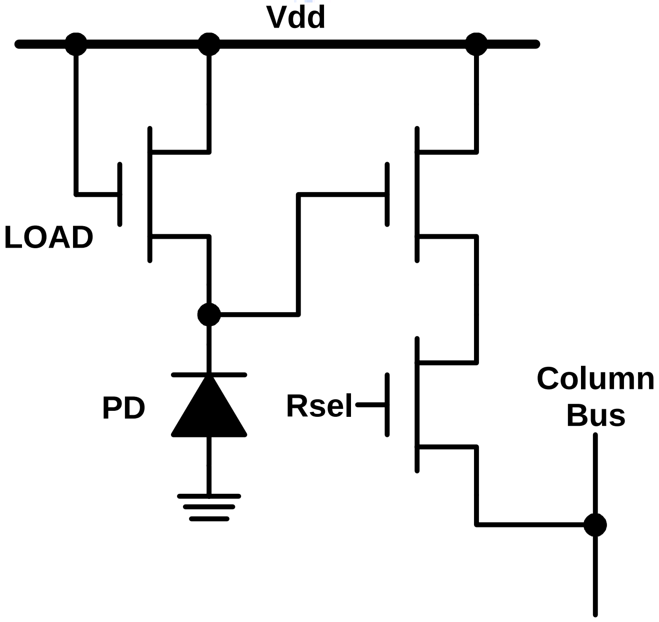


Fig. 2.4 Logarithmic pixel circuit.

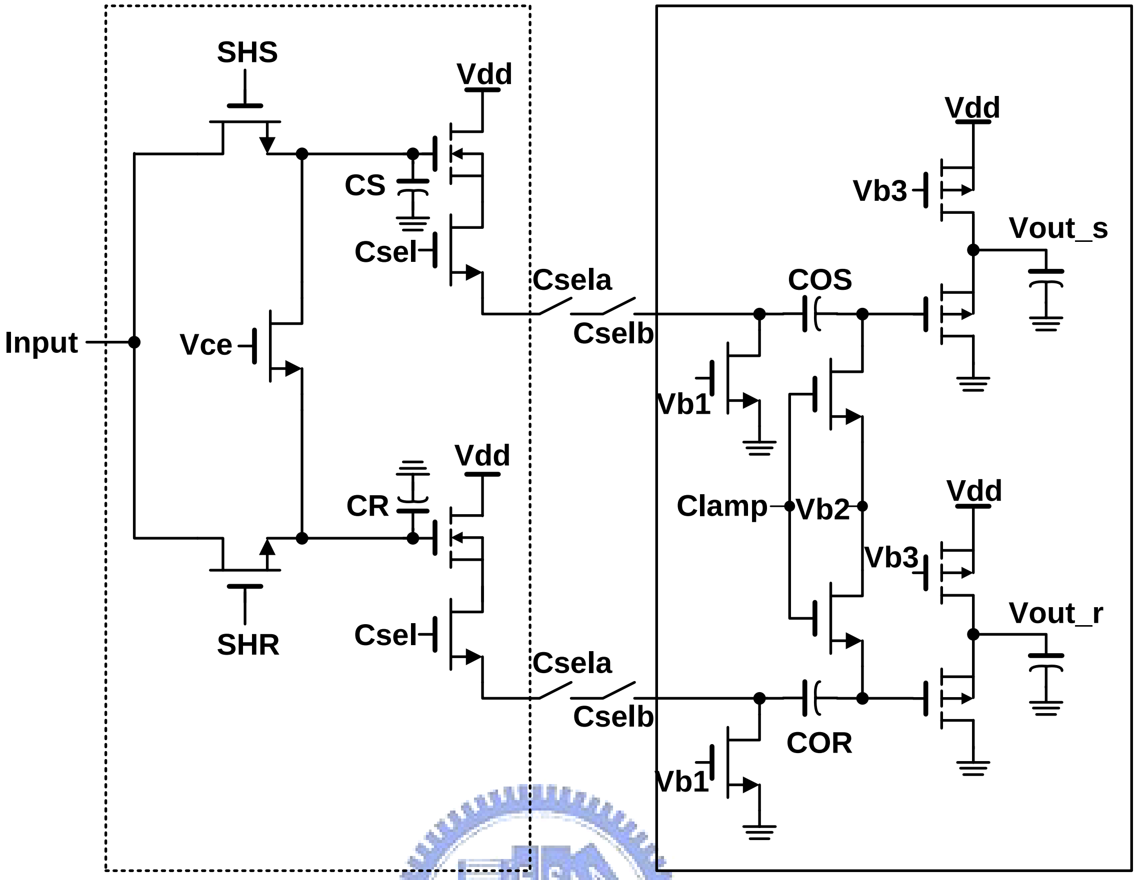


Fig. 2.5 Double delta sampling (DDS) circuit.

CHAPTER 3

DESIGN, OPTIMIZATION, AND PERFORMANCE ANALYSIS OF NEW PHOTODIODE STRUCTURES FOR CMOS ACTIVE-PIXEL-SENSOR (APS) IMAGER APPLICATIONS

3.1 INTRODUCTION

To achieve the performance requirements of CMOS imagers, one of the key elements is the photodiode array in which the photodiodes should be designed and optimized carefully. The two critical parameters in the design of photodiodes for imager applications are the dark current and the spectral response. Large dark current in the photodiode array of CMOS imagers can lead to non-uniformity, low scalability, and reduced dynamic range. The first source of dark current depends on doping concentrations, bandgap, and temperature of the reverse-biased photodiode [82]. The second source is the defect-generated dark current determined by the shape of photodiode layout, the cross-sectional structure of the photodiode, and the fill factor [82]. The shape of photodiode layout can be designed to reduce the dark current [82]. Generally, the second source of dark current is mainly generated from the pn junction depletion region under bird’s beak in LOCOS process [83] or in the interface isolation of STI (shallow trench isolation) as well as the surface damage caused by the implantation of high doping concentration.

The spectral response is another important parameter considered in the design of photodiodes. The high spectral response of photodiodes can be generated by using shallow and deep depth of the pn junctions to absorb photons for light of short and long wavelengths, respectively.

It is the aim of this chapter to propose two new photodiode structures with low dark current and high spectral response. The pn junction of p-substrate and the lightly-doped sensor implant SN– is used as a photodiode in both structures. The regions of bird’s beak in the two proposed structures are completely embraced by the SN– implant and the p-field implant, thus not located in the pn junction depletion region. Both pn junction depletion located under the bird’s beak and surface damage due to high doping concentration can be avoided and the generation of dark current can be suppressed. Furthermore, the use of shallow and deep pn junctions can increase the photo-sensitivity for light of short and long wavelengths, respectively. Thus the spectral response can be improved. Systematic comparisons on measurement results of dark currents and spectral responses among the proposed photodiode structures and other structures in CMOS technology with reasonable process modifications are presented. From the experimental results, it has been verified that the two proposed structures in the 5 μm x 5 μm APS cell of the CMOS imager have low dark currents of 30.6 mV/sec and 35.2 mV/sec at the reverse-biased voltage of 2 V as well as good spectral response.

The rest of this chapter is organized as follows. In Section 3.2, two new CMOS photodiode structures in 0.35 μm 1P3M 3.3 V CMOS technology with salicide process are described. Principles of reducing the dark current and improving the spectral response are also presented. Other photodiode structures for comparison purpose are also described. In Section 3.3, the layout consideration and optimization for the proposed photodiode structures and other structures for comparisons are described. In Section 3.4, experimental results of dark current and spectral responses of the fabricated photodiodes are presented, analyzed, and compared to verify the advantageous performance of the proposed new photodiode structures. Summary are finally made in Section 3.5.

3.2 ANALYSIS OF NEW CMOS PHOTODIODE STRUCTURES

Generally, it is difficult to accurately characterize and predict both dark current and spectral response of a pn-junction photodiode by using model equations. In this work, based on the analysis on the mechanisms for dark currents and spectral responses as well as the understanding of process technology, we proposed and designed two photodiode structures for low dark current and/or high spectral response. Several other structures were also designed. Through extensive experimental measurements on dark currents and spectral responses of all fabricated photodiode structure, the mechanism can be verified and the optimal structure can be confirmed.

The cross-sectional views of the two proposed photodiode structures called Type P1 and Type P2 with the explanations of all dimension notations are shown in Figs. 3.1(a) and 3.1(b), respectively. The modified 0.35 μm single-poly-triple-metal (1P3M) CMOS process with a lightly-doped p-substrate and LOCOS structure is adopted to realize the two new structures. All the layers and their functions in the design of CMOS imager are summarized in Table 3.1. The p-well is defined by a mask that differs from the complement of the n-well mask in this modified CMOS process. The p-field implant is defined by another mask and is completed before the use of the mask defined by the thin oxide. Following the growth of SiO2 and SiN on the region defined by the thin oxide, the thick field oxide (FOX) is grown in areas where SiN is absent. Field oxide is grown in both vertical and lateral directions. The growth in the lateral direction results in the bird’s beak. This technique of field oxide growth is so called LOCOS (local oxidation of silicon). The planarization technique used to etch the field oxide to its final thickness is then completed. The regions of the p-field implant below the field oxide are pushed downward during the growth of the field oxide. The cross-sectional views of the bird’s beak, FOX, and the p-field implant are shown in Figs. 3.1(a) and 3.1(b).

In the photodiode structures, all significant dimensions are mentioned in notations. These dimensions depend on different CMOS fabrication technologies, fabrication equipments, and different fabs. The real values for these dimensions should be carefully optimized for a certain technology or fabrication fab.

In the structure of the Type P1 photodiode, all regions of the thin oxide are implanted by the lightly-doped sensor implant SN– as shown in Fig. 3.1(a). Thus the pn junction of p-substrate and SN– is used as the photodiode. The length of d06 is longer than that of d02, so regions of the bird’s beak are completely embraced by SN–.

Since the bird’s-beak region has a high density of defects due to the high silicon/SiO2 stress, the dark current will be increased significantly if the depletion region of the pn junction photodiode is located in the bird’s-beak region. In the Type P1 structure, the regions of bird’s beak are not located in the depletion region of the pn junction photodiode formed by the p-field implant and SN– if the following equation is adopted.

$$d08 > d05 + d07 + \Delta d05 + \Delta d07 \qquad (3.1)$$

where Δd05 and Δd07 represent the mask misalignments of the p-field implant and SN–, respectively. Thus the dark current that results from the bird’s beak can be completely avoided in the Type P1 structure. Under these conditions, the depletion region of a photodiode is not located in the bird’s-beak region. Too large d08 will decrease the fill factor. If d08 is equal to or smaller than the sum of d05 and d07, then the depletion region of the p-field/SN– junction will be in the bird's-beak region to increase the dark current.

The dark current of the photodiode is also increased due to the surface damage generated by the sensor implant. The higher doping concentration of the sensor implant will result in greater surface damage causing larger dark current. The surface damage in the Type P1 structure is low due to the low doping concentration of SN–. This further decreases the dark current in P1.

In the Type P1 structure, p-well is replaced by p-substrate in the formation of the pn junction. Thus the depletion region of the photodiode becomes wider to absorb more photons due to the lower doping concentration of p-substrate than that of p-well. In the Type P1 structure, the depletion region of the p-substrate/SN– junction photodiode at the bottom plate is deep enough to absorb long wavelength photons. Thus the photo-sensitivity for the light of long wavelength can be improved. The depletion region of p-substrate and the side diffusion of SN– below FOX is effective in the absorption of short wavelength photons because this part of pn junction is shallow enough to absorb photons for the light of short wavelength. Absorption of photons is not affected by FOX because FOX is transparent.

In the Type P2 structure, the pn junction of p-substrate and SN– is used as a photodiode where SN– has the same doping concentration as in the Type P1 structure. In the Type P2, only the central part of thin-oxide region is implanted by SN– as shown in Fig. 3.1(b). The mask of SN– is defined inside the regions of thin oxide. The length of d09 is slightly larger than that of d04 because the regions of p-field implant below the thin oxide are not pushed out by the field oxide during its growth. The length of d09 is larger than that of d02. In the Type P2, the regions of bird's beak are completely embraced by the p-field implant.

The regions of bird's beak in the Type P2 structure are not located in the depletion region of pn junction photodiode formed by the p-field implant and SN– if the following two equations are adopted.

$$\mathrm{d03} < \mathrm{d10} + \mathrm{d12} + \Delta\mathrm{d10} \tag{3.2}$$

$$\mathrm{d13} > \mathrm{d10} + \mathrm{d11} + \Delta\mathrm{d10} + \Delta\mathrm{d11} \tag{3.3}$$

where Δd10 and Δd11 represent the mask misalignments of the p-field implant and SN–, respectively. If the sum of d10 and d12 is designed to be much larger than the length of d03, then the length of d13 can be designed to be shorter than the sum of d10 and d11. In this case, the p-field implant and SN– will be in contact together but the regions of bird’s beak will not be located in the depletion region of p-field/SN– junction because the doping concentration of p-field implant is higher than that of SN–. However, the fill factor is small in this case. If the sum of d10 and d12 is designed to be shorter than the length of d03, then the length of d13 must be designed to be much longer than the sum of d10 and d11 to prevent the regions of bird’s beak from being located in the depletion region of p-substrate/SN– junction. The fill factor is also small in this case.

The sum of d10 and d12 is designed to be slightly longer than the length of d03 and the length of d13 is designed to be slightly longer than the sum of d10 and d11 to protect the regions of bird’s beak from being located in the depletion region of pn junction and keep the fill factor as large as possible. The regions of bird’s beak in this optimal design are completely embraced by the p-field implant and are not located in the depletion region of p-field/SN– junction. Thus dark current from the bird’s beak can be completely avoided in P2. The surface damage is also kept low in P2 due to the low doping concentration of both p-field implant and SN–.

In the performance of photo-sensitivity, the depletion region of the p-substrate/SN– junction at the bottom plate is deep enough and is therefore used to absorb photons for the light of long wavelength. Moreover, the depletion region of the pn junction formed by the p-substrate and the side diffusion of SN– is used to absorb photons for the light of short wavelength.

Four structures, C1, C2, C3, and C4 with the explanations of all dimension notations shown in Figs. 3.2(a), 3.2(b), 3.2(c), and 3.2(d), respectively, are analyzed to compare their performance with that of the two proposed new photodiode structures. In Fig. 3.2(a), the p-substrate and N+ implant are used as the pn junction photodiode. This structure is the same as Type P1 except that SN– is replaced by N+. Type C1 is the conventional photodiode structure used in the standard CMOS process. However, the bird's beak cannot be embraced completely by N+ because the length of d14 is shorter than that of d02. Thus, some bird's-beak regions are located in the depletion region of the p-substrate/N+ junction. In the performance of photo-sensitivity, the shallow p-substrate/N+ junction at the bottom plate can be used to absorb photons for light of short wavelength.

In Fig. 3.2(b), the p-substrate and the SN+ implant are used as the pn junction photodiode. SN+ is an extra sensor implant used in the modified CMOS process. The photodiode structure of Type C2 is the same as that of Type P1 except SN– is replaced by SN+. The length of d16 is shorter than that of d02, so SN+ still cannot be used to embrace completely the regions of bird's beak. Thus some bird's-beak regions are located in the depletion region of the p-substrate/SN+ junction. In the performance of photo-sensitivity, the shallow p-substrate/SN+ junction at the bottom plate can be used to absorb photons for light of short wavelength.

In Fig. 3.2(c), the p-substrate and SN+ are used as the pn junction photodiode. The photodiode structure of Type C3 is the same as that of Type P2 except that SN– is replaced by SN+. The bird's beak will be located in the depletion region of the p-field/SN+ junction if the length of d19 is equal to that of d13 in Fig. 3.1(b) because the doping concentration of SN+ is larger than that of the p-field implant. The depletion region of the pn junction photodiode formed by the p-substrate and the side diffusion of SN+ can be used to absorb photons for light of short wavelength. Moreover, the shallow p-substrate/SN+ junction at the bottom plate can also be used to absorb photons for light of short wavelength.

In Fig. 3.2(d), the p-substrate and SN– are used as the pn junction photodiode. The photodiode structure of Type C4 is the same as that of Type P2 except that both P+ and p-field implant are used to embrace the bird’s beak. The distance between the two edges of the P+ mask and the p-field mask is equal to zero. The regions of bird’s beak are completely embraced by both of P+ and p-field implant if the lengths of d24 and d25 are equal to that of d12 and d13, respectively. The photo-sensitivity of Type C4 is the same as that of Type P2.

3.3 LAYOUT OPTIMIZATION OF NEW PHOTODIODE STRUCTURES IN APS CELLS

The circuit diagram of APS cell is shown in Fig. 3.3(a) where the NMOSFET of MR is used to reset the voltage of the photodiode. The two NMOSFETs of M1 and M2 are used as source follower and row selector, respectively. The layouts of the two proposed new photodiode structures applied to the 5 μm x 5 μm active-pixel-sensor (APS) cell are shown in Figs. 3.4(a) and 3.4(b), respectively. To show the layout of APS cell clearly, only masks of the thin oxide, poly, metal1, p-field block (pfb), N+ block (NB), SN–, P+ and contact are drawn in Figs. 3.4(a) and 3.4(b). Routing and interconnections of the APS cell are not shown in the layout diagrams. The placement of the three NMOSFETs is also shown in Figs. 3.4(a) and 3.4(b). The region of the p-field implant is defined outside the mask of pfb. The region of N+ is defined outside the mask of NB.

Even a single contact will drastically decrease the fill factor due to the small area of 5 μm x 5 μm APS cell. In the layout of Fig. 3.4(a), the source region of MR is directly connected to the photodiode to save one contact and increase the fill factor. The p-substrate contact has been moved outside the 5 μm x 5 μm APS cell. The contact at the gate of MR cannot be removed, otherwise the reset operation will be delayed and the dark current in the photodiode will be increased. Only six contacts are used in the layout of the 5 μm x 5 μm APS cell and the maximum fill factor can be large.

In Fig. 3.4(a), the photodiode structure of Type P1 is used in the 5 μm x 5 μm APS cell. SN– is used to embrace the bird's beak completely except for the two edges of A and B because the source region of MR should be implanted by N+. Although N+ is used to embrace the regions of bird's beak at the two edges, some bird's-beak regions are still located in the depletion region of the p-substrate/N+ junction because the depth of N+ is shallower than that of FOX below the thin oxide. This will increase the dark current. The distance between pfb and the edge of the thin oxide is designed according the design principle mentioned in the previous section. The fill factor in this structure is large because all regions of the thin oxide in the Type P1 are implanted by SN–. The fill factor is designed to be 32% in the layout of Fig. 3.4(a).

The regions of the photodiode should be covered by the SAB (silicide block) mask to remove the silicide from the top of photodiode due to its optically opaque and undesirably large leakage [22], [84], [85]. However, the large leakage current is induced in the interface of the silicided source region of MR and the non-silicided region of the photodiode. This situation is prevented by covering the total source regions of the NMOSFET MR by SAB as shown in Fig. 3.4(c) to reduce the effect of the silicided interface. Regions other than the photodiode should be shielded by metal from light irradiating. Regions covered by metal3 are also shown in Fig. 3.4(c). The shielding by metal3 and the block of silicide in the detailed layout of the APS cell are shown in Figs. 3.4(a) and 3.4(b).

In Fig. 3.4(b), the photodiode structure of Type P2 is used in the 5 μm x 5 μm APS cell. The regions of bird’s beak are all embraced by the p-field implant except for the four edges A, B, C, and D. The bird’s beaks at the two edges of both A and B are embraced by N+ with the p-field implant extended under N+ because the source region of MR must be implanted by N+. Thus, some bird’s-beak regions at the two edges of A and B will be located in the depletion region of the p-field/N+ junction. The regions of bird’s beak will be located in the depletion region of the p-field/SN– junction at the two edges of C and D because the contact in the photodiode should be embraced by SN– and both regions of the p-field implant and SN– are extended outside the thin-oxide edge. Although the contact in the photodiode can be put in the right side of the current position, this will reduce the fill factor due to the shielding effect of metal. The distance between the two edges of the pfb mask and the thin-oxide mask as well as the distance between the two edges of the pfb mask and the SN– mask are designed according to the optimal value as determined in Fig. 3.1(b). The fill factor is designed to be 15% in the layout of Fig. 3.4(b).

The layouts of photodiode structures in both Type C1 and Type C4 for comparisons in 5 μm x 5 μm APS cell are shown in Figs. 3.4(c) and 3.4(d), respectively. In Fig. 3.4(c), the conventional photodiode structure of Type C1 uses N+ to embrace the bird’s beak. The mask of the p-field implant is the same as that of the layout in Fig. 3.4(a). Some regions of the bird’s beak will be located in the depletion region of the p-substrate/N+ junction as referred to Fig. 3.2(a). The fill factor in this layout is the same as that of Type P1. The layouts of Type C2 and Type C3 are the same as those of Type P1 and Type P2, respectively except that SN– is replaced by SN+. In Fig. 3.4(d), the layout of Type C4 is the same as that of Type P2 except that

P+ implant is added to embrace the bird’s beak. P+ cannot be used to embrace all bird’s-beak regions in Fig. 3.4(d) because pn junction breakdown will be caused if the distance between P+ and N+ is too short. The bird’s beak at the four edges of A, B, C, and D are still located in the depletion region of the pn junction as referred to Fig. 3.4(b). The fill factor in this layout is the same as that of Type P2.

3.4 EXPERIMENTAL RESULTS

In the conventional measurement method of dark currents [82], the dark current in each pixel is integrated at the node of APS cell for a certain period of time and determined from the integrated voltage. The variations of dark currents among pixels of the entire imager array can be observed in this method. In this work, the experimental dark-current characteristics of different photodiode structures versus reverse-biased voltages are required for comparisons. The main focus is not on the variation of dark current in each pixel. Thus the measurement method with large number of photodiodes in parallel is used.

The interconnection in the APS cell is changed to that shown in Fig. 3.3(b) to measure directly the dark current of the photodiode. Rsel and Vout are connected to ground and Vdd, respectively. Thus, no current flows in the NMOSFETs of M1 and M2. If Reset is set to ground to turn off MR, then the relationship of current to voltage (I-V) at Dout under the reverse bias of the dark photodiode represents the characteristics of the dark current of the photodiode. However, the current in a single APS cell is too small to be measured. Thus an APS cell array with all the Reset (Dout) nodes connected together is used to increase the current. There are 25600 APS cells for each new photodiode structure. The I-V characteristics of each new photodiode structure can be obtained by dividing the measured total current by 25600. The dark current measurements were taken at room temperature (300 K), which is kept constant.

The dark current of an APS cell can be represented in the form of $\frac{dV(t)}{dt}$ at Dout of Fig. 3.3(b). The effective dark current of $\frac{dV(t)}{dt}\Big|_{V=Vo}\left(=\frac{I(Vo)}{C(Vo)}\right)$ can be obtained by measuring *I(Vo)* and *C(Vo)* at the fixed bias Vo where *I(Vo)* and *C(Vo)* represent the current and capacitance at Dout under the reverse-biased voltage of *Vo* and no light irradiating. Note that *I(Vo)* and *C(Vo)* of an APS cell can be obtained from the corresponding measured data of the parallel APS cell array by dividing those data by 25600. All the measured data are obtained from the statistical average of different measured chips.

The method for measuring the spectral response of photodiodes is the same as the proposed method except that the regions of the photodiode should be irradiated by monotonic light with the wavelength between 400 nm and 700 nm.

3.4.1 Dark Current

The chip photograph of the fabricated parallel-connected APS cells with one new photodiode structure and the overall test chip are shown in Fig. 3.5(a) and 3.5(b), respectively. The capacitance of the dummy PAD must be measured and subtracted from the measurement results of *C(V)* to derive the capacitance at Dout in Fig. 3.3(b).

The measured *I(V)* and *C(V)* at Dout for the Type P1 photodiode structure are shown in Figs. 3.6(a) and 3.6(b), respectively, when the Reset is set to 0 volts as shown in Fig. 3.3(b). The effective dark current, $\frac{dV}{dt}$, of an APS cell with the photodiode structure of Type P1 can be derived from the results in Figs. 3.6(a) and 3.6(b). The dark current of an APS cell for other photodiode structures can also be derived from the *I(V)* and *C(V)*.

The measured dark current in 5 μm x 5 μm APS cells with the two proposed new photodiode structures and four other structures for comparisons are shown in Figs. 3.7(a) and 3.7(b). The reverse-biased voltage of the photodiode under the measurement is equal to 2 V, i.e. *Vo*=2 V. The dark current of one photodiode per unit area is shown in Fig. 3.7(a), whereas the effective dark current of one APS cell is shown in Fig. 3.7(b). The dark currents of Type P1 and Type P2 photodiode structures are 12.25 nA/cm^2 and 14.55 nA/cm^2, respectively. The dark currents of one APS cell with Type P1 and Type P2 photodiode structures are 30.6 mV/sec and 35.2 mV/sec, respectively. The proposed photodiode structure of Type P1 has the smallest dark current because all of the bird's-beak regions are embraced by SN– and the surface damage is low by using the low doping concentration of SN–. Furthermore, the first source of dark current in the photodiode structure of Type P1 is the lowest by using SN– and p-substrate as photodiode. The surface damage in the regions of the p-field implant below the thin oxide is slightly greater than that in SN– because the p-field implant has a higher doping concentration than that of SN–. Thus the dark current in the Type P2 structure is slightly larger than that in the Type P1 for photodiodes with the same area because the surface damage in the Type P2 is slightly greater than that of Type P1. Furthermore, the regions of bird's beak at the two edges of C and D in the layout of Type P2 are located in the depletion region of the p-field/SN– junction as shown in Fig. 3.4(b). This slightly increases the dark current in the Type P2. The measurement results of dark-current variations of the fabricated Type P1 and Type P2 photodiodes at the reverse-biased voltage of 2 V for seven different chips have been measured and shown in Fig. 3.8. The variations among different chips are small as shown in Fig. 3.8. Thus the effect of mask misalignment in the two proposed photodiode structures is not significant. Moreover, the dark current of Type P1 is smaller than Type P2, even with variations. Thus the statistically averaged dark current obtained from the measured data on different chips can represent the true result as shown in Fig. 3.7.

The surface damage in the Type C4 is greater than that in the Type P2 because of the addition of P+ to embrace the bird's beak. Thus the dark current in the Type C4 is larger than that in the Type P2. Some bird's-beak regions in the Type C1 photodiode structure are located in the depletion region of the p-substrate/N+ junction because N+ cannot be used to embrace the entire regions of bird's beak as referred to Fig. 3.2(a). Furthermore, the surface damage in the Type C1 is serious because of the high doping concentration of N+. Thus the dark current in the Type C1structure is larger than that in the Type C4.

The surface damage in the Type C2 is less than that in the Type C1 because SN+ has a lower doping concentration than N+. However, the dark current in the Type C2 is larger than that in the Type C1 because more bird's-beak regions are located in the depletion region of the pn junction in the Type C2 structure than in the Type C1 structure. Type C3 has the largest dark current because most regions of the bird's beak are located in the depletion region of the p-field/SN+ junction since SN+ has higher doping concentration than the p-field implant. The effect of surface damage in the Type C3 is also serious due to the use of the high doping concentration of SN+. The measurement results of the dark current, the fill factor, and pixel capacity in the two proposed new photodiode structures and the four structures for comparisons are given in Table 3.2.

3.4.2 Spectral Response

The spectral responses of Type P1, Type P2, Type C1, Type C2, and Type C3 are shown in Fig. 3.9. The spectral response in the Type C4 structure is the same as that in the Type P2. In the photo-sensitivity for light of long wavelength as shown in Fig. 3.9, the Type P1 has the best performance because all regions of the photodiode are composed of the deep p-substrate/SN– junction. The performance of Type P2 is worse than that of Type P1 because regions of deep pn junction in the Type P2 are smaller than those in the Type P1. Although the p-substrate/SN+ junction in the Type C2 can be used to absorb photons for light of long wavelength, its efficiency is not as good as that of SN– because the junction depth of SN+ is shallower than that of SN–. Thus the performance in the Type C2 is worse than that in the Type P2. The performance in the Type C1 is worse than that in the Type C2 because the junction depth of N+ is shallower than that of SN+. The performance in the Type C3 is slightly worse than that in the Type C1 because more N+ regions in the Type C1 can be used to absorb photons for light of long wavelength than the regions of SN+ in the Type C3 even although the junction depth of N+ is shallower than that of SN+.

In the photo-sensitivity for light of short wavelength, the performance of Type P2 is better than that of Type P1 because the regions of the shallow pn junction composed of p-substrate and the side diffusion of SN– in the Type P2 are larger than that of Type P1. Type P1 has better performance than Type C1 because longer side diffusion length in SN– than that in N+ can be used to absorb photons for light of short wavelength although the junction depth of N+ is shallower than that of SN–. The performance in the Type C1 and Type C3 is almost the same because the junction depth of N+ is shallower than that of SN+ but the side diffusion length of N+ in the Type C1 is shorter than that of SN+ in the Type C3. The Type C2 structure has the worst performance because the junction depth of SN+ is deeper than that of N+ and the side diffusion length of SN+ in the Type C2 is not long enough.

The measurement of dark current was performed by using the instruments of probe station, HP E3610A dc power supply, HP 4156B precision semiconductor parameter analyzer, and HP 4284A precision LCR meters. The measurement of spectral response was performed by using the instrument of monotonic light generator with its wavelength from 400 nm to 700 nm.

From the above measurement results, the two proposed new photodiode structures applied in the 5 μm x 5 μm APS cell show lower dark current and higher overall spectral response than the conventional structure and the other structures for comparisons. With the rapid scaling down of the CMOS process and the future requirements for a high quality imager, the 5 μm x 5 μm APS cell of the CMOS imager using the two proposed structures of Type P1 and Type P2 can be applied in the high resolution and high quality imager systems.

Because the CMOS technology used in the experimental results of this paper is 0.35 μm single-poly-triple-metal (1P3M) 3.3 V CMOS process with LOCOS structure, the LOCOS structure is discussed more in this work. Although the dark currents of photodiode structures with STI (shallow trench isolation) are smaller than those with LOCOS, the proposed photodiode structure can also be used to further improve the performance of dark current and spectral response.

3.5 SUMMARY

In this chapter, two new photodiode structures with low dark current and high spectral response are proposed and analyzed. The p-substrate and the SN– implant are used as the pn junction photodiode in both new structures. Regions of the bird’s beak in the two proposed structures are embraced by either the SN– implant or the p-field implant and are kept away from the depletion region of the pn junction. The surface damage can be lowered by using the low doping concentration of the SN– implant.

Thus, in the two new photodiode structures, the dark current generated in the regions of bird’s beak can be lowered and the increase of the dark current due to the effect of surface damage can be avoided. The spectral responses of the two structures can be improved by utilizing the shallow side diffusion and deep bottom diffusion of SN– to absorb the photons for light of short and long wavelengths, respectively.

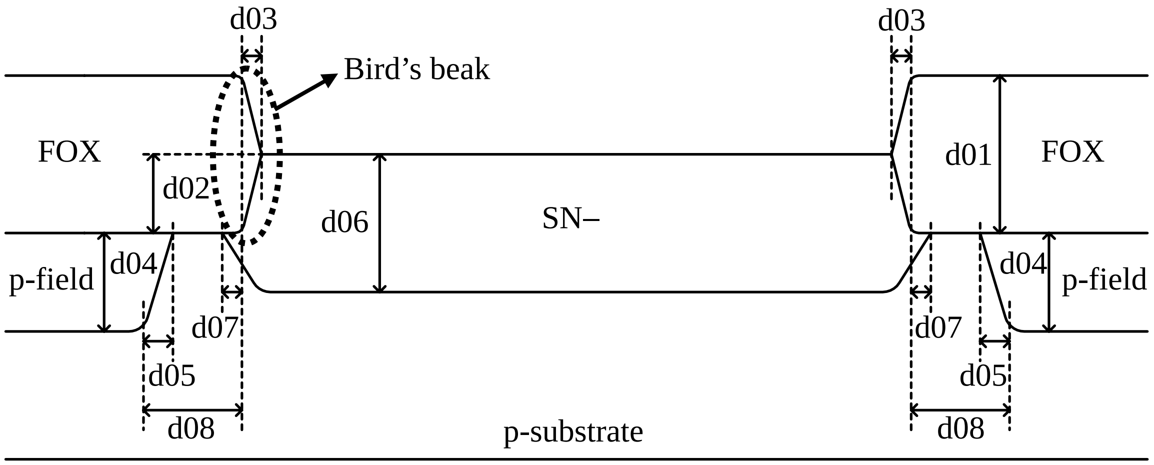
The layout of the 5 μm x 5 μm APS cell designed using the two proposed new photodiode structures are implemented in the 0.35 μm 1P3M 3.3 V CMOS technology. It has been verified by experimental results that the two proposed photodiode structures have lower dark current and higher overall spectral response as compared to other photodiode structures. Because the CMOS technology used in the experimental results of this chapter is 0.35 μm single-poly-triple-metal (1P3M) 3.3 V CMOS process with LOCOS structure, the LOCOS structure is discussed more in this work. However, the proposed photodiode structures can also be applied to improve the performance of dark current and spectral response in CMOS technologies with STI. Thus the two new photodiode structures can be applied to the design of high-performance CMOS imagers with small pixel size, high resolution, low dark current, and high spectral response. Future research will be conducted to design such high-performance CMOS imagers.

Table 3.1 All layers and their functions in the design of CMOS APS imager

Layer	Function
SN+	Sensor implant with high doping density
SN–	Sensor implant with low doping density
N+	Definition of N+ source/drain implantation
NB	Regions of N+ is defined outside the mask of NB
P+	Definition of P+ source/drain implantation
p-field	Regions of p-field implant
pfb	Regions of p-field is defined outside the mask of pfb
thin oxide	Definition of thin oxide for devices
FOX	Regions of field oxide
p-substrate	Regions of p-substrate
SAB	Definition of salicide protection
metal1(2)(3)	Definition of metal1(2)(3) for interconnections
via1	Definition of via1 hole between metal1 and metal2
via2	Definition of via2 hole between metal2 and metal3
contact	Definition of contact window for metal1 to thin oxide and to poly
N-well	Definition of N-well
poly	Definition of poly-silicon

Table 3.2 Fill factor, dark current, and pixel capacity in 5 μm x 5 μm APS cells at reverse-biased voltage of 2 V

Type	Fill Factor	Dark Current Per Area (nA/cm^2)	Dark Current (dV/dt) (mV/sec)	Dark Current (dQ/dt) (electrons/sec)	Pixel Capacity (electrons)
P1	32%	12.25	30.6	0.98×10^{-15}	51.25×10^{-15}
P2	15%	14.55	35.2	0.55×10^{-15}	25.01×10^{-15}
C1	32%	32.56	72.4	2.59×10^{-15}	57.46×10^{-15}
C2	32%	39.12	89.8	3.13×10^{-15}	55.78×10^{-15}
C3	15%	42.63	95.8	1.59×10^{-15}	26.72×10^{-15}
C4	15%	26.94	63.5	1.01×10^{-15}	25.46×10^{-15}



d01 : the thickness of the final field oxide.

d02 : the depth of the field oxide below the thin oxide.

d03 : the width of the bird's beak.

d04 : the depth of the p-field implant below the field oxide.

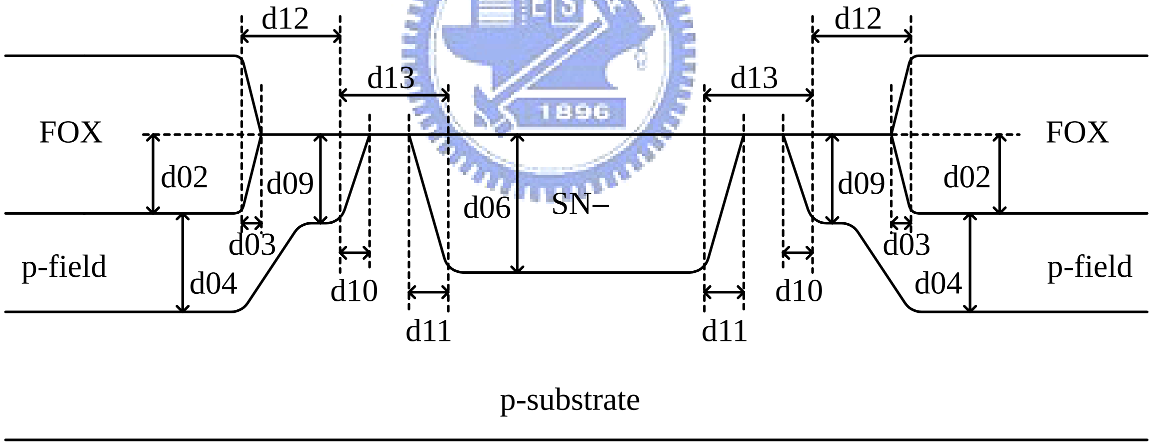
d05 : the side diffusion of the p-field implant below the field oxide.

d06 : the depth of the SN– below the thin oxide.

d07 : the side diffusion of the SN– below the field oxide.

d08 : the distance between the two edges of the p-field implant mask and the thin oxide mask below the field oxide.

(a)



d09 : the depth of the p-field implant below the thin oxide.

d10 : the side diffusion of the p-field implant below the thin oxide.

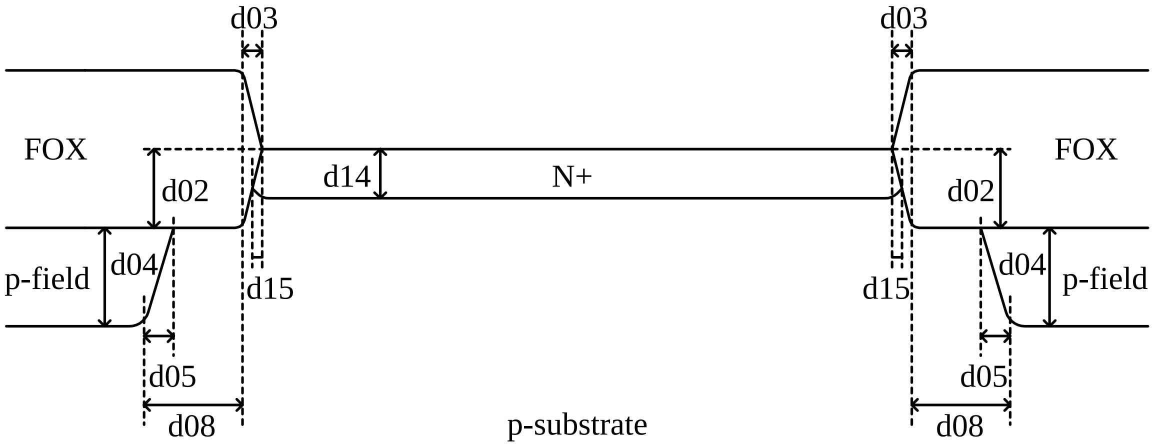
d11 : the side diffusion of the SN– below the thin oxide.

d12 : the distance between the two edges of the p-field implant mask and the thin oxide mask below the thin oxide.

d13 : the distance between the two edges of the p-field implant mask and the SN– mask below the thin oxide.

(b)

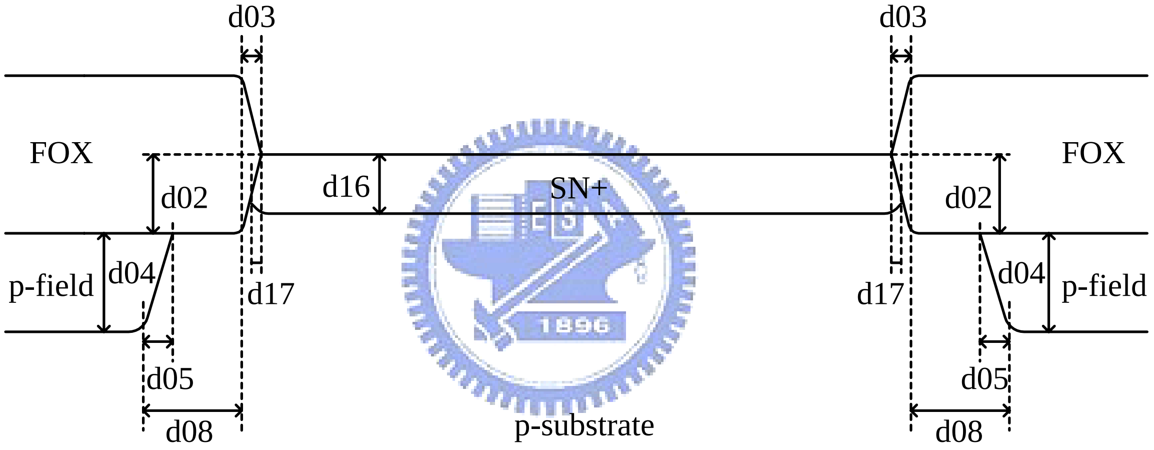
Fig. 3.1 Two proposed new photodiode structures: (a) Type P1: photodiode is composed of p-substrate and SN– with its bird's beak embraced by SN–. (b) Type P2: photodiode is composed of p-substrate and SN– with its bird's beak embraced by p-field.



d14 : the depth of the N+ below the thin oxide.

d15 : the side diffusion of the N+ below the bird’s beak.

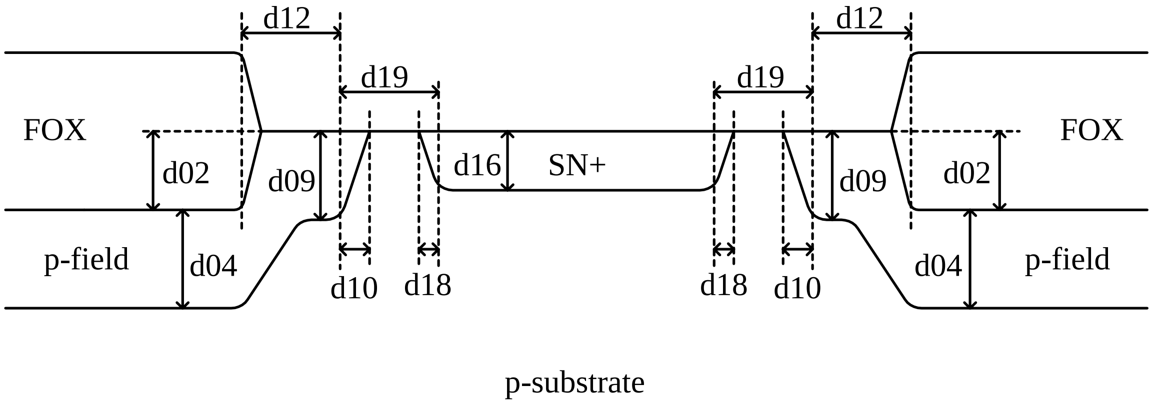
(a)



d16 : the depth of SN+ below the thin oxide.

d17 : the side diffusion of SN+ below the bird’s beak.

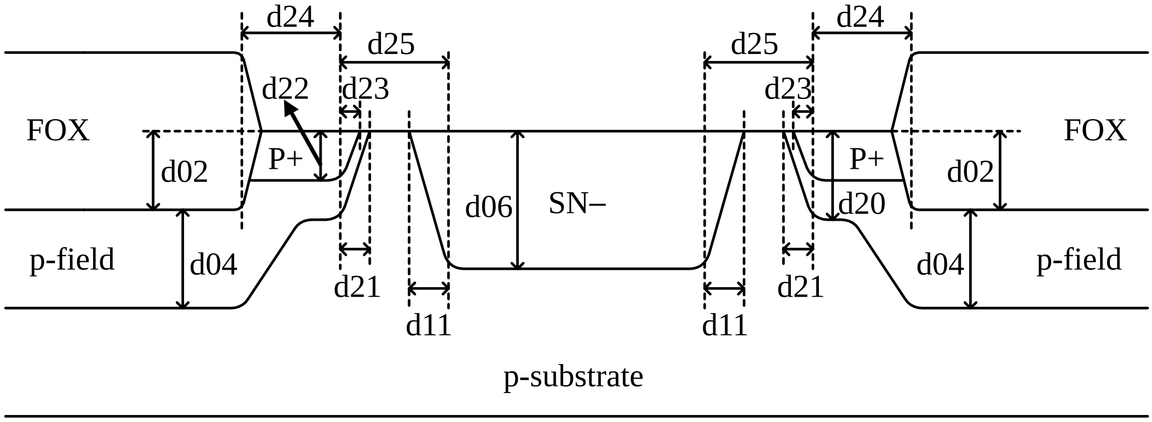
(b)



d18 : the side diffusion of SN+ below the thin oxide.

d19 : the distance between the two edges of the p-field implant mask and the SN+ mask below the thin oxide.

(c)



d20 : the depth of the p-field implant below the thin oxide.

d21 : the side diffusion of the p-field implant below the thin oxide.

d22 : the depth of the P+ below the thin oxide.

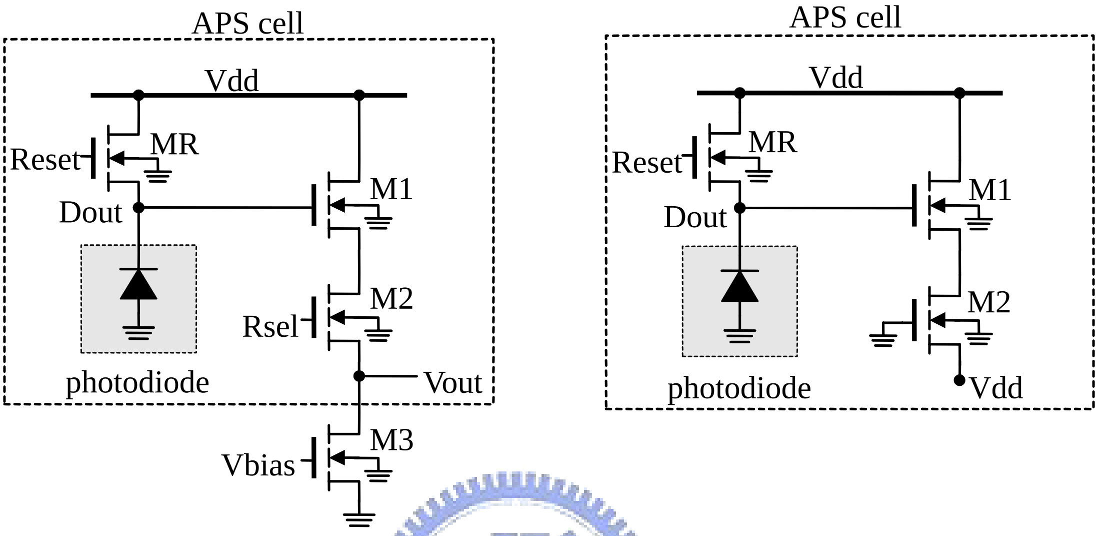
d23 : the side diffusion of the P+ below the thin oxide

d24 : the distance between the two edges of the P+ mask and the thin-oxide mask below the thin oxide.

d25 : the distance between the two edges of the SN− mask and the P+ mask below the thin oxide.

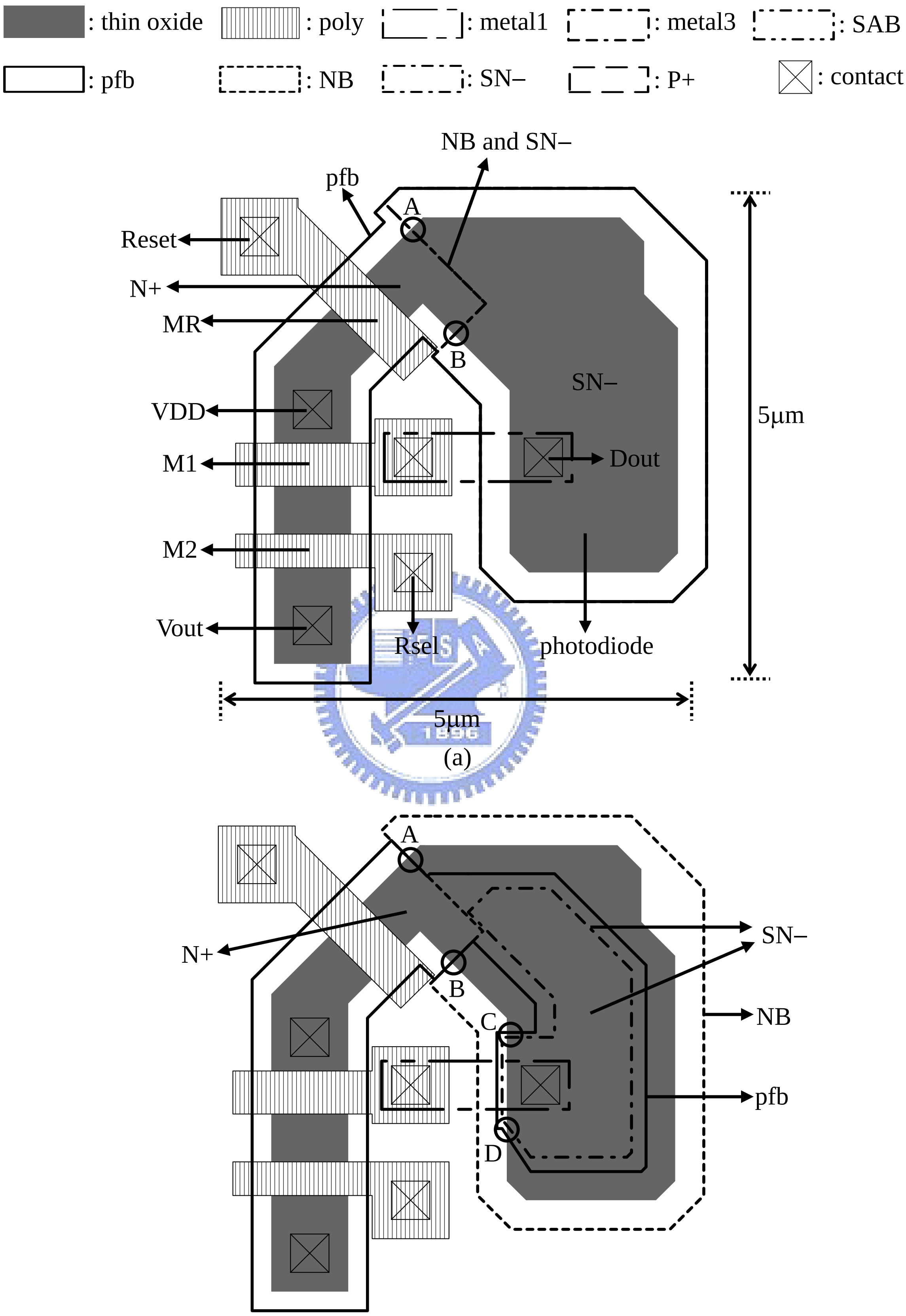
(d)

Fig. 3.2 Four photodiode structures for comparisons: (a) Type C1: SN− is replaced by N+ in the structure of P1 (conventional structure in CMOS imager). (b) Type C2: SN− is replaced by SN+ in the structure of P1. (c) Type C3: SN− is replaced by SN+ in the structure of P2. (d) Type C4: P+ is added to embrace the bird’s beak in the structure of P2.



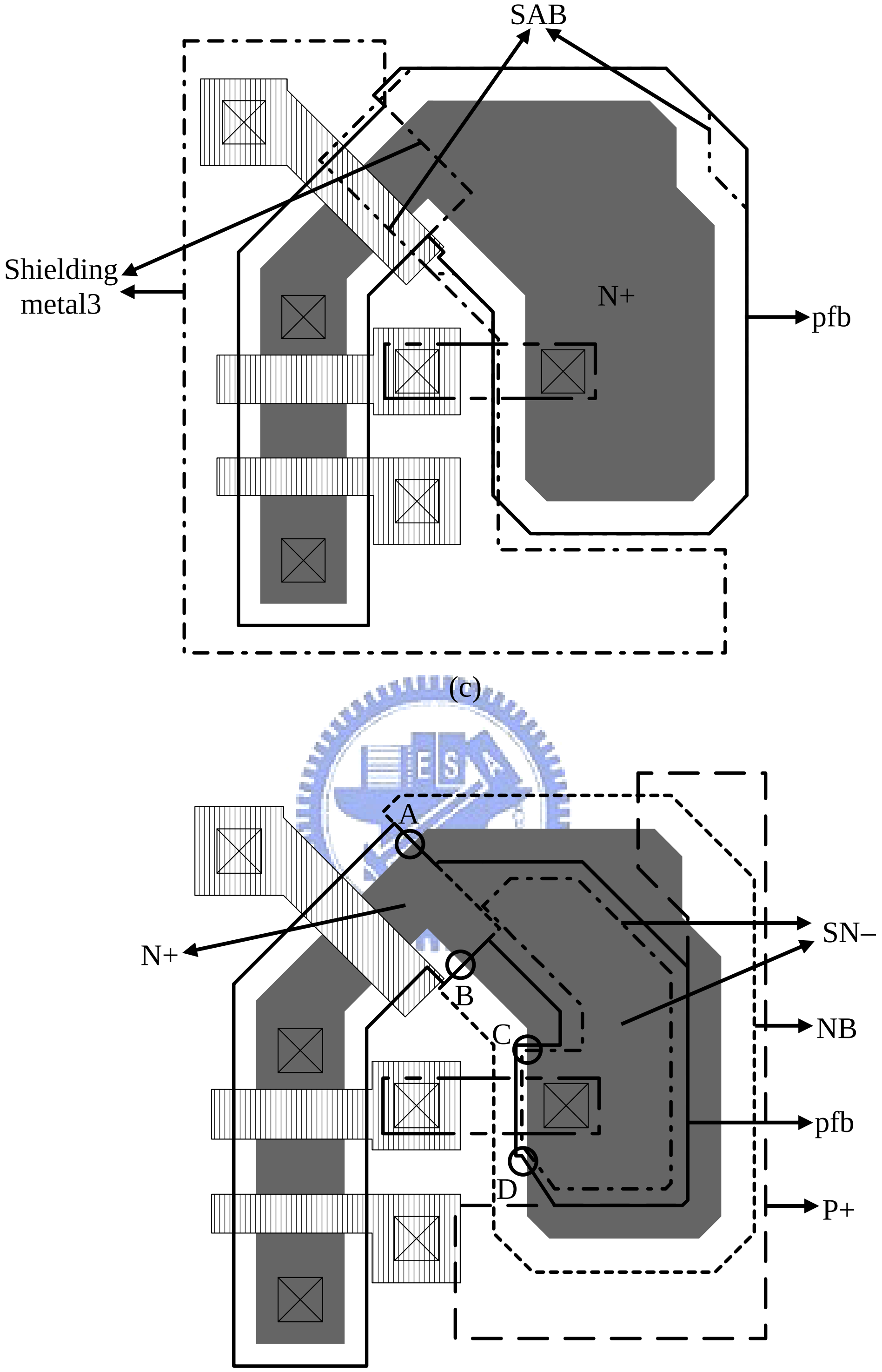
(a) (b)

Fig. 3.3 (a) Circuit diagram of APS cell. (b) Circuit diagram of APS cell with its Rsel and Vout connected to gnd and Vdd, respectively.


: thin oxide
: poly
: metal1
: metal3
: SAB
: pfb
: NB
: SN–
: P+
: contact
NB and SN–
pfb
A
Reset
N+
MR
B
SN–
VDD
M1
Dout
M2
Vout
Rsel
photodiode
5μm
5μm
A
N+
B
SN–
C
NB
pfb
D

(a)

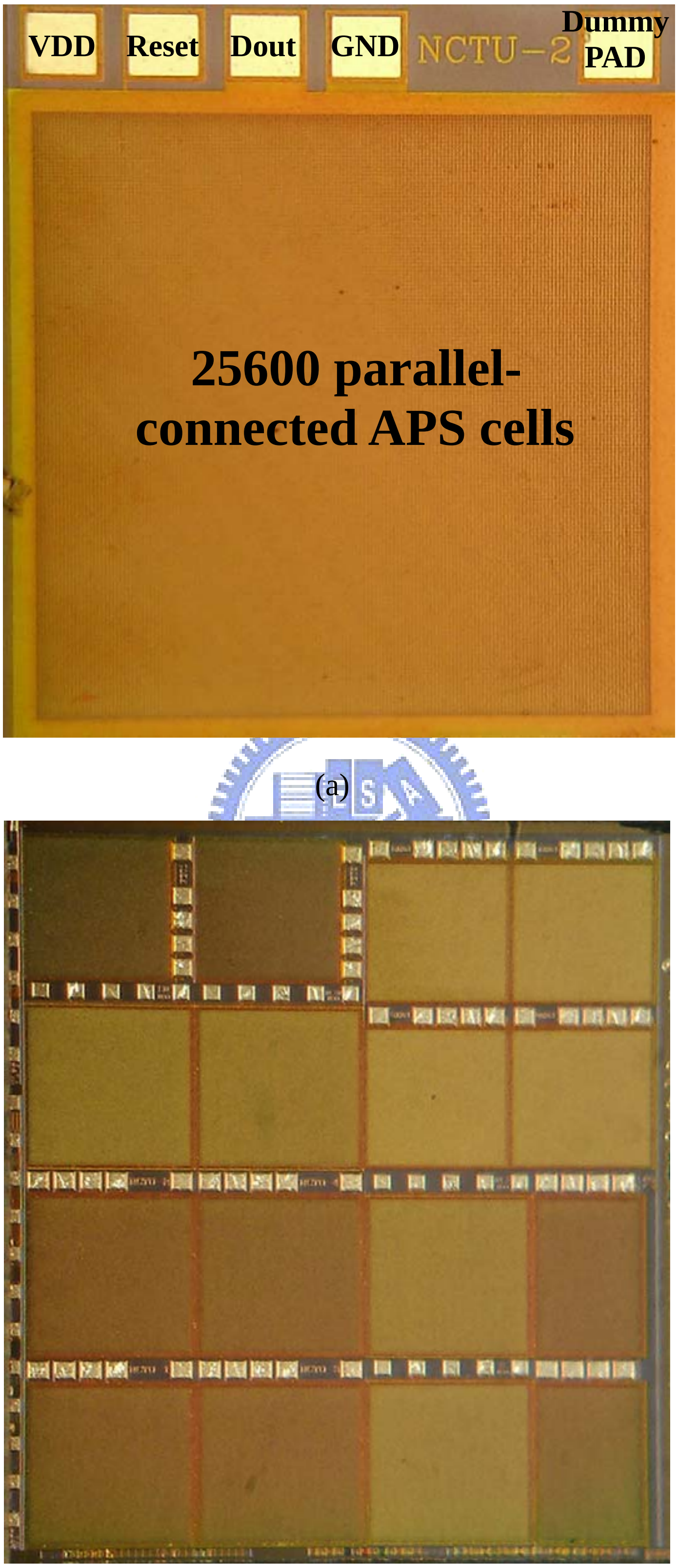
(b)



(c)

(d)

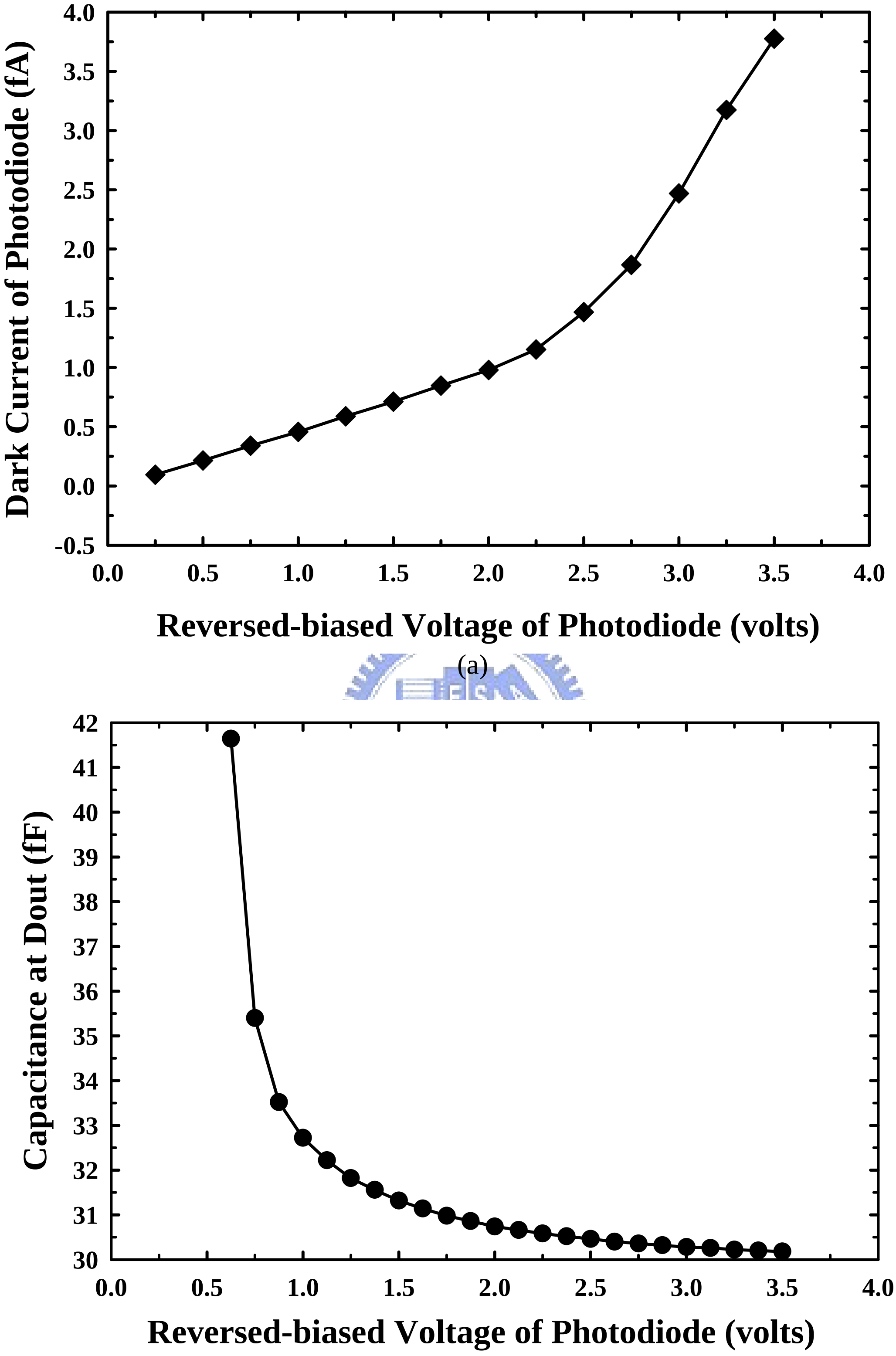
Fig. 3.4 Layout of photodiode in 5 μm x 5 μm APS cell: (a) Type P1: fill factor = 32%. (b) Type P2: fill factor = 15%. (c) Type C1: fill factor = 32%. (d) Type C4: fill factor = 15%.



(a)

(b)

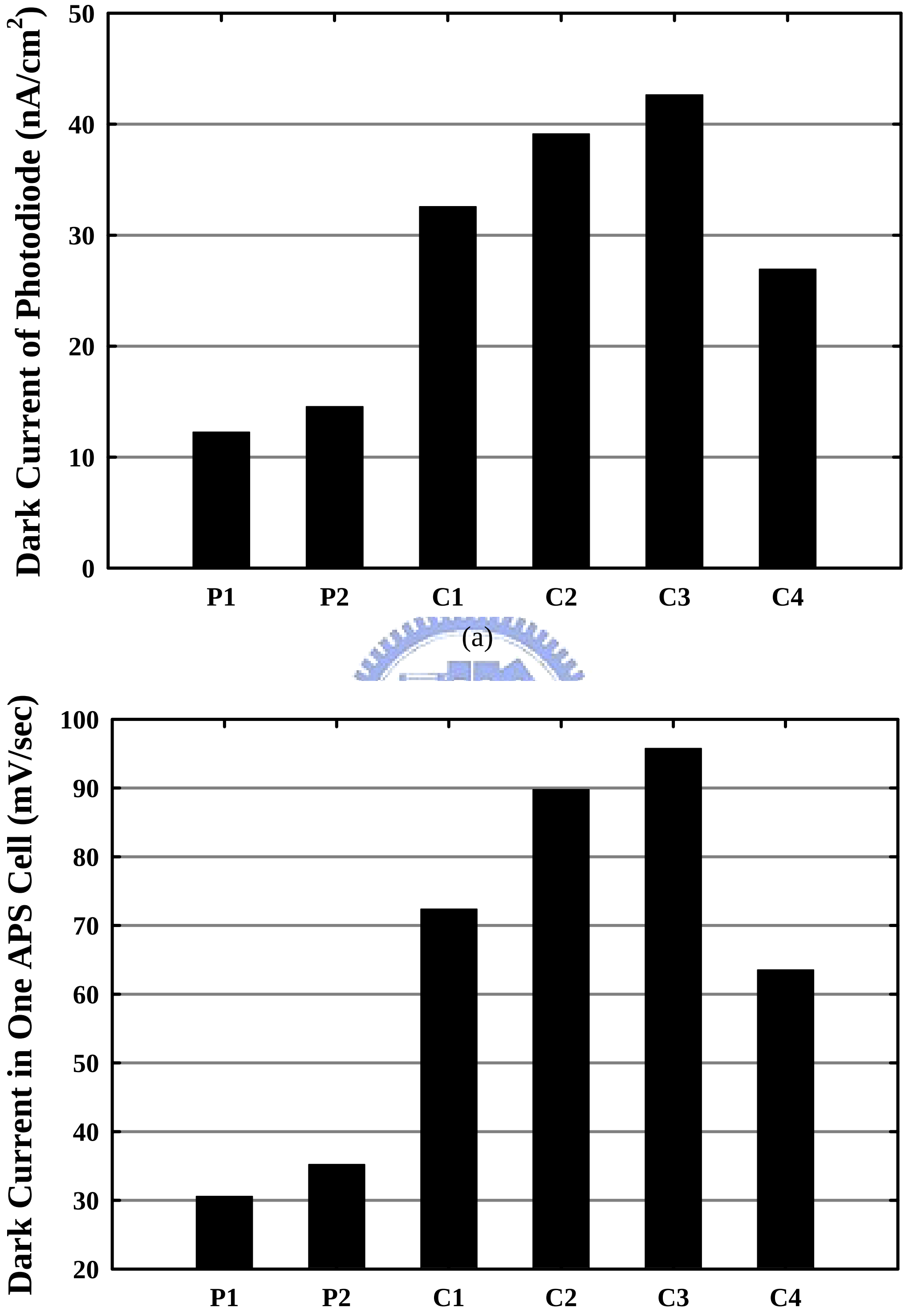
Fig. 3.5 Photographs of (a) one photodiode structure in test chip and (b) overall test chip.



(a)

(b)

Fig. 3.6 Dark current characteristics of photodiode in an APS cell with the photodiode of Type P1: (a) Current to voltage curve: I(V). (b) Capacitance to voltage curve: C(V).



(a)

(b)

Fig. 3.7 Measurement results of dark current at the reverse-biased voltage of 2 V: (a) One photodiode. (b) One APS cell for imager applications.

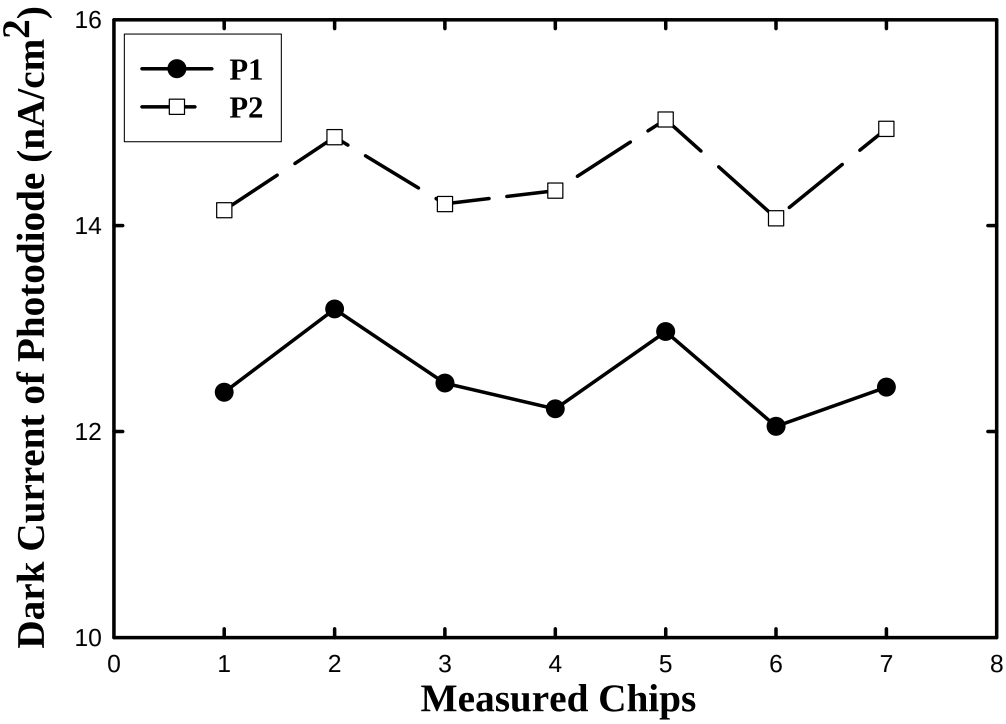


Fig. 3.8 Measurement results of dark current variations of Type P1 and P2 at the reverse-biased voltage of 2 V among seven different chips.

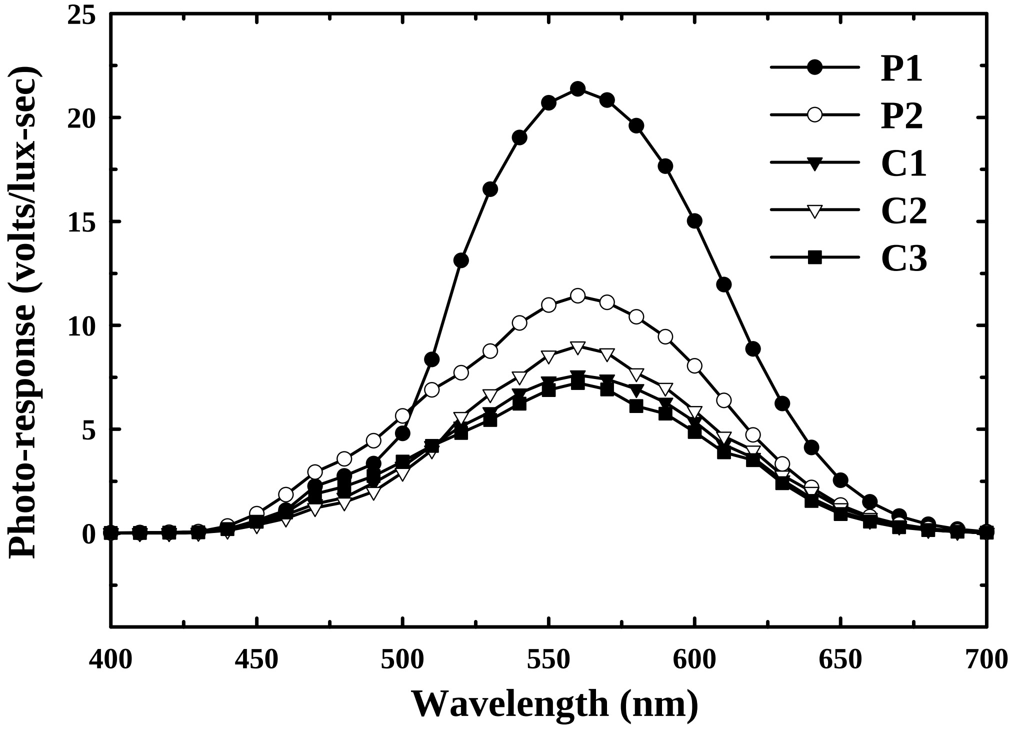


Fig. 3.9 Spectral responses in the photodiode structures of Type P1, Type P2, Type C1, Type C2, and Type C3.

CHAPTER 4

A NEW CMOS PIXEL STRUCTURE FOR LOW-DARK-CURRENT AND LARGE-ARRAY-SIZE STILL IMAGER APPLICATIONS

4.1 INTRODUCTION

Temporal noise sets the fundamental limit on image sensor performance at room temperature [86]. The dominant source of temporal noise in high illumination is the shot noise that is proportional to the sum of photocurrent and dark current in a photodiode [86]. Large dark current in the photodiode array of a CMOS imager could lead to high noise, low signal-to-noise ratio (SNR), non-uniformity, low scalability, and reduced dynamic range. Therefore, reducing dark current in the photodiode also eliminates the temporal noise in CMOS imager at room temperature.

Dark current is dominantly generated from the reverse-biased photodiode and parasitic pn junctions in the pixel. Generally, higher (lower) reverse-biased voltage leads to larger (smaller) dark current. In the conventional active pixel sensor (APS) [22], [87], [88] the dark current is dominantly generated from the photodiode, which is different in every pixel due to the different reverse-biased voltages of photodiodes when the incident light on every pixel is not the same. Thus, the effect of dark current cannot be reduced even under the use of dummy photodiode in the pixel. In the passive pixel sensor (PPS) [22], the dark current is generated from both photodiode and parasitic pn junction in the column bus. The two effects are also different in every pixel during the signal readout operation.

Several techniques have been proposed to cancel dark current such as differential passive pixel imager with FPN reduction [89] and phototransistor pixel sensor with dark current cancellation [90]. The differential passive pixel imager still cannot effectively reduce dark current due to the mismatch between the photodiode in the photodiode array and that in the dummy shielded pixel. The structure of phototransistor pixel sensor with dark current cancellation contains one dummy shielded photodiode in each pixel [90]. The total dark current still cannot be effectively cancelled because the reverse-biased voltage of the photodiode differs from that of the dummy shielded photodiode. In addition, the large pixel size in this structure degrades the image resolution and increases cost.

Fill factor is another parameter considered in the design of high-resolution and large-array-size CMOS imager. High fill factor could lead to high spectral sensitivity under the same pixel size. In other words, the pixel must be composed of devices as few as possible. Among the APS CMOS imagers, the pixel structure composed of one photodiode and three MOSFETs cannot be effectively shrunk to satisfy the requirements of small pixels with the advancement of CMOS technology because most pixel area is filled by the three MOSFETs and the contacts for connections. In the conventional PPS CMOS imager, there are one MOSFET and one photodiode. Although the fill factor is high, the noise from the capacitive column bus is large [22]. In addition, passive pixel cannot be shrunk too small and the array size cannot be too large because the small capacitance of photodiode and the large capacitance of column bus will result in high readout noise [22].

Several other pixel structures for the design of large-array-size CMOS imager such as the differential passive pixel imager [89] and the imager with pixel-level ADC

[91] have been proposed to reduce pixel area and maintain high performance. However, the effect of dark current is still the problem to be solved.

It is the aim of this chapter to propose a new pixel structure called the pseudo active pixel sensor (PAPS) for the large-array-size still CMOS imagers with low dark current and high fill factor [92]. A new readout circuit is also proposed to readout the sensor current to the column bus and performs the outside-pixel integration using the APS-like structure. The new readout circuit keeps the biases of both photodiode and parasitic pn junctions in the column bus at or near zero bias to achieve low dark current, low column leakage current, and high linearity. The improved double delta sampling (DDS) circuit is used to reduce fixed pattern noise, clock feedthrough noise, and the noise from the effect of channel charge injection. From the experimental results, it has been shown that the proposed new pixel structure and readout circuit can be applied to the design of low-dark-current and large-array-size still CMOS imagers.

The rest of this chapter is organized as followers. In Section 4.2, the new structure of the proposed pseudo active pixel sensor (PAPS) is described and the principles to reduce dark current and increase fill factor are presented. The operation of improved DDS circuits is also described. In Section 4.3, the chip architecture is described. In Section 4.4, the simulation results, chip layout, and experimental results are presented, analyzed, and compared to verify the advantageous performance of the proposed new pixel structure and readout circuit. Finally, the summary is given in Section 4.5.

4.2 PIXEL STRUCTURE AND READOUT CIRCUITS

4.2.1 Pseudo Active Pixel Sensor (PAPS) Structure

The proposed pseudo active pixel sensor (PAPS) structure is shown in Fig. 4.1. The pixel structure is composed of one photodiode and one row select switch. The integration capacitor and source follower in the APS structure are moved out of the pixel. The cathode of the photodiode is connected to the pixel bias voltage Vpix, whereas the anode is connected to the column bus through the select switch. The column bus biased at Vcom which is nearly the same as Vpix. Thus the effective voltage drop across the pixel is zero or nearly zero. This structure is the same as that of the passive pixel sensor (PPS), but the pixel voltage drop is kept at zero. Moreover, the readout operation is different from that of the conventional PPS structure, as will be described later.

In order to achieve a small pixel size, only a single type of MOSFET is used as the select switch within the pixel. As shown in Fig. 4.1, the PMOSFET is selected as the row switch in the pixel because the voltage at the N-well of the PMOSFET can be connected to the positive voltage Vpix to keep both source and drain junctions at the bias voltage of 0 V. Furthermore, to achieve the antiblooming effect, the P+-diffusion/N-well junction is used as the photodiode to ensure that the excess charges generated by strong incident light can be drained away by the vertical substrate PNP bipolar-junction-transistor [93]. This prevents the excess charges from leaking to the neighboring pixels or directly to the column bus. The P+-diffusion of the photodiode can be connected to the source of Mrsel to increase the fill factor.

In the N-well CMOS technology, the P+/N-well pn junction is used as the photodiode. In a test chip, 10000 photodiodes are connected in parallel to form a photodiode array. The current-to-voltage (I-V) characteristics of a single photodiode can be obtained by dividing the measured total current by 10000. The measured dark current I_d of the photodiode shielded from light and the measured photocurrent I_p of the photodiode generated under the light of 20mW bulb are shown in Figs. 4.2(a) and

4.2(b), respectively. As shown in Fig. 4.2(a), the dark current is increased with the reverse-biased voltage V_R because higher electric field is generated in the pn junction depletion region when the reverse-biased voltage is higher. For the same reasons, the photocurrent is also increased with the reverse-biased voltage.

In Fig. 4.2(a), the dark current I_d of the photodiode approaches zero when the reverse-biased voltage V_R is decreased toward zero. However, the photocurrent of I_{p1} at the reverse-biased voltage of 0 V is not much smaller than that of I_{p2} at the reverse-biased voltage of 3 V as shown in Fig. 4.2(b). The measured values of I_{d1}, I_{d2}, I_{p1}, I_{p2}, I_{p1}/I_{d1}, and I_{p2}/I_{d2} are listed in Table 4.1. From the measurement results, it is found that the ratio of the photocurrent I_{p1} to the dark current I_{d1} at the reverse bias of 0 V is much larger than I_{p2}/I_{d2} at the reverse bias of 3 V. Generally, the pn-junction photodiode has the characteristic as

$$\left.\frac{I_p}{I_d}\right|_{|V_R|=0} > \left.\frac{I_p}{I_d}\right|_{|V_R|>0} \qquad (4.1)$$

Thus, biasing the photodiode at or near zero voltage can achieve lower dark current, lower shot noise [86], and higher signal-to-noise ratio (SNR) as compared with that at higher reverse-biased voltage.

From the above results, it is shown that both photodiode and all the parasitic pn junctions in the row select switches must be operated at the reverse bias of 0 V to effectively reduce the dark current. Thus the voltage difference between the cathode of the photodiode and the column bus is operated at 0 V in the proposed PAPS structure in order to maintain the zero bias of both photodiode and parasitic pn junctions as shown in Fig. 4.1. When the row select switch of Mrsel is on, the voltage at the source of Mrsel is the same as that of the column bus which is Vpix. The photodiode, the parasitic pn junction between the source and the substrate of Mrsel, and the parasitic pn junction between the drain and the substrate of Mrsel are all operated at the reverse-biased voltage of 0 V. The photocurrent is then delivered to the column bus for charge integration while both dark current of the photodiode and leakage current of the parasitic pn junctions are decreased to near 0 A.

When the row select switch of Mrsel is turned off by setting the signal of Rsel at Vdd, the circuit diagram of PAPS is shown in Fig. 4.3. In Fig. 4.3, the source of Mrsel, N-well, and the drain of Mrsel form the parasitic lateral pnp BJT device Q1 with base and collector connected to Vpix and Vcom, respectively, and the emitter connected to node A. The source of Mrsel, N-well, and P-substrate form the parasitic vertical pnp BJT device Q2 with the P-substrate collector connected to ground. Under incident light, the photodiode is forward-biased with the voltage drop equal to V_F and operated as a solar cell. Thus the current of I_F is expressed as [94]

$$I_F = I_{p0} - I_{SP}(e^{\frac{V_F}{V_T}} - 1) \qquad (4.2)$$

where I_{SP} is the reverse saturation current of photodiode, I_{p0} is the photocurrent when the photodiode is biased at 0 V, and V_T is the voltage equivalent of temperature. With V_F as the forward substrate bias between source and body of Mrsel, the threshold voltage Vtp of Mrsel is decreased due to the body effect. But the row select switch device Mrsel is still kept off because the voltage at the node A which is Vpix+V_F, is smaller than Vdd+Vtp. However, the collector current I_{C1} of Q1 flows into the column bus as the dark current. As shown in Fig. 4.3, the current of I_F in the photodiode is equal to the sum of the emitter current I_{E1} of Q1 and I_{E2} of Q2. Furthermore, both of the parasitic laternal pnp BJT device Q1 and parasitic vertical pnp BJT device Q2 are operated in the forward-active region because their emitter-base junctions are forward-biased and collector-base junctions are reverse-biased. From the simplification of Ebers-Moll current equation, we have

$$I_F = I_{p0} - I_{SP}(e^{\frac{V_F}{V_T}} - 1) = I_{E1} + I_{E2} = I_{S1}(e^{\frac{V_F}{V_T}} - 1) + I_{S2}(e^{\frac{V_F}{V_T}} - 1) \qquad (4.3)$$

where I_{S1} and I_{S2} are the reverse saturation current of parasitic lateral BJT device Q1 and parasitic vertical BJT device Q2, respectively. From (4.3), the total equivalent dark current I_{TED} from the parasitic BJT device Q1 flowing into the column bus can be expressed as

$$I_{TED} = (Np - 1)I_{C1} = (Np - 1)\alpha I_{E1} = (Np - 1)\alpha I_{p0}\frac{I_{S1}}{I_{SP} + I_{S1} + I_{S2}} = 2.107 \times 10^{-5} \times (Np - 1)I_{p0} \quad (4.4)$$

where Np is the number of pixels connected to the same column and α is the common-base current gain of Q1.

The values of I_{SP}, I_{S1}, I_{S2}, and α in the proposed PAPS CMOS imager with 0.25 μm CMOS technology and channel width(length) of Mrsel are given in Table 4.2. From (4.4), the ratio of I_{p0}/I_{TED} is larger than that of APS CMOS imager if Np is smaller than 2000. Thus the dark current contributed by the current I_{TED} in the proposed PAPS CMOS imager is smaller than the dark current of APS CMOS imager if Np is smaller than 2000 which is equivalent to a 4M-pixel imager if a square pixel array is used. Thus, the proposed PAPS CMOS imager can be applied to the large-array-size imager with the dark current contributed by I_{TED} in (4.4) smaller than the dark current of APS CMOS imager.

The value of I_{S1} can be decreased by increasing the channel length of Mrsel. Lower I_{S1} leads to larger ratio of I_{p0}/I_{TED} in (4.4) and thus larger of Np. However, the fill factor is decreased to about 54% if the channel length of Mrsel is 0.7 μm. This fill factor is still larger than that of APS CMOS imager.

4.2.2 Zero-Bias Column Buffer-Direct-Injection (ZCBDI) Structure

Fig. 4.4 shows the PAPS pixel and the column readout circuit called the zero-bias column buffer-direct-injection (ZCBDI) structure with the P+/N-well photodiode. The bias voltage Vpix in the pixel is maintained at 1.8 V. In the left side of the pixel circuit, all the deselected PMOSFETs as the row select switches in the same column are added to include their leakage currents to the column bus. For a 352 x 288 (CIF) imager, the total number of deselected PMOSFETs is 287. The common N-well of all selected and deselected PMOS row switches is connected to 1.8 V to maintain zero reverse bias in the source/drain pn junctions. Thus the total column leakage current due to the deselected PMOS switches can be reduced to a very low level.

The column readout circuit is composed of the buffer-direct-injection (BDI) [95], [96] readout structure, the NMOS transistor Mrst as the reset switch, the APS-like structure with the PMOS source follower Mp1 and Mp2, and an optional integration capacitor Cint with a switch. In the BDI readout structure, the inverting input of a gain stage with gain A is connected to the column bus (CB) and the noninverting input is connected to the bias voltage Vcom. The output of the gain stage is connected to the gate of Min as a common-gate input stage. The gain stage is implemented by a CMOS differential pair to reduce the chip area. The circuit diagram of the gain stage is shown in Fig. 4.5. The device parameters in the circuit diagram of the gain stage are given in Table 4.3. Through the BDI circuit, the bias of column bus is controlled by the input voltage Vcom of the differential pair. The value of Vcom is set to be 1.8 V by a low-noise constant voltage source to maintain the voltage of column bus at or near 1.8 V. The additional power consumption of the differential pair in each column readout circuit can be reduced by proper design of gain stage with low bias current. The ZCBDI readout structure is similar to the readout circuit used in infrared focal plane array to obtain stable zero detector bias [97].

In additional to maintain the stable bias at the column bus, the input impedance in the BDI readout structure is decreased by a factor of A due to the negative-feedback structure. The injection current from the pixel is mainly drained toward the column bus due to the low input impedance. The current injection efficiency of the BDI readout structure which is the current ratio between Iin and Ir in Fig. 4.4 is expressed as [97], [98]

$$\eta(s) = \frac{(1+A)g_m Ro}{1+(1+A)g_m Ro}\left(\frac{1}{1+s/2\pi f_{BW}}\right) \tag{4.5}$$

$$f_{BW} = \frac{1+(1+A)g_m Ro}{2\pi Ro C_T} \tag{4.6}$$

where A is the gain of the buffer, g_m is the transconductance of Min, C_T is the capacitance at the column bus, and Ro is the output resistance of Mrsel. From (4.5), the current injection efficiency is increased by the gain of the buffer. In this design, the gain of A is about 100, which makes the injection efficiency close to 1.

Both the photocurrent from the selected pixel and the leakage current from the deselected pixels are injected into the integration capacitance through the BDI readout structure. However, from (4.4), the ratio between the photocurrent I_{p0} from the selected pixel and the total equivalent dark current I_{TED} from the deselected pixels is large if the number of pixels connected to the same column is small. Thus the current from the deselected pixels is negligibly small as compared with the photocurrent from the selected pixel due to the zero or near zero bias in parasitic pn junctions. The integration capacitance is composed of the gate capacitance of Mp1 and the optional capacitance of Cint with a switch. The optional capacitor of Cint is used to prevent saturation when the incident light is strong and the integration time is long such as the application of still imager in the environment of strong light. This leads to increase the dynamic range of the incident light. In this design, the value of Cint is designed as 0.2 pF, which only occupies small area of the total chip. The readout time of one frame image is longer than that of APS CMOS imager because the current integration is performed outside the pixel. Thus the proposed PAPS CMOS imager is mainly used in the application of still imager.

The photocurrent generated from the selected pixel is integrated on the integration capacitor after the reset operation when Mrst is open. After the integration, the integrated voltage is transferred through the source follower composed of Mp1 and Mp2. The reset switch and the source-follower form an APS-like structure to integrate the photocurrent outside the pixel. At the end of the integration, the reset switch Mrst is turned on and the voltage at the integrating capacitor is also transferred through the source follower to perform the operation of double delta sampling (DDS).

The source follower is composed of the two PMOSFETs of Mp1 and Mp2 with their N-well substrates connected to the sources as shown in Fig. 4.4. Thus the gain of the source follower can be designed to be nearly 1 without the gain loss due to the body effect. The output of the source follower is connected to column sampling circuits in the next stage of double delta sampling (DDS) operation circuit.

The ZCBDI readout circuit can be modified for the applications to the N+/P-substrate photodiode which has lower dark current and higher quantum efficiency. The modified ZCBDI readout circuit for the N+/P-substrate photodiode is shown in Fig. 4.6 where an extra NMOS device Min is added. In Fig. 4.6, the modified ZCBDI readout circuit is composed of the buffer-direct-injection (BDI) [95], [96] readout structure, the PMOS transistor Mrst as the reset switch, the APS-like structure with the NMOS source follower Mn1 and Mn2, and an optional integration capacitor Cint with a switch. The value of Vcom is set to be slightly larger than the threshold voltage Vtn of Min. Thus the bias at the column bus of node CB is equal to near zero voltage. The photodiode is biased at zero or near zero voltage when the row select switch of Mrsel is on. The impedance seen from the node of CB to Vdd is increased by $\frac{1}{g_{min}}$ where g_{min} is the transconductance of Min. To avoid the degraded injection efficiency, the channel geometric ratio W/L of Min should be large enough to increase g_{min}.

4.2.3 Improved Double Delta Sampling (DDS) Operation Circuit

The improved DDS operation circuit is shown in Fig. 4.7. The column sampling circuit is used in each column whereas the output CDS circuit is shared by all the columns. In the column sampling circuit as shown in Fig. 4.7, the NMOS devices of MS and MR controlled by the signals of SHS and SHR, respectively, are sampling switches whereas Mvce controlled by Vce is the equalization switch. The signals generated by the integration of photocurrent and the reset signal transferred through the source follower Mp1/Mp2 are sampled by the two NMOS devices of MS and MR, respectively. Both the effects of clock feedthrough and channel charge injection resulted from the sampling operation of MS and MR in the original DDS circuit [99] will degrade the performance of signal readout. In the improved DDS circuit of Fig. 4.7, the effect of signal-dependent channel charge injection caused by MS and MR during the falling edges of SHS and SHR is reduced by the two added dummy NMOS devices Ma and Mb with their drain and source connected together and their gates connected to the outputs of the two inverters invA and invB, respectively. The size of Ma and Mb is designed to be about one half of the size of MS and MR, respectively, because only the channel charges injected to the source regions of MS and MR are to be compensated by those to both drain and source regions of Ma and Mb, respectively.

The signals after the sampling are held at the nodes of A and B until they are readout to the output CDS circuit when the column switches Mn1 and Mn3 are on.

Since the column readout sampling is performed simultaneously in each column and the sampled column signals are readout to the output CDS circuit successively, the signal from the last column is held for the longest time that is almost equal to the integration time of the photocurrent. The held signal voltages at the last column will be decreased by the leakage currents at the nodes of A and B. An extra capacitor of 0.12 pF is added to the nodes of A and B to avoid the held voltage level from decreasing lower than 1 LSB of the output analog-to-digital converter. The extra capacitor of 0.12 pF is determined by the leakage current I_{leak} at the nodes of A and B, the gain G_{PGA} of the programmable gain amplifier (PGA) before the A/D converter, the node capacitances at the nodes of A and B C_{hold}, and the integration time of photocurrent T_{int}. The equation can be represented as

$$(C_{hold} + 0.12\ \text{pF})\ V_{1LSB} = G_{PGA}\ (I_{leak} \times T_{int}) \tag{4.7}$$

The values of C_{hold} and I_{leak} are determined from the process parameter. All the values of C_{hold}, V_{1LSB}, G_{PGA}, I_{leak}, and T_{int} are summarized in Table 4.4.

The photosignal (reset) voltage is sampled to the gate of Mn2(Mn4) of the second source follower composed of Mn2, Mn1, and Mn5(Mn4, Mn3, and Mn6) and sent out to the output CDS circuit through the column select switches Mn1(Mn3), Csela, and Cselb. The second source follower is composed of NMOS devices because PMOS devices are used in the first source follower. Thus the voltage dynamic range at the output of the second source follower is not reduced by the level shifting of threshold voltage. In the conventional N-well CMOS process, the substrates of all NMOS devices must be connected to the ground together due to the use of a single P-well. Under this circumstance, the source follower composed of NMOS devices suffers from the gain attenuation due to the body effect. However, the 0.25 μm 1P5M CMOS technology used in the design of the imager chip has the mask of deep N-well beneath the P-well. In other words, the potential of the P-well at the top of deep

N-well can be set to any value. Thus the substrates of Mn2 and Mn4 can be connected to their source and the gain in the NMOS source follower is not attenuated by the body effect. The dynamic range of the output voltage is almost equal to that of the voltage at the integrating capacitor although two types of the source follower are used in the design of column readout circuit. The equalization of both photosignal path and reset signal path controlled by Vce is performed after the readout of the held voltage. The equalized voltage at the two nodes of A and B is then readout to the output CDS circuit.

To reduce the load of the column sampling circuits to the output CDS circuit in the high-resolution CMOS imager and increase the readout speed, every eight column switches are connected together to one switch Csela whereas eight Csela switches are further connected to one switch Cselb [99]. In the output CDS circuit, the NMOS devices Mn7(Mn8) controlled by the signal Clamp is to clamp the voltage at the gate of Mp3(Mp5) in the output source follower Mp3 and Mp4 (Mp5 and Mp6) to Vb3. The capacitor of 2.3 pF are used to perform the operation of correlated double sampling (CDS).

The major operational timing diagram is shown in Fig. 4.8. Firstly, the row select signal Rsel#1 is low and the Reset control signal is high to reset the voltage at the integrating capacitor to 0 V. After the reset operation, the photocurrents of all pixels in the Row#1 are integrated at the gate of Mp1 of Fig. 4.7 during the integration time. Then the control signal of SHS is on to sample the photo-signal in the output of the first source follower Mp1/Mp2 to the node A of Fig. 4.7 as VS. After that, the Reset control signal is on again and then the control signal of SHR is on to sample the reset signal in the output of the first source follower to the node B of Fig. 4.7 as VR when the Reset control signal is off. As in the APS structure, the duration of reset time is kept long enough to eliminate the amount of residual charges due to incomplete reset. That is, the amount of KTC noise generated by the trapping of the switch thermal noise in the integration-reset function at the node D of Fig. 4.7 is the same in VS and VR if the settling time of the voltage at the node D of Fig. 4.7 during the reset operation is shorter than the reset time [86]. Thus the KTC noise due to the reset operation can be reduced by the CDS operation. The reset signal must be sampled after the Reset control signal is off because the effect of clock feedthrough on VS and VR from the Reset control signal is the same which can be reduced by the CDS operation. The integration time T_{int} and frame rate are expressed as

$$T_{int} = NT_{odr} \qquad (4.8)$$

$$\text{Frame rate} = 1/[M(N+3)T_{odr}] \qquad (4.9)$$

where M, N, and T_{odr} are row number of imager, column number of imager, and the reciprocal of output data rate, respectively. The registration time of one image is equal to the reciprocal of frame rate.

In the still imager application, the integration time can be adjusted according to the background light intensity. The photo-generated charges in the PAPS CMOS imager can be the same as that in the conventional APS CMOS imager by increasing the integration time. Under this circumstance, the value of signal-to-noise ratio (SNR) is increased due to the lower dark current which leads to lower shot noise. But the frame rate is smaller than that of APS CMOS imager. If high frame rate is required, the background light intensity should be increased to decrease the required integration time. Under this Circumstances, the optional capacitor Cint is not used because the voltage saturation at the node D of Fig. 4.4 will not be occurred.

The clamp signal in the output CDS circuit is then turned on to clamp the gate voltages of MP3 and MP5 to Vb3. Then, Csel, Csela, and Cselb are on to transfer the signal from the column sampling circuit to the output CDS circuit. Finally, Clamp is off and Vce is on, the voltage at both nodes of A and B of Fig. 4.7 becomes

(VS+VR)/2. If no loss in the stored charges of the capacitor, then the voltage change at the capacitor of 2.3 pF is transferred to the output node of the output source follower composed of Mp3 and Mp4(Mp5 and Mp6) as shown in Fig. 4.7. Thus we have [99]

$$Vout\_s \cong \frac{VR-VS}{2} + Vb3 + V_{cf,Mvce} + V_{SG,Mp3} \qquad (4.10)$$

$$Vout\_r \cong \frac{VS-VR}{2} + Vb3 + V_{cf,Mvce} + V_{SG,Mp5} \qquad (4.11)$$

where $V_{cf,Mvce}$ is the effect of clock feedthrough on the node of A and B of Fig. 4.7 when the MOSFET of Mvce is on and $V_{SG,Mp3}$($V_{SG,Mp5}$) is the voltage drop between source and gate of Mp3(Mp5). As may be seen from (4.10) and (4.11), the CDS operation is realized in the output CDS circuit. The fixed pattern noise in the NMOS source follower of column sampling circuit can be reduced by this CDS operation. The two output signals are sent out and subtracted each other by the subtraction circuit in the off-chip data acquisition (DAQ) card. Thus the complete operation of the double delta sampling circuit is realized. The fixed pattern noise caused in the PMOS source follower of ZCBDI circuit in Fig. 4.7 can be reduced by the subtraction in DAQ card. The effect of clock feedthrough by switching the signal of Vce to equalize the voltages at the two nodes of A and B can also be reduced from the subtraction. The final result after the subtraction of DAQ card can be written as [99]

$$Vout\_r - Vout\_s \cong VS - VR + V_{SG,Mp5} - V_{SG,Mp3} \qquad (4.12)$$

4.3 CHIP ARCHITECTURE

The block diagram of the proposed pseudo active pixel sensor (PAPS) CMOS imager is shown in Fig. 4.9. The 352 x 288 (CIF) format of CMOS imager is taken as an example to realize the new PAPS structure. As shown in Fig. 4.9, the proposed

PAPS pixel is composed of one photodiode and one select switch. The integration capacitor is put in the column readout circuit to perform off-pixel integration. The row decoder and the row counter on the left side of pixel array are used to generate the control signals for the row switches. The column decoder and the column counter on the top side of pixel array are used to generate the control signals for the column reset operation, the column switches, the improved double delta sampling (DDS) circuit of Fig. 4.7, and the row counter. Each column of the pixel array has a column readout circuit including the ZCBDI circuit to lower the leakage current in the column bus and the column sampling circuits to reduce the fixed pattern noise. The column readout circuit generates two analog output voltages. One is the signal proportional to the gray scale intensity of the image whereas the other is the signal proportional to the reset voltage at the integration capacitor. The output CDS circuit is used to drive the external loads and perform the CDS operation.

The image information is transformed as the photocurrent in the pixel array by using the photodiode. The photocurrent is delivered to the column bus and converted into a voltage signal proportional to the intensity of image after the current integration outside the pixel. The current-mode readout from pixel to column readout circuit avoids the voltage swing in the highly capacitive column bus. The photosignal and reset signal are used for the operation of the improved double delta sampling (DDS). The two signals generated in the output CDS circuit are delivered to the programmable gain amplifier (PGA), A/D converter, and display system outside the chip to generate the raw image.

4.4 SIMULATION AND EXPERIMENTAL RESULTS

The simulation results of the voltage at node of D and the voltage difference between Vout_r and Vout_s of the output CDS circuit in Fig. 4.7 are shown in Figs. 4.10(a) and 4.10(b), respectively, where the input photocurrent is from 20 pA to 80 pA under the readout frame rate of 30 frames/sec. As may be seen from these figures, the linearity of the readout circuit is greater than 90% and the maximum output swing is equal to 1.29 V. The readout speed is from 100 kHz to 10 MHz, corresponding to the maximum frame rate above 30 frames/sec.

In the experimental chip, a CIF CMOS imager using the proposed PAPS structure is designed and fabricated by using 0.25 μm 1P5M N-well CMOS process. The depth of N+ diffusion, P+ diffusion, N-well, and deep N-well of this CMOS process are summarized in Table 4.5. The pixel size is 5.8 μm x 5.8 μm and can be further shrunk. The layout diagram of a single pixel is shown in Fig. 4.11 where the source of row select transistor is connected directly to the P+ diffusion of the photodiode without contacts to increase sensor area and fill factor. The corner of the photodiode is clipped at 135° to reduce the effect of leakage current at the right angle. The fill factor in the PAPS pixel is 58% that is larger than that of APS pixel reported so far. The fill factor can be designed larger by moving the N-well contact outside the pixel. Thus the pixel size in the proposed PAPS structure can be designed smaller than that of APS pixel if their fill factor is the same.

To obtain the uniform characteristics of the sensor array, two layers of dummy photodiodes are added around the active sensor array. The P+ regions of the dummy photodiodes are connected to N-well to maintain zero bias such as the photodiodes in the active sensor array. The dummy photodiodes are completely shielded by metal 5. In addition, double guard rings are inserted around the sensor cell array to reduce substrate coupling of the digital switching noise. The analog-to-digital converter is not implemented to simplify the design of the test chip. The final chip photograph is shown in Fig. 4.12 where the area except the regions of sensor and capacitor are covered by metal 5 from light shielding. The total chip size is 3110 μm x 2760 μm.

To test the fabricated CIF PAPS CMOS imager chip, a data acquisition card with the function of A/D converter is utilized to capture the image. The measurement setup of image pattern, lens, and imager chip is shown in Fig. 4.13. The original image and the measured grayscale image captured by the fabricated 352 x 288 (CIF) PAPS CMOS imager chip under the white light intensity of 24 lux and Vcom of 1.79 V are shown in Fig. 4.14(a) and 4.14(b), respectively. The blurs produced in Fig. 4.14(b) is due to light bulb and can be avoided by using more uniform light sources. The measured images under the white light intensity of 24 lux and different values of Vcom are shown in Figs. 4.15(a)-(h). When the value of Vcom is 1.79 V, the image quality in Fig. 4.15(a) is good and no observable fixed pattern noise is presented. With the decrease of Vcom from 1.79 V to 1.45 V as shown in Figs. 4.15(b)-(h), the image quality is degraded by the effect of leakage current in the parasitic pn junctions of deselected row switches. The image cannot be clearly seen when the value of Vcom is smaller than 1.45 V because the leakage current from the parasitic pn junctions of deselected pixels is larger than the photocurrent from the selected pixel. Thus the function of the proposed new PAPS CMOS imager is successfully verified.

The measurement results of the proposed PAPS CMOS imager with the value of Vcom equal to 1.79 V are summarized in Table 4.6 where the corresponding parameters of the APS CMOS imager are also given for comparisons. The total power dissipation of the fabricated CMOS imager chip is equal to 24 mW under the power supply of 3.3 V. Dark current was measured by varying the master clock rate and thus linearly controlling the integration time in the dark [99]. An output-referred dark-current-induced-signal of 5.8 mV/sec was measured at room temperature. Based on the conversion gain, the dark current in PAPS CMOS imager is equal to 93 pA/cm^2 which is smaller than that of APS [100], [101] and PPS CMOS imager. The output swing of 1.2 V is smaller than that of simulation results because of the process variations in the threshold voltage of MOSFETs. The photo-sensitivity is shown in Fig. 4.16 and is equal to 0.16 V/lux·s after calculations. The optical dynamic range defined as the ratio of the brightest illuminance without reaching the saturation level of output voltage to the weakest with the output voltage larger than noise level is equal to 72 dB. The sensitivity in the PAPS CMOS imager is smaller than that of APS and PPS CMOS imager due to the low quantum efficiency of P+/N-well photodiode. But the optical dynamic range in PAPS CMOS imager is larger than that of APS [100], [101] and PPS CMOS imager because the dark current in PAPS structure is smaller and the use of the optional capacitor of Cint in Fig. 4.4. There are two sources of FPN, namely, pixel FPN, which is caused by mismatch in the pixel circuit, and column FPN, caused by mismatch in the column readout circuit [100]. The fixed pattern noise (FPN) is 5.3 mV which is smaller than that of APS CMOS imager with DDS circuits [100] due to the larger pixel FPN in APS CMOS imager although the PAPS CMOS imager has major FPN due to column differences which is larger than that of APS CMOS imager. Thus the proposed PAPS CMOS imager can be used in the low-dark-current and high-resolution still imager applications by keeping the value of Vcom equal to or slightly smaller than 1.8 V.

4.5 SUMMARY

In this chapter, a new pixel structure for still CMOS imager application called the pseudo active pixel sensor (PAPS) structure has been proposed and analyzed. In the PAPS structure, the PPS-like pixel circuit, the APS-like column circuit, and the new readout structure called the zero-bias column buffer-direct-injection (ZCBDI) are used to reduce column leakage current, decrease pixel area, and increase fill factor.

The gain loss in the source follower of NMOS devices can be avoided by using the mask of deep N-well to increase the output voltage dynamic range. The improved double delta sampling (DDS) circuits are also used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. An experimental chip of CIF PAPS CMOS imager is designed, fabricated, and measured. The measurement results verify the function of the new proposed PAPS structure.

With the advantageous characteristics of small pixel area, high fill factor, and low dark current, it is expected that the proposed new PAPS CMOS imager structure can be applied to the design of high-quality and large-array-size still CMOS imagers.

Table 4.1 The values of Id1, Id2, Ip1, Ip2, Ip1/Id1, and Ip2/Id2

Id1	0.13 fA
Id2	18.10 fA
Ip1	570 fA
Ip2	880 fA
Ip1/Id1	4384.61
Ip2/Id2	48.62

Table 4.2 The values of ISP, IS1, IS2, α, and width/length of Mrsel

ISP	1.97×10^{-17} A
IS1	4.20×10-22 A
IS2	3.02×10-20 A
α	0.99
width/length of Mrsel	0.50 μm / 0.35 μm

Table 4.3 The device parameters in the circuit diagram of the gain stage

	Width/length
Mp1	0.78 μm / 0.30 μm
Mp2	0.60 μm / 0.65 μm
Mp3	0.60 μm / 0.65 μm
Mn1	0.58 μm / 0.90 μm
Mn2	0.58 μm / 0.90 μm

Table 4.4 The values of Chold, V1LSB, GPGA, Ileak, and Tint

Chold	0.24 pF
V1LSB	0.3 mV
GPGA	8
Ileak	0.45 fA
Tint	30 ms

Table 4.5 The depth of N+ diffusion, P+ diffusion, N-well, and Deep N-well in 0.25 μm 1P5M N-well CMOS process

N+ diffusion	0.1 μm
P+ diffusion	0.1 μm
N-well	1.2 μm
Deep N-well	2.5 μm

Table 4.6 The measurement results of the proposed PAPS CMOS imager with the value of Vcom equal to 1.79 V and its comparisons with that of APS CMOS imager [101]

Pixel Structure	PAPS	APS [101]
Technology	0.25 μm 1P5M N-well CMOS	0.35 μm 1P3M N-well CMOS
Power Supply	3.3 V	3.3 V
Integration Capacitor	8.2 ~ 208.2 fF	–
Output Swing	1.2 V	0.8 V (estimate)
Readout Speed	30 frames/sec	30 frames/sec
Linearity	92%	80% (estimate)
Dark Current	93 pA/cm^2 (room temperature)	370 pA/cm^2 (room temperature)
Photo-sensitivity	0.16 V/lu·s	0.52 V/lu·s
Optical Dynamic Range	72 dB	53 dB
Fixed Pattern Noise (FPN)	5.3 mV	8 ~ 24 mV (estimate)
Chip Size	3110 μm x 2760 μm	5840 μm x 5010 μm
Pixel Area	5.8 μm x 5.8 μm	7.4 μm x 7.4 μm
Array Size	352 x 288 (CIF)	640 x 480
Area of Pixel Array	2041.6 μm x 1670.4 μm	4736 μm x 3552 μm
Fill Factor	58%	25% ~ 40% (estimate)
Fill Factor / Pixel Area	0.0172 μm^{-2}	0.00457 μm^{-2} ~ 0.0073 μm^{-2} (estimate)
Operating Temperature	25°C	25°C
Power Dissipation	24 mW	31 mW

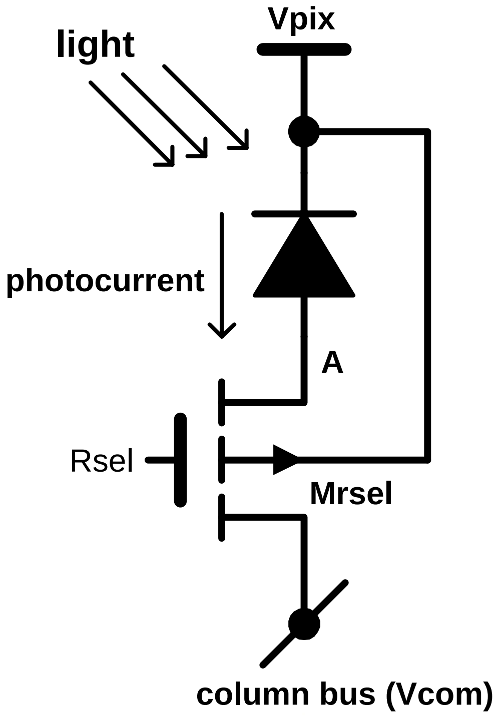
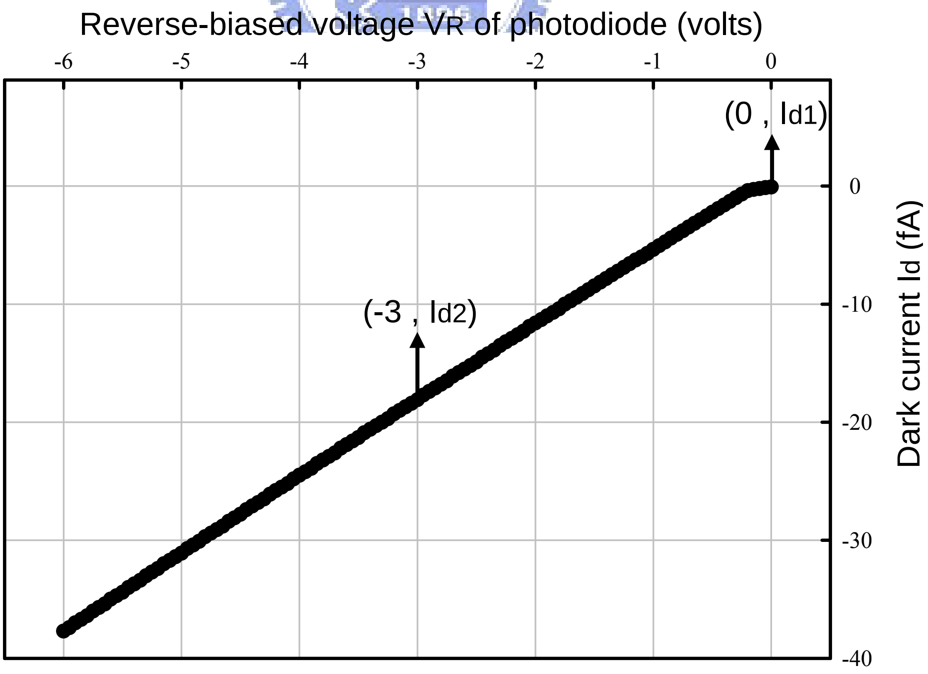
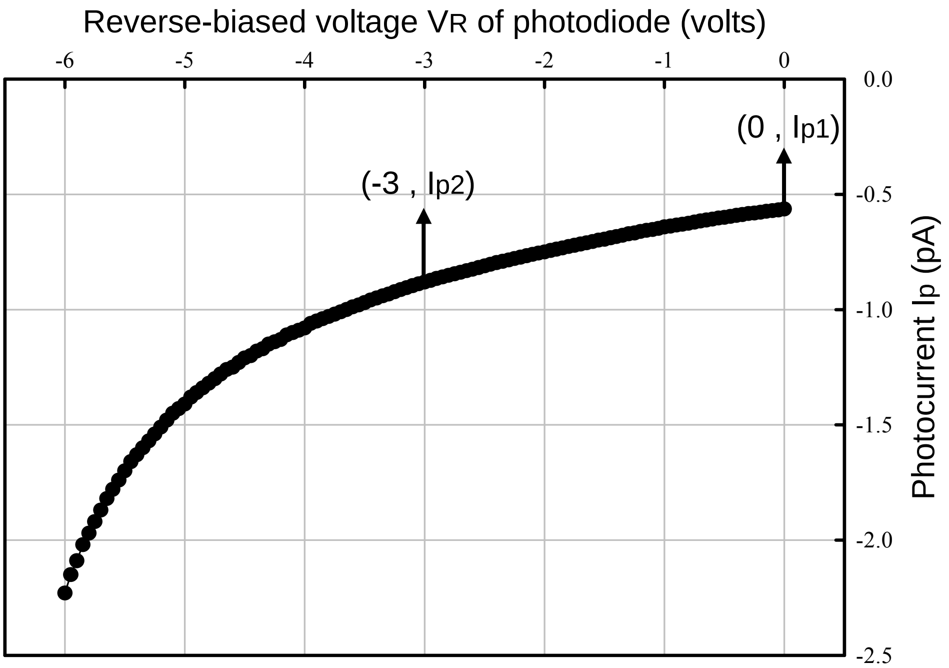


Fig. 4.1 The circuit of the pseudo active pixel sensor (PAPS).



(a)



(b)

Fig. 4.2 The measured (a) dark current I_d and (b) photocurrent I_p of the fabricated P+/N-well photodiode.

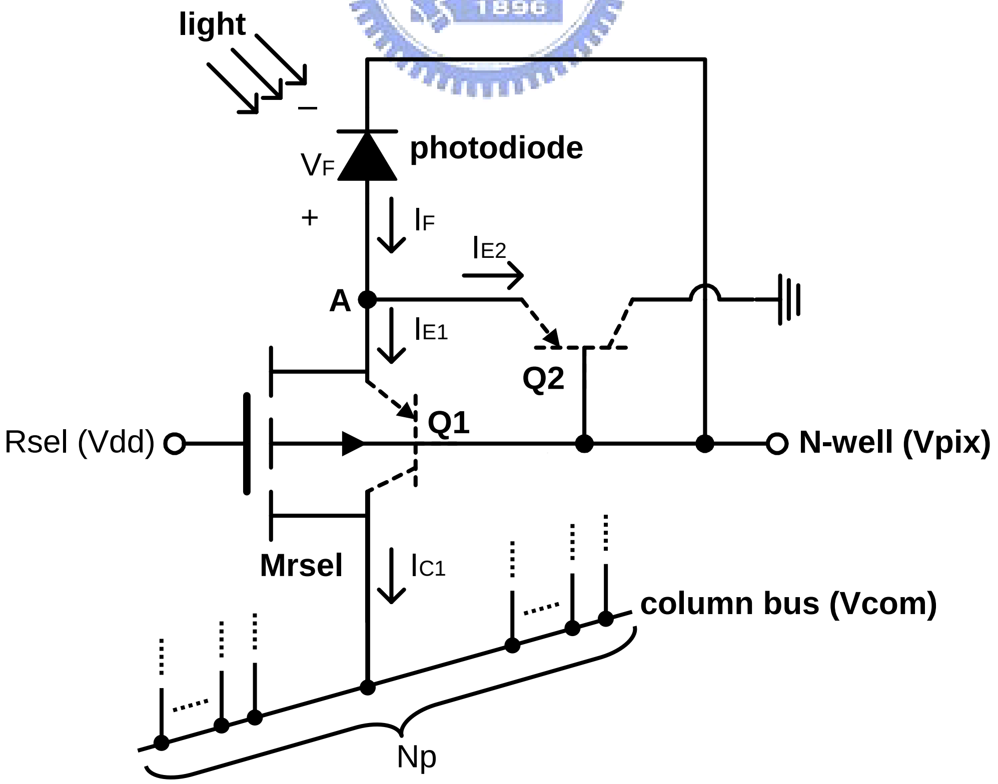


Fig. 4.3 The circuit diagram of PAPS when the row select switch of Mrsel is off.

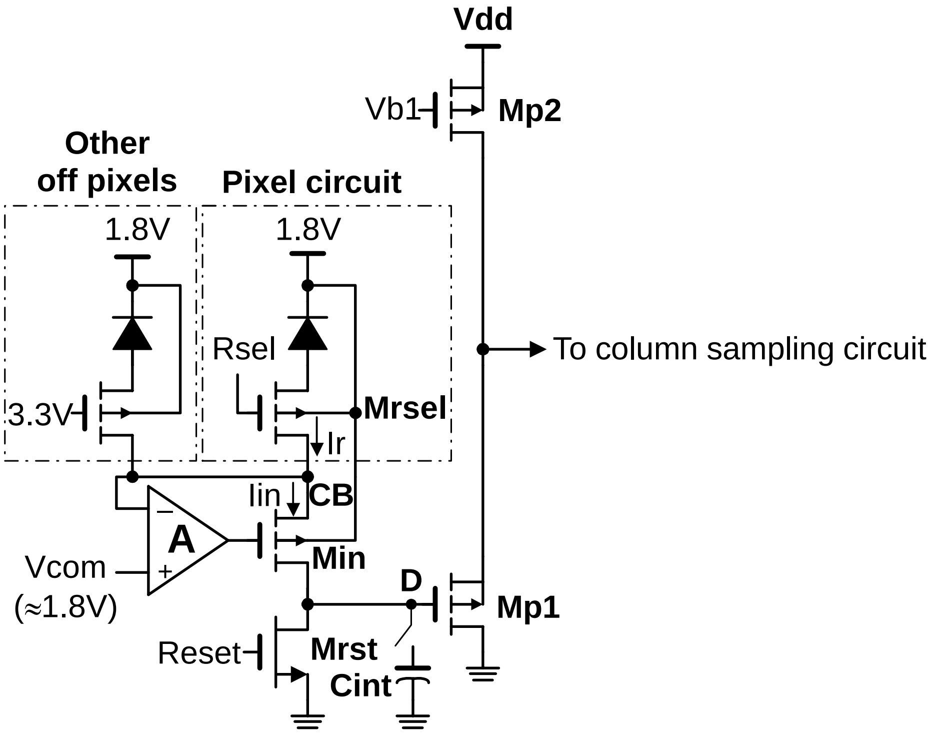


Fig. 4.4 Zero-bias column buffer-direct-injection (ZCBDI) readout circuit with the P+/N-well photodiode.

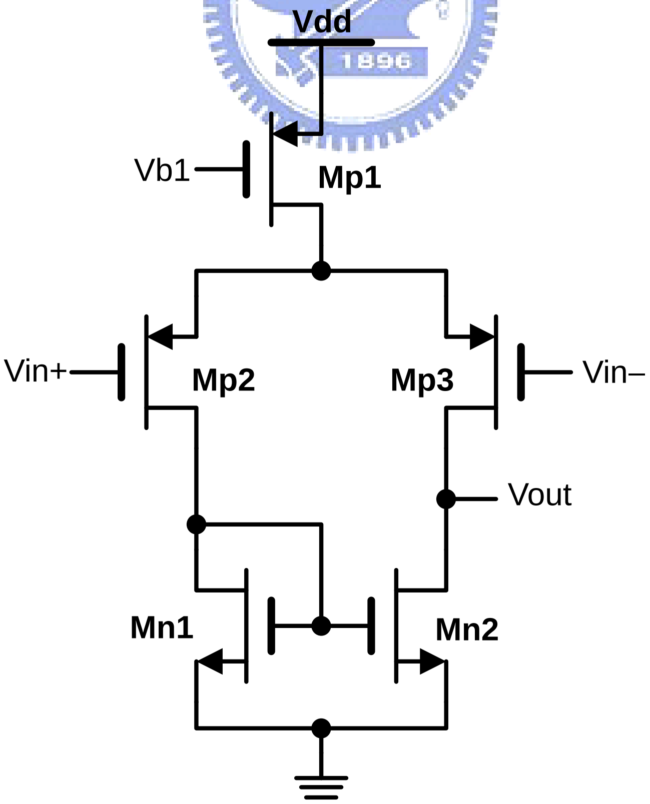


Fig. 4.5 The circuit diagram of the gain stage.

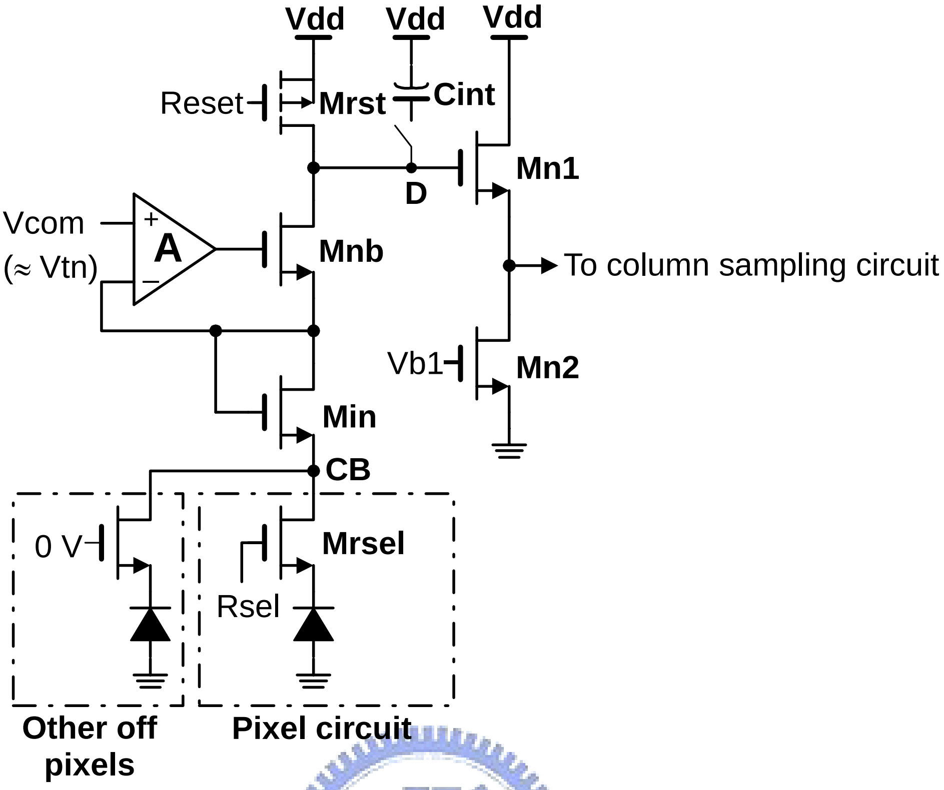


Fig. 4.6 The modified ZCBDI readout circuit with the N+/P-substrate photodiode.

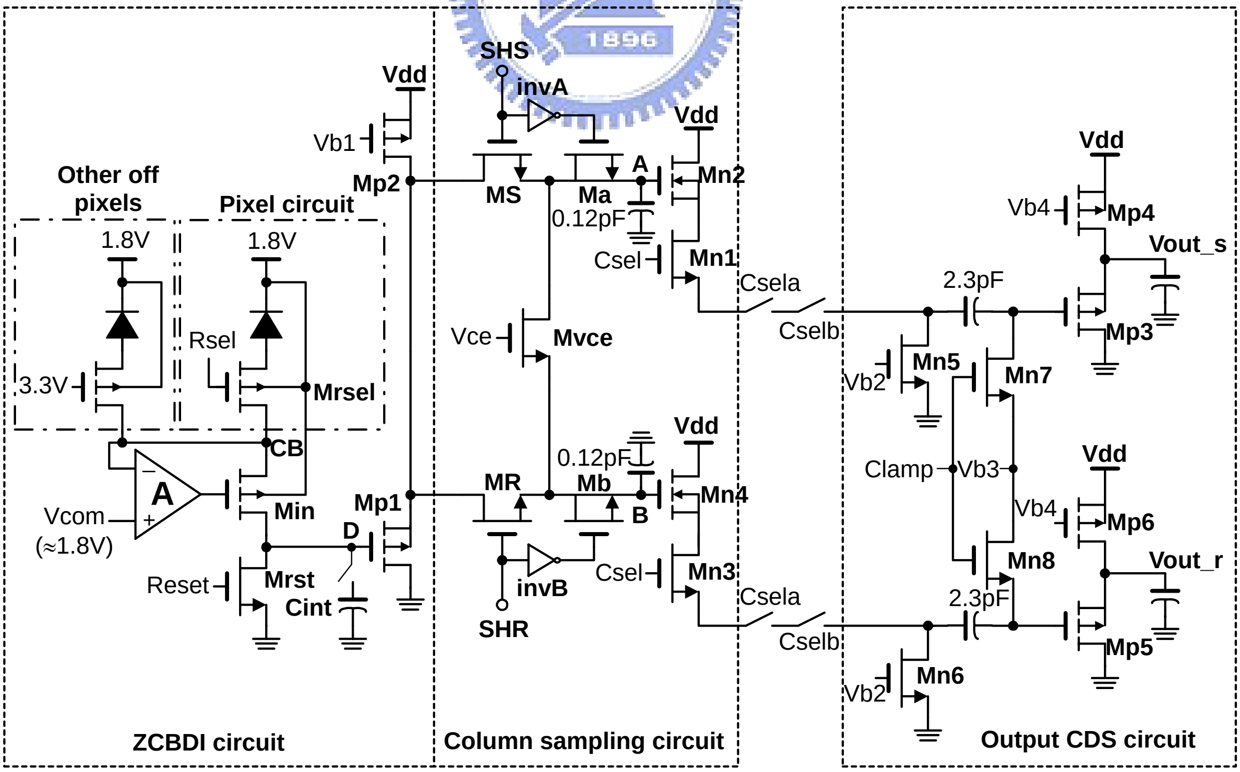


Fig. 4.7 The PAPS structure with ZCBDI readout circuit and the improved DDS circuit.

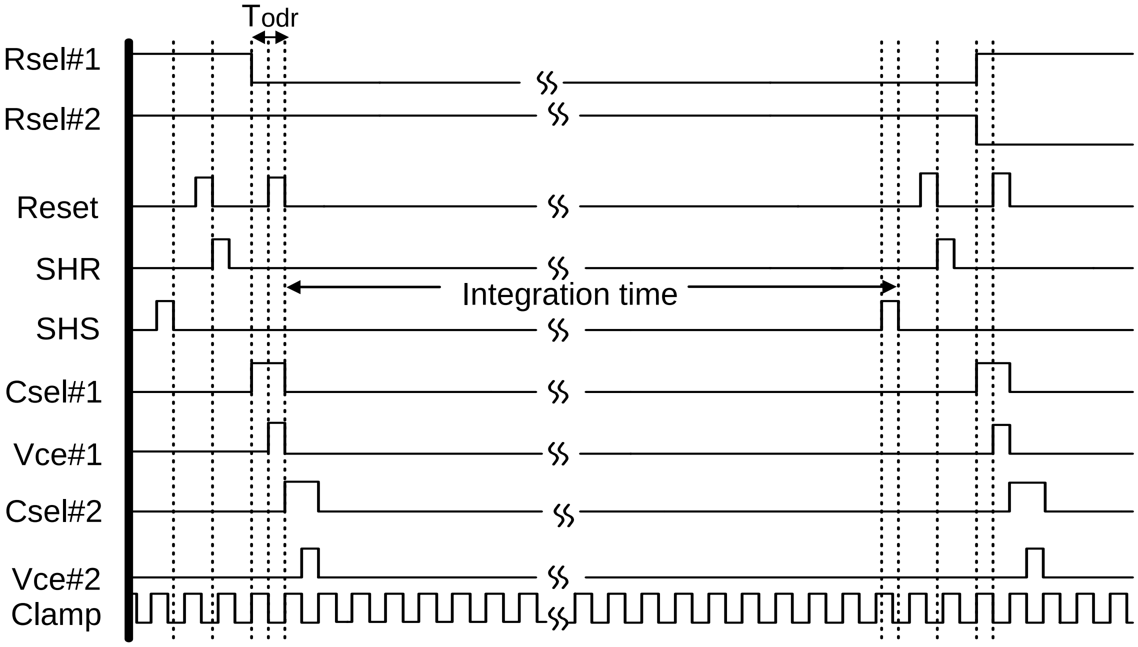


Fig. 4.8 The major timing diagram of the column readout circuit and the output driver circuit.

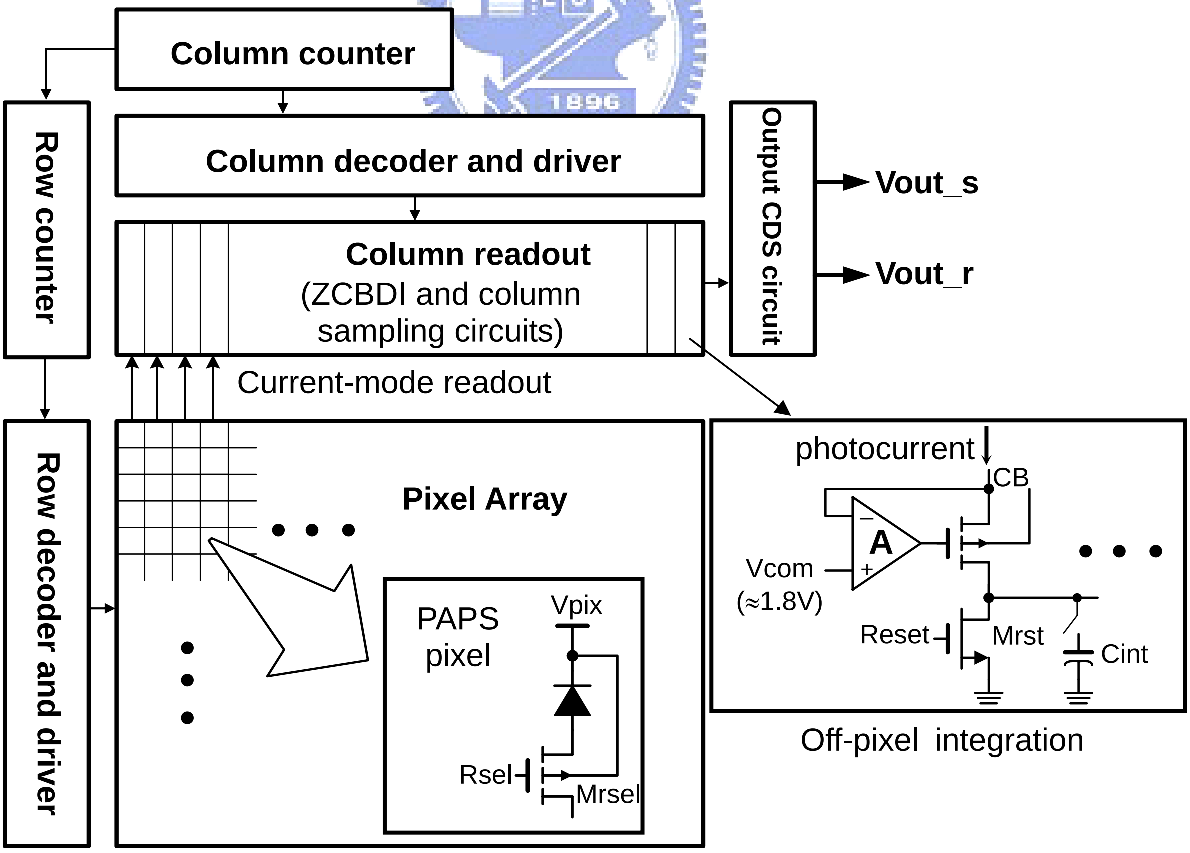
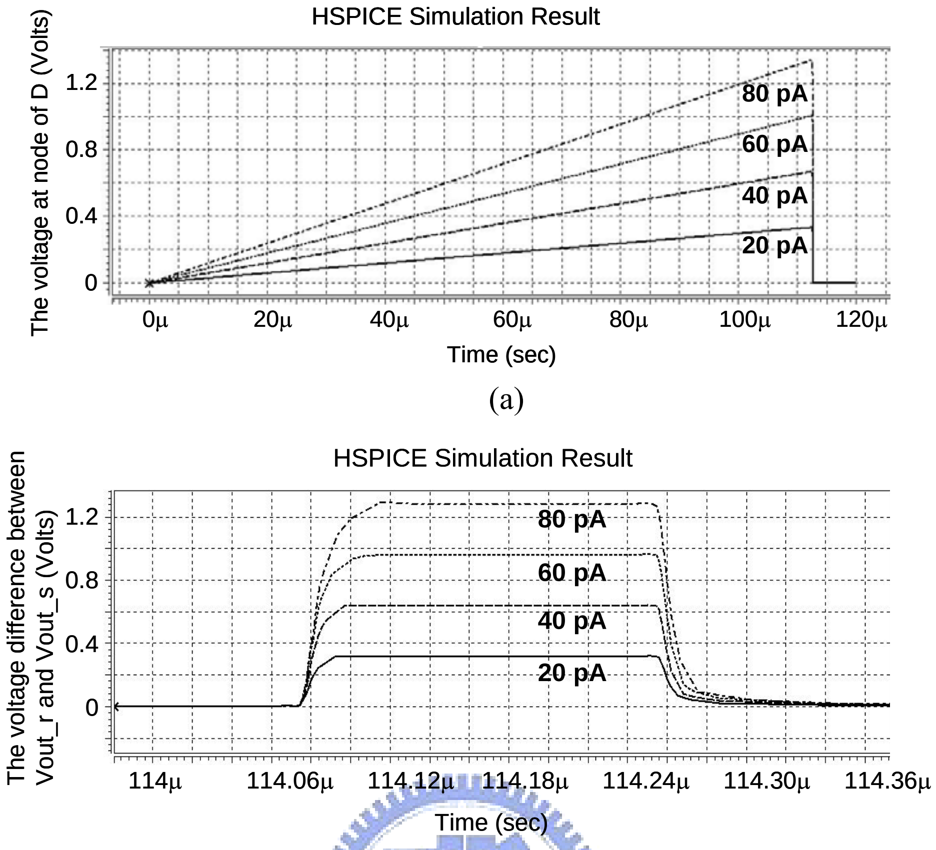


Fig. 4.9 Block diagram of the proposed PAPS CMOS imager.



(a)

(b)

Fig. 4.10 Simulation results of (a) the voltage at node of D and (b) the voltage difference between Vout_r and Vout_s of Fig. 4.6 for the input photocurrent from 20 pA to 80 pA.

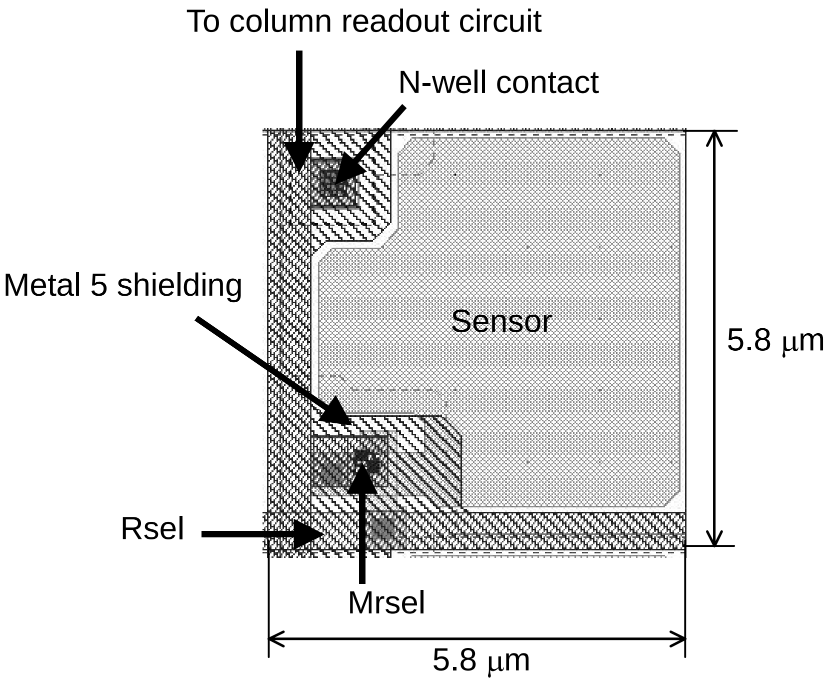


Fig. 4.11 The layout of PAPS pixel.

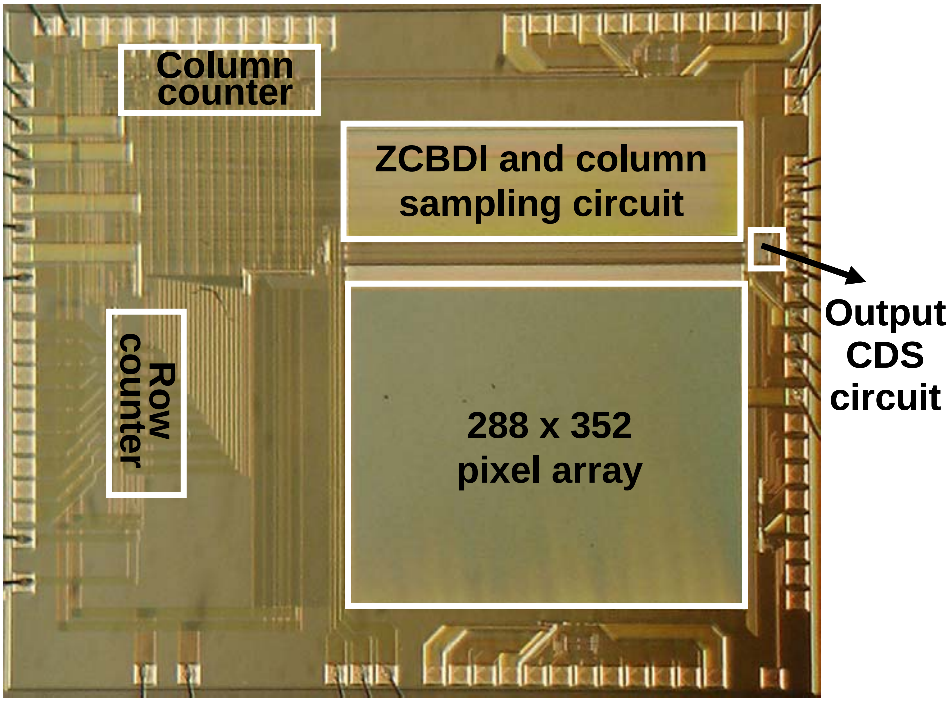


Fig. 4.12 Die photograph of the test chip.

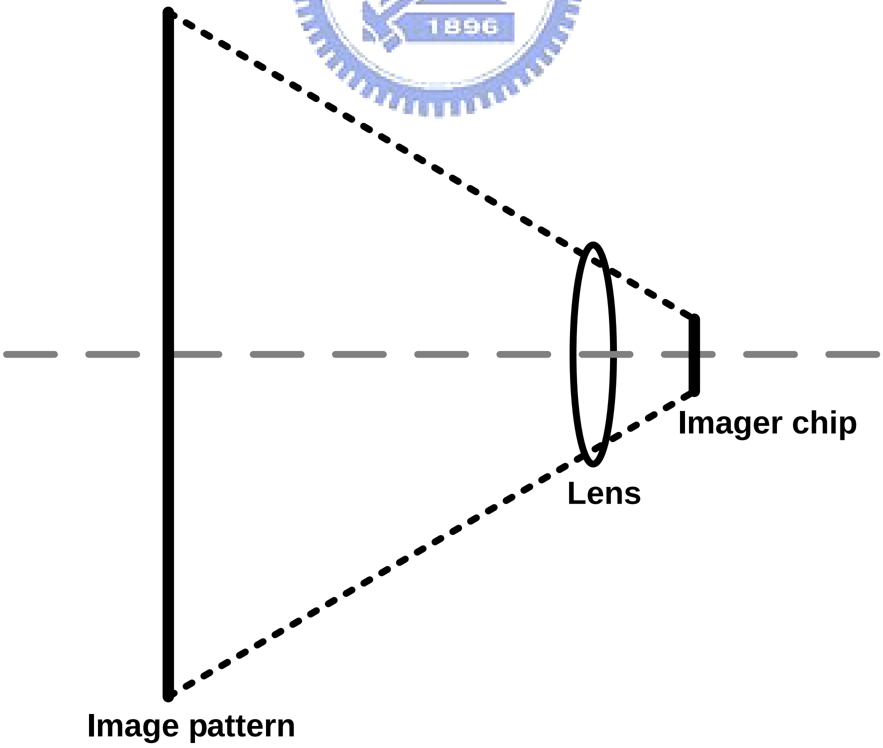
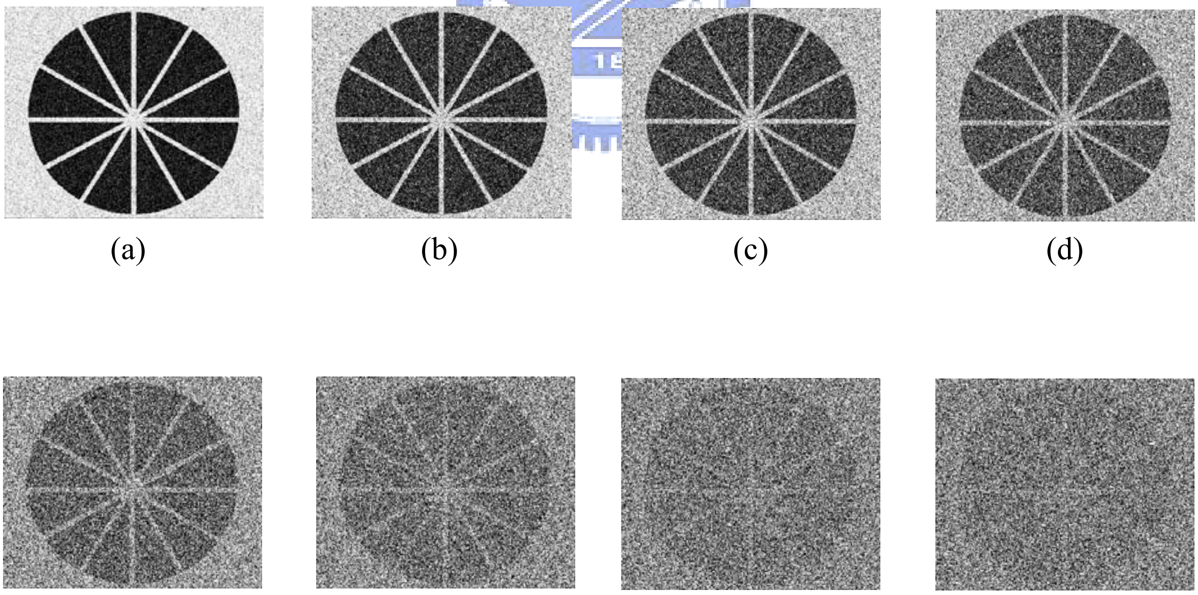


Fig. 4.13 The measurement setup of image pattern, lens, and imager chip.

(a) (b)

Fig. 4.14 (a) Original image and (b) grayscale image captured by the test chip under the white light intensity of 24 lux and Vcom of 1.79 V.



(a) (b) (c) (d)

(e) (f) (g) (h)

Fig. 4.15 Image captured by the test chip under the white light intensity of 24 lux and Vcom of (a) 1.79 V, (b) 1.75 V, (c) 1.70 V, (d) 1.65 V, (e) 1.60 V, (f) 1.55 V, (g) 1.50 V, and (h) 1.45 V.

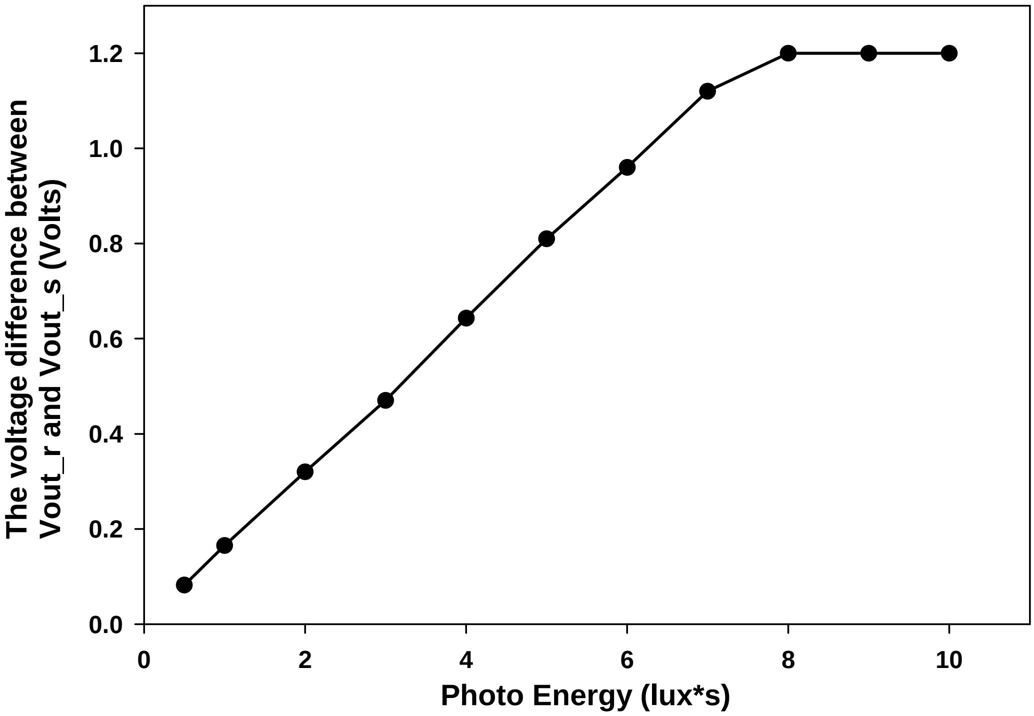


Fig. 4.16 Photo-sensitivity of PAPS CMOS imager.

CHAPTER 5

OPTIMAL DESIGN OF CMOS PSEUDO ACTIVE PIXEL SENSOR (PAPS) STRUCTURE FOR LOW-DARK-CURRENT AND LARGE-ARRAY-SIZE IMAGER APPLICATIONS

5.1 INTRODUCTION

It is the aim of this chapter to optimize the design of the structure of PAPS for the large-array-size CMOS imagers with low dark current. In the proposed optimal PAPS (OPAPS) structure, a buffer circuit called the zero-biased-buffer direct injection (ZBBDI) is shared by limited number of pixels to keep the photodiodes at zero or near zero bias and readout the selected pixel current [102]. Then the integration of readout current is performed by using an APS-like circuit. A new factor called the photocurrent-to-dark-current ratio per pixel area (PDRPA) is defined and optimized for the OPAPS structure. In the OPAPS design, both column sampling circuit and output correlated double sampling (CDS) circuit are used to reduce fixed pattern noise, clock feedthrough noise, and the noise from the effect of channel charge injection. The experimental results successfully verified the function of the proposed OPAPS structure and its performance.

In Section 5.2, the new structure of the proposed optimal PAPS (OPAPS) is described and the principles to decrease dark current and optimize the factor of PDRPA are presented. In Section 5.3, chip architecture and simulation results are described. In Section 5.4, chip layout and experimental results are presented and analyzed. Finally, the summary is given in Section 5.5.

5.2 OPTIMAL PSEUDO ACTIVE PIXEL SENSOR (OPAPS)

The general structure of the proposed optimal pseudo active pixel sensor (OPAPS) with P+/N-well photodiode is shown in Fig. 5.1 where one zero-biased buffer is shared by N pixels and each pixel has a pixel select switch device Mri where i = 1, 2, … , N. The gate of Mri is connected to the pixel select signal Ri. Moreover, the cathode of photodiode is connected to the pixel bias voltage of 1.8 V whereas the anode is connected to the shared zero-biased-buffer through the pixel select switch Mri. The inverting input of a gain stage G1 with the gain A is connected to the pixel bus of node D in Fig. 5.1 and its noninverting input is connected to the bias voltage Vcom. The output of the gain stage is connected to the gate of Min as a common-gate input stage. In the OPAPS circuit, the gain stage is implemented by a single CMOS differential pair to reduce the chip area.

The use of shared zero-biased-buffer in the OPAPS structure is the same as the buffer-direct-injection (BDI) [95], [96] readout structure. Through the shared zero-biased-buffer, the bias of pixel bus is controlled by the input voltage Vcom of the gain stage G1. The value of Vcom is set to 1.8 V by a low-noise constant voltage source to maintain the voltage of pixel bus at 1.8 V or near 1.8 V. Thus the effective voltage drop across the photodiode is zero or near zero when the pixel select switch of Mri is on.

The MOSFET of Mrst and the parasitic capacitor Cp are used to integrate the photocurrent at the node C of Fig. 5.1. Moreover, the gate control signal of Reset is used to reset the voltage of node C at zero voltage. The source follower, composed of

Mp1, Mrsel, and Mp2 is used as a buffer to transfer the voltage at the node C to the column sampling stage without interference. The gate control signal Rselj where j = 1, 2, … , K is used as the row selection. The gate of Mp2 is connected to the biased signal Vb1.

The interconnections of pixels, shared zero-biased-buffers, and column sampling stages in the OPAPS CMOS imager are shown in Fig. 5.2. The shared zero-biased-buffers are contained in the entire sensor array as shown in Fig. 5.2. The N pixels connected to the same shared-zero-biased-buffer and controlled by the pixel select switch Ri where i = 1, 2, … , N in one set of OPAPS circuit are put in the same column. K sets of OPAPS circuit controlled by the set select switch Rselj where j = 1, 2 … , K are also put in the same column. Thus the total number of pixels in the same column of the OPAPS CMOS imager are equal to NK. When both pixel select switch Ri and set select switch of Rselj are on, the image information of pixels in the ith row at the jth set of the OPAPS circuit in all columns are readout to the column sampling stage simultaneously. With both the pixel select switch Ri on and set select switches of Rsel1 to RselK on sequentially, 1/N frames of image information are transferred to the column sampling stage. Then the pixel select switch Ri is set to off and the next pixel select switch Ri+1 is on to transfer another 1/N frames of image information to the column sampling stage. The readout of the total image is completed after the N transformations of 1/N frames.

In additional to maintain the stable bias at the node D of Fig. 5.1, the input impedance seen from the node D is decreased by a factor of A due to the negative-feedback structure. The injection current from the pixel is mainly drained toward the node D due to the low input impedance. The current injection efficiency of the OPAPS readout structure is expressed as [97]

$$\eta(s) = \frac{(1+A)g_m Ro}{1+(1+A)g_m Ro}\left(\frac{1}{1+s/2\pi f_{BW}}\right) \tag{5.1}$$

$$f_{BW} = \frac{1+(1+A)g_m Ro}{2\pi Ro C_T} \tag{5.2}$$

where A is the gain of the buffer, g_m is the transconductance of Min, C_T is the capacitance at the node D and Ro is the output resistance of Mri. From (5.1), the current injection efficiency is increased by the gain of the buffer. In this design, the gain of A is about 100, which makes the injection efficiency close to 1.

In order to decrease the pixel area and reduce power dissipation, the use of MOSFETs in the pixel must be minimized. In addition, the power consumption of the shared zero-biased-buffer often becomes intolerable in the large-array-size CMOS imager. To solve the above problems, the same technique in the shared-buffer direct injection (SBDI) [98] is used. Thus the gain stage in the OPAPS circuit is composed of only one half of the differential pair [98]. The circuit diagram of the gain stage is shown in Fig. 5.3. The device parameters in the circuit diagram of the gain stage are given in Table 5.1. The additional power consumption of the gain stage can be reduced by proper design of the gain stage with low bias current. The effective total device number in the OPAPS circuit of Fig. 5.1 is (N+7) and one pixel is composed of only (1+7/N) MOSFETs.

The OPAPS circuit can be modified for the applications to the N+/P-substrate photodiode which has lower dark current and higher quantum efficiency. The modified OPAPS circuit for the N+/P-substrate photodiode is shown in Fig. 5.4 where an extra NMOS device Min is added. In Fig. 5.4, the modified OPAPS circuit is composed of the buffer-direct-injection (BDI) [95], [96] readout structure, the PMOS transistor Mrst as the reset switch, the APS-like structure with the NMOS source follower Mn1, Mrel, and Mn2, and a parasitic capacitor Cp. The value of Vcom is set to be slightly larger than the threshold voltage Vtn of Min. Thus the bias at the node D is equal to near zero voltage. The photodiode is biased at zero or near zero voltage when the pixel select switch of Mri is on. The impedance seen from the node D to Vdd is increased by $\frac{1}{g_{min}}$ where g_{min} is the transconductance of Min. To avoid the degraded injection efficiency, the channel geometric ratio W/L of Min should be large enough to increase g_{min}.

In the N-well CMOS technology, the P+/N-well pn junction is used as the photodiode. From the measurement results, it is found that the ratio of the photocurrent I_p to the dark current I_d under the reverse bias of 0 V is much larger than that under the reverse bias of 3 V [92]. Generally, the p-n junction photodiode has the characteristic as [92]

$$\left.\frac{I_p}{I_d}\right|_{|V_R|=0} > \left.\frac{I_p}{I_d}\right|_{|V_R|>0} \tag{5.3}$$

Thus, biasing the photodiode at zero or near zero voltage can achieve lower dark current, lower shot noise [86], and higher ratio of the photocurrent to the dark current as compared with that at higher reverse-biased voltage.

From the above results, it is shown that both photodiode and all the parasitic pn junctions in the pixel select switch must be operated under the reverse bias of 0 V to effectively reduce the dark current. Thus the voltage difference between the cathode of the photodiode and the node D of Fig. 5.1 is operated at 0 V in the proposed OPAPS structure in order to maintain the zero bias of both photodiode and parasitic pn junctions as shown in Fig. 5.1. When the pixel select switch of Mri is on, the voltage at the source of Mri is the same as that of node D which is 1.8 V. The photodiode, the parasitic pn junction between the source and substrate of Mri, and the parasitic pn junction between the drain and substrate of Mri are all operated under the reverse-biased voltage of 0 V. The photocurrent is then delivered to the node C for charge integration while both the dark current of the photodiode and the leakage current of the parasitic pn junctions are decreased to near 0 A.

When the pixel select switch of Mri is turned off by setting the signal of ri at Vdd, the diagram of pixel circuit in OPAPS is shown in Fig. 5.5. In Fig. 5.5, the source of Mri, N-well, and the drain of Mri form the parasitic lateral pnp BJT device Q1 with base and collector connected to 1.8 V and pixel bus, respectively, and emitter connected to node A. Moreover, the source of Mri, N-well, and P-substrate form the parasitic vertical pnp BJT device Q2 with the P-substrate collector connected to ground. Under incident light, the photodiode is forward-biased with the voltage drop equal to V_F and is operated as a solar cell. With V_F as the forward substrate bias between source and body of Mri, the threshold voltage Vtp of Mri is decreased due to the body effect. But the row select switch device Mri is still kept off because the voltage at the node A which is $1.8+V_F$, is smaller than Vdd+Vtp. However, the collector current I_{C1} of Q1 flows into the pixel bus as the dark current. As shown in Fig. 5.5, the current of I_F in the photodiode is equal to the sum of the emitter current I_{E1} of Q1 and I_{E2} of Q2. Thus we have

$$I_F = I_{p1} - I_{SP}(e^{\frac{V_F}{V_T}} - 1) = I_{E1} + I_{E2} = I_{S1}(e^{\frac{V_F}{V_T}} - 1) + I_{S2}(e^{\frac{V_F}{V_T}} - 1) \qquad (5.4)$$

where I_{SP}, I_{S1}, and I_{S2} are the reverse saturation current of photodiode, parasitic lateral BJT device Q1, and parasitic vertical BJT device Q2, I_{p1} represents the photocurrent when the photodiode is biased at 0 V, and V_T is the voltage equivalent of temperature. From (5.4), the total equivalent dark current I_{TED} from the parasitic BJT device Q1 flowing into the pixel bus can be expressed as

$$I_{TED} = (N-1)I_{C1} = (N-1)\alpha I_{E1} = (N-1)\alpha I_{p1}\frac{I_{S1}}{I_{SP} + I_{S1} + I_{S2}} = 2.107 \times 10^{-5} \times (N-1)I_{p1}$$

(5.5)

where N is the number of pixels connected to the same pixel bus and α is the common-base current gain of Q1.

The values of I_{SP}, I_{S1}, I_{S2}, and α in the proposed OPAPS CMOS imager with 0.25 μm CMOS technology and channel width(length) of Mri are given in Table 5.2. From (5.5), the ratio of I_{p1}/I_{TED} is larger than that of the APS CMOS imager if N is smaller than 2000. Thus the dark current contributed by the current I_{TED} in the proposed OPAPS CMOS imager is smaller than the dark current of the APS CMOS imager if N is smaller than 2000. Consequently, the proposed OPAPS CMOS imager can be applied to the large-array-size imager with the dark current contributed by I_{TED} in (5.5) smaller than the dark current of the APS CMOS imager.

The photocurrent generated from the selected pixel is integrated on the node C of Fig. 5.1 after the reset operation with Mrst off. After the integration, the row select switch signal Rsel is on and the integrated photo-signal voltage is transferred to the photo-signal sampling circuit in the column sampling stage through the source follower. At the end of integration, the reset switch Mrst is turned on and the reset-signal voltage at the node C is also transferred to the reset-signal sampling circuit in the column sampling stage to perform the operation of double delta sampling (DDS) [92].

In the OPAPS structure, as the number of pixels connected with the same shared-zero-biased-buffer is increased, the effective pixel area (EPA) is decreased if the photodiode area is kept constant. However, the photocurrent-to-dark-current ratio (PDR) is decreased because the dark currents from the deselected pixels are increased. Thus the optimal number of pixels connected with the shared zero-biased-buffer can be determined from the factor of PDR per pixel area (PDRPA). The effective pixel area in the OPAPS structure is expressed as

$$\mathrm{EPA} = \mathrm{Apsw} + \mathrm{Apd} + \mathrm{Asp} + \frac{\mathrm{Abuf}}{\mathrm{N}} \tag{5.6}$$

where A_{psw} is the area of pixel select switch, A_{pd} is the area of photodiode, A_{sp} is the average area of devices spacing and signal routing channel in a pixel, and A_{buf} is the area of the shared zero-biased-buffer.

The PDR at the node D of Fig. 5.1 is expressed as

$$\mathrm{PDR} = \frac{I_{p1}A_{pd}}{I_{d1}(A_{pd} + C_R A_{psw,S} + C_R N A_{psw,D}) + I_{TED}A_{pd}} \qquad (5.7)$$

where I_{p1} and I_{d1} are the photocurrent and dark current in photodiode, respectively, when it is biased at zero voltage, I_{TED} is the total equivalent dark current from the parasitic BJT device Q1 in Fig. 5.5 flowing into node D of Fig. 5.1, C_R is the dark-current ratio of the parasitic pn junctions between the source/drain and substrate of Mri in Fig. 5.1 and photodiode under the same area, $A_{psw,S}$ is the source area of Mri, and $A_{psw,D}$ is the drain area of Mri.

All the values of these parameters in 0.25 μm CMOS technology are listed in Table 5.3 where the photodiode area is 28.04 μm^2 which is nearly equal to that in a conventional APS pixels of 8.5 μm × 8.5 μm. Using the parameter values, the factor of PDRPA can be rewritten as

$$\mathrm{PDRPA} = \frac{\mathrm{PDR}}{\mathrm{EPA}} = \frac{280400}{(50.94 + \frac{65.22}{N})(64.54 + 5.91N)} \qquad (5.8)$$

The calculated values of the factor PDRPA in (5.8) versus N is shown in Fig. 5.5. As shown in Fig. 5.6, the factor of PDRPA has the maximum value when the value of N is equal to 4. Thus the optimized number of pixels connected with the shared zero-biased-buffer in the OPAPS structure is equal to 4 and the optimized factor of PDRPA is equal to 47.29 μm^{-2}. Under this circumstance, the factor of PDR in the OPAPS structure is equal to 3179.86 which is much larger than that of APS [92].

For different CMOS technologies, the optimal N value may not be equal to 4. It can be calculated by using (5.6) and (5.7) to generate the maximum value of PDRPA.

5.3 CHIP ARCHITECTURE AND SIMULATION RESULTS

The block diagram of the proposed optimal pseudo active pixel sensor (OPAPS) CMOS imager is shown in Fig. 5.7 where N=4, i.e. four pixels share the same zero-biased-buffer. The 352 x 288 (CIF) format of CMOS imager is taken as an example to realize the proposed OPAPS structure. As shown in Fig. 5.7, the proposed OPAPS circuit is composed of four pixels and one shared zero-biased-buffer. The row decoder and row counter on the left side of pixel array are used to generate the control signals to the row switches. In addition, the column decoder and column counter on the top side of pixel array are used to generate the control signals for the reset operation and those to the column switches, the output correlated double sampling (CDS) circuit, and the row counter. Each column of the pixel array has a column sampling circuit to reduce fixed pattern noise. The column readout circuit generates two analog output voltages. One is the signal proportional to the gray scale intensity of the image whereas the other is the signal proportional to the reset voltage at the integration capacitor. The output CDS circuit is used to drive the external loads and perform the CDS operation [92].

The image information is transformed as the photocurrent in the pixel array by using the photodiode. The photocurrent is delivered to the shared zero-biased-buffer and converted into a voltage signal proportional to the intensity of image after the current integration at node C of Fig. 5.1. The photo-signal and reset-signal are used for the operation of double delta sampling (DDS) [92]. The two signals generated in the output CDS circuit are delivered to the programmable gain amplifier (PGA), A/D converter, and display system outside the chip to generate the raw image [92].

The major operational timing diagram of the proposed OPAPS circuit is shown in Fig. 5.8. At first, the pixel select switch of r1 is low and the photocurrent of this pixel is integrated on the node C of Fig. 5.1 after the reset operation at the node C. After the photocurrent integration, the row select switches of Rsel1 to Rsel72 are on sequentially to transfer 1/4 frames of image information to the column sampling stage. Then the pixel select switch of r1 is switched off and the next pixel select switch of r2 is switched on to transfer another 1/4 frames of image information to column sampling stage. The readout of the total image is completed after the four transformations of 1/4 frames. The available integration time is divided by four for a fixed frame rate.

The HSPICE simulation results of the voltage at node C of the OPAPS circuit in Fig. 5.1 and the voltage difference between Vout_r and Vout_s of the output CDS circuit in Fig. 5.7 for the input photocurrent from 200 fA to 800 fA under the frame rate of 30 frames/sec are shown in Figs. 5.9(a) and 5.9(b), respectively. As may be seen from Fig. 5.9, the linearity of the readout circuit is 92% and the maximum output swing is equal to 0.98 V.

5.4 EXPERIMENTAL RESULTS

In the experimental chip, a 352 x 288 (CIF) CMOS imager based on the proposed OPAPS structure is designed and fabricated by using 0.25 μm 1P5M N-well CMOS process. The pixel size is 8.2 μm x 8.2 μm. The layout diagram of eight pixels in two OPAPS circuits is shown in Fig. 5.10 where the source of pixel select transistor is connected directly to the P+ diffusion of the photodiode without contacts to increase sensor area and fill factor. The corner of the photodiode is clipped 135° to reduce the effect of leakage current at the right angle. The fill factor in the OPAPS pixel is 42%. The fill factor can be designed larger by moving the N-well contact outside the pixel.

To obtain the uniform characteristics of the sensor array, two layers of dummy photodiodes are added around the active sensor array. The P+ regions of the dummy photodiodes are connected to N-well to maintain zero bias such as the photodiodes in the active sensor array. The dummy photodiodes are completely shielded by metal5. In addition, double guard rings are inserted around the sensor cell array to reduce substrate coupling of the digital switching noise.

The Analog-to-digital converter is not implemented to simplify the design in the test chip. The photograph of the fabricated imager chip is shown in Fig. 5.11 where the area except the regions of sensor and capacitor are covered by metal5 from light shielding. The total chip size is 3630 μm x 3390 μm.

To test the fabricated CIF OPAPS CMOS imager chip, a data acquisition card with the function of A/D converter is utilized to capture the image. The measurement setup of image pattern, lens, and imager chip is shown in Fig. 5.12. The original image and the measured grayscale image captured by the fabricated CIF OPAPS CMOS imager chip under Vcom of 1.79 V is shown in Fig. 5.13. Moreover, the measured raw images captured by the fabricated CIF OPAPS CMOS imager chip under different values of Vcom are shown in Figs. 5.14(a)-(d). When the value of Vcom is 1.75 V, the image quality in Fig. 5.14(a) is good and no observable fixed pattern noise (FPN) is presented. With the decrease of Vcom from 1.65 V to 1.35 V as shown in Figs. 5.14(b)-(d), the image quality is degraded by the effect of leakage current in the parasitic pn junctions of the deselected row switches.

The images captured by the fabricated CIF pseudo-active-pixel-sensor (PAPS) CMOS imager chip [92] under different values of Vcom are also shown in Figs. 5.14(e)-(h). As compared the images of Figs. 5.14(a)-(d) to the corresponding images of Figs. 5.14(e)-(h), respectively, it can be realized that the OPAPS structure has smaller dark current than that of PAPS structure because the leakage current from the parasitic pn junctions of deselected pixels in the OPAPS structure is smaller than that in the PAPS structure. Thus the function of the proposed OPAPS CMOS imager is successfully verified. It can be used in the high-resolution applications by keeping the value of Vcom equal to 1.8 V or slightly smaller than 1.8 V.

The measurement results of the proposed CIF OPAPS CMOS imager with the value of Vcom equal to 1.79 V are summarized in Table 5.4 where the corresponding measurement results of the PAPS [92] and APS [101] CMOS imager are also given for comparisons. The dark current in the OPAPS CMOS imager is equal to 82 pA/cm^2 which is smaller than that of the PAPS [92], APS [100], [101], and PPS CMOS imager. In addition, the optical dynamic range of 65dB in the OPAPS CMOS imager is larger than that of the APS [100], [101] and PPS CMOS imagers because the dark current in the OPAPS structure is the smallest.

The photo-sensitivity is shown in Fig. 5.15 and is equal to 0.25 V/lux·s after calculations. The photo-sensitivity in the OPAPS CMOS imager is smaller than that of the APS and PPS CMOS imagers due to the low quantum efficiency of P+/N-well photodiode. To achieve the same photo-sensitivity and quantum efficiency as that of the APS and PPS CMOS imagers, the OPAPS circuit can be modified for the applications to the N+/P-substrate photodiode as shown in Fig. 5.4. Fixed pattern noise (FPN) caused by device mismatch and process variation was evaluated using a dark image created by averaging 100 frames [100]. There are two sources of FPN, namely, pixel FPN, which is caused by mismatch in the pixel circuit, and column FPN, caused by mismatch in the column readout circuit [103]. The FPN in the OPAPS CMOS imager is 6.2 mV which is smaller than that of the APS CMOS imager with DDS circuits [103]. But the FPN in the OPAPS CMOS imager is slightly larger than that of the PAPS CMOS imager due to the larger pixel FPN in OPAPS CMOS imager.

This is because the shared zero-biased-buffers in the OPAPS CMOS imager are put in the sensor array and the mismatches among them increase the pixel FPN. In the PAPS CMOS imager, only one shared zero-biased-buffer is used per column and is put outside the sensor array. However, the FPN of both OPAPS and PAPS CMOS imagers is smaller than that of the APS CMOS imagers with DDS circuits [103]. The output swing of 0.9 V is smaller than that of simulation results because of the process variations in the threshold voltage of MOSFETs. The total power dissipation of the fabricated CMOS imager chip is equal to 30 mW under the power supply of 3.3 V. The power dissipation of OPAPS CMOS imager is larger than that of PAPS CMOS imager because more gain stages are used in OPAPS CMOS imager. Thus the proposed OPAPS CMOS imager can be used in low-dark-current and high-resolution imager applications by keeping the value of Vcom equal to 1.8 V or slightly smaller than 1.8 V.

5.5 SUMMARY

In this chapter, a pixel structure called the optimal pseudo active pixel sensor (OPAPS) structure, has been proposed and analyzed for the applications of CMOS imagers. In the OPAPS structure, the zero-biased buffer is shared by several pixels to increase fill factor, suppress dark current of photodiodes, and decrease the leakage current of parasitic pn junctions. The factor of photocurrent-to-dark-current ratio per pixel area (PDRPA) is defined and optimized in the OPAPS structure. It is found that one zero-biased-buffer shared by four pixels in 0.25 μm single-poly-five-level-metal (1P5M) N-well CMOS technology can achieve the maximum PDRPA factor and thus represents the best choice. The available integration time is divided by four for a fixed frame rate. The frame rate of OPAPS CMOS imager is smaller than that of APS

CMOS imager under the same integration time. In imagers with the OPAPS structure, the double delta sampling (DDS) circuits are also used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. An experimental chip of CIF OPAPS CMOS imager is designed, fabricated, and measured. The measurement results have verified the performance of the proposed OPAPS structure.

It has been found from the experimental results that dark current of 82 pA/cm^2 and optical dynamic range of 65dB in the fabricated CIF OPAPS CMOS imager are superior than those of the APS and PPS CMOS imagers. The number of transistors in the pixel of the OPAPS CMOS imager is smaller than that of the APS CMOS imager. In addition, the optical dynamic range of the OPAPS CMOS imager is larger than that of the APS and PPS CMOS imagers. With the advantageous characteristics of low dark current, high dynamic range, and high fill factor, it is expected that the proposed OPAPS CMOS imager structure can be applied to the design of high-quality and large-array-size CMOS imagers.

Table 5.1 The device parameters in the circuit diagram of the gain stage

	Width/length
Mp1a	0.78 µm / 0.30 µm
Mp1b	0.78 µm / 0.30 µm
Mp2	0.60 µm / 0.65 µm
Mp3	0.60 µm / 0.65 µm
Mn1	0.58 µm / 0.90 µm
Mn2	0.58 µm / 0.90 µm

Table 5.2 The values of I_{SP}, I_{S1}, I_{S2}, α, and width/length of Mri

I_{SP}	1.97×10^{-17} A
I_{S1}	4.20×10-22 A
I_{S2}	3.02×10-20 A
α	0.99
width/length of Mrsel	0.5 µm / 0.35 µm

Table 5.3 The design parameters of Id1, Ip1, Abuf, Apsw, Apsw, D, Apsw, S, Apd, Asp, and C_R for 0.25µm 1P5M N-well CMOS process

Id1	0.13fA
Ip1	570fA
Abuf	65.22 μm^2
Apsw	3.6 μm^2
Apsw, D	0.5 μm^2
Apsw, S	0.25 μm^2
Apd	28.04 μm^2
Asp	19.30 μm^2
C_R	3.8

Table 5.4 The measurement results of the proposed OPAPS CMOS imager with the value of Vcom equal to 1.79 V and its comparisons with that of PAPS [92] and APS CMOS imagers [101]

Pixel Structure	OPAPS	PAPS [92]	APS [101]
Technology	0.25 µm 1P5M N-well CMOS	0.25 µm 1P5M N-well CMOS	0.35 µm 1P3M N-well CMOS
Power Supply	3.3 V	3.3 V	3.3 V
Output Swing	0.9 V	1.2 V	0.8 V (estimate)
Readout Speed	30 frames/sec	30 frames/sec	30 frames/sec
Linearity	87%	92%	80% (estimate)
Dark Current	82 pA/cm^2 (room temperature)	93 pA/cm^2 (room temperature)	370 pA/cm^2 (room temperature)
Optical Dynamic Range	65dB	72dB	53dB
Photo-sensitivity	0.25 V/lux·s	0.16 V/lux·s	0.52 V/lux·s
Fixed Pattern Noise (FPN)	6.2 mV	5.3 mV	8 ~ 24 mV (estimate)
Chip Size	3630 µm x 3390 µm	3110 µm x 2760 µm	5840 µm x 5010 µm
Pixel Area	8.2 µm x 8.2 µm	5.8 µm x 5.8 µm	7.4 µm x 7.4 µm
Array Size	352 x 288 (CIF)	352 x 288 (CIF)	640 x 480
Area of Pixel Array	2886.4 µm x 2361.6 µm	2041.6 µm x 1670.4 µm	4736 µm x 3552 µm
Fill Factor	42%	58%	25% ~ 40% (estimate)
Fill Factor / Pixel Area	0.00625 µm^{-2}	0.0172 µm^{-2}	0.00457 µm^{-2} ~ 0.0073 µm^{-2} (estimate)
Operating Temperature	25°C	25°C	25°C
Power Dissipation	30 mW	24 mW	31 mW

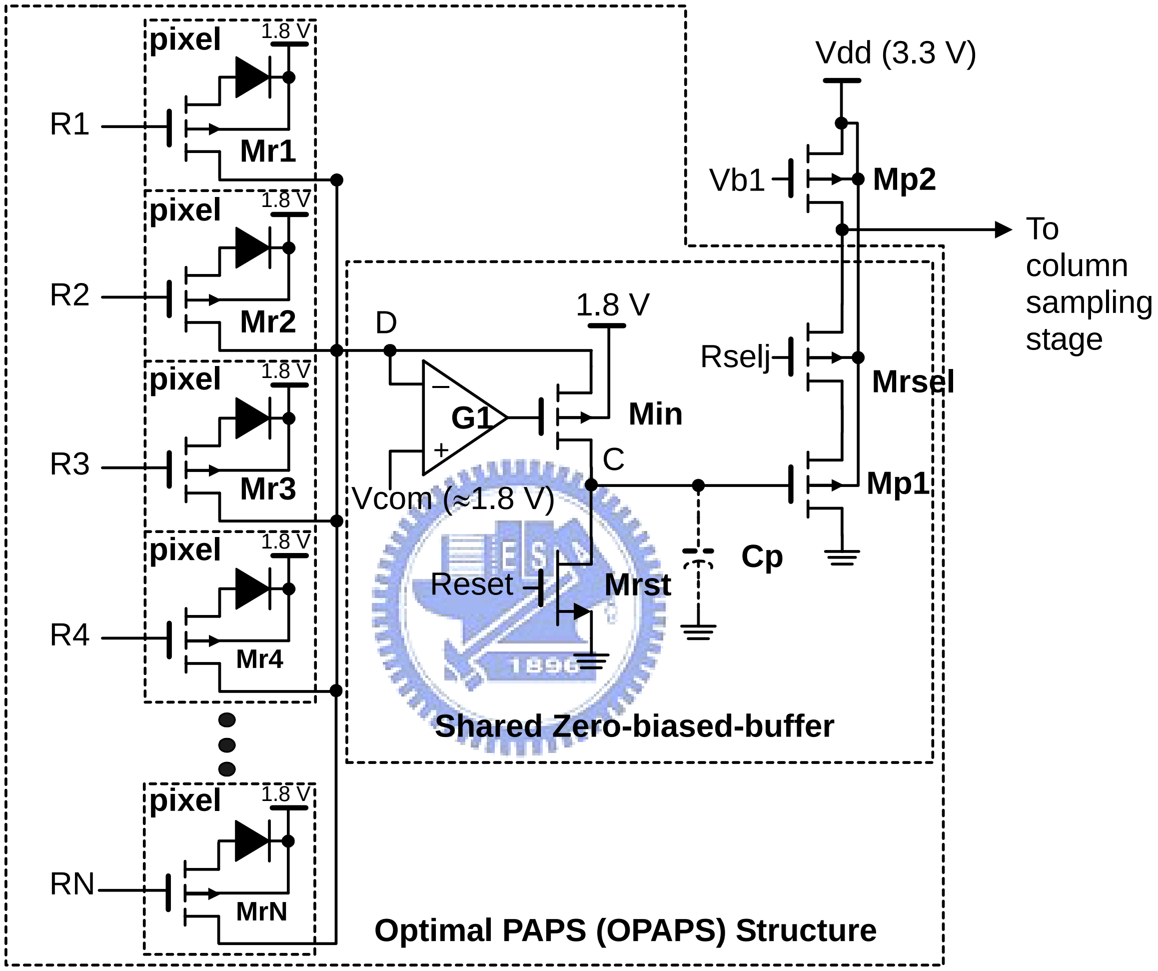


Fig. 5.1 The optimal pseudo active pixel sensor (OPAPS) circuit with P+/N-well photodiode.

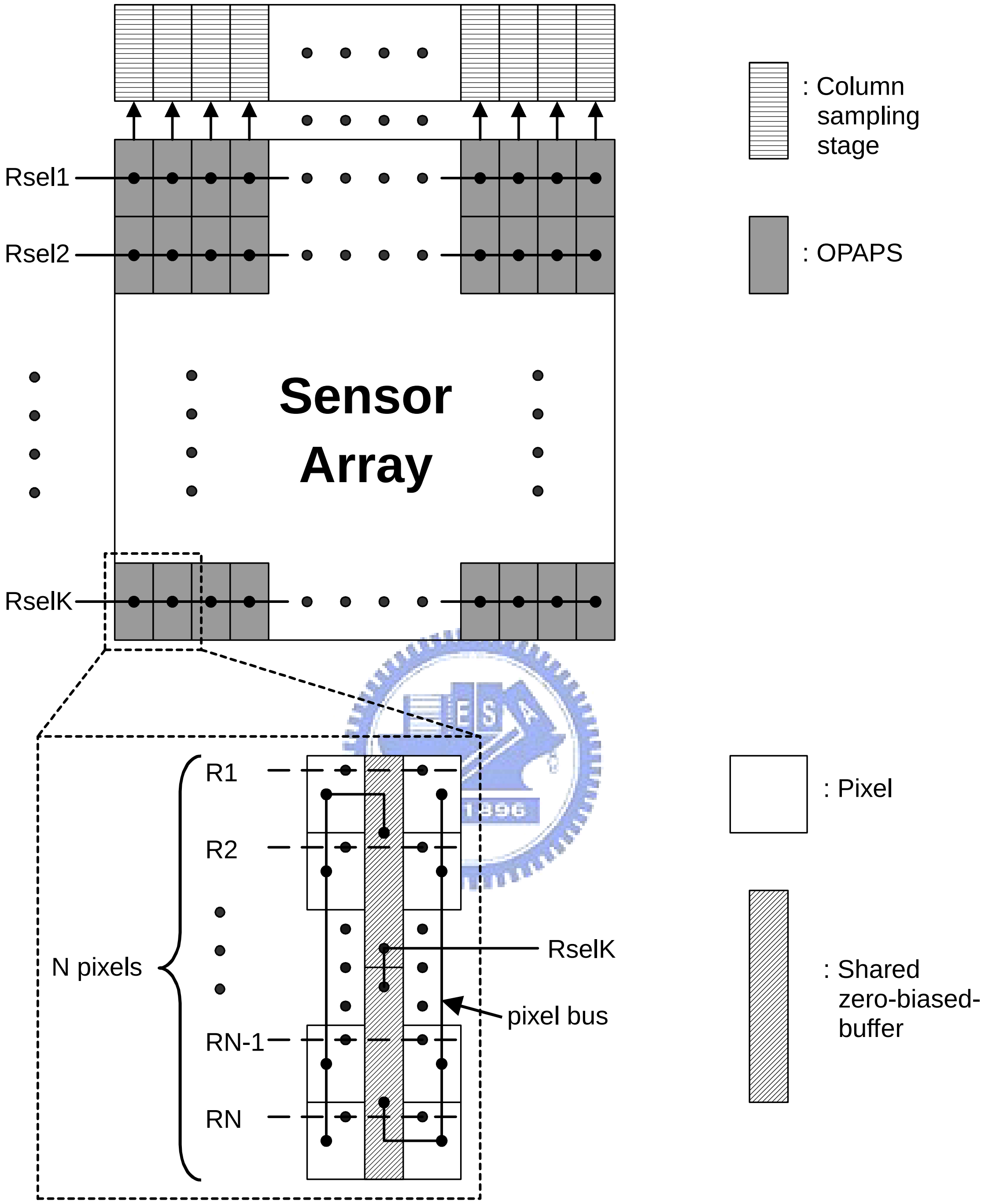


Fig. 5.2 Interconnections of pixels, shared zero-biased-buffers, and column sampling stages in the OPAPS CMOS imager.

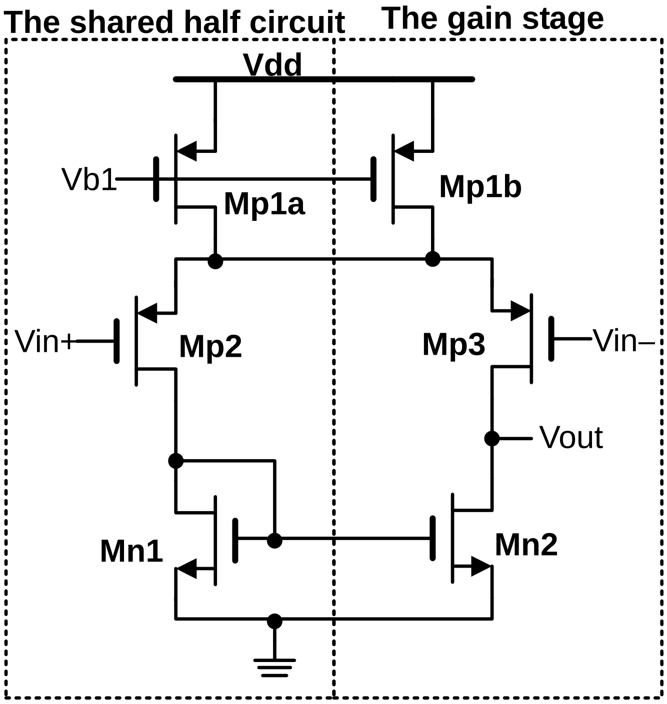


Fig. 5.3 The circuit diagram of the gain stage.

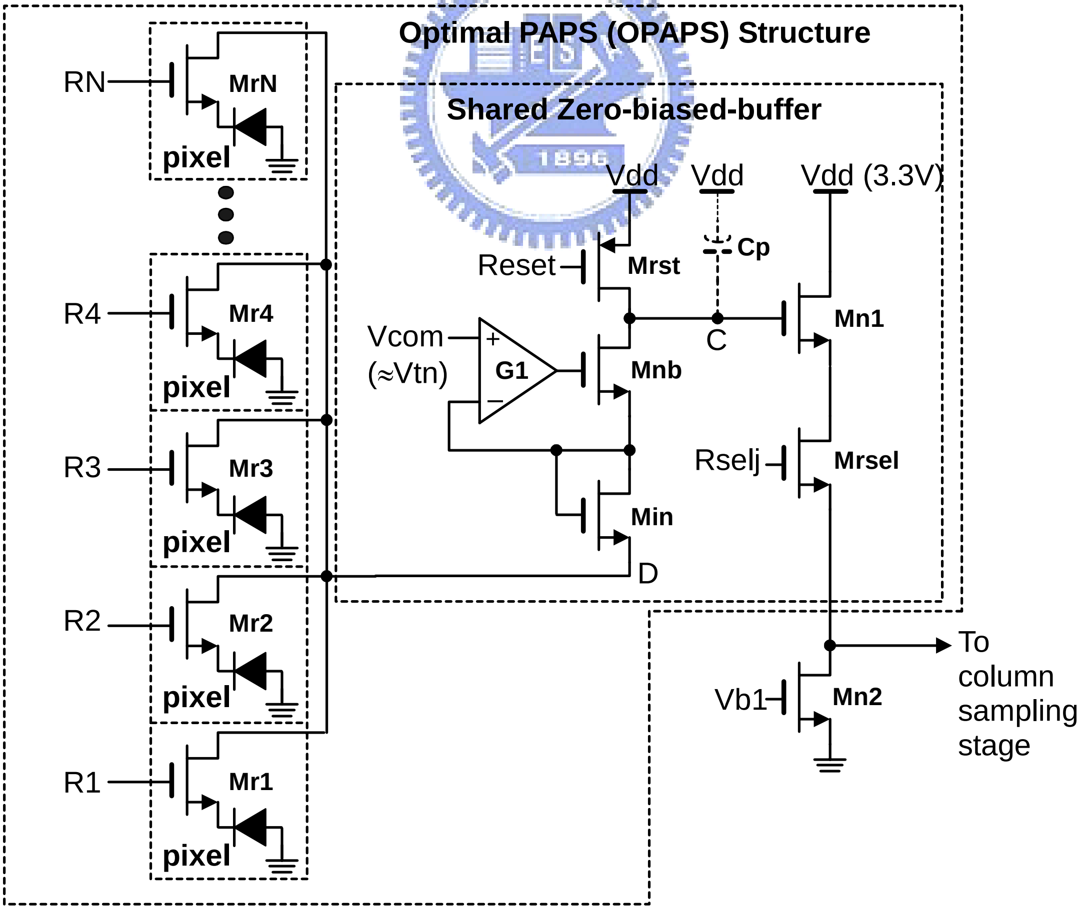


Fig. 5.4 The modified optimal pseudo active pixel sensor (OPAPS) circuit with N+/P-substrate photodiode.

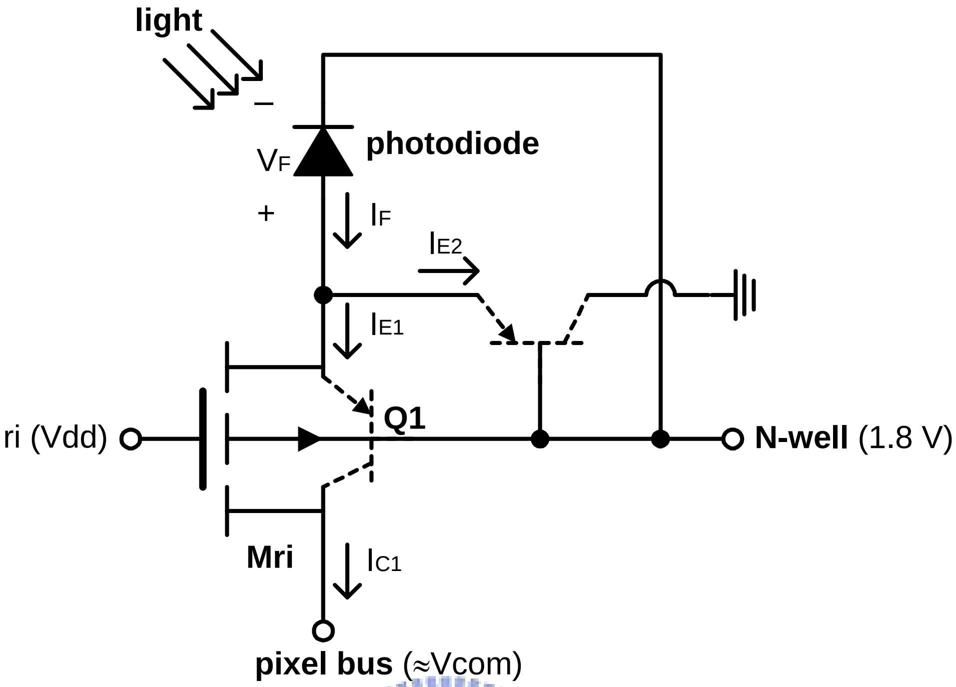


Fig. 5.5 The diagram of pixel circuit in OPAPS when the pixel select switch of Mri is off.

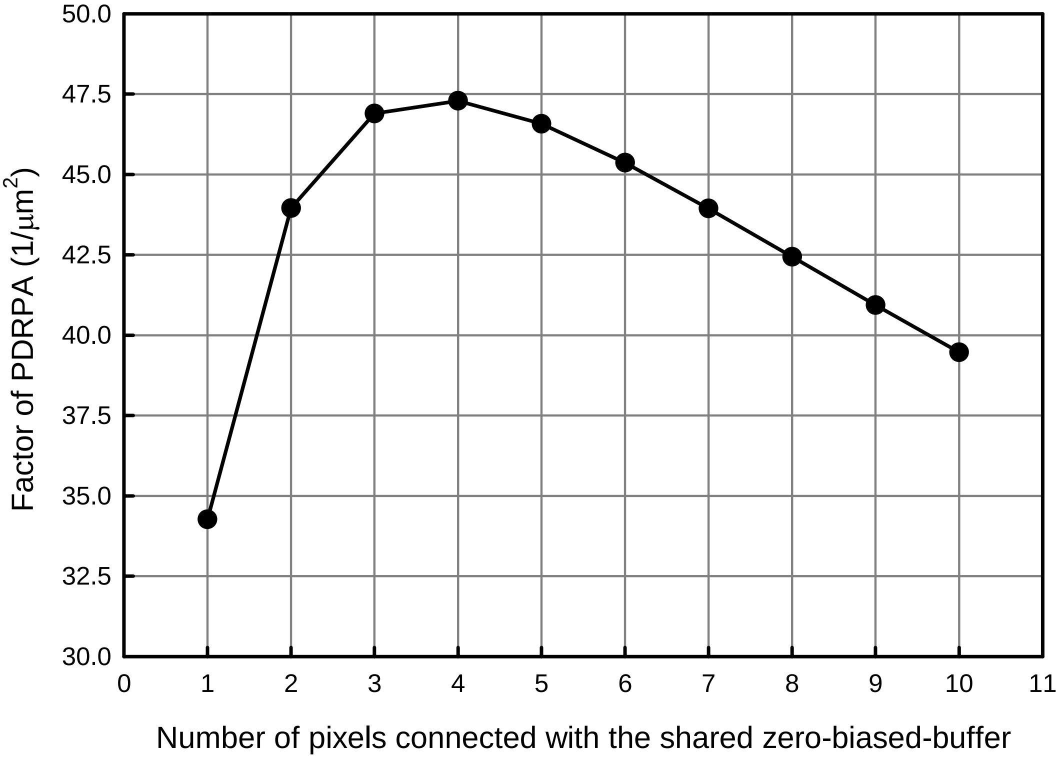


Fig. 5.6 The factor of PDRPA in the OPAPS circuit.

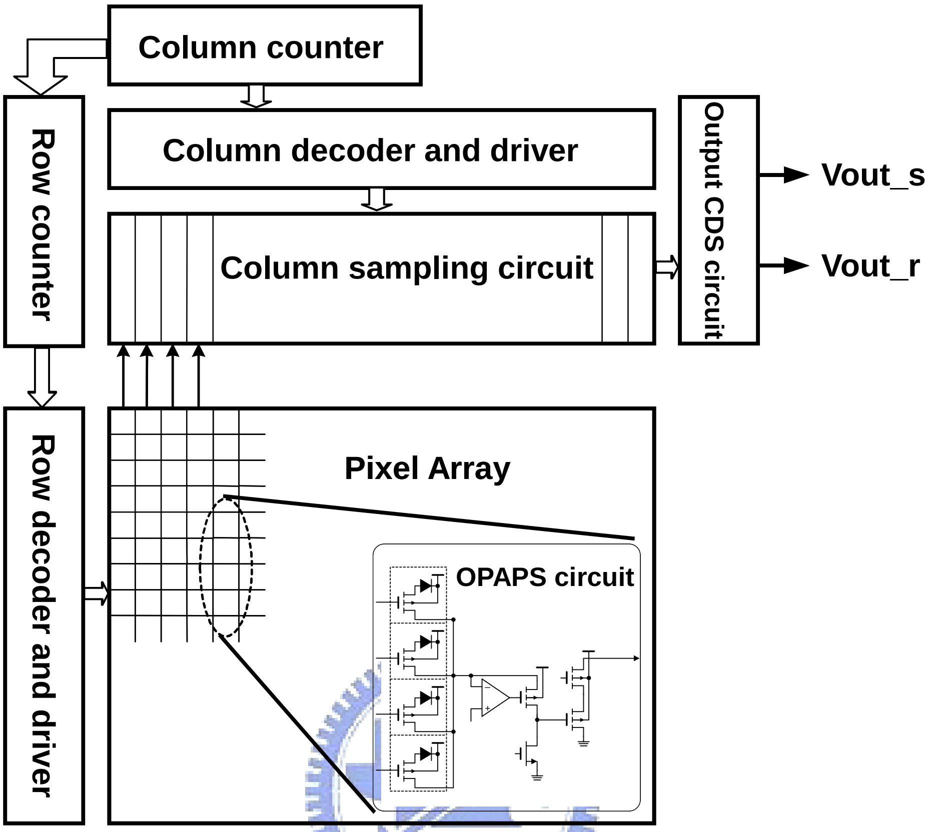


Fig. 5.7 Block diagram of the OPAPS CMOS imager.

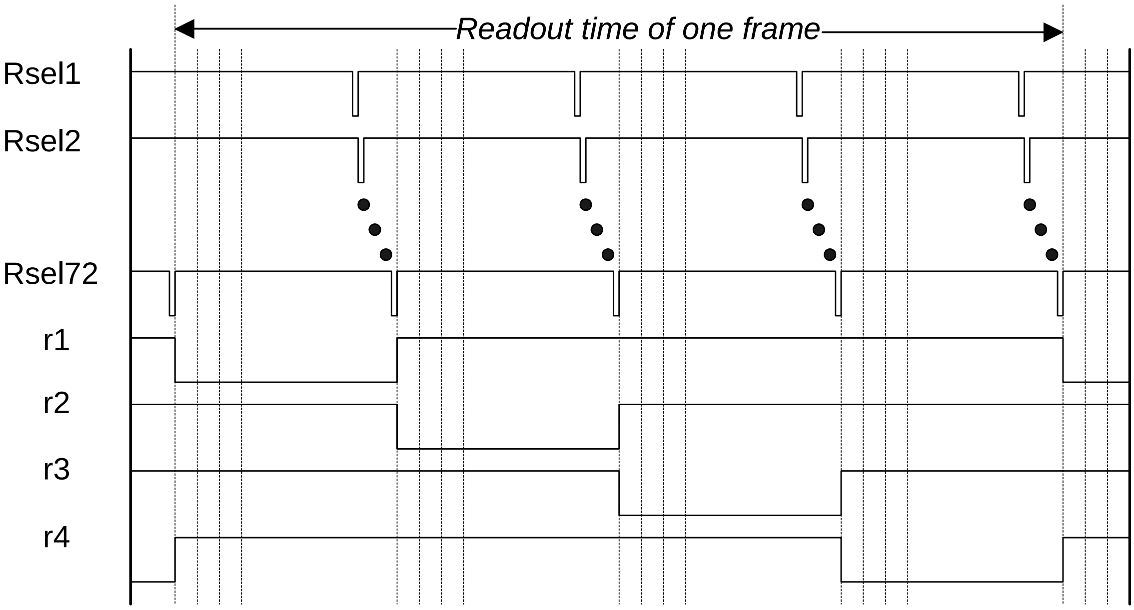
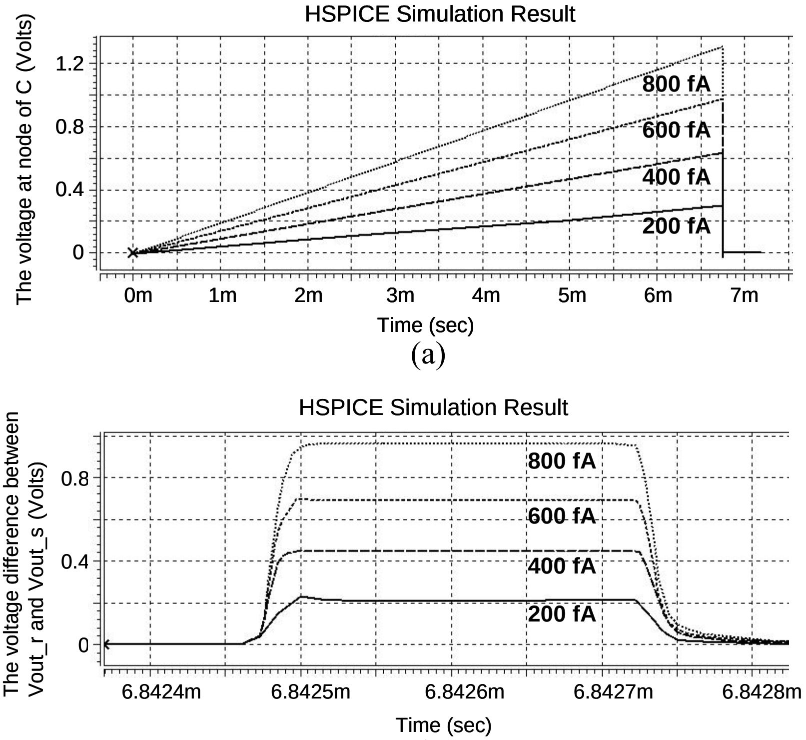


Fig. 5.8 The major timing diagram of the OPAPS circuit.



(a)

(b)

Fig. 5.9 HSPICE simulation results of (a) the voltage at node C of Fig. 5.1 and (b) the voltage difference between Vout_r and Vout_s of Fig. 5.6 for the input photocurrent from 200 fA to 800 fA.

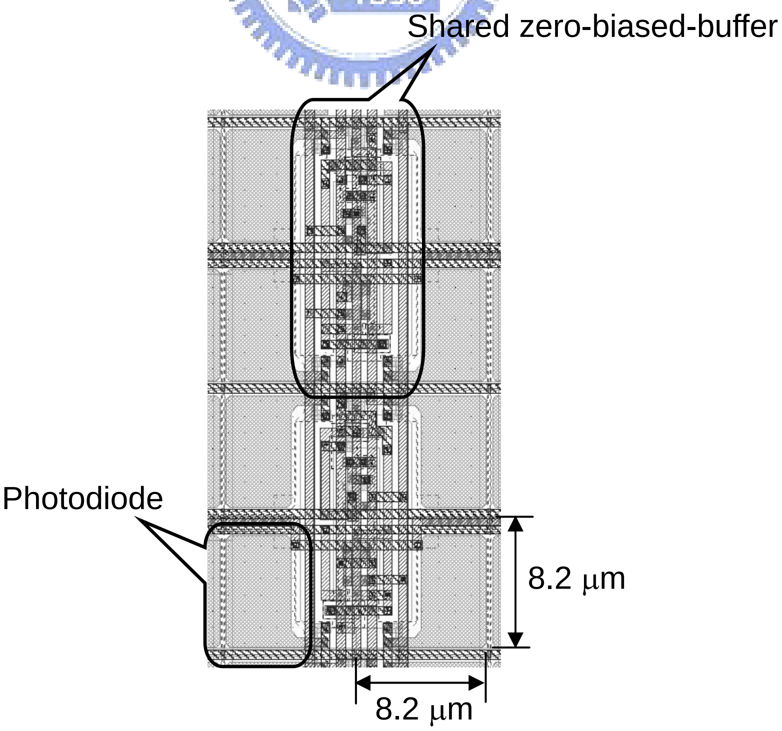


Fig. 5.10 The layout of eight pixels in the OPAPS CMOS imager chip.

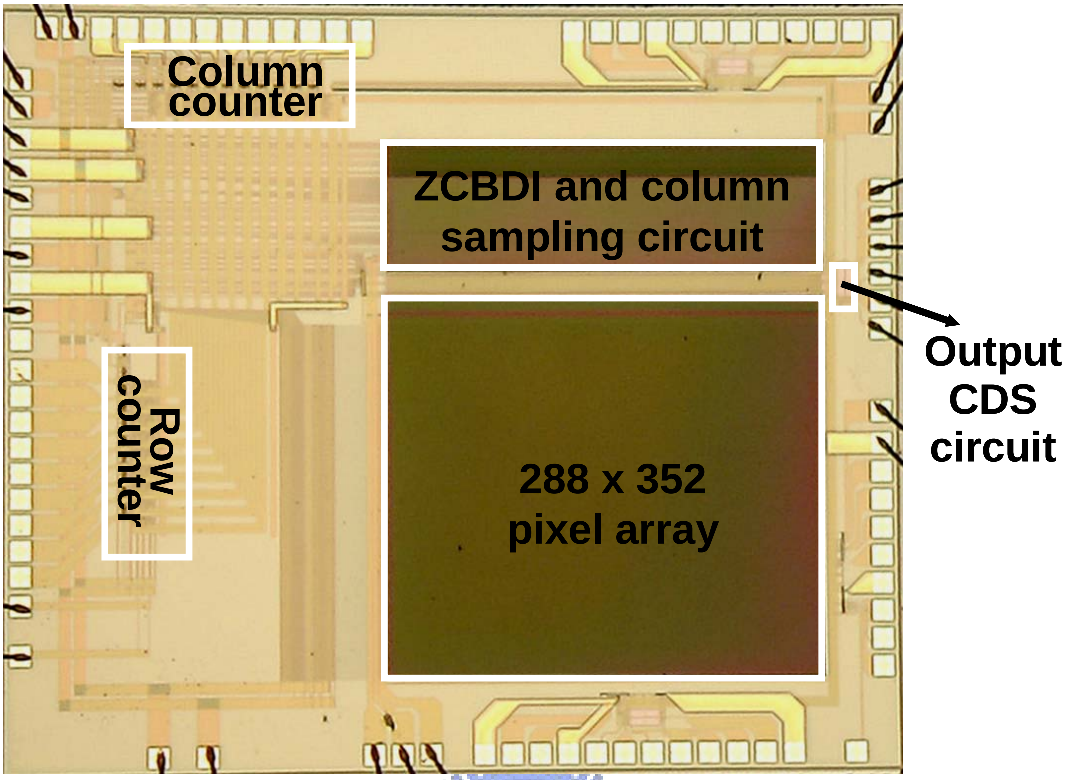


Fig. 5.11 Die photograph of the test chip.

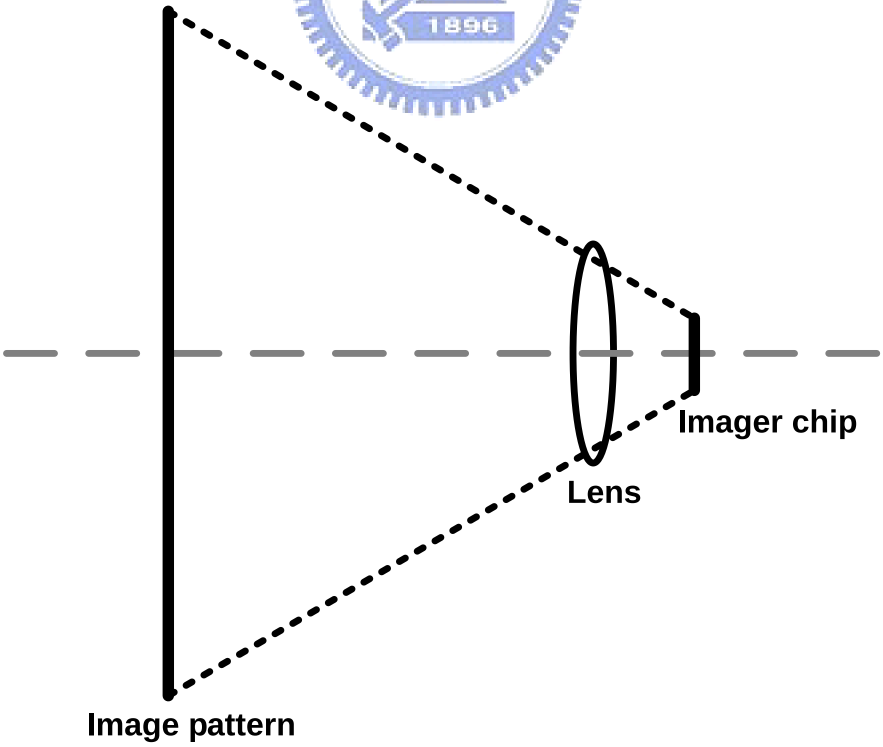
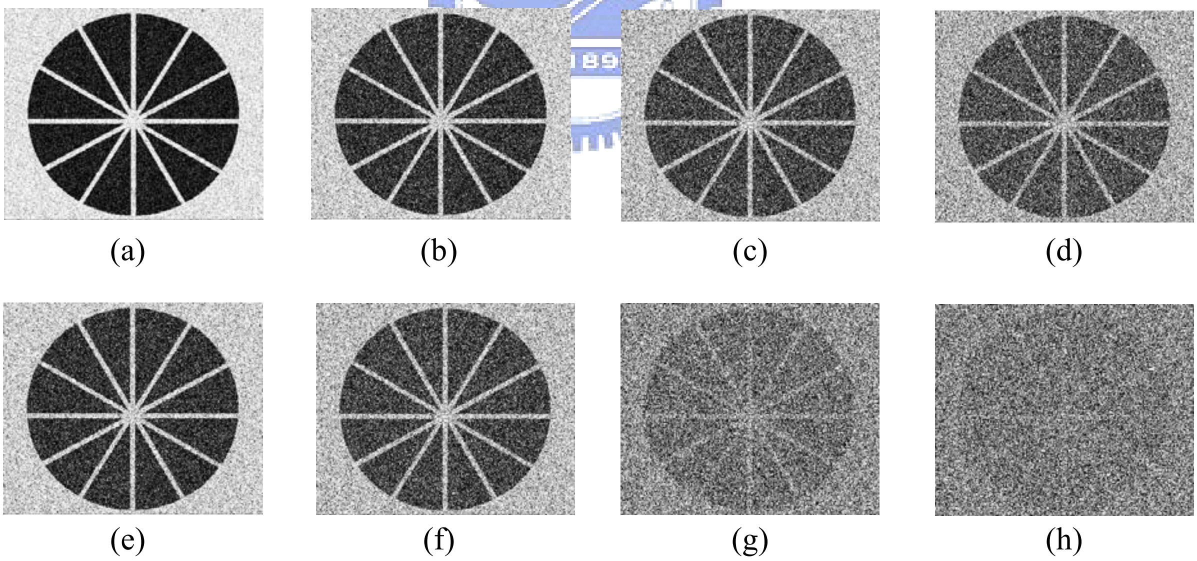


Fig. 5.12 The measurement setup of image pattern, lens, and imager chip.

(a) (b)

Fig. 5.13 (a) Original image and (b) grayscale image captured by the test chip under the white light intensity of 24 lux and Vcom of 1.79 V.



(a) (b) (c) (d)

(e) (f) (g) (h)

Fig. 5.14 Images captured by the test chip of OPAPS structure under the white light intensity of 24 lux and Vcom of (a) 1.75 V, (b) 1.65 V, (c) 1.50 V, and (d) 1.35 V and those captured by the test chip of PAPS structure under the white light intensity of 24 lux and Vcom of (e) 1.75 V, (f) 1.65 V, (g) 1.50 V, and (h) 1.35 V.

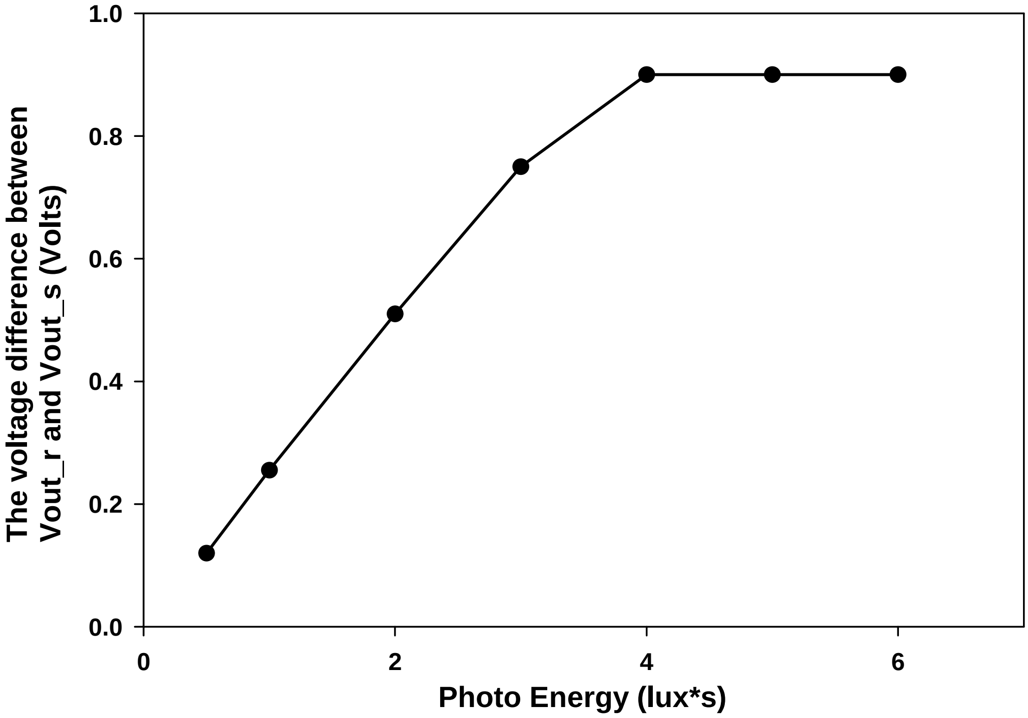


Fig. 5.15 Photo-sensitivity of OPAPS CMOS imager.

CHAPTER 6

CONCLUSIONS AND FUTURE WORKS

6.1 MAIN RESULTS OF THIS THESIS

In this thesis, new photodiode structures for CMOS active pixel sensor (APS) imager applications are proposed and analyzed. In addition, a new pixel structure for still CMOS imager applications and its optimization is also proposed and designed. Three experimental CMOS chips including two new photodiode structures, PAPS circuits, and OPAPS circuits have been designed, fabricated, and measured to verify the analysis results. Two new photodiode structures with the use of p-substrate and the SN– implant as the pn junction photodiode and applied in the 5 μm x 5 μm APS cell were fabricated by 0.35 μm single-poly-triple-metal (1P3M) 3.3 V N-well CMOS technology with LOCOS structure. The other two experimental CMOS imager chips, the pseudo active pixel sensor (PAPS) for the large-array-size still CMOS imagers with low dark current and high fill factor and the optimal PAPS (OPAPS) to achieve the maximum factor of photocurrent-to-dark-current ratio per pixel area (PDRPA), were fabricated by 0.25 μm single-poly-five-level-metal (1P5M) N-well CMOS technology.

In the design of new photodiode structures, two new photodiode structures with low dark current and high spectral response are proposed and analyzed. The p-substrate and the SN– implant are used as the pn junction photodiode in both new structures. Regions of the bird’s beak in the two proposed structures are embraced by either the SN– implant or the p-field implant and are kept away from the depletion region of the pn junction. The surface damage can be lowered by using the low doping concentration of the SN– implant. Thus, in the two new photodiode structures, the dark current generated in the regions of bird’s beak can be lowered and the increase of the dark current due to the effect of surface damage can be avoided. The spectral responses of the two structures can be improved by utilizing the shallow side diffusion and deep bottom diffusion of SN– to absorb the photons for light of short and long wavelengths, respectively.

It has been shown from the measurement results, the two proposed new photodiode structures applied in the 5 μm x 5 μm APS cell have lower dark currents of 30.6 mV/sec and 35.2 mV/sec at the reverse-biased voltage of 2 V and higher spectral response, as compared to the conventional structure and other photodiode structures. Thus the two new photodiode structures can be applied to the design of high-performance CMOS imagers with small pixel size, high resolution, low dark current, and high spectral response.

In the design of the new pixel structure for still CMOS imager application called the pseudo active pixel sensor (PAPS), the PPS-like pixel circuit, the APS-like column circuit, and the new readout structure called the zero-bias column buffer-direct-injection (ZCBDI) are used to reduce column leakage current, decrease pixel area, and increase fill factor. The gain loss in the source follower of NMOS devices can be avoided by using the mask of deep N-well to increase the output voltage dynamic range. The improved double delta sampling (DDS) circuits are also used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. The 352 x 288 CMOS PAPS chip is designed with the pixel size of 5.8 μm x 5.8 μm. The pixel readout speed is from 100 kHz to 10 MHz, corresponding to the maximum frame rate above 30 frames/sec. The proposed still CMOS imager has a fill factor of 58%, chip size of 3110 μm x 2760 μm, and power dissipation of 24 mW under the power supply of 3.3 V. The experimental chip has successfully demonstrated the function of the proposed new PAPS structure. It can be applied in the design of large-array-size still CMOS imager systems with low dark current and high resolution.

In the design of the optimal pseudo active pixel sensor (OPAPS) structure for the applications of CMOS imagers, the zero-biased buffer is shared by several pixels to increase fill factor, suppress dark current of photodiodes, and decrease the leakage current of parasitic pn junctions. The factor of photocurrent-to-dark-current ratio per pixel area (PDRPA) is defined and optimized in the OPAPS structure. It is found that one zero-biased-buffer shared by four pixels in 0.25 μm single-poly-five-level-metal (1P5M) N-well CMOS technology can achieve the maximum PDRPA factor and thus represents the best choice. In imagers with the OPAPS structure, the double delta sampling (DDS) circuits are also used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. An experimental chip of CIF OPAPS CMOS imager is designed, fabricated, and measured. The measurement results have verified the performance of the proposed OPAPS structure.

The 352 x 288 (CIF) OPAPS CMOS imager chip is designed to work under 3.3 V power supply. One shared zero-biased-buffer is used for four pixels where the PDRPA is equal to 37.7 μm^{-2}. The fabricated OPAPS CMOS imager has a pixel size of 8.2 μm x 8.2 μm, fill factor of 42%, and chip size of 3630 μm x 3390 μm. The measured maximum frame rate is 30 frames/sec and the dark current is 82 pA/cm^2. The measured optical dynamic range is 65dB. It is found that the proposed OPAPS CMOS imager has the smaller dark current than those of PAPS, APS, and PPS CMOS imagers and higher fill factor as well as higher optical dynamic range than that of APS

CMOS imager. Thus the proposed OPAPS structure has high potential for the applications of high-quality CMOS imagers.

6.2 FUTURE WORKS

In the proposed two new photodiode structures, the dark current has been reduced and the spectral response has been improved. In future research, the integration of the proposed photodiode structures with APS, PAPS, and OPAPS imagers will be performed. Although, more costs are needed in the use of the proposed photodiode structures because the additional mask of SN– is used, a good design trade-off between cost and performance can be obtained.

In the proposed PAPS pixel structure for the still CMOS imager application, the integration time can be adjusted according to the background light intensity. If high frame rate is required, the background light intensity should be increased to decrease the required integration time. Thus, in order to use the proposed PAPS CMOS imager with the frame rate as fast as that of APS CMOS imager, the appropriate background light is needed. In the future, low noise current amplifier with background current suppression can also be developed and designed to amplify the photocurrent, suppress background current, and improve the performance of frame rate. The proposed PAPS CMOS imager can also be applied in nano CMOS technology because the pixel size can be further shrunk due to its high fill factor and low dark current. In addition, it can be combined with biochemical reactions to form biochip.

In the proposed OPAPS pixel structure, it is a design trade-off between dark current and frame rate. However, the pixel size cannot be greatly shrunk in the used CMOS technology due to the distance between two N-wells with different potentials. Although the distance can be further shrunk depending on the fabricating fabs., the noise coupling between the two N-wells will degrade the image performance. Thus more different pixel shape like the hexagon and one buffer shared by more pixels can be developed and designed to decrease the effective pixel size while keeping the image performance.

In the fabricated PAPS and OPAPS CMOS imager chips, on-chip A/D conversion is replaced by a data acquisition card with the function of A/D converter. The on-chip A/D conversion is an advanced circuit technology which is applied to CMOS imager chips more recently [22], [88], [91]. Through the conversion, the digital output signal of CMOS imager chips instead of analog one can avoid noise coupling during signal transferring out of imager chips. Thus the system design can be simplified and the cables and IC chip counts can be reduced. However, the additional power and area consumptions may not be acceptable in some applications. Thus, the on-chip A/D conversion is usually used in high-performance applications. Some new structures of on-chip A/D conversion have been proposed for the design of CMOS imagers [22], [91].

In this thesis, new photodiode structures for CMOS active pixel sensor (APS) imagers and new CMOS pixel structures for low-dark-current and large-array-size imager applications are proposed, analyzed, and designed. All the structures and technologies discussed above have their uniqueness and features for different applications. Due to the development of new photodiode structures and pixel circuits and the fast advancement of CMOS technologies, high-performance and low-cost CMOS imaging system will be developed through the inventions of new device structure and circuit techniques. With innovative development of CMOS imager chips, a new generation of CMOS imaging systems is highly expected.

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The ANALYSIS AND DESIGN OF CMOS IMAGERS FOR LOW-DARK-CURRENT AND HIGH-SPECTRAL-RESPONSE APPLICATIONS

PUBLICATION LIST

(A) JOURNAL PAPERS

[1] Ude Lu, Ben C.-P. Hu, **Yu-Chuan Shih**, Yuh-Shyong Yang, Chung-Yu Wu, Chiun-Jye Yuan, Ming-Dou Ker, Tung-Kung Wu, Yaw-Kuen Li, You-Zung Hsieh, Wensyang Hsu, and Chin-Teng Lin, "CMOS chip as luminescent sensor for biochemical reactions," ***IEEE Sensors Journal***, vol. 3, pp. 310-316, June 2003.

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