國立交通大學

光電工程研究所

碩 士 論 文

高效能非晶系銦鎵鋅氧雙極性有機薄膜電晶體

High Performance Amorphous $InGaZnO_4$/Organic Ambipolar Thin Film Transistors

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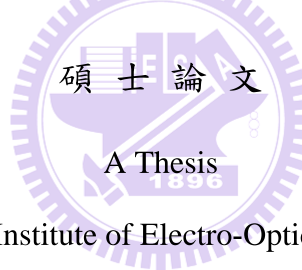

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摘　　要

在矽基板上，運用了兩種主動層材料 pentacene / a-IGZO 做成的雙極性薄膜電晶體，可以在大氣環境下有穩定的特性展現。Pentacene 在雙極性薄膜電晶體中扮演著電洞傳輸的角色，相對的 a-IGZO 則是提供了電子傳輸。許多傳統的電子傳輸材料，在空氣中都會有不穩定的效果，必須藉由覆蓋一層修飾層來達到在空氣中量測的目的，但是 a-IGZO 卻可以直接在大氣環境下有穩定的特性。而且其具有透明的新穎性，遠高於非晶矽的載子遷移率等較佳電性，還同時保留了非晶系材料的高均勻性優點。而低製程溫度的需求更進一步的揭示使用便宜的玻璃基板，塑膠基板的可行性，也暗示著軟性電子的應用。成功結合 pentacene/a-IGZO 兩種半導體材料製作成雙極性薄膜電晶體(ambipolar TFTs)，製作成 CMOS-like inverter circuit 可應用並簡化顯示器上之驅動電路。且其在第一象限有高達 70 的電壓增益，亦可工作在第三象限。

High Performance Amorphous $InGaZnO_4$/Organic Ambipolar Thin Film Transistors

Student：Yi-Hsing Chu **Advisor：Dr. Han-Ping D. Shieh**

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ABSTRACT

Air-stable ambipolar thin-film transistors (TFTs) based on double active layer of pentacene / a-IGZO (amorphous In_2O_3-Ga_2O_3-ZnO) have been examined on SiO_2 /p-Si substrates. The a-IGZO exhibits n-channel behavior, while pentacene presents p-channel characteristics. Most n-type organic materials are easily affected by moisture and oxygen, thus measuring ambipolar devices in ambience air is difficult. However, a-IGZO not only has outstanding mobility but also has good stability while being measured in ambient air. In our work, a CMOS-like inverter was constructed using two identical ambipolar transistors and the voltage gain up to 70 was obtained. CMOS-like inverter circuit was made to demonstrate the possibility for display applications. The inverter can be operated in both the first and the third quadrants, simplifying circuit design for active matrix flat panel display applications.

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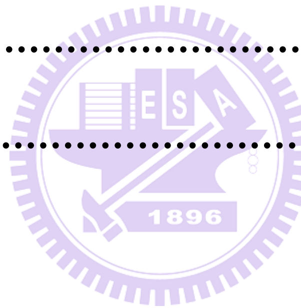

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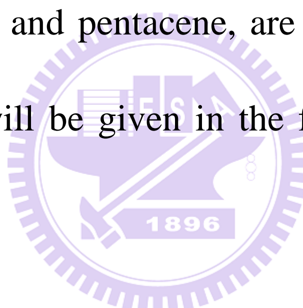
Chapter 1

Introduction

Pentacene and a-IGZO as active layer combined to make ambipolar TFTs. These devices show both p-type and n-type characteristic. Complementary-Metal-Oxide-Semiconductor-like inverter is composed of two ambipolar TFTs. In this chapter, ambipolar TFTs, CMOS-like inverter and the active layer material a-IGZO and pentacene, are presented, and the motivation and objective of the thesis will be given in the following. Final section is the organization of the thesis.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1.1. Ambipolar Thin Film Transistors

1.1.1 Introduction to Ambipolar Thin Film Transistors

An ambipolar thin film transistor is one in which both electrons and holes are accumulated depending on the applied voltages [1]. More recently, ambipolar organic field-effect transistors (OFETs) have been a focus of research due to their potential applications in organic integrated circuits (ICs). Such circuits

have many advantages, such as better immunity, lower power dissipation, simplifying fabrication and circuit design of ICs, etc.[2][3]. Ambipolar semiconductors are important for CMOS-like inverters that enable robust, low-power circuits with wide noise margins without using advanced patterning techniques to selectively deposit n- and p-channel materials. Currently there are three main structures of ambipolar OTFTs, shown in Figure 1-1, which are (a) blend structure, (b) single-component structure, and (c) bilayer structure. Blend structure is similar to single-component structure. However, the difference between blend structure and single-component structure is that blend structure is composed of 2 materials for respectively providing n-type and p-type characteristics while there is only one semiconductor material in single component structure. The active layer in bilayer structure is stacked of a p-type material and an n-type material for hole and electron transportation, respectively. Noticeable, it's not simple to find proper p-type material and n-type material because both the thickness and the junction properties affect the characteristics of OTFTs

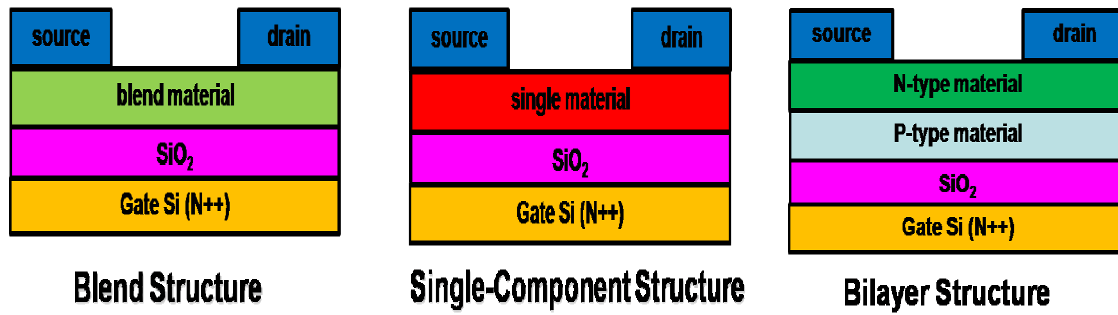


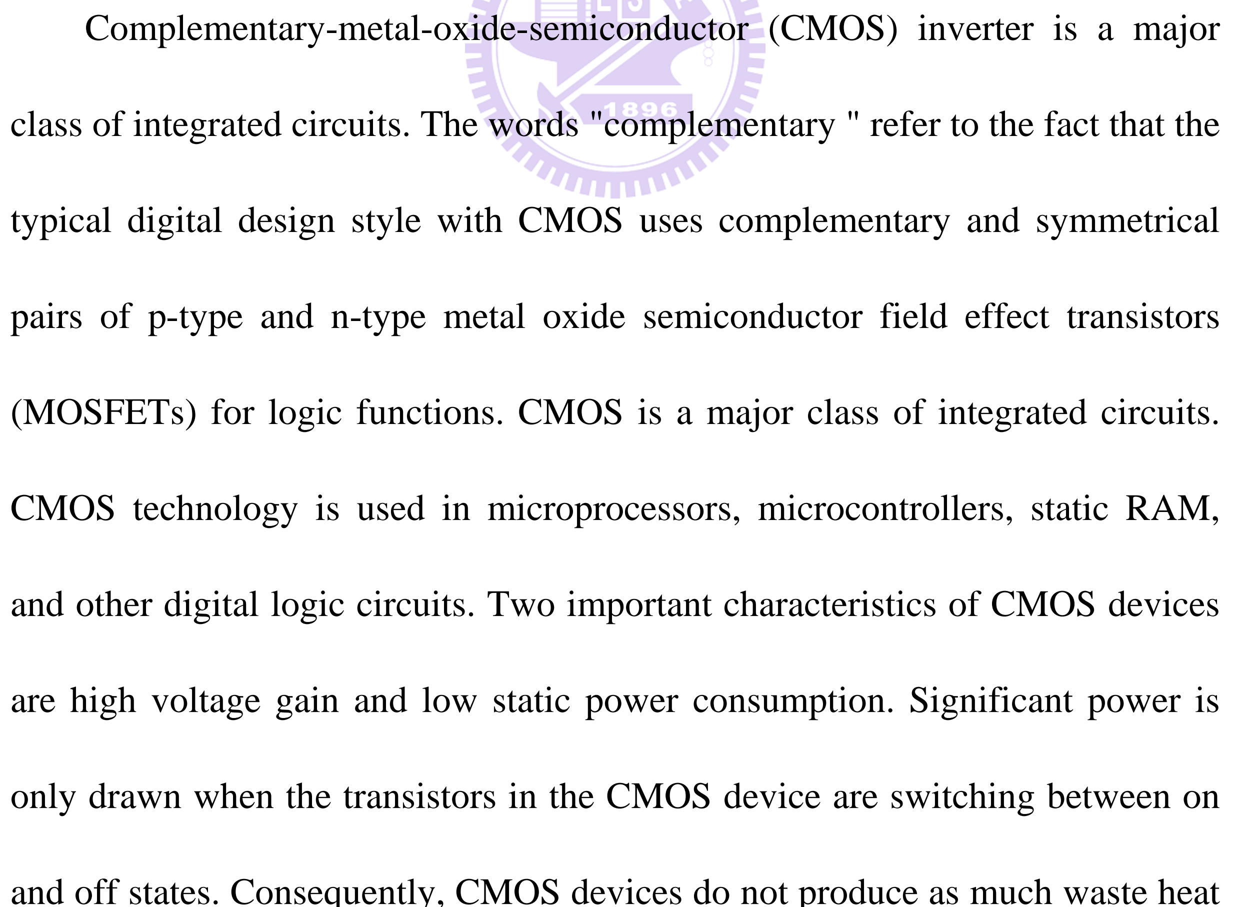
Fig. 1-1 (a) blend structure, (b) single-component structure, and (c) bilayer structure.

1.1.2 Issues of ambipolar thin film transistors

For n-type OTFTs, electron channel cannot be formed successfully in ambient air so that the TFTs show only p-type characteristics. The characteristic of ambipolar TFTs was measured in inert gas environment in most previous works [4-7]. Stability has always been an important issue for TFTs applications although some groups [8, 9] had developed ambipolar OTFTs operable in ambient air. For example, Haibo Wang, et al. [9] reported the bilayer structure composed of BP2T (5, 5'-bis (4-biphenylyl)-2, 2'-bithiophene) and F16CuPc (Copper hexadecafluorophthalocyanine) in reference, the electron and hole mobility were up to 0.036 cm^2/Vs and 0.04 cm^2/Vs, respectively. Organic thin films such as pentacene are widely studied as active channel layers for the TFTs [10]. Like most

of the p-type organic semiconductors studied, pentacene exhibits inherent p-type conduction when grown on a SiO_2 gate oxide. On the other hand, metal oxide systems such as indium oxide (In_2O_3) were found to be promising materials for the n-channel TFTs [11], [12]. However in previous studies mentioned above, the voltage gain is small. Further, n-type material is unstable in air; the fabrication of stable ambipolar OTFTs is hence limited to few materials.

1.2 Complementary-Metal-Oxide-Semiconductor Inverter



Complementary-metal-oxide-semiconductor (CMOS) inverter is a major class of integrated circuits. The words "complementary " refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. CMOS is a major class of integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. Two important characteristics of CMOS devices are high voltage gain and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat

as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which uses all n-channel devices without p-channel devices. The inverter circuit and standard symbol are shown in Figs. 1-2 (a) and (b), respectively [13]. The transfer characteristic curve can be divided into 5 regions as shown in fig. 1-2(c) and the states are listed in table 1-1. Otherwise, when PMOS and CMOS both are saturation, CMOS can be an analog signal amplifier to amplify small signal. (Fig. 1-2 (c)).

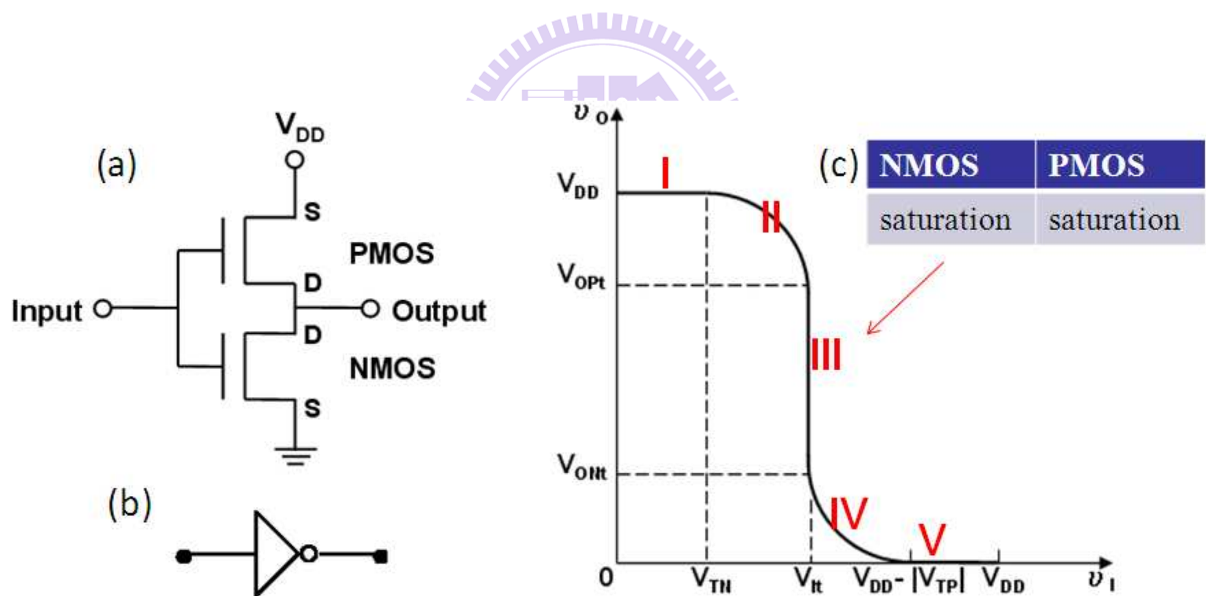


Fig. 1-2 (a) CMOS inverter circuit (b) standard symbol

(c) operate region

Table 1-1 CMOS operate regin

V_{in}	n-MOS	p-MOS	Vout
0	**cut-off**	**linear**	V_{DD}
$V_{TN}<V_{in}<V_{DD}/2$	**saturation**	**linear**	$\sim V_{DD}$
$V_{DD}/2$	**saturation**	**saturation**	$V_{DD}/2$
$V_{DD}-\|V_{TP}\|>V_{in}>V_{DD}/2$	**linear**	**saturation**	**~0**
V_{DD}	**linear**	**cut-off**	**0**

The function of CMOS inverter can be summarized by the following table:

Table 1-2 CMOS inverter characteristic

Input	Output
High	Low
Low	High

The output is the opposite of the input - this circuit inverts the input. Notice that always one of the transistors will be an open circuit and no current flows from the supply voltage to ground. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic

(TTL) or NMOS logic, which uses all n-channel devices without p-channel devices. CMOS also allows a high density of logic functions on a chip.

1.3 Amorphous IGZO Thin Film Transistors

1.3.1 Introduction to amorphous oxide semiconductor

Recently, amorphous oxide semiconductors (AOSs) have attracted much attention because AOS TFTs exhibit large mobility with low-temperature or even room-temperature fabrication.[14-19] The conduction bands of the AOSs are derived from the ns orbital of heavy metal cations such as In^{3+}, Ga^{3+}, and Zn^{2+} [19]. The electron transport path is very efficient because of the large radii and large overlap between adjacent ns orbital of spherical symmetry, which leads to insensitiveness to the distorted metal–oxygen–metal chemical bonds. However, metal oxide semiconductors such as zinc oxide (ZnO) are polycrystalline in nature. The grain boundaries of such metal oxides could affect device properties, uniformity and stability over large areas. To overcome this issue, a new ternary oxide material comprised of In, Ga, Zn and O has been proposed for use as the channel layer in TFTs. Figure 1-3 shows the differences in carrier transportation mechanism for covalent semiconductors, for example, silicon (Si), and ionic

oxide semiconductors, in certain molecular orbital configuration, like a-IGZO. The spatial spread of this vacant s-orbital is so large that direct overlap between the s-orbitals of the neighboring cations is possible in heavy metal oxides, and therefore an effective mass of electron is small in these oxides. Electron transport path is also very efficient because of the large radii and large overlap between the adjacent ns orbitals of spherical symmetry, which is less sensitive to the arrangement of atoms. Oxide semiconductors have shown comparable mobilities both in crystalline and amorphous phases, while covalent semiconductors such as silicon shows at least two to three orders of magnitude smaller mobility in the amorphous phase. (Fig. 1-3)

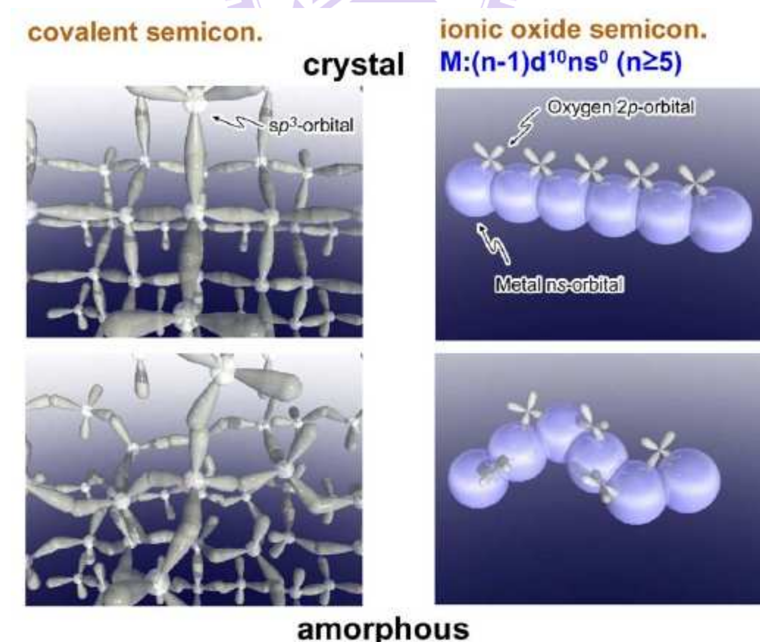


Fig. 1-3 Schematic orbital drawing of electron pathway in covalent and ionic oxide semiconductors

1.3.2 Introduction of a-IGZO

One of the most interesting oxide semiconductors for TFT application is a-IGZO. It was proposed by Hosono et al [20]. Amazingly, high mobility of 7 cm^2/V s and high on/off ratio of more than five orders of magnitude were achieved even at room temperature process [20]. Incorporating Ga ions is crucial in a-IGZO for suppressing excessive carrier generation via oxygen vacancy. Ga3+ is supposed to attract the oxygen ions tightly due to its high ionic potential (+3 valence and small ionic radius), and thereby suppressing electron injection which is caused by oxygen ion escaping from the thin film. Amorphous IGZO semiconductor possesses three unique features in comparison with conventional a-Si semiconductor, that is, high performance, low process temperature and transparency. a-IGZO film is transparent in visible light range (300~800 nm) and near infrared range of the spectrum with transmittance greater than 80 percent. Without expensive laser apparatus like the poly-Si TFT process, depositing a-IGZO thin film by sputter at room temperature is feasible on the large area. Room temperature sputter makes the mass production on flexible plastic or cheap soda-lime glass viable.

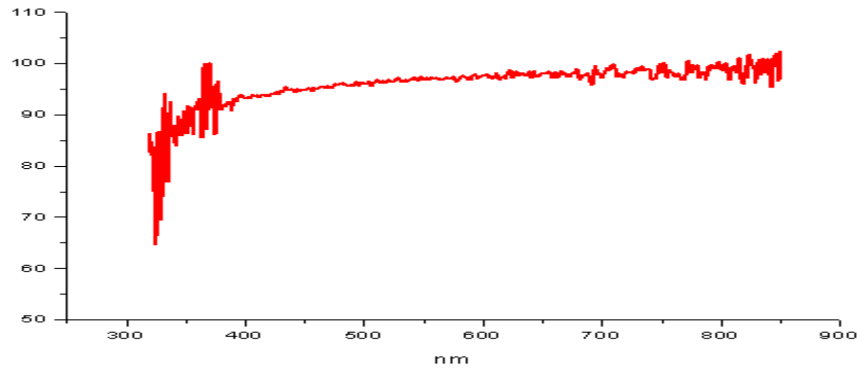


Fig.1-4 Transmittance of a-IGZO in visible light

1.4 Overview of Organic Thin Film Transistor (OTFT)

1.4.1 Introduction to Organic Thin Film Transistor

Organic semiconductor was discovered in 1940s [21]. The possibility of fabricating OTFTs with small conjugated molecules was proposed in 1989 with sexithiophene. For a decade, their OTFT performance is improved continuously. Because of their unique properties, organic materials are suitable to be made on the flexible substrates. Many interesting applications such as flexible displays, smart cards, radio frequency identification tags, as well as light-emitting diodes (LEDs) and lasers have been demonstrated (Fig. 1-5).

Fig. 1-5 Applications of organic transistors

1.4.2 Organic Materials- Pentacene

Pentacene, $C_{22}H_{14}$, a fused-ring polycyclic aromatic hydrocarbon, is one of the promising candidates of organic semiconductors. Its chemical structure is depicted in Fig. 1.6. There are ways to fabricate it as a continuous film such as the solution process, vapor phase deposition and thermal evaporation.

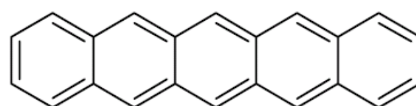


Fig. 1-6 Structure of n-type material pentacene

1.5 Motivation and objective

There are few researches using metal-oxide semiconductors to act as the n-type material for ambipolar TFTs. Using a-IGZO for ambipolar TFT has not been reported yet. Furthermore, stability in ambient air, poor characteristic is the critical issue of conventional organic n-type material such as PTCDI-C8, F16CuPc, etc. We adopted a-IGZO for this study due to its high mobility and it is insentivity to oxygen and moisture in air. A novel ambipolar TFT composed of active layer material a-IGZO and pentacene is illustrated in Fig. 1-7. Unlike conventional CMOS inverter, our CMOS-like inverter can be operated in two quadrants since our ambipolar TFTs have both n-type and p-type behavior. This makes the circuit design simpler, and can be adopted for display circuit applications.

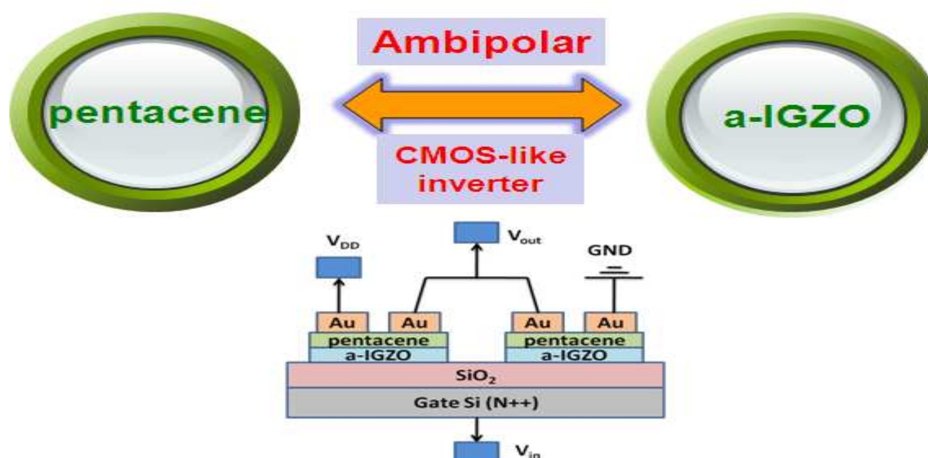
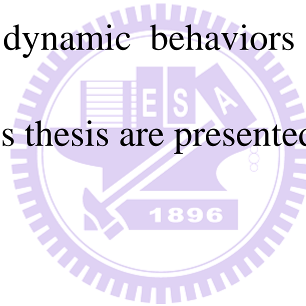


Fig. 1-7 Ambipolar TFT and CMOS-like inverter diagram

1.6 Organization of Thesis

This thesis is organized as follows: The important parameters about transistors and CMOS inverter, the sputter systems, and fabrication method are presented in **Chapter 2**. In **Chapter 3**, the novel fabrication process of the ambipolar TFTs is described introduced in detail, important parameters such as mobility, threshold voltage, subthreshold swing and on-off ratio are also described. The experimental results, including the I_{DS}-V_{DS} characteristic, I_{DS}-V_{GS} characteristic, voltage gain, dynamic behaviors are discussed in **Chapter 4**. Finally, the conclusions of this thesis are presented in **Chapter 5.**



Chapter 2

Principles and Theories

Important parameters associated with transistor and CMOS inverter are presented in this chapter. Besides, the principle of sputter system is described detail. Finally the operational principle for TFTs is described.

2.1. Important parameters of TFTs

The quality of a transistor can be examined through several parameters such as a high mobility, a threshold voltage (V_T) close to 0, and a small subthreshold swing (S.S).

2.1.1. Mobility (μ)

Under the external bias field, carriers can transport in the material. It is called mobility. The value of mobility can be defined in both linear and saturation regions.

(i) When the gate voltage (V_G) is low, the transistor works in linear region. The drain current (I_D) is linear to the V_G. The I_D can be expressed in terms of Eq. (2-1).

$$I_D = \mu C_{OX} \frac{W}{L} \left[V_G - V_T - \frac{V_D}{2} \right] V_D \qquad (2\text{-}1)$$

where

C_{OX} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_T is the threshold voltage.

If V_D is much smaller than $V_G - V_T$, I_D can be approximated as:

$$I_D = \mu C_{OX} \frac{W}{L} (V_G - V_T) V_D \qquad (2\text{-}2)$$

The transconductance (g_m) is defined as

$$g_m = \frac{\partial I_D}{\partial V_G} |_{VD=const.} = \frac{W}{L} \mu C_{OX} V_D \qquad (2\text{-}3)$$

Therefore, μ can be obtained by

$$\mu = \frac{L}{W C_{OX} V_D} g_m \qquad (2\text{-}4)$$

(ii)When V_D is larger thanV_G, the characteristic of TFTs is in saturation region. The I_D can be expressed as:

$$I_D = \mu C_{OX} \frac{W}{2L} (V_G - V_T)^2 \qquad (2\text{-}5)$$

Followed by taking square of the I_D, this term is taken differentiation to the

V_G, which can be expressed as:

$$\frac{\partial\sqrt{I_D}}{\partial V_G} = \sqrt{\frac{WC_{OX}}{2L}}\ \mu \tag{2-6}$$

μ can be expressed in Eq. (2-7).

$$\mu = \sqrt{\frac{2L}{WC_{OX}}} \times \frac{\partial\sqrt{I_D}}{\partial V_G} \tag{2-7}$$

2.1.2 Threshold voltage (V_T)

The V_T of a MOSFET is defined as the V_G where an inversion layer forms at the interface between the insulating layer and the substrate of the transistor. Conventionally the V_G at which the electron density at the interface is the same as the hole density in the neutral bulk material is called the V_T. Practically speaking, the V_T is the voltage at which there are sufficient electrons in the inversion layer that provides a low resistance conducting path between source and drain of MOSFET. If the V_G is below the V_T, the transistor is turned off and ideally there is no current from the drain to the source of the transistor. As shown in Fig. 2-1, if the V_G is above the V_T, the transistor is turned on, due to there being many electrons in the channel at the oxide-silicon interface, creating a low-resistance channel where charges can flow from drain to source.

2.1.3 Subthreshold swing (S.S)

Subthreshold swing (S.S in V/dec) is a typical parameter to describe the control ability of gate toward channel. It is defined as the amount of V_G required to increase/decrease I_D by one order of magnitude. Subthreshold swing, indicated in Fig.2-1, should be independent of V_D and V_G. However, in reality, S.S. might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punchthrough-like effect. The S.S. is also related to V_G due to undesirable factors such as serial resistance and interface states.

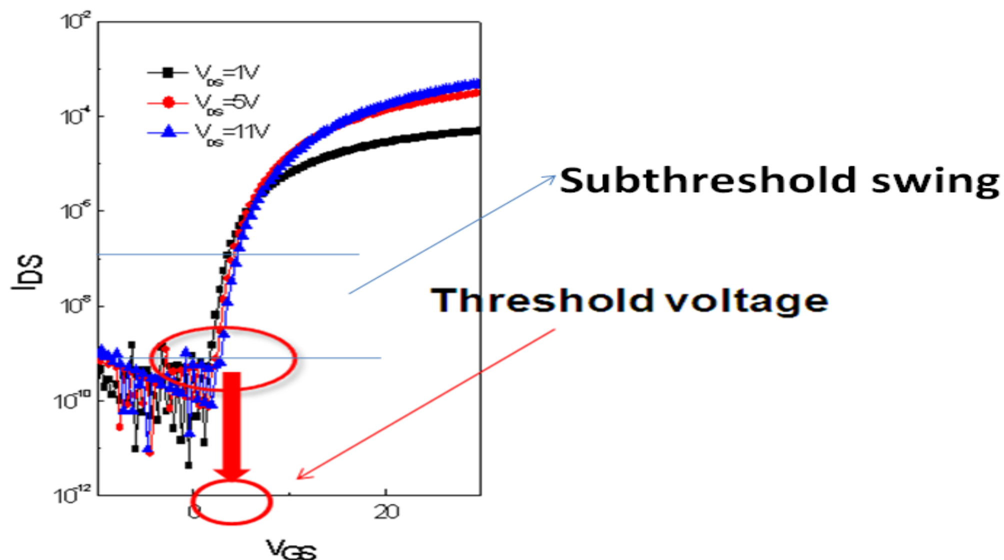


Fig. 2-1 Threshold voltage and subthreshold swing diagram

2.1.4 On-off ratio

On-current represents for the I_D when transistor is in on state. Contrary, off-current means the I_D when transistor is in off state. When the on/off current ratio is large, the leakage current can be regarded as negligible.

2.2. Important Parameters of CMOS Inverter

2.2.1. Voltage Gain

In electronics, gain is a measure of the ability of a circuit (often an amplifier) to increase the power or amplitude of a signal. It is usually defined as the mean ratio of the signal output of a system to the signal input of the same system. Voltage gain can be expressed as in Eq. (2-8)

$$\text{Voltage gain} = -\frac{dV_{out}}{dV_{in}} \tag{2-8}$$

2.2.2. Dynamic behavior

Dynamic behavior is an important parameter for CMOS inverter. Propagation delay and power dissipation are the key analysis in dynamic behavior. The delay of the CMOS inverter is a performance metric for how fast the circuit is. Fig.2-2 shows this delay is dependent upon the RC charging or discharging of the load

capacitor by the PMOS or NMOS devices respectively and provides a quantitative feel for the time that is taken by the output of the inverter to completely respond to a change at its input.

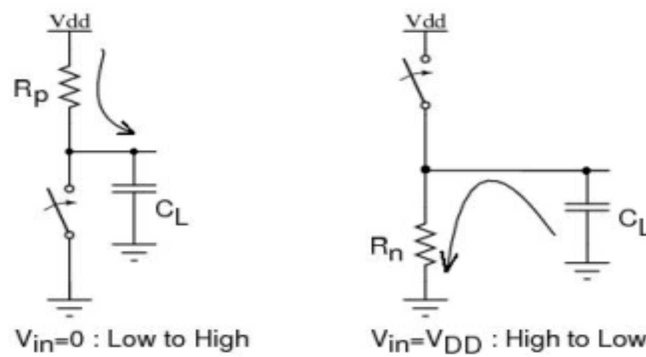


Fig.2-2 Charging and discharging process

Table 2-2 lists the definitions of temporal parameters of digital circuits. All percentages are of the steady state values.

Table 2-2 Parameters of digital circuits

Rise Time t_r	Time taken to rise from 10% to 90%
Fall Time t_f	Time taken to fall from 90% to 10%
Edge Rate t_{rf}	$(t_r + t_f) / 2$
H-to-L propagation delay t_{PHL}	Time taken to fall from V_{OH} to 50%
L-to-H propagation delay t_{PLH}	Time taken to rise from 50% to V_{OL}
Propagation delay t_p	$(t_{PHL} + t_{PLH}) / 2$

Graphical representation of dynamic behavior is shown in Fig. 2-3.

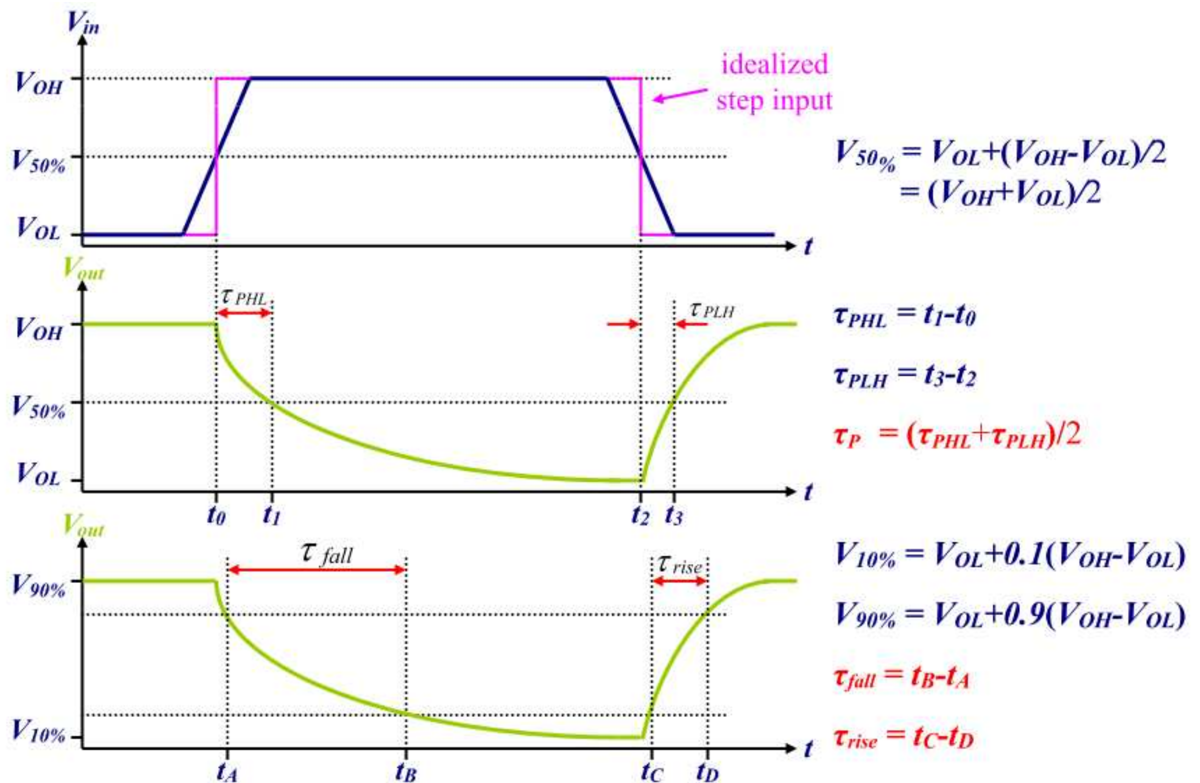


Fig. 2-3 Graphical depiction for dynamic behavior

2.3 Principle of Sputter Deposition

Sputter deposition is a physical vapor deposition (PVD) method on their agglomerates thin films. Sputtering is a process whereby atoms are ejected from a solid target material due to strike of the target by energetic ions on target. Figure. 2-4 (a) shows the construction of a sputter system. The primary particles for the sputtering process can be supplied in a number of ways, for example by a plasma, an ion source, an accelerator or by a radioactive material emitting alpha

particles. As shown in Fig. 2-4(b), argon (Ar) was ionized under high electrical field. The target particle is deposited on the substrate by Ar^+ striking on the target.

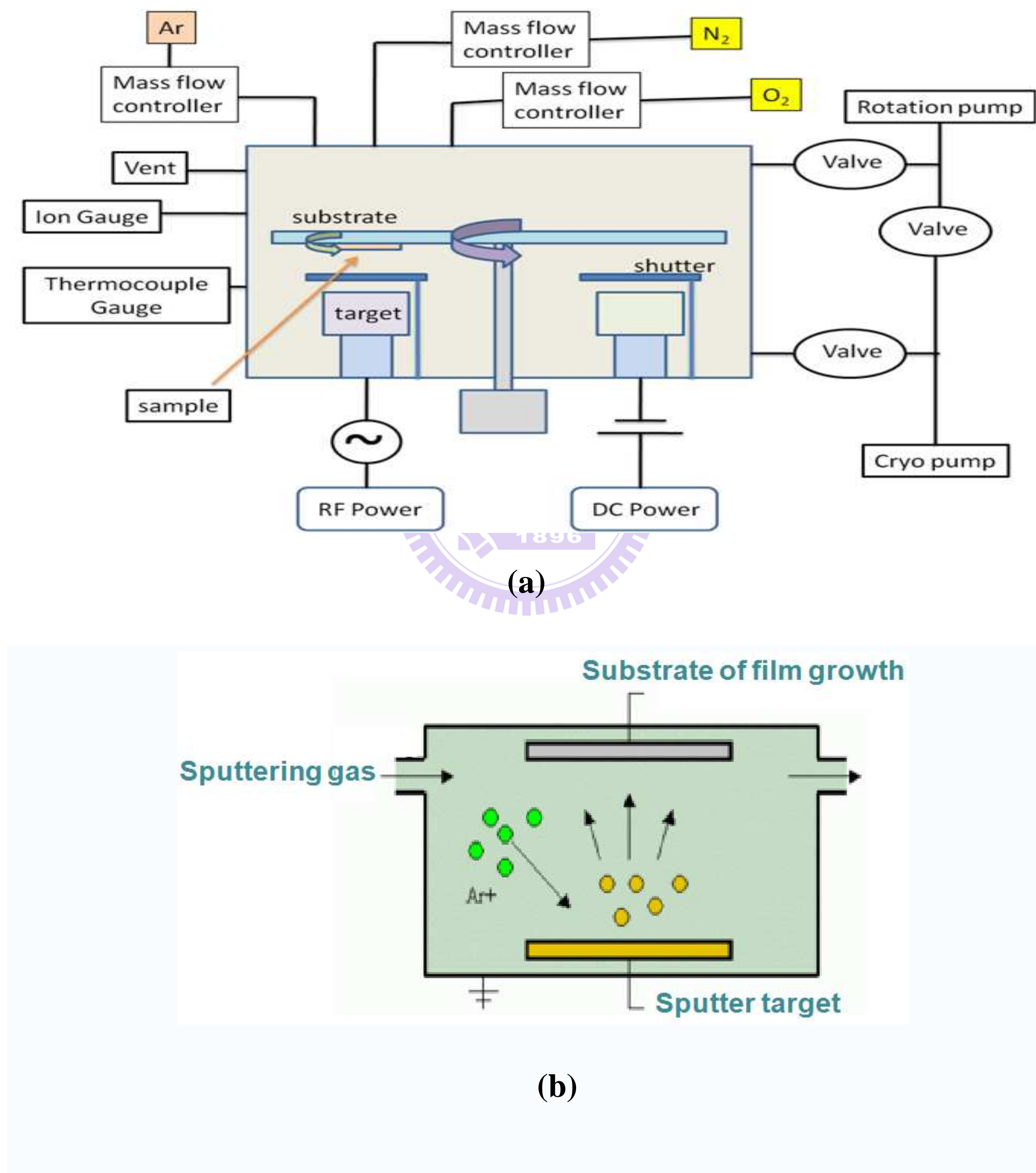


Fig. 2-4 (a) Sputter system diagram and (b) Sputter mechanism diagram.

Sputter system has two operate modes, D.C. (direct current) and RF (radio frequency) mode. The common arrangement for a D.C. sputter coater is to make the target material in negative bias state, while the substrate is in anodic state. The desired operating pressure is achieved by using a suitable vacuum system, usually comprised rotary pump and a high vacuum pump such as turbo pump or cryo pump. An inert gas, such as argon, is admitted to the chamber by a fine control valve. The sputtered atoms are neutrally charged and so are unaffected by the magnetic trap. Charge build-up on insulating targets can be avoided with the use of RF sputtering where the sign of the anode-cathode bias is varied at a high rate. RF sputtering works well to produce highly insulating oxide films but only with the added expense of RF power supplies and impedance matching networks. Figs. 2-4(c) and (d) show DC sputter system and RF sputter system, respectively.

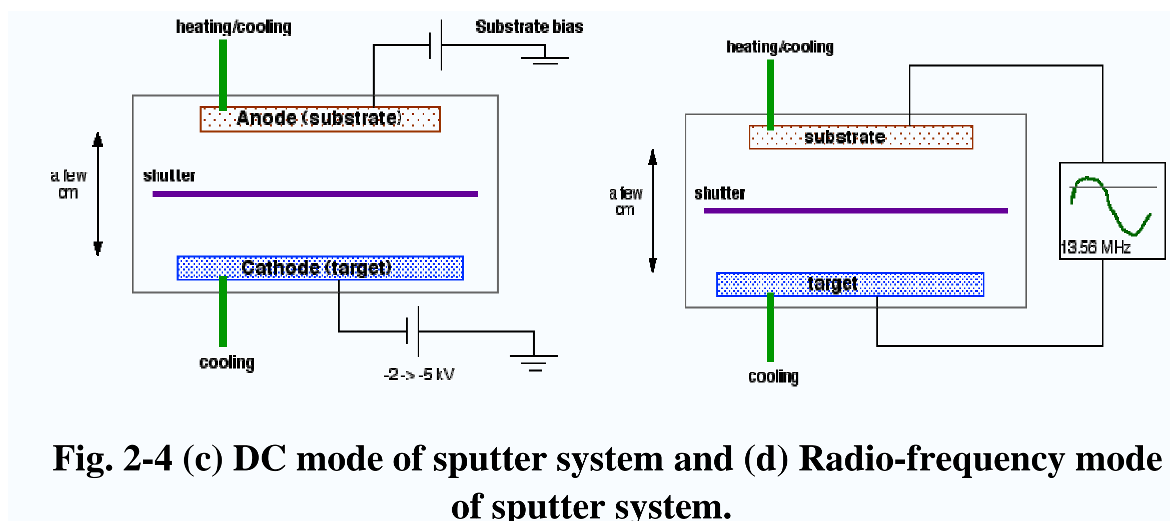


Fig. 2-4 (c) DC mode of sputter system and (d) Radio-frequency mode of sputter system.

2.4 **Operational Basics of Field Effect Transistors**

Generally, thin film transistors (TFTs) are composed of four components: substrate, semiconductor (also called active layer), insulator and electrodes. The configuration of these elements with two different structures, one is top contact and the other is bottom contact TFTS, are depicted in Fig. 2-5. The electrical characteristics of TFTs can be adequately described by models developed for inorganic semiconductors.

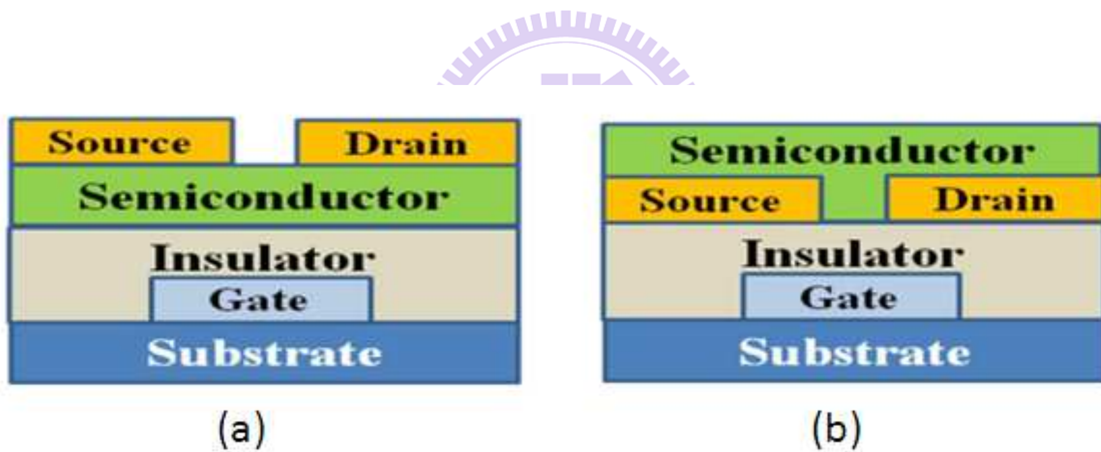


Fig. 2-5 Schematic view of (a) top contact and (b) bottom contact TFTs

The TFTs could be divided into two parts, according to the type of charges transported by the semiconductor. In semiconductors with n-type channel, the charges transported are negative. On the other hand, in semiconductors with p-type channel, the charges transported are positive. When the gate electrode is

biased positively with respect to the grounded source electrode, they operate in the depletion mode, and the channel region is depleted of carriers resulting in high channel resistance. When the gate electrode is biased negatively, they operate in the accumulation mode and a large concentration of carriers is accumulated in the transistor channel, resulting in low channel resistance. For n-type TFT operation, the electrode polarity is reversed and the majority carriers are electrons instead of holes. For instance, a p-type semiconductor is shown in Fig. 2-6 (a) When $V_D=V_S=V_G=0V$, a negative bias is forced on the gate to form the ohmic current I_D. After that, when $V_D=V_S=0V$ and $V_G<0V$, the gate current would across the insulator layer and some area of insulator-semiconductor interface would bend the band gap of the semiconductor. Then, the accumulation region is formed as shown in Fig. 2-6(b). The ohmic contact between source and drain electrodes leads to additional charges. When positive bias are applied on the gate electrode, an opposite curved band gap would occur in the insulator-semiconductor interface. This result conducts the depletion region of carriers. The higher bias on the gate electrode, the larger depletion the region expands. Finally, all of the semiconductor layer will be depleted. The voltage across the insulator and semiconductor layers depends on the position of the channel which is a functional relationship when drain voltage has strongly

negative bias effect as shown in Fig. 2-6 (d).

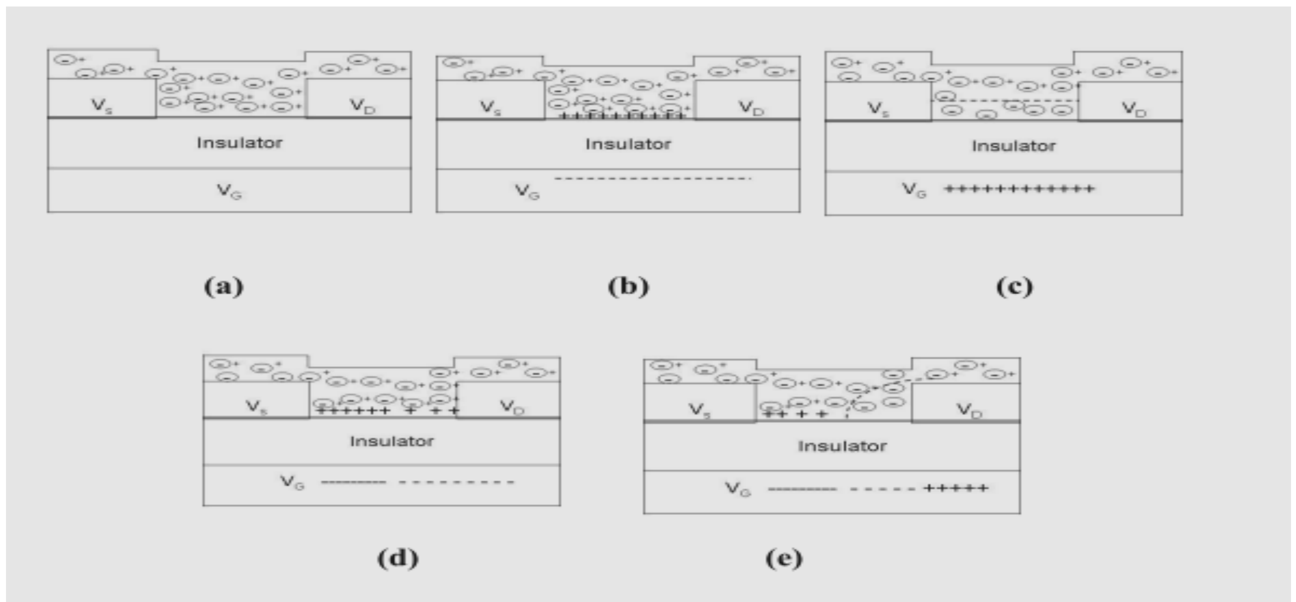


Fig. 2-6 Schematic of organic field-effect transistors operation in accumulation mode: (a) VD=VS=VG=0 V, (b) VD=VS= 0 V, VG ＜0, (c) VS = VD = 0 V, VG >0, (d) VS= 0 V, VG ＜VD＜0, and (e) VS= 0 V, VD ＜VG＜0.

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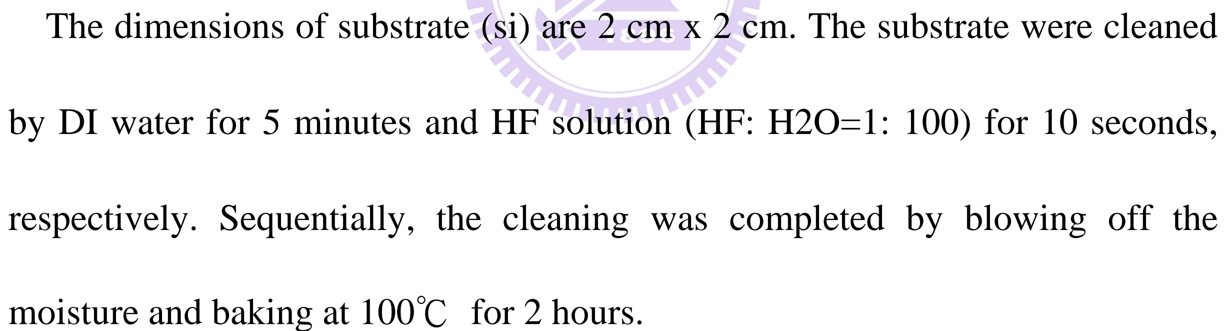
Chapter 3.

Experimental Method

The device fabrication and processing parameters are described in detail. The method of fabrication process of CMOS-like inverter is also presented in this chapter.

3.1 Experimental Steps

3.1.1 Substrates Cleaning



The dimensions of substrate (si) are 2 cm x 2 cm. The substrate were cleaned by DI water for 5 minutes and HF solution (HF: H2O=1: 100) for 10 seconds, respectively. Sequentially, the cleaning was completed by blowing off the moisture and baking at 100℃ for 2 hours.

3.1.2 Inorganic Active Layer Deposition

The sputter system with a background pressure $< 8 \times 10^{-6}$ torr shown in Fig. 3-1 was employed to deposit a-IGZO thin films. The deposition was came out at

RF power = 80W, pressures working at 8 x 10-6 torr, oxygen and argon flow rate are equal to 0.6 sccm and 0.8 sccm, respectively.

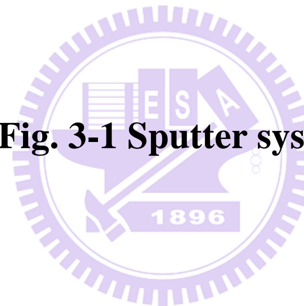
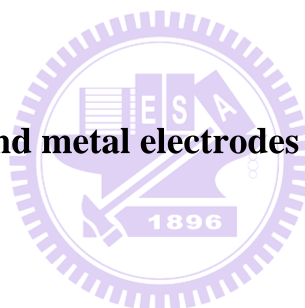


Fig. 3-1 Sputter system

3.1.3 Annealing Process

Using atmospheric anneal furnace in nitrogen ambience to rearrange a-IGZO lattice again. After annealing process, the electrical characteristic of the device is better than the device without annealing. Fig. 3-2 shows the instrument of atmospheric anneal furnace.

Fig. 3-2 Tube furnace



3.1.4 Organic active layer and metal electrodes deposition

The thermal evaporation system with background pressure about 3 x 10^{-6} shown in Fig. 3-3 was employed to deposit the pentacene layer and gold (Au) electrodes. The evaporation rate of pentacene was about 0.3~0.4 Å /sec. Subsequently, the Au electrodes were deposited onto the active layer with an evaporation rate of 1~1.5 Å /sec at a pressure of 5 x 10^{-6} torr.

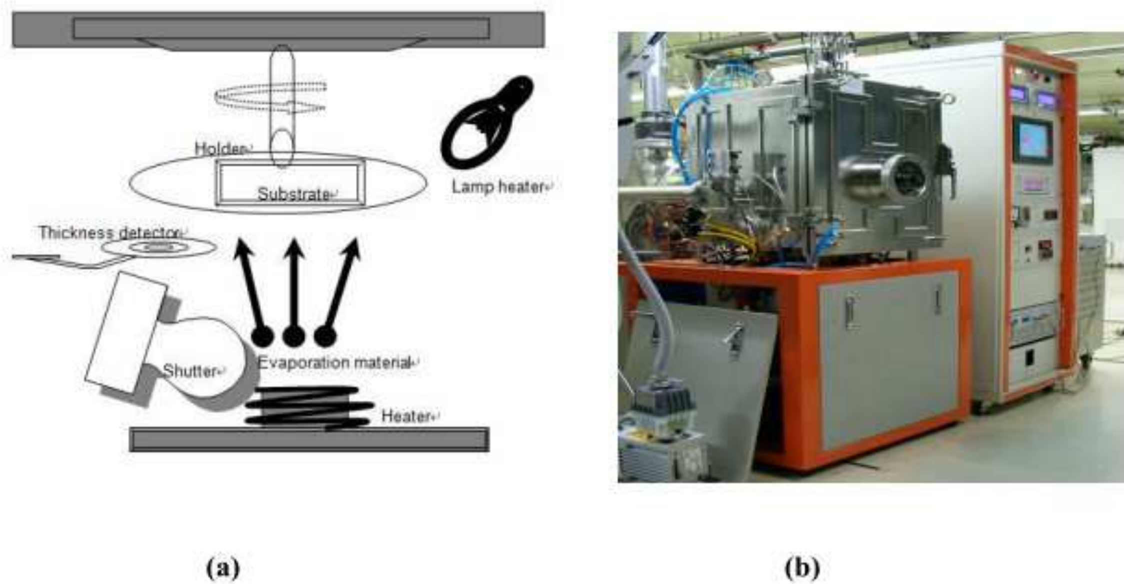


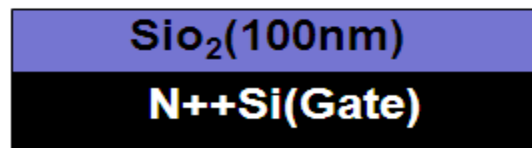
Fig. 3-3(a) A thermal evaporation system and (b) the photo of the thermal evaporated facility.

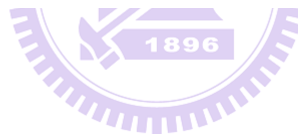
3.2 The fabrication process of a-IGZO/Pentacene TFTs

The bottom gate a-IGZO TFT structure was adopted in this study and the fabrication produces are depicted in Figure 3-4. The unit TFT was fabricated on heavily doped (n++) si wafer with 100-nm thick thermally grown oxide layer as the gate electrode and insulator, respectively. A 40-nm-thick a-IGZO film was deposited on to serve as the active channel (RT) by RF sputtering and the deposition was done in an oxygen atmosphere (~8 x 10^{-6}) without any

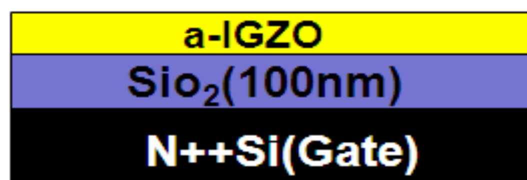
intentional substrate heating. After deposited a-IGZO film, pentacene layer was deposited by thermal coater. Finally, the Au source/drain electrodes were patterned through a stencil mask by thermal evaporation. Finally, two identical transistors were interconnected with each other to complete the CMOS inverter. All of our device characterizations were carried out in the dark at RT by using a semiconductor parameter analyzer (Keithley 4200).

(A)Start with n++Si / thermal oxide wafer & wafer clean

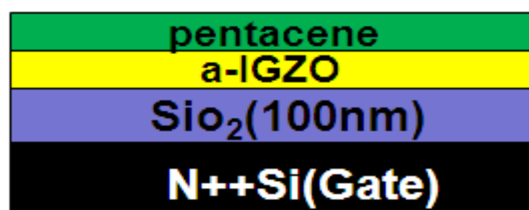




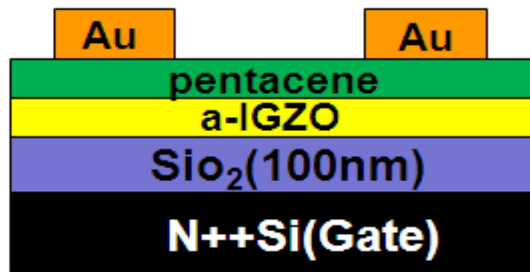
(B)Deposit a-IGZO thin film with sputter, no intentional heat



(C) Deposit pentacene layer by thermal coater



(D)Thermal evaporation of Au source/drain electrode (40nm)



(E)Ambipolar TFT is Composed of 2 single devices

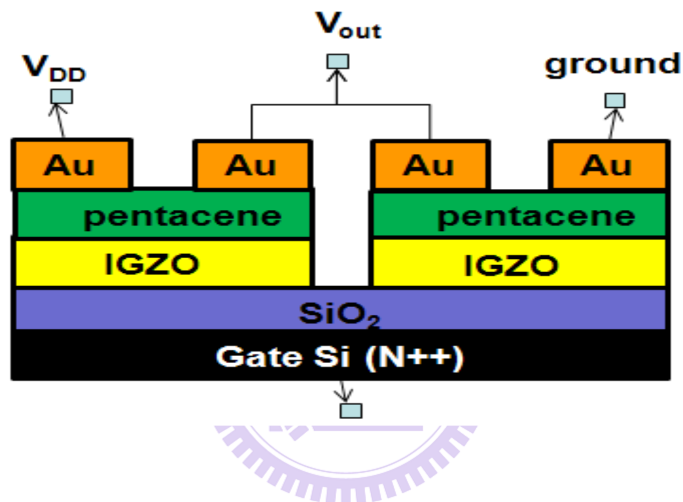


Fig. 3-4 Process of ambipolar TFT flow chart (A) Start with n++Si / thermal oxide wafer & wafer clean, (B) Deposit a-IGZO thin film with sputter, no intentional heat, (C) Deposit pentacene layer by thermal coater, (D) Thermal evaporation of Au source/drain electrode (40nm) and (E) Ambipolar TFT is Composed of 2 single devices

3.3 Electical Measurement and Morphology analyses

3.3.1 Film Morphology

An atomic force microscope (AFM) shown in Fig. 3-5 was utilized to measure the morphology of deposited active layer. The AFM was set to tapping mode and the probe oscillation frequency was 300 Hz. The tapping mode overcame the limitations arose due to thin layer of the condensed phase that formed on most sample surfaces in an ambient imaging environment. The grain size and shape of pentacene are critical when the pentacene crystals deposited on the different insulator layers. Measurements of the grain morphology by AFM were operated in the atmospheric condition. As shown in Fig. 3-6, pentacene thin films with three kinds of thicknesses, 20, 30, 40 nm, were measured by atomic force microscope (AFM). The roughness of 20, 30, and 40nm thick films were 0.162 nm, 0.151 nm, 0.137 nm, respectively.

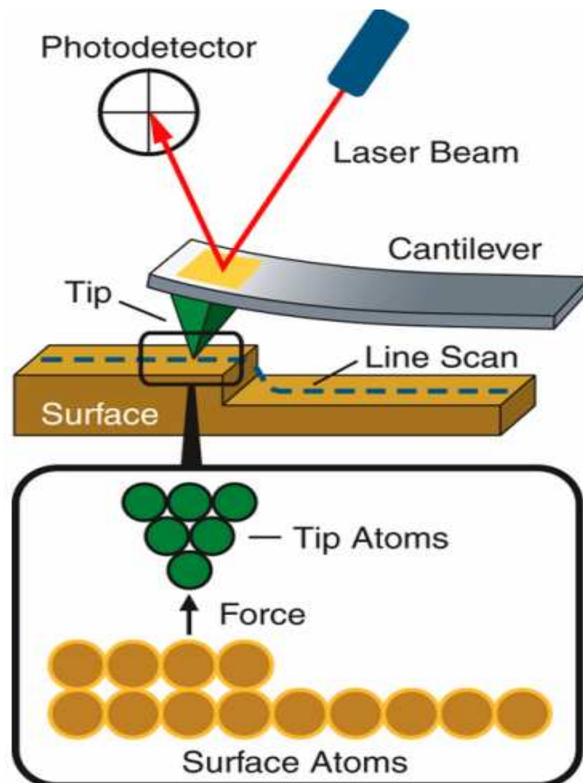


Fig.3-5 A schematic model of AFM.

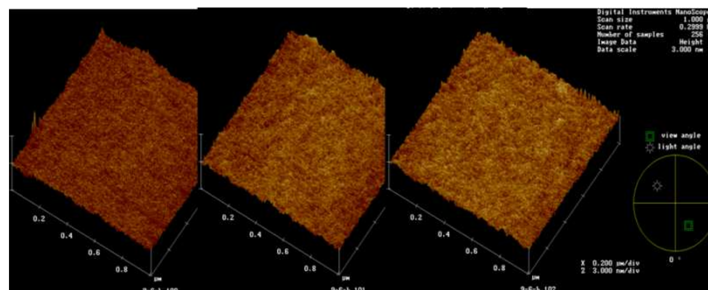


Fig. 3-6 (from left to right) AFM images of 20, 30, 40 nm thick a-IGZO films.

3.3.2 Electrical characteristics of OTFT devices

The electrical characteristics of the devices, such as degradation and hysteresis, can be evaluated by Keithley 4200 semiconductor analyzer. In addition, the relationship between I_{DS}-V_{GS} and I_{DS}-V_{GS} curves can be extracted from measurement results.

The relationship between wafers surfaces and active layers will affect the **Subthreshold swing (S.S).** Annealing process will cause the **Threshold voltage (Vth)** shift.

Chapter 4.

Results and Discussion

4.1 Optimization of the Characteristics of a-IGZO Thin Film Transistors

In order to control the electrical characteristics of a-IGZO film, TFT with the channel deposited by optimized deposition conditions (Ar / O_2 flow rate =10 sccm/0.6 sccm) was fabricated. However, post annealing process strongly affects the electrical properties of a-IGZO film; it is one of the key parameter to control the characteristics of TFT behavior. As shown in Fig. 4-1(a), the threshold voltage (Vth) shifted negatively after annealing at 350 ℃ in N_2 environment for 2 hours. Fig. 4-1(b) shows the I_{DS}-V_{DS} characteristics of the a-IGZO TFT after annealing at 350 ℃ for 1 hour. According to Figs. 4-1(a) and (b), the transfer characteristics of a-IGZO TFTs were optimized by adjusting oxygen/argon ratios during RF sputter and varying different post-annealing conditions.

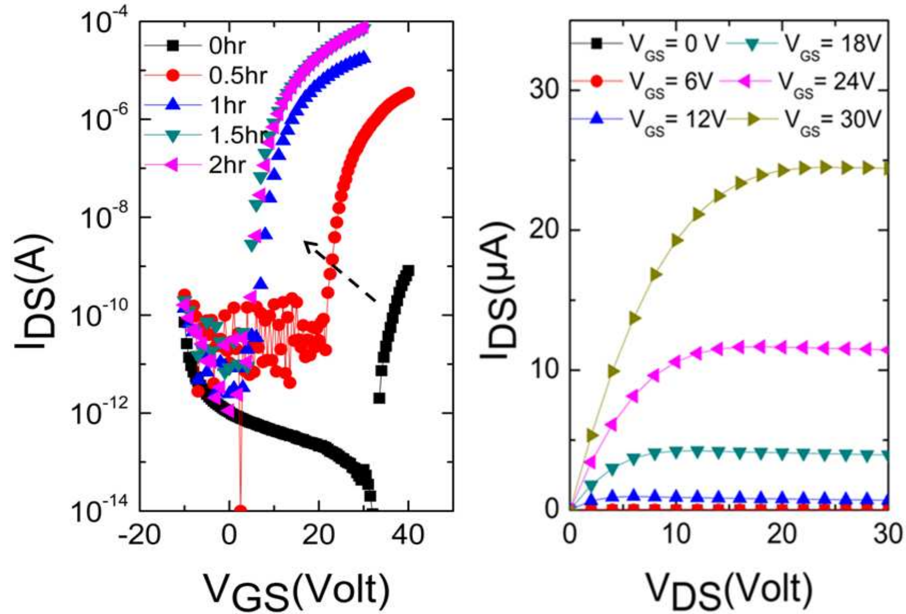


Fig.4-1 (a) I_{DS}-V_{GS} curves of a-IGZO TFT with different annealing time.

(b) I_{DS}-V_{DS} curves of a-IGZO TFT after annealing.

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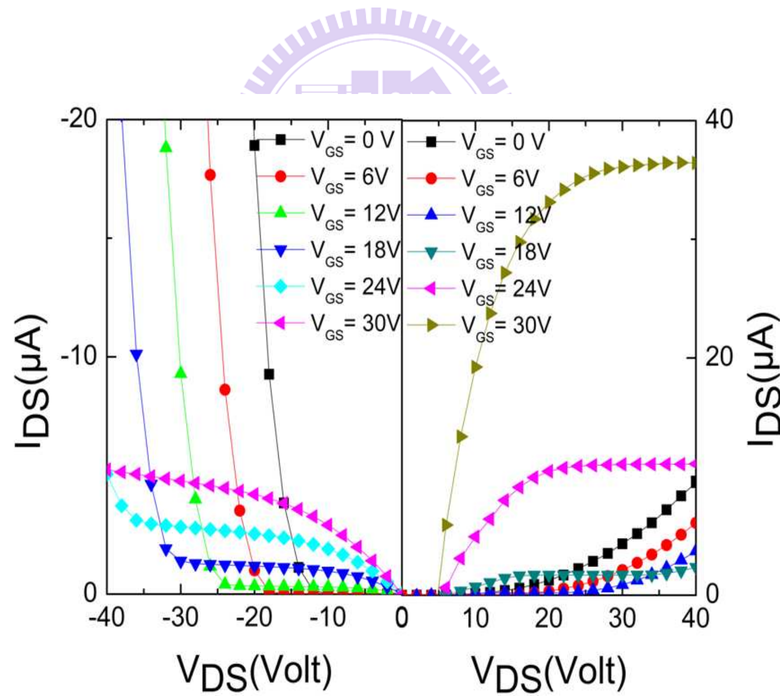
4.1.1. Discussions

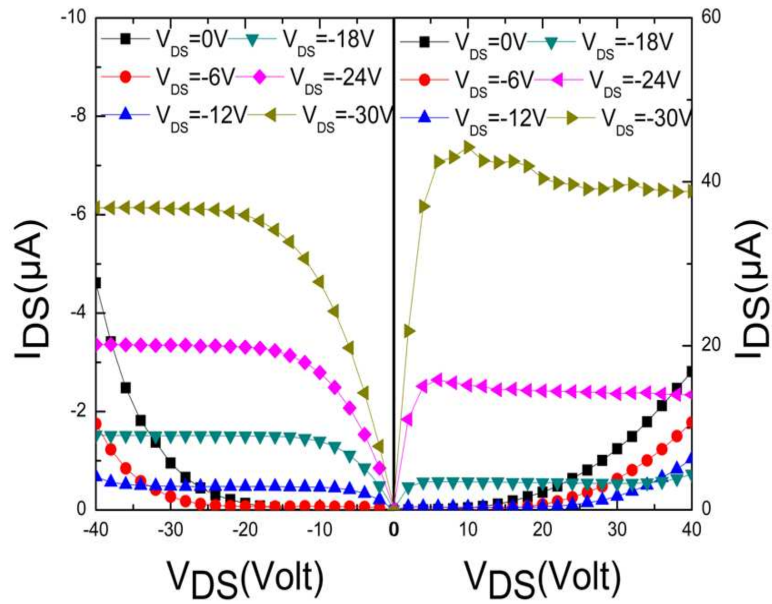
In I_{DS}-V_{GS} curves, the post annealing time from 0 to 2 hour in a half hour increment. It is noted that when the annealing time is over than 2 hour; TFTs do not exhibit an appreciable electrical characteristic and thus, are omitted from this plot. Consider the behavior of annealing time beyond 2 hour, the decrease of V_{TH} is possibly associated with crystallization (i.e., grain boundary-inhibited transport).

4.2 Characteristics of Pentacene/a-IGZO Ambipolar TFTs

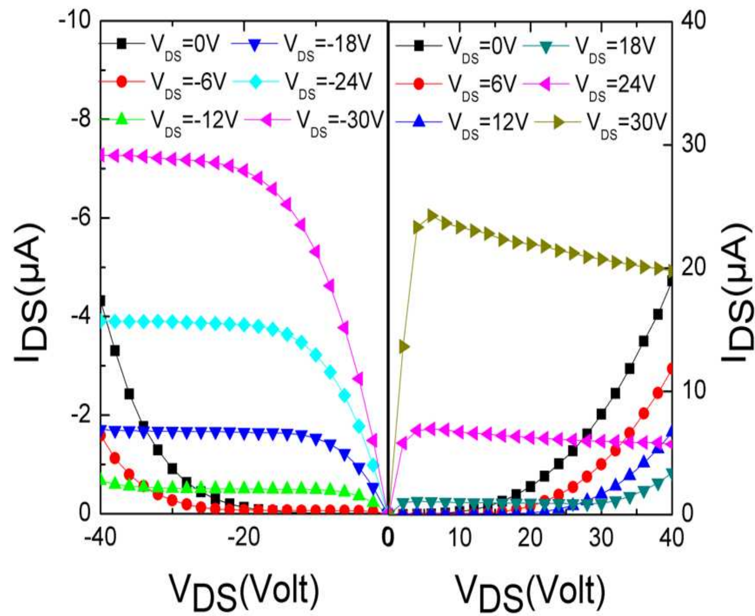
In order to optimize the electrical characteristics, several combinations of thicknesses were investigated. First, at by fixing a-IGZO thickness at 40 nm, change pentacene with thickness from 20 to 40 nm were fabricated and measured electrical property are shown in Figs. 4-2 (a) to (c). The reason for choosing a-IGZO thickness at 40 nm is that the thicker films can accumulate more carriers to attain high voltage gain.



(a)



(b)



(c)

Fig. 4-2 Thickness effect on devices (a) pentacene = 20 nm, IGZO = 40nm (b) pentacene = 30 nm, IGZO = 40nm and (c) pentacene and IGZO = 40 nm

When thicknesses of a-IGZO and pentacene films are 40 nm and 20 nm, respectively, a-IGZO layer will suppress pentacene layer's I_{DS}-V_{DS} curves. Increasing pentacene layer to 40 nm, the current is not saturated at high V_{DS}. It is noted that at the thickness of pentacene layer of 40 nm and a-IGZO layer of 20 nm, p-type layer will also suppress the n-type's electrical characteristics. Fig. 4-3 shows the effect of I_{DS}-V_{DS} curve.

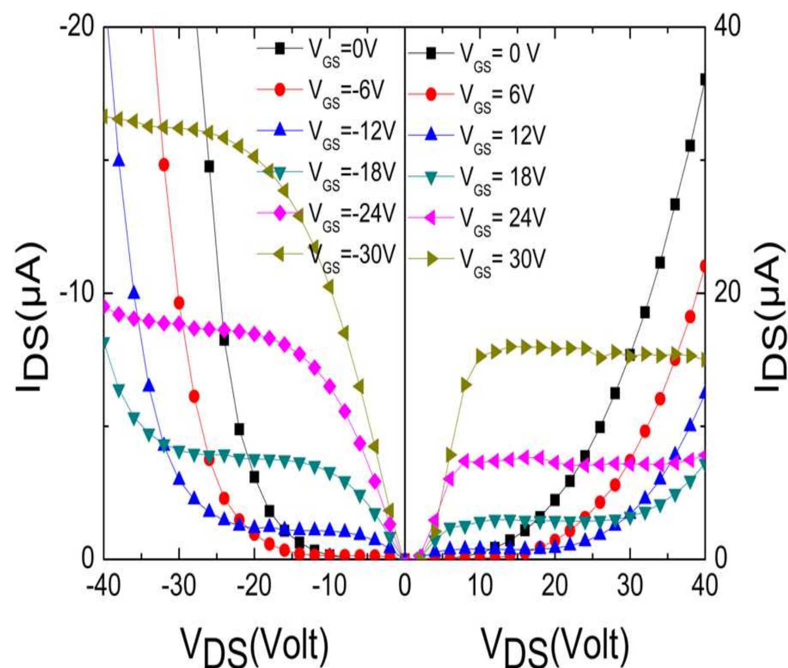


Fig. 4-3 I_{DS}-V_{DS} curves (a-IGZO/pentacene 20nm/40nm)

The optimal thicknesses of a-IGZO layer and pentacene layer were found to be 40nm and 30nm, respectively. The a-IGZO thin film (40nm) and pentacene

thin film (30nm) were deposited in order on the Si substrate with a thermally grown SiO_2 layer (100nm). Au was used as source and drain electrodes by thermal evaporation. Without any passivation layer, the TFT characteristics were successfully measured in ambient air. I_{DS}-V_{GS} curves are shown in Fig. 4-4. On/off current ratio is decreased when V_{DS} is increased. Take n-type operation for example, when $V_{DS} > V_{GS}$, holes are induced and injected into active layer due to electric field between gate and drain electrode. Mobility of 0.02 and 4.57 cm^2 V/s were estimated for holes and electrons, respectively.

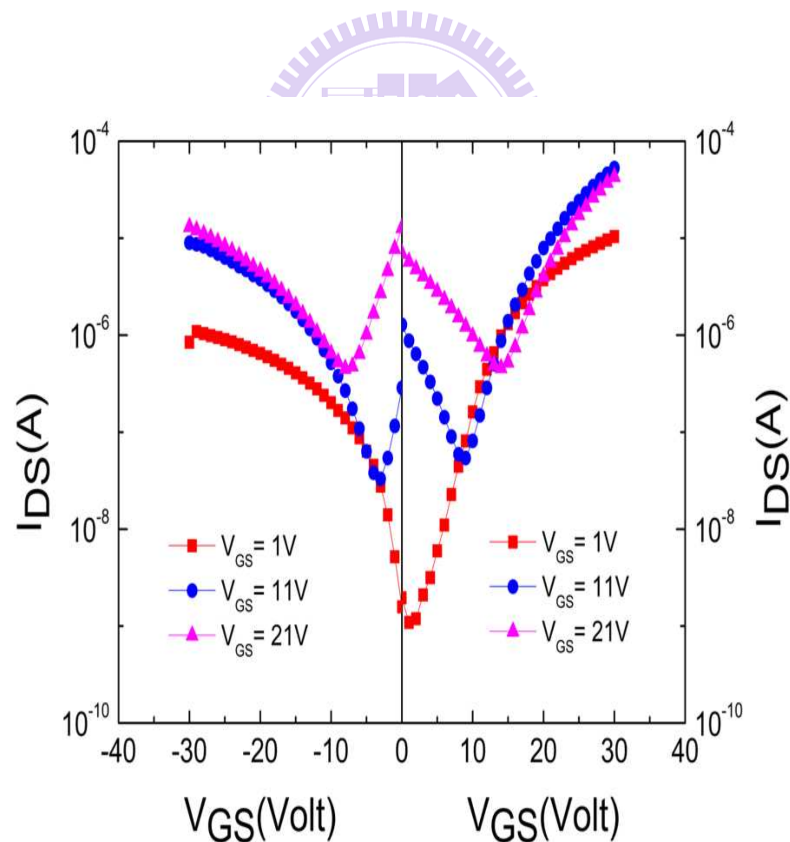
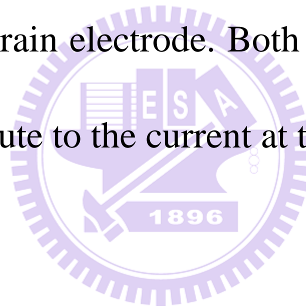


Fig. 4-4 I_{DS}-V_{GS} curve of optimized thicknesses of a-IGZO /pentacene layer

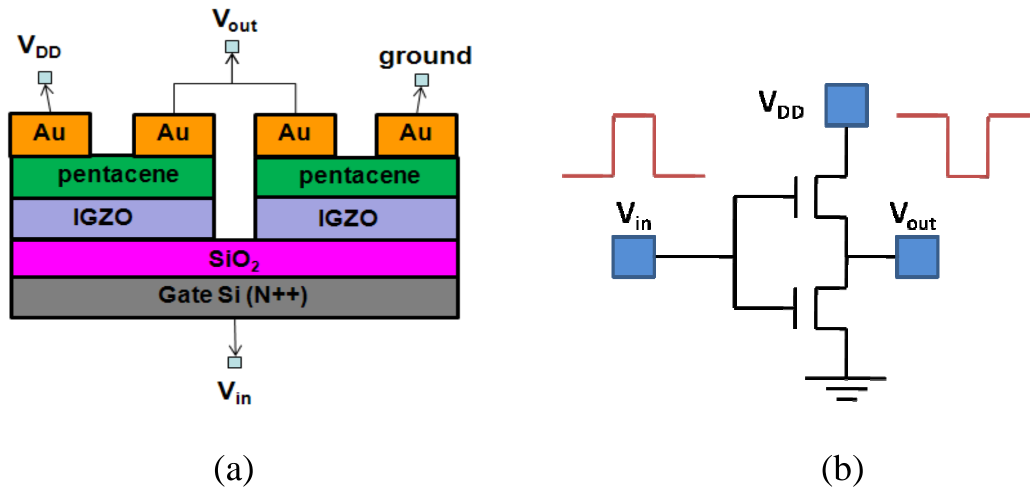
4.2.1. Discussions

There have several interesting phenomena observed during optimizing the thickness of a-IGZO/ pentacene. In the Figs. 4-2(a) and 4-3, at low V_{GS}, the current was not saturated at high V_{DS}, instead, it increased steeply. For example, when operated in n-type region, V_{GS} and V_{DS} are positively biased, when V_{DS}-V_{GS}>0, V_{DS} can be treated as 0 while V_{GS} as negative. Thus, when the voltage difference becomes larger than the amount pentacene film can sustain, holes accumulate under the drain electrode. Both electrons in n-type region and holes in p-type region contribute to the current at this moment.



4.3 Complementary Metal-Oxide-Semiconductor-Like inverter

A CMOS-like inverter was fabricated combining two ambipolar TFTs containing a-IGZO/pentacene layers. The cross-sectional view of this CMOS-like inverter and equivalent circuit are shown in Figs. 4-5 (a) and (b).



(a) (b)

Fig. 4-5 CMOS-like inverter (a) planar structure diagram (b) simplified circuit diagram

In the inverter circuit, the gate served as an input node and was shared by both transistors. The input voltage (Vin) range was 0V~ ±50V while V_{DD} was constantly biased at ±50V. Our inverter exhibits a high gain value ($-dV_{out}/dV_{in}$) about 70. In Fig. 4-6, maximum gain up to 70 was obtained when operating the inverter in n-type region. In p-type region the maximum gain up to 53. Previous studies [22, 23] reported the voltage gain of devices about 10. Higher voltage gain for CMOS and small hysteresis were observed. Small hysteresis implies small grain boundary in the surface between active layer and insulator. Unlike conventional CMOS inverter, our CMOS-like inverter can be operated in 2 quadrants, because the ambipolar TFTs have both n-type and p-type behavior.

This makes the circuit design simpler, and can be adopted for display circuit applications.

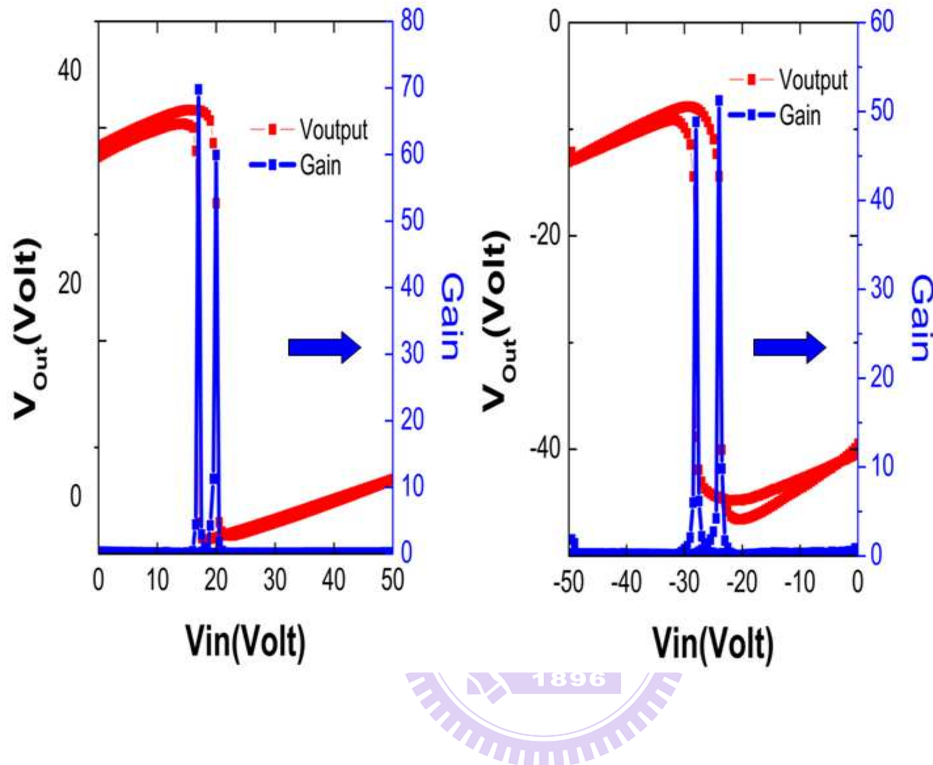


Fig. 4-6 Voltage transfer curve and their corresponding gains of ambipolar TFTs operated in the (a) first and (b) third quadrant

Dynamic response was performed by measuring the output signal V_{out} with respect to the input signal V_{in} using an oscilloscope with 1M**Ω** input impedance. At the frequency of 1 Hz, the input 30 V can invert to ~15 V. Until to the frequency of 20 Hz, the inverting action shows a little RC delay at on and off switching. Figure 4-7 shows the dynamic behavior of our inverter when

operating in the frequency range of 1Hz and 20 Hz. The rising (t_r) and falling times (t_f) at 20 Hz in our inverter was measured to be about ~2ms and 0.9 ms, respectively. Previous study published in APL [22] reported that the devices only can operate in the frequency less than 10 Hz. Our devices hence have the fastest frequency response in previous research. [22, 23]

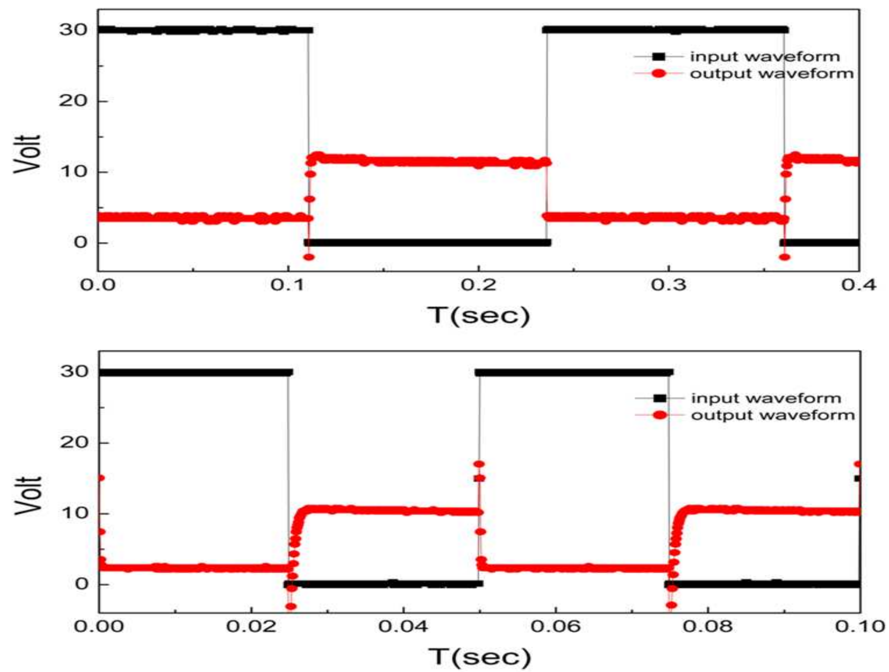
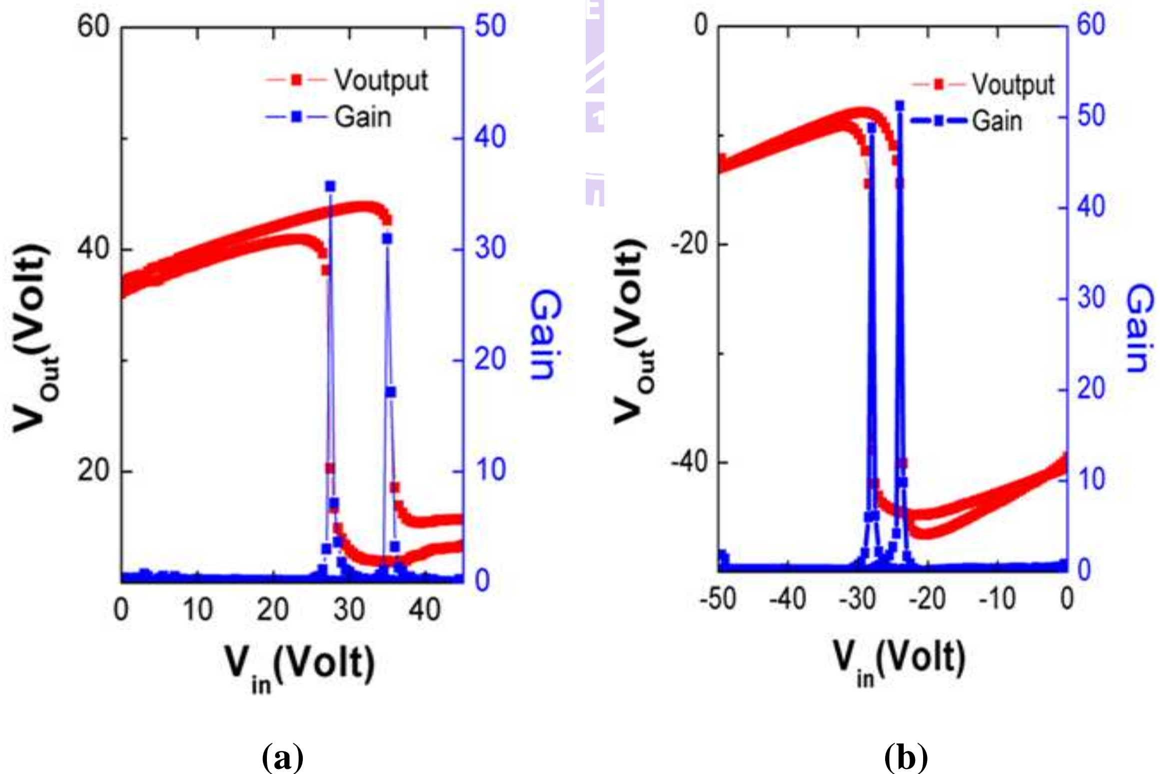


Fig. 4-7 The dynamic behavior of CMOS-like inverter. The top diagram is at 1 HZ. The bottom diagram is at 20 HZ

4.3.1. Discussions

In section 4.2, another interesting phenomenon observed during the optimization of thickness is the relationship between thickness and voltage gain. Figures. 4-8 (a) and (b) show the voltage gain diagrams. In Fig. 4-8 (a), pentacene layer and a-IGZO thin film are both at 20 nm. In Fig. 4-8 (b) pentacene layer and a-IGZO thin film are both both at 40 nm. Their I_{DS}-V_{GS} characteristic has no obviously different. However, the voltage gain is higher because the thicker active layers. The reason is that thicker films can accumulate more carriers to attain high voltage gain.



(a) (b)

Fig. 4-8 Voltage gain of CMOS-like inverter. Pentacene/a-IGZO films are (a) 20nm and (b) 40nm.

The other important parameters of CMOS inverter is dynamic behavior. To make a faster inverter (work at high frequency), Propagation delay (t_P) is a key.

$$t_{pLH} = \frac{\Delta V}{I} C = \frac{C_L \cdot V_{dd}}{k_p \cdot \frac{W}{L}\left(V_{dd} - |V_{TP}|\right)^2} \approx \frac{C_L}{k_p \cdot \frac{W}{L} V_{dd}}$$

$$t_{pHL} = \frac{\Delta V}{I} C = \frac{C_L \cdot V_{dd}}{k_n \cdot \frac{W}{L}\left(V_{dd} - |V_{TN}|\right)^2} \approx \frac{C_L}{k_n \cdot \frac{W}{L} V_{dd}}$$

$$t_p \approx \frac{1}{2}\left(t_{pLH} + t_{pLH}\right) = \frac{C_L}{2 \cdot \frac{W}{L} V_{dd}}\left(\frac{1}{k_n} + \frac{1}{k_p}\right)$$

So to reduce the propagation delay (t_P), it is necessary increase k_n 、k_p 、W/L and V_{DD} and reduce the load capacitance (C_L).

Another important issue of CMOS inverter is power consumption. The power consumption can be expressed in Eq. (4-2).

$$E = \text{Energy / transition} = \frac{1}{2} \times C_L \times V_{dd}^2 \quad (4\text{-}1)$$

$$P = \text{Power} = 2 \times f \times E = f \times C_L \times V_{dd}^2 \quad (4\text{-}2)$$

f : cycle / sec

The output is the opposite of the input is an ideal model of inverter. However, in order to make a low power consumption inverter, load capacitance (C_L), work frequency and V_{DD} need to be reduced. However, the power is a function of frequency, as shown in Eq. (4-2). So considered the trade off of power

consumption and time delay, increase of W/L implies the larger size, and V_{DD} increase results in more power dissipation.

NMOS logic also can be the CMOS inverter. However, the resistance cause more power consumption when V_{dd} is high, as shown in Fig. 4-9. For our devices, increasing W/L of the ambipolar TFT near drain side can reduce the resistance achieve low power consumption.

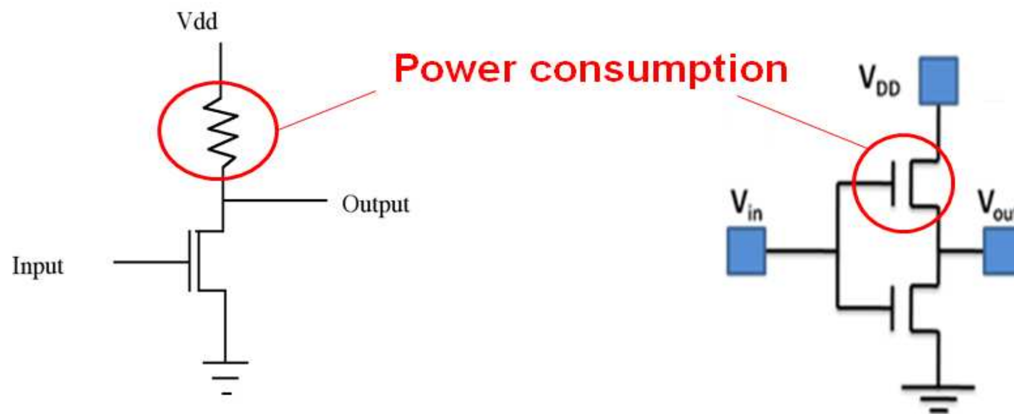


Fig. 4-9 Power consumption issue from NMOS logic and CMOS-like inverter

Chapter 5

Conclusion
And Future Works

5.1 Conclusions

In this study, we fabricated ambipolar TFTs through a hybrid route by combining organic/oxide semiconductors. These ambipolar TFTs can be a CMOS-like inverter circuit. The contributions of this study are: (1) Largest gain and fastest operation frequency are achieved in CMOS-like inverter. (2) leading the researches regarding to the CMOS-like inverter composed of a-IGZO and pentacene.

First of all, in order to control the electrical characteristics of a-IGZO TFTs, optimization by adjusting oxygen/argon ratios during RF sputter and adjustment of post-annealing conditions were required. Annealing time over than 2 hour; TFTs do not exhibit an appreciable characteristic. One hour is the best time duration of annealing process for our device with 100-nm thick thermally grown oxide layer as the insulator. Both n channel and p channel behaviors of the ambipolar TFTs were analyzed together with their

corresponding inverter circuits. The optimal thicknesses of a-IGZO layer and pentacene layer were found to be 40nm and 30nm, respectively. The initial inverter showed a high voltage gain about 70 under the supply voltage (V_{DD}) of 50V. Dynamic behavior of the inverter at 20 Hz rising (t_r) time and falling times (t_f) were measured to be about ~2ms and 0.9 ms, respectively. The largest gain and fastest dynamic behavior were achieved in our COMS-like inverter.

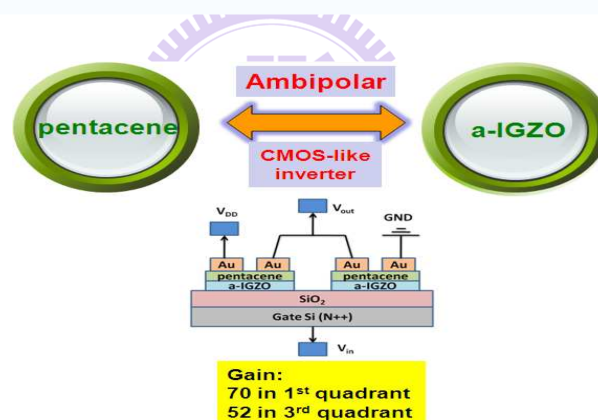


Fig. 5-1 CMOS-like inverter achievements

Overall, a-IGZO/pentacene TFTs exhibits an ambipolar behavior with balanced field effect mobility and qualifies themselves as promising candidates

for the applications in AMFPDs. Table 5-1 compares our latest results (the gain value of 70) and similar studies reported elsewhere. [12, 22].

Table 5-1 Summary & comparison for ambipolar TFTs and inverters

Inverter Comparison	APL 2008 Vol. 93, 033306 NCKU	APL 2008 Vol. 93, 213505 U. of Tokyo	2008 Submitted to SID09 NCTU
TFT type	Ambipolar	P-type + N-type	Ambipolar
Inverter	CMOS-like	CMOS	CMOS-like
P- type TFT	pentacene	pentacene	pentacene
N-type TFT	In_2O_3	a-IGZO	a-IGZO
Gain (dV_{out}/dV_{in})	9	56	**70**
Operation quadrant	1+3	1	1+3
Process	Easy	Complex	Easy

5.2 Future Works

Using platinum (Pt) as the electrodes and buffer layer between active layer and insulator is a way to enhance hole's transport. Platinum enables both n-type and p-type characteristics for a-IGZO at the same time. The fabrication process can be simplified.

Operating voltage, output frequencies, and gain values of CMOS-like inverter will be further studied and optimized. These ambipolar TFTs open a viable way to fabricate high performance logic devices with mechanical flexibility and good reliability in air ambient.

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