國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

鋯酸鍶基電阻轉換記憶元件之特性研究

Characteristics of Resistive Switching in Strontium Zirconate Based Memory Devices

研 究 生：林 群 傑

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博 士 論 文

A Dissertation
Submitted to Department of Electronics Engineering
and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy

in Electronics Engineering

July 2007

Hsinchu, Taiwan, Republic of China

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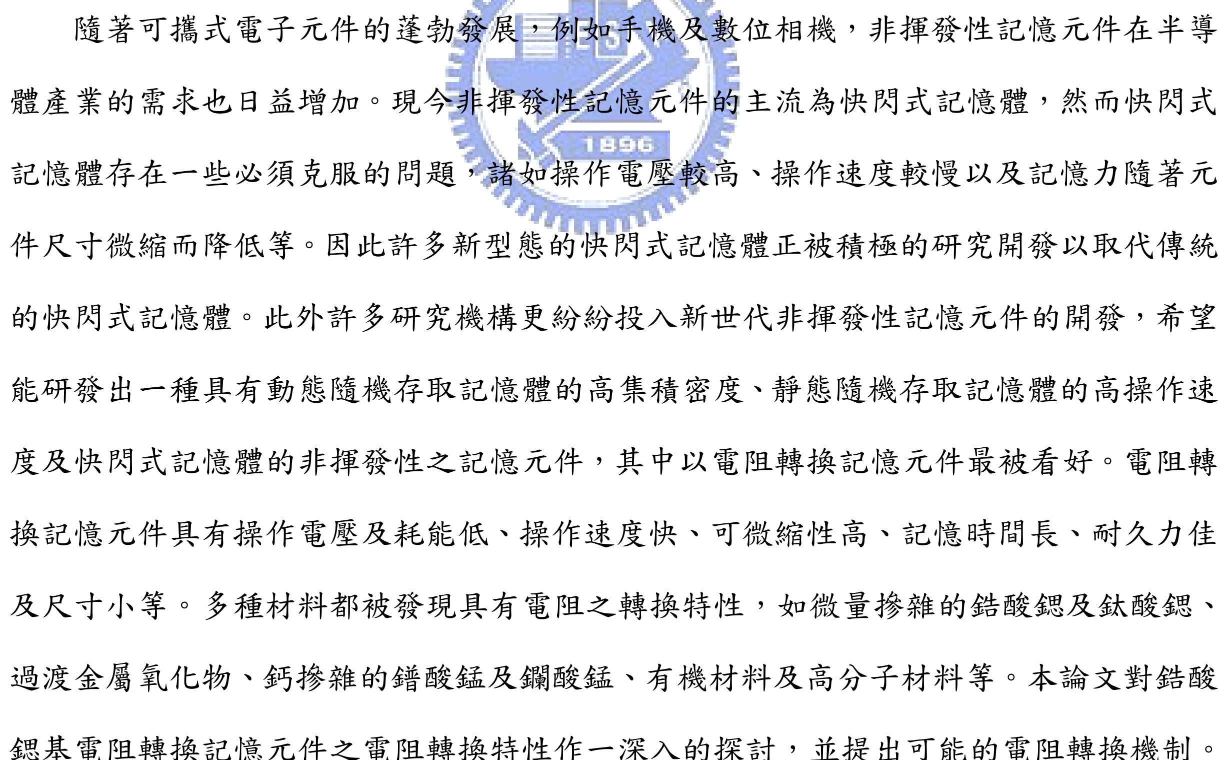
摘要



隨著可攜式電子元件的蓬勃發展，例如手機及數位相機，非揮發性記憶元件在半導體產業的需求也日益增加。現今非揮發性記憶元件的主流為快閃式記憶體，然而快閃式記憶體存在一些必須克服的問題，諸如操作電壓較高、操作速度較慢以及記憶力隨著元件尺寸微縮而降低等。因此許多新型態的快閃式記憶體正被積極的研究開發以取代傳統的快閃式記憶體。此外許多研究機構更紛紛投入新世代非揮發性記憶元件的開發，希望能研發出一種具有動態隨機存取記憶體的高集積密度、靜態隨機存取記憶體的高操作速度及快閃式記憶體的非揮發性之記憶元件，其中以電阻轉換記憶元件最被看好。電阻轉換記憶元件具有操作電壓及耗能低、操作速度快、可微縮性高、記憶時間長、耐久力佳及尺寸小等。多種材料都被發現具有電阻之轉換特性，如微量摻雜的鋯酸鍶及鈦酸鍶、過渡金屬氧化物、鈣摻雜的鐠酸錳及鑭酸錳、有機材料及高分子材料等。本論文對鋯酸鍶基電阻轉換記憶元件之電阻轉換特性作一深入的探討，並提出可能的電阻轉換機制。

本論文之第一章為記憶體簡介，並深入的介紹電阻轉換記憶元件。第二章為實驗步驟，本論文所述之所有元件製備及量測分析方法，均在此章有詳細的說明及介紹。第三章介紹以鎳酸鑭為底電極及以鋁為頂電極之鋯酸鍶基電阻轉換記憶元件之電阻轉換特

性，此結構之元件具有電壓極性之電阻轉換特性，施加負電壓於頂電極可將元件之電阻值由高電阻狀態轉換至低電阻狀態，而施加正電壓於頂電極可將元件轉換回原本的高電阻狀態。本章亦對掺雜濃度對電阻轉換記憶元件之特性作一探討，發現適當的掺雜濃度可將電阻轉換記憶元件之特性最佳化。研究的結果顯示，具有百分之 0.3 釩掺雜的鋯酸鍶基電阻轉換記憶元件具有最佳的電阻轉換特性，例如兩個電阻狀態的比值高達一萬倍；元件的記憶能力長達一年以上。此外該元件在攝氏 100 度下操作仍具有極佳的穩定性。

第四章介紹以白金為底電極、鎳酸鑭為緩衝層及以鋁為頂電極之鋯酸鍶基電阻轉換記憶元件之電阻轉換特性，此結構元件之電阻轉換沒有電壓極性，亦即該元件可藉由施加正電壓或負電壓使它改變其電阻值。由研究結果顯示，無電壓極性之電阻轉換為鋯酸鍶基電阻轉換記憶元件之本質特性，而電極的選擇將限制某個電壓方向之電阻轉換，進而成為有電壓極性之電阻轉換行為。此元件利用高導電率的白金作為底電極，並成長具有(100)及(200)方向之鎳酸鑭作為緩衝層，而成長於上的鋯酸鍶電阻層亦具有(100)及(200)之優選方向，有該優選方向之鋯酸鍶薄膜已被研究具有極佳的電阻轉換特性。此外由於底電極的導電率佳，因此該元件之操作電壓可小於 7 伏特，且操作速度可高達 10 奈秒。該元件的電阻比值更高達一千萬倍；元件的記憶能力長達八個月以上。此外該元件在攝氏 150 度下操作仍具有極佳的穩定性。

由各方的研究得知，鋯酸鍶基電阻轉換記憶元件之電阻轉換機制為導電路徑的形成與破壞，當導電路徑形成時即為低電阻狀態，而當導電路徑被打斷時即為高電阻狀態，而導電路徑的形成與破壞與鋯酸鍶薄膜中的缺陷有關。低電阻狀態及高電阻狀態的導電機制分別為 Ohmic 及 Frenkel-Poole 機制，由此可證明電阻的轉換發生於鋯酸鍶薄膜內部，而非發生於界面層。

鋯酸鍶基電阻轉換記憶元件具有良好的電阻轉換特性，例如操作電壓及耗能低、操作速度快、記憶時間長及結構簡單等。因此鋯酸鍶基電阻轉換記憶元件是有可能取代動態隨機存取記憶體、靜態隨機存取記憶體及快閃式記憶體之新世代非揮發性記憶元件。

最後為本文之總結，並對未來可行的研究工作作一具體之建議。

Characteristics of Resistive Switching in Strontium Zirconate Based Memory Devices

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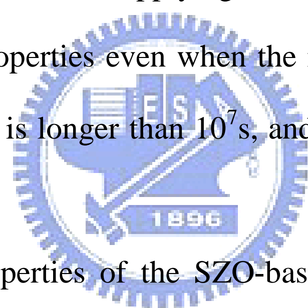
Abstract

Due to the popularity of portable equipment, such as mobile phone and MP3 player, the requirements of nonvolatile memory (NVM) increase significantly in the semiconductor industry. The mainstream of NVM nowadays is the Flash memory; however, the Flash memory has some issues such as high operation voltage, low operation speed, and poor retention time and coupling interference effect during the memory scaling down. Therefore, some new-type Flash memories, such as charge-trapping (SONOS) Flash and band-engineered SONOS Flash are studied to replace the traditional Flash memory. Besides, researchers are eagerly finding one kind of next-generation NVM possessing the advantages of high density, high speed, and nonvolatility of DRAM, SRAM, and Flash memory, respectively. One of the promising candidates of next-generation NVMs is the resistive random access memory (RRAM) owing to its low operation voltage and power, high operation speed, high scalability, good endurance, small size, etc. Resistive switching properties have been observed in many kinds of materials, such as doped $SrZrO_3$ (SZO) and doped $SrTiO_3$, transition metal oxides, $Pr_{1-X}Ca_XMnO_3$ and $La_{1-X}Ca_XMnO_3$, and organic and

polymer materials. In this dissertation, the resistive switching properties and mechanisms of the SZO-based memory devices are studied in depth.

In this dissertation, Chapter 1 introduces the memories, especially for the RRAM. Chapter 2 shows the experimental procedures of the devices indicated in this dissertation. Chapter 3 presents the properties of the SZO-based memory devices with $LaNiO_3$ (LNO) bottom electrode and Al top electrode (Al/SZO/LNO, ERE devices), which have bipolar resistive switching characteristics. The doping effects of the SZO-based ERE devices are investigated, indicating that a proper concentration of doping into the SZO film can improve the resistive switching properties, such as resistance ratio and stability. The resistance ratio between high resistance state (HRS) and low resistance state (LRS) of the 0.3%-V:SZO ERE device is over 10^4, and retains 1000 after applying 100 voltage sweeping cycles. This device has stable resistive switching properties even when the measurement is performed at 100^oC. The retention time of the device is longer than 10^7s, and the nondestructive readout property of the device is also examined.



Chapter 4 presents the properties of the SZO-based memory devices with Pt bottom electrode, LNO buffer layer, and Al top electrode (Al/SZO/LNO/Pt, ERBE devices), which possess nonpolar resistive switching characteristics. The nonpolar switching is considered as an intrinsic property of the SZO-based memory devices, while the electrode materials employed in the devices would determined the resistive switching polarities. The operation voltages of the 0.3%-V:SZO ERBE device are less than 7V, and the resistance ratio of the device is higher than 10^7. This device with Pt bottom electrode has lower resistive switching voltages and higher resistance ratio comparison with the 0.3%-V:SZO ERE device with LNO bottom electrode. The resistive switching speed of the 0.3%-V:SZO ERBE device is 10ns, which is the fastest speed in comparison with that of the previous reports. The device has stable resistive switching properties even when the measurement is performed at 150^oC. The nondestructive readout property of the device is also demonstrated, and the retention time of

the device is longer than 10^7s.

The resistive switching mechanism of the SZO-based memory devices are considered as the formation and disruption of the current paths, which possibly attributed to the storage and release of electrons in the trap states of the SZO film. The conduction mechanisms of both LRS and HRS currents of the SZO-based memory devices are dominated by Ohmic conduction and Frenkel-Poole emission, respectively.

Consequently, the SZO-based memory device with good resistive switching characteristics including low operation voltage, low power consumption, high operation speed, long retention time, nondestructive readout, and simple structure is a promising candidate for next-generation NVM applications.

Finally, the experimental results and discussion are summarized in chapter 5. Some suggestions for future work are also provided in this chapter.

誌　謝

竹湖晨風輕拂，我的心思卻異於往常的紊亂，長達二十一年的學生生涯即將結束，裝滿心裡的是深深的感謝與祝福。首先要感謝母校提供我最理想的求學環境，讓我能不間斷的吸收陽光與溫暖，讓我能盡情的成長，我以身為交大人為榮。

玉樹康莊向榮，能夠順利完成博士學位，最感謝的人是指導教授曾俊元老師，您的鼓勵與提攜是最可貴的記憶，您秉持嚴格訓練的精神，讓我能養成嚴謹的態度，並在我遭遇挫折時不斷給我鼓勵，讓我能繼續堅持下去。也感謝華邦電子林晨曦副總經理的指導與建議，與各位口試委員多次的論辯與指正，讓這一份艱難的工作能更趨完美。

荷塘月光皎潔，感謝如明月般的周景揚教授、汪大暉教授、陳明哲教授、黃調元教授、雷添福教授、陳茂傑教授、崔秉鉞教授、羅正忠教授、林振德教授、裘性天教授等等，感謝您們無論在學業上的指導與生活上的照顧，以及做人處事方面的叮嚀。

西亭晚霞笑語，感謝秀玉學姊、加星學長、思毅學長、志益學長、佳穎學姊、豊文等等，感謝你們不厭其煩的指導我，讓我無論在做實驗、分析數據及撰寫論文上都能得心應手。也感謝洋ㄟ、杜比、猛男、僑生、蟲哥、影帝、小尤等等學弟們，沒有大家的合力演出，也沒有此時謝幕的掌聲，我的記憶裡永遠保存大家半夜趕實驗的瘋狂，永遠記得彼此失落時互相鼓勵的場景，也永遠記得我們曾經豪氣的歲月，我們是獨一無二的團隊，也是永遠的夥伴，祝福你們都能一帆風順，比我更快畢業。

掌聲響起，而幕永不落下，我願將所有的掌聲與榮耀，都獻給我最摯愛父母親與家人，感謝您們對我的付出、包容與無止盡的愛，這才是我能順利完成博士學位的原動力。

群傑 2007 夏

於 交通大學 新竹

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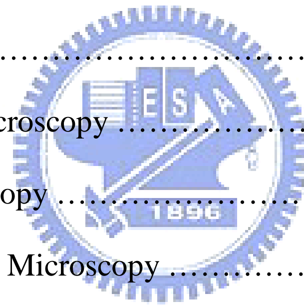

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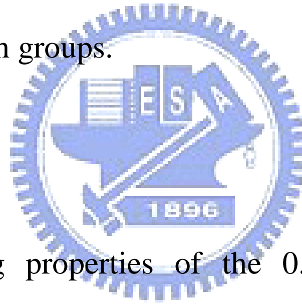

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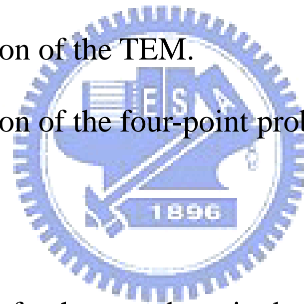

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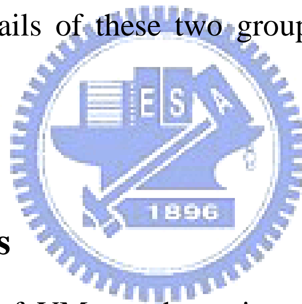
Chapter 1

Introduction

1.1 Introduction to Memories

Memories can be classified into two groups according to their volatility. The first group is the volatile memory (VM). The most important feature of the VM is that the stored data loses immediately as soon as the system is turned off. In other words, it requires a constant power supply to maintain its stored information. The second group is nonvolatile memory (NVM), whose stored data can be retained for a long time without any power supply. The details of these two groups of memories are discussed in the following sections.



1.1.1 Volatile Memories

Two main kinds of VM are dynamic random access memory (DRAM) and static random access memory (SRAM). The DRAM and SRAM cells are shown in Figs. 1-1 and 1-2, respectively. The size of a DRAM cell consisting of one transistor and one capacitor (1T1C) is very small (6-12F^2) [1], so the density and capacity of DRAM is very high. However, to repeatedly refresh each DRAM cell is necessary to retain the stored information, or the stored data will lose within a few milliseconds. A SRAM cell (50-80F^2) which consists of six transistors is more complicated than the DRAM cell [1], so the cost of SRAM is higher than that of DRAM. In addition, the operation speed of SRAM is much higher than that of DRAM due to the refresh process is not needed for the SRAM. Hence, the SRAM with high operation speed is usually used as a computer cache memory.

1.1.2 Nonvolatile Memories

Due to the popularity of portable equipment, such as mobile phone and MP3 player, the requirements of NVMs increase significantly in the semiconductor industry. An ideal NVM includes the properties of low operation voltage, low power consumption, high operation speed, high endurance, long retention time, nondestructive readout, simple structure, small size, low cost, etc [1]. However, there is no one kind of NVM possessing all of the above properties up to now.

The mainstream of NVM nowadays is Flash memory, containing the NOR Flash and NAND Flash. The NOR Flash has higher operation speed, which is suitable for use of computer coding memory. On the other hand, the NAND Flash with higher density is used for data storage memory. A typical memory cell of the Flash memory is consisted of one MOSFET-like transistor with one floating gate as shown in Fig. 1-3. The logic high or low is determined by charges stored in the floating gate or not, which alter the threshold voltage of the MOSFET-like transistor.

However, the Flash memory has some issues such as high operation voltage, low operation speed, and poor retention time and coupling interference effect during the memory scaling down [2]. Therefore, some new-type Flash memories, such as charge-trapping (SONOS) Flash and band-engineered SONOS Flash are studied to replace the traditional Flash memory. Besides, researchers are eagerly finding one kind of next-generation NVM possessing the advantages of high density, high speed, and nonvolatility of DRAM, SRAM, and Flash memory, respectively. Four possible candidates for next-generation NVMs, including ferroelectric random access memory (FeRAM) [3]-[5], magnetoresistive random access memory (MRAM) [6]-[8], phase change random access memory (PCRAM) [9]-[14], and resistive random access memory (RRAM) [1], [15]-[110], are discussed in detail in Sec. 1.2.

1.2 Introduction to Next-generation Nonvolatile Memories

1.2.1 Ferroelectric Random Access Memory

A material with a spontaneous polarization and the polarization can being altered by applying an electric field is called it ferroelectric material. A typical structure of the ferroelectric material is the ABO_3 structure (perovskite structure) as shown in Fig. 1-4, where the A, B, and O atoms are located at corner, body center, and face center of the cubic, respectively. When an electric field is applied to the ferroelectric material, the B atom with two thermodynamically stable positions is located depended on the polarity of the applied electric field. The polarization hysteresis curve of the ferroelectric material is shown in Fig. 1-5. The hysteresis phenomenon of ferroelectric material can be used for NVM applications called it FeRAM. The FeRAM can be subdivided into two types. The first type is the metal-ferroelectric-semiconductor FET (MFSFET) structure as shown in Fig. 1-6. The structure is very similar to the MOSFET except the oxide film is replaced by the ferroelectric film. The polarizations (+Pr or -Pr) of the ferroelectric film will affect the drain current of the transistor, and the memory effect of the MFSFET type FeRAM is nonvolatile and with nondestructive readout property. The second type is the DRAM-like 1T1C structure similar to Fig. 1-1, where the dielectric of the capacitor is replaced by the ferroelectric film. The polarizations of the ferroelectric film will also affect the current of the device. The memory effect of the DRAM-like FeRAM is also nonvolatile; however, the read process is destructive and needing a re-write process.

1.2.2 Magnetoresistive Random Access Memory

The basic MRAM cell is the magnetic tunneling junction which consists of two magnetic layers sandwiching a thin tunneling layer as shown in Fig. 1-7. The

magnetization of one magnetic layer (reference layer) is fixed and kept in a specific direction. The other layer (storage layer) can be switched to parallel or antiparallel to the reference layer by applying a specific magnetic field. The logic high or low is determined by the resistance of parallel or antiparallel state. In read process, a small current flowing through the tunneling layer is detected to recognize the resistance states. The MRAM with nonvolatility like Flash memory, high operation speed like SRAM, and high density like DRAM seems a possible candidate for the next-generation NVM. However, the reliability of the tunneling layer and the limitation during the device scaling is the most important challenge of MRAM.

1.2.3 Phase Change Random Access Memory

The PCRAM, also named it phase change memory (PCM) or ovonic unified memory (OUM), is a promising technology to meet the requirements of the ideal NVM. The basic memory cell of PCRAM is shown in Fig. 1-8 [10], where the GeSbTe (GST) chalcogenide alloy material has been adopted as a primary material of the PCRAM. The PCRAM utilizes two different structural phases of the GST, amorphous and polycrystalline, for data storage. In reset process, a high magnitude current pulse with short trailing edge is applied on the programmable volume of the phase change material. The temperature of the material exceeds the melting point which eliminates the polycrystalline order in the volume. When the reset pulse is terminated, the device cools to “freeze in” the amorphous structure. This cooling time about several nanoseconds is determined by the thermal environment of the device, and the fall time of the reset pulse. In set process, a moderate magnitude current pulse with sufficient duration is applied to maintain the device temperature for crystal growth. The amorphous structural state [high resistance state (HRS)] or the polycrystalline structural state [low resistance state (LRS)] is read by applying a

low magnitude and long duration current pulse. The time-temperature relationship of the PCRAM is shown in Fig. 1-9 [10]. During the set and reset processes, large Joule heating is applied on the phase change material, and hence, huge power is consumed. How to reduce the power consumption during the PCRAM operation is a significant challenge of the PCRAM.

1.2.4 Resistive Random Access Memory

Resistive switching properties have been observed in many kinds of materials, such as transition metal oxides and perovskite oxides. The resistance of the material can be switched to another stable value by applying an electric signal, such as sweep voltage or voltage pulse, and it can be switched back to the original value by applying another electric signal. Table 1-1 performs the comparison with the Flash memory and next-generation NVMs [1]. This table shows that the RRAM with low operation voltage and power, high operation speed, high scalability, good endurance, small size, etc., which is the most potential candidate of next-generation NVM. The details of the RRAM such as structures, materials, operation methods, and possible resistive switching mechanisms are discussed in Sec. 1.3.

1.3 Introduction to Resistive Random Access Memory

1.3.1 Structures

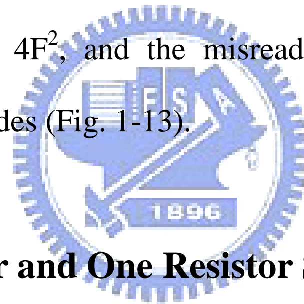
- **Cross-point Memory Array**

The simplest structure of RRAM is the cross-point memory array shown in Fig. 1-10 [15]. The memory materials are sandwiched between two sets of electrodes, which form an electrode/resistor/electrode (ERE) structure. This structure results in a minimum cell size of $4F^2$. Besides, a stack of cross-point memory array can

reduce the minimum cell size to 4 F^2/n for n layers stacking as shown in Fig. 1-11 [15]. However, the cross-point memory array has a serious problem of misread. Fig. 1-12 describes the misread of the cross-point memory array [16]. For instance, the resistance of (3, 3) cell is misread from HRS to LRS because the read current flows through 3 neighboring cells which were switched to LRSs. Therefore, one diode and one resistor (1D1R), and one transistor and one resistor (1T1R) structures are developed and discussed in the following sections.

- **One Diode and One Resistor Structure**

The basic circuit diagram and the cross section view schematic diagram of the 1D1R structure are shown in Figs. 1-13 and 1-14, respectively. In this structure, the minimum cell size is $4F^2$, and the misread problem can be prevented by the combination of the diodes (Fig. 1-13).



- **One Transistor and One Resistor Structure**

The 1T1R structure of RRAM is depicted in Figs. 1-15 and 1-16 [17], where the transistor and the ERE device are fabricated in the front-end and back-end of the conventional CMOS process, respectively. The minimum cell size of the 1T1R structure is $6F^2$. Besides, some improved structures based on these three structures are also proposed, such as plug electrodes. Fig. 1-17 performs the plug bottom electrode (BE) of the ERE device. Baek *et al.* had demonstrated that the uniformity of resistive switching can be improved by using the plug electrodes [16].

The ERE device is the key element of RRAMs, so we mainly focus on the ERE device (Chapter 3) and its modification (Chapter 4) in this dissertation.

1.3.2 Operation Method

The operation methods of RRAM including write (turn-on), erase (turn-off), and read are discussed in this section and shown in Fig. 1-15. To write or erase the selected resistor, a specific electric signal is applied on the bit line (BL). A tiny electric signal, which cannot switch the resistor, is applied on the BL for reading the resistance value of the selected cell.

1.3.3 Material Groups

Resistive switching properties have been observed in many kinds of materials, such as doped $SrZrO_3$ (SZO) and doped $SrTiO_3$ (STO) [18]-[40], transition metal oxides [16], [17], [41]-[76], $Pr_{1-X}Ca_XMnO_3$ (PCMO) and $La_{1-X}Ca_XMnO_3$ (LCMO) [1], [22], [77]-[99], and organic and polymer materials [15], [100]-[110]. For example, Beck *et al.* proposed that the Cr-doped SZO can switch its resistance value by applying a sweep voltage or voltage pulse [18]. The multilevel switching was also demonstrated in this paper [18]. Seo *et al.* proposed that the polycrystalline NiO possesses the resistive switching behavior in proper growth ambiance [41]. They also demonstrate the effect of the area of top electrode (TE) [42]. Liu *et al.* demonstrated the electric-pulse-induced reversible resistance change effect in PCMO [77]. Unlike the PCRAM, there is no polycrystalline-amorphous phases transition in these materials. In this dissertation, the resistive switching properties and mechanisms of the SZO-based memory devices such as retention time and endurance are studied in depth.

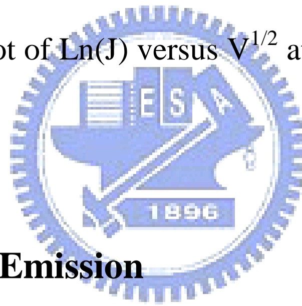
1.3.4 Conduction Mechanisms

The resistive switching mechanisms of each RRAM material are not clearly understood up to now. Therefore, the conduction mechanisms of each resistance

state of the RRAM device are studied for further understanding of the resistive switching mechanisms in each RRAM material. In this section, six basic conduction mechanisms in insulator are summarized in Table 1-2 [111] and discussed in follows.

● Schottky Emission

The Schottky emission is caused by thermionic emission of carriers across the interface between metal and insulator or between insulator and semiconductor [111]. Therefore, the Schottky emission is also named it thermionic emission. If carriers transport in an insulator is by this mechanism, a plot of $Ln(J/T^2)$ versus 1/T in a specific voltage is a straight line, and the slope can determine the permittivity of the insulator. Besides, a plot of Ln(J) versus $V^{1/2}$ at a fixed temperature is also a straight line.



● Frenkel-Poole Emission

The Frenkel-Poole (F-P) emission is due to field-enhance thermal excitation of trapped electrons into the conduction band [111]. For the F-P emission, plots of Ln(J) versus 1/T in a specific voltage and Ln(J/V) versus $V^{1/2}$ at a fixed temperature are straight lines. The quantity $\sqrt{q/\pi\varepsilon_i}$ of Schottky emission is a half than that of F-P emission due to the Schottky effect (image-force-induced lowering effect) [112], and the F-P emission is highly relative to the trap density of the insulator.

● Tunnel or Field Emission

The tunnel or field emission corresponds to electrons tunneling from the metal Fermi energy into the insulator conduction band or field ionization of trapped

electrons into the conduction band [111]. This emission is strongly dependent on the applied voltage, but is essentially independent on the temperature. A plot of Ln(J/V^2) versus 1/V is a straight line in this conduction mechanism.

- ### Space-charge-limited Current

The space-charge-limited current (SCLC) is caused by carriers injected into the insulator and no compensation charge is present [111]. The density of SCLC is direct proportion to V^2, and is essentially independent on the temperature.

- ### Ohmic Conduction

The Ohmic conduction is results from thermally excited electrons hopping from one isolated state to the next state [111]. If carriers transport in an insulator is by this conduction, plots of Ln(J) versus Ln(V) at a fixed temperature and Ln(J) versus 1/T in a specific voltage are straight lines with unity slope.

- ### Ionic Conduction

The ionic conduction is similar to a diffusion process. In this mechanism, the voltage and current dependence is the same with the Ohmic conduction at a fixed temperature, and a plot of Ln($J \times T$) versus 1/T in a specific voltage is a straight line with unity slope. In addition, each conduction mechanism may dominate in some voltage and temperature ranges, and there are possibly two or more mechanisms causing the conduction in an insulator.

1.3.5 Resistive Switching Mechanisms

The resistive switching properties have been proposed in many RRAM materials with some similar or different characteristics; however, the resistive

switching mechanisms of each material are not clearly understood and explained so far. The reasons of resistive switching can be roughly classified into three types, including charge transfer, modulation of Schottky barrier, and formation and rupture of conducting paths. Besides, some possible resistive switching mechanisms proposed by several well-known research groups and companies are also discussed in this section.

- **Charge Transfer**

The first type of resistive switching mechanisms is causing by the charge transfer, such as trapping and detrapping of trap states, and changes in valences. Based on these mechanisms, the resistive switching occurs in the bulk resistive layer.

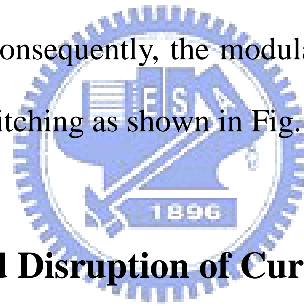
Odagawa [National Institute of Advanced Industrial Science and Technology (AIST), Japan] *et al.* proposed that the resistive switching in PCMO film with Ohmic contacted with Pt and Ag electrodes is ascribed to trapping and detrapping of carriers (holes), due to the currents of the PCMO-based device follow the trap-controlled SCLC [82]. Chen (Spansion) *et al.* proposed that the resistive switching of the Cu_xO-based ERE device is corresponded to carriers trapped and detrapped in deep traps. In this device, a dramatically increased current occurs while the deep traps are filled. The retention time is determined by the thermal release time of deep traps [53].

Beck (IBM) *et al.* reported that the resistive switching in Cr-doped SZO-based device is due to the transformation of the valences (Cr^{3+} and Cr^{4+}) [18]. In this study, the transitional element (Cr) is doped into the SZO film to form some energy gap states. Applying an electric signal on the device can change the valences of the dopants, and then the energy level of the dopants is also changed. Hence, this

changing of energy level can cause the resistive switching in the RRAM material.

- **Modulation of Schottky Barrier**

The second type of resistive switching mechanism is causing by the modulation of the Schottky-like barrier. Sawa (AIST, Japan) *et al.* reported that resistive switching in PCMO film with Ti and $SrRuO_3$ (SRO) electrodes is ascribed to the modulation of the Schottky-like barrier in the PCMO film near the Ti electrode [22], [80]. In this study, applying a positive voltage on Ti (reverse bias) causes the electrons accumulating into the interface states, and hence raises the height and/or width of the Schottky-like barrier. In addition, applying a forward bias leads to the electrons extracting from the interface states, and lowers the barrier height and/or width. Consequently, the modulation of the Schottky-like barrier can lead to the resistive switching as shown in Fig. 1-18 [22].



- **Formation and Disruption of Current Paths**

The third type of resistive switching mechanism is causing by the formation and disruption of current paths. Based on this mechanism, the resistive switching occurs in the bulk resistive layer. Liu (University of Huston) *et al.* proposed that the resistive switching in the PCMO-based device is ascribed to the formation and disruption of current paths [77]. These paths are formed by applying a positive voltage pulse, and ruptured by applying a negative voltage pulse. Similarly, Seo (Samsung) *et al.* reported the formation and disruption of current paths in the NiO-based device [42]. However, the reasons of formation and disruption of current paths are still controvertible. The possible reasons are the nucleation and dissolution of metallic or carbon clusters, traps trapping and detrapping, formation and disruption of grain boundaries, etc.

Besides, the resistive switching mechanisms should be related to the materials used and structures of the devices, and could also be related to the fabricating methods of the devices, which may lead to different defect densities.

1.3.6 Resistive Switching Polarities

The resistive switching properties can be divided into two types based on the resistive switching polarities. First, Fig. 1-19 perform the typical current-voltage (I-V) curves of the bipolar resistive switching. For example, applying a positive voltage can switch the device from HRS to LRS, and applying an opposite (negative) voltage can switch the device back to HRS [Fig. 1-19(a)], and vice versa [Fig. 1-19(b)]. Second, Fig. 1-20 shows the typical I-V curve of nonpolar resistive switching. Nonpolar switching means that the device can be switched to another state by applying an electric signal regardless of the directions. In other words, applying one positive (negative) voltage can switch the device to LRS, and applying another positive (negative) voltage can switch the device back to HRS.

1.3.7 Criteria

For the industrial application of RRAM, there are some criteria should be taken into consideration described in follows.

- **Operation Voltage**

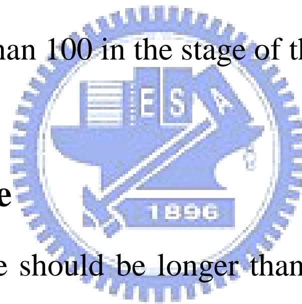
The resistive switching voltage smaller than 10V is anticipated. The large operation voltage of Flash memory is considered as a drawback for application. A large operation voltage will result large power consumption and cause a reliability issue.

- **Operation Speed**

Generally, the higher the operation speed is the better the device performance. The operation speed of Flash memory is about 1ms so far. Therefore, in order to replace the Flash memory, the operation speed of the RRAM should be less than 1ms. In addition, the operation speed should be less than 10ns for replacing the DRAM.

- **Resistance Ratio**

The larger the resistance ratio is the better the device performance. The larger resistance ratio will provide a larger sensing margin to read the stored data. The resistance ratio should be larger than 5 at least for accurate sensing; however, the ratio should be larger than 100 in the stage of thin film deposition.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- **Retention Time**

The retention time should be longer than 10 years at room temperature (RT). Up to now, the reported results of RRAM are about several months at RT. Besides, a thermal acceleration test is also used for testing the retention time of RRAM.

- **Nondestructive Readout**

The specification of nondestructive readout is that the stored information can be read for 10^{12} times without any degradation.

- **Endurance**

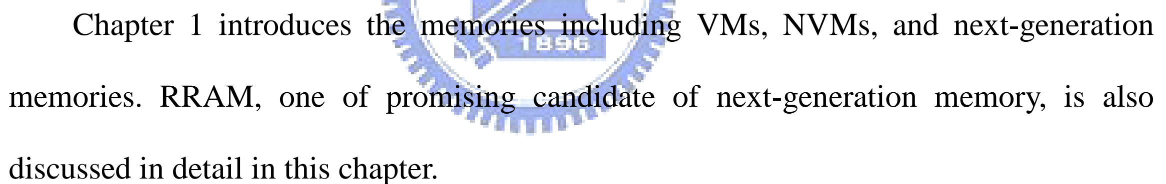
The endurance should be larger than 10^{6} for replacing the Flash memory, and be larger than 10^{12} for replacing the DRAM.

- **Resistance Value**

The specification of the resistance value of LRS is about 1~100kΩ. For instance, the current density of RRAM device should be 10^5~10^7 A/cm^2 for the device area of 0.01 μm^2. However, there are a few reported results satisfy this requirement.

- **Multilevel Switching**

Some RRAM materials have been reported that they have multilevel switching properties. The multilevel memory states can improve the density and capacity of RRAM.



1.4 Outlines of This Dissertation

Chapter 1 introduces the memories including VMs, NVMs, and next-generation memories. RRAM, one of promising candidate of next-generation memory, is also discussed in detail in this chapter.

Chapter 2 presents the experimental procedures and the techniques used in this dissertation to characterize the electrical and physical properties of the RRAM devices.

Chapter 3 presents the bipolar resistive switching properties of the SZO-based ERE device. The conduction mechanisms of each resistance state and the possible resistive switching mechanisms are discussed in this chapter. In addition, the electrical and physical properties, such as crystallization, retention time, endurance, and nondestructive readout properties, are also demonstrated.

Chapter 4 discusses the nonpolar resistive switching properties of the SZO-based electrode/resistor/buffer/electrode (ERBE) device. The electrical and physical properties of this device are presented in this chapter.

Chapter 5 is the conclusions of this dissertation and the suggestions of future work.

1.5 Value of This Dissertation

RRAM is the most promising candidate of next-generation NVM. In this dissertation, the resistive switching characteristics of the SZO-based ERE and ERBE devices are carefully investigated in detail. The results show that the SZO-based devices possess excellent properties including high operation speed, low operation voltage and power consumption, nondestructive readout, long retention time, simple structure, etc. In addition, the conduction and possible resistive switching mechanisms are also demonstrated in this dissertation, which could assist us and other researchers to improve the reliability and performance of the SZO-based RRAM device.

Table 1-1 Comparison with the Flash memory and next-generation NVMs [1].

Function	DRAM	SRAM	Flash	OUM	MRAM	RRAM
Non-volatility	No	No	Yes	Yes	Yes	Yes
Program power	Low	Low	High	Low	High	Low
Program voltage	Lo1	Lo1	High		Medium	Low
Read dynamic margin	100-200mV	100-200mV	Delta Current	10X – 100X	20 – 40%	10X – 1000X
Write - Erase time	50ns - 50ns	8ns - 8ns	1μs – 1-100ms	10ns - 50ns	30ns - 30ns	10ns - 30ns
Read time	50ns	8ns	50ns	20ns	30ns	20ns
Program energy	Medium	High	High	Low	Medium	Low
Multi-bit storage	No	No	Yes	Yes	No	Yes
Scalability limits	Capacitor	6T	T-Ox/HV	Litho	Current	Litho
Endurance	∞	∞	10^{12}	$>10^{12}$	$?10^{15}$	$?10^{15}$
Cell size (F^2)	6-12	50-80	7-11	5-8	?	4

Table 1-2 Basic conduction mechanisms in insulator [111].

mechanism	expression	voltage and temperature dependence
Schottky emission	$J = A^* T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_i}\right)}{kT}\right]$	$J \sim T^2 \exp\left(+a\sqrt{V}/T - q\phi_B/kT\right)$
F-P emission	$J \sim E \exp\left[\frac{-q\left(\phi_B - \sqrt{qE/\pi\varepsilon_i}\right)}{kT}\right]$	$J \sim V \exp\left(+2a\sqrt{V}/T - q\phi_B/kT\right)$
tunnel or field emission	$J \sim E^2 \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E}\right]$	$J \sim V^2 \exp(-1/V)$
SCLC	$J = \frac{9\varepsilon_i \mu V^2}{8d^3}$	$J \sim V^2$
Ohmic conduction	$J \sim E \exp(-\Delta E_{ae}/kT)$	$J \sim V \exp(-1/T)$
ionic conduction	$J \sim \frac{E}{T} \exp(-\Delta E_{ai}/kT)$	$J \sim \frac{V}{T} \exp(-1/T)$

A^* =effective Richardson constant, ϕ_B =barrier height, E =electric field, ε_i =insulator dynamic permittivity,

m^* =effective mass, d =insulator thickness, ΔE_{ae} =activation energy of electrons, ΔE_{ai} =activation energy of ions,

and $a = \sqrt{q/4\pi\varepsilon_i d}$.

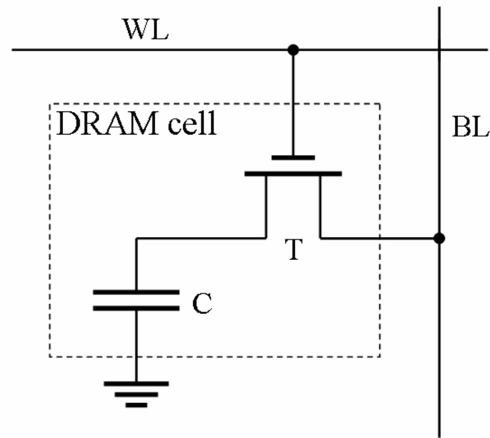


Fig. 1-1 DRAM cell with 1T1C structure. The access transistor is selected by word-line (WL) and bit-line (BL).

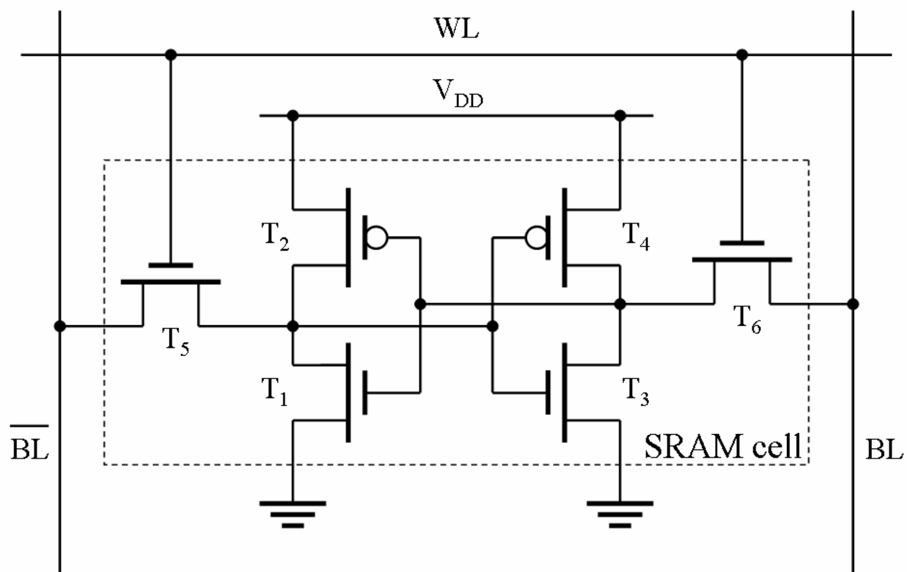


Fig. 1-2 SRAM cell with six transistors.

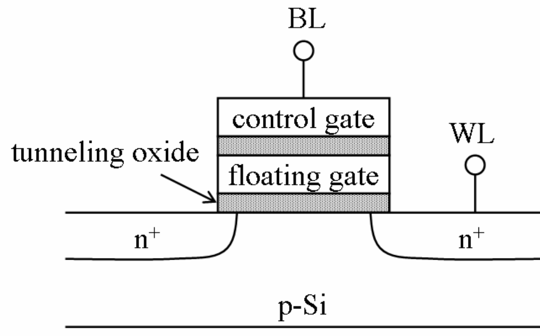


Fig. 1-3 Typical Flash memory cell with a floating gate.

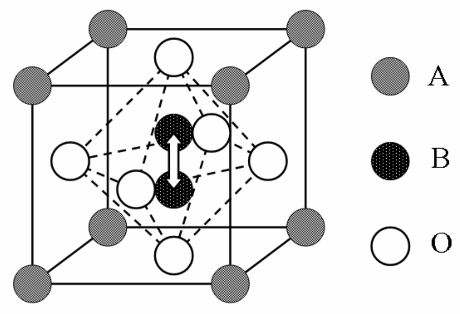


Fig. 1-4 ABO_3 structure (perovskite structure).

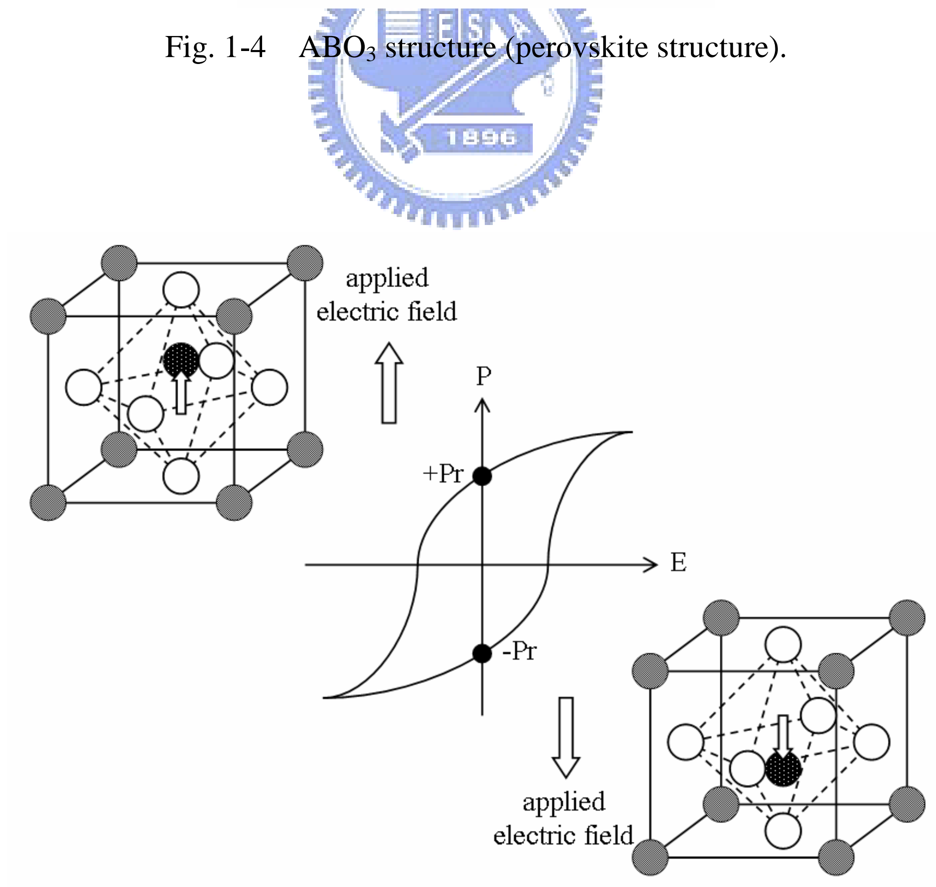


Fig. 1-5 Polarization hysteresis curve of the FeRAM material.

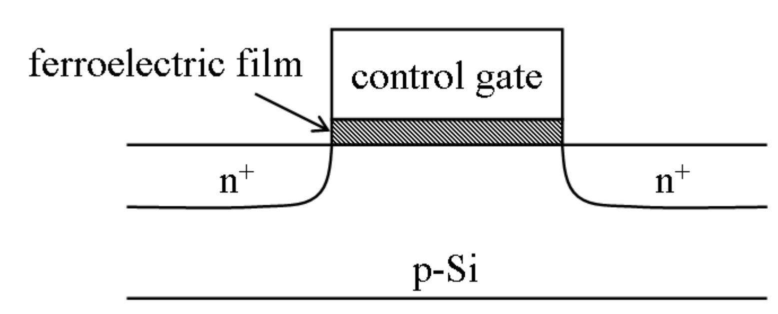


Fig. 1-6   MFSFET structure of the FeRAM.

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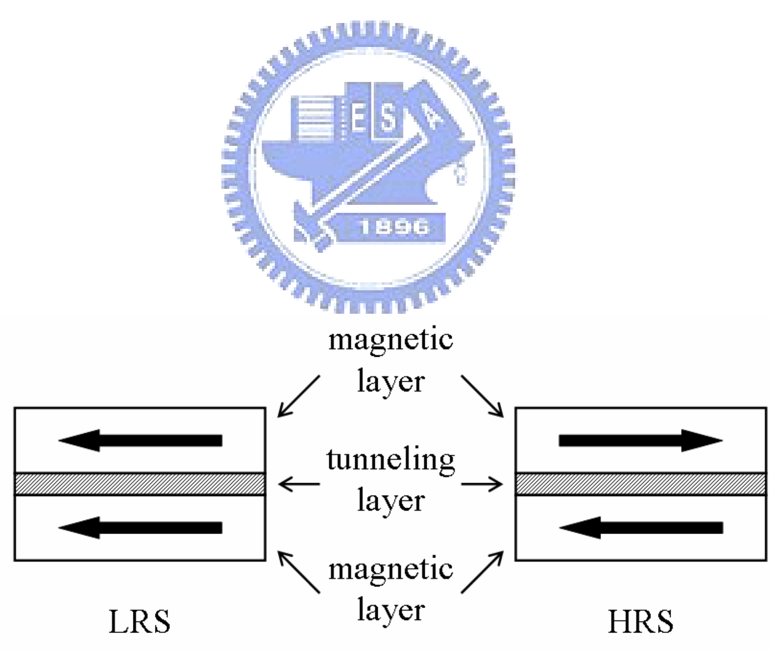


Fig. 1-7   Parallel state [low resistance state (LRS)] and antiparallel state [high resistance state (HRS)] of the MRAM.

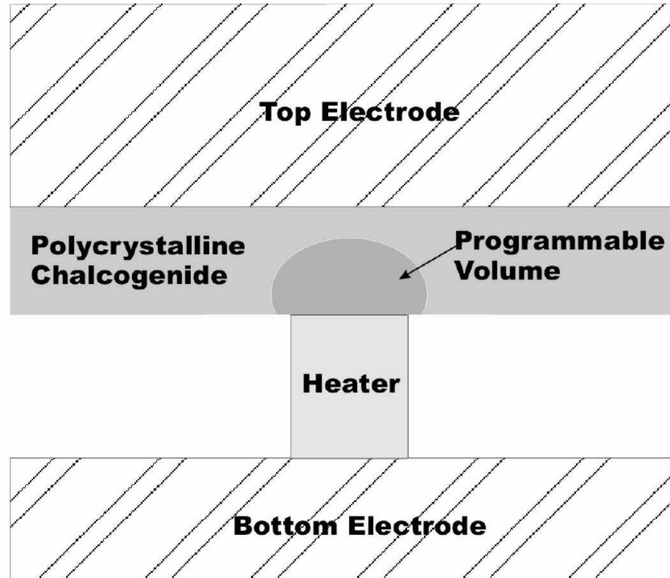


Fig. 1-8 Basic memory cell of the PCRAM [10].

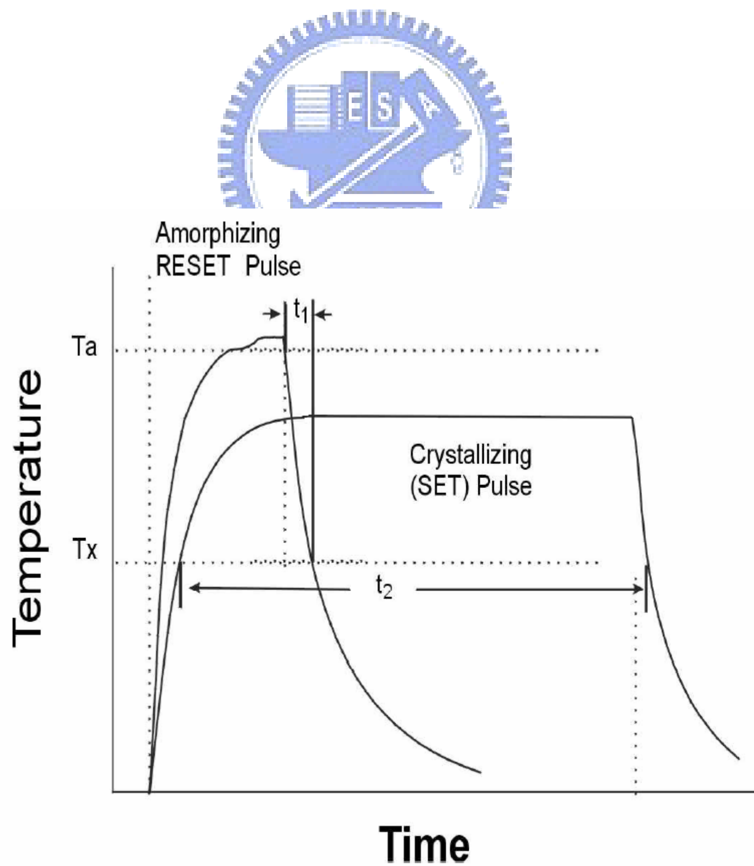


Fig. 1-9 Time-temperature relationship of the PCRAM [10].

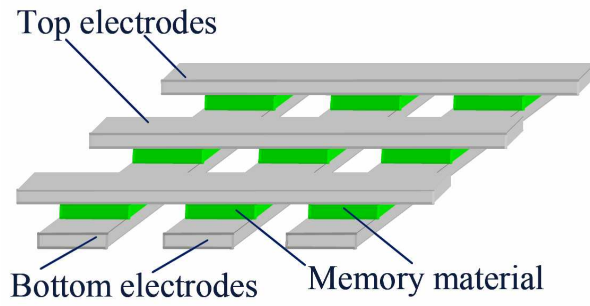


Fig. 1-10 Cross-point memory array of the RRAM [15].

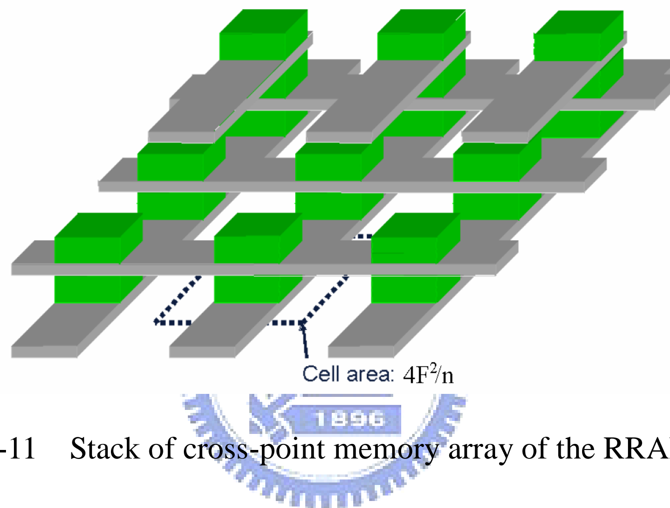
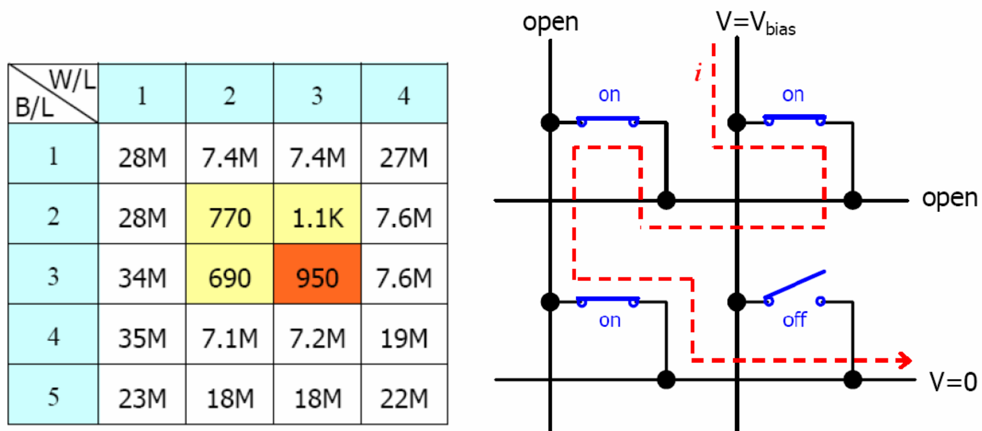


Fig. 1-11 Stack of cross-point memory array of the RRAM [15].



B/L \ W/L	1	2	3	4
1	28M	7.4M	7.4M	27M
2	28M	770	1.1K	7.6M
3	34M	690	950	7.6M
4	35M	7.1M	7.2M	19M
5	23M	18M	18M	22M

Fig. 1-12 Misread case of the cross-point memory array [16].

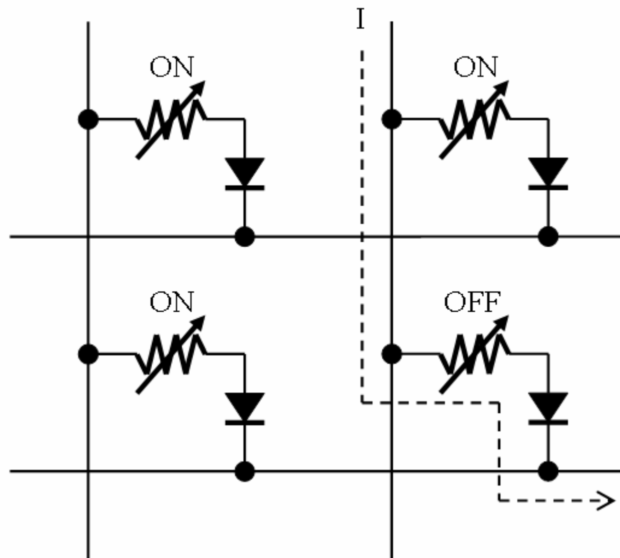
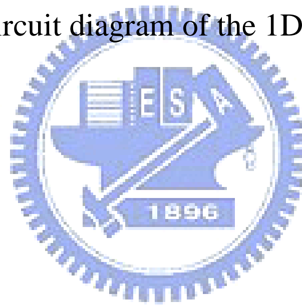


Fig. 1-13 Basic circuit diagram of the 1D1R structure of RRAM.



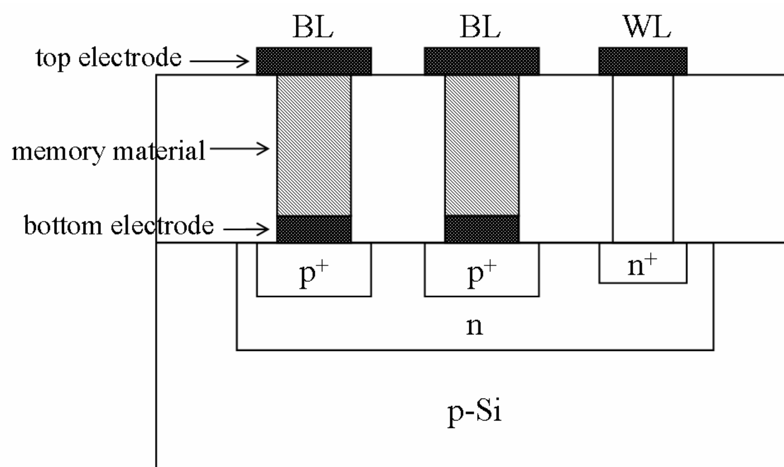


Fig. 1-14 Cross section view schematic diagram of the 1D1R structure of RRAM.

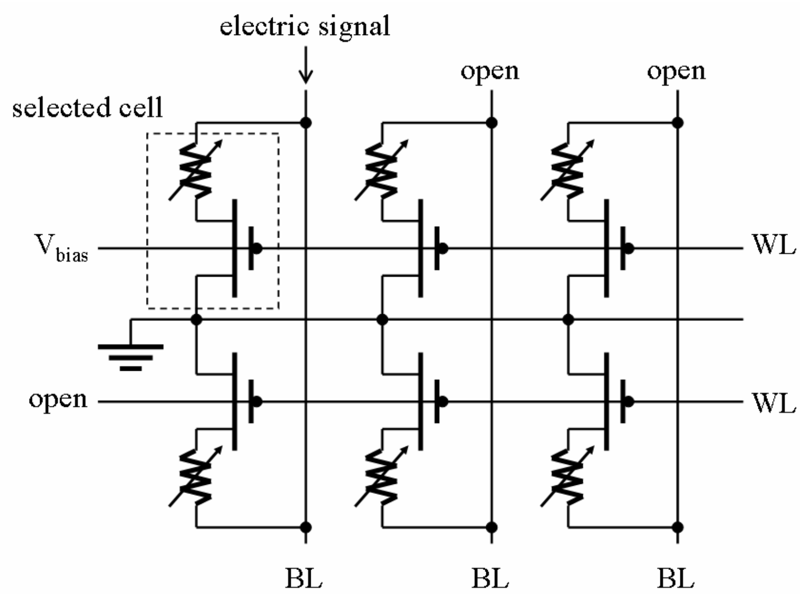
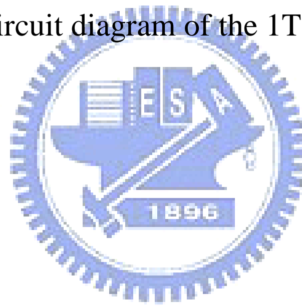


Fig. 1-15   Basic circuit diagram of the 1T1R structure of RRAM.



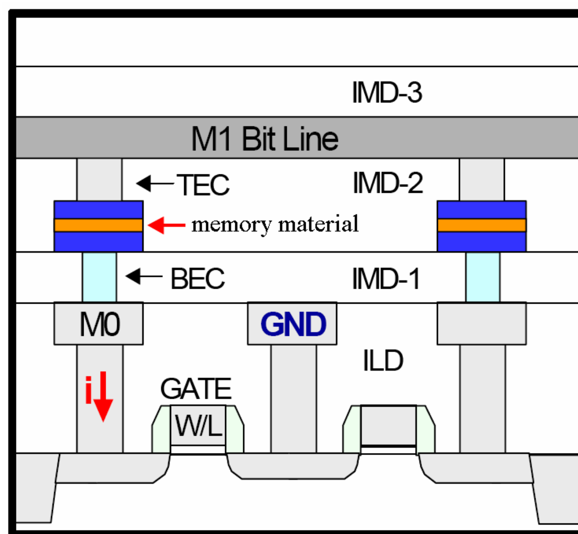


Fig. 1-16   Cross section view schematic diagram of the 1T1R structure of RRAM [17].

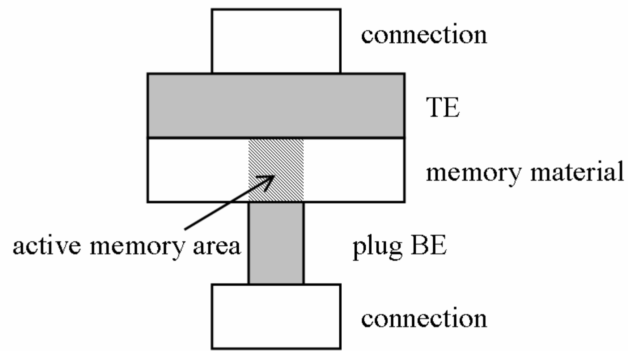


Fig. 1-17 Plug BE structure of the ERE device.

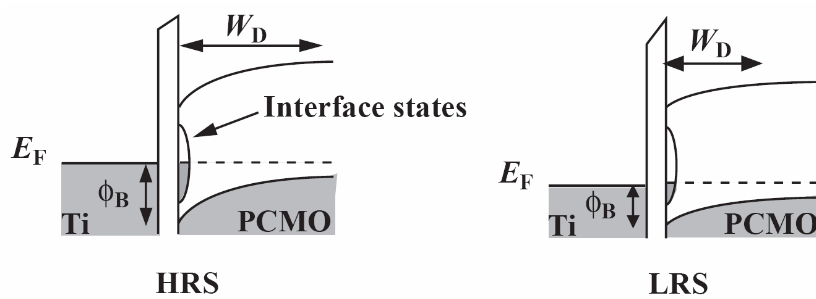


Fig. 1-18 Modulation of the Schottky-like barrier [22].

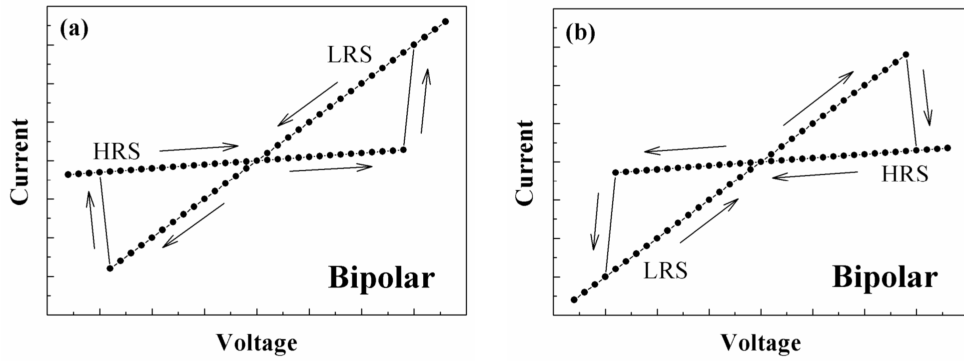


Fig. 1-19 Typical I-V curves of the bipolar resistive switching.

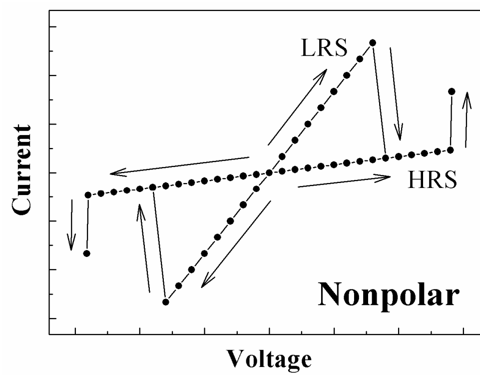


Fig. 1-20 Typical I-V curve of the nonpolar resistive switching.

Chapter 2

Experimental Details

2.1 Radio-frequency Magnetron Sputtering System

Sputtering system has been extensively used to deposit metal and dielectric films because of its easy-control and low-cost properties. In this dissertation, we utilize a radio-frequency (RF) sputtering system to deposit the dielectric thin films including the $LaNiO_3$ (LNO) bottom electrode and SZO resistive layer. The illustration of the system is shown in Fig. 2-1, and the system is composed of the following components.

- Sputtering chamber: including a 3-inch sputtering gun with target and shutter, and a rotatable substrate holder controlled by a DC motor.
- Vacuum system: consisting of one mechanical pump for rough vacuum, one diffusion pump for high vacuum, and several exhausting valves to control the vacuum system.
- Pressure and ambient control system: consisting of several vacuum gauges, gas supply, and mass flow controllers. The vacuum gauges and exhausting valves are used during the pumping process. The base pressure of the chamber was evacuated to 1×10^{-5} Torr before a deposition process. The exhausting valve, gas supply and mass flow controllers can control the flow rates of Ar and O_2 gases and the working pressure during a deposition process.
- Heating module: with four quartz lamps and two thermal couples. The substrate was heated by the quartz lamps, and the substrate temperature was calibrated by thermal couples, one sat near the lamps and the other direct contacted with the substrate.
- RF generating system: including one RF power generator (13.56 MHz) and an

automatic matching box which can adjust the impedance of the total network for minimum reflected power.

- Cooling system. During a deposition process, the heating lamps and plasma produce a lot of heat in the chamber. The cooling water is used to prevent a heat damage of rotating system and sputtering gun.

2.2 Sample Preparation I

The p-type 4-inch Si (100) wafer was cleaned by the standard RCA cleaning process. And then, the wafer was chemically etched by dip in dilute HF solution to remove the chemical oxide on the wafer. After the cleaning process, a 200-nm-thick SiO_2 oxide film was thermally grown on the Si wafer at 950^oC in an oxidation furnace in H_2 and O_2 ambient to perform an isolation layer. Then, a 100-nm-thick LNO conducting film was deposited on the SiO_2/Si substrate using the RF magnetron sputtering system. Details are discussed in Sec. 2.2.1. The LNO film was heat-treated by the rapid thermal annealing (RTA) furnace in O_2 ambient at 600, 700 or 800^oC for 1 min. After that, a 50-nm-thick pure SZO or V-doped SZO (V:SZO) film was deposited on the LNO BE by the sputtering system. Details are discussed in Sec. 2.2.2. Finally, a 300-nm-thick Al TE was deposited on the substrate at RT using thermal evaporator to form an ERE sandwich structure. The area of the TEs defined by a shadow mask was 4.91×10^{-4} cm^2. The device structure is shown in Fig. 2-2.

2.2.1 Deposition of LNO Bottom Electrode

The LNO conducting film was deposited at 250^oC at fixed power of 150W by the RF magnetron sputtering from a powder target. During the deposition, the working pressure is 10 mTorr maintained by a mixture of Ar and O_2 gased at a fixed

ratio of 3:2 with a total flow rate of 40 sccm.

The LNO sputtering target was prepared in the following method. First, the La_2O_3 and NiO powders were mixed in a stoichiometric ratio and ball-milled in absolute ethanol for 24h. After that, the mixture was dried in a heat oven. Then, the dried powder was calcined at 1300°C in a furnace for 4h. After that, the calcined powder was ball-milled for 1h without any additive to get the final LNO powder. Finally, the LNO powder was spread on a target holder and pressurized at 2×10^4 pounds for 40s to make it to a disk-shaped sputtering target. The fabrication flow of the LNO sputtering target is shown in Fig. 2-3.

2.2.2 Deposition of SZO Resistive Layer

The pure SZO and V:SZO films were deposited at 500°C at fixed power of 150W by the RF magnetron sputtering from a powder target. During the deposition, the working pressure is 10 mTorr maintained by a mixture of Ar and O_2 gases at a fixed ratio of 3:2 with a total flow rate of 40 sccm.

The pure SZO sputtering target was prepared in the following process. First, the $SrCO_3$ and ZrO_2 powders were mixed in a stoichiometric ratio and ball-milled in absolute ethanol for 24h. The mixture was dried in a heat oven. Then, the dried powder was heated at 600 and 800°C for 2h, respectively, and calcined at 1250°C for 8h. The powder was ball-milled for 1h without any additive. After that, the powder was heated again at 600 and 800°C for 2h, respectively, and calcined at 1400°C for 10h. The calcined powder was ball-milled again for 1h without any additive to get the final SZO powder. Finally, the SZO powder was spread on a target holder and pressurized at 2×10^4 pounds for 40s to make it to a disk-shaped sputtering target. On the other hand, the V:SZO sputtering target was prepared in the same way except the powder mixture. In this dissertation, V_2O_5 was used for V

doping. Because the V atom was added to substitute for the Zr atom in the V:SZO powder, the atomic percentage of Zr should be subtracted. For instance, if we want to synthesize a 0.2%-V:SZO powder, we should take 1 mol of $SrCO_3$, 0.998 mol of ZrO_2, and 0.001 mol of V_2O_5 powders (noticing that there is 2 mol of V atoms in 1 mol of V_2O_5). The fabrication flow of the pure SZO and V:SZO sputtering targets are shown in Fig. 2-4.

2.3 Sample Preparation II

Similar to the ERE device preparation shown in Sec. 2.2, the device with ERBE structure was fabricated in the following process. First, a 200-nm-thick SiO_2 oxide film was thermally grown on the RCA-cleaned (100) Si wafer to perform an isolation layer. Second, a 10-nm-thick Ti adhesion layer and a 100-nm-thick Pt conducting layer were sequentially deposited on the SiO_2/Si substrate using an electron beam evaporator to form the BE. Then, a 100-nm-thick LNO buffer layer was deposited on the Pt BE at 250°C using the RF magnetron sputtering system. The LNO film was heat-treated by the RTA furnace in O_2 ambient at 600°C for 1 min. After that, a 50-nm-thick V:SZO film was deposited on the LNO BE by the sputtering system. Finally, a 300-nm-thick Al TE was deposited on the substrate at RT using a thermal evaporator. Therefore, the device with ERBE structure was completed. The area of the TEs defined by a shadow mask was 4.91×10^{-4} cm^2. The device structure is shown in Fig. 2-5.

2.4 Physical Analyses

2.4.1 X-ray Diffraction

The crystal structure and orientations of the LNO, pure SZO, and V:SZO thin films were determined by the X-ray diffractometer (Bede D1) with Cu Kα radiation (λ=0.15405nm). The schematic illustration of the X-ray diffractometer is shown in

Fig. 2-6. The scanning step was 0.02°, and the scanning speed was 4 °/min. Based on the X-ray diffraction (XRD) pattern, the average grain size of each orientation can be estimated by using Scherrer's formula,

$$D=\frac{0.9\times\lambda}{B\times\cos\theta} \tag{2-1}$$

where D is the average grain size of the film, λ is the wavelength of the incident X-ray (0.15405nm), B is the full width of half maximum (FWHM) of the specific XRD peak, and θ is the diffraction angle.

2.4.2 Scanning Electron Microscopy

The surface morphology and cross section view of the LNO, pure SZO, and V:SZO thin films were characterized by the scanning electron microscopy (SEM) (Hitachi S-4700I) with a resolution of 1.5nm operated at 15kV. During the determination, a cold-cathode electron gun is used as a source of electron beam with an operation voltage from 0.5 to 30kV. The accelerated electron beam can be emitted to the specimen, and the secondary electrons originated within a few nanometers from the specimen surface are detected and rendered into a bright SEM image. The schematic illustration of the SEM is shown in Fig. 2-7.

2.4.3 Atomic Force Microscope

The surface roughness and surface morphology of the LNO and V:SZO thin films were characterized by the atomic force microscopy (AFM) (Digital Instruments NanoScope IIIa) in tapping mode. The mean roughness and root mean square (RMS) roughness of the films are automatically calculated by the software. The schematic illustration of the AFM is shown in Fig. 2-8.

2.4.4 Transmission Electron Microscopy

The thickness and interface morphology of the LNO and V:SZO thin films were determined by the transmission electron microscopy (TEM) (JEPL JEM-2100F). First, electron beam is accelerated and focused on the specimen, which must be sufficiently thin to be transparent of incident electrons. Then, the transmitted and forward-scattered electrons form a diffraction pattern in the focus plane and a magnified bright image in the main screen. The schematic illustration of the TEM is shown in Fig. 2-9.

In this dissertation, focused ion beam (FIB) (FEI Nova 200) with resolution of 7nm was used to prepare the thin-enough TEM specimen. We use the milling action of the FIB to excavate the material from both sides of the final thin target, and then cut the objective and transfer it to a TEM specimen grid.

2.4.5 Four-point Probe

The sheet resistance of the LNO film was measured by the four-point probe (NAPSON RT-7). The schematic illustration of the four-point probe is shown in Fig. 2-10. During the measurement, the voltage is applied between P_2 and P_3, and current is determined between P_1 and P_4. Assuming that the dimension of the specimen is much larger than the probe spacing (S), and the thickness of the specimen is much smaller than S, so the sheet resistance of the specimen can be estimated by this formula,

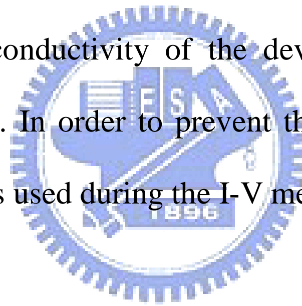
$$R_{sheet} = \frac{\pi}{\ln(2)}\left(\frac{V}{I}\right) \cong 4.53\left(\frac{V}{I}\right) \qquad (2\text{-}2)$$

2.5 Electrical Analyses

The resistive switching properties of the SZO-based ERE and ERBE devices were recorded by the semiconductor parameter analyzer (Agilent 4155C) and pulse pattern generator (Agilent 81110A). The low-leakage switch mainframe (Agilent E5250A) was used to switch the input and output of the electric signals, and a computer with the Agilent VEE software was utilized to control the above instruments. During the electrical analyses, electric signals including the sweep voltage and voltage pulse were applied on the TE, while the BE was grounded.

2.5.1 Current-voltage Measurement

The I-V measurements of the ERE and ERBE devices were performed by the Agilent 4155C. The conductivity of the device can be changed by applying a specific sweep voltage. In order to prevent the electrical damage of the device, a current compliance was used during the I-V measurement for the ERBE device.



2.5.2 Retention Time Test

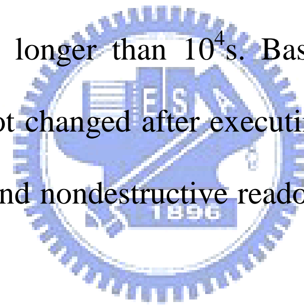
The retention time is the time of stored information which can be kept without any power supply. In this dissertation, the retention time of the SZO-based device is measured by Agilent 4155C. First, two identical devices were switched to HRS and LRS, respectively. After a period, read the currents of these two devices by applying a tiny voltage, which cannot change the memory state of the device. In addition to the read process, the devices were placed in a dry environment at RT without any power supply. Besides, a thermal acceleration test was also used for the retention test because the retention time of the SZO-based device is very long.

2.5.3 Endurance Test

The endurance is the number that a device can be stably switched its resistance states between HRS and LRS by applying a sweep voltage or voltage pulse. In this dissertation, the endurance of the SZO-based device is determined by repeatedly applying a sweep voltage by Agilent 4155C.

2.5.4 Nondestructive Readout Test

The nondestructive readout behavior of the SZO-based device is demonstrated by Agilent 4155C in the following two ways. Firstly, thousands of sweep voltages between ±5V were applied on two identical devices which were switched to HRS and LRS. Secondly, a DC bias voltage was applied on the devices with HRS and LRS, respectively, for longer than 10^4s. Based on the experimental results, the memory states were not changed after executing these two examinations at RT and 85°C, so the stability and nondestructive readout behavior of the SZO-based device is investigated.



2.5.5 Resistive Switching by Voltage Pulse

The resistive switching behavior of the ERBE device was performed by the Agilent 4155C, 81110A, and E5250A. The resistance states of the ERBE device can be switched by applying a specific voltage pulse with a period of 10ns.

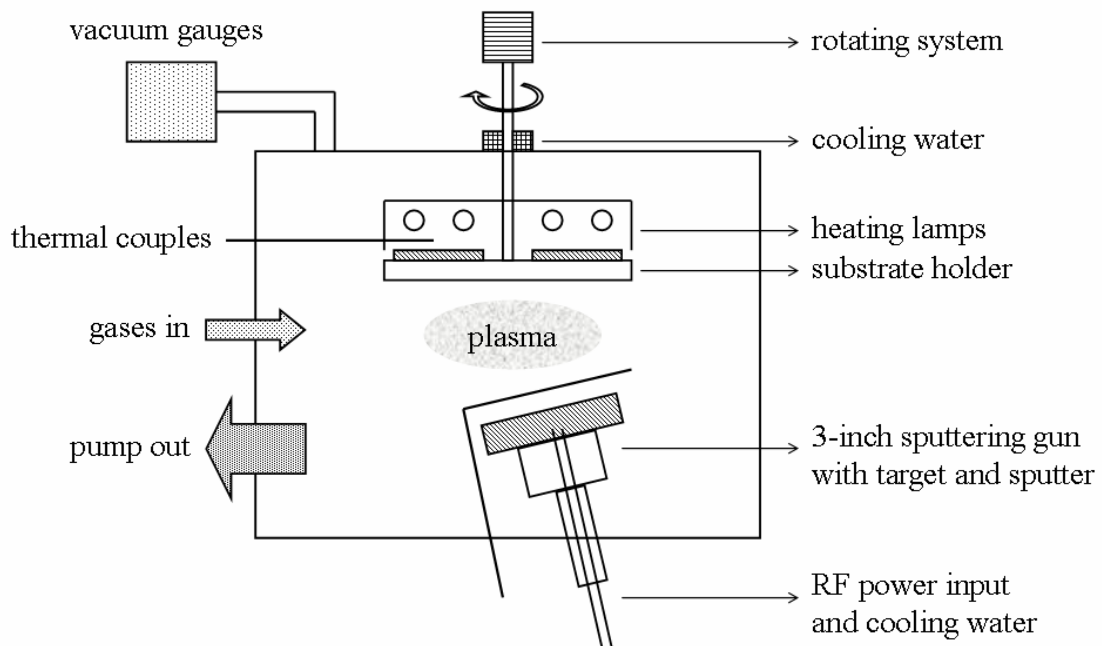


Fig. 2-1 Illustration of the RF magnetron sputtering system.

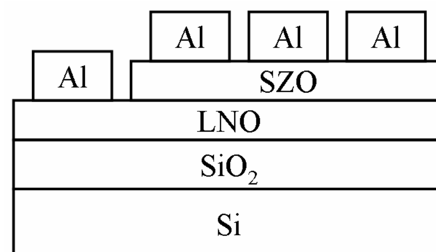


Fig. 2-2 Device structure of the ERE device.

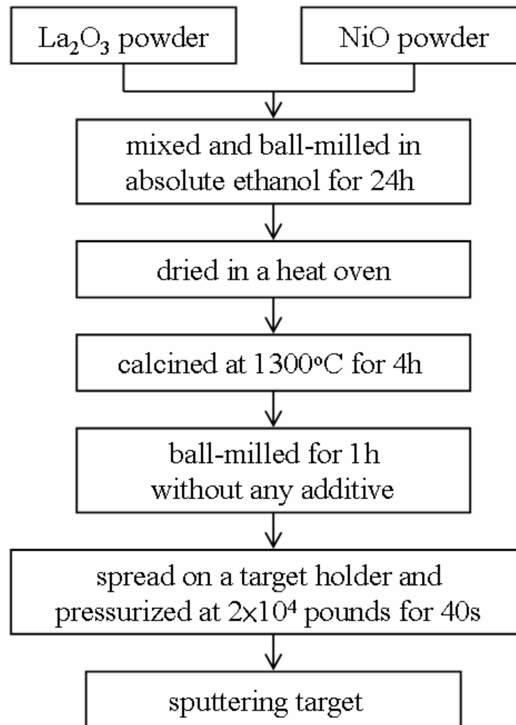


Fig. 2-3 Fabrication flow of the LNO sputtering target.

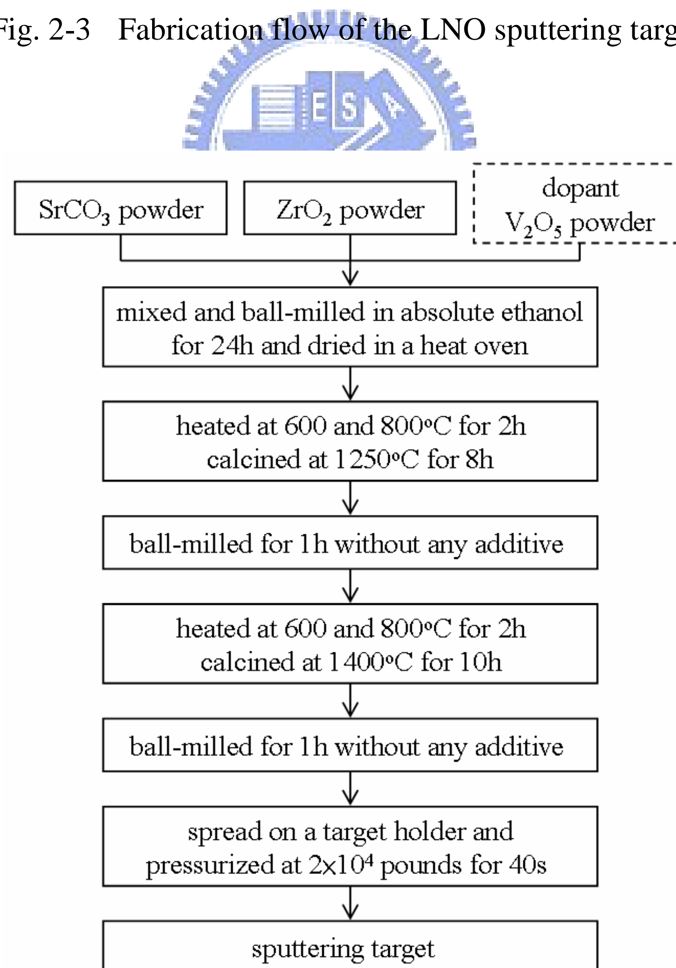


Fig. 2-4 Fabrication flow of the pure SZO and V:SZO sputtering targets.

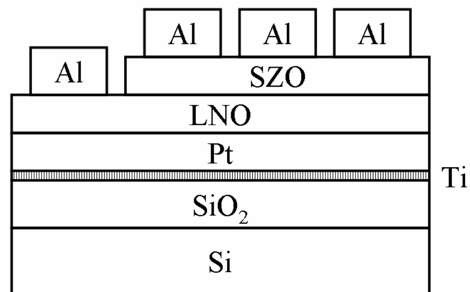


Fig. 2-5 Device structure of the ERBE device.

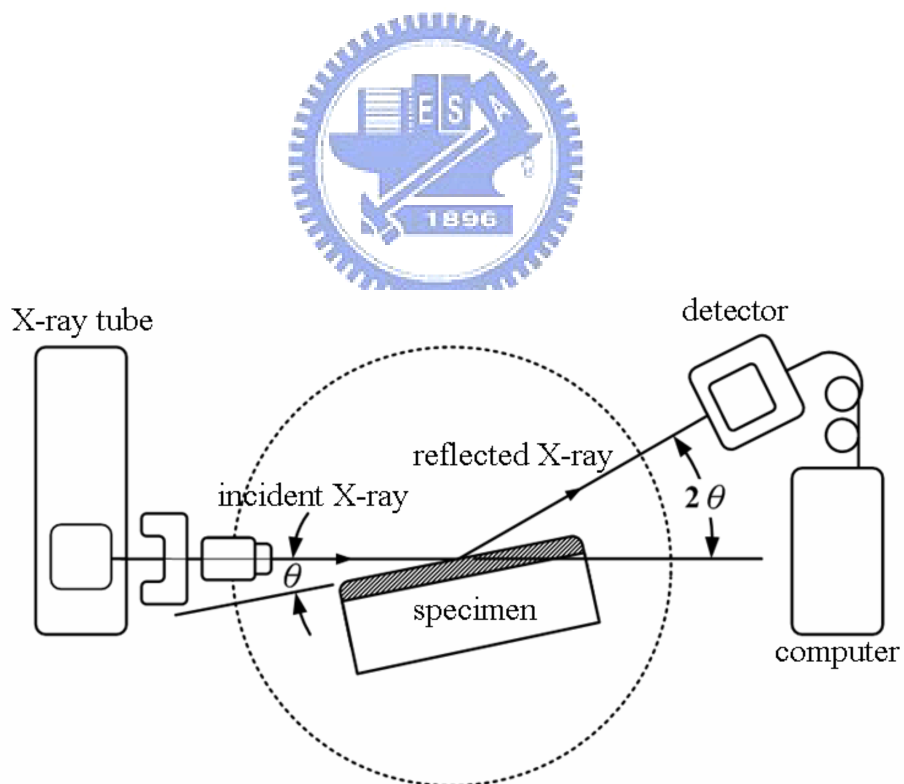


Fig. 2-6 Schematic illustration of the X-ray diffractometer.

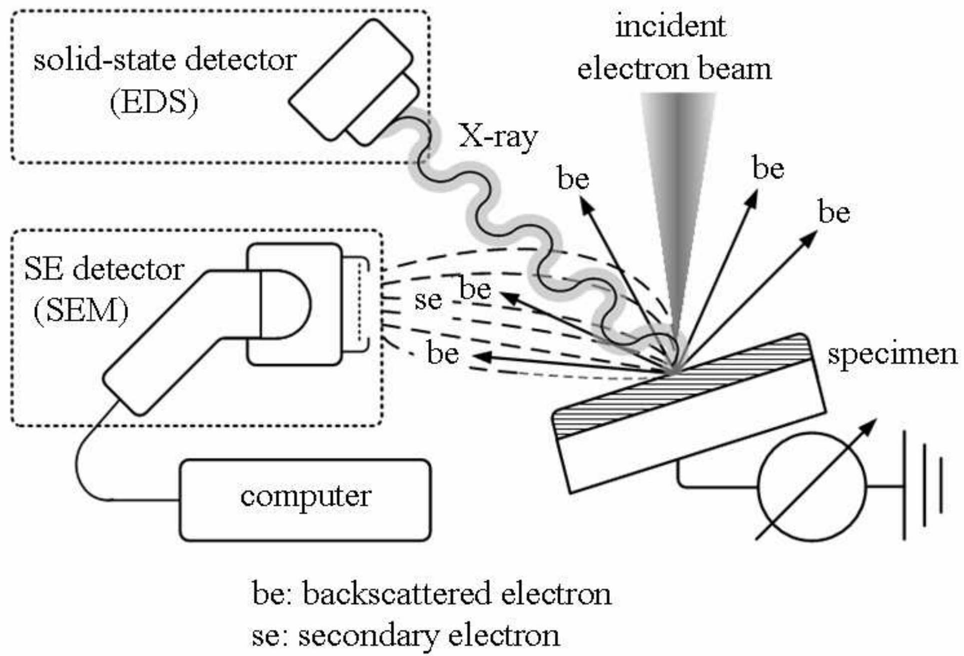


Fig. 2-7 Schematic illustration of the SEM.

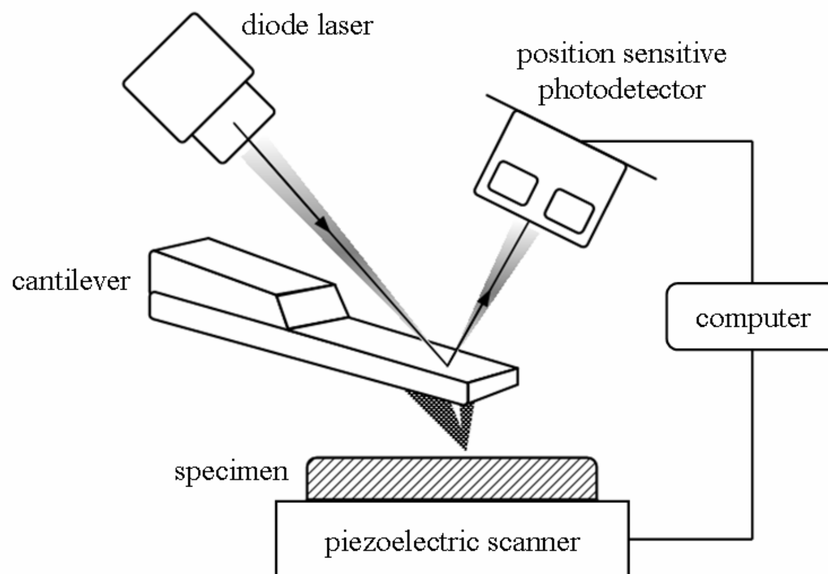


Fig. 2-8 Schematic illustration of the AFM.

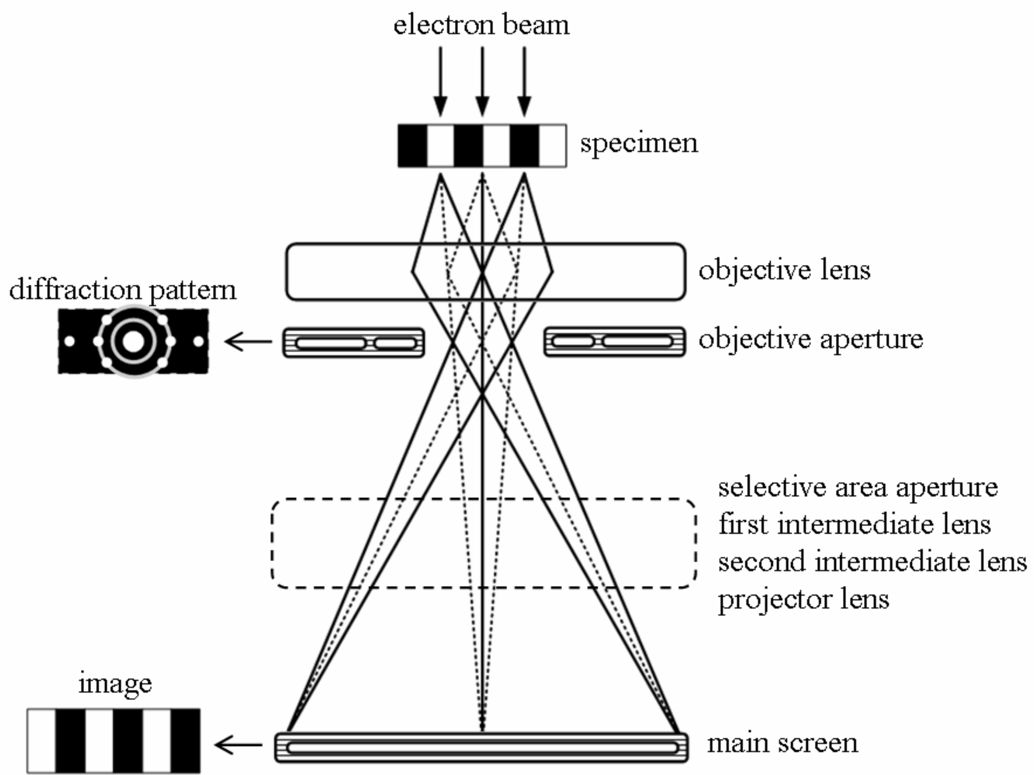


Fig. 2-9　Schematic illustration of the TEM.

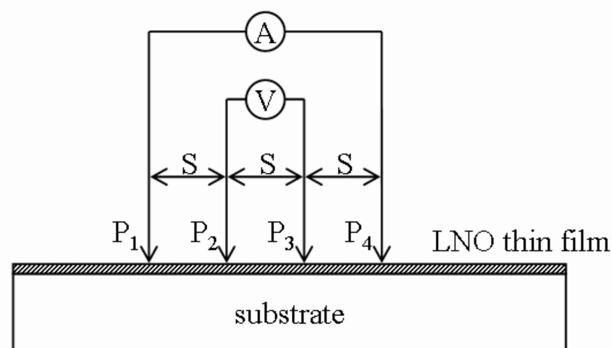


Fig. 2-10　Schematic illustration of the four-point probe.

Chapter 3

Results and Discussion of Bipolar Resistive Switching in the $SrZrO_3$-based Electrode/Resistor/Electrode Devices

3.1 Introduction

The bipolar resistive switching properties such as resistance ratio, retention time, nondestructive readout property, stability, and doping effect of the SZO-based electrode/resistor/electrode (ERE) devices are discussed in this chapter. The resistive switching mechanism of the SZO-based memory devices is also demonstrated. The fabricating process of the SZO-based ERE device is shown in Sec. 2.2 (Sample Preparation I).

3.2 Properties of the $LaNiO_3$ Bottom Electrodes

The 100-nm-thick LNO films were deposited at 250°C and then annealed at 600, 700, or 800°C. The sheet resistance of the as-deposited LNO film is about 142 Ω/□, and those of the 600, 700, and 800°C-annealed LNO films are about 82, 68, and 59 Ω/□, respectively. The result shows that the higher the annealing temperature, the lower the sheet resistance.

Fig. 3-1 depicts the XRD patterns of the as-deposited LNO, and 600, 700, and 800°C-annealed LNO films, showing that the LNO films have (100) and (200) orientations, which have been reported that a SZO film deposited on the (100)-orientated LNO film had good resistive switching behavior [27]. Besides, an (110) peak is observed in the 700 and 800°C-annealed LNO films. The average size of the (110)-orientated

grains in the 700°C-annealed LNO film is about 63.3nm estimated by Scherrer's formula (Eqn. 2-1).

Figs. 3-2 and 3-3 show the surface SEM images of the 600 and 700°C-annealed LNO films, respectively. The 600°C-annealed film performs a smooth surface, but the surface roughness of the 700°C-anneald film degraded due to the unwilling precipitates presented in the LNO surface, which corresponds to the XRD patterns shown in Fig. 3-1. Fig. 3-4 indicates the surface AFM image of the 600°C-annealed LNO film. The mean roughness and the RMS roughness of the LNO film are 0.923 and 1.227nm, respectively. Therefore, based on the experimental results, the annealing temperature of the LNO BE is decided at 600°C to get the smooth surface and high conductivity.

3.3 Properties of the $SrZrO_3$ Resistive Layers

Fig. 3-5 shows the XRD patterns of the 600°C-annealed LNO film, and the SZO films with different doping concentration deposited on the 600°C-annealed LNO films. The result shows that a little doping does not change the crystal structure of the SZO film. To deserve to be mentioned that the doping concentration shown in this dissertation indicates the concentration of the sputtering targets discussed in Sec. 2.2.2.

Fig. 3-6 performs the surface SEM image of the 0.3%-V:SZO film deposited on the LNO film, indicating that the SZO film is very smooth. Fig. 3-7 shows the surface AFM image of the 0.3%-V:SZO film deposited on the LNO film. The mean roughness and the RMS roughness of the SZO film are 0.812 and 1.037nm, respectively.

Fig. 3-8 indicates the cross section TEM image of the 0.3%-V:SZO/LNO/SiO_2 structure. The interfaces between two films are even, and the thicknesses of the LNO and SZO films are about 100 and 45nm, respectively.

3.4 Typical Current-voltage Characteristics of the $SrZrO_3$-based Electrode/Resistor/Electrode Devices

Fig. 3-9(a) depicts the I-V curves of pure SZO and 0.2%-V:SZO ERE devices in semilogarithm scale rather than linear scale as indicated in Figs. 1-19 and 1-20. The I-V curve plotted in semilogarithm scale is easily to observe the resistance ratio of the device. When a negative sweep voltage is applied on the TE, the current of the device rapidly increases, and the device is switched from HRS to LRS, which is defined as “turn-on” process. The resistance state retains on LRS after sweeping the voltage from negative to 0V. Otherwise, when a positive sweep voltage is applied, the current of the device decreases, and the device is switched from LRS back to HRS after passing the transition region, defined as “turn-off” process. The resistance state firmly retains on HRS after sweeping the voltage from positive to 0V. The resistive switching is attributed to the formation and disruption of current paths [19], [34], [39], which is discussed in detail in Sec. 3.7. The LRS currents of these two devices are almost the same because the conductivities of the current paths in these two devices are almost identical. However, the HRS current of the 0.2%-V:SZO ERE device is much lower than that of the pure SZO ERE device owing to the doping effect, which is achieved by Zr^{4+} sites being substituted by V^{5+} leading to suppressing the formation of oxygen vacancies [113]. On the other hand, the turn-on voltage of the pure SZO ERE device is a little higher than that of the 0.2%-V:SZO ERE device, which indicates that the current paths in the pure SZO ERE device are more difficult to be formed. Obviously, the V_2O_5 doped into the SZO-based ERE device can decrease the HRS current and the turn-on voltage; hence, the resistance ratio between HRS and LRS is increased from 20 to 1000 measured at -1V for the pure SZO and 0.2%-V:SZO ERE devices, respectively [shown in Fig. 3-9(b)].

Figs. 3-10(a) and (b) perform the I-V curve and the resistance ratio of the 0.3%-V:SZO ERE device, respectively. The result shows that the resistance ratio is

higher than that of the less-doped devices due to the doping effect [113]. Figs. 3-11(a) and (b) exhibit the I-V curves and the resistance ratios of the 0.7%-V:SZO and 1.0%-V:SZO ERE devices, respectively, showing that the resistive switching property degrades in the 0.7%-V:SZO ERE device, and disappears in the 1.0%-V:SZO ERE device, which could be due to the segregation of vanadium oxides or other compounds.

Fig. 3-12 shows the statistical chart of the resistance ratios of pure SZO, and 0.1%-V:SZO to 1.0%-V:SZO ERE devices measured at -1V, indicating that the pure SZO ERE device possesses the resistive switching behavior, which can be considered as an intrinsic property of the SZO-based memory device. Besides, a proper concentration of doping into the SZO film can improve the resistive switching properties. Therefore, the resistive switching properties of the 0.2 and 0.3%-V:SZO ERE devices with higher resistance ratios are discussed in detail in the following sections.

3.5 Bipolar Resistive Switching Properties of the 0.2%-V-doped $SrZrO_3$ Electrode/Resistor/Electrode Device

The resistive switching properties of the 0.2%-V:SZO ERE device are performed in this section. Figs. 13(a) and (b) indicate the fitting curves of LRS and HRS currents of the device shown in Fig. 3-9(a) (open circles) by Ohmic conduction and F-P emission, respectively. The fitting curves of the LRS currents are two straight lines, and the slopes are very close to unity, which indicates that the LRS currents confirm to the Ohmic conduction, relating to thermal excited electrons hopping from one isolated state to the next [111]. On the other hand, the HRS currents are dominated by the trap-controlled F-P emission, which corresponds to the field-enhanced thermal excitation of trapped electrons into the conduction band [111], as indicated by the linear fittings of the experimental data. Therefore, both LRS and HRS conductions are bulk-controlled, not

interface-controlled. Moreover, the ERE device with asymmetric TE and BE performing the symmetric fitting curves between the positive and negative voltage regions can also demonstrate the bulk effect.

Fig. 3-14(a) shows the endurance of the 0.2%-V:SZO ERE device. While the number of the voltage sweeping cycles (from HRS switched to LRS, and then switched back to HRS) is increased, the HRS currents slowly increase leading to the decreasing in resistance ratios between two resistance states. Fig. 3-14(b) indicates Ohmic conduction fitting curves of both LRS and HRS currents for the 1st, 50th, and 100th voltage sweeping cycles. The LRS conductions retain the Ohmic behavior after applying the voltage sweeping cycles as indicated, but the HRS conductions change from F-P emission to Ohmic conduction after applying the voltage sweeping cycles, which is attributed to a degradation of the capability of defects to trap electrons.

Fig. 3-15 shows the statistical chart of both LRS and HRS currents of the 0.2%-V:SZO ERE device measured at -1V. The resistive switching properties can be observed in more than 70% of the devices. In the chart, the LRS currents are more stable than the HRS currents due to the stable conductivities of the current paths in the SZO films. The resistance ratio between two states is over 20 for the worst case.

Figs. 3-16(a) and (b) perform the nondestructive readout property of the 0.2%-V:SZO ERE devices measured at RT and 85°C, respectively. During the measurement, two devices are switched to LRS at RT, and then apply thousands of voltage reading cycles (from +5V sweeping to -5V) on the devices at RT and 85°C. After that, these two devices are switched to HRS at RT, and then also apply thousands of voltage reading cycles on the devices at RT and 85°C. The results indicate that the LRS currents of these two devices keep almost unchanged, while the HRS currents decline with the increased voltage reading cycles. Therefore, the resistance ratio between two resistance states increases with the increased voltage reading cycles, which is a good

tendency for accurate readout.

3.6 Bipolar Resistive Switching Properties of the 0.3%-V-doped $SrZrO_3$ Electrode/Resistor/Electrode Device

The resistive switching properties of the 0.3%-V:SZO ERE device are performed in this section. Fig. 3-17(a) performs the fitting curves of both LRS and HRS currents indicated in Fig. 3-10(a) by Ohmic conduction. The slopes of the LRS fitting curves are very close to unity, indicating that the LRS currents dominate by Ohmic conduction, which corresponds to the result shown in Fig. 3-13(a). On the other hand, the HRS currents follow the F-P emission as indicated by the linear fittings to the HRS currents shown in Fig. 3-17(b). However, the fitting curve of the HRS is not an absolutely straight line when the voltage is swept over the turn-off voltage (about 13V). The inset of Fig. 3-17(b) exhibits the linear fitting of the HRS current by SCLC while the device is swept over 13V. Therefore, the F-P mechanism dominates at the sweep voltage less than the turn-off voltage, whereas the SCLC becomes predominant at the voltage over the turn-off voltage. Either the F-P emission or SCLC is related to the trapped electrons.

Fig. 3-18(a) depicts the I-V curves of the 0.3%-V:SZO ERE device for the 1st, 50th, and 100th voltage sweeping cycles. The improved stability of the HRS currents of this device in comparison with that of the 0.2%-V:SZO ERE device is indicated, which is believed to be the result of doping effect [113]. The LRS and HRS currents firmly retain on Ohmic conduction and F-P emission, respectively, after applying 100 voltage sweeping cycles. Fig. 3-18(b) shows the endurance of the 0.3%-V:SZO ERE device. The resistance ratio between two resistance states retains at 1000 after applying 100 voltage sweeping cycles.

Fig. 3-19 shows the statistical chart of both LRS and HRS currents of the

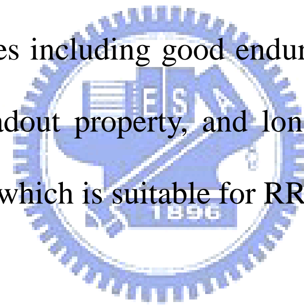
0.3%-V:SZO ERE device measured at -1V. The resistive switching properties can be observed in more than 90% of the devices. In the chart, the LRS currents are more stable than the HRS currents due to the stable conductivities of the current paths in the SZO films. Besides, the HRS currents of the device are more stable than those of the 0.2%-V:SZO ERE device indicated in Fig. 3-15 also owing to the doping effect [113]. The resistance ratio between two resistance states is over 500 for the worst case and over 1000 in general.

Fig. 3-20 depicts the I-V curves of the 0.3%-V:SZO ERE device measured at 70 and 100°C, indicating that the resistive switching property of the device is not degraded while measured at 100°C. The resistance ratio between two resistance states of the device retains at least 1000. Because of the large variation in HRS currents of the device, no clear temperature dependence is observed. In addition, while the measurement is performed at 150°C, the HRS current of the device significantly increases, and hence, the resistance ratio decreases possibly due to the electrons with higher thermal energy, which would be difficultly trapped at such a high temperature (as shown in the inset of Fig. 3-20). When the 150°C-measured device is performed the measurement at 100°C or less again, the HRS current returns to its lower value as shown in Fig. 3-20. Hence, such degradation at high temperature is a temporary phenomenon.

Figs. 3-21(a) and (b) depict the nondestructive readout property of the 0.3%-V:SZO ERE devices measured at RT and 85°C, respectively. During the measurement, two devices are switched to LRS or HRS at RT, and then apply thousands of voltage reading cycles on the devices at RT and 85°C, indicating that the LRS currents of two devices keep almost unchanged, while the HRS currents decline with the increased voltage reading cycles. Hence, the resistance ratio between two resistance states increases with the increased voltage reading cycles, which is a good tendency for accurate readout. Fig. 3-22 also performs the nondestructive readout property of the device. The resistance

values of the LRSs and HRSs measured at RT and 85°C retain almost unchanged after continuously biased at -5V for more than 10^4s, which implies that the resistance states will not be varied after applying 10^{12} of read pulses (assuming that the read pulse is -5V with 10ns period).

Figs. 3-23(a) and (b) show the retention time of the 0.3%-V:SZO ERE devices measured at RT and 85°C, respectively. During the measurement, a voltage reading cycle which would not change the memory state was applied after a span, and then the current of the specific state measured at -1V is indicated in the figures. The results show that the retention time is longer than 3×10^7s measured at RT, and the resistance ratio between two resistance states retains higher than 1000. In addition, the retention time is longer than 10^5s measured at 85°C with the resistance ratio of 1000. Consequently, the superior resistive switching properties including good endurance, good uniformity, good thermal stability, nondestructive readout property, and long retention time are obtained in the 0.3%-V:SZO ERE devices, which is suitable for RRAM applications.



3.7 Resistive Switching Mechanism of the $SrZrO_3$-based Memory Devices

The resistive switching mechanism in the SZO-based memory devices has been proposed of the formation and disruption of current paths [19], [39]. Liu *et al.* explained the modal of current paths in the SZO-based memory device by the size effect [39]. Fig. 3-24 indicates that the LRS currents are almost unchanged with the increased area of TEs. In other words, the current density of the LRSs is increased with the decreased area of TEs. This result means that the total amount of the current paths do not be varied with the changing of the area of TEs, leading to almost unchanged LRS currents. In addition, Rossel *et al.* explained that the resistive switching mechanism in the SZO-based memory device is due to the changing of distribution and intensity of the current paths as

indicated in Figs. 3-25(a) to (d) [19]. Fig. 3-25(a) shows the electron beam induced current (EBIC) picture and the corresponding I-V curve of the initial HRS of the device (747kΩ). The EBIC picture performs about ten white spots with various sizes. Fig. 3-25(b) shows the EBIC picture and the I-V curve of the LRS (11.6kΩ). The EBIC image shows the clear appearance of two new intense spots indicated by arrows. As the device was switched back to HRS (606kΩ), and the two new spots almost disappeared as shown in Fig. 3-25(c). At the same time, some of the existing spots became more intense. In order to check the two new-formed spots shown in Fig. 3-25(b) was reversible or not, the device was switched again to LRS (10.5kΩ), indicating that only one of the two spots reappeared, and accompanied with three new intense spots as shown in Fig. 3-25(d). The experimental results can conclude that the resistive switching in the SZO-based memory device is due to the changing of distribution and intensity of the current paths. Rossel *et al.* also proposed that doping with a rather high concentration of Cr ion (10^{19} /cm^3) seems to help in stabilizing the resistive switching properties [19], which corresponds to the experimental results shown in this dissertation. Therefore, the resistive switching mechanism in the SZO-based memory devices is the formation and disruption of current paths, which is almost uncontroversial.

On the other hand, the causes of the formation and disruption of current paths are not clearly understood so far. Based on our experimental results, we consider that the causes are the storage and release of carriers in trap states in the SZO film based on two reasons. First, the conduction mechanisms of HRS current in the SZO-based ERE device are dominated by trap-controlled F-P emission and SCLC, indicating that the current of HRS is controlled by trap states. Second, the resistive switching properties are affected by the doping concentration significantly owing to the doping effect discussed in Sec. 3.4.

Figs. 3-26(a) to (d) indicate the hypothetical diagrams of the current paths in the

SZO film. In the turn-on process, the biased electrons can find one or few conducting paths consisting of possible point defects, such as oxygen vacancies, and ionic and electronic defects associated with Zr^{4+} replaced by V^{5+}; simultaneously, the electrons hope through the SZO film by these paths, causing to a significant increase in current. Fig. 3-26(a) shows the hypothetical diagram of these current paths. Besides, the defects in the SZO film can randomly trap electrons in the turn-off process. In the transition region as indicated in Fig 3-10(a), the current decreases while the trapping just occurs at the current paths, and hence, a part of the current paths is ruptured as shown in Fig. 3-26(b). However, the current does not decrease to the stable HRS at a time because the carriers can flow through other unruptured or new-formed current paths indicated in Fig. 3-26(c). Nevertheless, the current should return to the stable HRS after passing the transition region while the defects in the SZO film trap electrons to some degree, and then the paths can be considered as fully ruptured [Fig. 3-26(d)]. Such a switching behavior indicate that the turn-off process is more complicated and consumes more power than the turn-on process, which exhibits the same tendency with the different transition speeds in dynamic pulse voltage analyses of the SZO-based ERE device [23].

3.8 Forming Process

The forming process is necessary for the SZO-based memory device to perform the stable resistive switching behavior. The forming process is defined as applying a sufficiently high voltage on an as-prepared SZO-based memory device (never applied with any electric signal) to switch it from original state to LRS. After that, the SZO-based memory device can be repeatedly switched between LRS and HRS, but never be switched back to the original state by applying any sweep voltage. Fig. 3-27(a) shows the forming process and the I-V curve after the forming of the 0.3%-V:SZO ERE device,

showing that applying a negative voltage to the as-prepared device can switch the device from original state to LRS. However, applying a positive voltage to the as-prepared device cannot switch the device from the original state to the stable HRS, which can be explained by the hypothetical band diagrams of the interface between the SZO and LNO films shown in Figs. 3-27(b) to (d). The original state current in the as-prepared SZO-based ERE device follows the Schottky behavior indicated in the inset of Fig. 3-27(a), which is similar to a Schottky-like behavior in the reported interface between Nb-doped STO and SRO films [22]. Fig. 3-27(b) shows a hypothetical band diagram of the Schottky-like contact of the as-prepared SZO and LNO films, implying that the original state current follows the Schottky behavior. Fig. 3-27(c) exhibits the band diagram obtained when applying a negative voltage to the as-prepared SZO-based ERE device, which facilitates a switching of the device from original state to LRS. After the forming process, the conduction band of the SZO film near the interface can be modulated by charging or decharging the interface states, and then an Ohmic-like contact of the SZO/LNO interface is formed as indicated in Fig. 3-27(d). However, applying a positive bias voltage to the as-prepared SZO-based ERE device cannot modulate the Schotty-like contact into the Ohmic-like contact. Consequently, a positive sweep voltage cannot switch the device from the original state to a stable HRS. So, the forming process can be considered as the modulation of the SZO/LNO interface, leading to the resistive switching of the as-prepared SZO-based ERE device from original state to LRS.

3.9 Summaries

The resistive switching properties of the SZO-based ERE devices are investigated in this chapter. The 600°C-annealed LNO BE with smooth surface has the (100) and (200) orientations. The SZO films with different doping concentration deposited on the LNO

BEs also have (100) and (200) preferred orientations, which have been proposed that a SZO film with (100) preferred orientation had good resistive switching behavior [27].

The doping effect is discussed in this chapter. The pure SZO ERE device possesses the resistive switching characteristic, which is considered as an intrinsic property of the SZO-based memory device. Besides, a proper concentration of doping into the SZO film can improve the resistive switching properties, such as resistance ratio and stability. The resistance ratio between two resistance states of the 0.3%-V:SZO ERE device retains 1000 after applying 100 voltage sweeping cycles. This device has stable resistive switching properties even when the measurement is performed at 100°C. The retention time of the device is longer than 10^7s. The nondestructive readout property of the device is also examined in this chapter.

Based on the size effect [39], the current density of LRS of the 0.3%-V:SZO ERE device measured at -1V is estimated of 6.3×10^5 A/cm^2 for the 0.1μm technology node as shown in Fig. 3-28, which is conformed to the criterion of the RRAM indicated in Sec. 1.3.7. Besides, the resistance values of LRS and HRS of the device indicated in Fig. 3-10(a) are about 10kΩ and 100MΩ measured at -1V, respectively.

The resistive switching mechanism of the SZO-based ERE devices is the formation and disruption of the current paths, which is possibly attributed to the storage and release of carriers in the trap states of the SZO film. The conduction mechanisms of LRS and HRS currents of the SZO-based memory device are dominated by Ohmic conduction and F-P emission, respectively. In addition, the forming process of the device is firstly proposed of the modulation of the SZO/LNO interface, which can be used to explain the switching behavior from the original state to LRS.

In summary, the 0.3%-V:SZO ERE device has good resistive switching characteristics, such as high stability, good endurance, and long retention time, which make it a promising candidate for next-generation NVM applications.

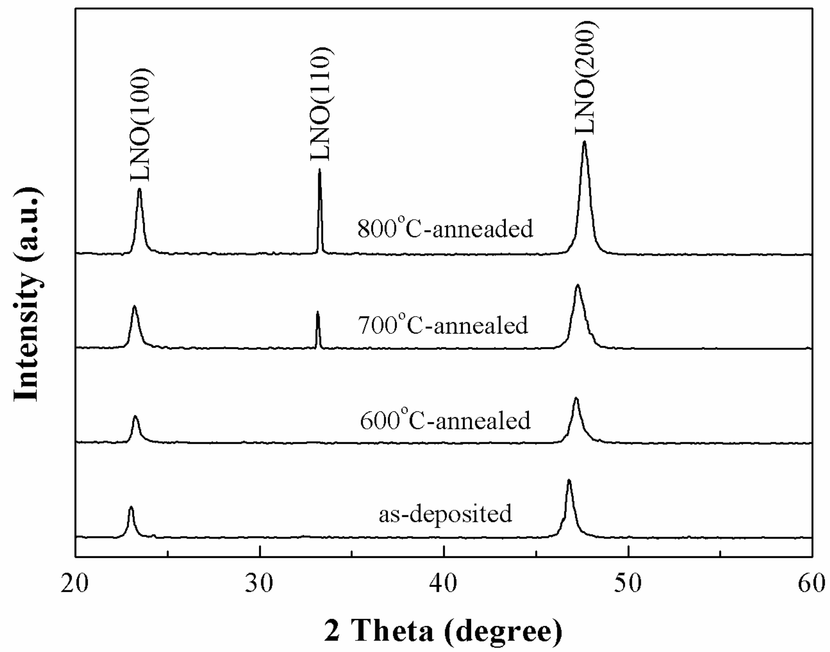


Fig. 3-1 XRD patterns of the as-deposited LNO, and 600, 700, and 800°C-annealed LNO films.

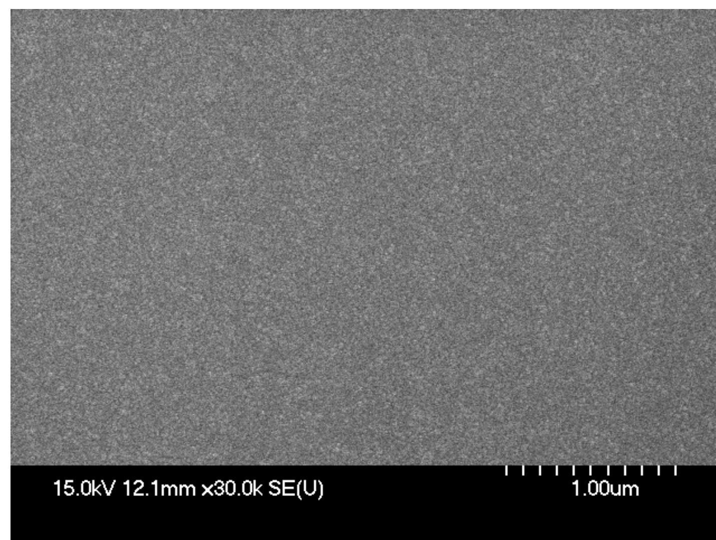


Fig. 3-2 Surface SEM image of the 600°C-annealed LNO film.

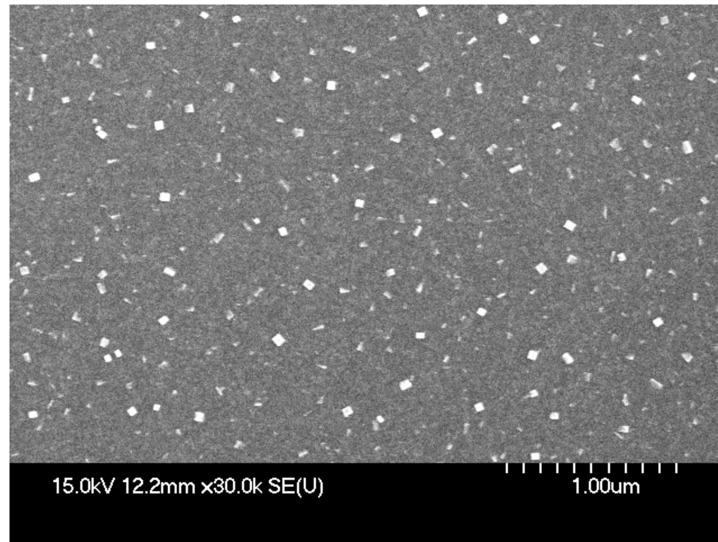


Fig. 3-3 Surface SEM image of the 700°C-annealed LNO film.

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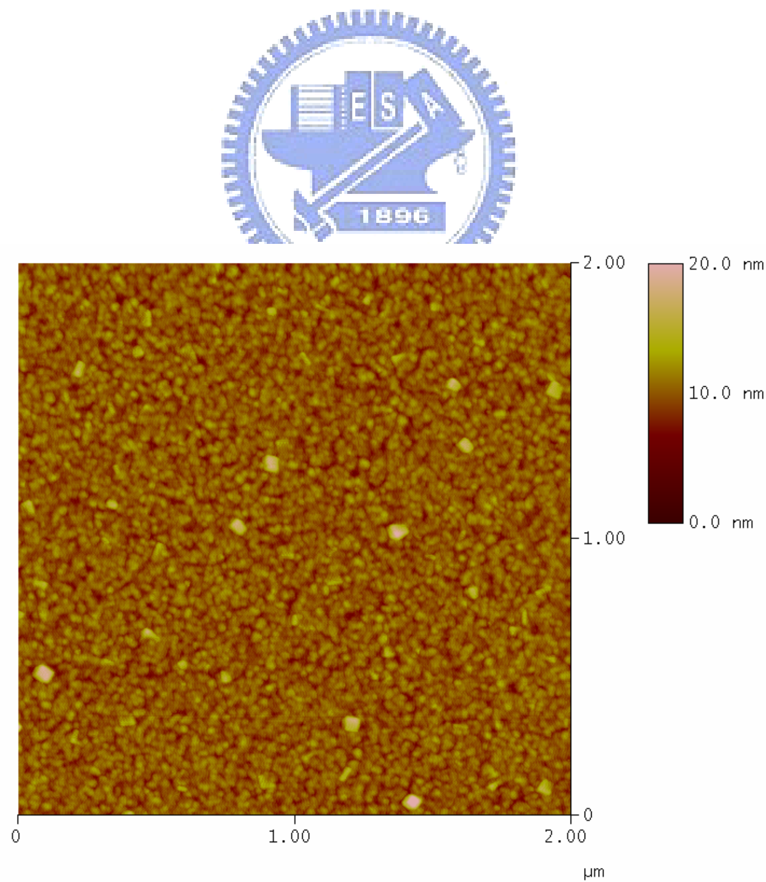


Fig. 3-4 Surface AFM image of the 600°C-annealed LNO film.

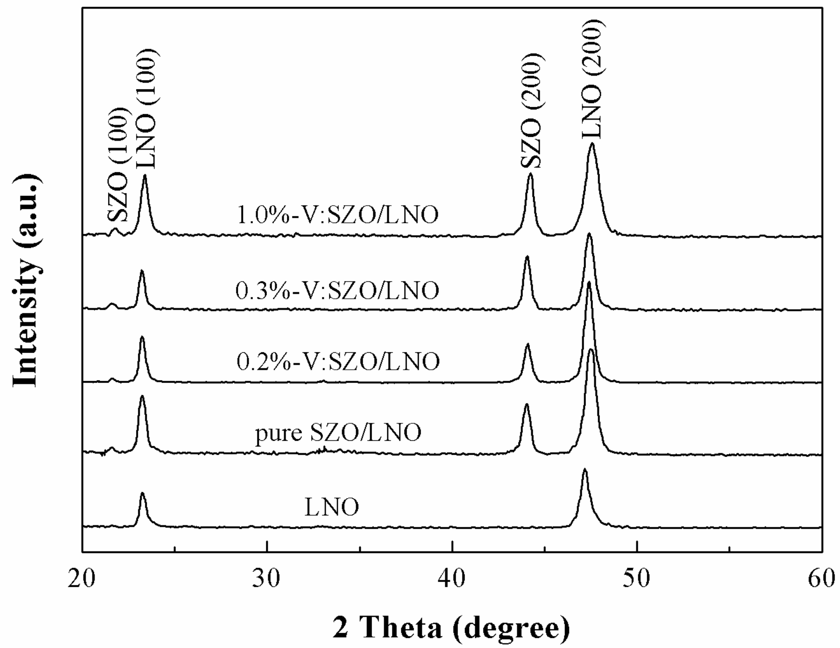


Fig. 3-5 XRD patterns of the 600°C-annealed LNO film, and the SZO films with different doping concentration deposited on the 600°C-annealed LNO films.

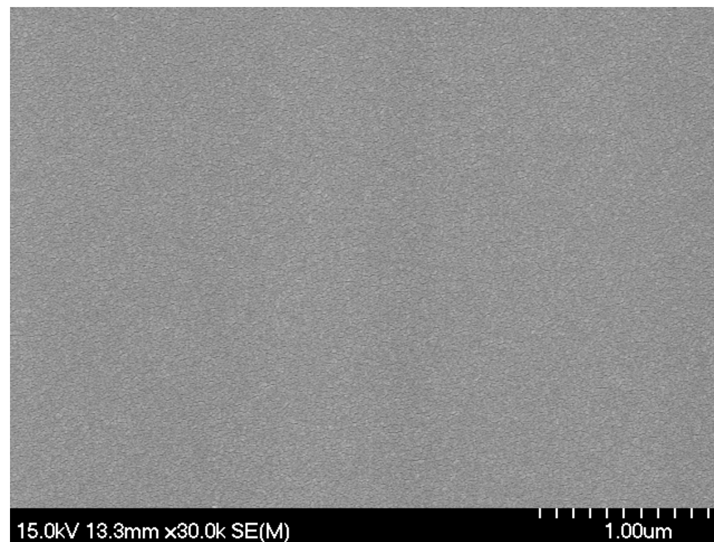


Fig. 3-6 Surface SEM image of the 0.3%-V:SZO film deposited on the LNO film.

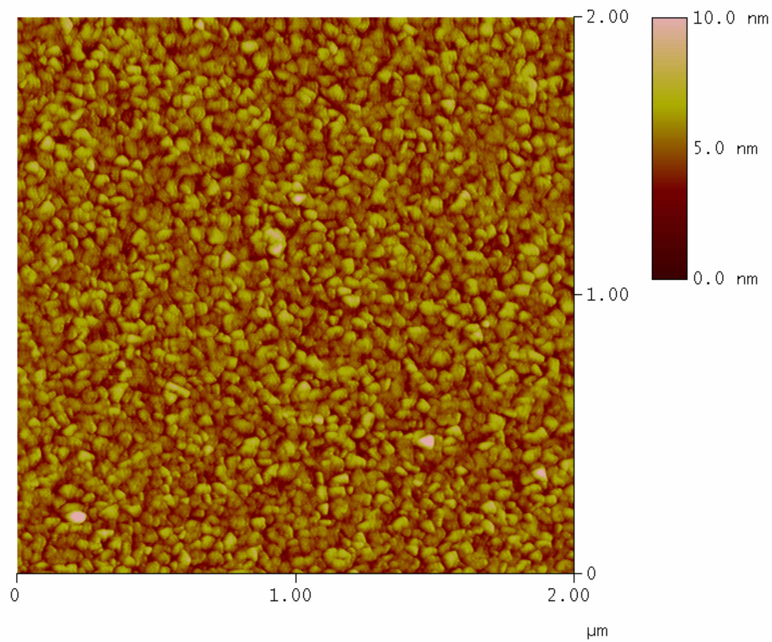
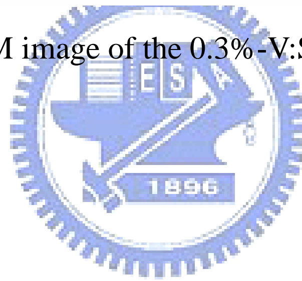


Fig. 3-7 Surface AFM image of the 0.3%-V:SZO film on the LNO film.



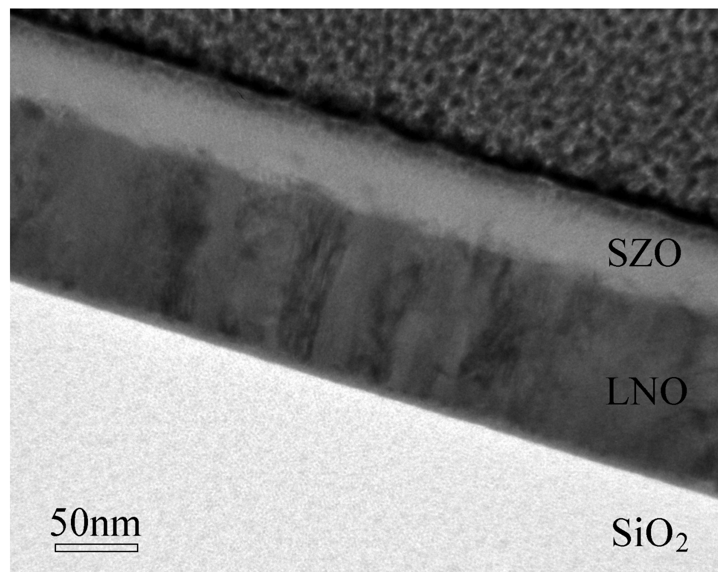


Fig. 3-8 Cross section TEM image of the 0.3%-V:SZO/LNO/SiO_2 structure.

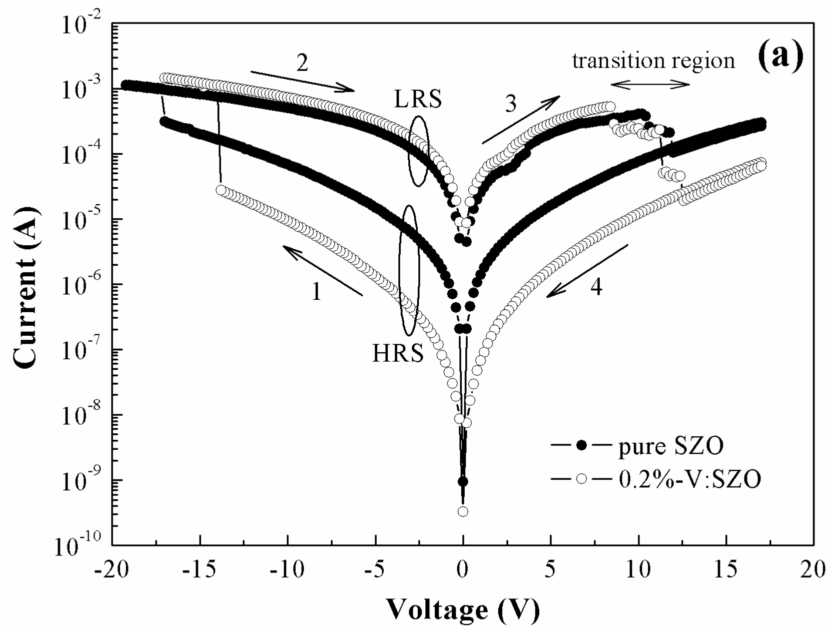


Fig. 3-9(a) I-V curves of the pure SZO and 0.2%-V:SZO ERE devices.

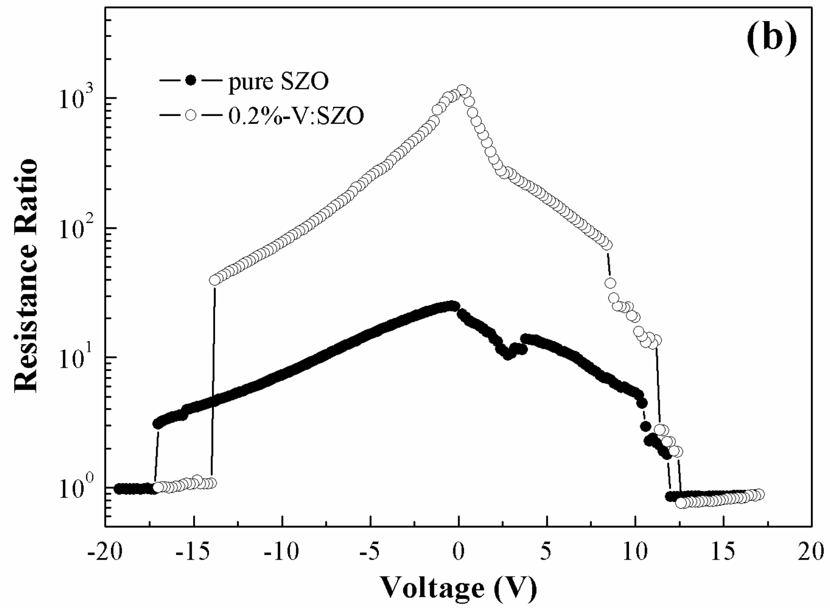


Fig. 3-9(b) Resistance ratios of the pure SZO and 0.2%-V:SZO ERE devices.

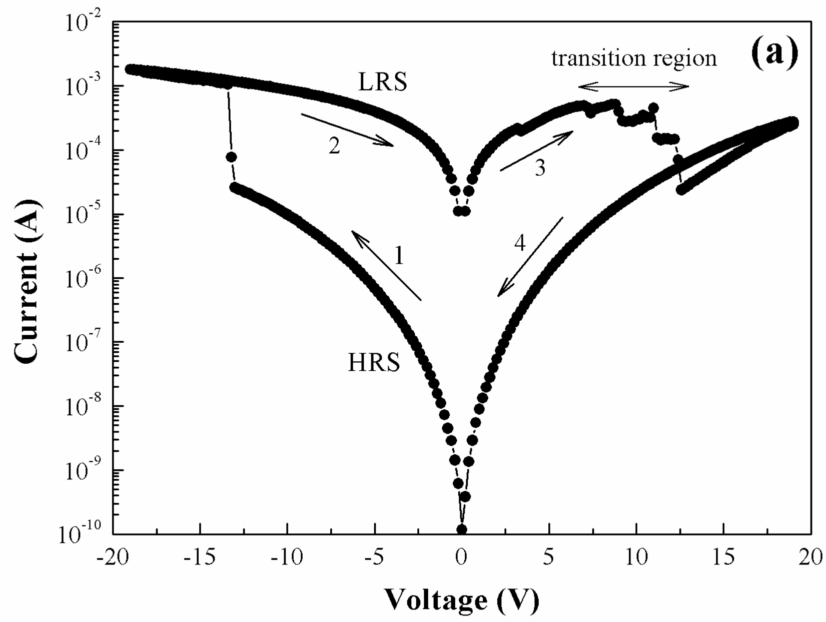
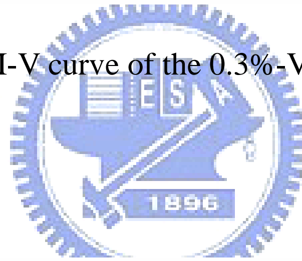


Fig. 3-10(a) I-V curve of the 0.3%-V:SZO ERE device.



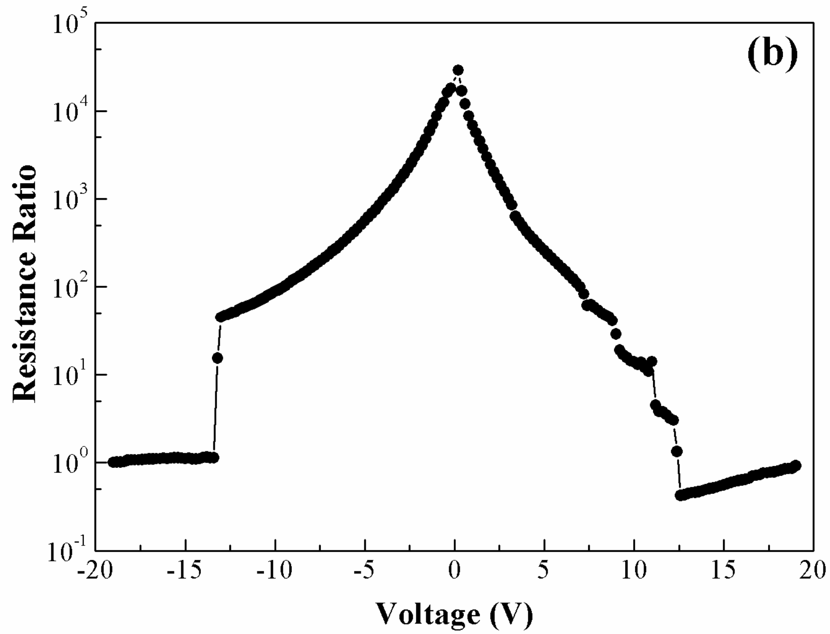


Fig. 3-10(b) Resistance ratio of the 0.3%-V:SZO ERE device.

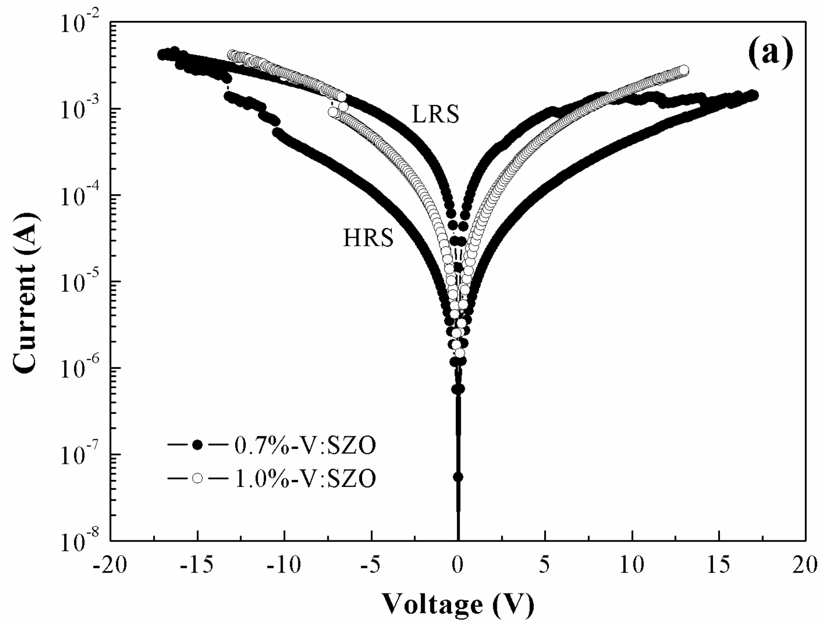


Fig. 3-11(a) I-V curves of the 0.7%-V:SZO and 1.0%-V:SZO ERE devices.

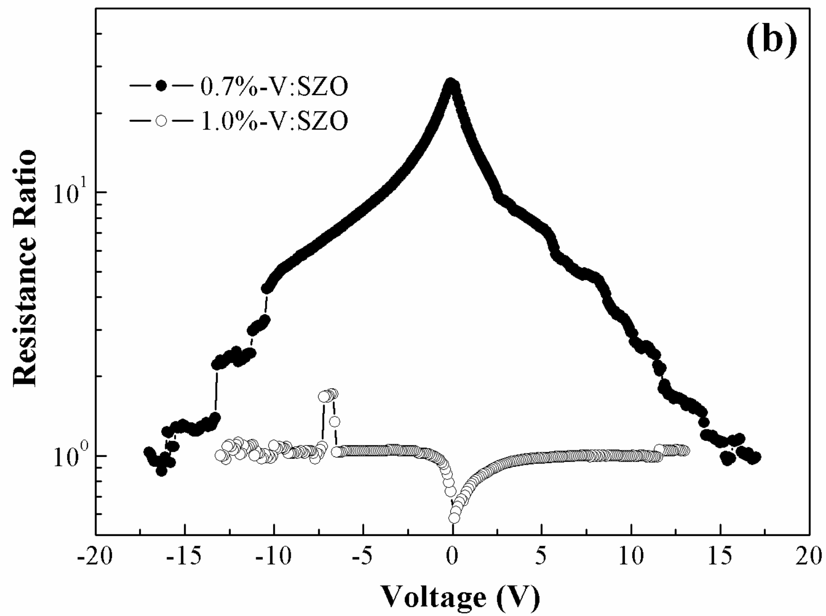


Fig. 3-11(b) Resistance ratios of the 0.7%-V:SZO and 1.0%-V:SZO ERE devices.

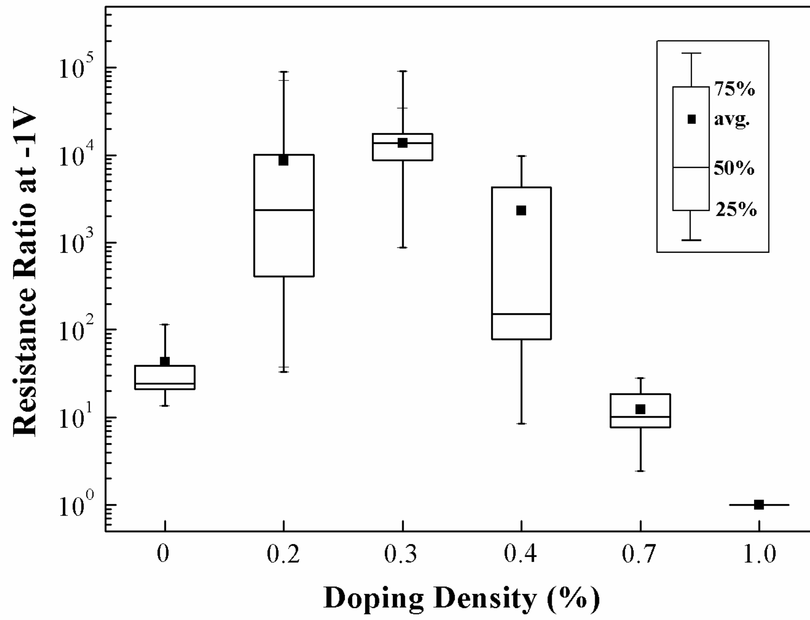


Fig. 3-12 Statistical chart of the resistance ratios of pure SZO, and 0.1%-V:SZO to 1.0%-V:SZO ERE devices.

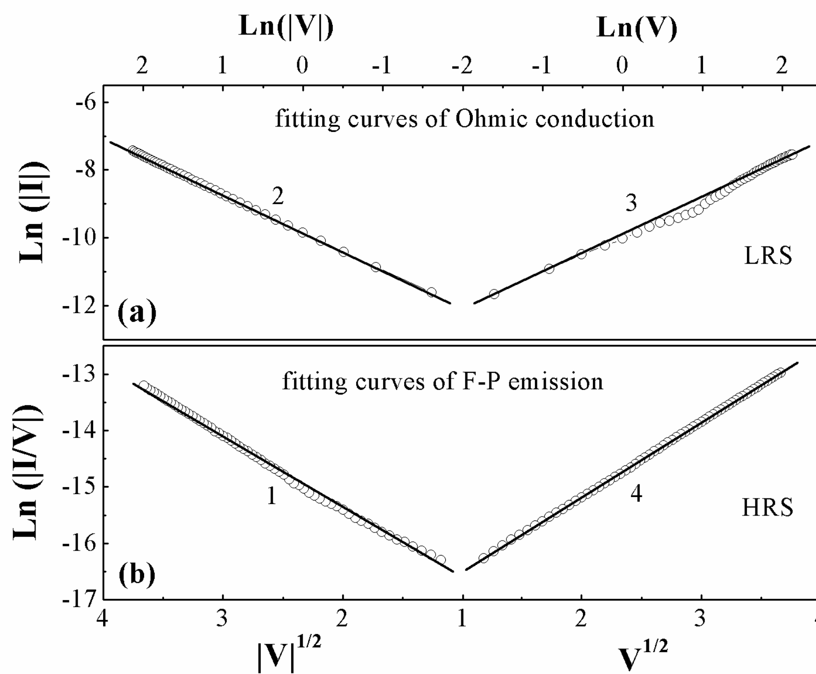


Fig. 3-13 Fitting curves of the LRS and HRS currents of the 0.2%-V:SZO ERE device by (a) Ohmic conduction, and (b) F-P emission.

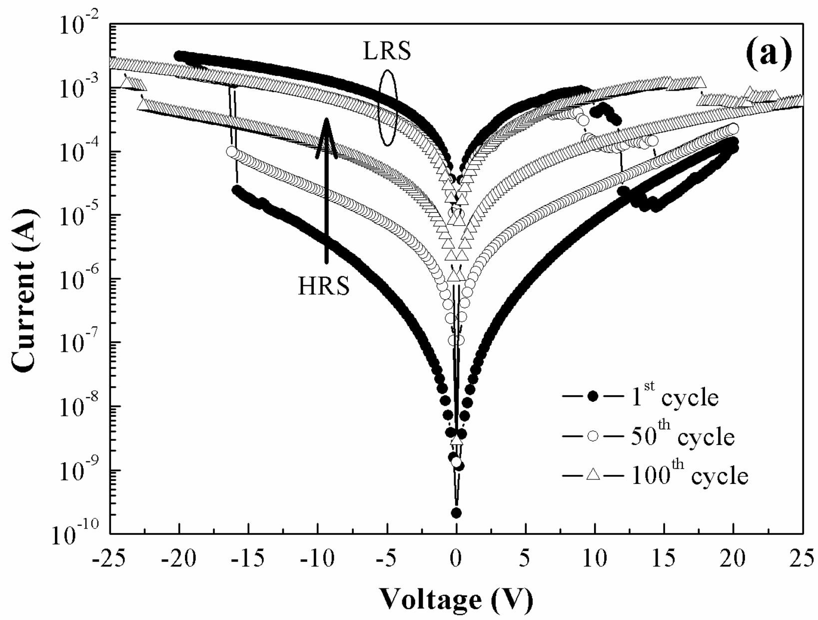


Fig. 3-14(a) Endurance of the 0.2%-V:SZO ERE device.

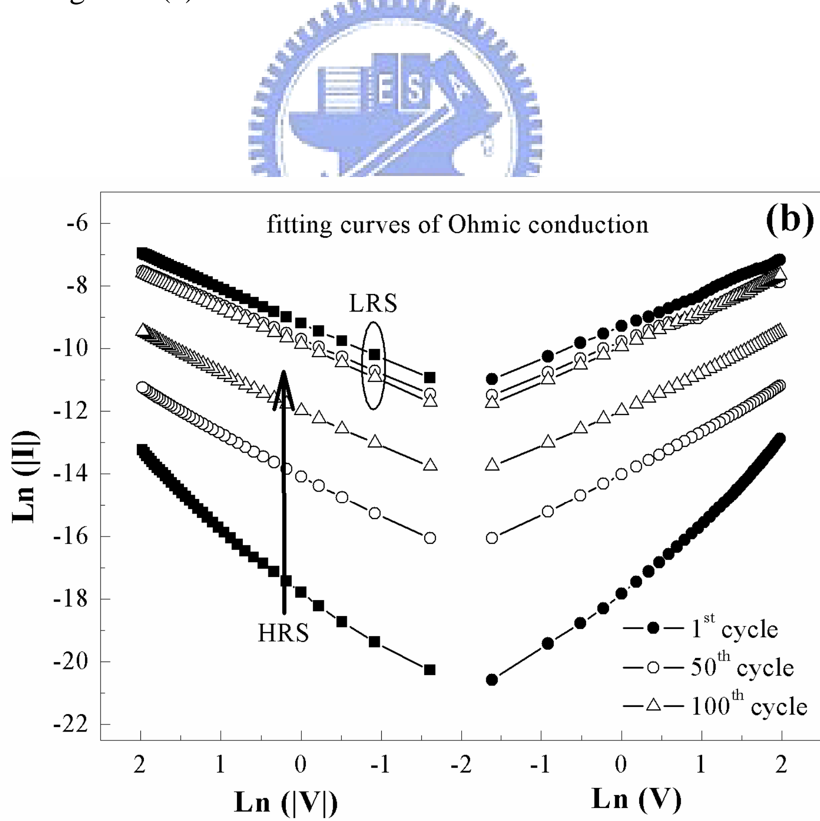


Fig. 3-14(b) Ohmic conduction fitting curves for the 1st, 50th, and 100th voltage sweeping cycles of the 0.2%-V:SZO ERE device.

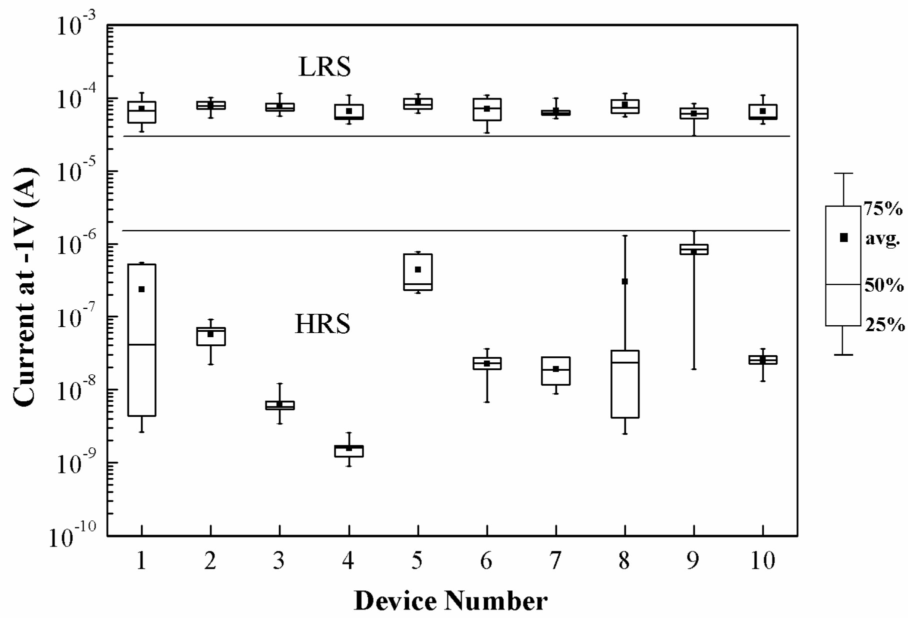


Fig. 3-15 Statistical chart of both LRS and HRS currents of the 0.2%-V:SZO ERE device measured at -1V.

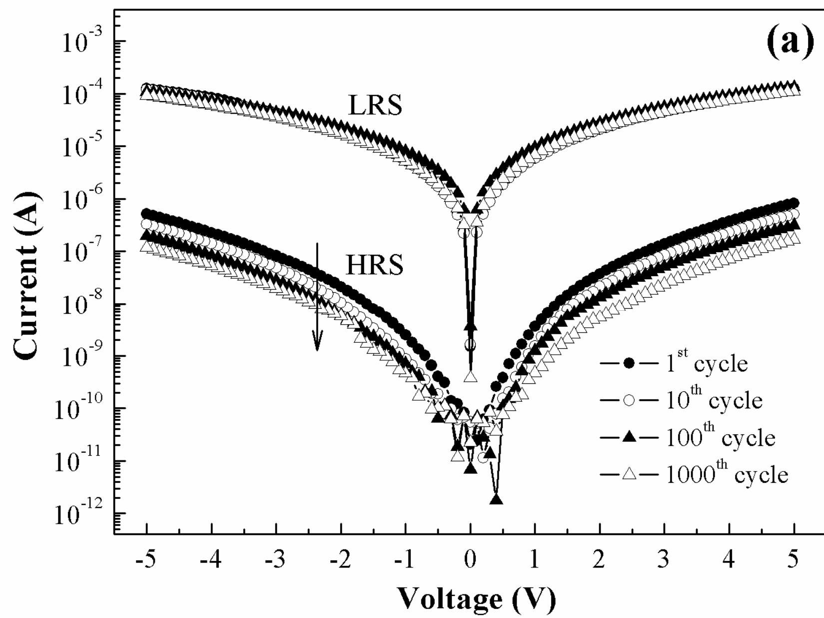


Fig. 3-16(a) Nondestructive readout property of the 0.2%-V:SZO ERE device measured at RT.

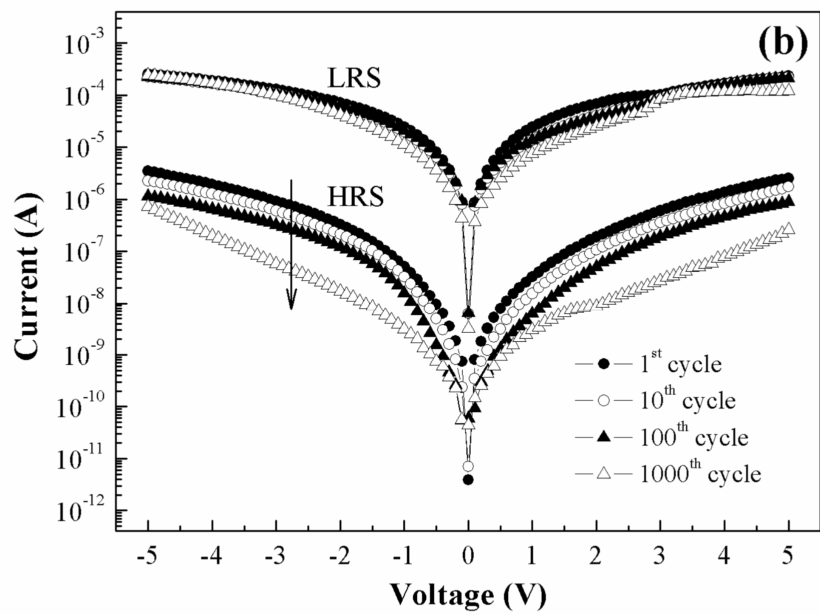


Fig. 3-16(b) Nondestructive readout property of the 0.2%-V:SZO ERE device measured at 85°C.

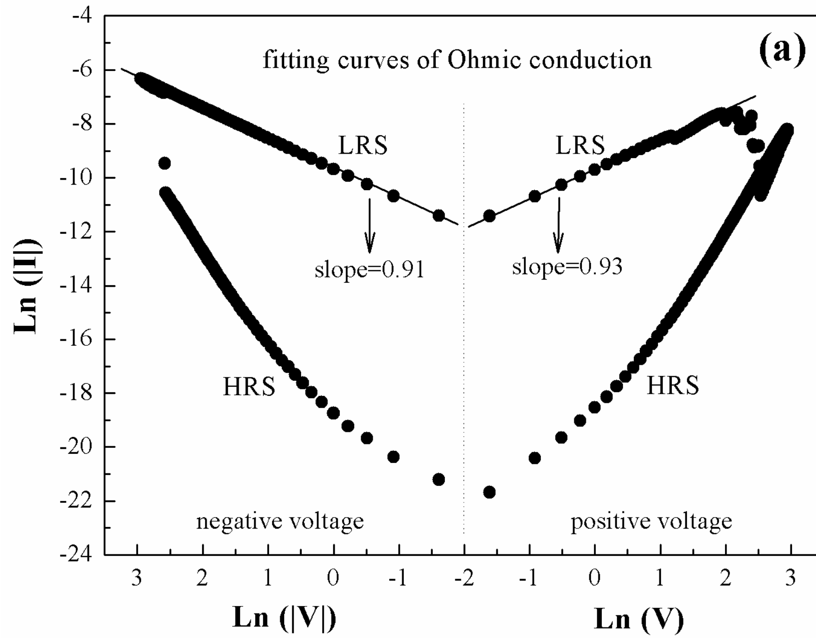


Fig. 3-17(a) Fitting curves of both LRS and HRS currents of the 0.3%-V:SZO ERE device by Ohmic conduction.

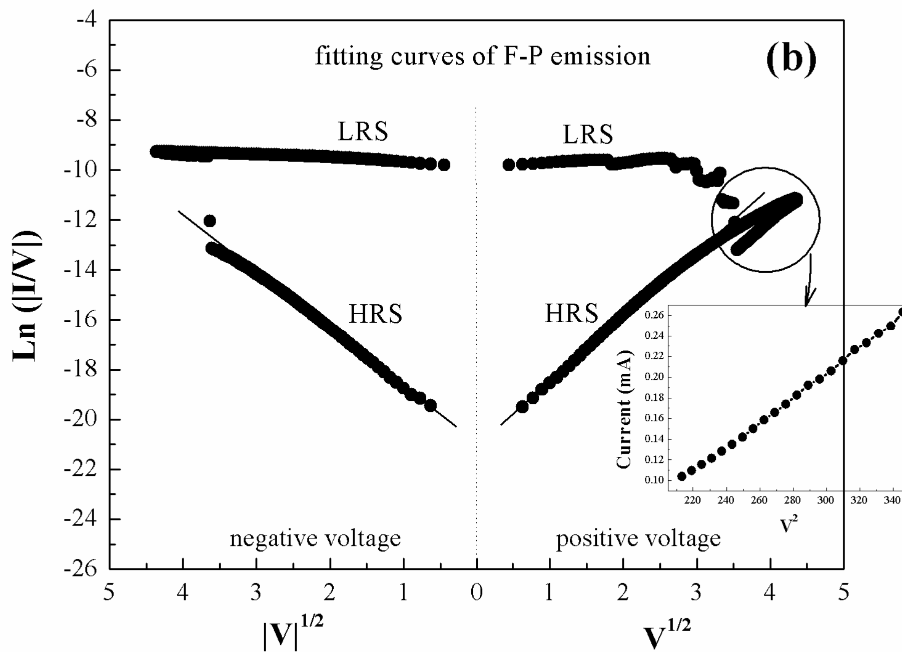


Fig. 3-17(b) Fitting curves of the LRS and HRS currents of the 0.3%-V:SZO ERE device by F-P emission. The inset is the fitting curve of HRS current by SCLC at high voltage.

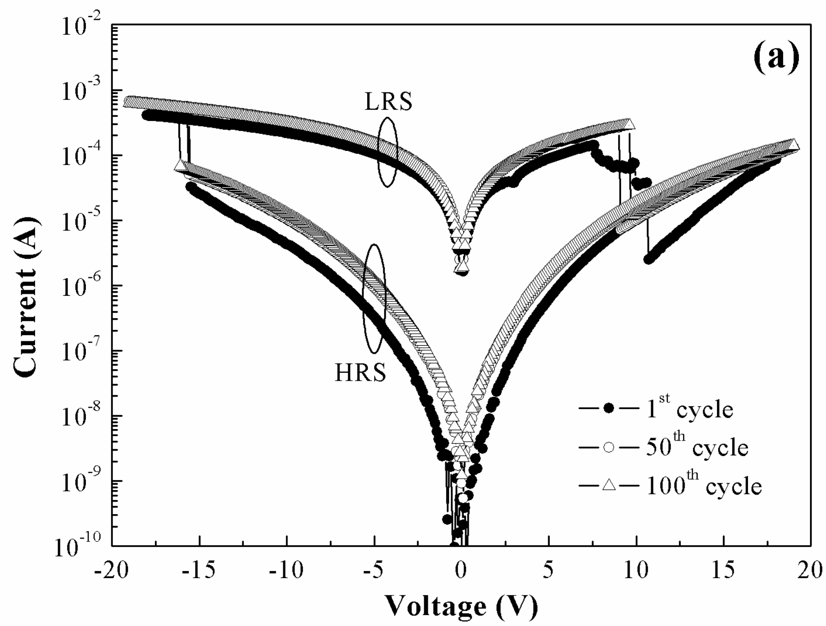


Fig. 3-18(a) I-V curves of the 0.3%-V:SZO ERE device for the 1st, 50th, and 100th voltage sweeping cycles.

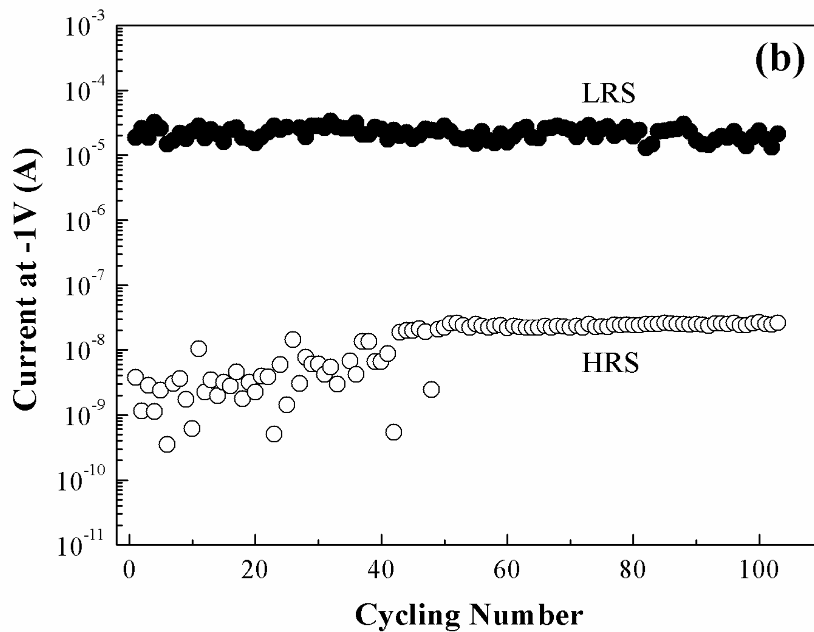


Fig. 3-18(b) Endurance of the 0.3%-V:SZO ERE device.

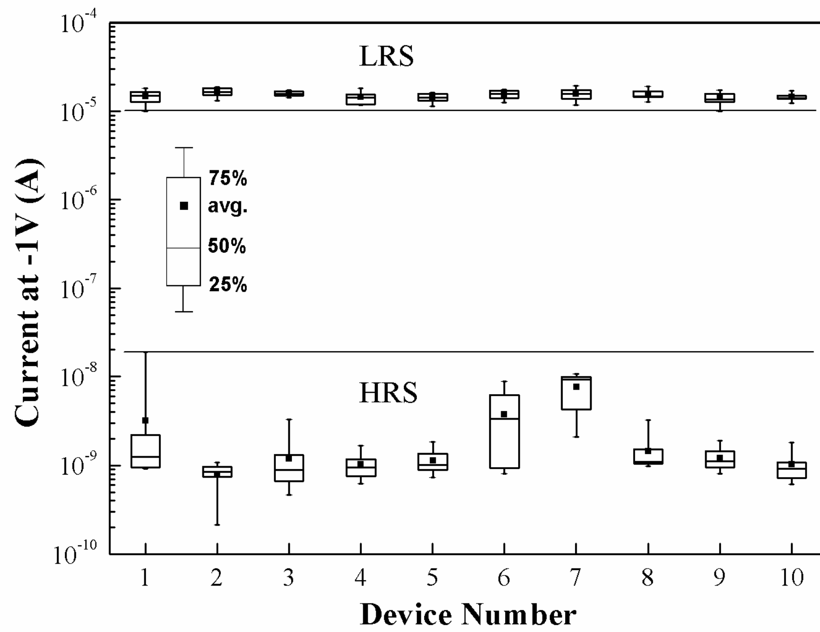


Fig. 3-19 Statistical chart of both LRS and HRS currents of the 0.3%-V:SZO ERE device measured at -1V.

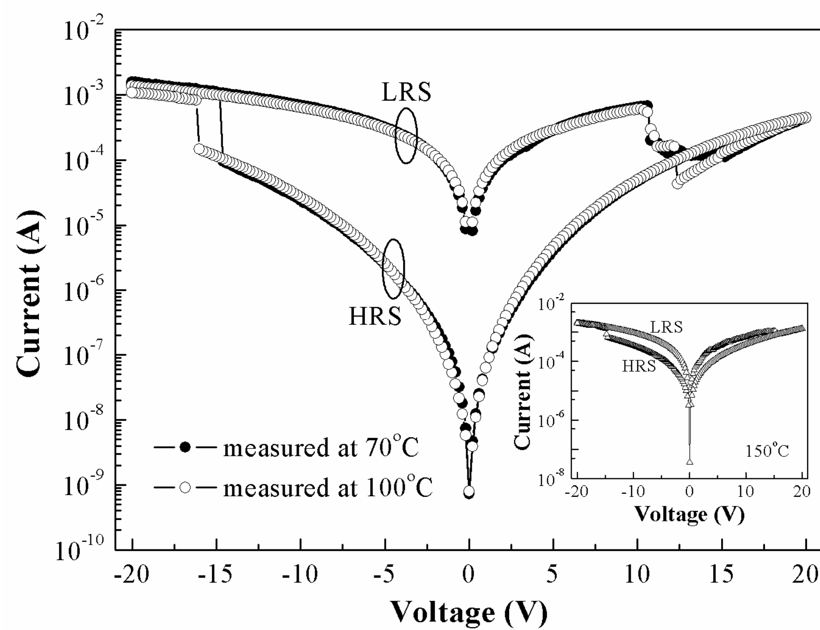


Fig. 3-20 I-V curves of the 0.3%-V:SZO ERE device measured at 70 and 100°C. The inset is the I-V curve of the device measured at 150°C.

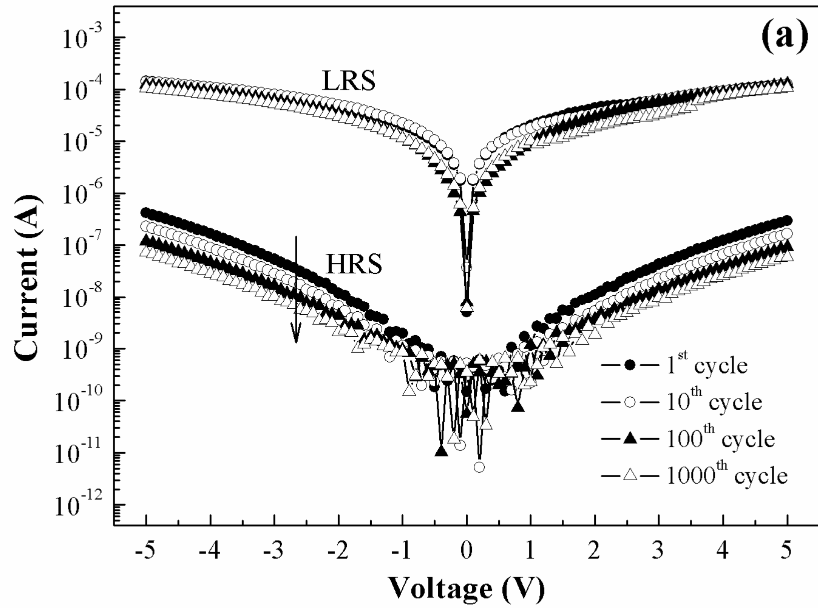


Fig. 3-21(a) Nondestructive readout property of the 0.3%-V:SZO ERE device measured at RT.

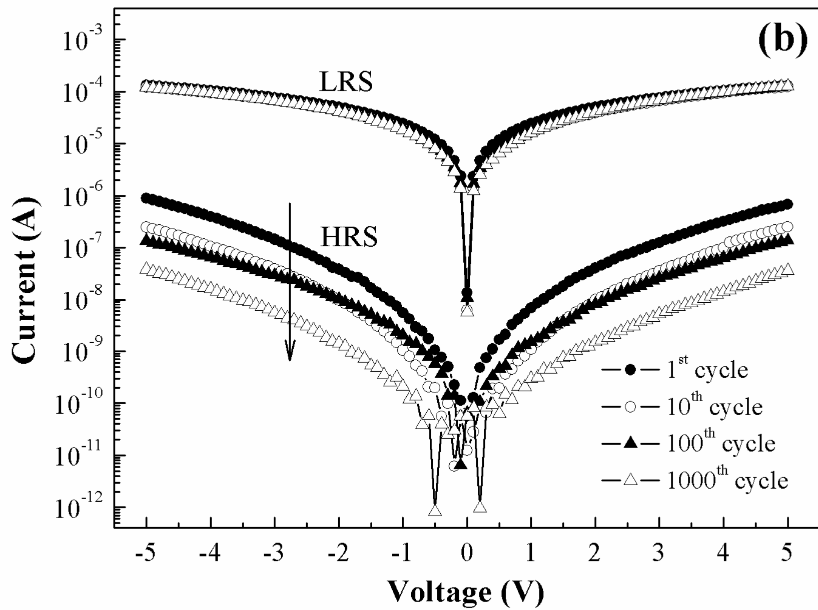


Fig. 3-21(b) Nondestructive readout property of the 0.3%-V:SZO ERE device measured at 85°C.

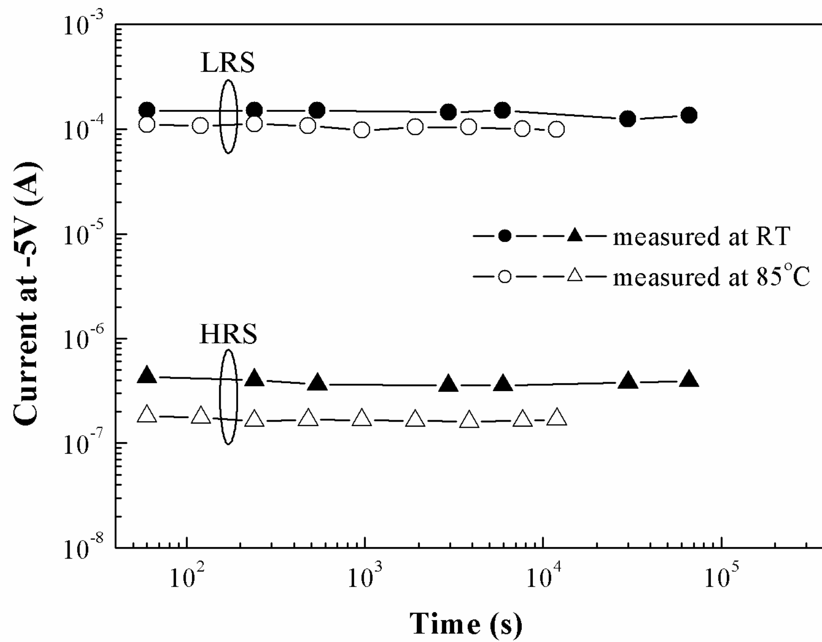


Fig. 3-22 Nondestructive readout property of the 0.3%-V:SZO ERE devices.

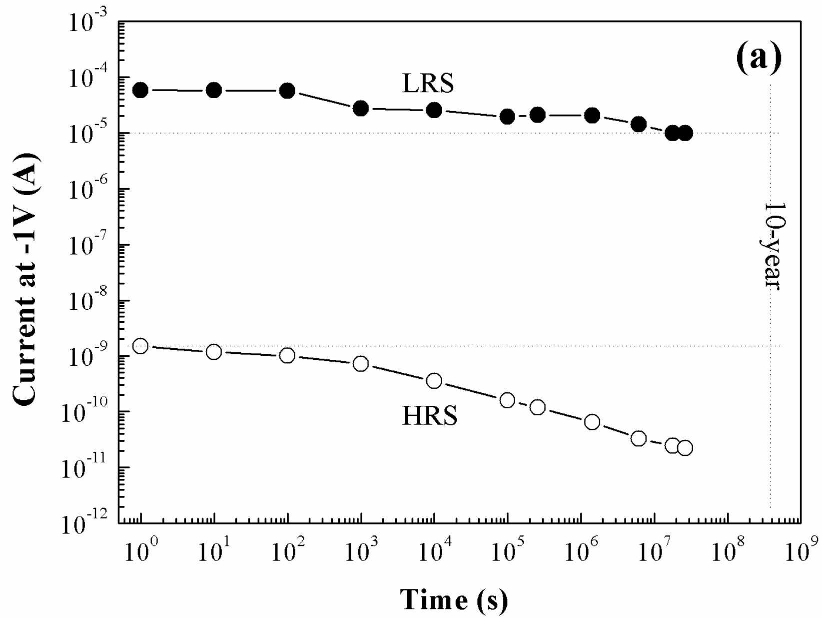


Fig. 3-23(a) Retention time of the 0.3%-V:SZO ERE devices measured at RT.

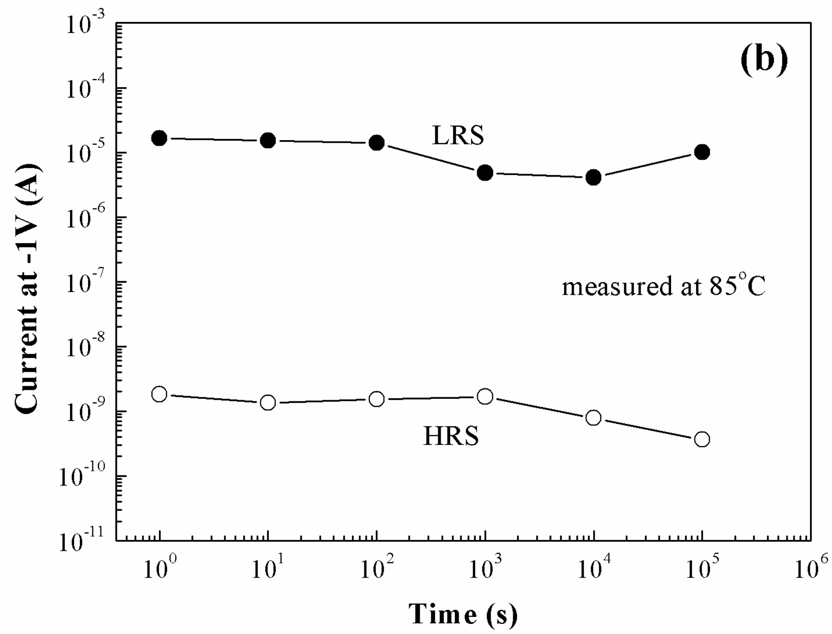


Fig. 3-23(b) Retention time of the 0.3%-V:SZO ERE devices measured at 85°C.

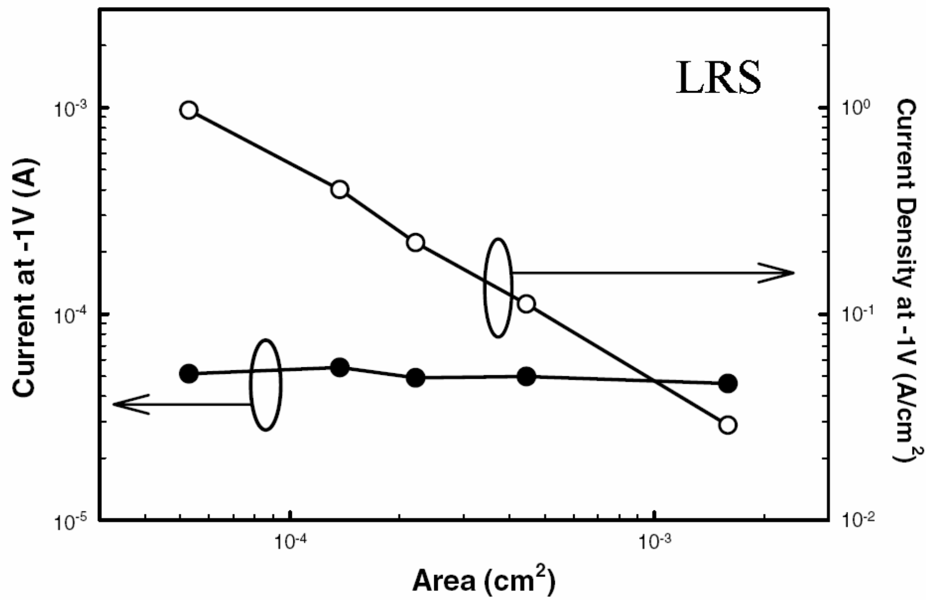


Fig. 3-24 Plot of the current and current density of LRS versus the area of TE [39].

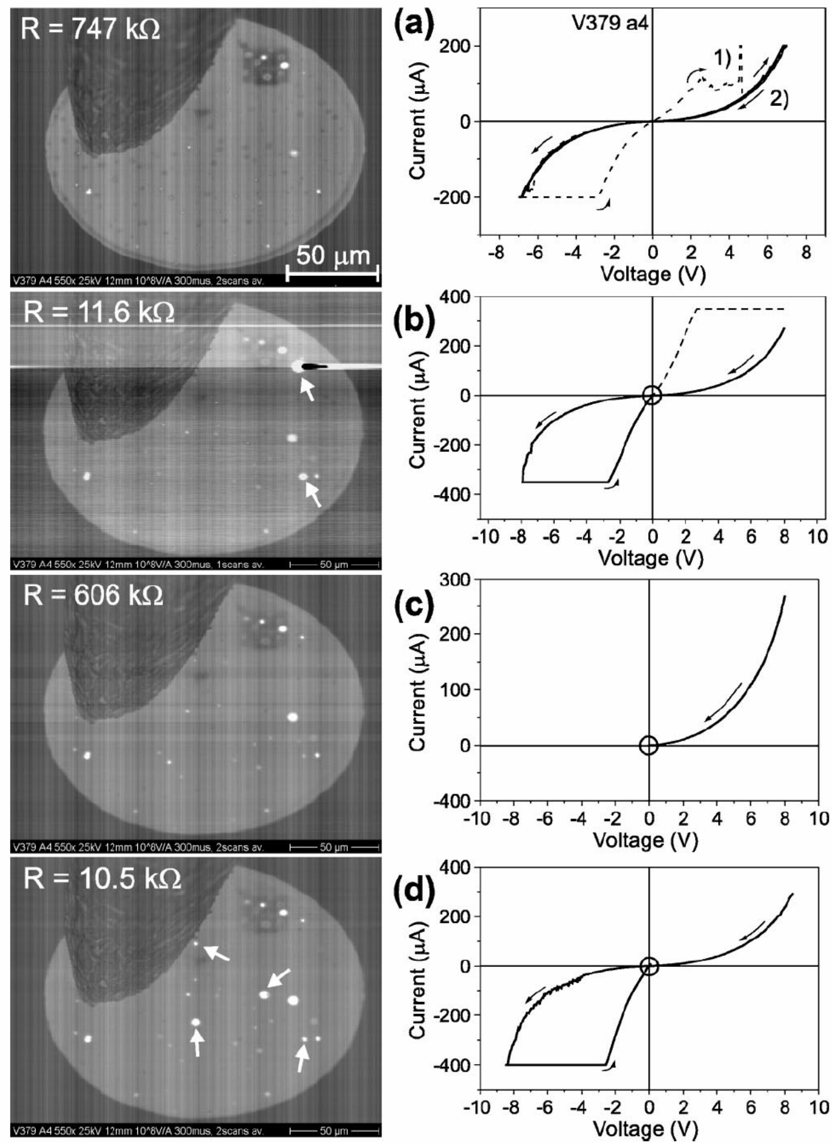


Fig. 3-25 The EBIC images and the corresponding I-V curves of the SZO-based memory device of (a) initial HRS, (b) LRS, (c) another HRS, and (d) another LRS [19].

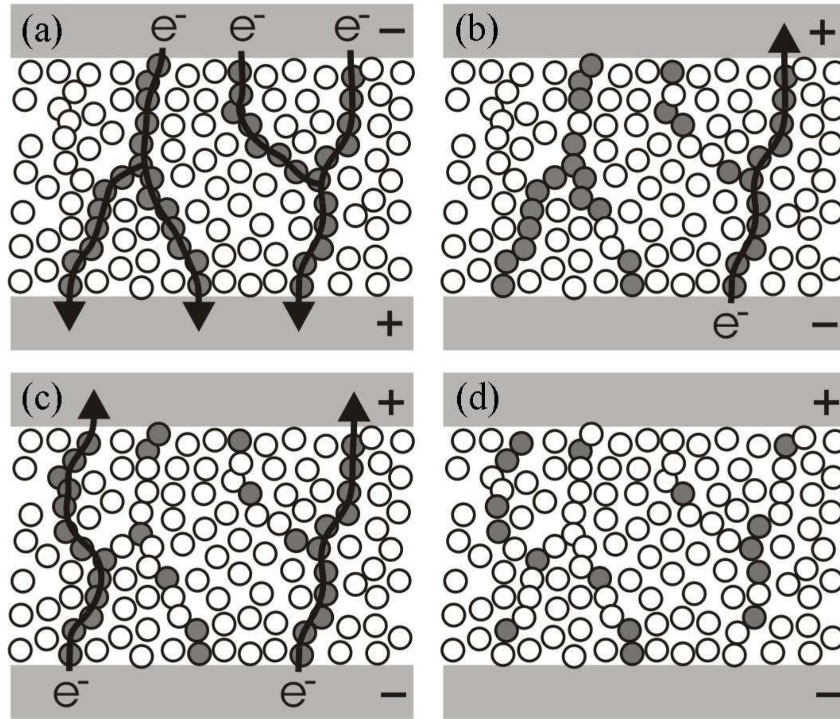


Fig. 3-26 Hypothetical diagrams of the current paths of (a) the turn-on process, and (b) to (d) the turn-off process (in the transition region).

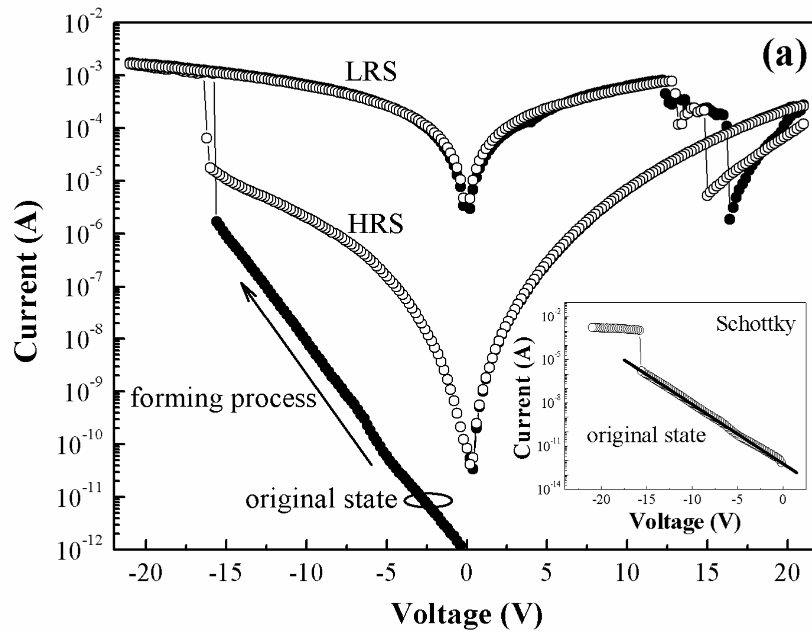
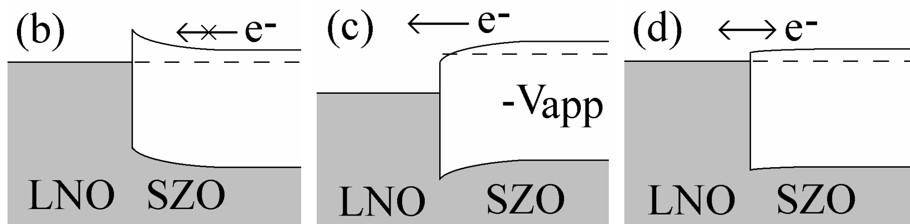


Fig. 3-27(a) Forming process of the 0.3%-V:SZO ERE device. The inset is the fitting curve for Schottky behavior of the original state current of the device.



Figs. 3-27(b) to (d) Hypothetical band diagrams (b) before forming, (c) during forming, and (d) after forming of the LNO/SZO interface.

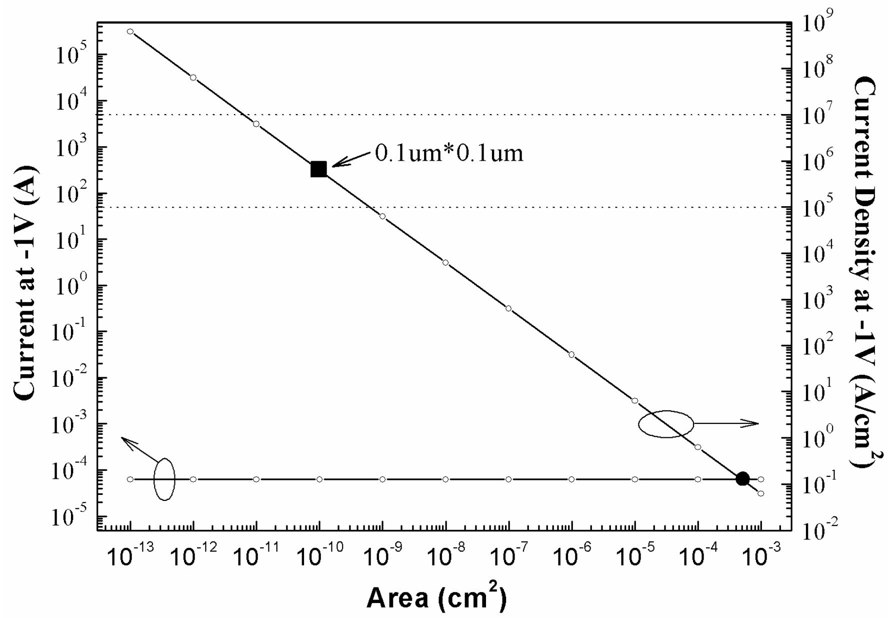
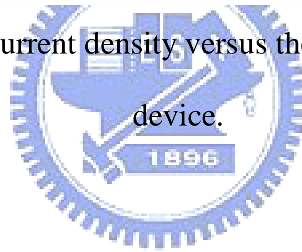


Fig. 3-28 Estimation plot of current density versus the area of TE of the SZO-based ERE device.



Chapter 4

Results and Discussion of Nonpolar Resistive Switching in the $SrZrO_3$-based Electrode/Resistor/Buffer/Electrode Devices

4.1 Introduction

The nonpolar resistive switching properties of the SZO-based electrode/resistor/buffer/electrode (ERBE) devices are discussed in this chapter. Based on the material of the resistive layer, the studies of RRAM can be classified into four groups, containing doped SZO and STO [18]-[40], transition metal oxides [16], [17], [41]-[76], PCMO and LCMO [1], [22], [77]-[99], and organic and polymer materials [15], [100]-[110]. However, the resistive switching voltage, nonpolar or bipolar switching, and polarity of bipolar switching of these devices are quite different from each other. For instance, Choi *et al.* proposed that the Pt/TiO_2/Ru device was nonpolar switching [49], while Fujimoto *et al.* reported that the Pt/TiO_2/TiN device was bipolar switching [65]. Besides, the resistive switching behavior of the SZO-based memory devices in the previous studies has been reported of the bipolar switching, and hence, the bipolar switching was considered as an intrinsic property of the SZO-based memory device. Nevertheless, in this dissertation, we firstly proposed the nonpolar resistive switching properties of the SZO-based ERBE devices achieved by using Pt and Al for BE and TE, respectively. The resistive switching time of the device reported in this dissertation is 10ns, which is the fastest speed in comparison with the previous reports [18], [23], [24]. The fabricating process of the SZO-based ERBE device is shown in Sec. 2.3 (Sample Preparation II).

4.2 Properties of the $LaNiO_3$ Buffer Layer and $SrZrO_3$ Resistive Layer

Fig. 4-1 depicts the XRD patterns of the 600°C-anneaded LNO films deposited on the SiO_2/Si and Pt/Ti/SiO_2/Si substrates, showing that the LNO film deposited on the Pt/Ti/SiO_2/Si substrate also has (100) and (200) orientations, which have been reported that a SZO film deposited on the (100)-orientated LNO film had good resistive switching behavior [27]. Figs. 4-2 and 4-3 show the surface SEM and AFM images of the 600°C-annealed LNO film deposited on the Pt/Ti/SiO_2/Si substrate. The LNO film performs a smooth surface, and the mean roughness and the RMS roughness of the LNO film are 2.218 and 2.842nm, respectively. Figs. 4-4 and 4-5 exhibit the surface SEM and AFM images of the 0.3%-V:SZO film deposited on the LNO/Pt/Ti/SiO_2/Si substrate. The mean roughness and the RMS roughness of the SZO film are 1.458 and 2.035nm, respectively. The roughness of the LNO and SZO films deposited on two kinds of substrates are presented in Table 4-1, indicating that the surface roughness of the SZO film deposited on the LNO/Pt/Ti/SiO_2/Si substrate is a little higher than that deposited on the LNO/SiO_2/Si substrate.

4.3 Nonpolar Resistive Switching Properties of the 0.3%-V-doped $SrZrO_3$ Electrode/Resistor/Buffer/Electrode Devices

Fig. 4-6(a) depicts the I-V curve of the 0.3%-V:SZO ERBE device. When a sweep voltage is applied from zero to +7 or -7V, the current of the device rapidly increases, and the device is switched from HRS to LRS (turn-on). On the other hand, when a sweep voltage is applied from zero to +2 or -2V, the current decreases suddenly and the device is switched from LRS back to HRS (turn-off). The current compliance is set at 1mA during the turn-on process for preventing the degradation of the device, but no current compliance is used in the turn-off process. The voltage window between turn-on and

turn-off processes is clear enough for accurate switching the device. The nonpolar resistive switching behavior is firstly proposed in the SZO-based memory device. The LRS resistance of the device is about 15Ω, and the equivalent circuit of this device is shown in Fig. 4-7(a), where the parasitic capacitance is assumed to be ignored. The following is the series resistance of this device:

$$R_{SZO}+R_{LNO}+R^{C}_{Pt}+R_{P}=15\Omega \quad (4\text{-}1)$$

where R_{SZO}, R_{LNO}, R^{C}_{Pt}, and R_P are the thin film resistance of the SZO film and the contact resistance of the Al/SZO and SZO/LNO interfaces, the LNO thin film resistance and the LNO/Pt contact resistance, the crabwise resistance of the Pt BE, and other parasitic resistance, respectively. The resistance of each item shown in Eqn. (4-1) is lower than 15Ω. The resistance ratio between two resistance states of this device is higher than 10^7 measured at -1V, which is shown in Fig 4-6(b). In addition, a little asymmetric of the I-V curve of the device may be due to the different materials of BE and TE, which have different work functions and contact resistance with LNO and SZO films, respectively.

On the other hand, the bipolar resistive switching characteristics of the SZO-based memory devices are presented in chapter 3. The LRS resistance of the 0.3%-V:SZO ERE device shown in Fig. 3-10(a) is about 15kΩ, and the equivalent circuit of the device is shown in Fig. 4-7(b) (parasitic capacitance assumed to be ignored). The following is the series resistance of this device:

$$R_{SZO}+R^{C}_{LNO}+R_{P}=15k\Omega \quad (4\text{-}2)$$

where R_{SZO}, R^{C}_{LNO}, and R_P are the thin film resistance of the SZO film and the contact resistance of the Al/SZO and SZO/LNO interfaces, the crabwise resistance of the LNO BE, and other parasitic resistance, respectively. The resistance ratio between two resistance states of this device is higher than 10^4 measured at -1V [Fig. 3-10(b)]. However, the resistance ratio of this device is three orders of magnitude lower than that

of the 0.3%-V:SZO ERBE device owing to the difference between the LRS resistance of these two devices. Comparison with Eqns. (4-1) and (4-2), we can easily understand that the crabwise resistance of the LNO BE of the 0.3%-V:SZO ERE device mainly contributes to the LRS resistance, which is similar to the compliance effect although the resistance of the SZO films and parasitic resistance of two devices maybe have some differences under distinct turn-on processes. Therefore, the 0.3%-V:SZO ERBE device with lower resistive switching voltages and higher resistance ratio is more suitable for practical NVM applications. Besides, if the SZO film is directly deposited on Pt or other metals, such as Al, Ti, Ta, Zr, Ni, and Nb, no (100)-orientated film can be deposited. Therefore, the LNO buffer layer is needed for the SZO-based ERBE device with good resistive switching properties. Besides, in order to prove that the resistive switching does not occur in the LNO film, the resistive switching property was determined between Pt BE and LNO film as indicated in Fig. 4-7(a), no resistive switching behavior was observed. Hence, the resistive switching occurring in the LNO film can be eliminated. The voltage polarity of resistive switching will be discussed in Sec. 4.4.

Fig. 4-8(a) indicates the plots of Ln(|I|) versus Ln(|V|) of both LRS and HRS currents for the 0.3%-V:SZO ERBE device. The slopes of LRS curves close to unity, indicating that the LRS currents are dominated by Ohmic conduction. On the other hand, the HRS curves are not straight lines, implying that the HRS currents are dominated by other conduction mechanisms. Fig. 4-8(b) shows the plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of both HRS and LRS currents for the device. The linear fittings of the device indicate that the HRS currents follow the F-P emission at low voltage. These results are similar to that presented in chapter 3, which implies that the resistive switching mechanism can be considered as the formation and disruption of current paths. Besides, both Ohmic behavior and F-P emission are bulk conduction, so that the resistive switching occurring at the interface can be eliminated.

Fig. 4-9(a) shows the forming, turn-off, and turn-on processes of the 0.3%-V:SZO ERBE device by applying negative sweep voltages. After the forming process, the device can be repeatedly switched between LRS and HRS. Fig. 4-9(b) indicates the turn-on and turn-off voltage distributions of the device, showing that the turn-off voltages are more stable, while the turn-on voltages have a variation between -3 to -5.5V. In addition, the distributions of LRS and HRS currents are presented in Fig. 4-9(c), indicating that the LRS currents are more stable than HRS currents, which is corresponding to the results shown in Chapter 3.

Fig. 4-10 indicates the resistive switching speed of the SZO-based ERBE device. Fig. 4-10(a) shows the I-V curves of the device with HRS and after applying a -6V voltage pulse with 10ns period, indicating that the device is switched from HRS to LRS. On the other hand, this device is switched back to HRS after applying a -4V voltage pulse with 10ns period shown in Fig. 4-10(b). The switching speed of turn-on and turn-off processes is 10ns. Liu *et al*. had reported that the device with Al/SZO/LNO ERE structure can be turned on and turned off by applying -20V, 5ns and +20V, 500μs voltage pulses, respectively [23]. Obviously, the resistive switching speeds between turn-on and turn-off processes have a significant difference of five orders of magnitude. The asymmetry of resistive switching speeds can be explained by the LNO compliance effect. In the turn-off process, electrons are injected from the LNO BE to the resistive layer in the SZO-based ERE device, so the conductivity of the electrode will determine the resistive switching speed of the device. Therefore, the SZO-based memory device using Pt BE can significantly improve the resistive switching speed. In this dissertation, we propose that the 0.3%-V:SZO ERBE device with high-speed resistive switching within 10ns, which is the fastest speed in comparison with that reported in the previous studies [18], [23], [24].

Fig. 4-11(a) indicates the nondestructive readout property of the 0.3%-V:SZO

ERBE device. The currents of LRSs and HRSs switched by both sweep voltages and voltage pulses retain almost unchanged after continuously biased at -0.5V for more than 10^4s at RT, which indicates that the resistance states are not varied after performing 10^{12} of read pulses (assuming that a read pulse is -0.5V with 10ns period). Because a sweep voltage can be look on as a voltage pulse with infinite duration [114], the LRS/HRS current switched by the sweep voltage is higher/lower than that by the voltage pulse, and hence, the resistance ratio between two resistance states switched by sweep voltages is higher than that by voltage pulses. Fig. 4-11(b) performs the nondestructive readout property of the device switched by voltage pulses measured at 85°C, indicating that the resistance states are not varied after performing 10^{12} of read pulses at high temperature.

Fig. 4-12(a) depicts the I-V curves of the 0.3%-V:SZO ERBE device for the forming process, and 1st, 10th, and 50th voltage sweeping cycles measured at 150°C. The result shows that the resistive switching property of the device is not degraded while performed at 150°C. Fig. 4-12(b) indicates the distributions of turn-on and turn-off voltages, and Fig. 4-12(c) presents the distributions of LRS and HRS currents indicating that the LRS currents are very stable, and the HRS currents increase with the increased cycle number, which corresponds to the result shown in Fig. 3-18(b).

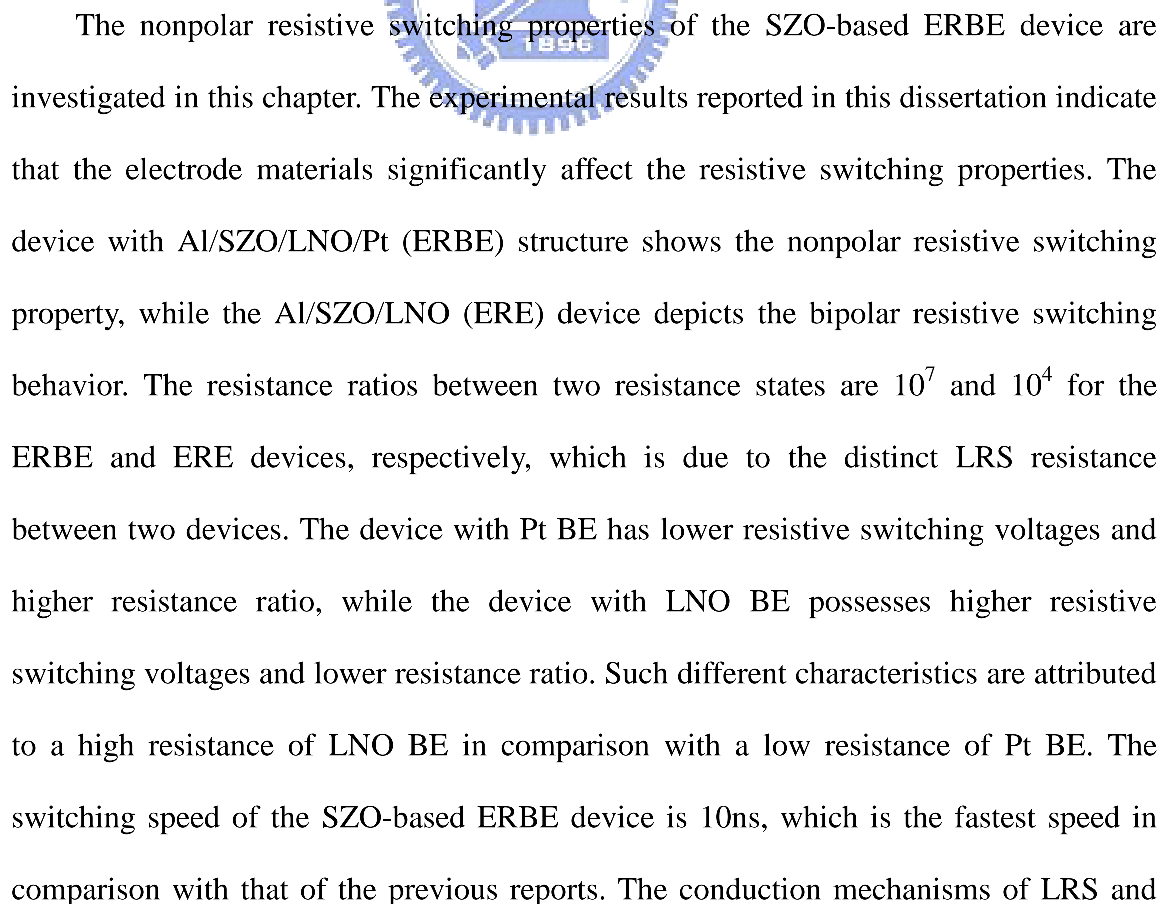
Fig. 4-13(a) shows the retention time of the 0.3%-V:SZO ERBE devices measured at RT, indicating that the retention time is longer than 10^7s, and the resistance ratio between two resistance states retains higher than 10^7. Fig. 4-13(b) performs the retention time of the devices switched at RT, and measured at high temperature, indicating that the retention time is longer than 6×10^6s, and the resistance ratio between two resistance states retains at 10^6.

4.4 Resistive Switching Polarities

Table 4-2 shows the resistive switching properties of SZO-, TiO_2-, and PCMO-based memory devices reported by several well-known research groups. Based on the experimental results shown in this chapter, the SZO-based memory device is nonpolar switching, which is different from the bipolar switching results reported in the previous studies [18], [30]. However, in their studies the polarities of turn-on and turn-off voltages are fully opposite; Beck *et al.* proposed that their device with Au/SZO/SRO structure could be turned on/off by applying a negative/positive sweep voltage [as shown in Fig. 4-14(a)] [18]; nevertheless, Park *et al.* reported that Pt/SZO/SRO device could be turned on/off by applying a positive/negative sweep voltage [Fig. 4-14(b)] [30]. The distinct resistive switching properties between these two studies might be due to their different top electrodes used. Therefore, these results indicate that the electrode materials used would determine the bipolar or nonpolar switching, and the polarity of the bipolar switching of the device. In Fig 3-10(a), for instance, when the device is turned on, electrons are injected from the Al TE into the SZO film; while in the turn-off process, electrons flow from the LNO BE into the SZO film slowly and trapped by defects uniformly. However, the device cannot be turned on by applying a positive voltage because the electrons injected from the LNO BE are trapped by the defects existed in the SZO film and cannot flow to the Al TE. Therefore, the distinct resistive switching properties of the devices shown in Figs. 4-6(a) (nonpolar switching) and 3-10(a) (bipolar switching) are due to the different BEs used. Similar results are also observed in the TiO_2- and PCMO-based memory devices. In the TiO_2-based memory devices, Choi *et al.* reported the nonpolar switching of the Pt/TiO_2/Ru device [49]; however, Fujimoto *et al.* proposed the bipolar switching of the Pt/TiO_2/TiN device [65]. In the PCMO-based memory devices, Sawa *et al.* reported the bipolar switching of the Ti/PCMO/SRO device [80], while Fujimoto *et al.* showed the

nonpolar switching of the Pt/PCMO/Pt device [97]. Consequently, we consider that the nonpolar switching is an intrinsic property of SZO-, TiO_2-, and PCMO-based memory devices; however, the electrode materials employed in the device would dominate their bipolar or nonpolar switching, and the polarity of bipolar switching. Therefore, the appropriate electrode materials chosen are indeed very important for obtaining the RRAM devices with excellent switching properties. However, other factors such as the conductivity and work function of electrodes, contact resistance between two films, microstructure of resistive layer, and work function difference and property in each interface are still needed for further detailed studies for developing an excellent RRAM device.

4.5 Summaries



The nonpolar resistive switching properties of the SZO-based ERBE device are investigated in this chapter. The experimental results reported in this dissertation indicate that the electrode materials significantly affect the resistive switching properties. The device with Al/SZO/LNO/Pt (ERBE) structure shows the nonpolar resistive switching property, while the Al/SZO/LNO (ERE) device depicts the bipolar resistive switching behavior. The resistance ratios between two resistance states are 10^7 and 10^4 for the ERBE and ERE devices, respectively, which is due to the distinct LRS resistance between two devices. The device with Pt BE has lower resistive switching voltages and higher resistance ratio, while the device with LNO BE possesses higher resistive switching voltages and lower resistance ratio. Such different characteristics are attributed to a high resistance of LNO BE in comparison with a low resistance of Pt BE. The switching speed of the SZO-based ERBE device is 10ns, which is the fastest speed in comparison with that of the previous reports. The conduction mechanisms of LRS and

HRS currents of the device are Ohmic conduction and F-P emission, respectively. This device has stable resistive switching properties even when the measurement is performed at 150°C. The nondestructive readout property of the device is demonstrated, and the retention time of the device longer than 10^{7}s is also performed in this chapter. Therefore, the SZO-based ERBE device possessing good switching properties is a promising candidate for next-generation NVM applications.

Table 4-1 Roughness of the LNO and 0.3%-V:SZO films deposited on two kinds of substrates.

Structure	mean roughness (nm)	RMS roughness (nm)
LNO/SiO_2/Si	0.923	1.227
SZO/LNO/SiO_2/Si	0.812	1.037
LNO/Pt/Ti/SiO_2/Si	2.218	2.842
SZO/LNO/Pt/Ti/SiO_2/Si	1.458	2.035

Table 4-2 Device structures, resistive switching polarities, and switching voltages of the SZO-, TiO_2-, and PCMO-based memory devices proposed by well-known research groups.

material	**device structure***	**switching polarity**	**turn-on**	**turn-off**	**reference**
SZO	Al / SZO / LNO / Pt	nonpolar	sweep ±7V pulse ±6V, 10ns	sweep ±2V pulse ±4V, 10ns	this work
SZO	Au / SZO / SRO	bipolar	sweep -0.5V	sweep +0.5V	[18]
SZO	Pt / SZO / SRO	bipolar	sweep +2V	sweep -1.5V	[30]
TiO_2	Pt / TiO_2 / Ru	nonpolar	sweep ±2V	sweep ±1V	[49]
TiO_2	Pt / TiO_2 / TiN	bipolar	pulse -2V, 20ns	pulse +2.2V, 30ns	[65]
PCMO	Ti / PCMO / SRO	bipolar	sweep -5V	sweep +2V	[80]
PCMO	Pt / PCMO / Pt	nonpolar	pulse ±3V, 10μs	pulse ±5V, 100μs	[97]

* TE / resistive layer / BE

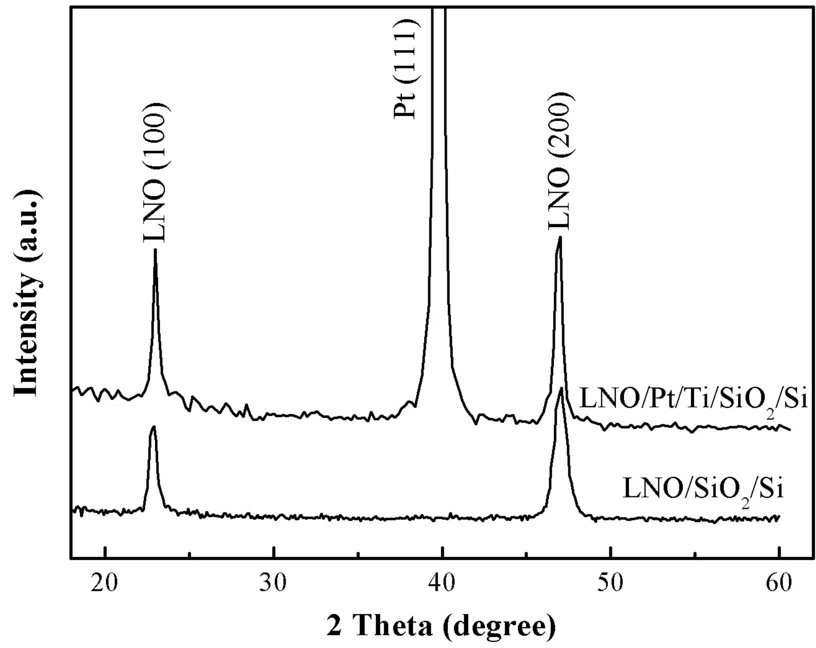


Fig. 4-1 XRD patterns of the 600°C-annealed LNO films deposited on the SiO_2/Si and Pt/Ti/SiO_2/Si substrates.

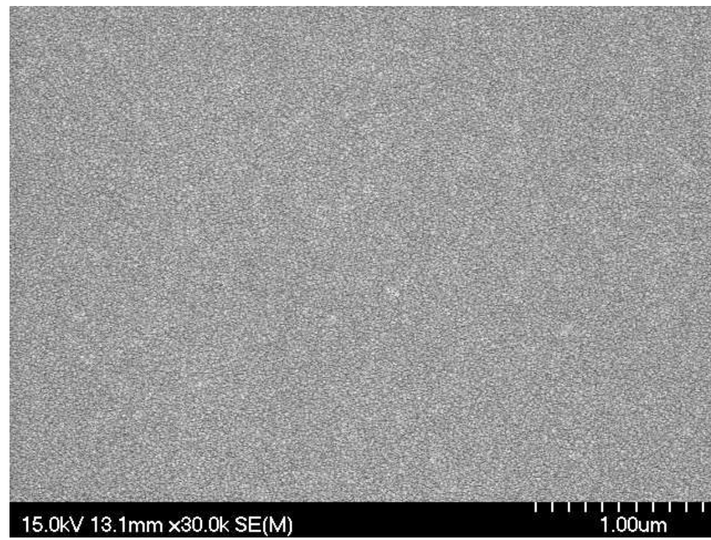


Fig. 4-2 Surface SEM image of the 600°C-annealed LNO film deposited on the $Pt/Ti/SiO_2/Si$ substrate.

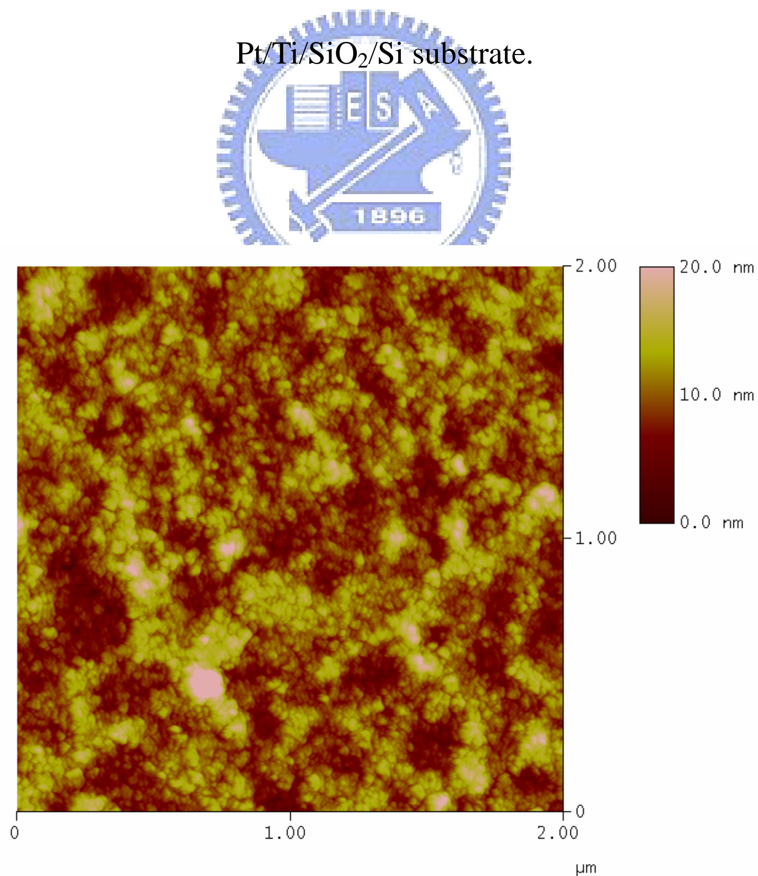


Fig. 4-3 Surface AFM image of the 600°C-annealed LNO film deposited on the $Pt/Ti/SiO_2/Si$ substrate.

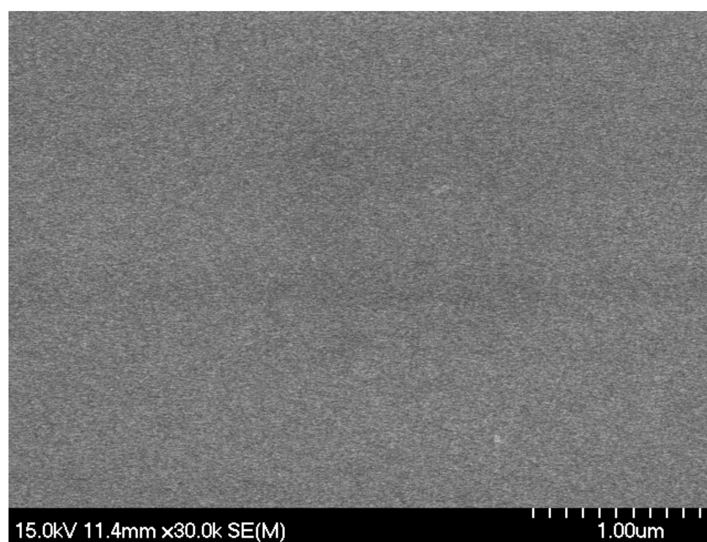


Fig. 4-4 Surface SEM image of the 0.3%-V:SZO film deposited on the LNO/Pt/Ti/SiO_2/Si substrate.

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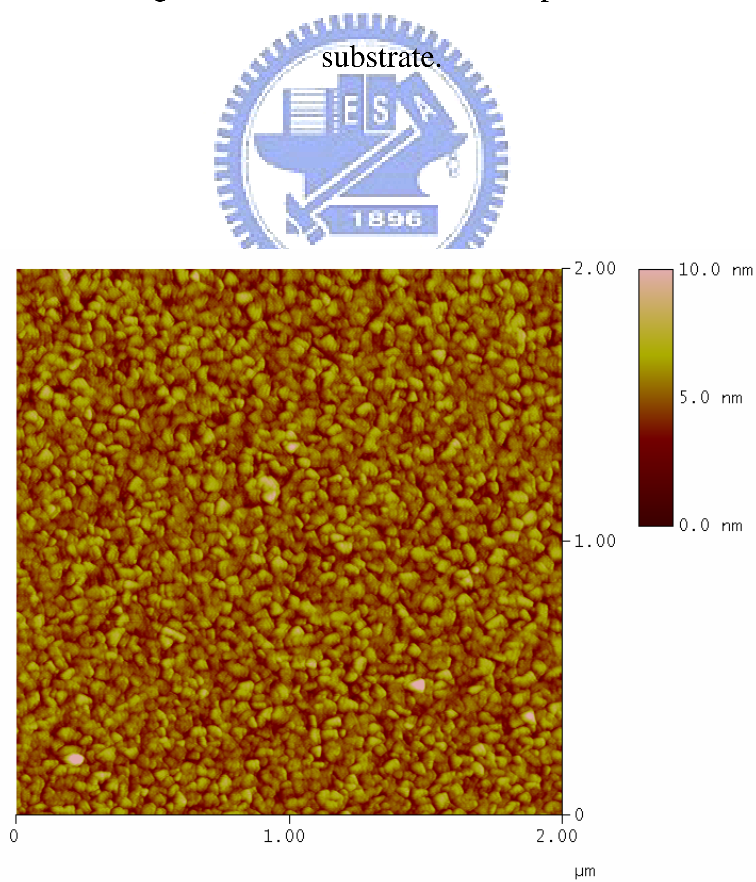


Fig. 4-5 Surface AFM image of the 0.3%-V:SZO film deposited on the LNO/Pt/Ti/SiO_2/Si substrate.

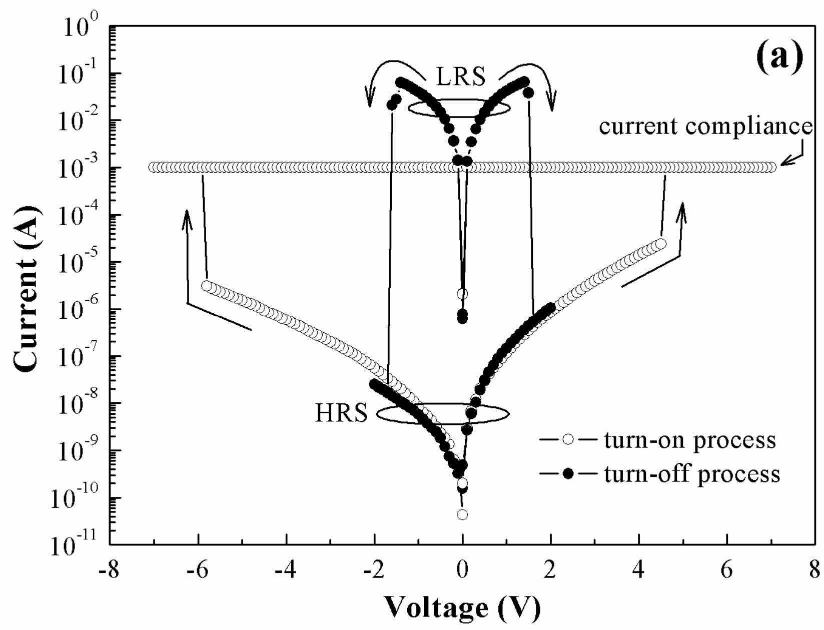
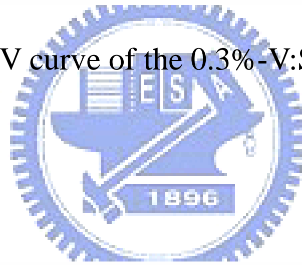


Fig. 4-6(a) I-V curve of the 0.3%-V:SZO ERBE device.



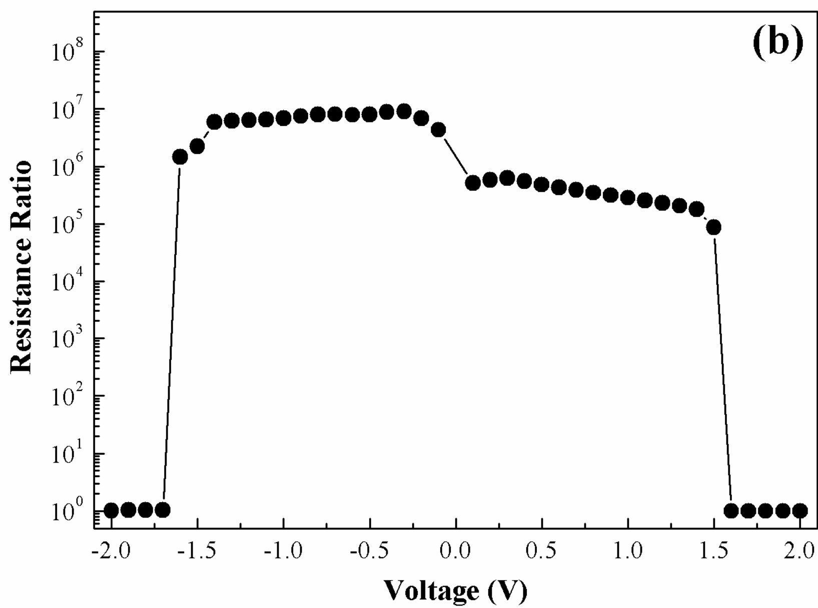


Fig. 4-6(b) Resistance ratio of the 0.3%-V:SZO ERBE device.

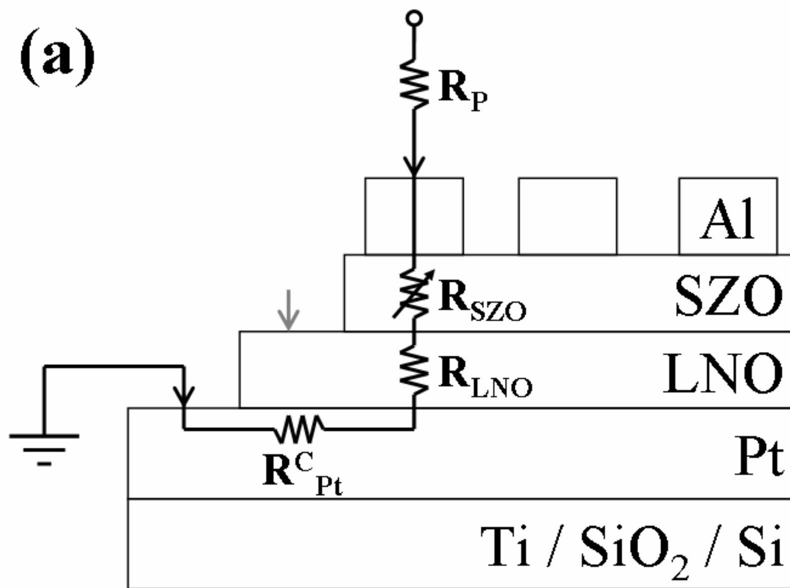


Fig. 4-7(a) Equivalent circuit of the 0.3%-V:SZO ERBE device.

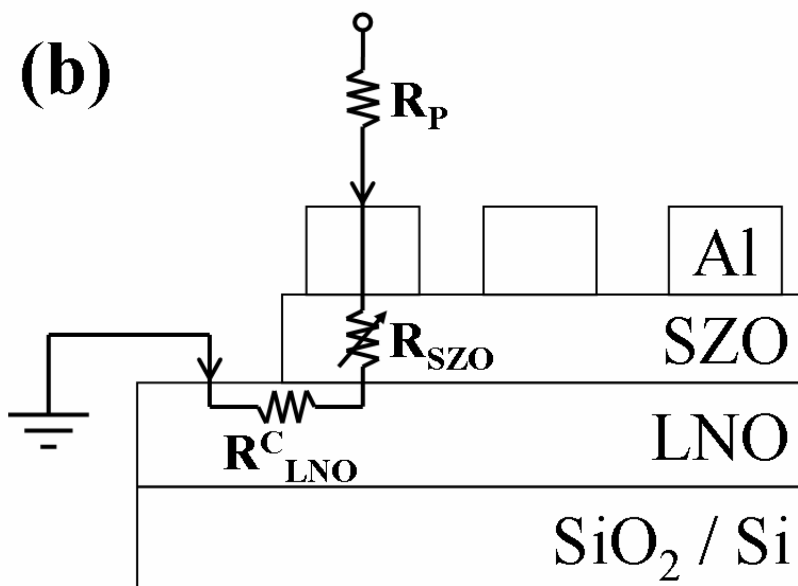


Fig. 4-7(b) Equivalent circuit of the 0.3%-V:SZO ERE device.

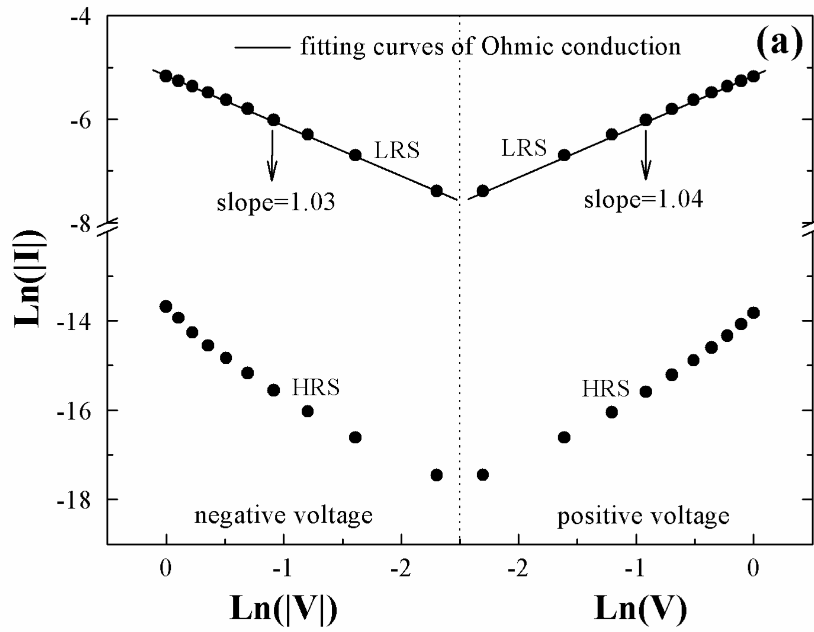


Fig. 4-8(a) Fitting curves of both LRS and HRS currents of the 0.3%-V:SZO ERBE device by Ohmic conduction.

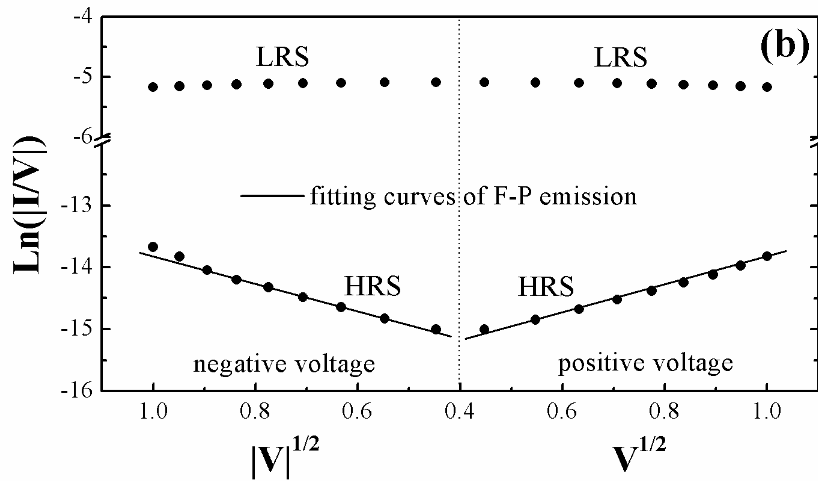


Fig. 4-8(b) Fitting curves of both LRS and HRS currents of the 0.3%-V:SZO ERBE device by F-P emission.

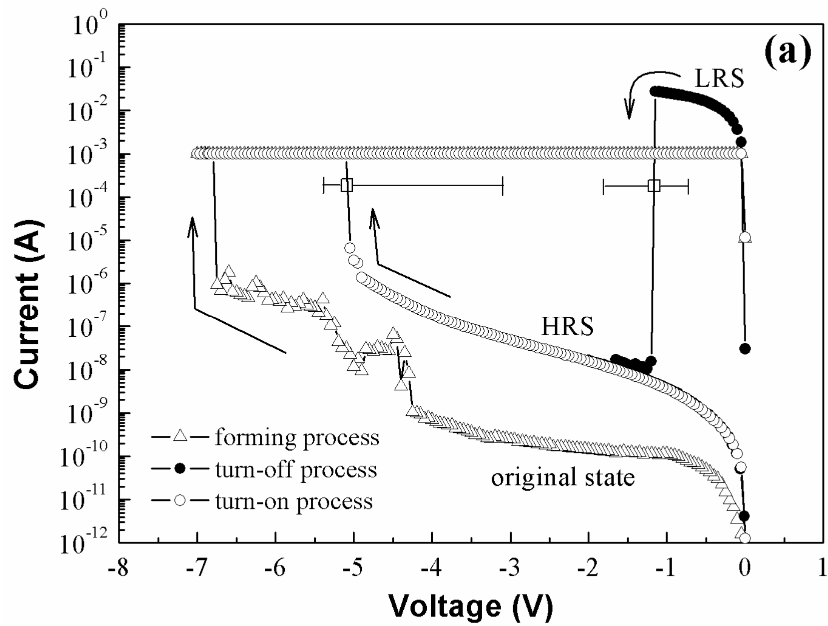


Fig. 4-9(a) Forming, turn-off, and turn-on processes of the 0.3%-V:SZO ERBE device by applying negative sweep voltages.

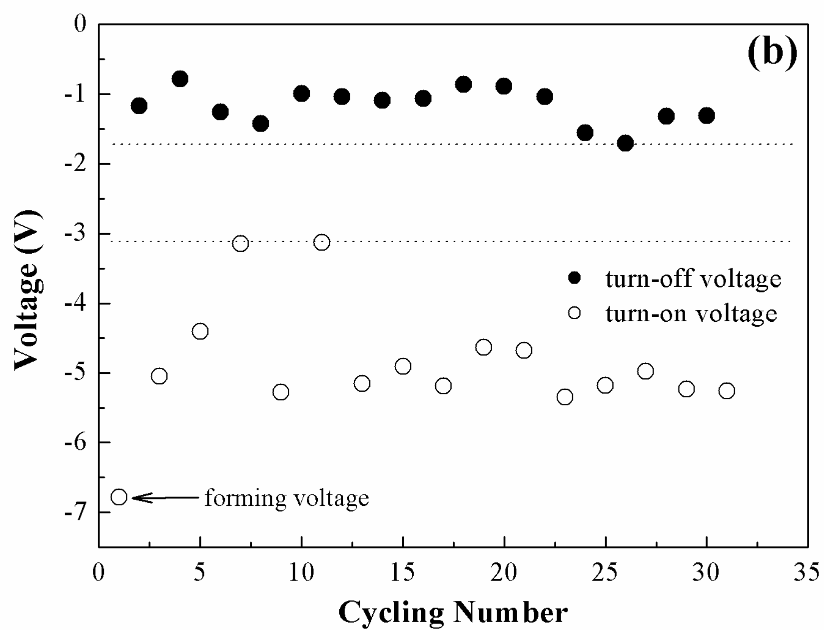
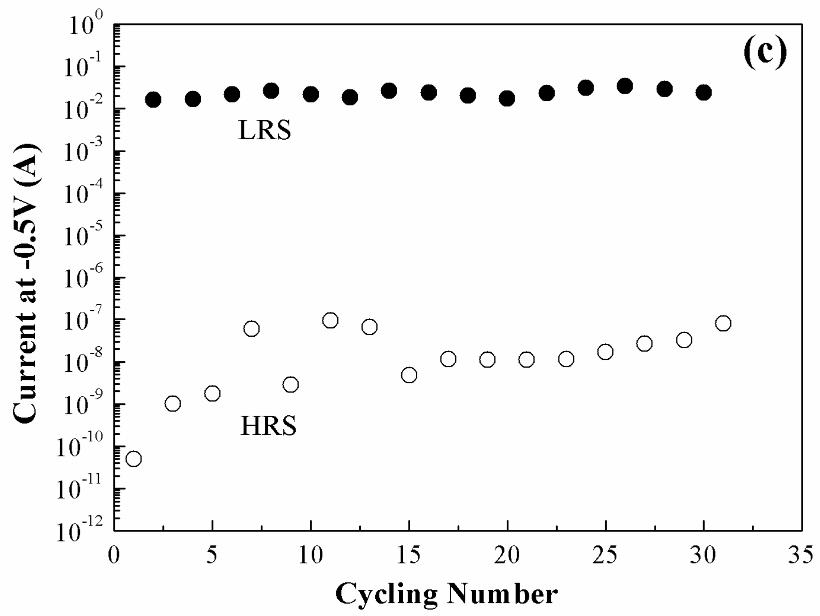


Fig. 4-9(b) Distributions of the turn-on and turn-off voltages of the 0.3%-V:SZO ERBE device.



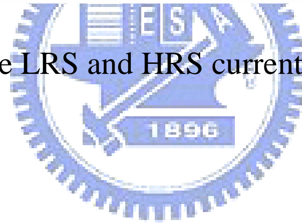


Fig. 4-9(c) Distributions of the LRS and HRS currents of the 0.3%-V:SZO ERBE device.

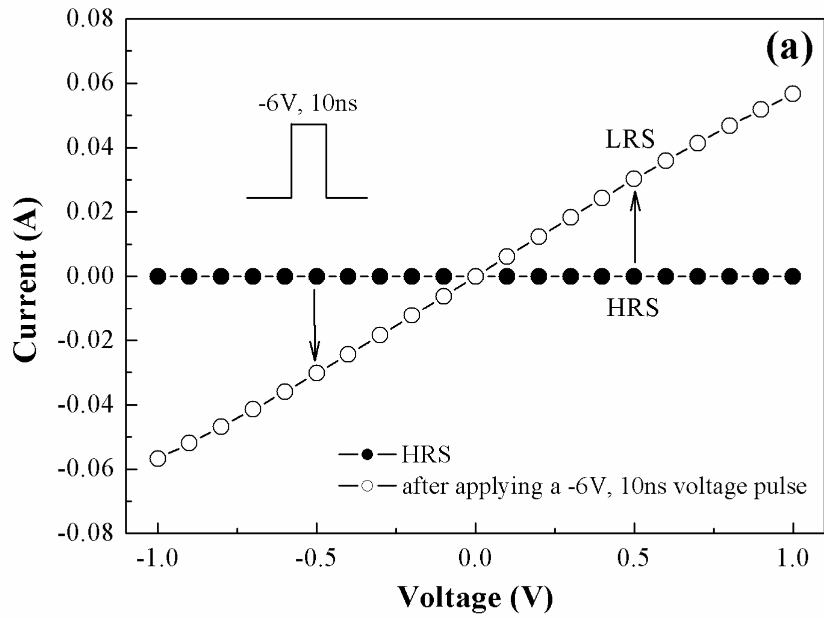


Fig. 4-10(a) Turn-on speed of the 0.3%-V:SZO ERBE device.

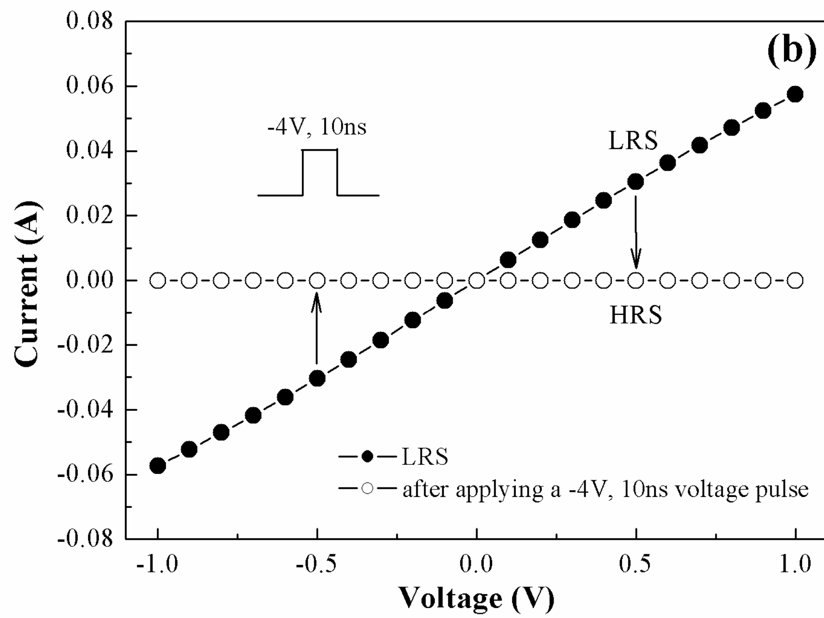


Fig. 4-10(b) Turn-off speed of the 0.3%-V:SZO ERBE device.

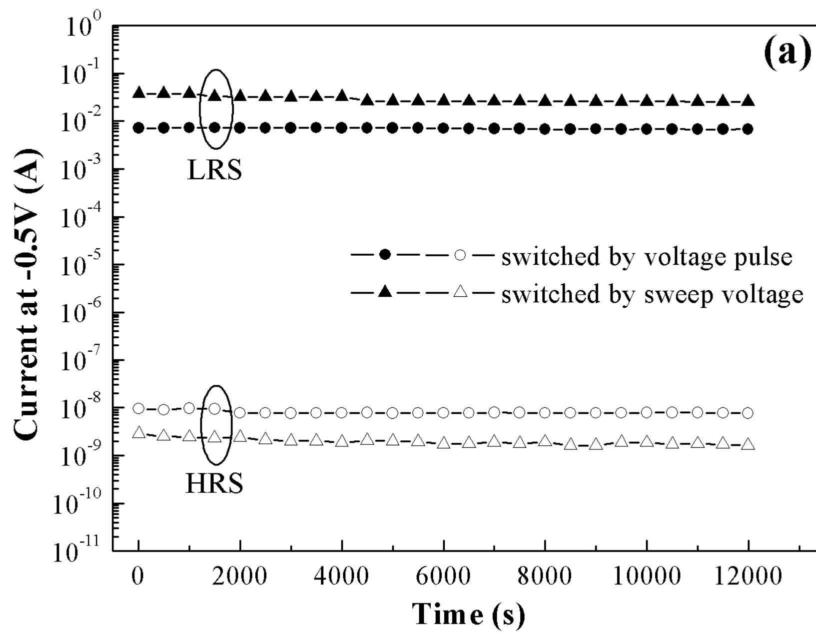
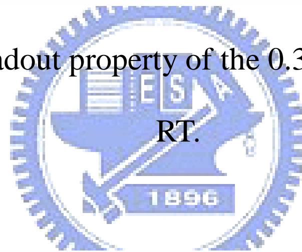


Fig. 4-11(a) Nondestructive readout property of the 0.3%-V:SZO ERBE device measured at RT.



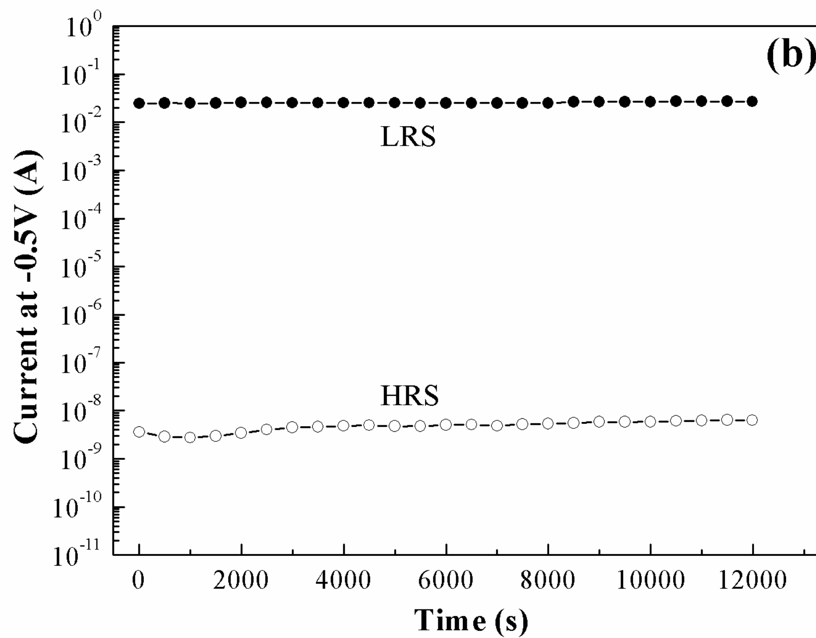


Fig. 4-11(b) Nondestructive readout property of the 0.3%-V:SZO ERBE device switched by voltage pulses measured at 85°C.

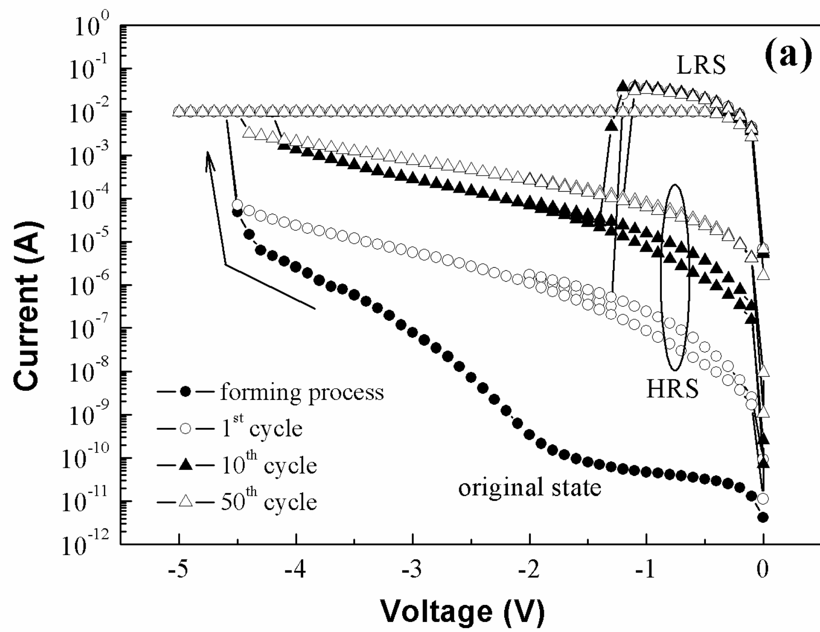


Fig. 4-12(a) Forming process, and 1st, 10th, and 50th voltage sweeping cycles of the 0.3%-V:SZO ERBE device measured at 150°C.

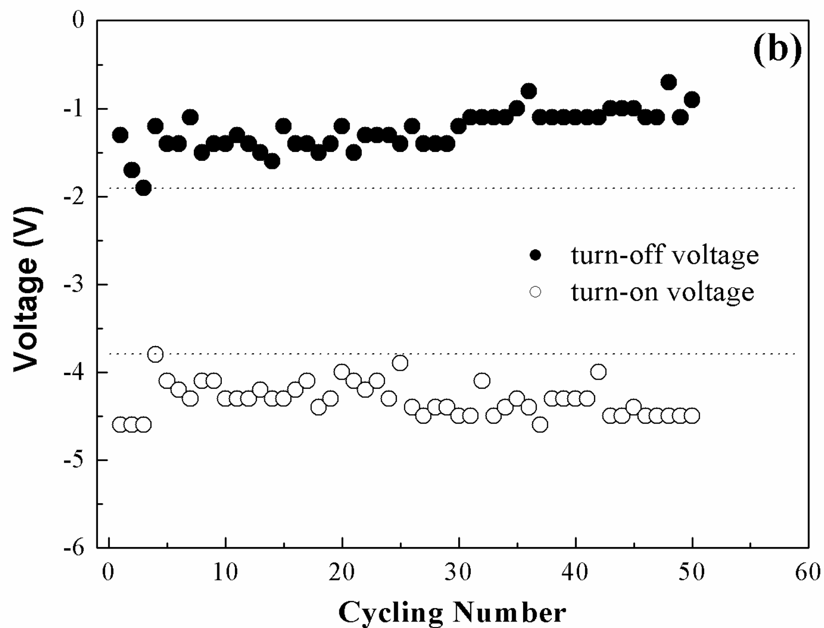


Fig. 4-12(b) Distributions of the turn-on and turn-off voltages of the 0.3%-V:SZO ERBE device measured at 150°C.

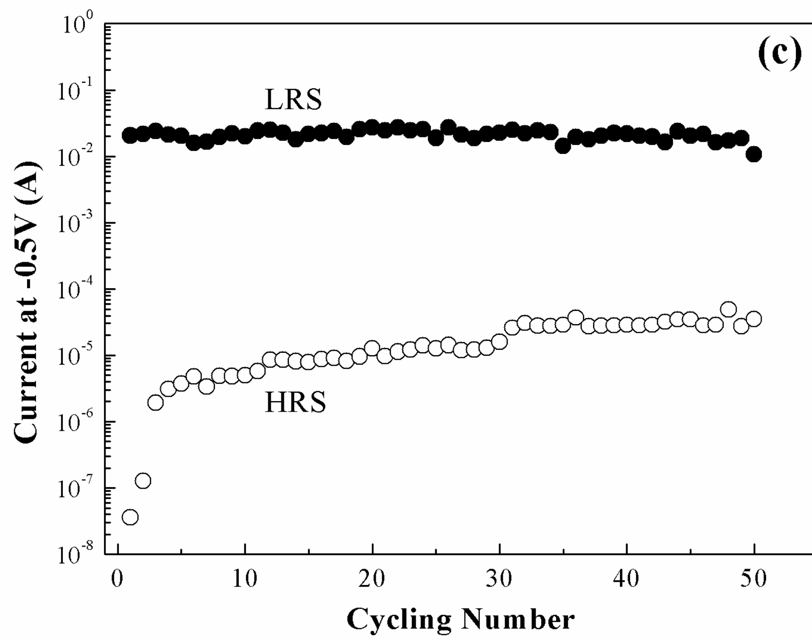


Fig. 4-12(c) Distributions of the LRS and HRS currents of the 0.3%-V:SZO ERBE device measured at 150°C.

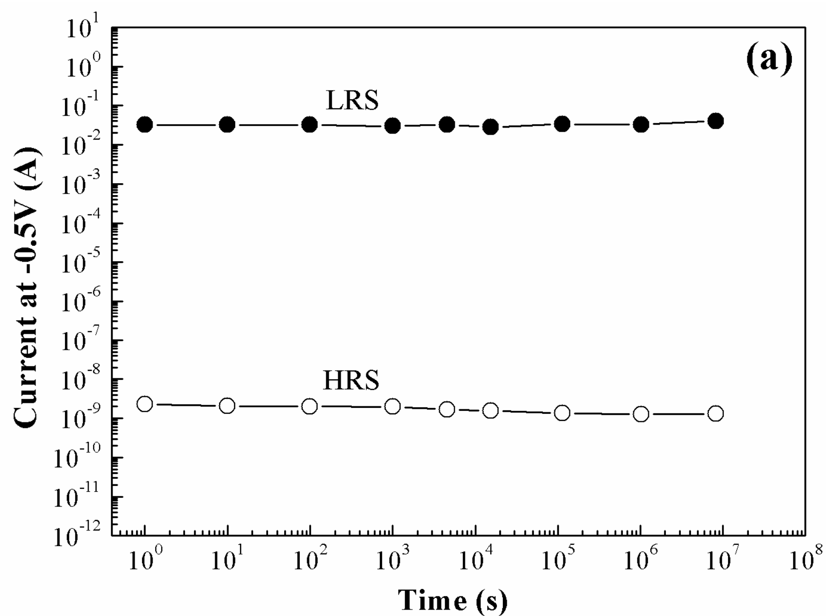


Fig. 4-13(a) Retention time of the 0.3%-V:SZO ERBE device measured at RT.

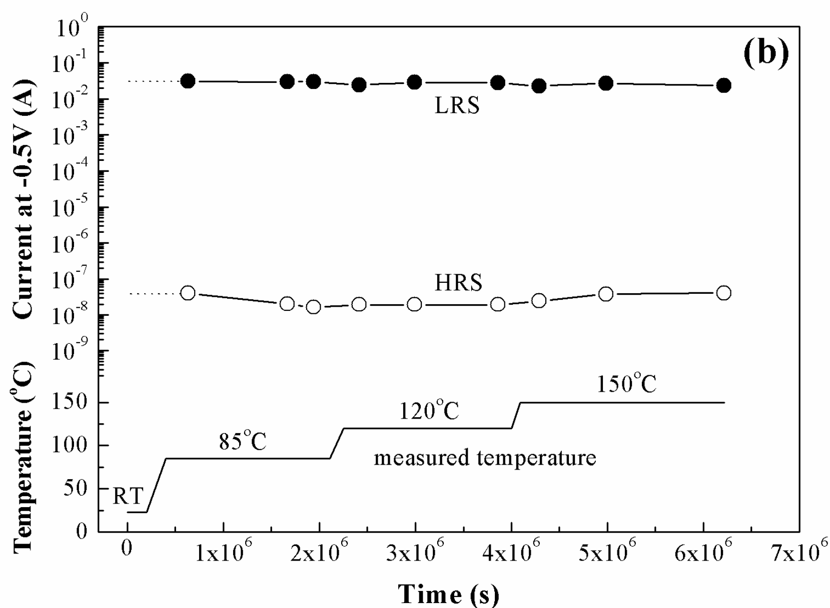


Fig. 4-13(b) Retention time of the 0.3%-V:SZO ERBE device measured at high temperature.

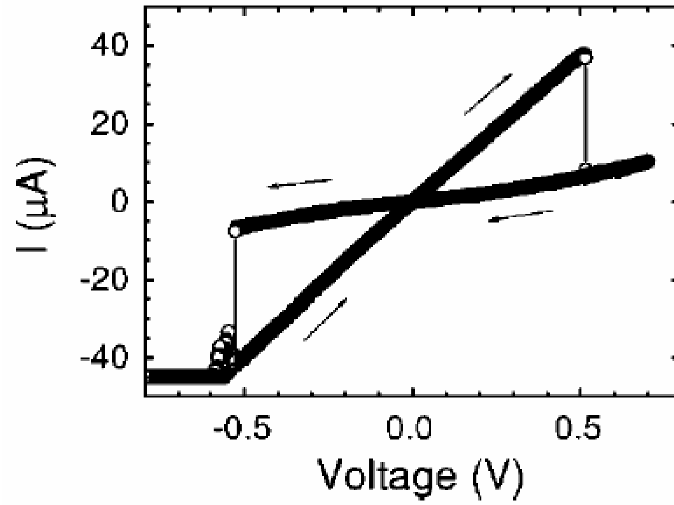


Fig. 4-14(a) Bipolar resistive switching behavior of the Au/SZO/SRO device [18].

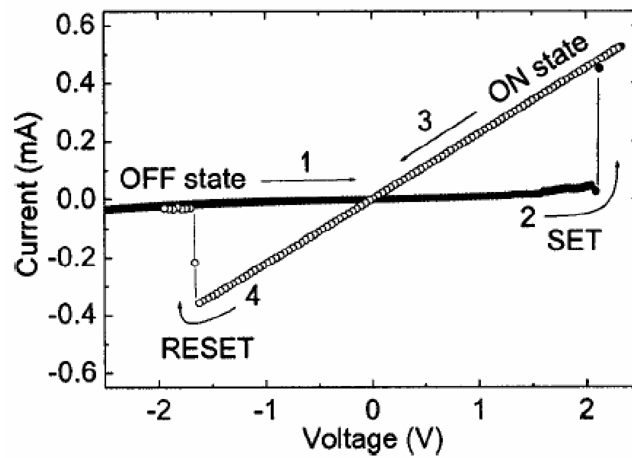


Fig. 4-14(b) Bipolar resistive switching behavior of the Pt/SZO/SRO device [30].

Chapter 5

Conclusions

5.1 Conclusions

The resistive switching properties of the SZO-based memory devices for RRAM applications are investigated in this dissertation. The SZO-based memory devices with LNO BE and Al TE (Al/SZO/LNO, ERE devices) have bipolar resistive switching characteristics, whereas the devices with Pt BE, LNO buffer layer, and Al TE (Al/SZO/LNO/Pt, ERBE devices) possess the nonpolar resistive switching behavior. The similar characteristics in resistive switching polarities of the TiO_2- and PCMO-based memory devices were also proposed by other research groups. The nonpolar switching is considered as an intrinsic property of the SZO-based memory devices, while the electrode materials employed in the devices would determined the resistive switching polarities.

The resistive switching mechanism of the SZO-based memory devices are considered as the formation and disruption of the current paths, which possibly attributed to the storage and release of electrons of the trap states in the SZO film. The conduction mechanisms of both LRS and HRS currents of the SZO-based memory devices are dominated by Ohmic conduction and F-P emission, respectively.

The 600°C-annealed LNO films act as the BE and buffer layer of the ERE and ERBE devices, respectively, have smooth surfaces, high conductivities, and (100) and (200) orientations. The SZO films with different doping concentration deposited on the LNO films also have (100) and (200) preferred orientations, which have been proposed that had good resistive switching behavior.

The doping effects of the SZO-based ERE devices are discussed in this dissertation, indicating that a proper concentration of doping into the SZO film can improve the resistive switching properties, such as resistance ratio and stability. The resistance ratio between two resistance states of the 0.3%-V:SZO ERE device is over 10^4, and retains 1000 after applying 100 voltage sweeping cycles. This device has stable resistive switching properties even when the measurement is performed at 100°C. The retention time of the device is longer than 10^7s, and the nondestructive readout property of the device is also examined. The resistive switching properties of the 0.3%-V:SZO ERE device comparison with the criteria of RRAM are shown in Table 5-1.

On the other hand, the operation voltages of the 0.3%-V:SZO ERBE device are less than 7V, and the resistance ratio of the device is higher than 10^7. This device with Pt BE has lower resistive switching voltages and higher resistance ratio comparison with the 0.3%-V:SZO ERE device with LNO BE. The resistive switching speed of the 0.3%-V:SZO ERBE device is 10ns, which is the fastest speed in comparison with that of the previous reports. The device has stable resistive switching properties even when the measurement is performed at 150°C. The nondestructive readout property of the device is also demonstrated, and the retention time of the device is longer than 10^7s. The resistive switching properties of the 0.3%-V:SZO ERBE device comparison with the criteria of RRAM are also shown in Table 5-1.

Consequently, the SZO-based memory device with good resistive switching characteristics including low operation voltage, low power consumption, high operation speed, long retention time, nondestructive readout properties, and simple structure is a possible candidate for next-generation NVM applications.

5.2 Suggestions for Future Work

5.2.1 Resistive Switching Mechanisms

The possible resistive switching mechanism of the SZO-based memory devices is proposed and investigated in this dissertation. However, the resistive switching mechanisms in each material are not clearly understood and unified explained so far. In order to improve the resistive switching properties of the RRAM devices, an extensive understanding of resistive switching mechanisms in each material is necessary.

5.2.2 Possible Ways to Improve the Endurance

The endurance of the SZO-based memory devices is about 100, which does not match the criterion of NVM applications, which is possibly due to the electrical degradation of the device. During the turn-on processes, the current paths are formed disorderedly, and hence, the turn-on voltages are not identical. Therefore, applying a higher voltage is necessary to successfully turn-on the device, which causes the electrical degradation of the device. In order to improve the endurance of the SZO-based memory devices, two ways are possibly practicable. The first one is the using of plug electrode as shown in Fig. 1-17. Baek *et al.* had proposed that the using of plug BE can confine the area and number of the formation of current paths [16], which can significantly improve the uniformity and stability of the resistive switching properties. Fig. 5-1 shows the turn-off current distribution of the plug BE versus that of the planar BE [16], indicating that the uniformity of the plug BE is higher than that of the planar BE. The second way is the using of series diode (1D1R structure). Besides the avoiding of the misread as indicated in Sec. 1.3.1, the 1D1R structure also can provide a stable current compliance for protecting of the device [67]. In addition, the 1D1R structure can also control the LRS current of the

SZO-based ERBE device within the criterion of RRAM. Therefore, the use of plug BE and 1D1R structure could possibly improve the stability and endurance of the SZO-based memory device, which should be an interesting work.

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Table 5-1 Resistive switching properties of the 0.3%-V:SZO ERE and ERBE devices comparison with the criteria of RRAM.

	criteria of RRAM	ERE device	ERBE device
switching polarity		bipolar	nonpolar
operation voltage	10V	15V	5V
operation speed	1ms / 10ns *[1]	5ns / 500μs *[3]	10ns
current density	10^5~10^7 A/cm^2	10^6 A/cm^2 (estimated)	10^8 A/cm^2 (estimated)
resistance ratio	100	10^4	10^7
endurance	10^6 / 10^{12} *[2]	100	100
retention time	10 years	16 months (so far)	8 months (so far)
nondestructive readout	10^{12}	10^{12} (estimated)	10^{12} (estimated)
thermal stability		> 100°C	> 150°C

*[1] 1ms for replacing the Flash memory, and 10ns for replacing the DRAM.

*[2] 10^6 for replacing the Flash memory, and 10^{12} for replacing the DRAM.

*[3] 5ns for turn-on process, and 500μs for turn-off process [23].

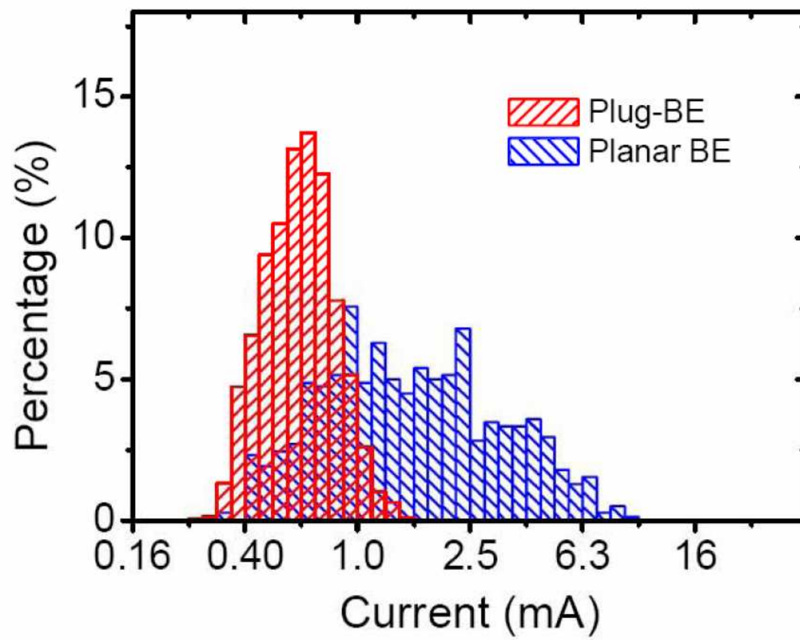

Fig. 5-1 Turn-off current distribution of the plug BE versus that of the planar BE [16].

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