國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

具有氮化矽覆蓋之形變通道金氧半場效電晶體特性與相關可靠性問題研究

A Study on Characteristics and Reliability Issues of Strained Channel MOSFETs with SiN Capping

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中華民國九十七年十一月

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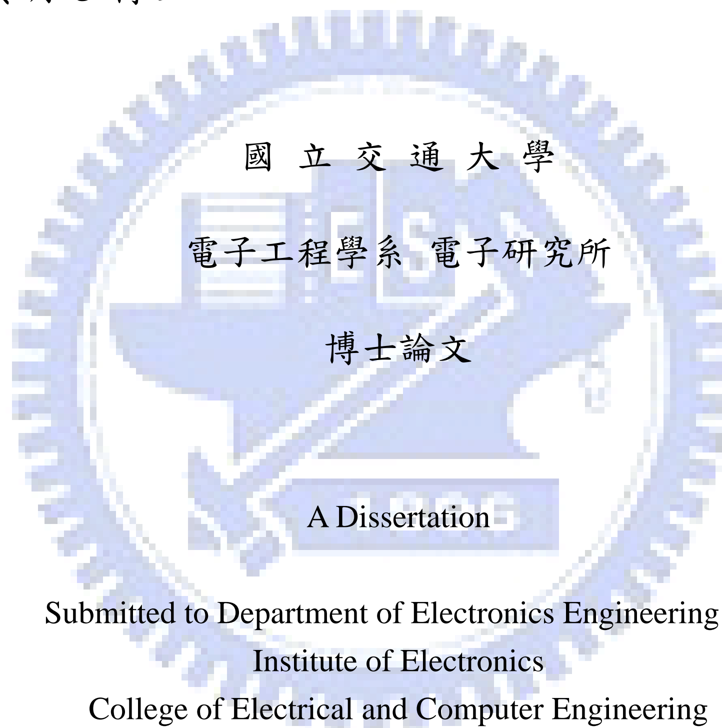

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電子工程學系 電子研究所

博士論文

A Dissertation

Submitted to Department of Electronics Engineering &
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering
November 2008
Hsinchu, Taiwan, Republic of China

中華民國九十七年十一月

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摘　要

在本論文中，我們針對氮化矽覆蓋層對元件特性與相關可靠性影響作一系列之研究，主要涵蓋內容包括具有薄緩衝層(buffer layer)之氮化矽覆蓋 n 型與 p 型通道金氧半場效電晶體之製作與特性分析；利用改變前趨物氣體流量與沉積溫度，來最佳化氮化矽薄膜；以及對具有氮化矽覆蓋之元件作漏電流機制分析與閃爍雜訊(flicker noise)之探討。此外，我們也對氮化矽覆蓋造成的能階窄化效應(bandgap narrowing effect)與熱載子測試(hot-carrier stress)後之界面缺陷橫向分佈及負偏壓溫度不穩定性(NBTI)之交流可靠性分析做詳細的探討。

我們發現，雖然氮化矽覆蓋能有效提升載子遷移率及驅動電流，但卻犧牲熱載子與負偏壓溫度不穩定之可靠性，其主要原因歸咎於沉積氮化矽的過程，使用含氫元素的反應氣體，如氨氣(NH_3)、矽甲烷(SiH_4)，使得大量的氫元素擴散進入通道區域，因而造成熱載子與負偏壓溫度不穩定性之劣化。為了消弭這項缺失，我們提出，利用在閘極與氮化矽覆蓋層間加入一層薄緩衝層來抑制氫的擴散，結果證實，熱載子與負偏壓溫度不穩定之可靠性均獲得顯著改善，而且不會犧牲因氮化矽覆蓋造成之元件電流提升。

因為氮化矽覆蓋層中的氫是劣化元件可靠性之主因，因此，接下來我們藉由

改變前趨物氣體流量與沉積溫度，直接調整氮化矽薄膜的組成。從 X 光光電子能譜術(XPS)與傅立葉轉換紅外光譜儀(FTIR)及應力量測系統之分析結果，我們發現，增加氮氣流量會增加氮化矽薄膜之伸張應力與氮含量，這是有助於 n 型通道元件之載子遷移率提升，此外，增加氮氣流量與沉積溫度會消減氮化矽中的矽氫鍵結，因此，可提升熱載子或負偏壓溫度不穩定之可靠性。

接下來，雖然伸張應力能提升 n 型金氧半場效電晶體之特性，但卻造成元件關閉時漏電流增加。結果顯示，閘極引發汲極漏電(gate-induced drain leakage)為此漏電流增加之主要原因。伸張應力造成之能階窄化將增強能帶與能帶間的穿遂(band-to-band tunneling)，因此導致閘極引發汲極漏電增加。這也說明了為何伸張應力會增加元件之漏電流。

最後，我們探討氮化矽覆蓋元件對閃爍雜訊之影響。雖然在沉積氮化矽過程中增加氮氣流量能提升 n 型通道金氧半場效電晶體之特性與可靠性，但氮化矽中氫含量之減少將降低界面處缺陷與懸浮鍵(dangling bond)之修補，因為此缺陷為造成閃爍雜訊之主因，故導致閃爍雜訊劣化。

關鍵字: 氮化矽覆蓋，緩衝層，氫擴散，氣體流量，閘極引發汲極漏電，負偏壓溫度不穩定性，熱載子測試，閃爍雜訊

A Study on Characteristics and Reliability Issues of Strained Channel MOSFETs with SiN Capping

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Abstract

In this thesis, we have investigated the impacts of SiN capping layer on the device performance and the related reliability issues. This study includes the fabrication and characterization of SiN-capped n- and p-channel MOSFETs with a thin buffer layer over the gate, the optimization of SiN film by varying precursor gas flow rate and deposition temperature, and investigation of off-state leakage current mechanism and flicker noise characteristics on the SiN-capped devices. In addition, bandgap narrowing effect induced by SiN capping, lateral distribution of interface state after hot-carrier stress, and AC NBTI stress are also investigated.

We found that although the SiN capping can dramatically enhance the carrier mobility and thus the drive current, the robustness to hot-carrier and negative bias temperature instability (NBTI) degradation is compromised as well, owing to the large amount of hydrogen contained in the SiN layer by using the hydrogen-containing precursors, i.e., NH_3 and SiH_4, which may diffuse into the channel region during the SiN deposition process. To eliminate this shortcoming, the insertion of a thin buffer layer between the gate and the SiN capping layer was proposed to suppress the diffusion of hydrogen, and the result demonstrates that the hot-carrier and NBTI reliability of the SiN-capped devices can be restored without compromising the current enhancement by

the SiN capping.

Since abundant hydrogen species contained in the SiN capping layer are the primary culprit for aggravated reliability, we have directly adjusted the composition of SiN film by varying precursor gas flow rate and deposition temperature. From the analysis of X-ray photoelectron spectroscopy (XPS), Fourier transform infrared spectrometer (FTIR), and stress measurement system, we found that increasing N_2 flow rate will increase tensile stress and nitrogen content in the SiN film, which is beneficial for mobility enhancement of n-channel devices. In addition, increase in N_2 flow rate and deposition temperature tend to weaken the signal of Si-H bonds, which is helpful for the improvement of hot-carrier and NBTI reliability.

In addition, although tensile stress can boost NMOSFETs' performance, we found that it also results in off-state leakage current increase. Our results indicate that gate-induced drain leakage (GIDL) current is the major reason for increased off-state leakage current. Bandgap narrowing induced by tensile stress will enhance the band-to-band tunneling process, resulting in GIDL current increase, which accounts for off-state leakage current increase by tensile stress.

Finally, we have also investigated the impacts of SiN-capped devices on the flicker noise characteristics. Although NMOSFETs' performance and hot-carrier reliability can be improved by increasing N_2 flow rate in the SiN deposition, the accompanying decrease of hydrogen content reduces the passivation of defects and dangling bonds near the interface, which is considered to be the main culprit for flicker noise, resulting in the degradation of flicker noise.

***Keyword*:** SiN capping, buffer layer, hydrogen diffusion, gas flow rate, gate-induced drain leakage (GIDL), negative bias temperature instability (NBTI), hot-carrier stress, flicker noise

誌　謝

本論文的完成，首先，要特別感謝我的指導教授林鴻志博士與黃調元博士。林老師提供了我很多學習的機會，讓我在求學期間，就曾在台積電與工研院打工，提早跟業界接觸與學習，也提供了我很多實驗上的想法，讓我燃起鬥志重新回學校做實驗，而老師對元件物理的觀念以及研究嚴謹的態度，更讓學生獲益良多，雖然老師常常說自己很嘮叨，但是學生還是非常感激老師的用心與指教；黃老師博學多聞，做事小心謹慎，且待人和藹可親彬彬有禮，不僅學術上的專業，平常處世的方法與態度以及文學上的造詣，都讓學生非常佩服。有幸獲得兩位恩師的教導，學生感激之情，實難以用言語形容。另外要感謝簡昭欣老師與郭治群老師，謝謝你們平日對學生的關心與祝福。

由衷感謝呂嘉裕學長帶我進入無塵室，給予我啟蒙訓練以及實驗上的傳承；感謝李耀仁學長在我徬徨時給予鼓勵並提供建議與幫忙；感謝侯拓宏、歐士傑、吳偉豪、林宏年、俞正明、李達元與陳啟群等學長在台積電的照顧；感謝陳百宏、林哲歆學長在工研院的幫助；感謝葉冠麟、李明賢、盧文泰、李維、賴大偉等學長在實驗上的建議與分享；感謝與我同居的蘇俊榮在研究路上的陪伴；感謝與我一起打拚的黃健銘、陳瀅弘、蔡子儀、詹凱翔等學弟，讓我不再孤軍奮戰，以及先進元件技術實驗室的學弟，張伊鋒、張凱翔、徐行徽、謝雨霖、趙志誠、陳威臣、李冠樟、林哲民、林政頤、郭嘉豪及其他碩班的學弟妹們，在這段期間的陪伴與相互鼓勵學習；也感謝我曾經帶過的專題生，陳宇航與邱筱芸在研究上的幫忙。

另外，衷心的感謝國家奈米元件實驗室，提供良好的設備與環境，並感謝沈士文、謝錦龍、彭馨誼、劉正財、宋金龍、范庭瑋、李春杏、陳琇芝、周家如、徐台鳳、林婉貞、蔣秋芬、趙子綾、魏雅嵐、蕭明娟等人在元件製作上的協助；感謝陳坤明博士與陳柏源先生在高頻實驗室裡的幫忙；以及感謝那些許許多多曾經幫助過我的人。

特別要感謝我的父母，盧振興先生與林月祝女士，感謝你們三十年來的養育之恩，並總是默默的在背後給予我支持與協助；感謝我的妹妹盧佩宜小姐以及所有關心我的親朋好友，在我求學時間的支持與鼓勵；再則更要感謝我女友王品雯小姐，在研究路上有你的關心與陪伴，讓我不再孤單。你們的關心，是我精神的慰藉，也提供了我繼續向前的動力。

最後，謹以此論文獻給我的家人，及所有關心我的朋友。

盧景森
誌于風城交大
2008/11

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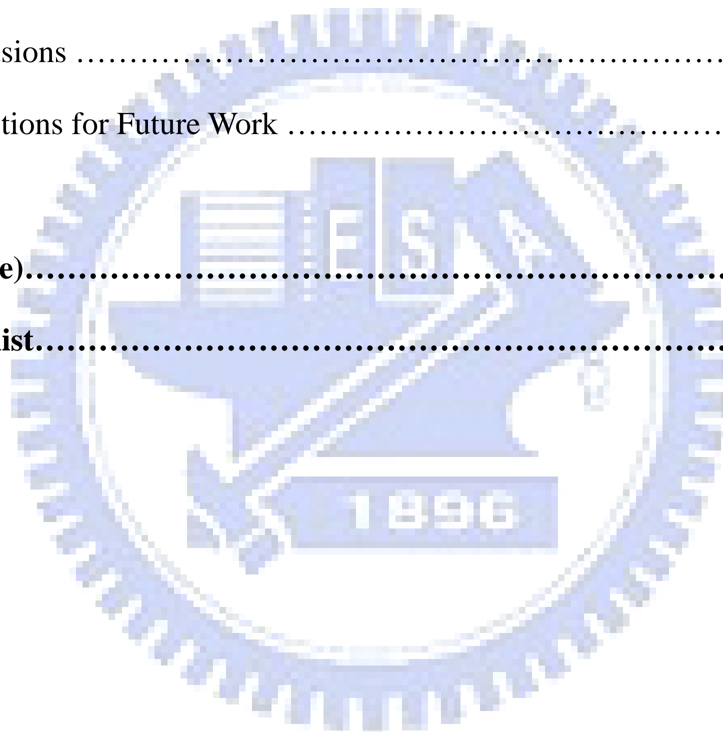

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Chapter 1

Introduction

1.1 General Background

1.1-1 Strained Channel Technology

The origin of strained channel to improve MOS devices can be traced back to thin Si layers grown on relaxed SiGe substrates in the 1980s [1-2]. The thin Si layer takes the larger lattice constant of the SiGe and creates bi-axial tensile stress. Drive current of both NMOSFET and PMOSFET can be enhanced by the bi-axial tensile stress when more than 20% of Ge is incorporated in the relaxed SiGe layer [3]. It is noted that the thickness of the top strained-Si layer must be thinner than a critical thickness that depends on the Ge content of the underlying relaxed SiGe layer to avoid the generation of high amount of dislocations. The yield issue associated with high threading dislocation density (typically > 10^4 cm^{-2}) of the virtual SiGe substrate represents a major obstacle for practical applications. In addition to defect issue, bi-axial strain suffers from other concerns such as high Ge out-diffusion, high wafer cost, and performance loss at high vertical electric field [4]. In the 1990s, another strained channel technology was proposed, i.e., so-called uni-axial strain, which is based on process-induced strain and free from the aforementioned concerns of bi-axial strain.

Uni-axial strain was experimentally and theoretically studied by a large number of researchers in recent years. Various methods of uni-axail strain were proposed such as using SiN contact etch-stop layer [5-8], shallow trench isolation [9-11], source/drain (S/D) silicidation [12], and embedded SiGe [13-14] or SiC [15-16] in the S/D. In addition, depending on the SiN deposition conditions, the SiN layer can generate either tensile or compressive stress [5], enabling the dual-SiN stressor technology for CMOS

manufacturing [17]. Furthermore, the behaviors of carrier mobility under uni-axial strain depend on the strength of the strain and the orientation [17]. Electron and hole mobilities respond to the three-dimensional (3D) mechanical stress in different, even opposite ways. Table 1-I summarizes the impact of 3D strain direction on device performance [18]. Only increasing tensile stress in the in-plane transverse direction of carrier transport (i.e., y-direction) benefits NMOSFET's and PMOSFET's performance simultaneously, while it is a trade-off for stress in the other two directions.

We summarize some major advantages of uni-axial versus bi-axial strain as follows. First, uni-axial stress provides significantly larger hole mobility enhancement at both low strain and high vertical electric field due to the difference in the warping of the valence band under strain [19]. Large mobility enhancement at low strain is important since yield loss via dislocations occurs at high strain. Second, uni-axial stress provides larger current improvement for nano-scale short-channel devices, and it can be enhanced by shortening the channel length [20-21]. Third, it is reported that the threshold voltage shift for devices with uni-axial stress is smaller than that with bi-axial stress [22-23]. Lastly, uni-axial stress is more easily implemented in modern VLSI technology. With these advantages, process-induced uni-axial stress is present in nearly all high performance logic technologies at the 90, 65, and 45 nm technology nodes for both microprocessor and consumer products [24-25].

1.1-2 Mobility Enhancement Physics

The carrier mobility is given by $\mu = \frac{q\tau}{m^*}$, where $1/\tau$ is the scattering rate and m^* is the conductivity effective mass. Strain enhances the mobility by reducing the conductivity effective mass and/or the scattering rate [26]. For electron transports in bulk Si, the conduction band is comprised of six degenerate valleys (Δ6) of the same

energy. Strain removes the degeneracy between the four in-plane valleys (Δ4) and the two out-of-plane valleys (Δ2) by splitting them in energy [27]. Among Δ4 valleys, two are in-plane transverse (y) and two are longitudinal (x) in the direction of carrier transport. The energy difference (ΔE) between Δ2 and Δ4 sub-bands determines the total population of the bands. The mobility enhancement will be reinforced by decreasing inter-valley scattering that results from the splitting of conduction band [28]. In addition, the lower energy of the Δ2 valleys indicates that they are preferentially occupied by electrons. The electron mobility is also improved by reducing in-plane and increasing out-of-plane effective mass due to the favorable mass of the Δ2 valleys [29]. When operating the device in strong inversion, the electrons in the inversion layer will be subjected to a strong quantum confinement [30]. Note that the Δ2 valleys are longitudinal in the direction of quantization (z) and will thus merely react. However, the Δ4 valleys are all transverse in the direction of quantization. Therefore, they will strongly increase their energy and lose their electron to Δ2 valleys [30]. The fraction of transverse electrons will further increase as will the sub-band splitting. Both will contribute to the increase of mobility in the strong inversion regime [23].

For holes, the valence band structure of Si is more complex than the conduction band [23]. Holes occupy the top two bands (i.e., heavy-hole and light-hole bands) for unstrained Si. With the application of strain, the effective mass of hole becomes highly anisotropic due to band warping, and the energy levels become mixtures of the pure heavy-hole, light-hole, and split-off bands. Thus, the light-hole and heavy-hole bands lose their meaning [31]. The light-hole band will lower the energy under the impact of strain. The fraction of light holes will increase, and that of heavy holes will decrease, leading to a lower conductivity mass, and thus a higher mobility [30]. In addition, the sub-band splitting will prevent inter-band passages of holes, and leading to a further

increase in mobility due to decrease in scattering rate. However, for bi-axial tensile strain in the strong inversion, the splitting of sub-bands will be cancelled [25,30]. Because under the effect of quantum confinement, the light-hole band will increase its energy much than the heavy-hole band [23]. Therefore, the initial reparation between the light and heavy holes is then restored in the hole population, and the impact on hole mobility enhancement vanishes [4].

1.1-3 Hot-Carrier Effects

One of the serious reliability problems by continued shrinking of MOSFETs into the submicron regime is the hot-carrier effect [32-34]. Hot electrons produced by the high lateral electric field near the drain in short-channel devices can generate electron-hole pairs via impact ionization, and creates more hot carriers. The resulting hot carriers are injected into the gate oxide via hot-carrier injection (HCI), leading to the creation of interface states [35]. The interface states cause threshold voltage shift and increase subthreshold slope, and degrade the device over time.

One method to determine hot-carrier degradation in n-channel devices is to bias the device at maximum substrate current ($I_{sub,max}$). The generated hot holes enter the substrate and constitute a parasitic substrate current, and thus substrate current can be used to indirectly monitor hot-carrier effect. The substrate current depends on the channel lateral electric field. At low gate voltage (Vg), the lateral electric field increases with increasing gate voltage until Vg = Vd/3 ~ Vd/2 [36]. Substrate current increases to a maximum at that gate voltage. For higher gate voltage, the lateral electric field decreases as does the substrate current. The device is biased at $I_{sub,max}$ for a certain time and the device parameters, such as threshold voltage, saturation current, transconductance, or interface states, are measured. In general, the device lifetime is

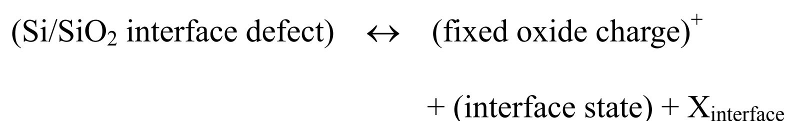
defined as the time when the measured parameter has changed by 10 ~ 20%.

When considering high mobility strained channel devices, it is clear that higher mobility could lead to more energetic electrons. Also, the lower bandgap in the strained-Si could make impact ionization easier [37-39]. These two factors will cause increased hot-carrier injection in the strained channel devices.

1.1-4 Negative Bias Temperature Instability (NBTI)

Negative bias temperature instability (NBTI), known since the late 1960s [40-43], has been recognized as one of the most serious reliability concerns for p-channel MOSFETs, because it can result in the failure of the integrated circuit (IC). Either negative gate voltages or an elevated temperature can produce NBTI, but a stronger and faster effect is produced by their combination. Generally, the NBTI stress is performed at an elevated temperature with oxide electric field typically below 6 MV/cm, and this leads to the degradation of device parameters, such as threshold voltage, drive current, and interface states. The degradation phenomenon of NBTI was first reported by Miura and Matukura [41], and further characterized by researchers at Bell Laboratories [43-44], Fairchild Semiconductor [40], and RCA Laboratories [42]. Despite many research efforts, detailed NBTI degradation mechanism has not yet been fully understood.

NBTI depicts a fractional power-law dependence on time. The value of the exponent is most likely 1/4. From the $t^{1/4}$-like evolution, Jeppson and Svensson first proposed the diffusion-controlled electrochemical reaction model for the NBTI of MOSFETs [45]. Later, this model was refined by Ogawa et al. [46-47]. The reaction can be expressed as follows,



$$(\text{Si/SiO}_2 \text{ interface defect}) \leftrightarrow (\text{fixed oxide charge})^+ + (\text{interface state}) + X_{interface}$$

$$+ e^- \text{ (to the silicon)} \tag{1-1}$$

and
$$X_{interface} \leftrightarrow X_{bulk} \tag{1-2}$$

where X denotes the diffusion species, which is thought to be the dissociated hydrogen species (either H^0 or H^+) or water-related species [45,48-49]. The initial Si/SiO_2 interface defect is comprised of hydrogen-terminated trivalent Si bonds (Si-H), and interface state is supposed to be a silicon dangling bond denoted as Si・ which results when H is removed from Si-H. When the Si/SiO_2 interface defect is electrically activated, the diffusion species leaves a defect site at Si/SiO_2 interface where an interface state and a positive fixed oxide charge are generated. This model agrees with the observation that equal numbers of interface states and fixed oxide charges are produced [50]. The Si-H bonds have been proposed as the origin for both fixed oxide charge and interface state generation under NBTI stress.

As proven by Jeppson and Svensson [45], the behavior of the interface state generation suggests that the generation process is diffusion-controlled. N_{it} buildup equals the total number of released H species. Hole-assisted reaction breaks interfacial Si-H bonds, resulting in N_{it} generation:

$$\Delta N_{it} = S_N (D_x t)^n \tag{1-3}$$

where D_x is the diffusion coefficient of X in the oxide, time exponent value depends on the type of H species trapped and released in the oxide bulk [51].

1.1-5 Flicker Noise Characteristics

Flicker noise in MOSFETs has been extensively studies in the past [52-62]. It is commonly known as 1/f noise since the noise spectral density is inversely proportional to frequency. In the early days of flicker noise research in MOS devices, two major theories have been raised to explain its physical origins.

In the carrier number fluctuation theory, originally proposed by McWhorter [52-53], the flicker noise is attributed to the random trapping and detrapping processes of charges in the oxide traps near the Si/SiO_2 interface [54-55]. Using this theory, the input-referred noise will be independent of the gate bias voltage, and the magnitude of the noise spectra is proportional to the density of the interface trap density. The slope η of the $1/f^{\eta}$ noise spectra is usually chosen to be 1 if the trap density is assumed to be uniform in the gate oxide [56]. Based on this theory, input-referred gate voltage noise spectral density (S_{Vg}) can be given by

$$S_{Vg} = \frac{S_{Id}}{g_m^2} = \frac{kTq^2}{\gamma C_{ox}^2} \frac{N_{ot}}{WL} \frac{1}{f} \quad (1\text{-}3)$$

where S_{Id} is drain current noise spectral density; g_m is transconductane; C_{ox} is the oxide capacitance per unit area; γ is the McWhorter tunneling parameter; N_{ot} is the oxide trap density per unit volume and unit energy; W and L are channel width and length, respectively.

The mobility fluctuation theory, on the other hand, considers flicker noise as a result of fluctuation in bulk mobility. This theory is based on Hooge's empirical relation for the spectral density of flicker noise in a homogeneous sample [57]. Adapting Hooge's model to a typical MOS device, S_{Vg} in strong inversion is given by [58]

$$S_{Vg} = \frac{q\alpha(Vg - V_{th})}{C_{ox}WLf} \quad (1\text{-}4)$$

where α is the Coulomb scattering coefficient. This model suggests a linear dependence of S_{Vg} with the gate voltage in strong inversion.

Some authors have combined both the carrier number fluctuation and the mobility fluctuation models to explain a broader set of data [59-60]. However, they have combined the two theories in an uncorrelated manner, whereas in fact both fluctuations arise from the same mechanism. Based on the new information obtained from the study

of random telegraph signal in small area MOSFETs, a unified flicker noise model was proposed by K. K. Hung [61-62], which incorporates both the carrier number fluctuation and the mobility fluctuation mechanisms in a correlated manner. The S_{Vg} can be written as

$$S_{Vg} = \frac{kTq^2 N_{ot}}{\gamma f W L C_{ox}^2}(1 + \alpha \mu_0 C_{ox}(Vg - V_{th}))^2 \qquad (1\text{-}5)$$

This equation depicts that S_{Vg} will show a quadratic increase with the gate voltage.

1.2 Motivation

Channel strain engineering has been pursued aggressively for mobility enhancement in nano-scale MOS devices, especially by using uni-axial strain technology, which can be free from the concerns related to bi-axial strain arising from the use of SiGe virtual substrate, such as substrate defects, high Ge out-diffusion, self-heating, and high wafer cost. Generally, uni-axial strain can be engineered by applying the strain boosters, such as SiN stress liner, embedded SiGe or SiC in the S/D region, shallow trench isolation, and S/D silicidation. Among these approaches, SiN capping technique has received much attention because it is easily implemented in modern VLSI technology. In addition, depending on the SiN deposition conditions, the SiN layer can generate either tensile or compressive stress, enabling the dual-SiN stressor technology for CMOS manufacturing. Therefore, in this thesis, we focus on the fabrication and characterization of strained channel MOS devices with SiN capping layer.

Although the SiN capping can dramatically enhance the carrier mobility and thus the device drive current, the robustness to hot-carrier and NBTI degradation is compromised as well, owing to the large amount of hydrogen contained in the SiN layer

by using the hydrogen-containing precursors, i.e., NH_3 and SiH_4 (or SiH_2Cl_2), which may diffuse into the channel region during the process. In order to eliminate this shortcoming, in Chapters 2 & 5, the insertion of a thin buffer layer between the gate and the SiN capping layer is proposed to suppress the diffusion of hydrogen species into the channel region, and the result demonstrates that the hot-carrier and NBTI reliabilities can be restored without compromising current enhancement due to the SiN capping. In addition, in Chapter 3, another useful approach is also explored to directly adjust the composition of SiN film by varying precursor gas flow rate and deposition temperature. We successfully develop the SiN film with high tensile stress but low hydrogen content, which is beneficial for NMOSFETs' performance and hot-carrier reliability.

After investigating the device performance enhancement and related reliability issues, we found that increasing tensile stress will result in off-state leakage increase. Therefore, we are devoted to investigate the impact of stress induced by SiN capping on the leakage current in Chapter 4. In addition, flicker noise is very important for low frequency analog circuits and rf applications; however, very few literatures have paid attention to its study on the strained channel device. Therefore, the impacts of SiN-capped NMOSFETs on the flicker noise characteristics are investigated in Chapter 6.

1.3 Thesis Organization

This dissertation is divided into seven chapters.

In Chapter 1, the backgrounds and motivations of the thesis are reviewed.

In Chapter 2, a novel scheme involving the insertion of a thin buffer layer between the gate and the SiN layer is proposed and demonstrated to restore the hot-carrier reliability of the SiN-capped devices without compromising the current enhancement

due to the SiN capping. Bandgap narrowing effect induced by SiN capping and the lateral distribution of interface state after hot-carrier stress are also investigated.

In Chapter 3, the strained n- and p-channel MOSFETs with different types of SiN film by varying the N_2 flow rate and deposition temperature during the deposition step are fabricated and characterized. X-ray photoelectron spectroscopy (XPS), Fourier transform infrared spectrometer (FTIR), and film stress measurement system are applied to analyze the properties of the SiN films. We found that tensile stress increases with increasing N_2 flow rate, therefore boosting the NMOSFETs' performance. In addition, the increase in N_2 flow rate and deposition temperature tends to weaken the signal of Si-H bonds. Finally, the immunity for devices to hot-carrier degradation and NBTI reliability is mainly affected by the hydrogen content, rather than the stress level.

In Chapter 4, we have fabricated strained-channel NMOSFETs with different tensile stress by adjusting SiN thickness. The impacts of stress induced by SiN capping on the leakage current are investigated. Gate-induced drain leakage (GIDL) current is identified to be responsible for increased off-state leakage current.

In Chapter 5, SiN-capped PMOSFETs with a thin HfO_2 buffer layer were fabricated and characterized. HfO_2 buffer layer is helpful to mitigate the degradation of NBTI. In addition, AC NBTI stress of devices is further studied. The aggravated NBTI degradation in the SiN-capped devices can be alleviated by high frequency operation, while HfO_2-buffered sample still depicts less degradation than SiN-capped sample.

In Chapter 6, the impacts of devices with SiN capping layer on the flicker noise characteristics are investigated. Both carrier number fluctuation theory and mobility fluctuation theory are utilized to model the flicker noise. We found that hydrogen species contained in the SiN film play an important role in the flicker noise characteristics.

In Chapter 7, we conclude with summaries of the experimental results. Recommendations for future research are also given.

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Table 1-I Impacts of 3D strain direction on device performance. X represents the longitudinal direction of carrier transport, Y represents the in-plane transverse direction of carrier transport, and Z represents the direction of out-of-plane. [18]

Strain Direction	Increasing Tensile Stress	
	NMOSFET	PMOSFET
X	Improve	Degrade
Y	Improve	Improve
Z	Degrade	Improve

Chapter 2

Impacts of Buffer Layer on the Performance and Reliability of Strained Channel NMOSFETs with SiN Capping

2.1 Introduction

Channel-strain engineering has emerged as one of the most effective remedies for boosting the drive current in the scaled devices [1-11]. This could be accomplished by either applying high biaxial tensile strain to the channel region with a SiGe virtual substrate [1-2], or by uniaxially straining the channel with strain boosters, such as stress liner [3-4], embedded SiC in the source/drain (S/D) [5-6], and shallow trench isolation [7]. The approach of using SiGe virtual substrate, however, suffers from a number of drawbacks such as Ge up-diffusion and high defect density. In contrast, the approach of uniaxially straining the channel is essentially free from the aforementioned drawbacks. Capping a tensile-strain SiN layer over the gate of NMOSFETs as contact etch-stop layer (CESL) has been shown to enhance drive current by improving channel mobility [8-11]. Such scheme is attractive and practical because it can be easily implemented using integrated circuit processing.

Nevertheless, with the demonstrated performance improvement, attentions should now be paid to the associated reliability issues for practical applications. Currently, device degradation caused by hot-carriers represents one of the most critical reliability issues in deep sub-micron NMOSFETs [12-14]. Although the physical mechanisms and characteristics of hot-carrier degradation have been extensively examined [15-18], there seems to be very few works investigating the impact of SiN capping and the associated deposition process on hot-carrier reliabilities of strained devices. Furthermore, the effect

of capping a buffer layer prior to the SiN layer has not been reported in literature. In this thesis, we have investigated this issue and demonstrated that the incorporation of a thin TEOS or poly-Si buffer layer over the gate could improve the device reliability without compromising the performance enhancement by the SiN capping. In addition, the barrier height at the Si/oxide interface for strained channel devices and lateral distribution of interface state after hot-carrier stress were also investigated.

2.2 Devices Fabrication

The NMOSFETs were fabricated on 6-inch p-type (100) Si wafers with conventional local oxidation of silicon (LOCOS) isolation. Gate oxide with a thickness of 3 nm was grown in vertical furnace in O_2 at 800˚C. After gate oxide growth, 150 nm poly-Si layer was deposited by a low-pressure chemical vapor deposition (LPCVD) system to serve as the gate electrode. After As^+ implantation (at 20 KeV and 5×10^{15} cm^{-2}), 40 nm TEOS was deposited to serve as as hard mask. An I-line stepper was used to define the gate. Afterwards, standard procedures were applied to form TEOS spacer and S/D junction. Dopant activation was performed at 900˚C for 30 sec.

Afterwards, most wafers were capped with a 300nm-thick SiN layer (denoted as the SiN-capped split). While for some other wafers, a thin LPCVD TEOS or undoped poly-Si buffer layer, with a thickness of either 10 nm or 20 nm, were capped prior to the SiN deposition (denoted as the BL-10nmTEOS, BL-20nmTEOS, BL-10nmPOLY, and BL-20nmPOLY splits, respectively). The SiN deposition was performed at 780˚C with SiH_2Cl_2 and NH_3 as the reaction precursors using LPCVD system. To simulate the effect of deposition temperature during the SiN deposition, the control devices (i.e., without SiN capping) received a placebo treatment (i.e., the same temperature and treatment time as that used in the SiN deposition) in the N_2 ambient.

In some of the SiN-capped wafers, the SiN layer was deliberately removed after deposition in order to evaluate the impact of SiN deposition process itself on the device performance (denoted as the SiN-removal split). Wafers were then combined to receive a 200 nm-thick TEOS as the topmost passivation layer, followed by contact holes and metallization processes. Finally, the processing steps were completed with a forming gas anneal at 400˚C. The cross-sectional TEM pictures for SiN-capped, control, BL-10nmTEOS, BL-20nmTEOS, BL-10nmPOLY, and BL-20nmPOLY samples were shown in Fig. 2.1(a) ~ Fig. 2.1(f), respectively. Electrical characterizations were performed using an Agilent 4156 system. The interface traps were evaluated using the charge pumping method with a fixed amplitude of 1.5V at 1MHz.

2.3 Results and Discussion

2.3-1 Effects of Channel Strain on Device Performance

The stress induced by LPCVD SiN layer with and without TEOS or poly-Si buffer layer was first examined by a Tencor FLX-2320 stress measurement system. This system evaluates the stress by measuring the changes in curvature of the silicon substrate before and after deposition of a blanket SiN film with or without buffer layer. We confirmed that the stresses are tensile in nature with a magnitude of around 300 MPa for all samples, irrespective of the presence of TEOS or poly-Si, indicating that the incorporation of either 10 nm-thick or 20 nm-thick buffer layer does not jeopardize the stress induced by SiN capping.

Next, the electrical characteristics were performed using an Agilent 4156 system. Figure 2.2 shows the subthreshold characteristics and transconductance of NMOSFETs for all splits (i.e., control, SiN-capped, BL-10nmTEOS, BL-20nmTEOS, BL-10nmPOLY, BL-20nmPOLY, and SiN-removal) with channel length of 0.4 μm. It

can be seen that all splits exhibit similar subthreshold slope, confined in a narrow range between 74 ~ 75 mV/decade, as shown in Fig. 2.3. Nevertheless, two categories of transconductance are clearly distinguished among the samples: SiN-capped and all buffer-layer splits depict significant increase with respective to the control, while such an enhancement disappears in the SiN-removal sample. Two important implications are obtained from the results: (1). The performance enhancement is indeed related the channel strain induced by the SiN capping layer. (2). Insertion of the 10 nm-thick or 20 nm-thick TEOS or poly-Si buffer layer between the SiN and the gate does not sacrifice such performance enhancement. To validate these findings, output characteristics of NMOSFETs are shown and compared in Fig. 2.4. Still, drive current enhancement over the control sample is clearly observed for the SiN-capped and all buffer-layer splits, while SiN-removal samples show negligible enhancement.

It should be noted that such performance improvement is related to the device dimensions, a unique feature associated with the uniaxial channel strain [19-20]. To illustrate this point, Figure 2.5 shows the percentage increase of the transconductance for the SiN-capped, all buffer-layer splits, and SiN-removal samples with respect to the controls, as a function of channel length. Each datum point represents the mean measurement result performed on six devices in this figure. We can see that the transconductance enhancement reaches about 33% at a channel length of 0.4 μm in SiN-capped and all buffer-layer samples. When the SiN capping layer is removed, such enhancement becomes negligible. These observations demonstrate that the transconductance is truly due to the uniaxial tensile strain induced by the SiN capping which increases with decreasing channel length and the induced tensile strain is not released by such buffer layer. The capacitance-voltage *(C-V*) characteristics of the samples are shown in Fig. 2.6. Basically the *C-V* curves coincided altogether, indicating

that the above observations are not caused by the thickness difference among gate oxides. In addition, the physical thickness of gate oxide was also evidenced from the TEM pictures in Fig. 2.1(a) ~ Fig. 2.1(f).

2.3-2 Oxide Thickness and Barrier Height Extracted by Fowler-Nordheim Current

Several techniques have been adopted to extract gate oxide thickness, such as the above-mentioned TEM image that can directly extract the physical oxide thickness or *C-V* measurement method to extract electrical oxide thickness. In this section, by fitting the Fowler-Nordheim (F-N) tunneling current model to the measured data, not only the physical gate oxide thickness but also the barrier height (Φ_B) at the Si/oxide interface could be determined. F-N tunneling current is the flow of electrons through a triangular potential barrier. The energy band diagram is illustrated in Fig. 2.7. F-N current density J_{FN} is given by the expression [21-22]:

$$J_{FN} = AE_{ox}^2 \exp(-B/E_{ox}) \tag{2.1}$$

where E_{ox} is the electrical field across the oxide, which is equal to the ratio of oxide voltage over gate oxide thickness (V_{ox}/T_{ox}), where V_{ox} is given by

$$V_{ox} = V_G - V_{fb} - \phi_s - V_p \cong V_G - V_p \tag{2.2}$$

where V_{fb} is the flat band voltage, ϕ_s is the Si surface potential, and V_p is the voltage drop due to poly-depletion. A and B are the constants given by the following relationships:

$$A = \frac{q^3}{8\pi h}\left(\frac{1}{\Phi_B m^*}\right), \tag{2.3}$$

$$B = \frac{8\pi}{3qh}\sqrt{2m^*\Phi_B^3} \tag{2.4}$$

where h is the Plank constant, and Φ_B is the barrier height at the interface in eV. The m*

is the average effective mass in the bandgap of SiO_2 relative to the free electron mass. Generally, A and B are equal to 9.92×10^{-7} A/V^2 and 2.635×10^{8} A/cm, respectively [23].

As an example, Figure 2.8 shows the plot of J_G versus V_G for the control sample. By fitting the F-N current curve, the extracted oxide thickness is about 2.919 nm. This result is close to that of TEM picture, as shown in Fig. 2.1(a). In addition, it should be noted that both A and B are function of barrier height. The plot of $\ln(J_{FN}/E_{ox}^2)$ versus $1/E_{ox}$, known as the F-N plot, is shown in Fig. 2.9. The intercept of the linear F-N plot gives A, while the slope yields B. Using the value of the slope, the extracted barrier height for the control samples is about 3.03 eV.

Figure 2.10 shows the J_G versue V_G for all splits. The extracted oxide thicknesses are about 2.919 nm, 2.933 nm, 2.932 nm, 2.935 nm, 2.933 nm, 2.934 nm, and 2.919 nm for control, SiN-capped, BL-10nmTEOS, BL-20nmTEOS, BL-10nmPOLY, BL-20nmPOLY, and SiN-removal splits, respectively. It can be seen that all SiN-capping samples with or without the buffer layer show slightly increase in the gate oxide thickness, and exhibit similar and lower gate leakage current than the control, while SiN-removal samples show comparable curve with the control. The extracted barrier height versus gate oxide thickness for all splits is shown in Fig. 2.11. We can see that the barrier heights for all SiN capping samples are larger than the control. We believe that the increase of barrier height is due to the tensile strain by SiN capping which induces bandgap narrowing lower of the conduction band [11,24-26]. Therefore, once the SiN capping was removed, the increase in barrier height disappears, as shown in SiN-removal split. The increase value in barrier height is estimated to be about 100 meV by 300 nm-thick LPCVD SiN capping. The lowering of Si conduction band also accounts for the decrease of gate leakage current for all SiN-capping samples. In addition, the bandgap narrowing phenomenon can also be evidenced from the

worsening of the threshold voltage roll-off, as shown in Fig 2.13, which will be discussed in the next section.

As we know, the barrier height between the conduction band of Si and SiO_2 for conventional non-strained devices is about 3.1 eV. This result is inconsistent with that of the above-mentioned control samples. We believe the shorter F-N current region for the extraction of the barrier height due to thinner gate oxide is the main cause. Figure 2.12 shows the extracted barrier height for thicker gate oxide with thickness in the neighborhood of 4.3 nm. We can see that the barrier height for conventional non-strained samples is close to 3.1 eV, while the SiN-capping samples still exhibit a barrier height increase of about 100 meV. We therefore confirm that the 300 nm-thick LPCVD SiN capping in this work causes about 100 meV increase in the barrier height.

2.3-3 Short Channel Effects

Threshold voltage (V_{th}) roll-off characteristics for all splits are shown in Fig. 2.13. These results are obtained at V_{DS} = 0.05 V from the mean of six devices. From the figure, control samples depict reverse short channel effect (RSCE). This is probably due to boron segregation at the implant-damaged regions located near the edge of the channel [27]. However, this phenomenon is not observed on all SiN-capping splits, with or without the buffer layer. Instead, these splits exhibit similar and significant threshold voltage roll-off trend. It is believed that bandgap narrowing effect is the culprit for the aggravated threshold voltage roll-off in the strained devices. From the above-mentioned results, we know that the tensile strain generated form the SiN capping would result in the lowering of Si conduction band. This band offset shifts the Fermi level closer to the conduction band which, in turn, induces more electrons in the inversion layer under the same gate bias. Therefore, the devices with SiN capping lower the threshold voltage and

lead to aggravated threshold voltage roll-off. In addition, for SiN-removal splits, when the SiN is removed (i.e., channel strain is eliminated), the pronounced threshold voltage roll-off behavior would be relaxed and becomes compatible to the control ones.

Drain induced barrier lowering (DIBL) is also examined to evaluate the short channel effect. We use the interpolation method to calculate DIBL effect for all splits. The results are shown in Fig. 2.14. It is clearly seen that there is no distinguishable difference among all splits. This indicates that the use of SiN capping and TEOS or poly-Si buffer layers would not worsen the DIBL of the devices.

2.3-4 Hot-Carrier Stress

Next we shift our attention to the hot-carrier characterization to see if the use of TEOS or poly-Si buffer layer is helpful in improving the resistance to the degradation. Figure 2.15 shows the substrate current (I_{sub}) versus gate voltage for all splits. It can be seen that the substrate current of all SiN-capping samples, with or without buffer layer, show similar trend and is larger than that of the control counterparts. This result indicates clearly that the channel strain plays an important role in affecting the generation of channel hot electrons and the associated impact ionization process. In addition, a thin TEOS or poly-Si buffer layer of 10 nm and 20 nm seems not to release the stress by the SiN capping, judging from the comparable maximum substrate current ($I_{sub,max}$), and is consistent with the inference deduced from Fig. 2.2. Origins for the increase in substrate current for the strained samples are ascribed to the bandgap narrowing effect induced by the channel strain as well as the increased mobility, both tend to enhance the impact ionization rate [26,28-29], and may potentially worsen the hot-electron degradation in the strained devices. In addition, when the SiN layer is removed, the substrate current becomes comparable to that of the control, especially in

the region near the peak substrate current.

Typical results of hot-electron stressing for all splits of samples are shown in Fig. 2.16(a) ~ Fig. 2.16(g). Channel length and width of the test devices are 0.5 μm and 10μm, respectively. The devices were stressed at V_{DS} = 4.9 V and V_{GS} at the maximum substrate current. The I_D-V_G characteristics at V_{DS} = 0.05 V were measured before and after the 5000 sec hot-carrier stressing to examine the degradation caused by the hot electrons. As can be seen in Fig. 2.16, the degradation is the worst in the SiN-capped sample among all splits, in terms of transconductiance reduction, threshold voltage shift, and subthrehold swing increase. The aggravation is alleviated in the devices with buffer layer and SiN removal, though the resultant degradation is still worse than the control sample.

To observe the evolution of degradation, Fig. 2.17 shows the shift of threshold voltage (ΔV_{th}) as a function of the stress time. As mentioned above, the SiN-capped sample depicts the worst degradation in terms of threshold voltage shift, while the use of buffer layer apparently shows improvement in hot-carrier degradation. It is speculated that the increased mobility and abundant hydrogen contained in the SiN capping are the two primary culprits for the aggravated hot carrier degradations [29-30]. The increased carrier mobility may increase the device substrate current, as evidenced in Fig. 2.15, and lead to higher degradation. On the other hand, the deposited SiN contains a large amount of hydrogen species, owing to the use of H-containing precursors, i.e., SiH_2Cl_2 and NH_3, which may diffuse into the gate oxide and channel region. It is well known that the breaking of Si-H bonds is one of the major origins responsible for the hot-carrier damage [15,30], the voluminous hydrogen species definitely aggravate the reliability. This is evidenced from the figure as the SiN-removal devices depict much severe degradation than the control and all buffer-layer samples,

even though the channel strain has been eliminated by the SiN removal. This phenomenon clearly indicates that, although the channel strain is removed, the SiN deposition process itself may cause the enhanced damage effect in the short channel devices.

Figure 2.18(a) shows several possible pathways for hydrogen diffusion in SiN-capped samples, namely, through the gate electrode (Path A1) or oxide spacer (Path A2) into the gate oxide and channel region, or through the S/D contacts into the Si-substrate and laterally into the channel region (Path A3). The results shown in Fig. 2.17 for SiN-removal samples imply that such diffusion processes occur during the SiN deposition. However, the buffer layer can block the diffusion of hydrogen species into the channel, as shown in Fig. 2.18(b), resulting in less broken Si-H bonds and thus less interface state generated during the stressing as compared with the SiN-capped samples without buffer layer.

The results could be validated form the charge pumping current. The charge pumping currents of fresh devices for all SiN-capping samples, with or without buffer layer, are shown in Fig. 2.19. We can see that the SiN-capped samples exhibit the lowest charge pumping current, while the BL-20nmTEOS samples exhibit the highest. In addition, the curves for BL-10nmPOLY and BL-20nmPOLY samples are similar and slightly higher than that for SiN-capped samples, albeit less than that for TEOS-buffered sample. The results indicate that the TEOS buffer layer, especially for 20 nm TEOS, can effectively block the diffusion of hydrogen during the SiN deposition process into the channel region, while such barrier effect seems to be reduced for the BL-POLY splits. It has been pointed out previously that the poly-Si is a diffusion barrier of the hydrogen [31-32]. But it should be noted that, the precursor gas (SiH_4) for poly-Si deposition is also H-containing. Before the SiN deposition, the abundant hydrogen species may have

spread to the Si/SiO_2 interface to passivate the interface states. As a consequence, since 20 nm TEOS buffer layer has been shown to be more effective in blocking the hydrogen diffusion into the Si/SiO_2 interface, the BL-20nmTEOS split shows the best hot-carrier reliability among all splits, while BL-POLY splits show less improvement due to higher amount of Si-H bonds, as shown in Fig. 2.17.

2.3-5 Lateral Distribution of Interface State

The lateral distribution of interface state after hot-carrier stress for all splits was also evaluated in this work based on the method developed in Ref. 33 and the measurement setup is shown in Fig. 2.20. The experimental procedures of this method are briefly described below:

(1) Measure the Icp-V_h curve on a virgin MOSFET from the drain junction (with the source junction floating), thereby establishing the V_h versus $V_{th}(x)$ relationship near the junction of interest [34].

(2) Re-measure the Icp-V_h curve after hot-carrier injection.

(3) Obtain the hot-carrier-induced interface state distribution, $N_{it}(x)$, from the difference of the Icp-V_h curves before and after hot-carrier stress.

It should be noted that the local V_{th} and V_{fb}, across the MOSFET, are not uniform due to the lateral doping variation as illustrated in Fig. 2.21. In order to detect the interface states, the voltage pulses applied during measurements must undergo alternate accumulation and inversion cycles. Therefore, there should be no Icp as the high-level voltage (V_h) is lower than the minimum V_{th} under the gate. Only after V_h starts to exceed the local V_{th} in the channel will Icp begin to grow. Before V_h reaches the maximum local V_{th} in the channel, only interface states residing near the drain side will contribute to Icp, as the needed electrons cannot yet flow to the drain side from the

source.

We choose the control sample for an example. If we assume that the interface state density is spatially uniform along the channel, which can be written as

$$I_{cp,\max} = q\, f\, N_{it}\, W\, L \tag{2.5}$$

where f is the gate pulse frequency, W is the channel width, and L is the channel length. In Fig. 2.22, the corresponding Icp (V_h) comes from the interface state distributed in the region between the gate edge and the position where its local V_{th} is equals to V_h, i.e.,

$$I_{cp}(V_h) = q\, f\, N_{it}\, W\, x \tag{2.6}$$

where x represents the distance from the gate edge to the position where V_{th} (x) = V_h. Comparing Eq. (2.5) and (2.6), we can derive

$$x = \frac{L I_{cp}(V_h)}{I_{cp,\max}} \tag{2.7}$$

Figure 2.23 shows the local V_{th} versus distance x of the control sample. The local V_{th} decreases sharply as x is smaller than 0.09 µm. We can presume that the drain junction is near x = 0.09 µm.

After subjecting to 100 second of hot-carrier stress (V_G@$Isub_{max}$ and V_{DS} = 4.9 V), the incremental charge pumping current (ΔIcp), as shown in Fig. 2.24, at a given V_h, is proportional to the number of generated interface traps from the gate edge to the point x. ΔIcp can be written as

$$\Delta I_{cp} = q\, f\, W \int_0^x N_{it}(x)\, dx \tag{2.8}$$

Therefore, the N_{it}(x) generated by the hot-carrier stress can be expressed as follows:

$$N_{it}(x) = \frac{d\Delta I_{cp}}{dx}\frac{1}{q\, f\, W} = \frac{d\Delta I_{cp}}{dV_h}\frac{dV_h}{dx}\frac{1}{q\, f\, W} \tag{2.9}$$

The derived lateral profiles of the interface states for all splits of devices could be extracted by Eq. (2.9), and the results are shown in Fig 2.25. From this figure we can

directly calculate the damage region and the amount of interface states generated by the hot-carrier stress. We can see that the major damage region is confined within 0.1 μm near the drain edge in all splits. This is reasonable since the hot-carrier stress belongs to edge effect stress. It is obviously seen that interface state generation sharply increases in SiN-capped samples near the drain region. However, all the buffer-layer samples and the SiN-removal samples show smaller degradation than the SiN-capped split, albeit larger than the control one. These results are consistent with those mentioned above.

In short, buffer-layer samples show alleviated hot-carrier degradation. This is because the buffer layer can block the diffusion of hydrogen species, especially for the BL-20nmTEOS split. In addition, the aggravated hot-carrier stress of the SiN-removal devices is presumably due to the extra hydrogen species that may pile up at the S/D edge during the SiN deposition. This explains why the SiN-removal devices show larger generation of interface state than control devices.

2.3-6 Optimization of Buffer Layer Thickness

From the above discussions, we can see that the 20 nm-thick buffer layer does not compromise the performance enhancement due to the tensile strain by SiN capping and the BL-20nmTEOS split depicts the best hot-carrier reliability. By continuing to increase the thickness of TEOS buffer layer, can we still keep the performance gain while maintaining better immunity in hot-carrier degradation? In this section, another lot of devices with control, SiN-capped, BL-10nmTEOS, BL-30nmTEOS, and BL-50nmTEOS splits was fabricated additionally to evaluate what optimized thickness of TEOS buffer layer is. Figure 2.26 shows the subthreshold characteristics and transconductance of NMOSFETs for these splits. We can see that the SiN-capped split and the BL-10nmTEOS split still depict similar and larger transconductance than the

control sample. The transconductance enhancement starts to diminish for the device with 30 nm-thick buffer layer, and the BL-50nmTEOS split depicts the worst transconductance among the splits with TEOS-buffered layer, albeit still much better than the control sample. These results imply that the tensile strain induced by SiN capping is partially released by the 30 nm-thick buffer layer, and the thicker the buffer layer is, the more the transconductance enhancement diminishes. The threshold voltage shift as a function of stress time for these splits is shown in Fig. 2.27. The devices with W/L = 10/0.5 μm were stressed at V_{DS} = 4.6 V, and V_G at maximum substrate current. The BL-50nmTEOS split depicts the best hot-carrier reliability since thicker buffer layer could more effectively suppress the diffusion of hydrogen during the SiN deposition process. Therefore, the thickness of buffer layer has to be optimized carefully. We suggest that the optimized thickness of TEOS buffer layer should be between 20 nm and 30 nm so that the device performance is not sacrificed while the hot-carrier reliability can also be improved.

2.4 Summary

The effects of LPCVD SiN capping and the associated deposition process on the device performance and hot-carrier degradation were investigated in this work. A novel scheme involving the insertion of a buffer layer between the SiN and the gate for improving the device reliability was proposed and demonstrated. We found that the 20 nm-thick buffer layer does not compromise the mobility enhancement due to the SiN capping, while the device performance enhancement starts to diminish if the thickness of the buffer layer exceeds 30 nm.

The accompanying bandgap narrowing effect and the increased carrier mobility tend to worsen the hot-carrier reliability. This work confirms that hot-carrier

degradation is adversely affected when the SiN layer is deposited over the gate, even if the SiN layer is removed later and the channel strain is relieved. Abundant hydrogen species incorporated into the channel region during the SiN deposition process, owing to the use of hydrogen-containing precursors, is the primary culprit for aggravated reliability. By blocking the diffusion of hydrogen species, the devices with 20 nm-thick TEOS buffer layer can effectively improve the hot-carrier reliability without degrading the performance enhancement. Optimizations of both the SiN deposition process and the use of the new buffer layer (e.g., high-*k* film) are thus essential to the implementation of the uniaxial strain in NMOS devices.

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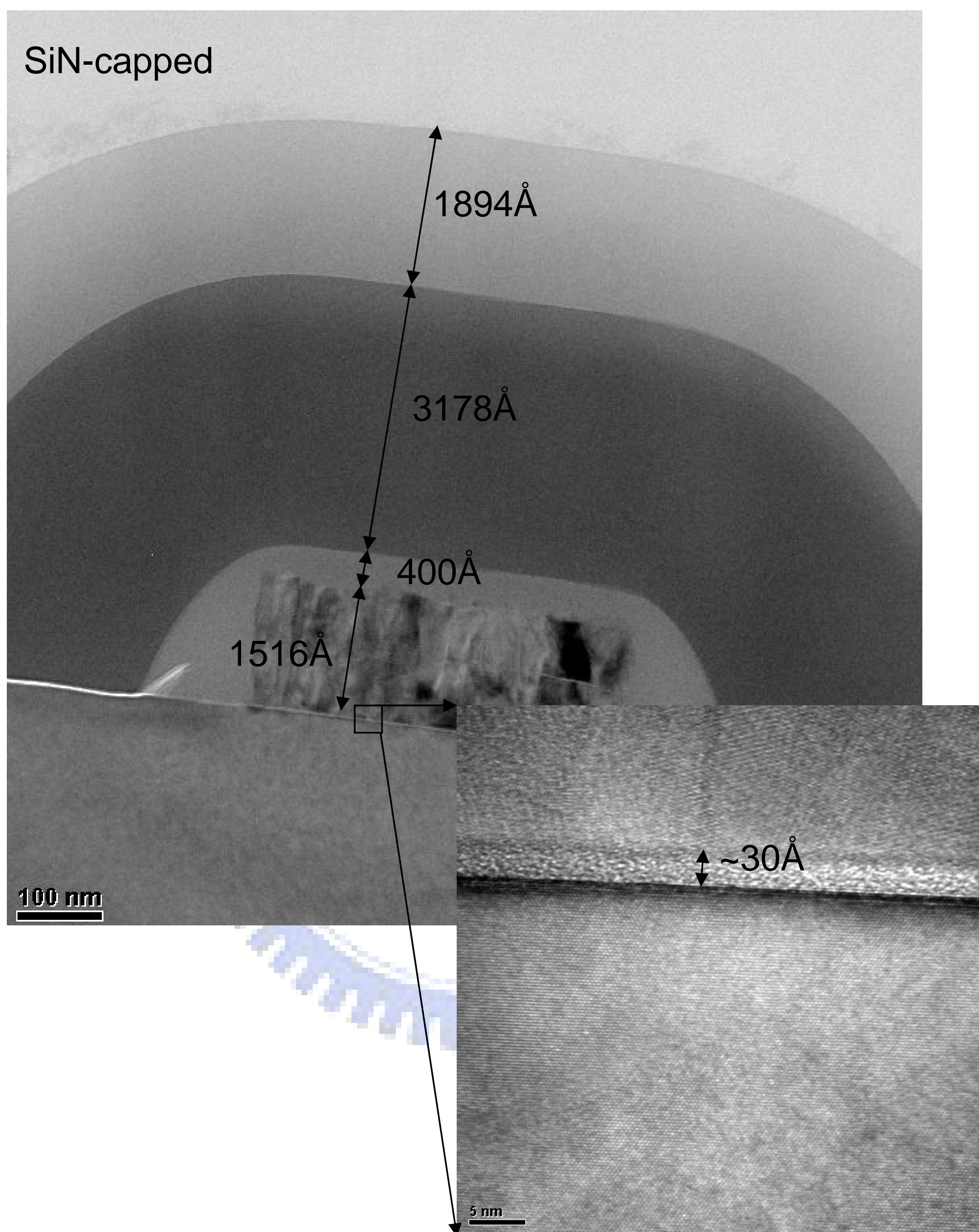

Fig. 2.1(a) Cross-sectional TEM pictures for SiN-capped samples.

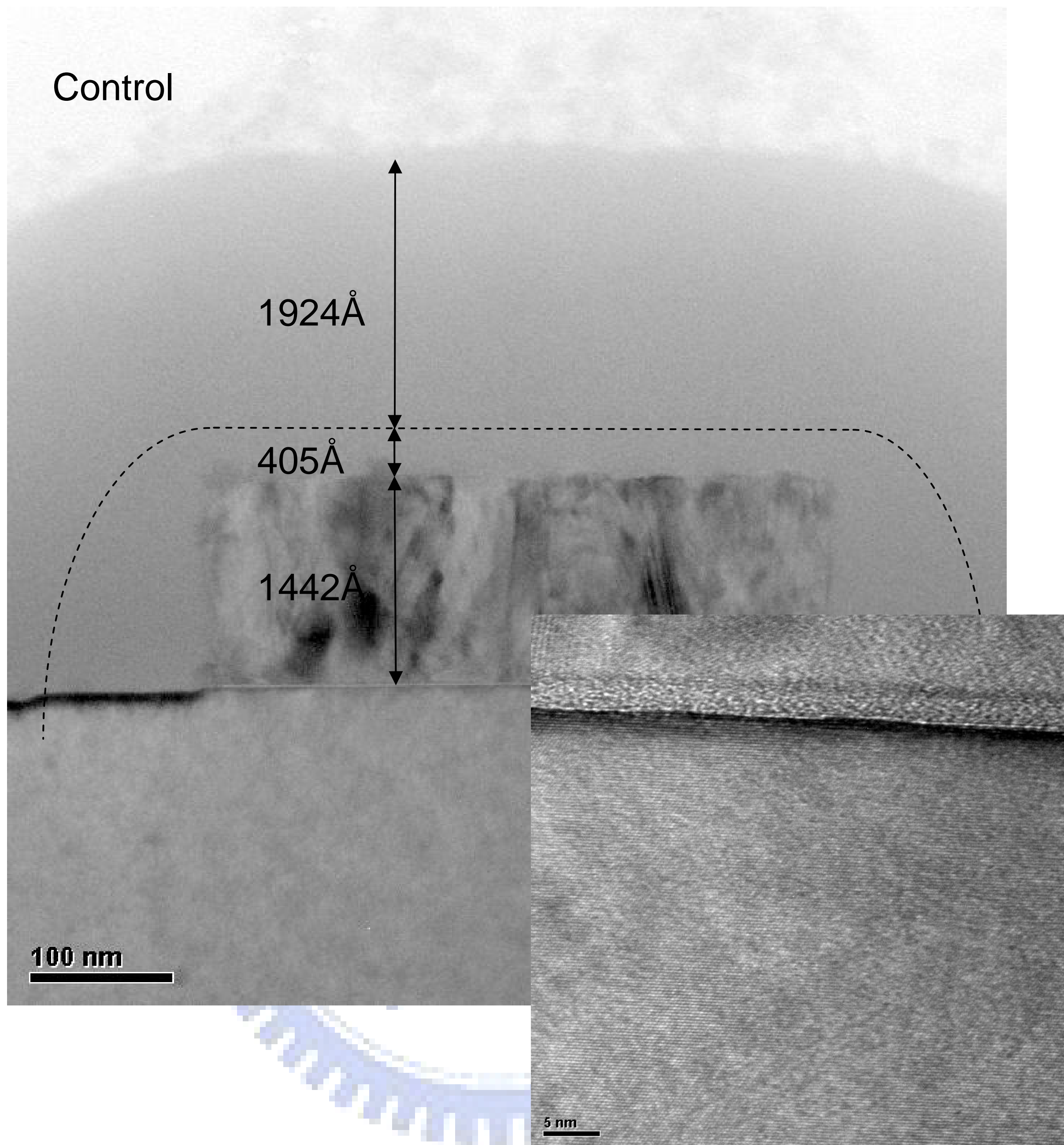

Fig. 2.1(b) Cross-sectional TEM pictures for control samples.

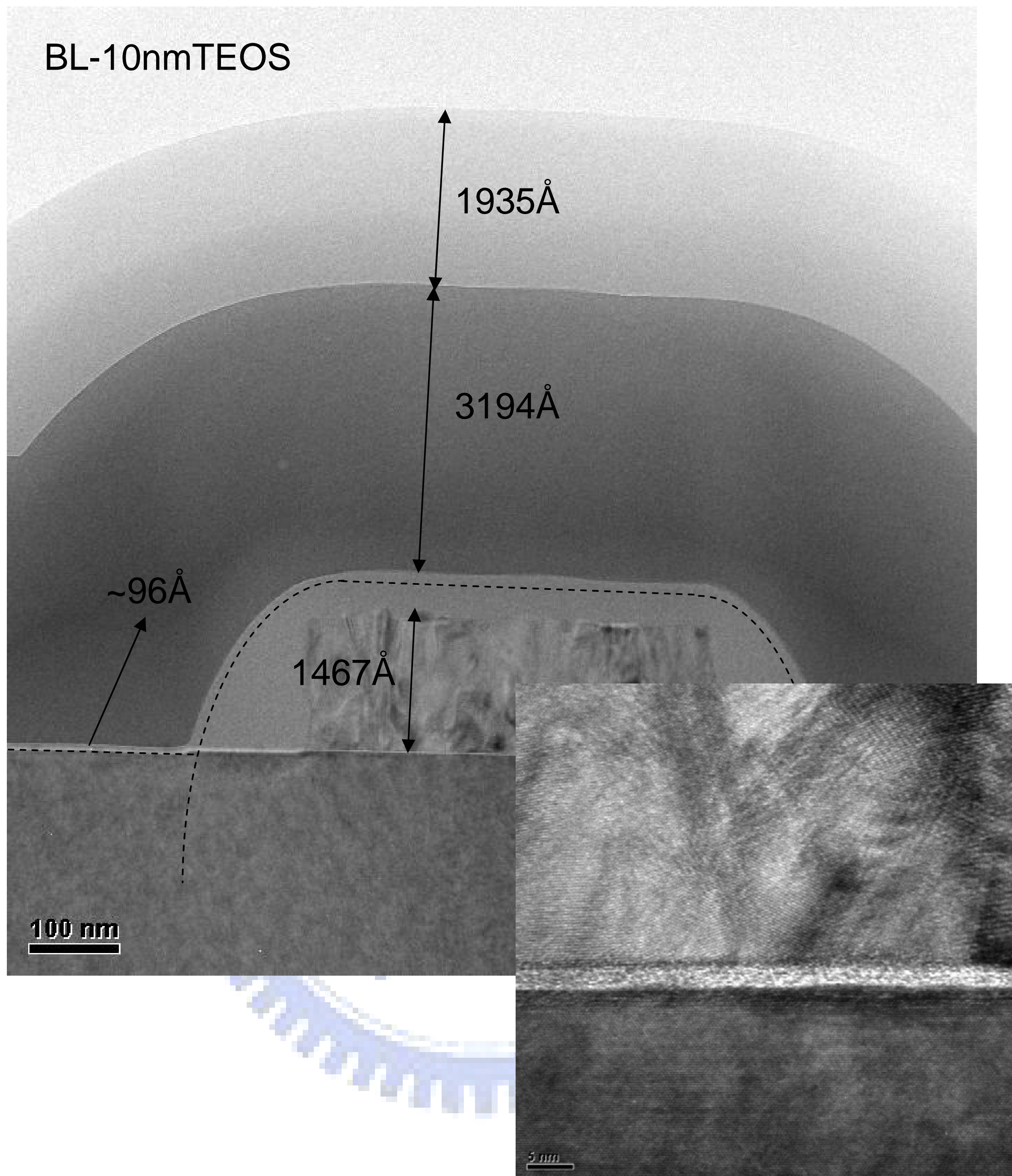

Fig. 2.1(c) Cross-sectional TEM pictures for BL-10nmTEOS samples.

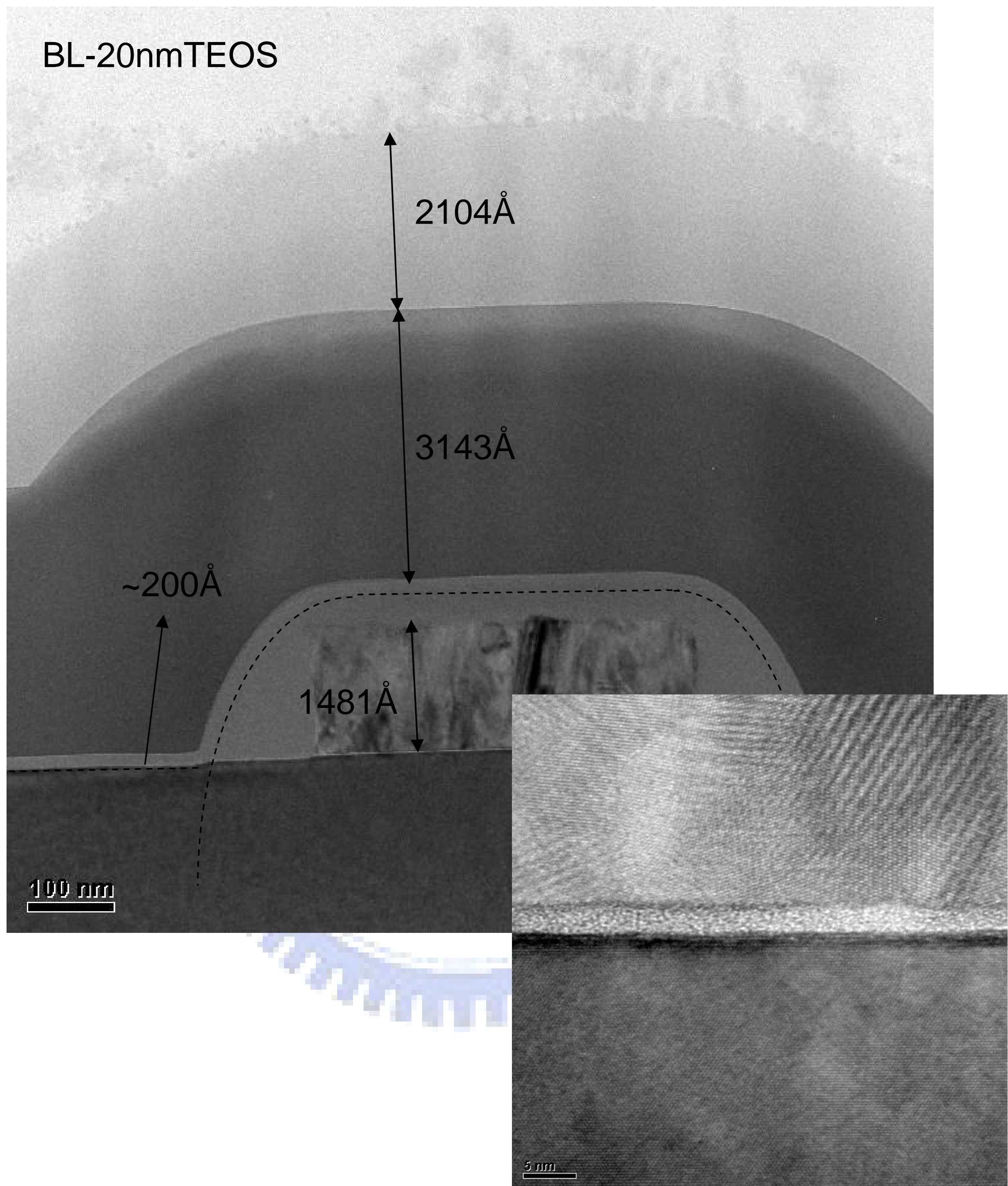

Fig. 2.1(d) Cross-sectional TEM pictures for BL-20nmTEOS samples.

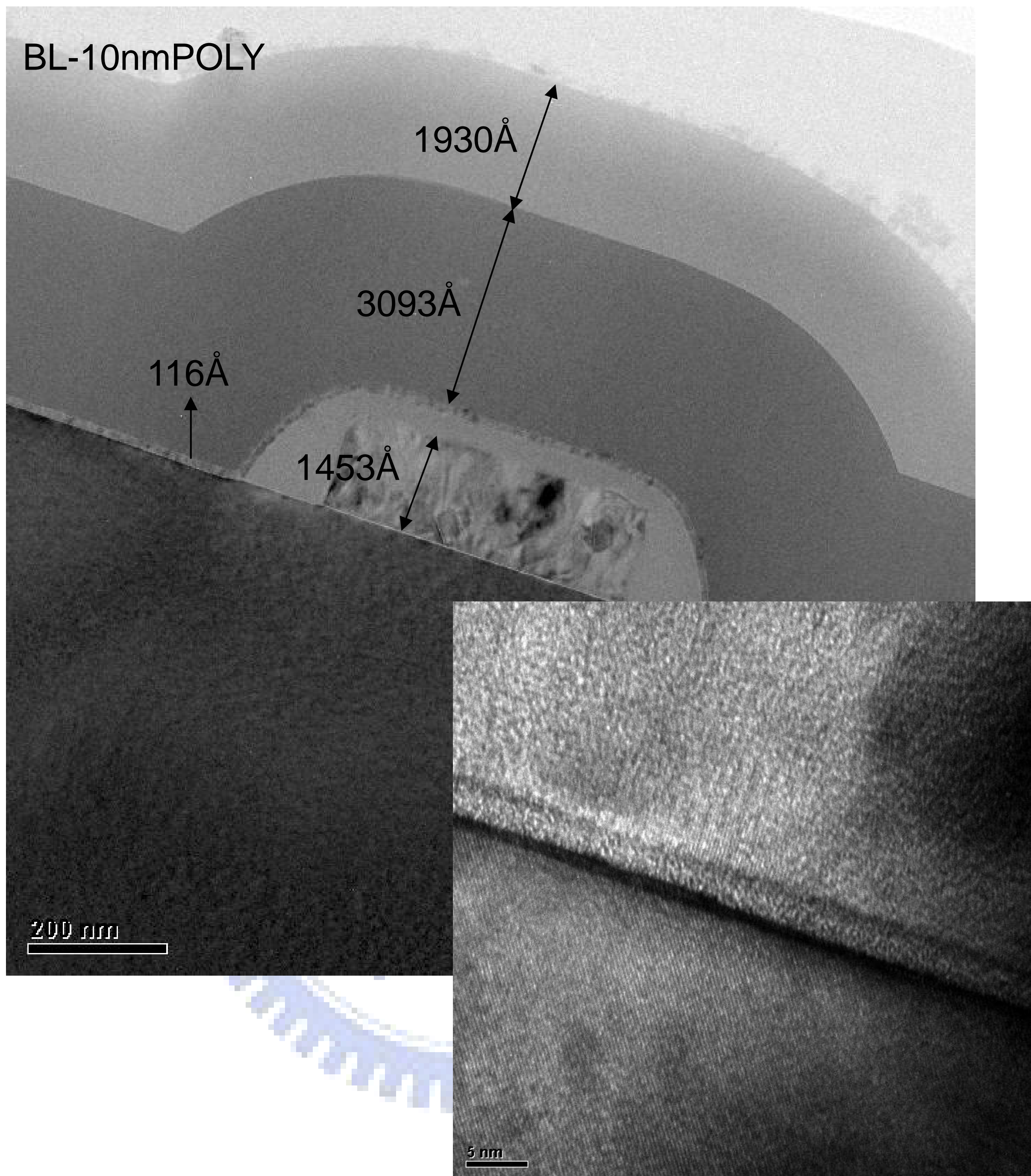

Fig. 2.1(e) Cross-sectional TEM pictures for BL-10nmPOLY samples.

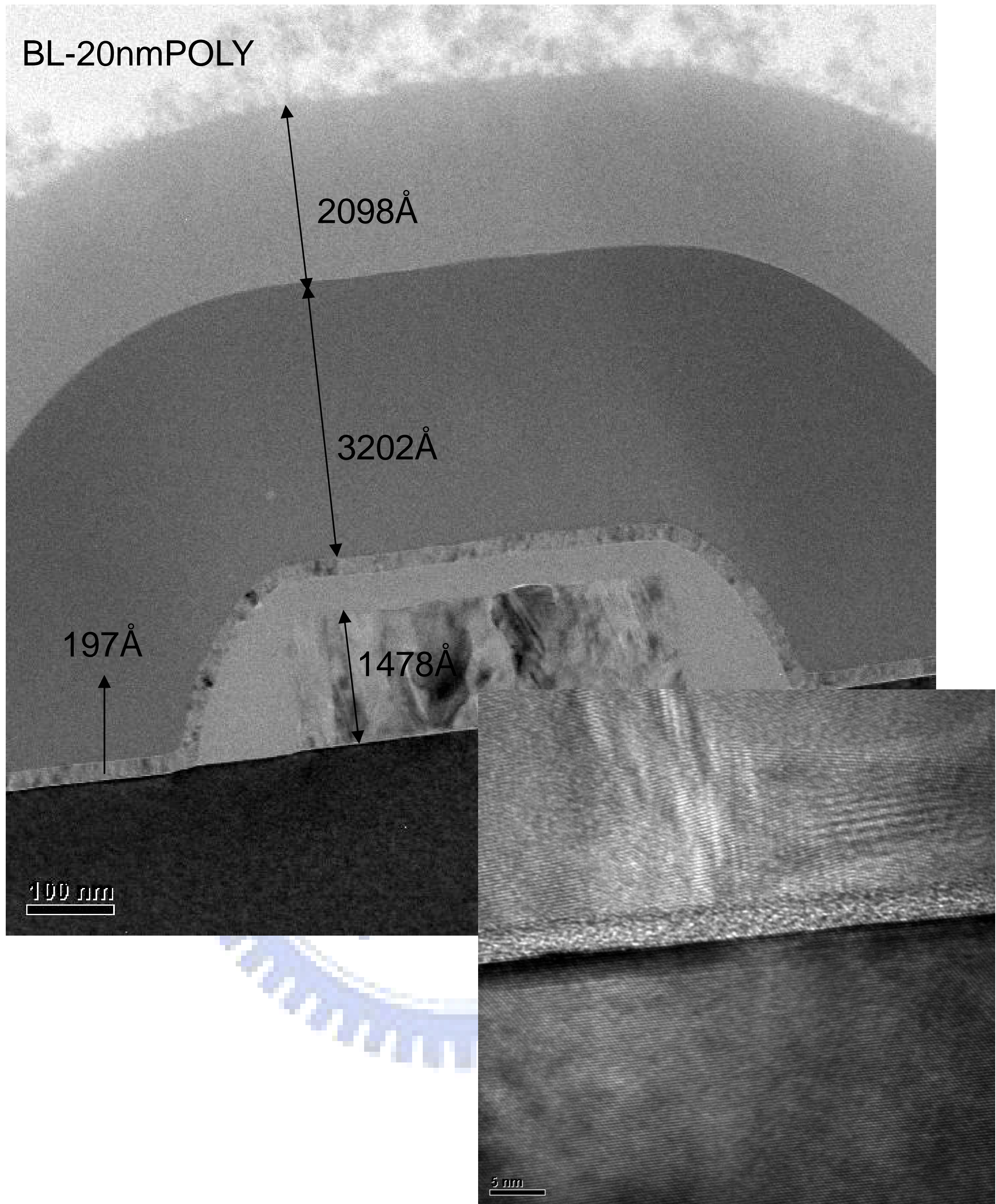

Fig. 2.1(f) Cross-sectional TEM pictures for BL-20nmPOLY samples.

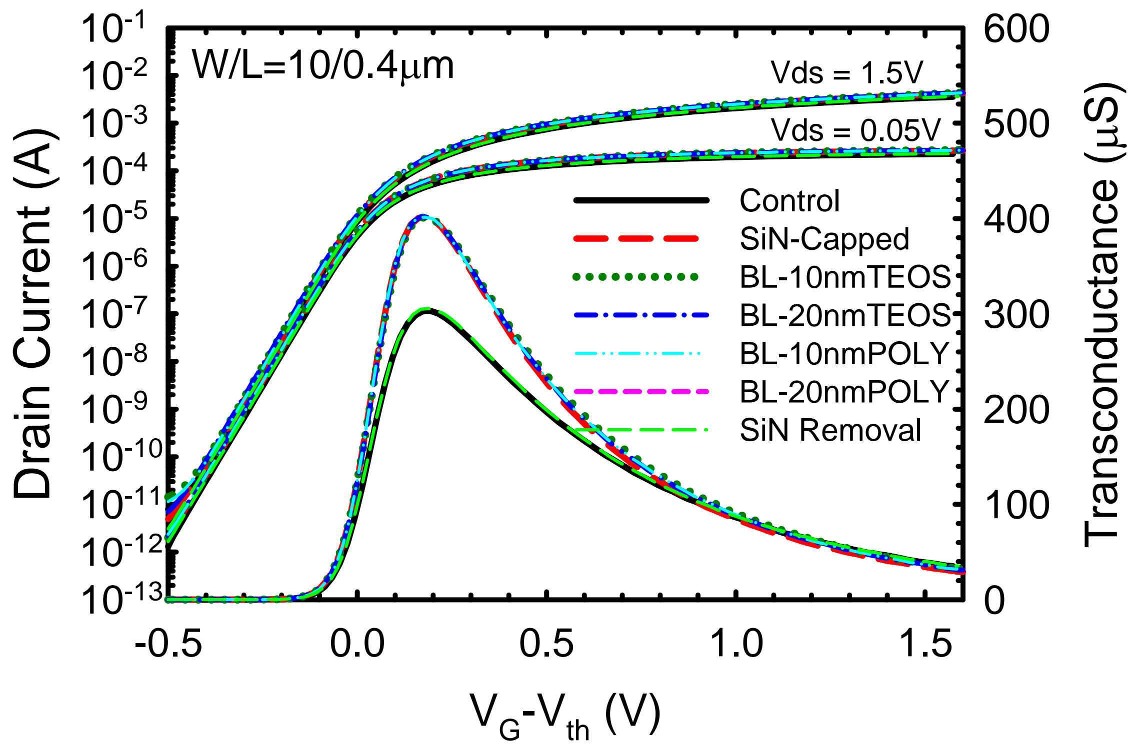

Fig. 2.2 NMOSFETs subthreshold characteristics and transconductance for all seven splits. The subthreshold swing is nearly identical among the seven splits, while the transconductance is obviously larger for the SiN-capped and all buffer layer samples.

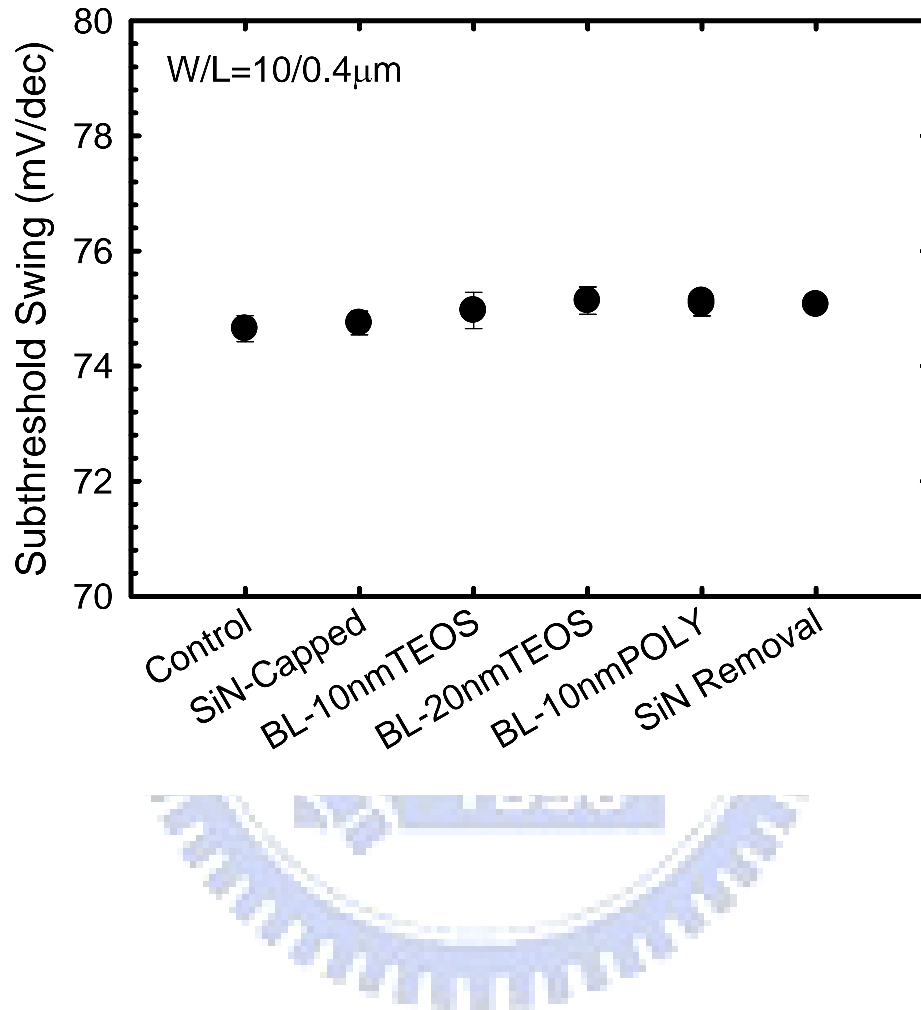

Fig. 2.3 Subthreshold swing of NMOSFETs for all splits of samples with W/L = 10/0.4 μm

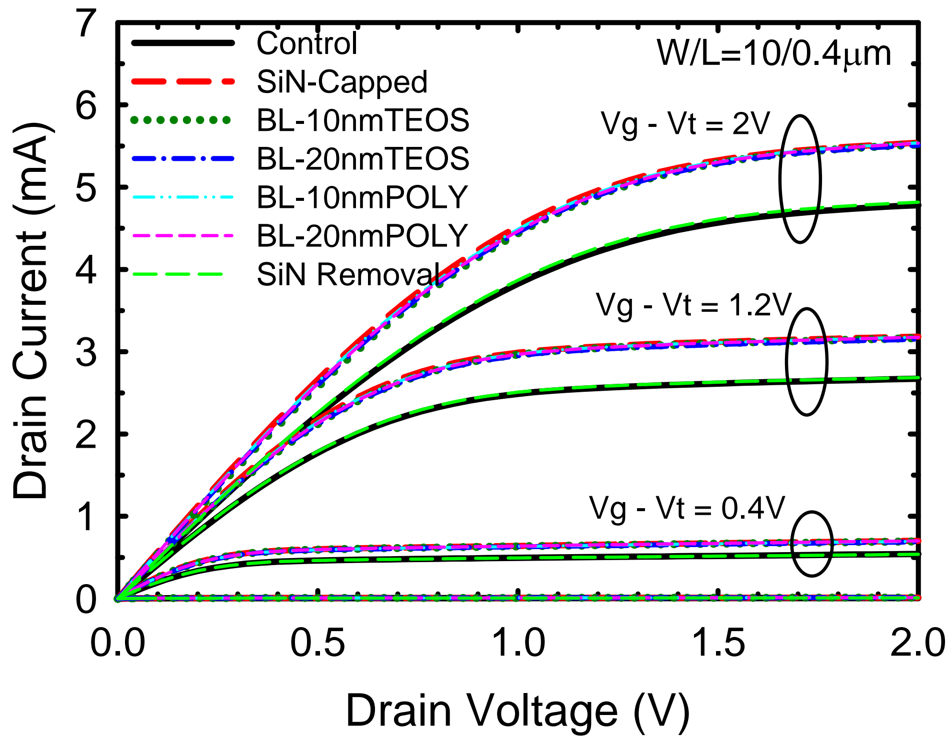

Fig. 2.4 Output characteristics of NMOSFETs for all splits. Drive current enhancement is clearly observed for the SiN-capped and all buffer layer splits. The SiN-removal samples show negligible enhancement.

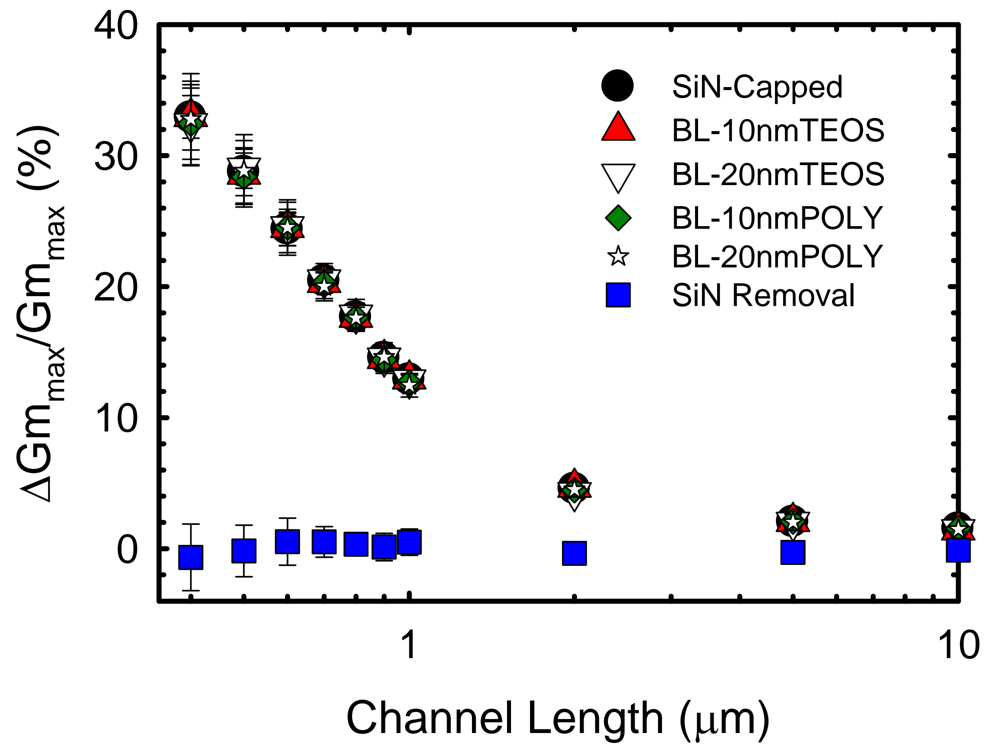

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Fig. 2.5 Percentage increase of transconductance versus channel length for all splits of samples with respect to the control ones. Each datum point represents the mean measurement result performed on six devices.

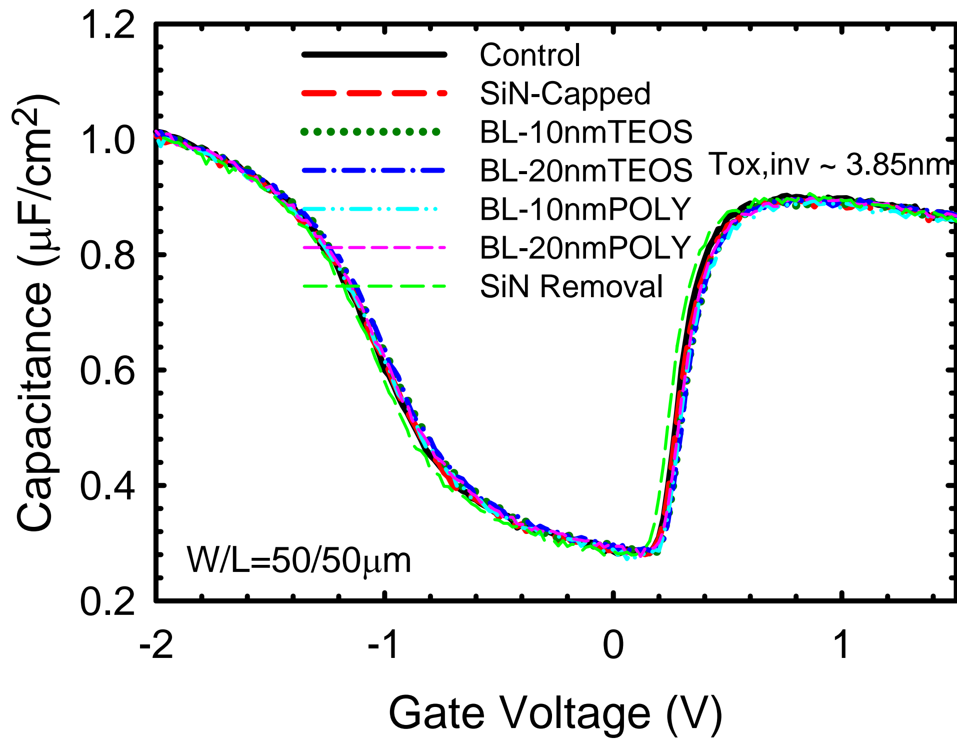

Fig. 2.6 Capacitance-Voltage (*C*-*V*) characteristics for all seven splits. Basically the seven splits show almost identical curve, indicating that the oxide thickness difference among these seven splits is negligible.

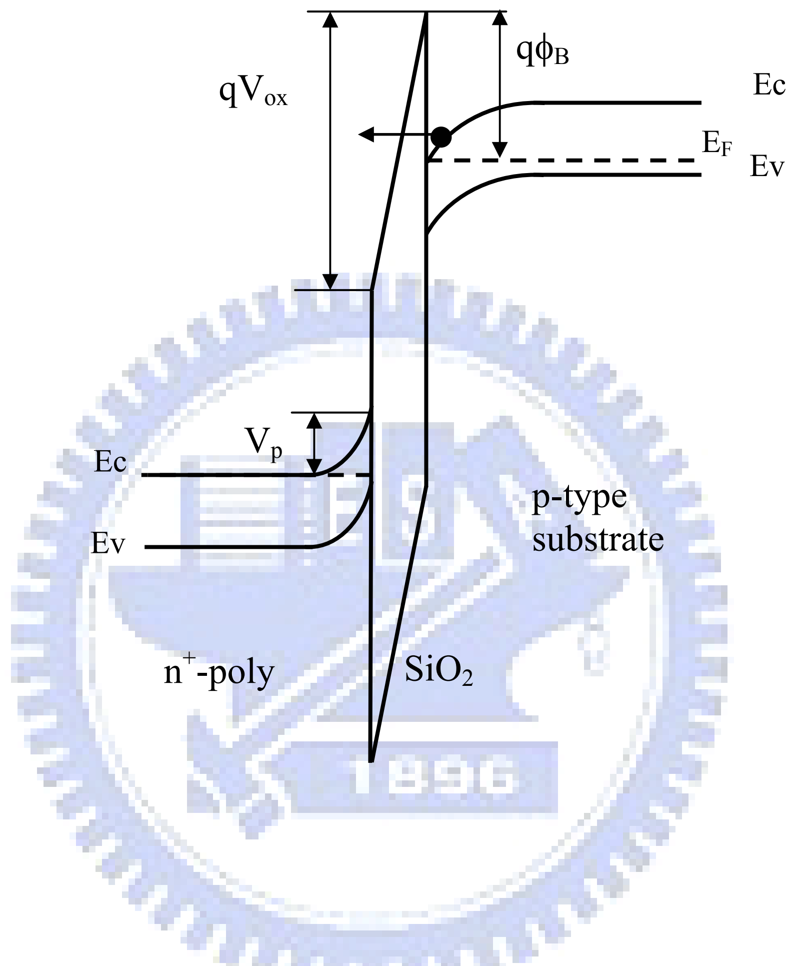

Fig. 2.7 Energy band diagram illustrating F-N tunneling.

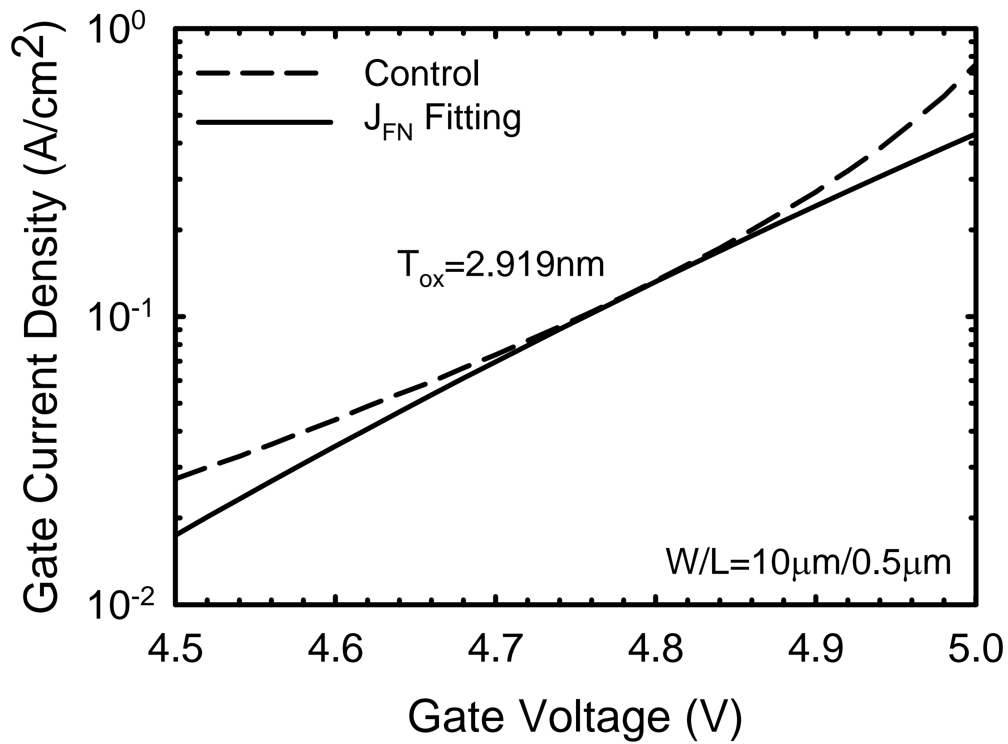

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Fig. 2.8 The plot of J_G versus V_G for control samples. The extracted oxide thickness by F-N current fitting is about 2.919 nm.

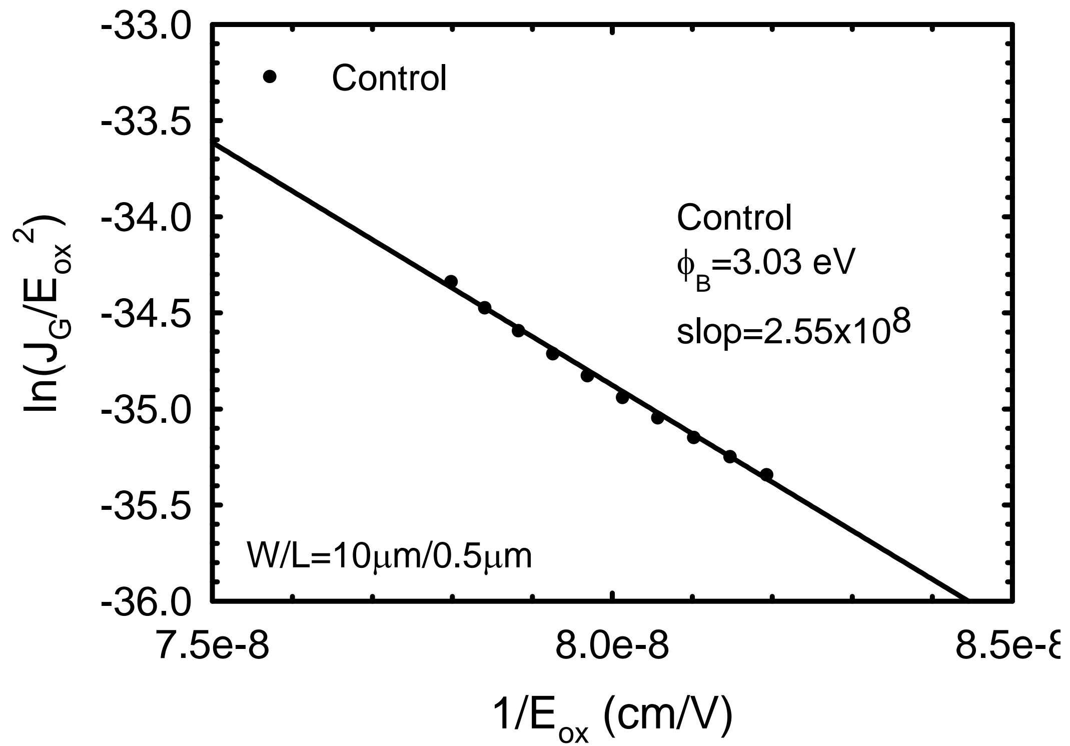

Fig. 2.9 F-N plot for control samples. The extracted barrier height is about 3.03 eV.

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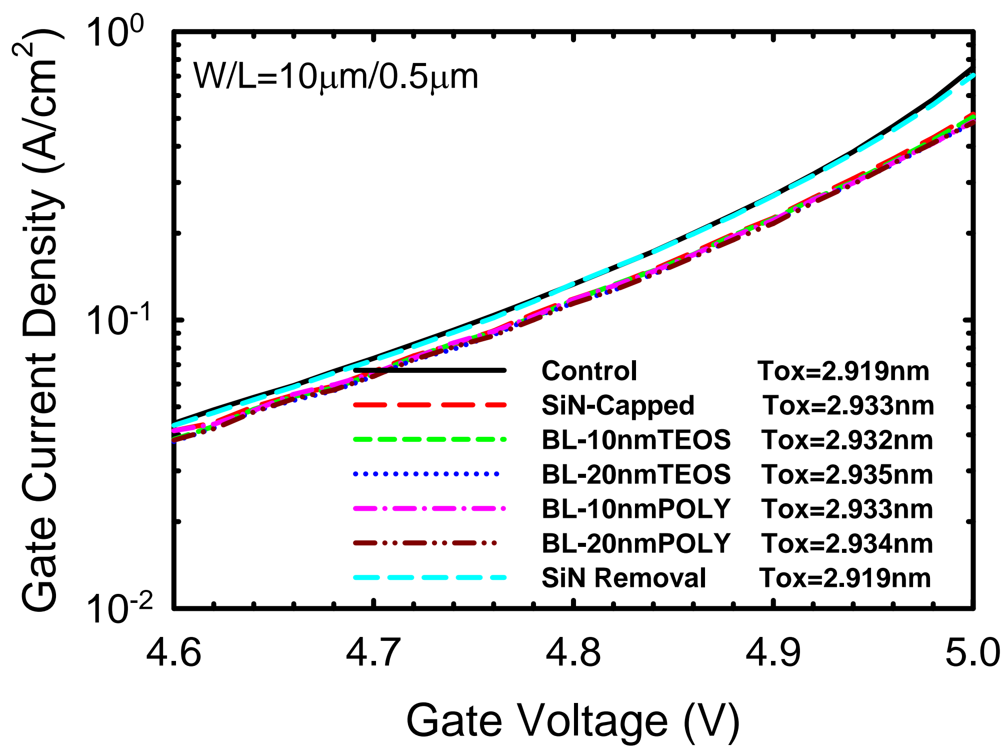

Fig. 2.10 The plot of J_G versus V_G for all splits.

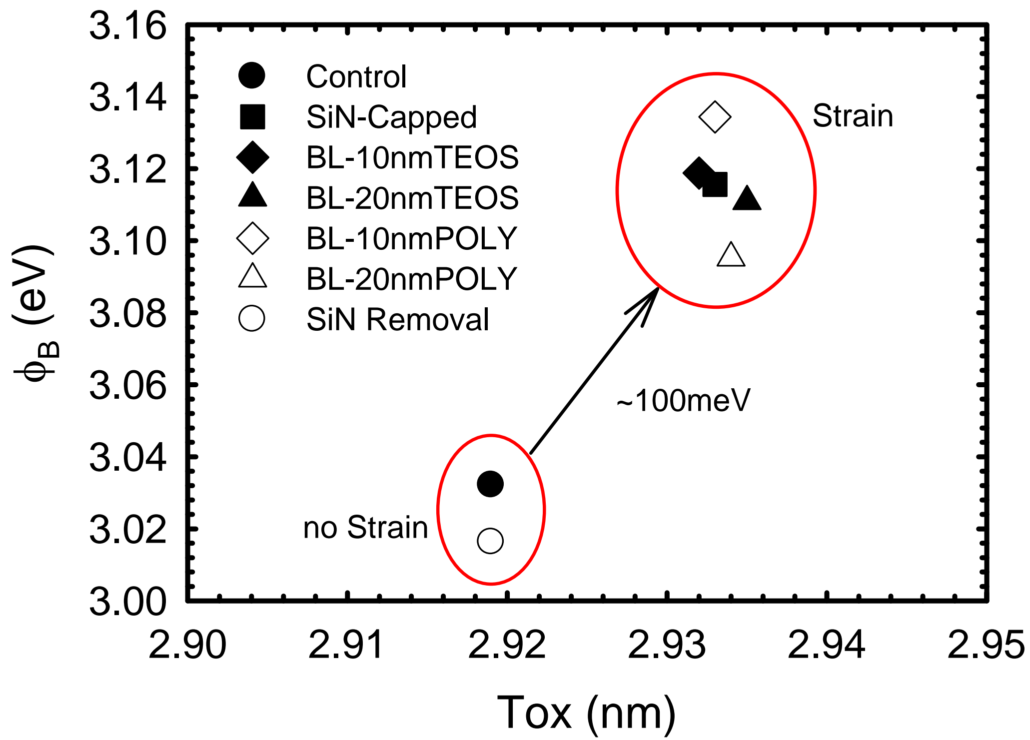

Fig. 2.11 The extracted barrier height versus gate oxide thickness for all splits. We can see that the barrier heights for all SiN capping samples are larger than control ones.

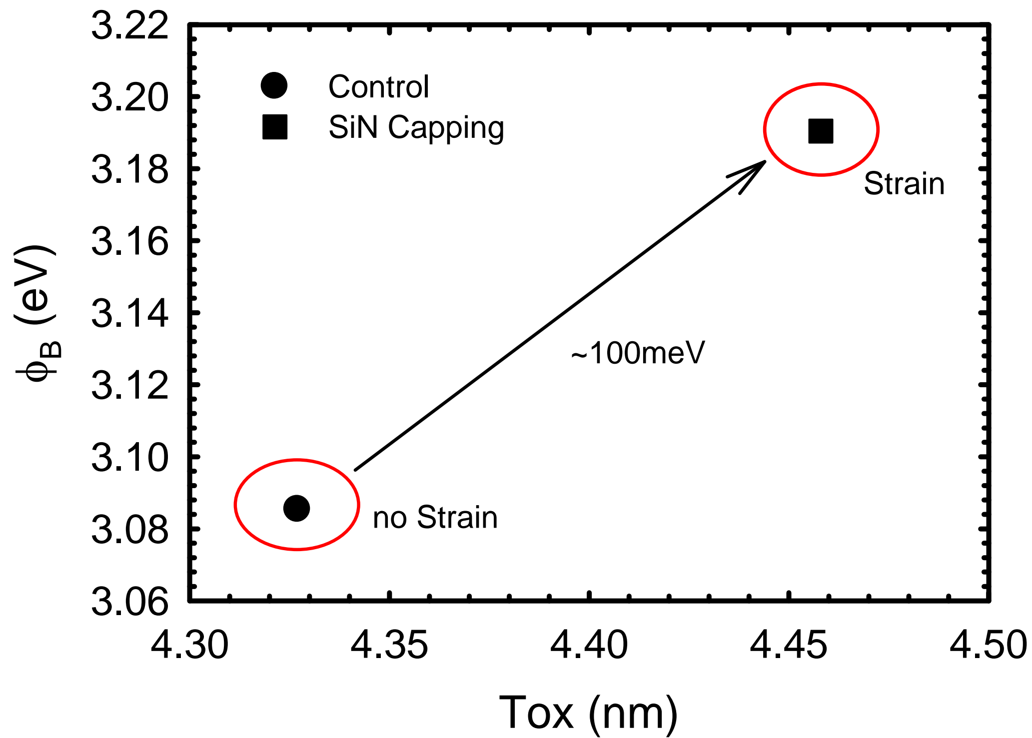

Fig. 2.12 The extracted barrier height for thicker gate oxide thickness (~4.3 nm). The barrier height for non-strained samples is close to 3.1 eV, while the SiN capping samples still exhibit barrier height increased of about 100 meV.

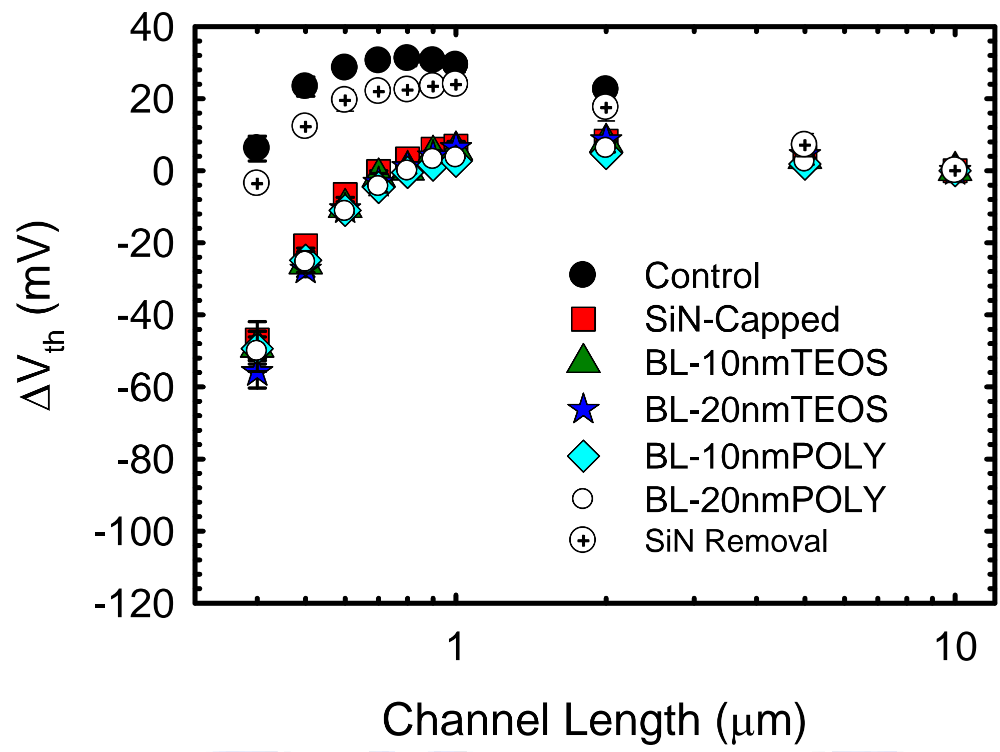

Fig. 2.13 Threshold voltage roll-off characteristics as a function of channel length for all splits of samples.

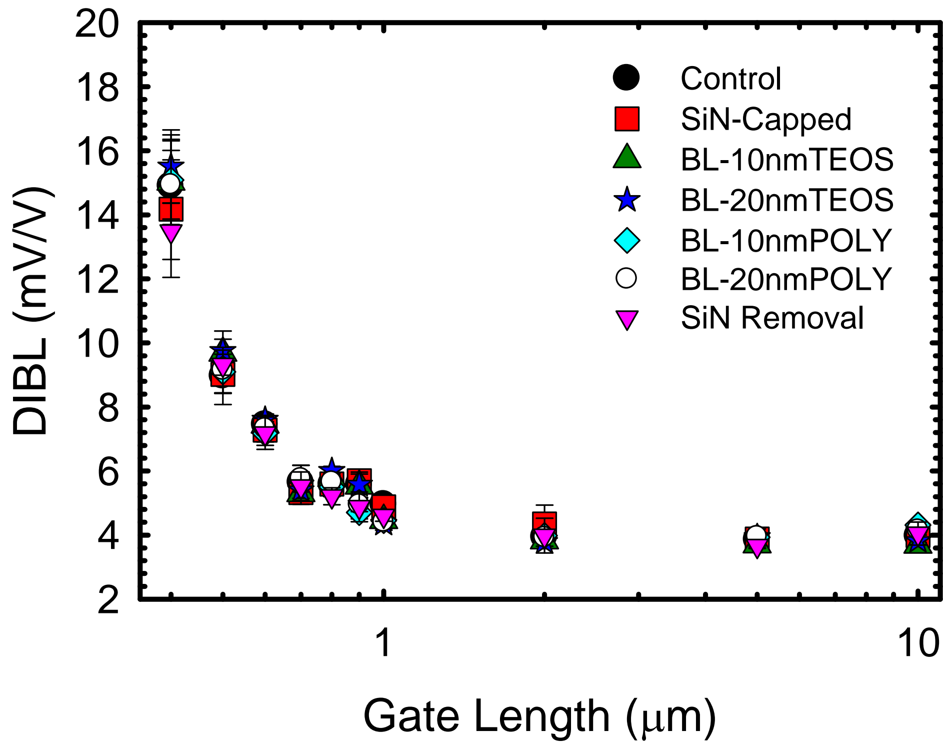

Fig. 2.14 Drain induced barrier lowering (DIBL) characteristics as a function of channel length for all splits of samples.

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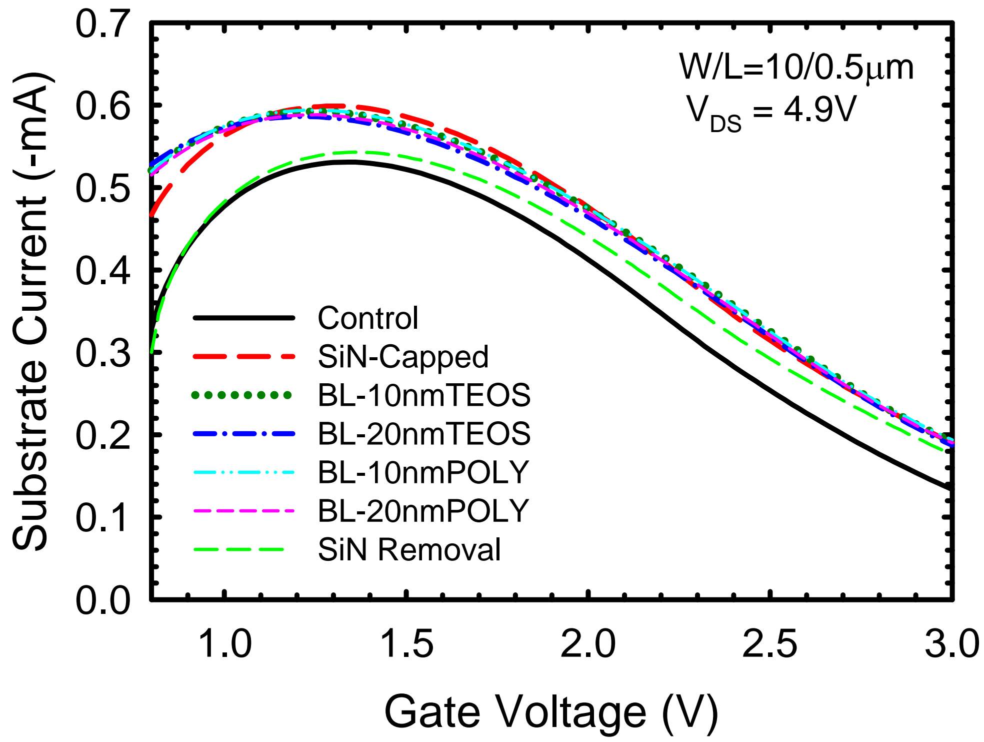

Fig. 2.15 Substrate current versus gate voltage for all splits of samples with W/L = 10/0.5 μm.

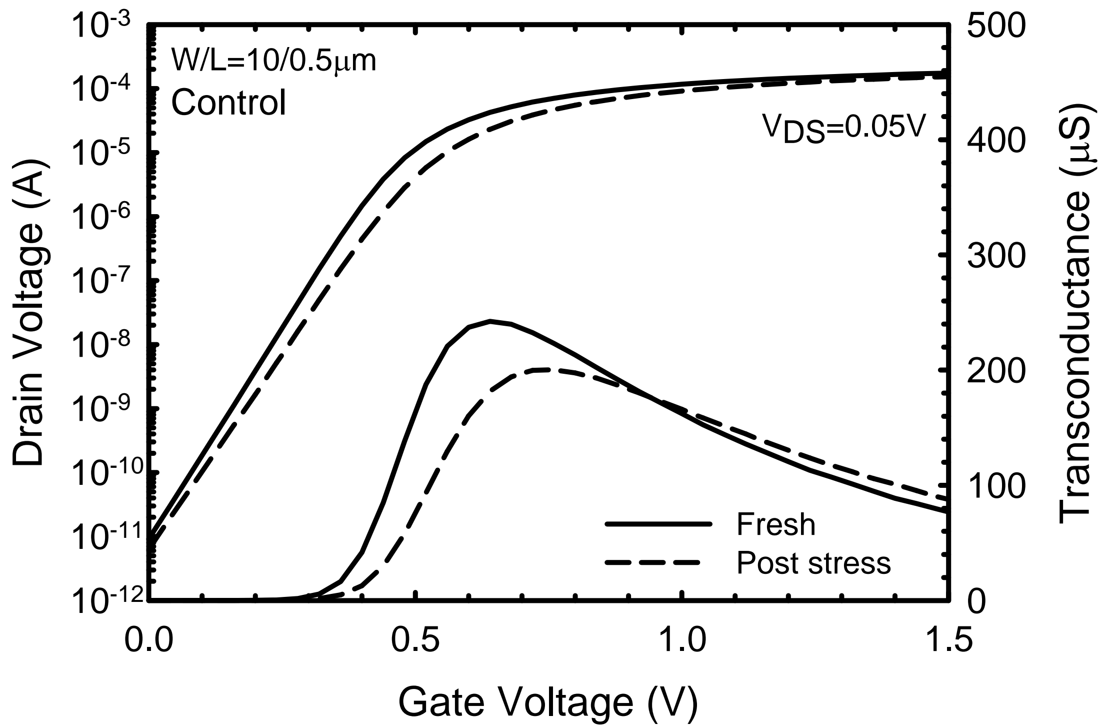

Fig. 2.16 (a) Subthreshold characteristics and tranconductance of devices with W/L = 10/0.5 μm before and after 5000 sec hot-carrier stressing for control samples.

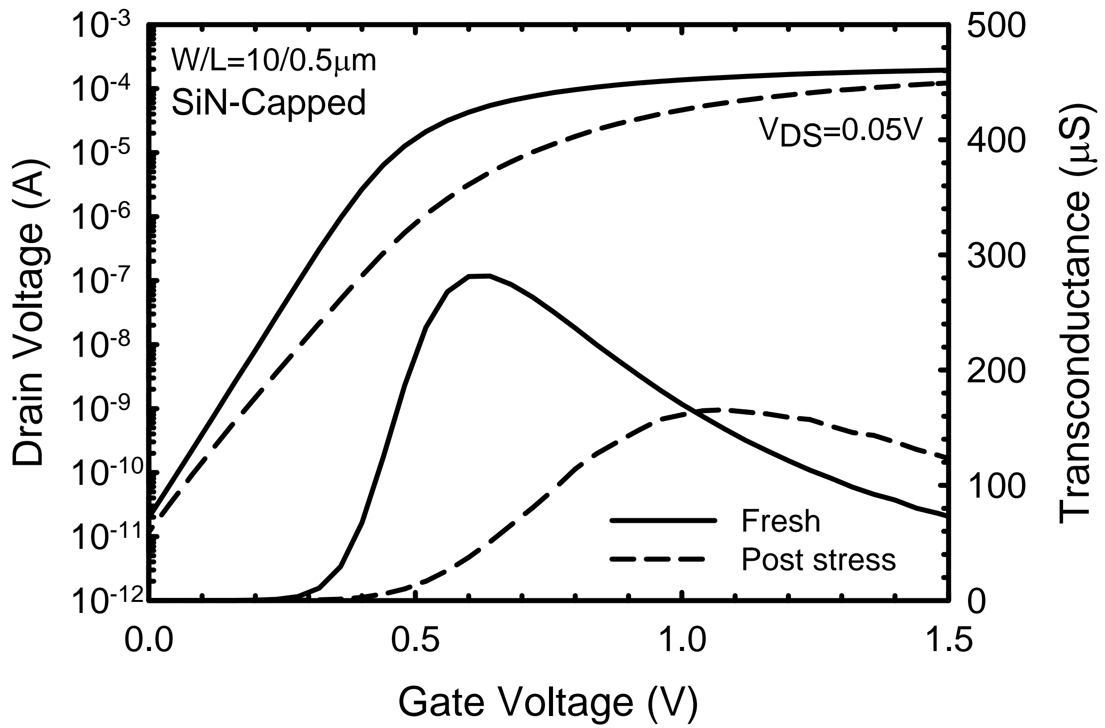

Fig. 2.16 (b) Subthreshold characteristics and tranconductance of devices with W/L = 10/0.5 μm before and after 5000 sec hot-carrier stressing for SiN-capped samples.

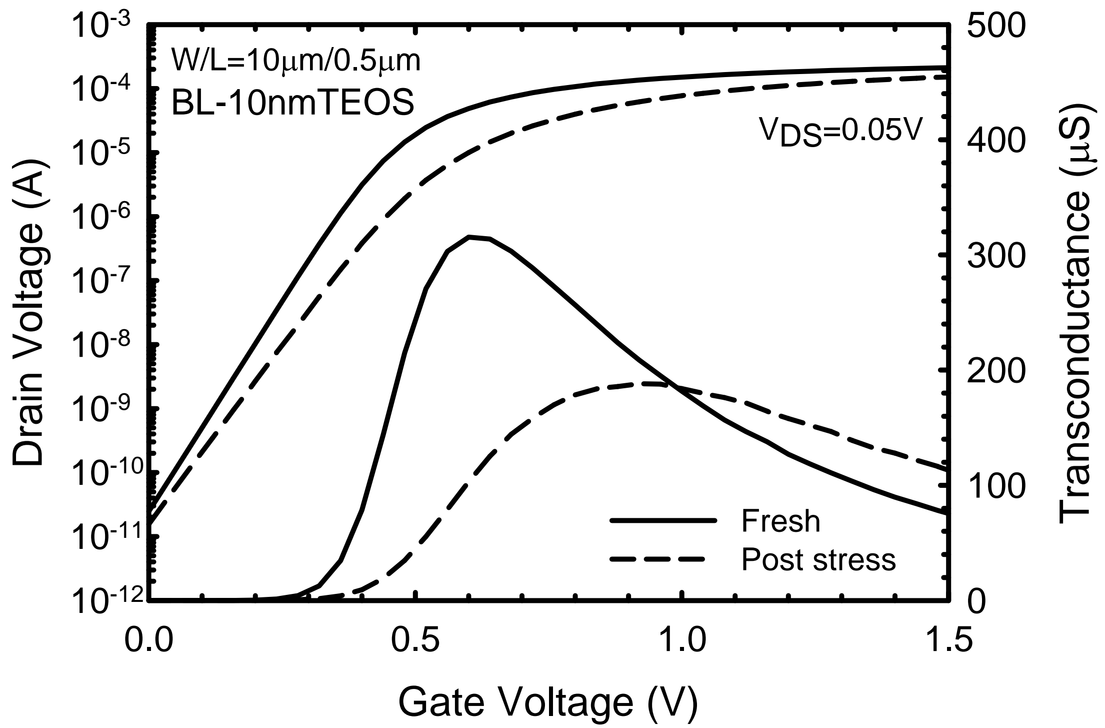

Fig. 2.16 (c) Subthreshold characteristics and tranconductance of devices with W/L = 10/0.5 μm before and after 5000 sec hot-carrier stressing for BL-10nmTEOS samples.

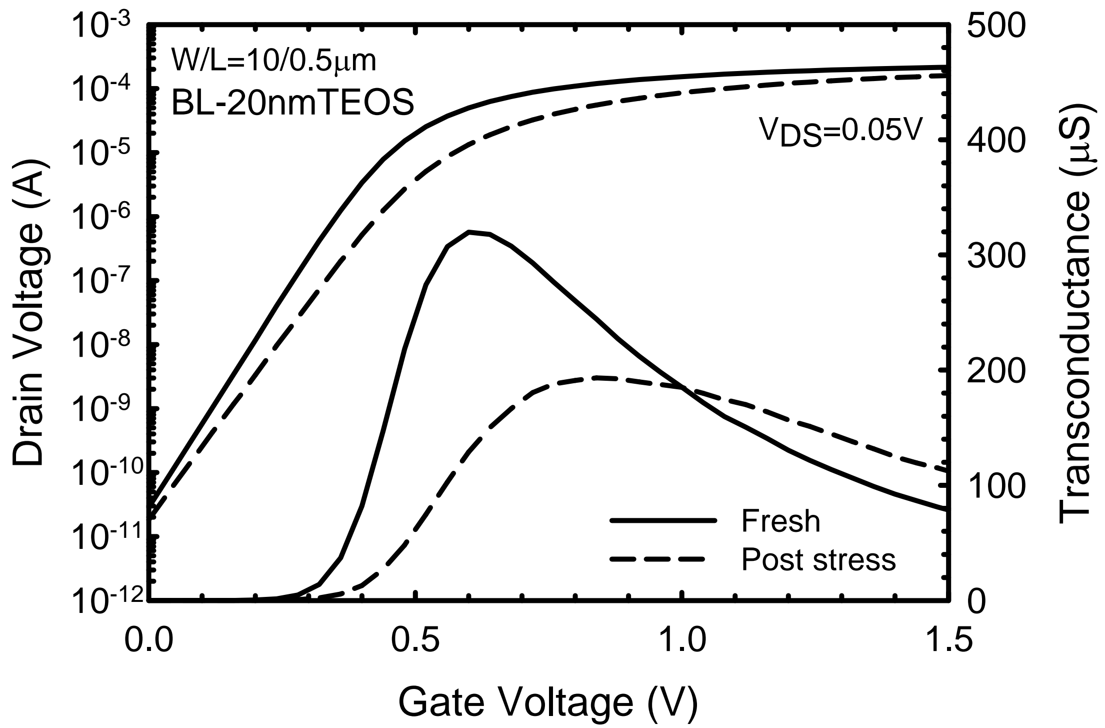

Fig. 2.16 (d) Subthreshold characteristics and tranconductance of devices with W/L = 10/0.5 μm before and after 5000 sec hot-carrier stressing for BL-20nmTEOS samples.

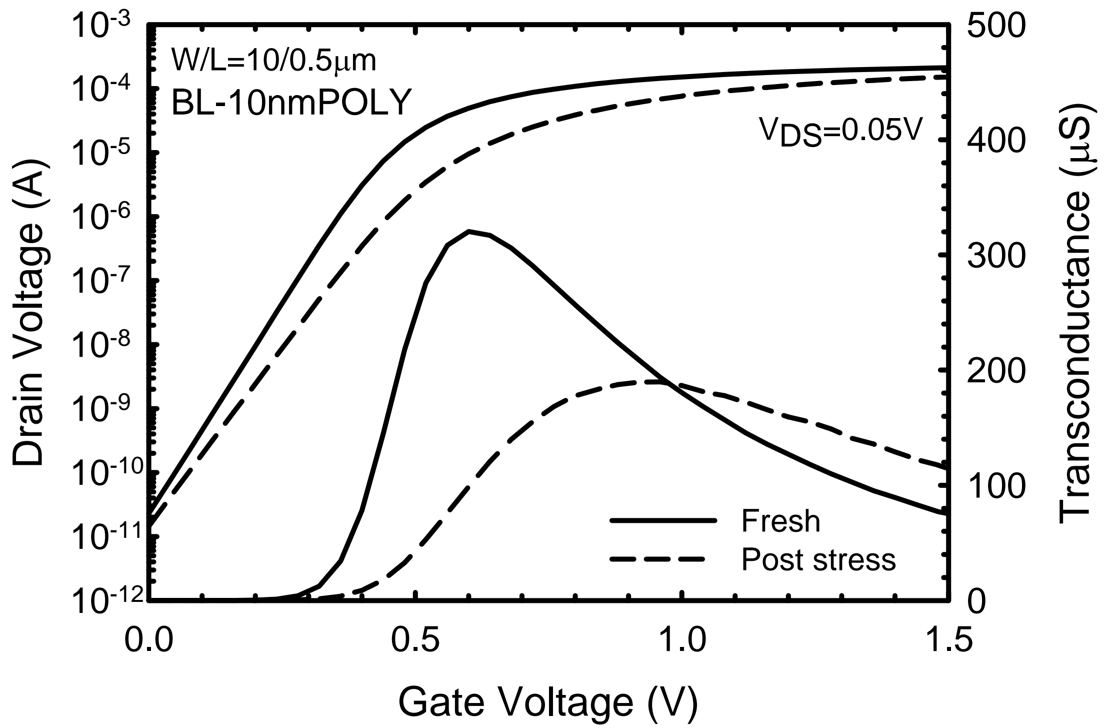

Fig. 2.16 (e) Subthreshold characteristics and tranconductance of devices with W/L = 10/0.5 μm before and after 5000 sec hot-carrier stressing for BL-10nmPOLY samples.

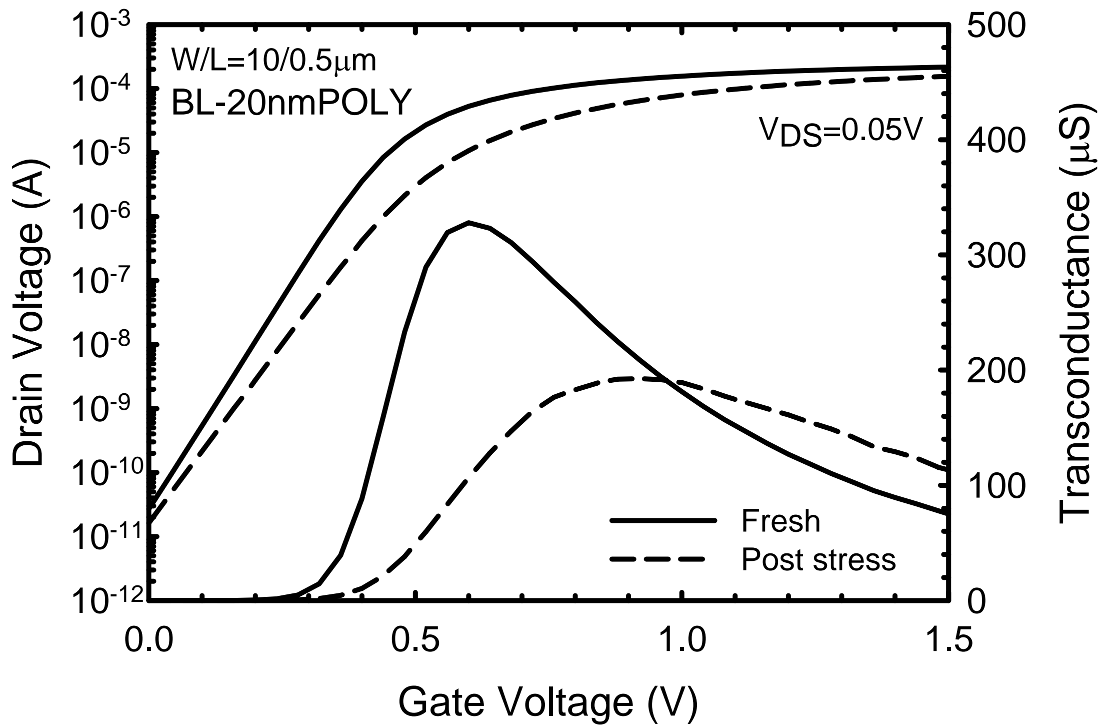

Fig. 2.16 (f) Subthreshold characteristics and tranconductance of devices with W/L = 10/0.5 μm before and after 5000 sec hot-carrier stressing for BL-20nmPOLY samples.

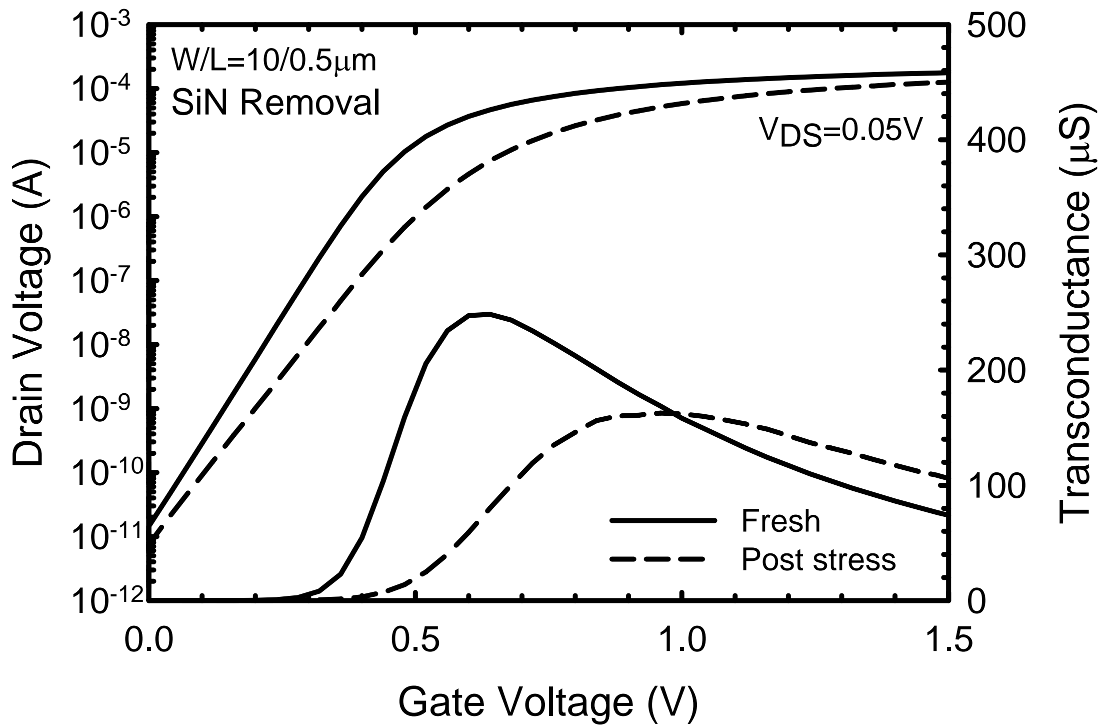

Fig. 2.16 (g) Subthreshold characteristics and tranconductance of devices with W/L = 10/0.5 μm before and after 5000 sec hot-carrier stressing for SiN-removal samples.

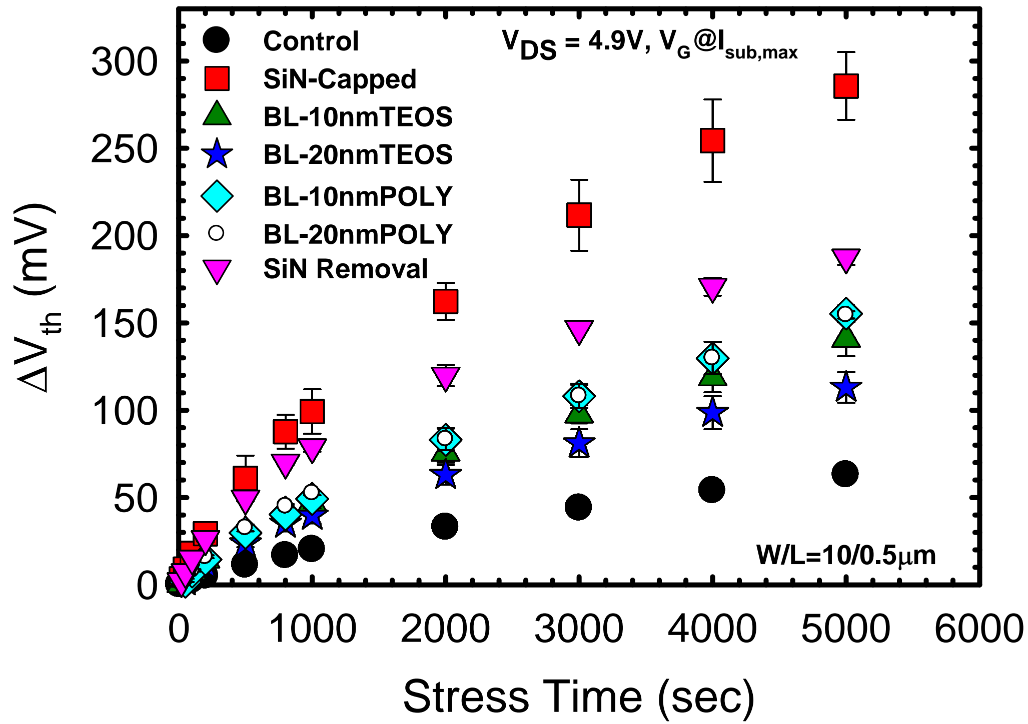

Fig. 2.17 Threshold voltage shift as a function of stress time. Devices with W/L = 10/0.5 μm were stressed at V_{DS} = 4.9 V, and V_G of maximum substrate current. Each datum point represents the mean measurement results performed on three devices.

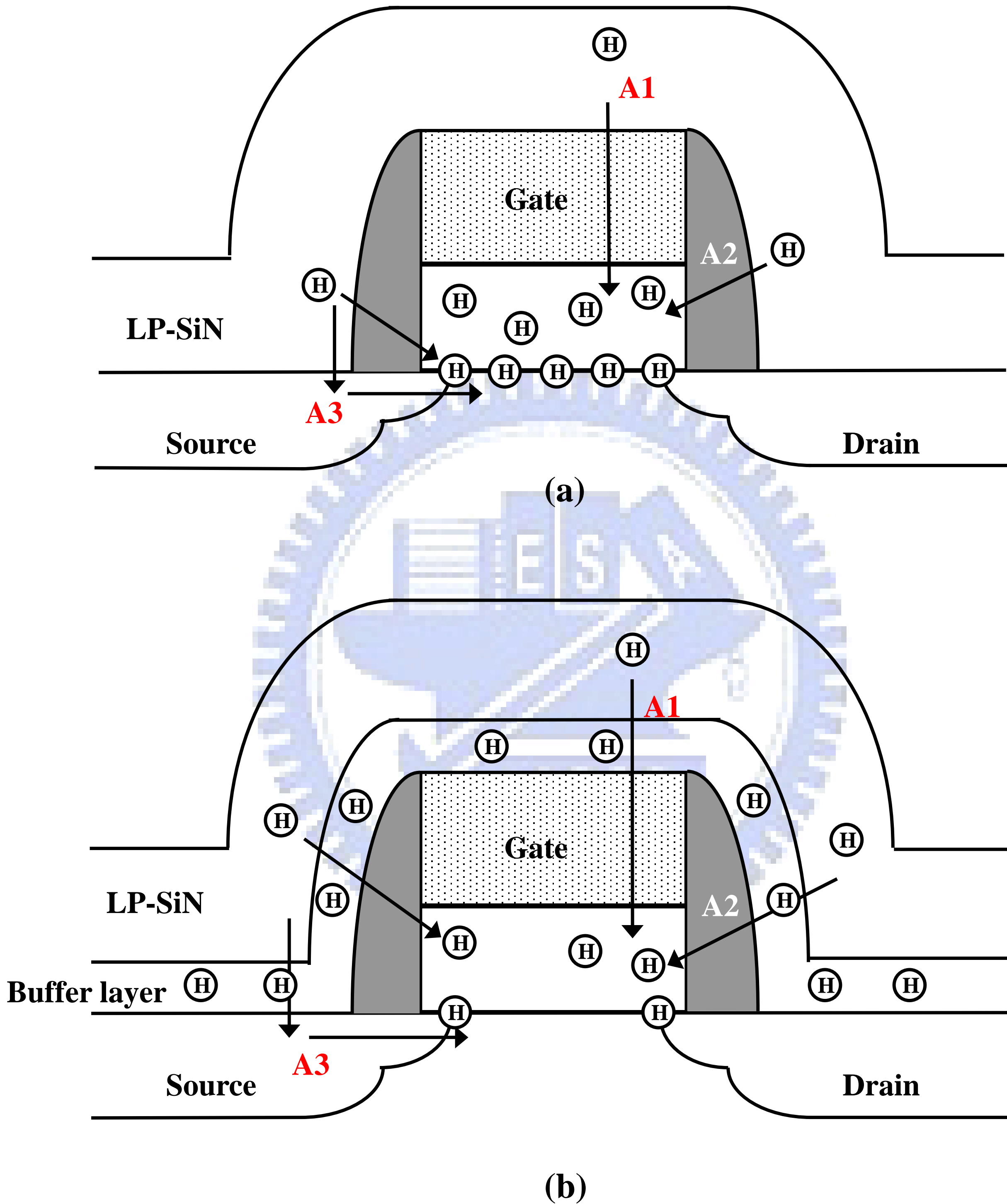

Fig. 2.18 (a) In SiN-capping devices, a large amount of hydrogen species from the SiN layer diffuse to the gate oxide layer and the channel region through three possible pathways. (b) In the devices with buffer layer, the diffusion of hydrogen species can be suppressed by the buffer layer.

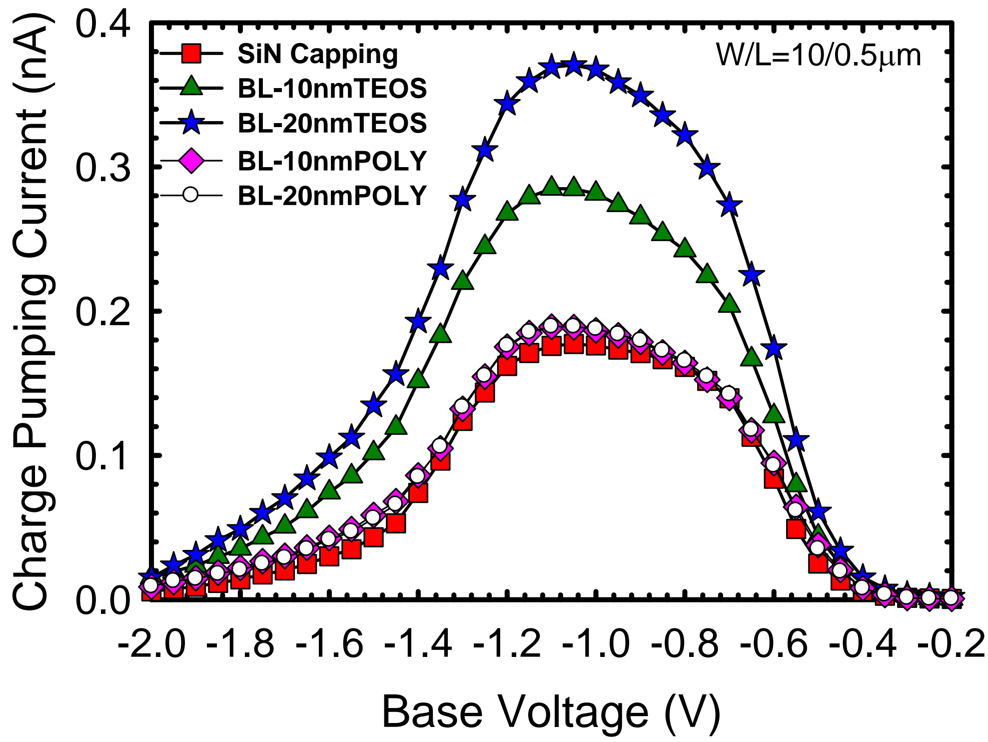

Fig. 2.19 Charge pumping current for all SiN capping samples with or without buffer layer with W/L = 10/0.5 μm.

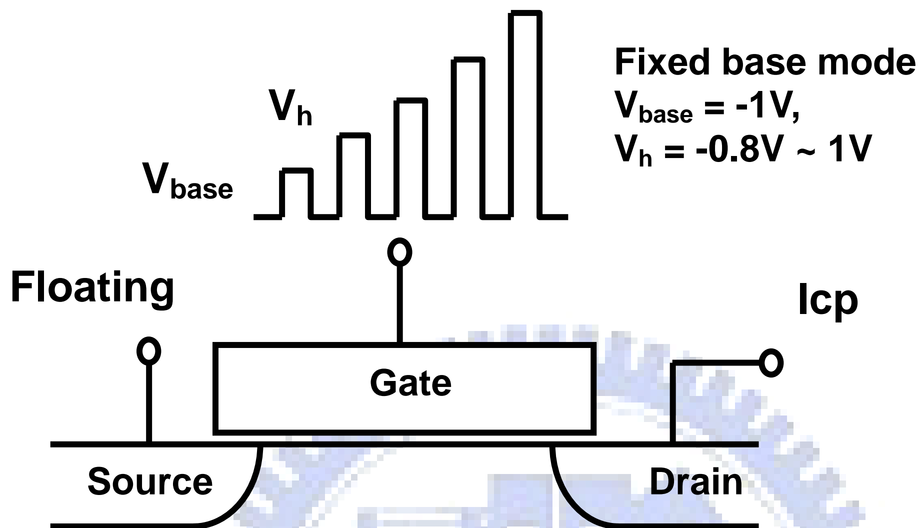

Fig. 2.20 Single junction charge pumping measurement setup.

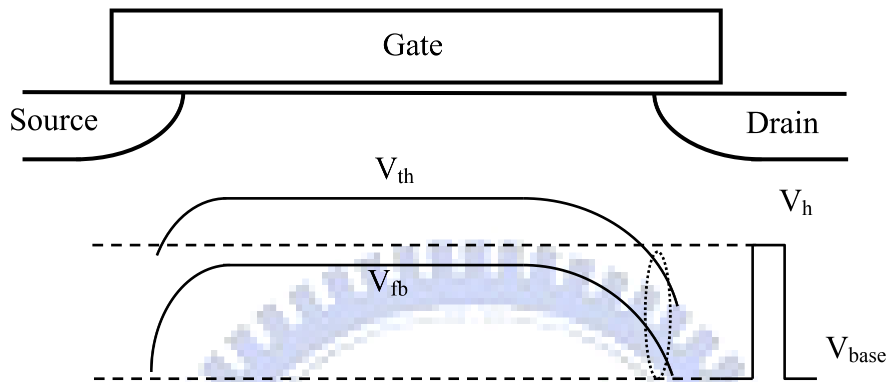

Fig. 2.21 Nonuniform distribution of local threshold voltage and flat band voltages across device caused by variation in lateral doping concentration.

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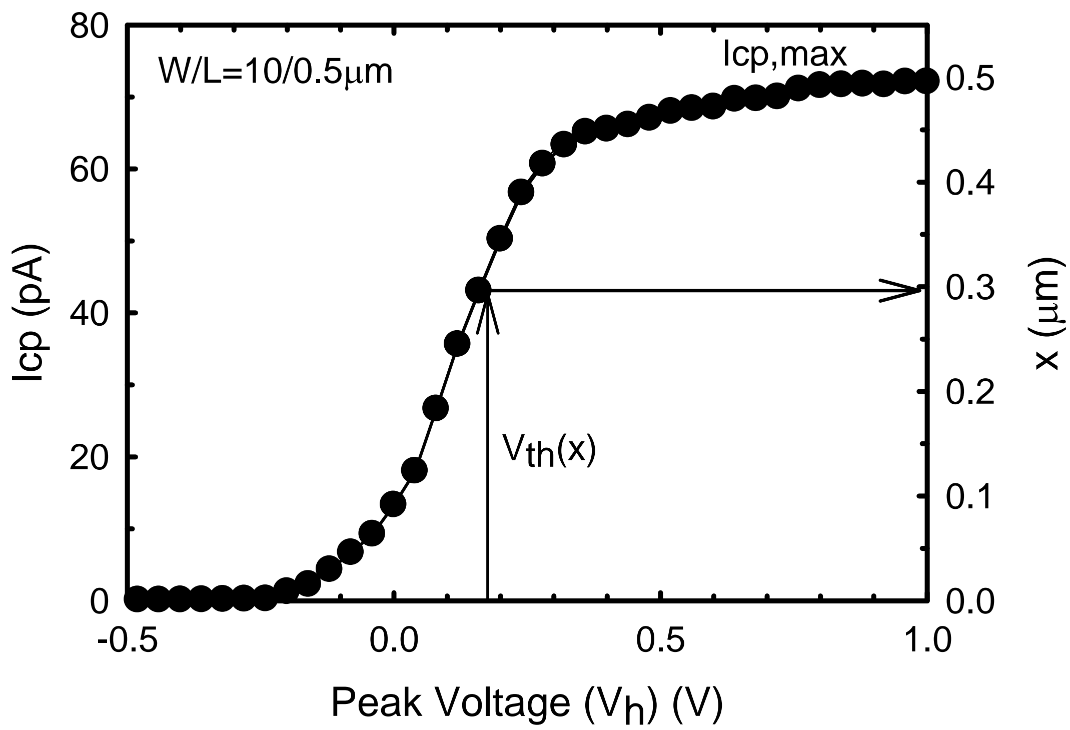

Fig. 2.22 Derived relationship between local threshold voltage and lateral distance x from single junction charge pumping data of control device.

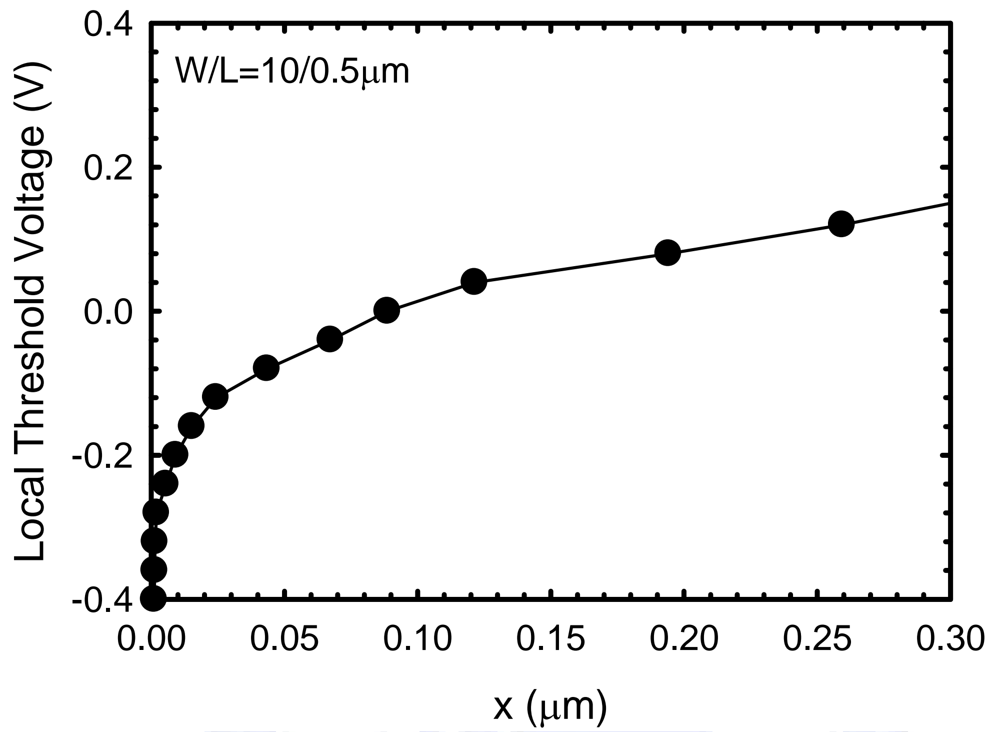

Fig. 2.23 Extracted lateral profile of local threshold voltage near graded drain junction in control sample.

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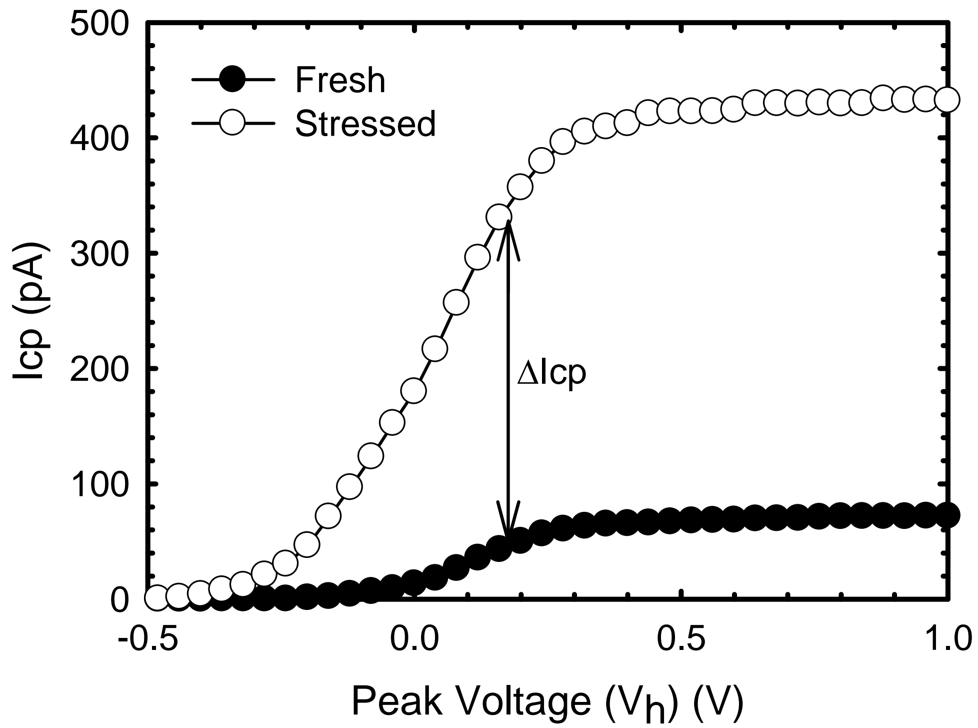

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Fig. 2.24 Charge pumping current before and after 100 s hot-carrier stressing (V_G at $I_{sub,max}$ and V_{DS} = 4.9V) with W/L = 10/0.5 μm.

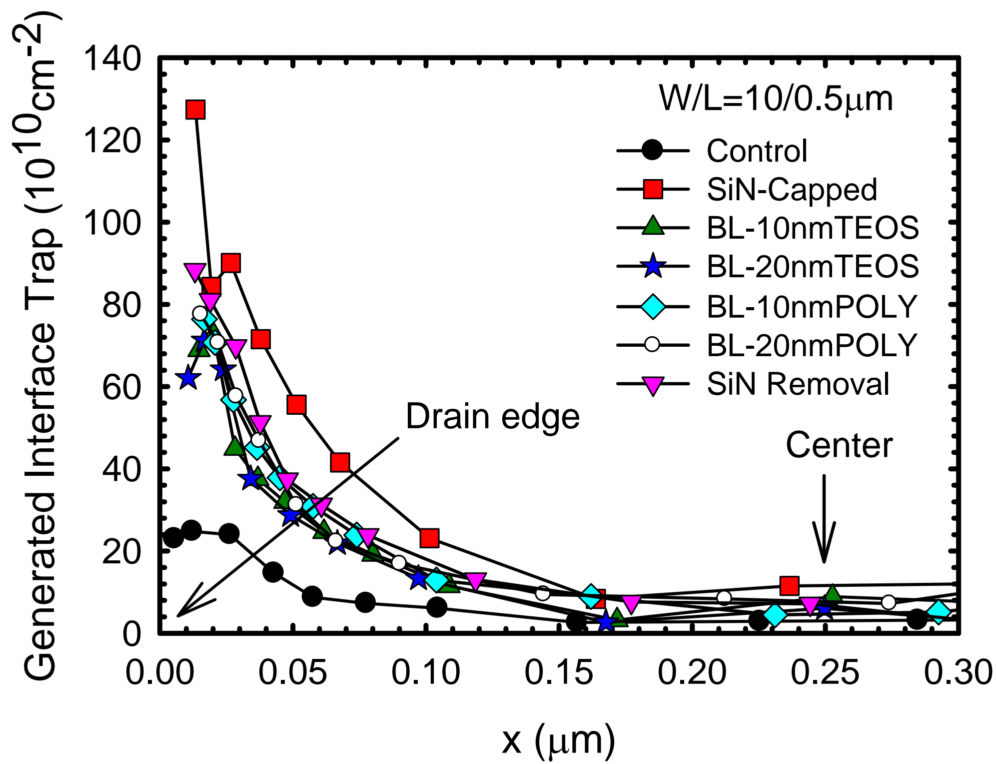

Fig. 2.25 Lateral profile of interface state generation after hot-carrier stress for all splits of samples.

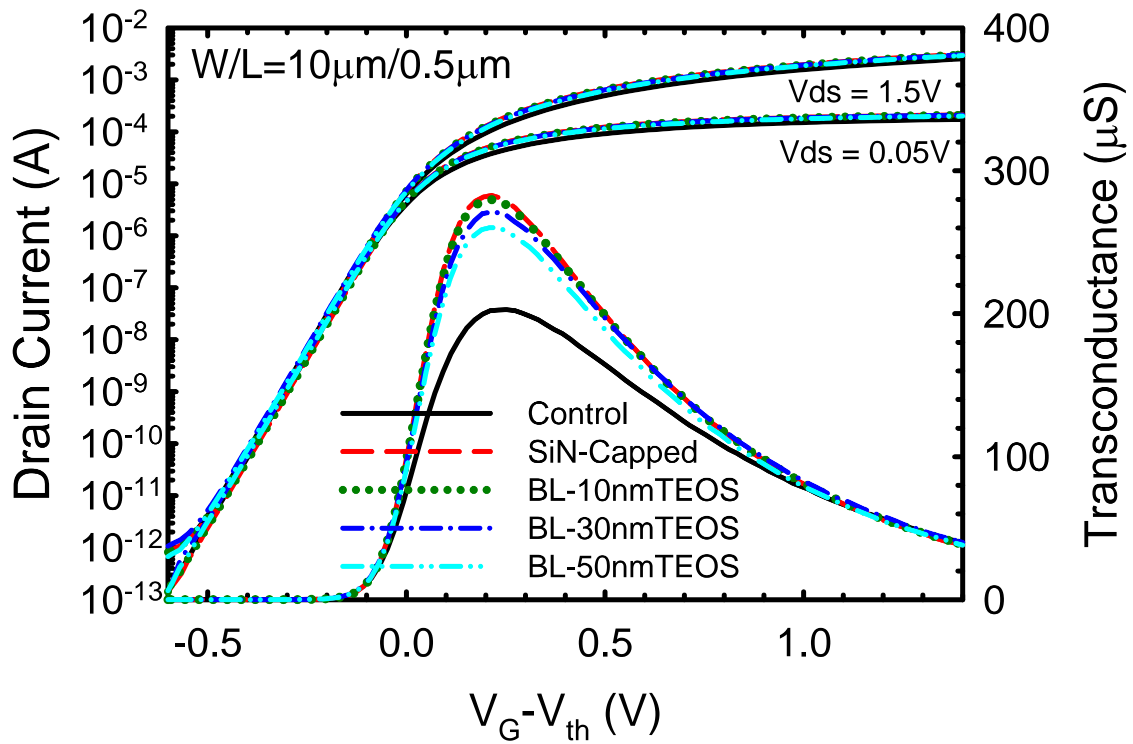

Fig. 2.26 NMOSFETs subthreshold characteristics and transconductance for control, SiN-capped, BL-10nmTEOS, BL-30nmTEOS, and BL-50nmTEOS splits. The transconductance enhancement starts to diminish for BL-30nmTEOS split.

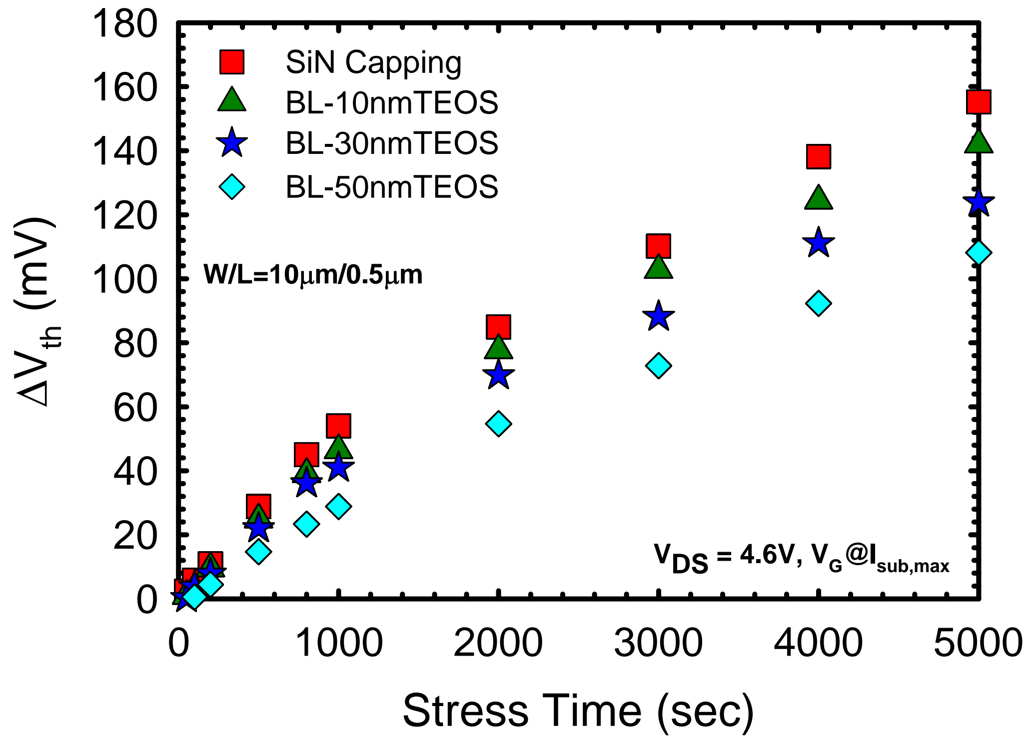

Fig. 2.27 Threshold voltage shift as a function of stress time. Devices with W/L = 10/0.5 μm were stressed at V_{DS} = 4.6 V, and V_G of maximum substrate current.

Chapter 3

Optimization of SiN Deposition Conditions and Its Impacts on Strained n- and p-Channel MOSFETs

3.1 Introduction

Channel strain engineering such as embedded SiC source/drain (S/D) [1-2] and highly tensile SiN capping layer [3-4,10-13] for n-channel metal-oxide-semiconductor field-effect-transistors (NMOSFETs) or embedded SiGe S/D [5-8] and highly compresseive SiN capping layer [7-9] for PMOSFETs has been pursued aggressively for mobility enhancement in scaled complementary metal-oxide-semiconductor (CMOS) devices. Among these methods, SiN capping technique has received much attention because it is easily implemented in modern VLSI technology. In addition, depending on the SiN deposition conditions, stress from highly tensile to highly compressive is adjustable, enabling the dual-SiN stressor technology for CMOS manufacturing [10].

Although SiN capping can dramatically enhance the device performance, the abundant hydrogen species generated during the SiN deposition process may diffuse into the channel region, resulting in aggravated hot-carrier degradations [11]. Recently, the insertion of an ultra-thin buffer layer underneath the SiN capping layer has been proposed to suppress the hydrogen diffusion and restore the reliability without compromising device performance [12-13]. In this thesis, another useful approach to directly adjust the composition of SiN film by varying precursor gas flow rate and deposition temperature is explored. Our results indicate that it is indeed possible to alleviate the dramatic aggravation of device reliability without compromising the device performance caused by the channel strain.

3.2 Devices Fabrication

The NMOSFETs characterized in this study were fabricated on 6-inch p-type (100) Si wafers with conventional local oxidation of silicon (LOCOS) isolation. The 3 nm-thick thermal oxide was grown in a vertical furnace, followed by the deposition of a 150nm-thick polycrystalline-silicon (poly-Si) layer to serve as the gate electrode. After S/D doping and self-aligned spacers formation steps, rapid thermal anneal (RTA) was then carried out in a nitrogen ambient at 900°C for 30 sec to activate dopants in the gate and S/D junctions. Afterwards, a 300nm-thick SiN capping layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) system. The schematic structure of the fabricated device was shown in Fig. 3.1. In this work, we evaluated devices with five different types of SiN film using $SiH_4/NH_3/N_2$ gas mixtures at either 300°C or 400°C (denoted as SiN-1, SiN-2, SiN-3, SiN-1(400°C), and SiN-3(400°C) splits, respectively). The detailed gas flow rates are listed in Table 3-I, and the major parameter adjusted was the N_2 gas flow rate. Deposition pressure and rf power were fixed at 1 Torr and 100W, respectively. In addition to SiN-capped samples, the control devices with 300nm-thick PECVD oxide were also fabricated for comparison purpose (denoted as SiO_2 split).

On the other hand, the PMOSFETs were also fabricated on 6-inch n-type (100) Si wafers with LOCOS isolation, and have 3nm-thick gate oxide and 150nm-thick poly-Si gate electrode. After standard procedures to form TEOS spacers, S/D junction, and RTA anneal, the devices were capped with a 300 nm-thick PECVD oxide, SiN-1 film, and SiN-3 film (as described in Table 3-I), denoted as p_SiO_2, p_SiN-1, and p_SiN-3 splits, respectively. After contact hole and metallization processes, the processing steps were completed with a forming gas anneal at 400°C. Electrical characteristics were performed using an Agilent 4156 system. The interface traps were evaluated using the

charge pumping method with a fixed amplitude of 1.5V at 1 MHz.

3.3 Results and Discussion

3.3-1 Material Analysis

X-ray photoelectron spectroscopy (XPS) and Fourier transform infrared spectrometer (FTIR) were employed to investigate the material properties of the deposited SiN films. Major results are given in Fig. 3.2 and Fig. 3.3, respectively. From XPS analysis, as shown in Fig. 3.2(a), we confirmed that the SiN-3 split contains higher N content than the other samples. Obviously the use of higher N_2 flow rate in the deposition process is responsible for the finding. When the deposition temperature is raised to 400°C, as shown in Fig. 3.2(b), we can see that the SiN-1(400°C) and SiN-3(400°C) samples depict similar trend with the SiN-1 and SiN-3 splits, respectively, implying that N content in the SiN film does not seem to be affected by the temperature of 400°C. In addition, Figure 3.3 shows the analysis of FTIR measurement. It can be seen that the SiN-1 split contains the largest amount of Si-H bonds among all splits, while increase in N_2 flow rate (shown in SiN-3 split) [14] and deposition temperature (shown in SiN-1(400°C) and SiN-3(400°C) splits) [15] tend to weaken the signal of Si-H bonds. Later we will show that this finding is important for robusting the immunity of devices to hot-carrier and NBTI degradations.

Besides, mechanical stress was also investigated in this work. The stress measurements were performed on a Tencor FLX-2320 system. This system evaluates the stress by measuring the change in curvature of the silicon substrate before and after deposition of a blanket SiN layer with a thickness of 300 nm. We confirmed that the stress is tensile in nature with the magnitude of around 127, 344, 556, 96, and 576 MPa for SiN-1, SiN-2, SiN-3, SiN-1(400°C), and SiN-3(400°C) splits, respectively, as listed

in Table 3-I. It can be seen that the tensile stress increases with increasing N_2 flow rate, as shown in Fig. 3.4, while it is only mildly affected by the two deposition temperatures studied in this work.

3.3-2 Devices Characteristics for NMOSFETs

Next, the electrical characteristics were performed using an Agilent 4156 system. Figure 3.5 compares transconductance (Gm) enhancement for all splits with channel width/length (W/L) = 10/0.4 μm. It can be seen that SiN-3 and SiN-3(400°C) splits depict the largest and identical Gm among all samples, while the SiN-1 and SiN-1(400°C) splits show comparable Gm with the SiO_2 split, and the SiN-2 split falls between these two groups. Similar enhancement trend in drive current is also observed, as shown in Fig. 3.6. These electrical results are consistent with the results of film stress measurement listed in Table 3-I. Figure 3.7 shows the Gm_{max} as a function of tensile stress with W/L = 10/0.4 μm for all SiN-capping samples. Gm_{max} increases with increasing tensile stress, and a linear dependence is observed in this figure.

Figure 3.8 shows the percentage increase of Gm for all SiN-capping samples, compared with the SiO_2 controls, as a function of channel length. Each datum point represents the mean measurement result performed on six devices. We can see that SiN-3 and SiN-3(400°C) splits depict similar and the largest Gm enhancement ratio, and the enhancement up to 16% at a channel length of 0.4 μm is observed. It is noted that Gm enhancement ratio increases with decreasing channel length, a unique feature associated with the uniaxial strain induced by SiN capping [16]. The capacitance-voltage (*C*-*V*) characteristics of these samples are shown in Fig. 3.9. It can be observed that the *C*-*V* curves coincide altogether, indicating that the above-mentioned results are not caused by oxide thickness difference.

The subthreshold characteristics and extracted subthreshold swing are shown in Fig. 3.10 and Fig. 3.11, respectively. We can see that the subthreshold swing of all SiN-capping splits depicts similar value and is slightly lower than that of SiO_2 control. Subthreshold swing of an MOSFET at room temperature can be expressed as [17]

$$S.S. = 60[1 + \frac{C_d + C_{it}}{C_{ox}}] \ (mV/dec) \tag{3.1}$$

where C_{ox} is the gate capacitance, C_d is the depletion capacitance, and C_{it} is interface state capacitance. The PECVD SiN film contains a large amount of hydrogen due to the use of hydrogen-containing precursors (SiH_4 and NH_3) [14,18]. These hydrogen species may diffuse into the SiO_2/Si interface and passivate the dangling bonds, resulting in a decrease in C_{it} [14,19] and a reduction in S.S.

3.3-3 Hot-Carrier Stress for NMOSFETs

Next, we turn our attention to the hot-carrier characteristics. Devices with W/L = 10/0.5 μm were stressed at V_{DS} = 4.6 V and V_G at maximum substrate current. Threshold voltage shift (ΔV_{th}) as a function of stress time for all splits is shown in Fig. 3.12. ΔV_{th} is defined as $V_{th}(t) - V_{th}(0)$ for transistors with W/L = 10/0.5 μm. It can be seen that SiN-1 split depicts the worst degradation in terms of the largest ΔV_{th}, while SiN-1(400°C) split apparently fares better, although both depict similar stress level to the control devices. By contrast, SiN-3 and SiN-3(400°C) splits show much improvement in the immunity to hot-carrier damage as compared with the other SiN samples. Note that the difference between SiN-3 and SiN-3(400°C) is much smaller than that between SiN-1 and SiN-2. Since the SiN-3 split has the least hydrogen content, this implies that the effect of deposition temperature becomes weaker as the SiN contains less hydrogen. Figure 3.13 shows the difference of charge pumping current before and after 1000 sec hot-carrier stress among all splits. After hot-carrier stress, we

can see that more interface states are generated for SiN-1 split, while SiN-3(400°C) split fares better in this aspect. The trend of interface state generation is consistent with that of above-mentioned threshold voltage shift.

From the FTIR results, we suspect that the amount of Si-H bonds contained in the SiN film is mainly responsible for the hot-carrier immunity of the SiN samples. Note that the nominal Si-H bonds have bond strength (314 kJ/mole) much weaker than N-H bonds (389 kJ/mole) [20-21]. It is thus reasonable to assume that the hydrogen pertaining to the former bonds is much easier to dissociate and release from the SiN film. As a consequence, the high amount of Si-H bonds in the SiN-1 split (Fig. 3.3) would release extra H species to the device and form new Si-H bonds at the Si/channel interface [14,19]. The breaking of Si-H bonds at the Si/channel interface during stressing is believed to be one of the major root causes responsible for the hot-carrier degradation [9-11,22]. These passivated Si-H bonds act as precursors to hot-carrier degradation [23-24] and are more easily broken during subsequent stressing [22]. Therefore, SiN film containing abundant hydrogen species would depict aggravated hot-carrier reliability. Since SiN-1 film contains the highest amount of Si-H bonds, the worsening of hot-carrier reliability occurs indeed most dramatically in the SiN-1 split, even though its strain level is not high. Increase in both N_2 flow rate [14] and deposition temperature [15] could reduce the amount of Si-H bonds, as evidenced in FTIR analysis. Therefore, SiN-3(400°C) shows the best hot-carrier reliability among all SiN-capping samples, even though its stress level and the resultant device performance enhancement are the highest (Figs. 3.5~3.8). However, the difference between SiN-3(400°C) and SiN-3 is small. This indicates that, as the amount of Si-H bonds contained in the SiN layer is reduced, the deposition temperature plays a less important role in affecting the device performance as well as the hot-carrier degradation.

Channel strain engineering using highly tensile SiN capping has been popularly applied to modern technology to enhance the driving current of NMOS. Based on the results presented in this thesis, the N content and the Si-H bonds contained in the capping layer must be carefully controlled. Special attention should be paid to the NMOS devices in the input/output (I/O) regions which have more concerns on hot-carrier reliability, since they typically are subjecting to a working voltage higher than the core device.

The lateral distribution of interface states ($N_{it}(x)$) after hot-carrier stress was also investigated by the method cited in Ref. 25. $N_{it}(x)$ can be expressed as

$$N_{it}(x) = \frac{d\Delta I_{cp}}{dx} \frac{1}{q f W} \tag{3.2}$$

where f is the gate pulse frequency, W is the channel length, x represents the distance from the gate edge on the drain side, and ΔIcp is the incremental charge pumping current, as shown in Fig. 3.14 after 200 sec hot-carrier stress for the control samples. According to the equation, the derived lateral distribution of the interface states for all splits of devices is extracted, and the results are shown in Fig. 3.15. From this figure, we can see that the major damage region is confined within 0.1 μm near the drain edge. This is reasonable since the hot-carrier stress is known to induce localized damage. In addition, the damage trends are consistent with the above-mentioned results.

3.3-4 Impacts of Performance and NBTI reliability on PMOSFETs

In this section, PMOSFETs were fabricated and characterized to investigate the effects of SiN-1 and SiN-3 capping on the device performance and NBTI reliability. Devices with PECVD SiO_2 capping were also fabricated for comparison purpose. Figure 3.16 compares the transconductance data for these three splits with W/L = 10/0.6 μm. It can be seen that the transconductance is degraded by SiN-1 and SiN-3 capping,

especially for SiN-3 capping samples, since SiN-3 film has the highest tensile stress, described in Table 3-I. In addition, the filed-effect mobility (μ_{FE}) can be derived by the equation:

$$\mu_{FE} = \frac{LG_m}{WC_{ox}V_D} \tag{3.3}$$

The extracted maximum filed-effect mobility for these three splits is shown in Fig. 3.17. Each datum point represents the mean measurement results performed on four devices. We can see that increasing tensile stress in the channel direction degrades PMOSFETs but benefits NMOSFETs performance. Therefore, tensile stress in the channel direction is a trade-off for N and PMOSFETs. *C-V* characteristics for these three splits are shown in Fig. 3.18. These *C-V* curves also coincide altogether, indicating the performance degradation is not caused by the oxide thickness difference.

Next, we will discuss the NBTI characteristics. It is known that hydrogen plays a major role during the NBTI stressing. Although hydrogen can passivate Si dangling bonds resulting in less interface state generation, the breaking of Si-H bonds during the stressing would greatly contribute to the NBTI degradation [26-27]. Therefore, abundant hydrogen species generated during the SiN deposition process, owing to the use of hydrogen-containing precursors, would cause NBTI degradation [9,28]. The setup of NBTI measurement is shown in Fig. 3.19. The source, drain, and substrate are all grounded, with gate bias of V_G-V_{th} = -3.3 V at temperature of 125°C. The results for the three PMOSFET splits after 1000 sec NBTI stress are shown in Fig. 2.20. We can see that the p_SiN-1 split depicts the worst NBTI degradation in terms of the largest threshold voltage shift, while the degradation of p_SiN-3 split is mitigated and becomes comparable to that of the SiO_2 control. The threshold voltage shift shows a power law dependence on time ($\Delta V_{th}=A \cdot t^n$), and the values of the exponent (n) are around 0.26 (likely 1/4), which could be explained by the diffusion-controlled electrochemical

reaction model proposed by Jeppson and Svensson [29]. In addition, the trend of NBTI degradation is consistent with that of the above-mentioned hot-carrier degradation. From these results, we can again confirm that SiN-3 film deposited with larger N_2 flow rate could have weaken Si-H bonds, and resulting in better hot-carrier and NBTI reliability, even though it has higher stress level.

3.4 Summary

In this chapter, we have fabricated strained n- and p-channel MOSFETs with different types of SiN capping by varying the N_2 flow rate and deposition temperature during the deposition step. Tensile stress is found to increase with increasing N_2 flow rate, therefore boosting the NMOS device performance, especially for short-channel devices. However, the tensile stress would degrade PMOS device performance. On the other hand, we found that the immunity for devices to hot-carrier degradation and NBTI reliability is mainly affected by the hydrogen content, rather than the stress level. Therefore, SiN film with high tensile stress but low hydrogen content is ideally suitable for NMOSFETs, and nitrogen-rich film can fulfill the requirement.

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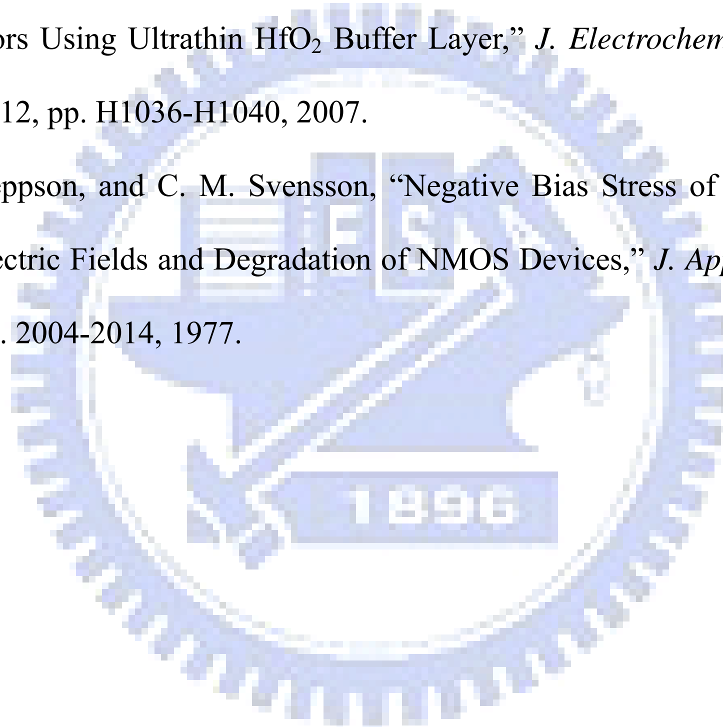

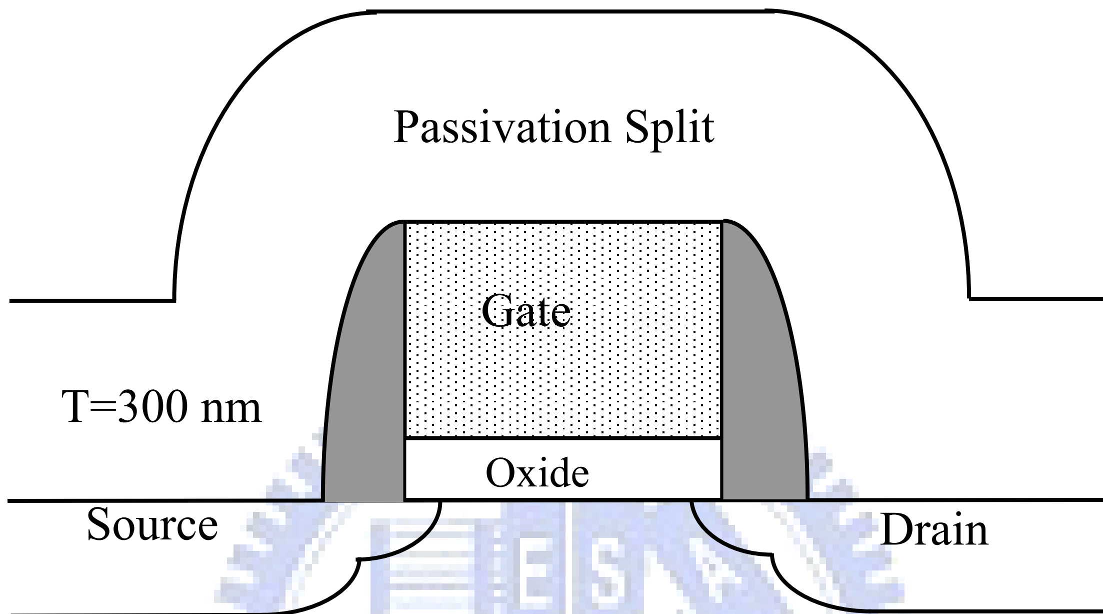

Fig. 3.1 Schematic structure of fabricated devices with different types of passivation. The passivation thickness is fixed at 300 nm.

Table 3-I Precursor flow rates, deposition temperature, and measured tensile stress for SiN film. Deposition pressure and rf power were fixed at 1 Torr and 100W, respectively.

	SiH_4 (sccm)	NH_3 (sccm)	N_2 (sccm)	Temp. (°C)	Stress (MPa)
SiN-1	50	6	50	300	127
SiN-2	50	6	100	300	344
SiN-3	50	6	1000	300	556
SiN-1(400°C)	50	6	50	400	96
SiN-3(400°C)	50	6	1000	400	576

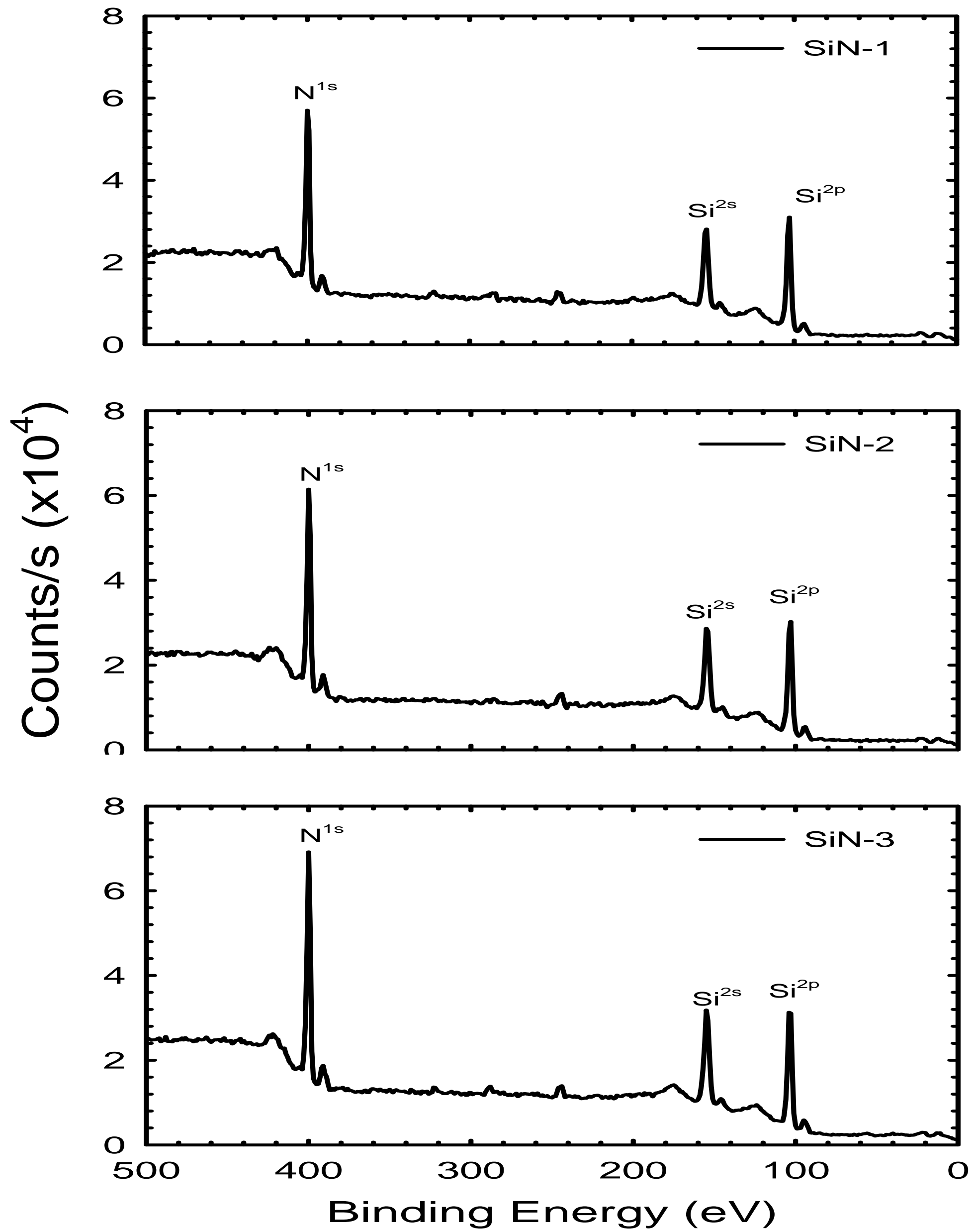

Fig. 3.2(a) Results of XPS analysis for SiN-1, SiN-2, and SiN-3 splits. The SiN-3 split contains the highest N content among all splits, owing to the use of the highest N_2 flow rate in the deposition process.

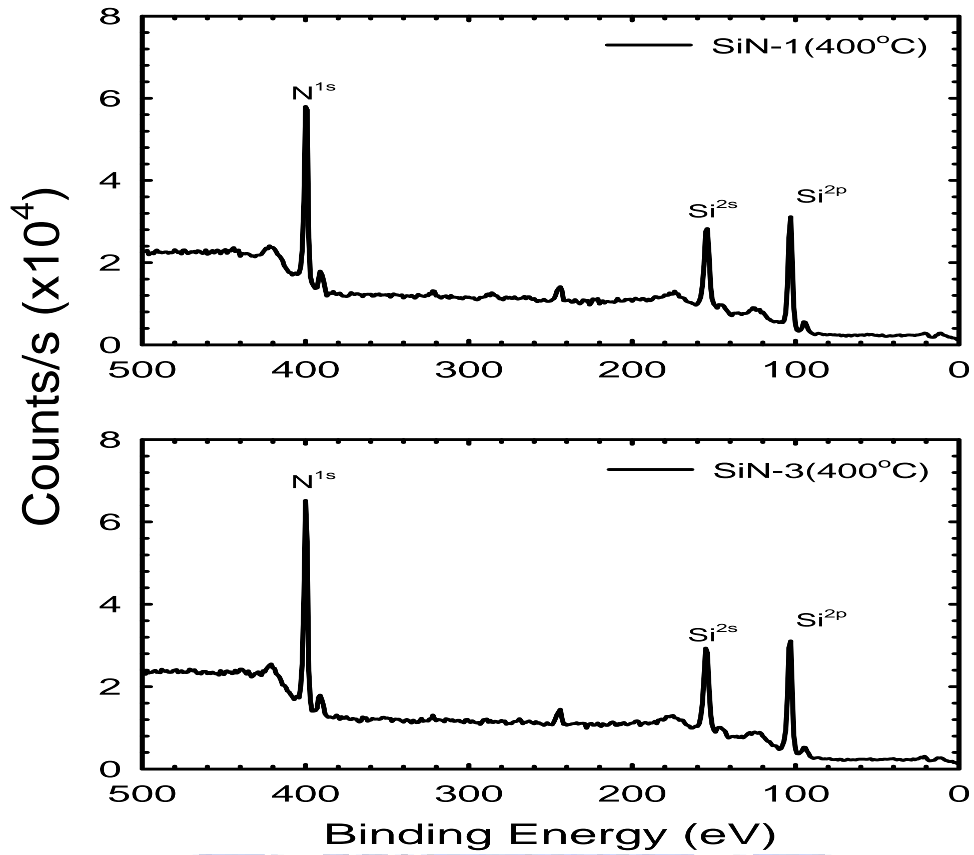

Fig. 3.2(b) Results of XPS analysis for SiN-1(400°C), and SiN-3(400°C) splits. The SiN-1(400°C) and SiN-3(400°C) samples depict similar trend with the SiN-1 and SiN-3 split, respectively, implying that N content in the SiN film does not seem to be affected by the temperature of 400°C.

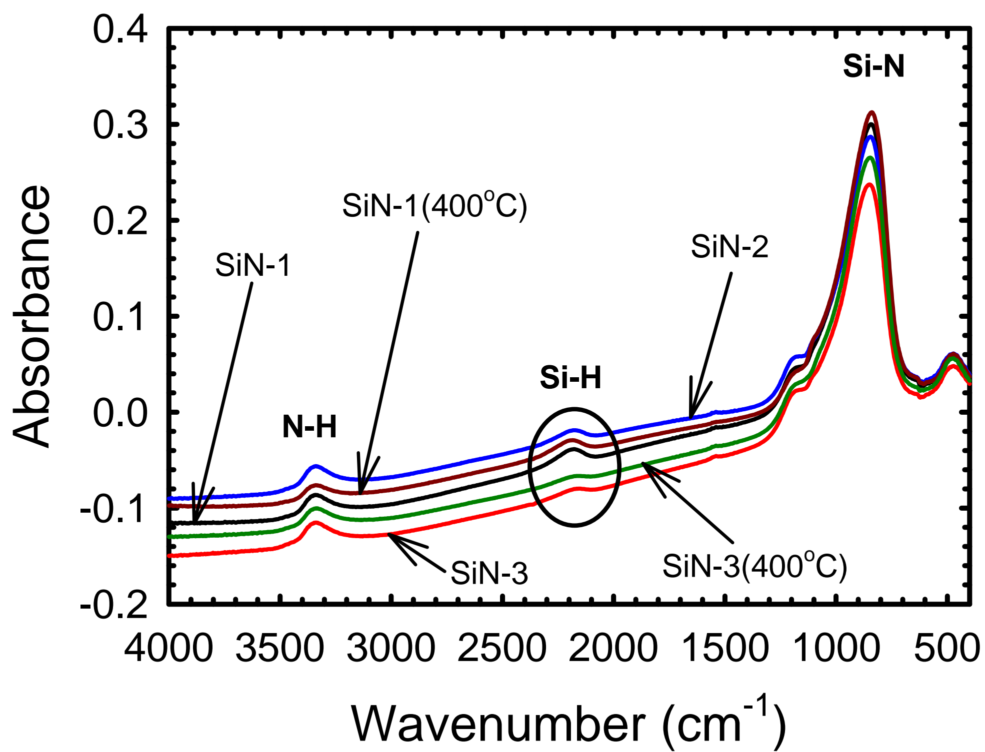

Fig. 3.3 Results of FTIR analysis: SiN-1 sample contains the highest number of Si-H bonds among all splits. Increase in N_2 flow rate and deposition temperature tends to weaken the signal of Si-H bonds.

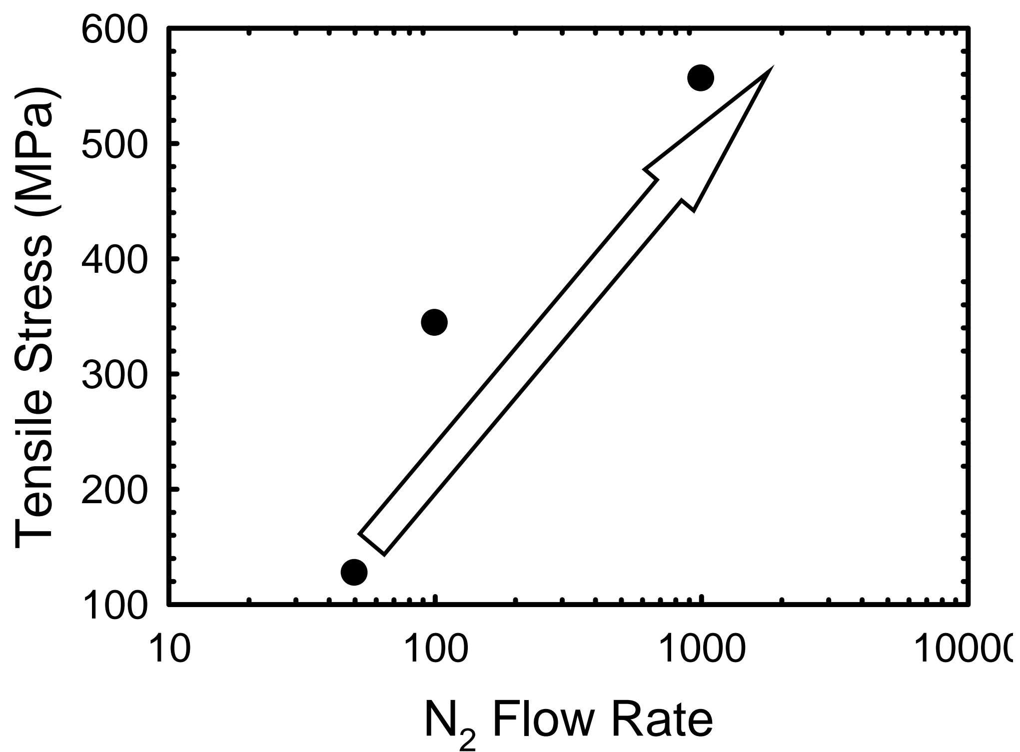

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Fig. 3.4 Tensile stress versus N_2 flow rate. The tensile stress increases with increasing N_2 flow rate.

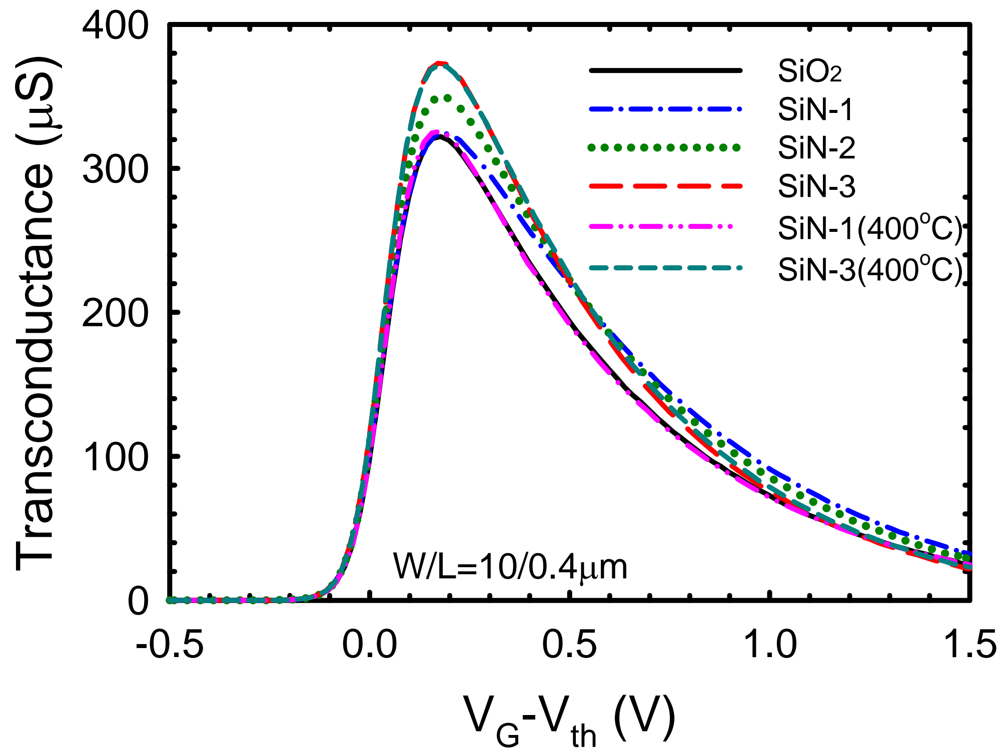

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Fig. 3.5 Transconductance (Gm) versus V_G-V_{th} for all splits with W/L = 10/0.4 μm. The SiN-3 and SiN-3(400°C) splits depict the largest and identical Gm among all splits, owing to the largest tensile stress level.

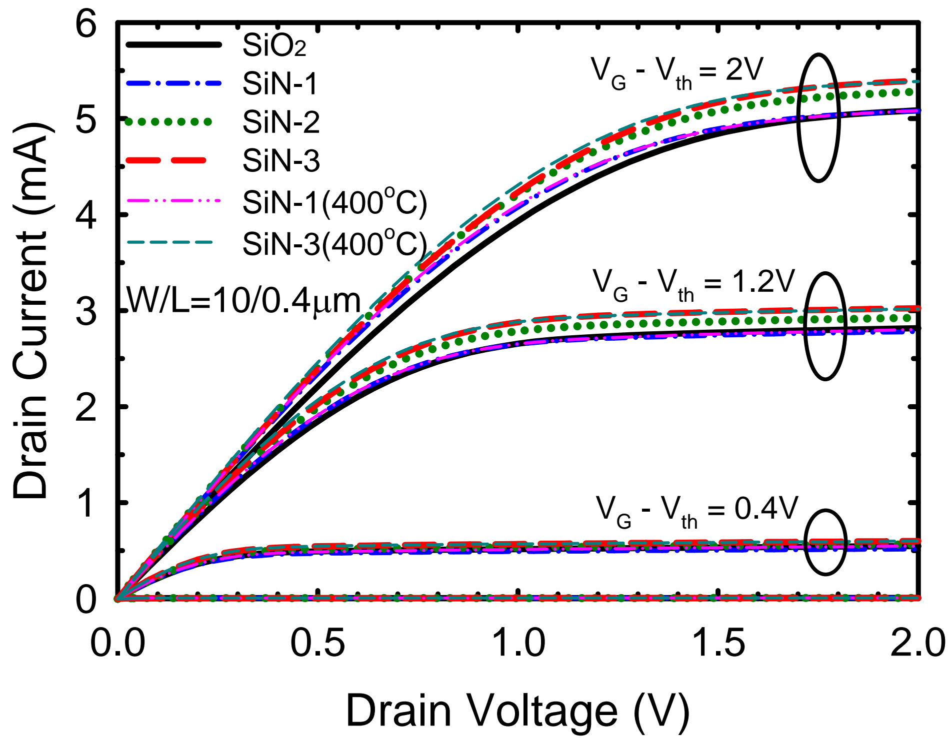

Fig. 3.6 Output characteristics of NMOSFETs for all splits. The enhancement trend in drive current is similar to that of Gm enhancement.

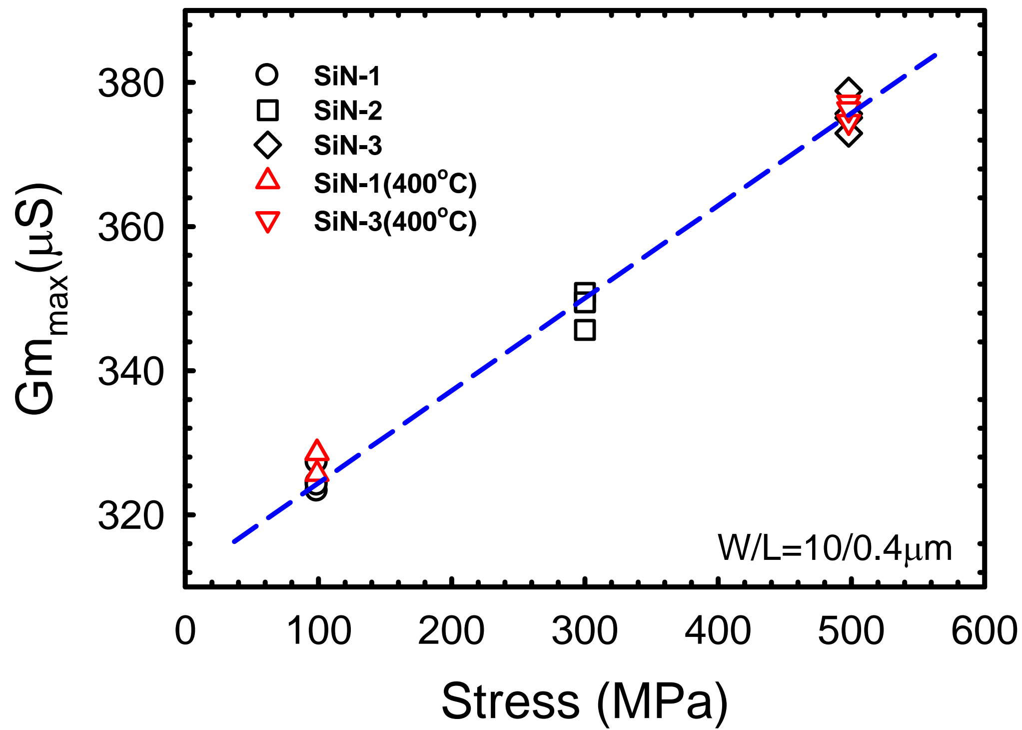

Fig. 3.7 Gm_{max} as a function of tensile stress with W/L = 10/0.4 μm for all SiN-capped splits. Gm_{max} increases with increasing tensile stress and a linear dependence is observed in the figure.

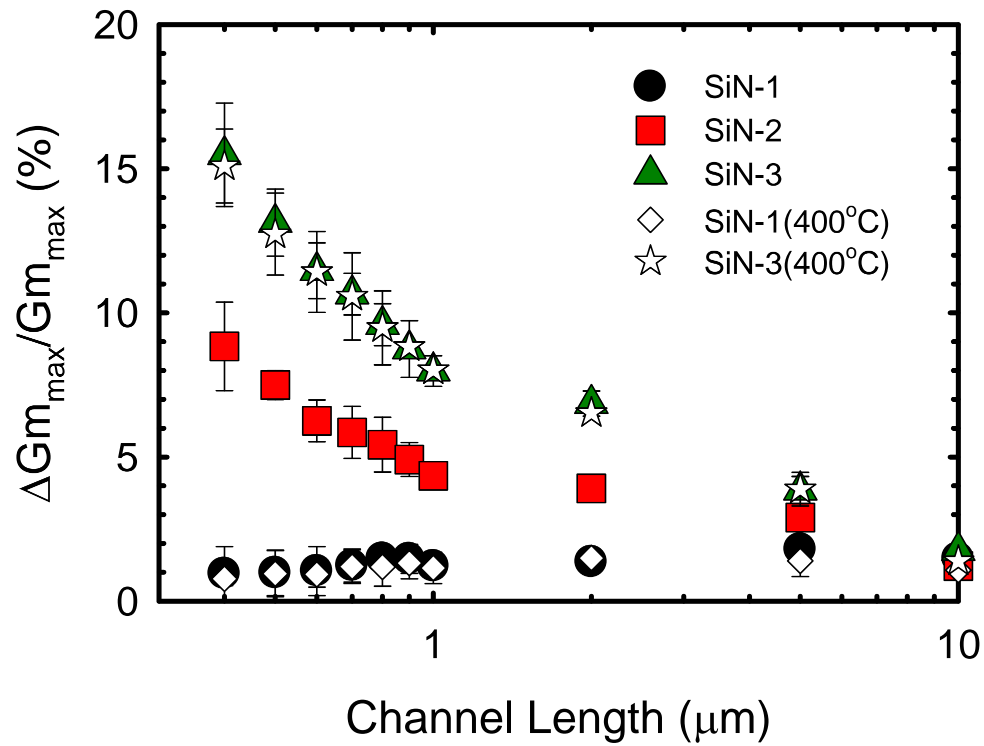

Fig. 3.8 The percentage increase of Gm for all SiN-capping samples, compared with the SiO_2 controls, as a function of channel length. Each datum point represents the mean measurement result performed on six devices.

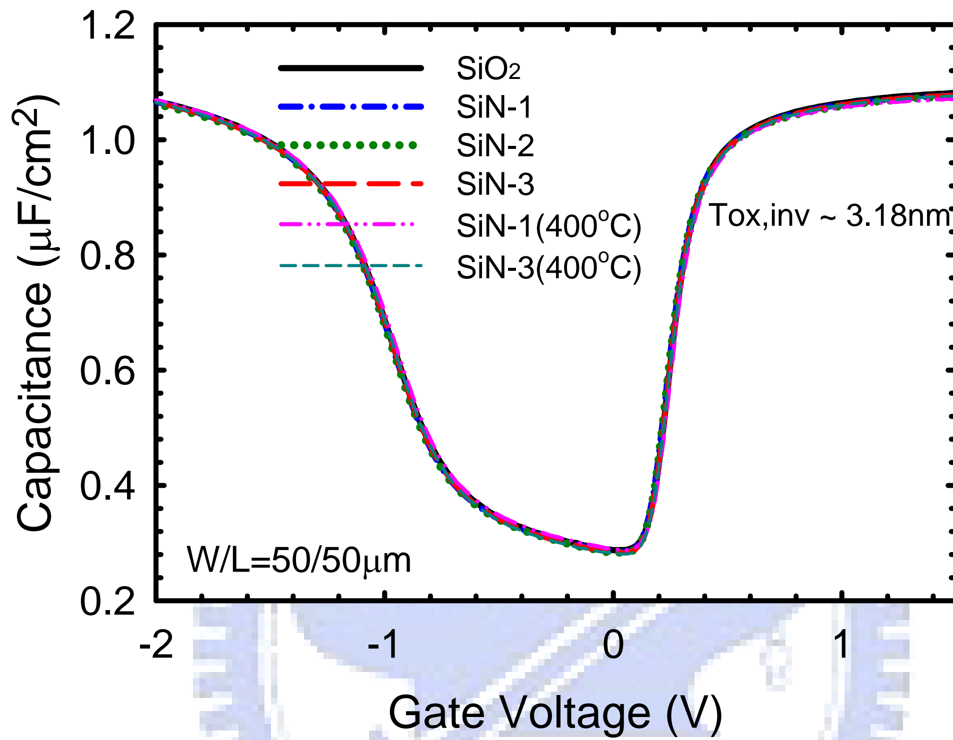

Fig. 3.9 Capacitance-Voltage (*C*-*V*) characteristics for all splits of samples. The *C*-*V* curves coincide altogether, indicating that the above-mentioned results are not caused by oxide thickness difference.

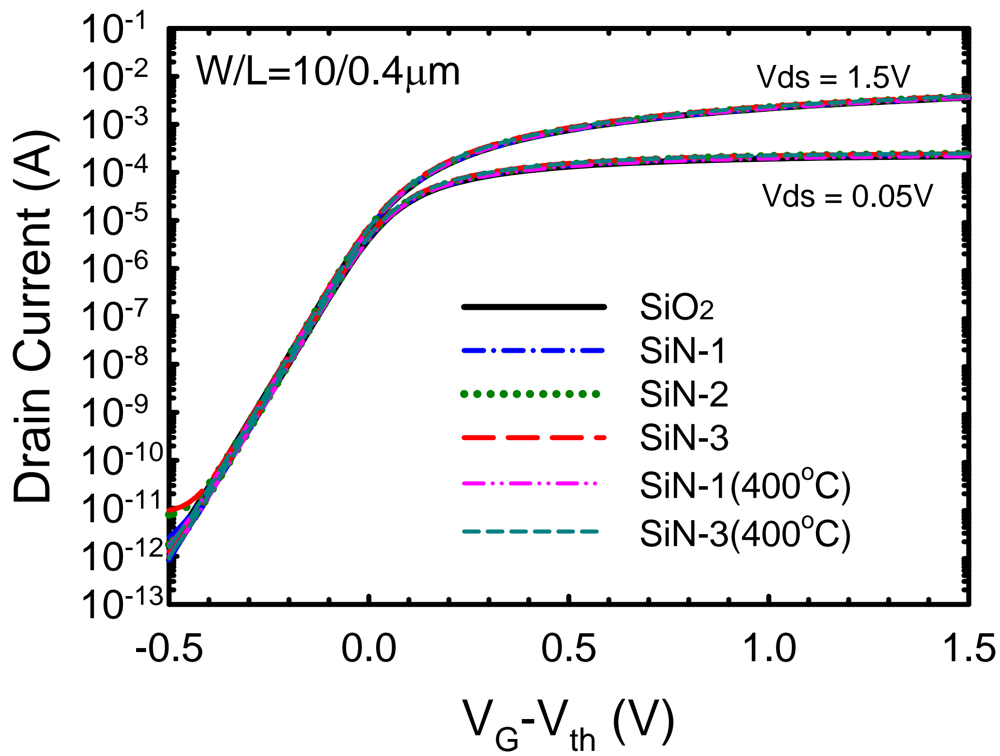

Fig. 3.10 Subthreshold characteristics of NMOSFETs for all splits with W/L = 10/0.4 μm.

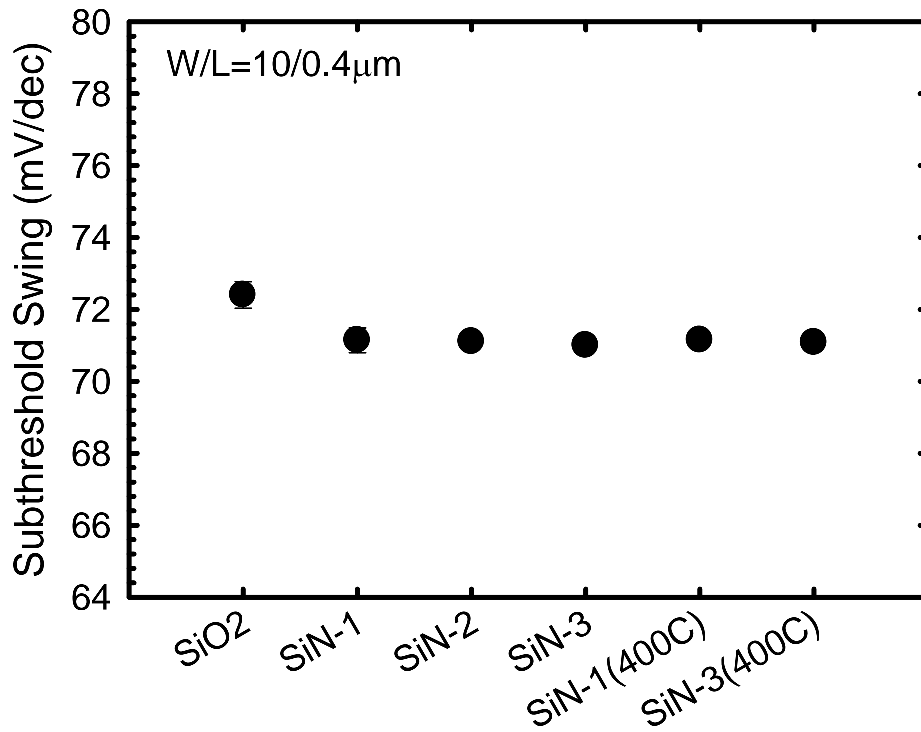

Fig. 3.11 Subthreshold swing of NMOSFETs for all splits with W/L = 10/0.4 μm.

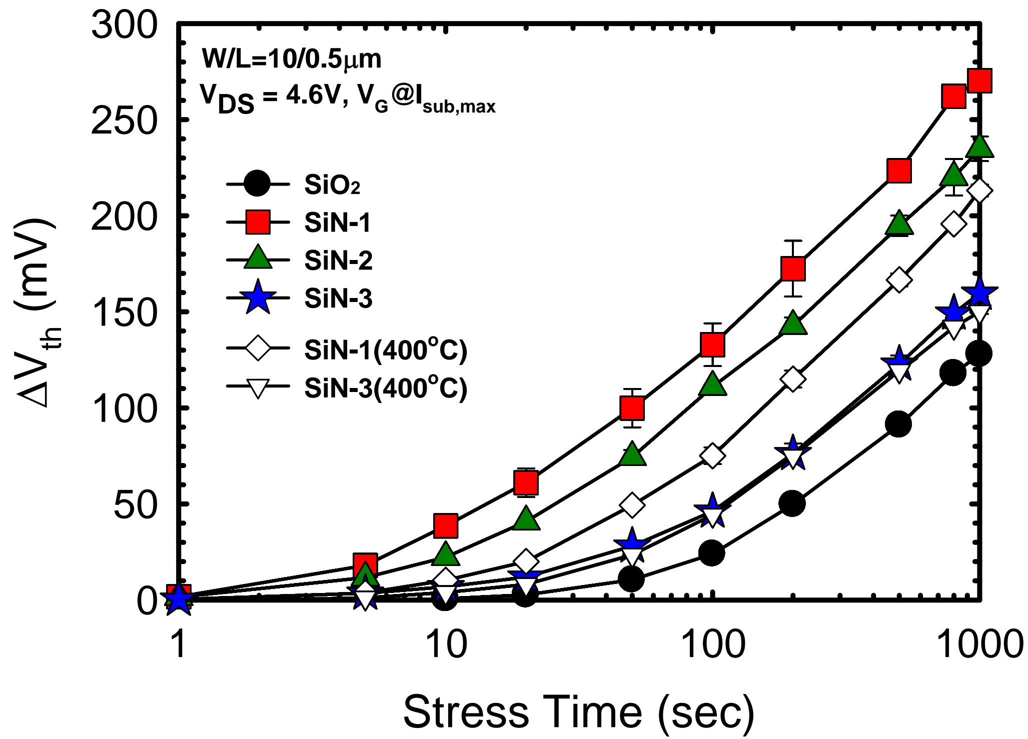

Fig. 3.12 Threshold voltage shift (ΔV_{th}) as a function of stress time for all splits. Devices were stressed at V_{DS} = 4.6 V, and V_G at maximum substrate current. ΔV_{th} is defined as $V_{th}(t) - V_{th}(0)$ for transistors with W/L = 10/0.5 μm.

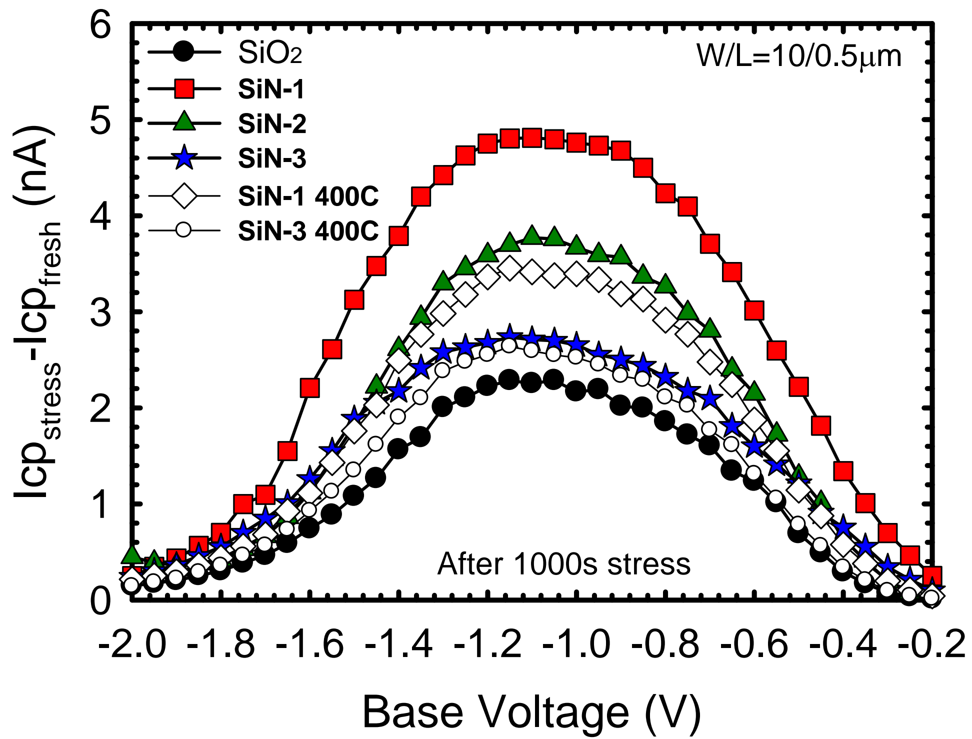

Fig. 3.13 The difference of charge pumping current before and after 1000 sec hot-carrier stress among all splits. The largest amount of interface states are generated for SiN-1 split, while SiN-3(400°C) split fares better in this aspect.

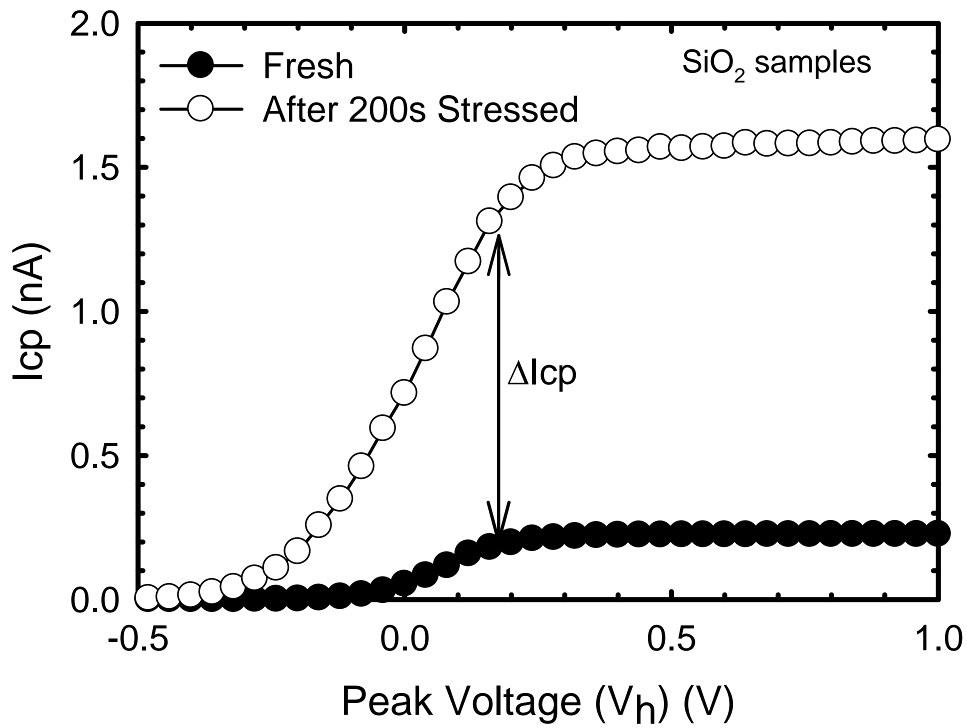

Fig. 3.14 Charge pumping current before and after 200 s hot-carrier stress for a control sample.

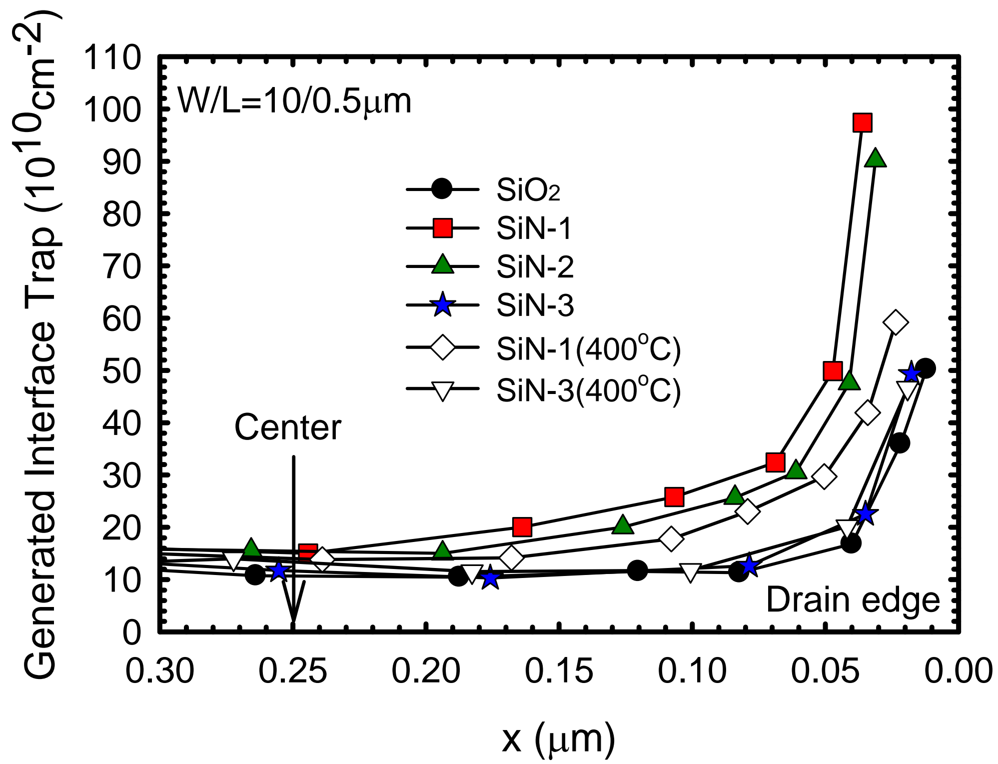

Fig. 3.15 Lateral distribution of interface state generation after hot-carrier stress for all splits. The major damage region is confined within 0.1 μm near the drain edge.

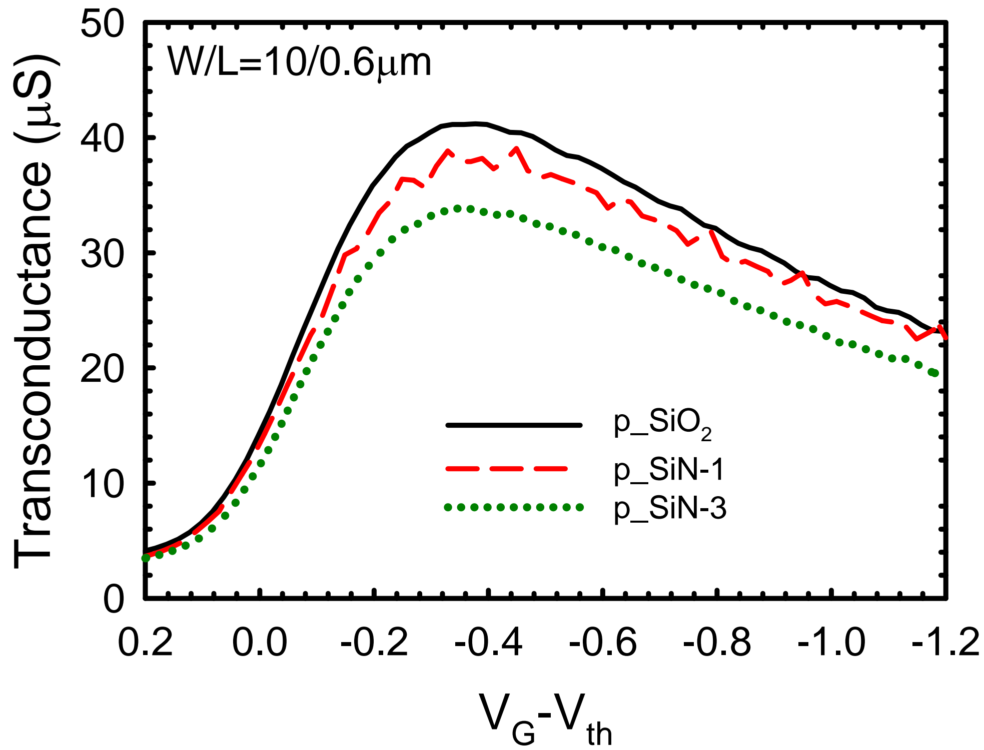

Fig. 3.16 Transconductance versus V_G-V_{th} for the three SiN-capped PMOSFET splits. Transconductance is degraded by SiN-1 and SiN-3 capping layers, especially for SiN-3 capping samples, since SiN-3 film depicts maximum tensile stress.

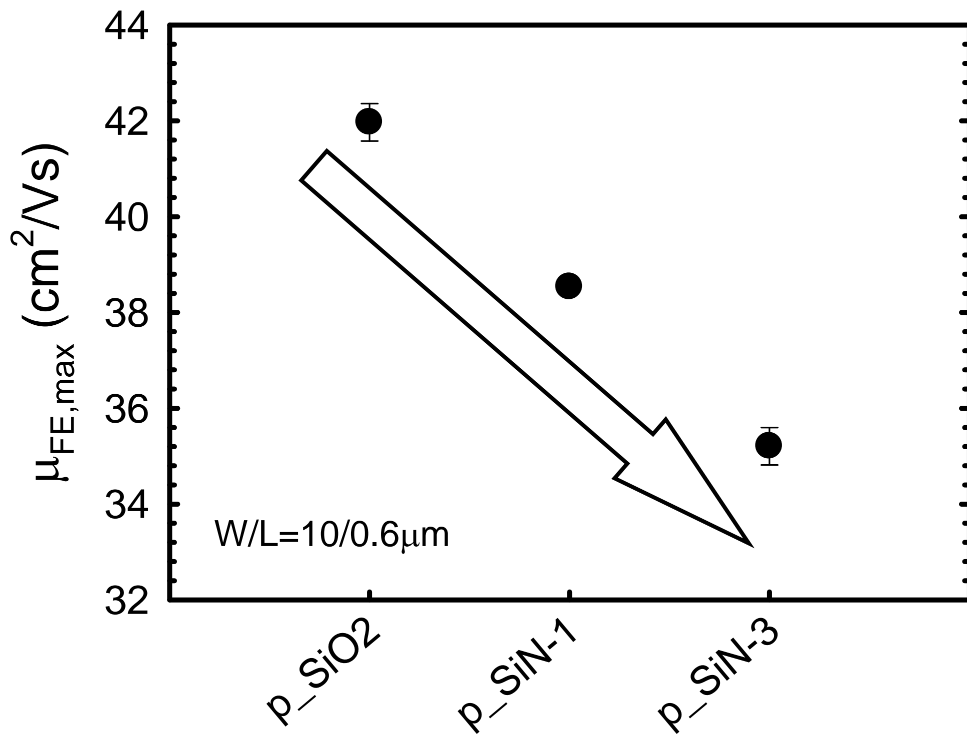

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Fig. 3.17 Maximum filed-effect mobility of PMOSFETs for SiN-1, SiN-3, and the control. Each datum point represents the mean measurement results performed on four devices.

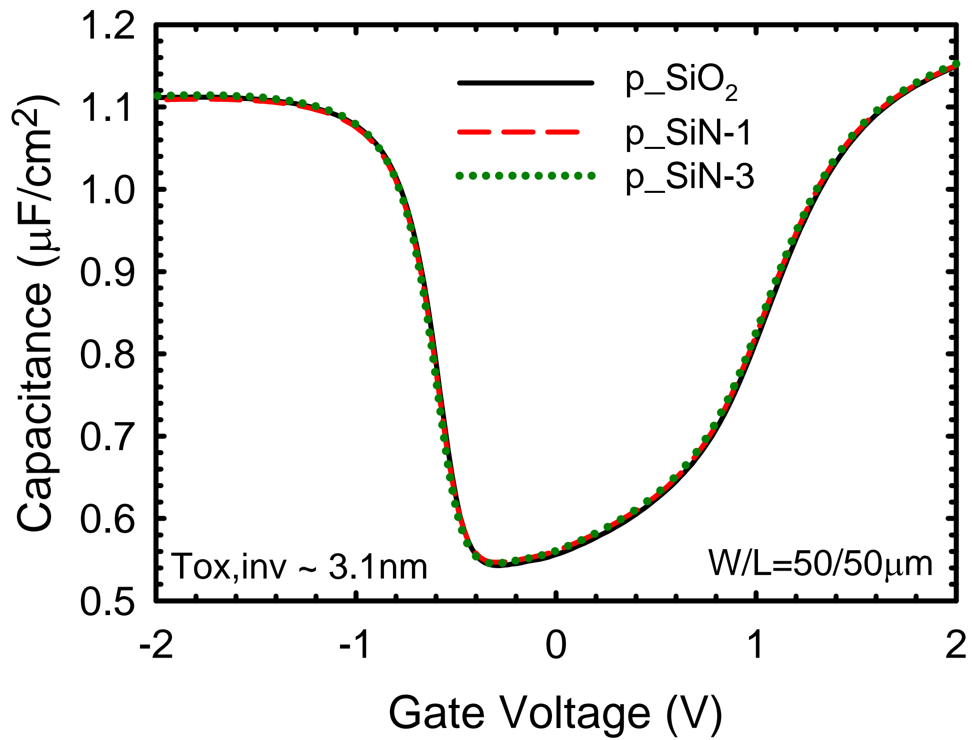

Fig. 3.18 Capacitance-Voltage (*C-V*) characteristics for SiN-1, SiN-3, and the control. These *C-V* curves also coincide altogether, indicating the performance degradation is not caused by the oxide thickness difference.

Stress: $V_G - V_{th}$ = -3.3V

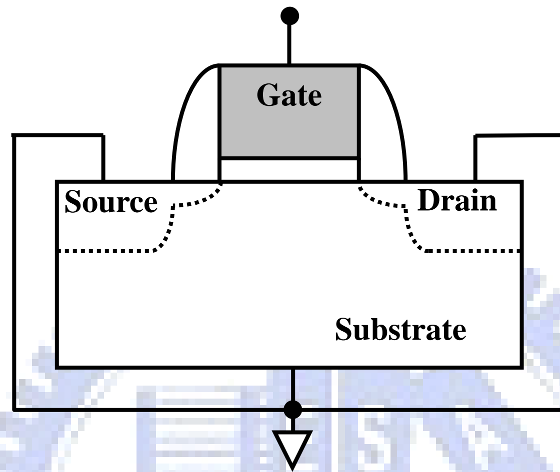

Fig. 3.19 The setup of NBTI measurement with source, drain and substrate grounded and gate bias of V_G-V_{th} = -3.3 V at temperature of 125°C.

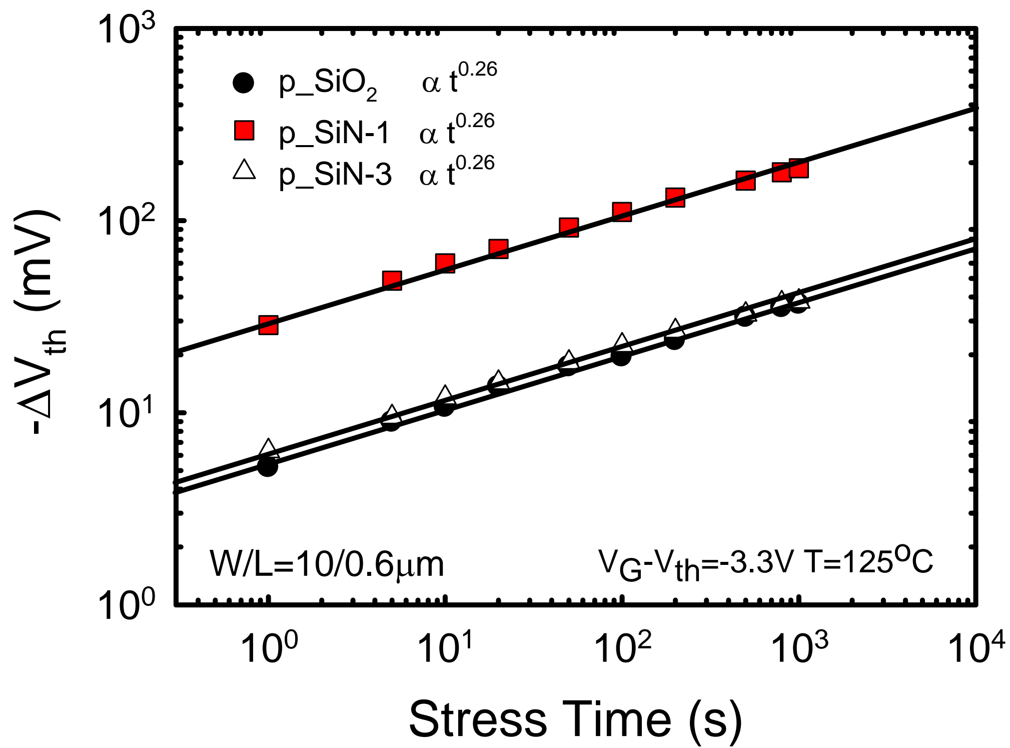

Fig. 3.20 Threshold voltage shift (ΔV_{th}) of PMOSFETs versus stress time for SiN-1, SiN-3, and the control. The NBTI stress was performed with V_G-V_{th} = -3.3 V at temperature of 125°C. The p_SiN-1 split depicts the worst NBTI degradation in terms of the largest threshold voltage shift, while the NBTI degradation in p_SiN-3 split is mitigated and becomes comparable to that of the SiO_2 control.

Chapter 4

Off-State Leakage Current Mechanisms of Strained Channel NMOSFTs with Different SiN Thickness and Its Impacts on the Performance and Hot-Carrier Reliability

4.1 Introduction

Channel-strain engineering has emerged as one of the most effective remedies to boost the drive current in the scaled devices [1-15]. Tensile stress such as embedded SiC source/drain (S/D) [1-2] and highly tensile contact etch-stop layer (CESL) [3-4,11-14] would benefit n-channel metal-oxide-semiconductor field-effect-transistors' (NMOSFETs) performance, while compressive stress such as embedded SiGe S/D [5-8] and highly compresseive CESL layer [7-10] is beneficial for PMOSFETs' mobility enhancement. Among these methods, CESL technique has received much attention because it is easily implemented in modern VLSI technology. However, voluminous hydrogen-related species generated during the SiN deposition process would diffuse into the channel region and aggravate device reliability [9-14]. Recently, the techniques of inserting an ultra-thin buffer layer underneath the SiN capping [10-13] or optimization of SiN film by adjusting the deposition flow rate [14] have been proposed to improve the immunity on reliability degradation without compromising device performance enhancement.

In this work, the strained-channel NMOSFETs were fabricated with different tensile stress by adjusting the SiN thickness. In addition to investigating its impacts on the performance and hot-carrier reliability, we will verify the main source of off-state leakage current and understand the physical mechanisms.

4.2 Devices Fabrication

The NMOSFETs were fabricated on 6-inch p-type (100) Si wafers with resistivity of 15~25Ω-cm. The p-well was formed first by BF_2^+ implantation at 100 Kev and 1×10^{13} cm^{-2}. Next, a standard local oxidation of silicon (LOCOS) process with channel stop implant (by BF_2^+ implantation at 120 keV and 4×10^{13} cm^{-2}) was used for device isolation. Threshold voltage adjustment and anti-punch through implantation were done by implanting 40 keV BF_2^+ and 35 keV B^+, respectively. After the growth of 3nm-thick thermal gate oxide, a 150nm poly-Si layer was deposited by low-pressure chemical vapor deposition (LPCVD) system, followed by gate etch process to pattern the gate. The S/D extension regions were then formed by As^+ implantation at 10 keV and 5×10^{14} cm^{-2}. After a 150 nm oxide spacer formation by high-density plasma chemical vapor deposition (HDPCVD) system, S/D regions were formed by P^+ implantation at 15 keV and 5×10^{15} cm^{-2}. Afterwards, the substrate electrode patterning was performed through lithography and etching processes, and the substrate junction was formed by BF_2^+ implantation at 40 keV and 5×10^{15} cm^{-2}. Rapid thermal anneal (RTA) was then carried out in a nitrogen ambient at 900°C for 30 sec to activate dopants in the gate, S/D, and substrate regions.

Next, most samples were split to receive different SiN stress layer of 0, 200 Å, and 1000 Å by plasma enhanced chemical vapor deposition (PECVD) system. The SiN deposition was performed at 300°C with SiH_4, N_2, and NH_3 as the reaction precursors. The split with oxide capping was also fabricated to serve as the control. Subsequently, an oxide passivation layer was deposited by HDPCVD system. The total passivation layer, including SiN and oxide, was controlled at 3000 Å. The schematic structure is shown in Fig. 4.1, and the split conditions are listed in Table 4-I. After contact holes and

metallization processes, the process steps were completed with a forming gas anneal at 400°C. Electrical characteristics were performed using an Agilent 4156 system. The interface traps were evaluated using the charge pumping method with a fixed amplitude of 1.5 V at 1 MHz.

4.3 Results and Discussion

4.3-1 Device Characteristics

Figure 4.2 compares transconductance (Gm) enhancement with channel width/length (W/L) = 10/0.6 μm for all splits of samples. It can be seen that Gm increases with increasing SiN thickness, confirming that the stress becomes more tensile as the SiN thickness increases [16]. The enhancement reaches about 7% for SiN-1000Å split. The Capacitance-Voltage (*C-V*) characteristics for all splits of samples are shown in Fig. 4.3. All *C-V* curves coincide altogether, indicating that the above-mentioned enhancement is not caused by the oxide thickness difference, and the extracted electrical thickness is about 3.38 nm. Figure 4.4 shows the subthreshold characteristics for all splits. All splits exhibit similar subthreshold slope and the extracted subthreshold swings are shown in Fig. 4.5. They are confined in a narrow range between 76 ~ 77 mV/decade. However, from the off-state leakage region, we can see that the SiN-1000Å split depicts the largest off-state leakage current among the three splits and the leakage current increases with increasing gate bias.

Figure 4.6 shows threshold voltage (V_{th}) roll-off characteristics for all splits of devices. The results are obtained at V_{DS} = 0.05 V. Threshold voltage shift (ΔV_{th}) increases with increasing SiN capping layer thickness. This is mainly ascribed to the bandgap narrowing effect caused by the tensile stress [17-18].

4.3-2 Off-State Leakage Current

Figure 4.7 illustrates various leakage paths in the device with Vd = 1.5 V, Vg = 0 ~ -1 V, and Vs = Vb = 0 V. Basically the leakage paths can be divided into the following categories: drain-to-gate (Ig_off), drain-to-source (Is_off), and drain-to-substrate (Ib_off). These four-terminal leakage currents are individually shown in Figs. 4.8(a) & (b) for the control and SiN-1000Å split, respectively We can see that Ib_off leakage current is comparable to Id_off, while Ig_off and Is_off leakage current depict much smaller values in the regime when the gate voltage is smaller than -0.2 V. Figure 4.9 compares the Ib_off leakage current for all three splits. It can be seen that SiN-1000Å split depicts the largest Ib_off among all splits. The statistical box plot of these off-state current for all splits is shown in Fig. 4.10. These data were measured from seven different die positions with Vd = 1.5 V and Vg = -0.9 V at W/L = 10/0.6 μm. From this figure, we confirmed that the main source of Id_off leakage current comes from Ib_off leakage current and Ib_off leakage current increases with increasing SiN thickness (i.e., increasing tensile stress).

From the strong dependence on Vg exhibited by Ib_off in the negative Vg regime, as shown in Fig. 4.8, gate-induced drain leakage (GIDL) is identified to be responsible for the conduction mechanism. It is well known that GIDL current is attributed to the band-to-band tunneling (BBT) process taking place in the deep-depleted drain region underneath the gate oxide. Electron-hole pairs are generated by the tunneling of valence band electrons into the conduction band and subsequently collected by the drain and substrate separately. The schematic energy band diagram of the gate-drain overlap region is shown in Fig. 4.11. The BBT current (I_{BBT}) could be simplified as [19]

$$I_{BBT} = AE_s \exp(-\frac{B}{E_s}) \qquad (4.1)$$

where A is a constant, E_s and B can be approximated as:

$$E_s = \frac{V_{DG} - 1.2}{3T_{ox}} \tag{4.2}$$

$$B = \frac{4\sqrt{2m^*}}{3q\hbar}\sqrt[3]{E_g} \tag{4.3}$$

where $\hbar$ is Plank's constant divided by 2π, m^* is the effective mass, and Eg is the energy bandgap. From these equations, it should be noted that BBT current is dependent on Eg. Therefore, if Eg decreases, the band-to-band tunneling current (I_{BBT}) increases.

Previous literatures have pointed out that tensile stress would result in bandgap narrowing [17-18]. Therefore, the BBT current would be increased by tensile stress. This accounts for Ib_off leakage current increase with increasing tensile stress. Besides, the bandgap narrowing phenomenon could be also evidenced from the threshold voltage shift, as shown in Fig. 4.4 and Fig. 4.6, in which the SiN-1000Å split depicts the lowest threshold voltage because it has the largest tensile stress among all splits. In short, the main source of off-state leakage current in these SiN-capped NMOSFETs comes from the GIDL current. Tensile stress induces bandgap narrowing and, in turn, increases the GIDL current, resulting in off-state leakage current increase.

4.3-3 Hot-Carrier Stress

Although the device performance is improved by applying channel strain induced by the SiN-capping layer, however, these devices could encounter aggravated hot-carrier degradation. Figure 4.12 shows the substrate current (I_{sub}) versus gate voltage for all splits of devices with W/L = 10/0.5 μm at V_{DS} = 4.5 V. It can be seen that the substrate current increases with increasing SiN thickness. This result indicates clearly that channel strain affects the generation of channel hot electrons. This could be related to the bandgap narrowing effect induced by the tensile strain as well as the increased mobility; both tend to increase the impact ionization rate. Therefore, as the

SiN capping layer becomes thicker, larger substrate current is observed.

Based on the I_{sub} measurements, typical results of hot-carrier stress for all spits of devices are shown in Fig. 4.13. The devices were stressed at V_{DS} = 4.5 V with V_G at a maximum I_{sub}. The I_D-V_G characteristics at V_{DS} = 0.05 V were measured before and after 5000 sec stress to observe the degradation caused by hot-carrier. As can be seen in Fig. 4.13, the threshold voltage, subthreshold swing, and transconductance aggravate with increasing SiN thickness. In order to understand the evolution of degradation, threshold voltage shift under hot-carrier stress as a function of stress time for all splits of devices is shown in Fig. 4.14. The SiN-1000Å split depicts the worst degradation in terms of the largest threshold voltage shift. The increased electron mobility and abundant hydrogen species incorporated during the SiN deposition process are the two primary factors for the aggravated hot-carrier degradation. Since the PECVD SiN deposition employs hydrogen-containing precursors, e.g., SiH_4 and NH_3, voluminous hydrogen contained in the deposited films is expected. This could be confirmed by the Fourier transform infrared spectrometer (FTIR) measurements and the results are shown in Fig. 4.15. Obviously, the extra Si-H bonding signals are observed, implying that SiN film indeed has a higher hydrogen content. These hydrogen species may diffuse into the channel region, causing the aggravated reliability [20]. The thicker SiN capping not only has larger mobility but also needs longer deposition time, and therefore the SiN-1000Å split depicts the worse hot-carrier reliability. The difference of charge pumping current before and after 5000 sec hot-carrier stress for all splits of samples is shown in Fig. 4.16. The results also indicate that more interface states would be generated during the hot-carrier stress for the SiN-1000Å split.

In addition, the lateral distribution of interface states ($N_{it}(x)$) after hot-carrier stress was also investigated by the method cited in Ref. 21. $N_{it}(x)$ can be expressed as

$$N_{it}(x) = \frac{d\Delta I_{cp}}{dx} \frac{1}{q\,f\,W} \tag{4.4}$$

where f is the gate pulse frequency, W is the channel length, x represents the distance from the gate edge on the drain side, and ΔI_{cp} is the incremental charge pumping current. According to the equation, the derived lateral distribution of the interface states for all splits of devices is extracted, and the results are shown in Fig. 4.17. From this figure, we can confirm that the hot-carrier degradation is highly localized and the major damage region is confined within 0.1 μm near the drain edge.

4.4 Summary

In this thesis, we have fabricated strained-channel NMOSFETs with different tensile stress by adjusting the SiN thickness. Tensile stress is found to increase by increasing the SiN thickness, and thus enhancing the device performance, especially for short-channel devices. However, the off-state leakage current is also increased by the tensile stress. We demonstrate that GIDL current is the major reason for increased off-state leakage current. Bandgap narrowing induced by tensile stress would enhance the band-to-band tunneling process, thus resulting in GIDL current increase. On the other hand, the hot-carrier reliability is also degraded owing to the increase in mobility and the use of hydrogen-containing precursors during the SiN deposition. How to deposit highly tensile SiN film but with low hydrogen content is therefore essential to the implementation of uniaxial channel strain in MOS devices.

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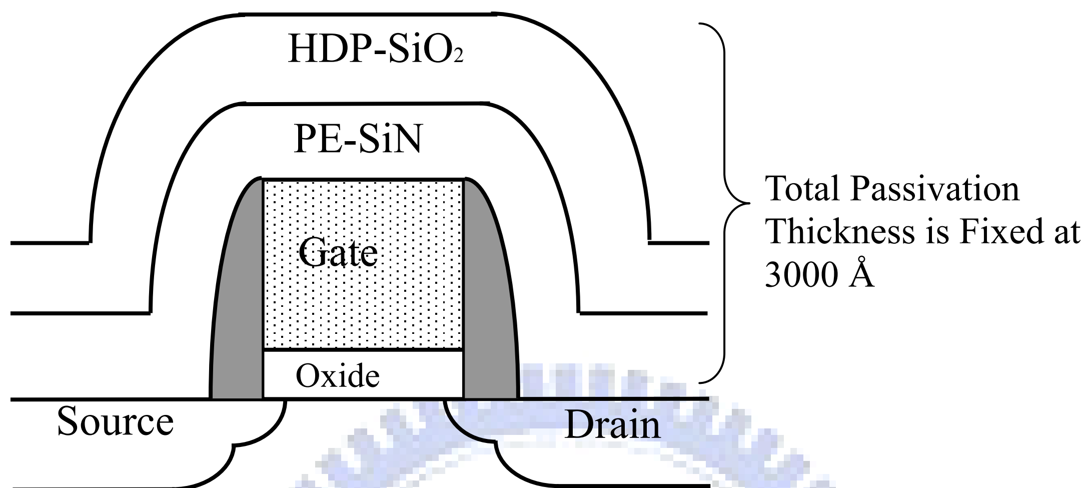
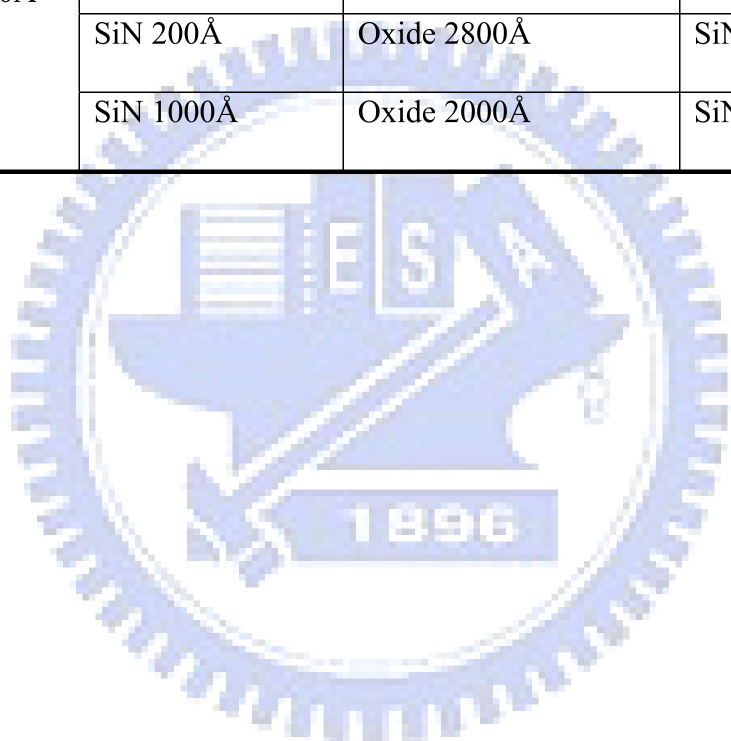


Fig. 4.1 The schematic structure of fabricated devices with different types of passivation. The total passivation thickness, including SiN and SiO_2, is fixed at 3000 Å.

Table 4-I Split conditions for all samples, denoted as control, SiN-200Å, and SiN-1000Å, respectively.

Gate		SiN Stress layer	Oxide Passivation layer	Denoted
Oxide 30Å	poly-Si 1500Å	SiN 0Å	Oxide 3000Å	Control
		SiN 200Å	Oxide 2800Å	SiN-200Å
		SiN 1000Å	Oxide 2000Å	SiN-1000Å



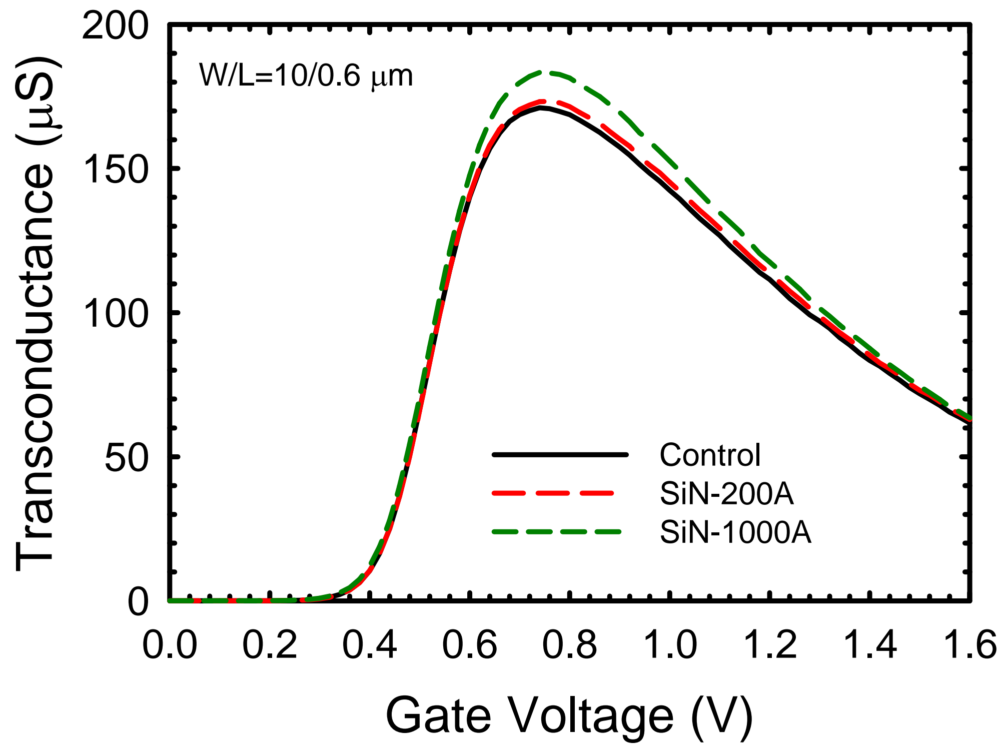


Fig. 4.2 Transconductance (Gm) enhancement with W/L = 10/0.6 μm for all splits of samples. Gm increases with increasing SiN thickness, confirming that the stress becomes more tensile as the SiN thickness increases.

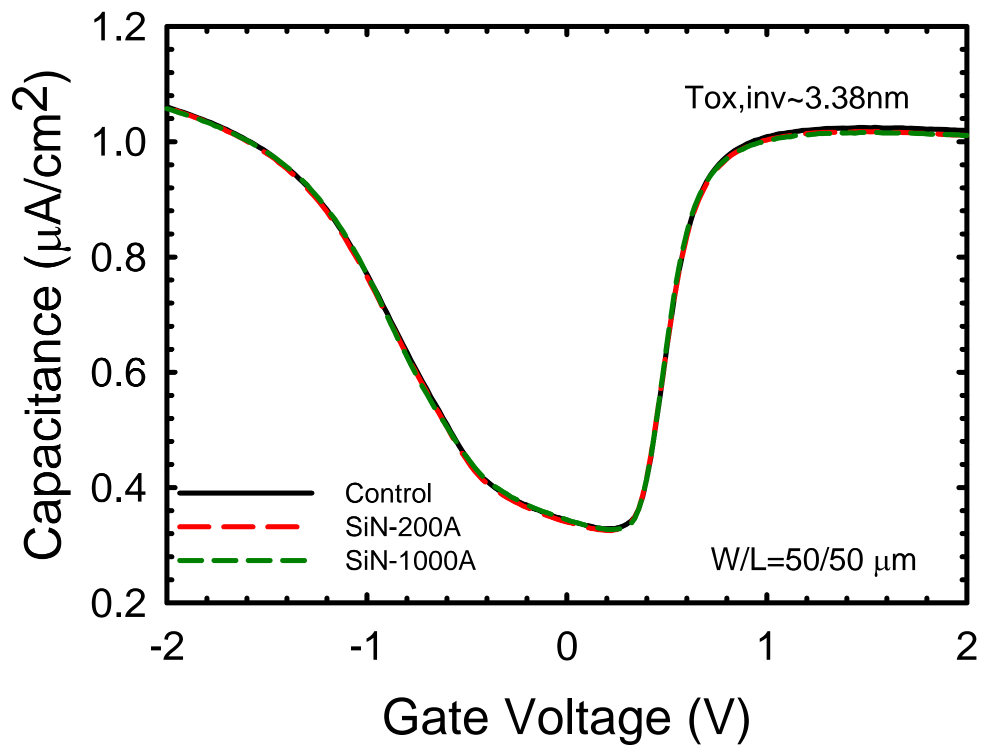


Fig. 4.3 Capacitance-Voltage (*C*-*V*) characteristics for all splits of samples, showing almost identical curves and the extracted electrical thickness is about 3.38 nm.

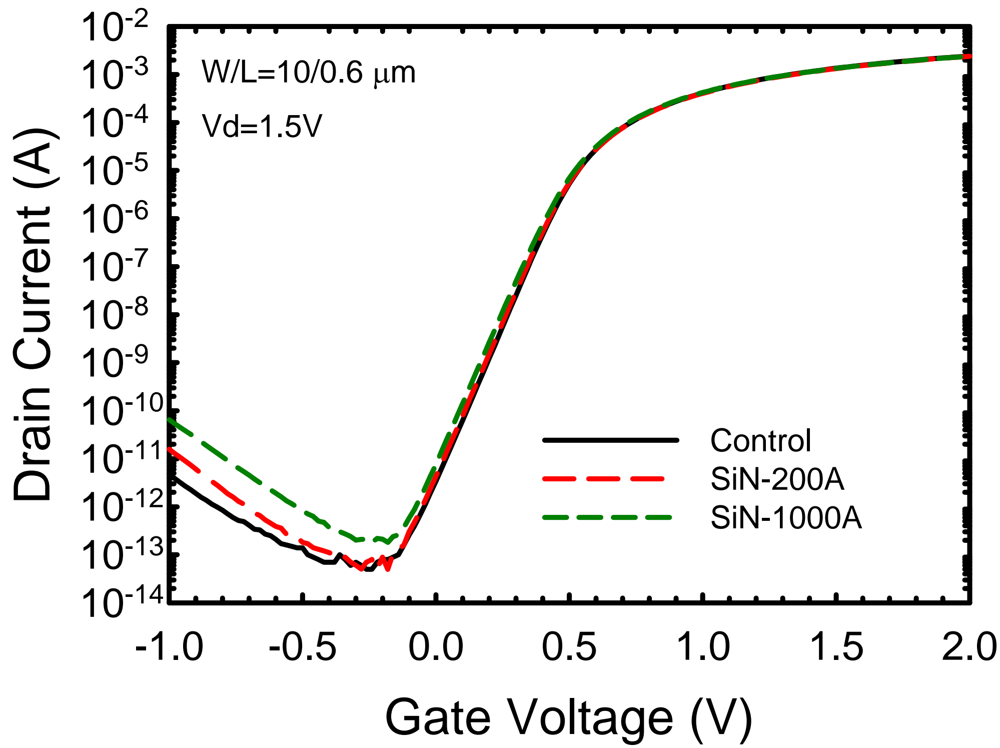


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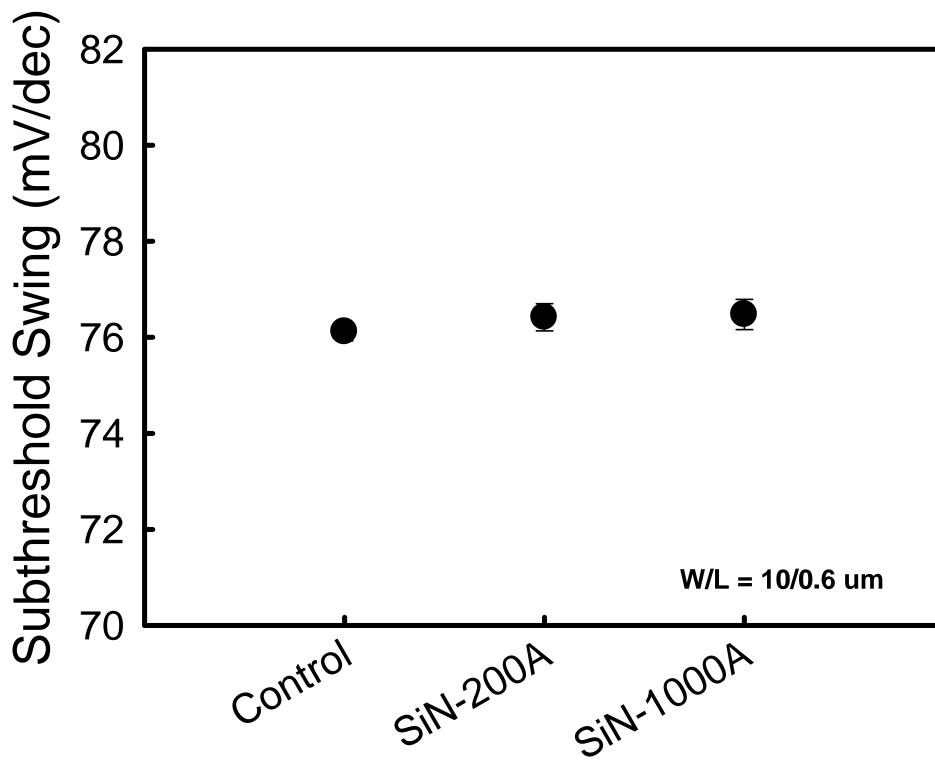
Fig. 4.4 Subthreshold characteristics of NMOSFETs for all splits of samples with W/L = 10/0.6 μm. The SiN-1000Å split depicts the largest off-state leakage current among all splits and the leakage current increases with increasing gate bias.



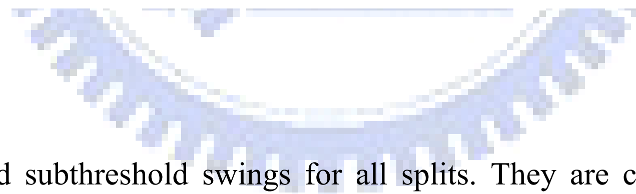
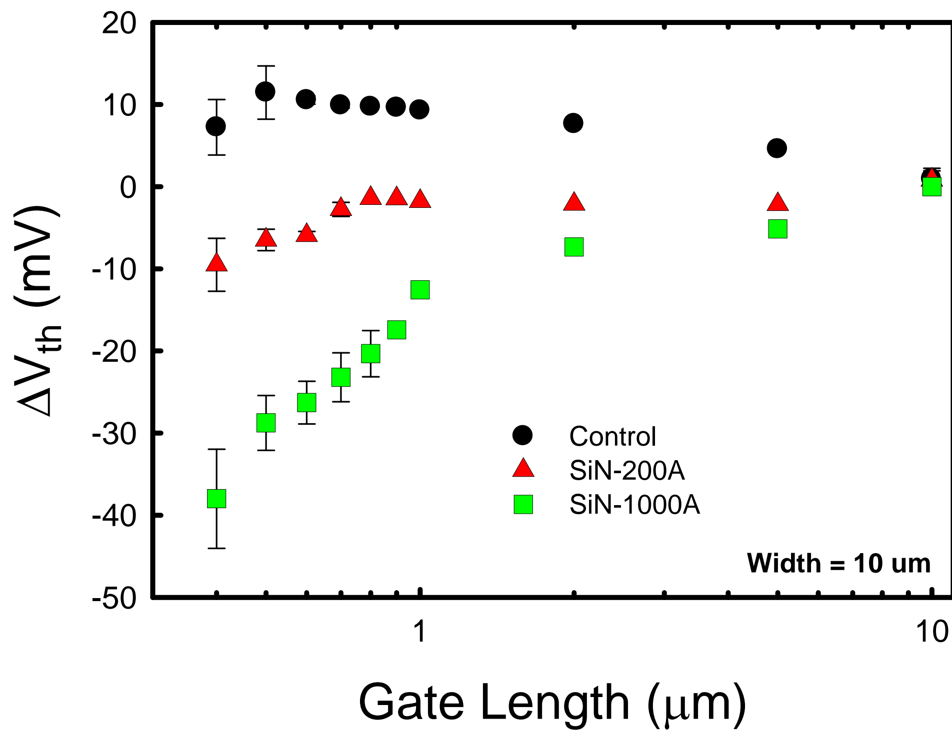


Fig. 4.5 Extracted subthreshold swings for all splits. They are confined in a narrow range between 76 ~ 77 mV/decade.



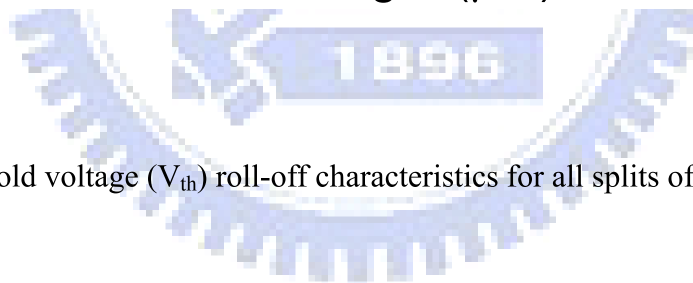


Fig. 4.6 Threshold voltage (V_{th}) roll-off characteristics for all splits of devices.

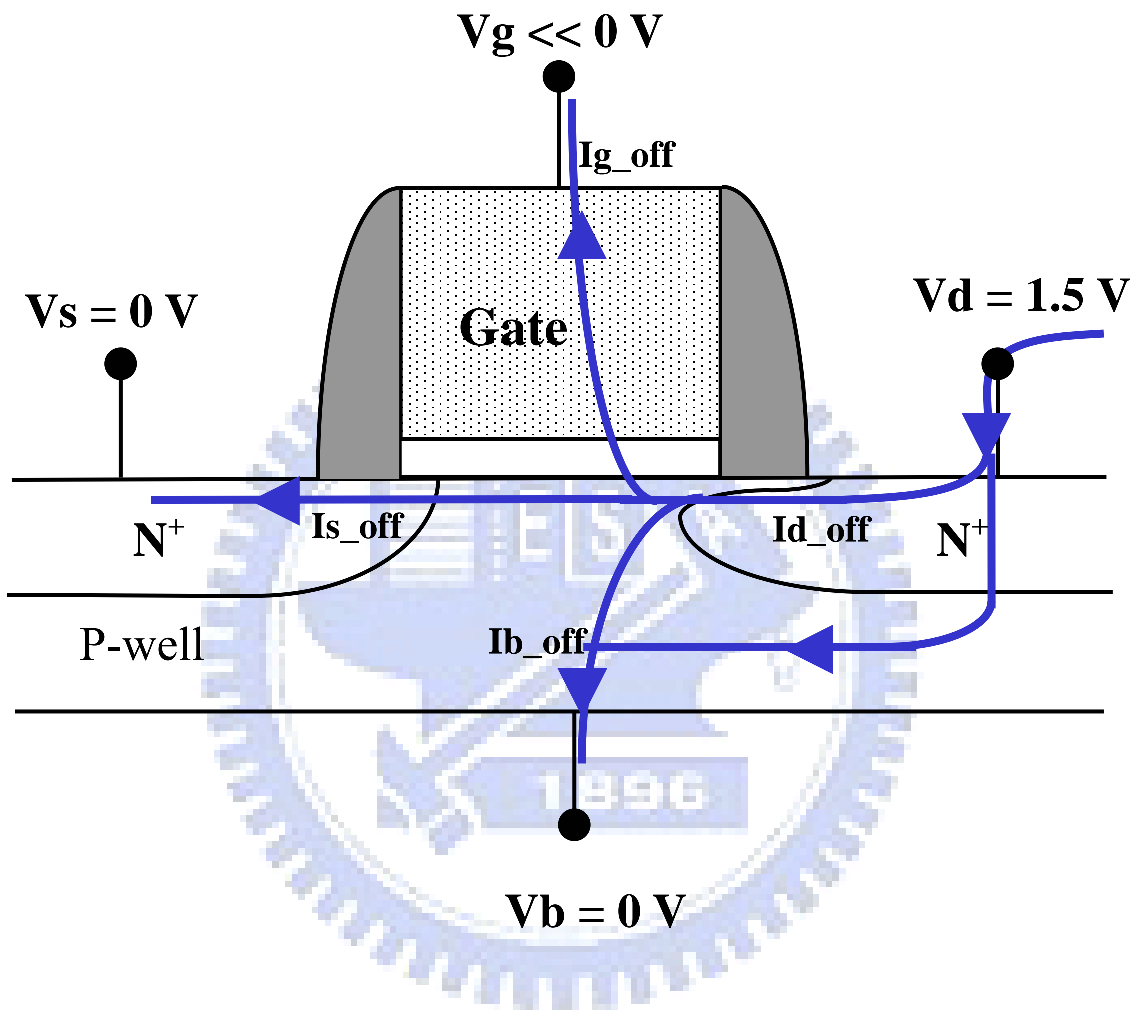
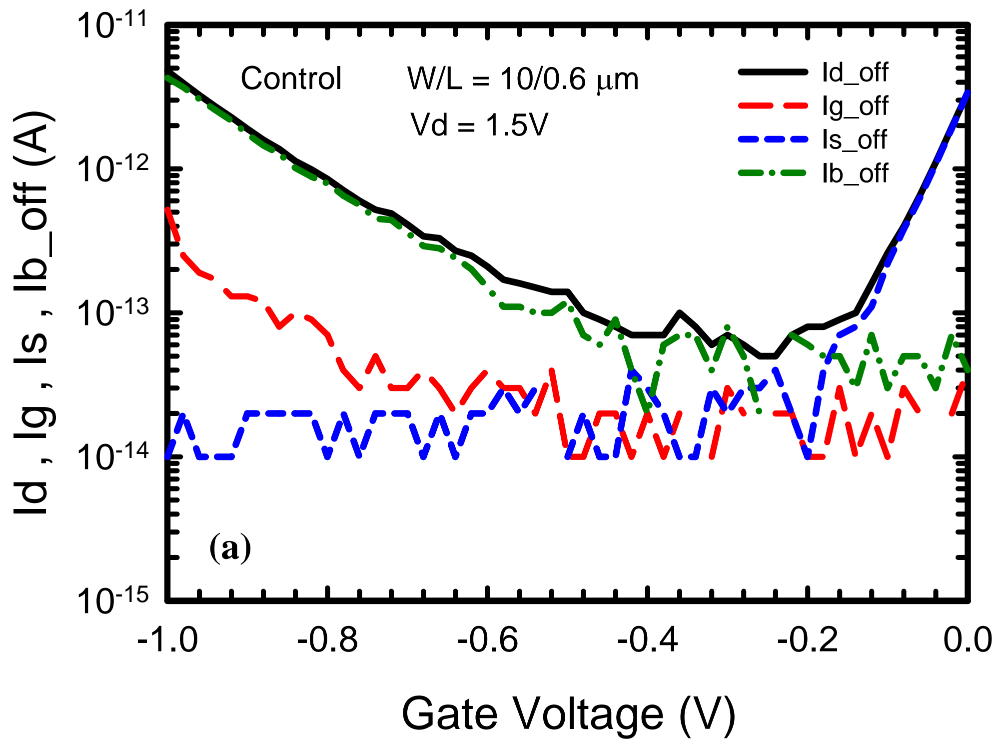


Fig. 4.7 Illustration of various leakage paths for NMOSFETs with Vd = 1.5 V, Vg = 0 ~ -1 V, and Vs = Vb = 0 V.



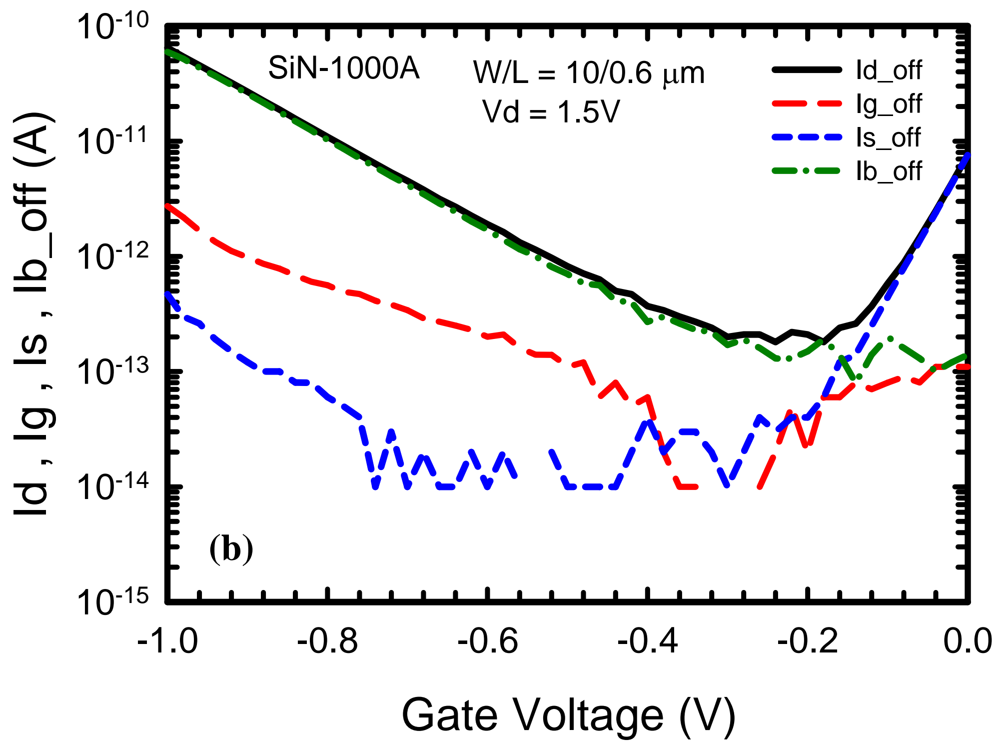


Fig. 4.8 The four-terminal leakage current (Id_off, Ig_off, Is_off, and Ib_off) for (a) control, and (b) SiN-1000Å samples, respectively, when Vg was swept from 0 to -1 V and Vd fixed at 1.5 V.

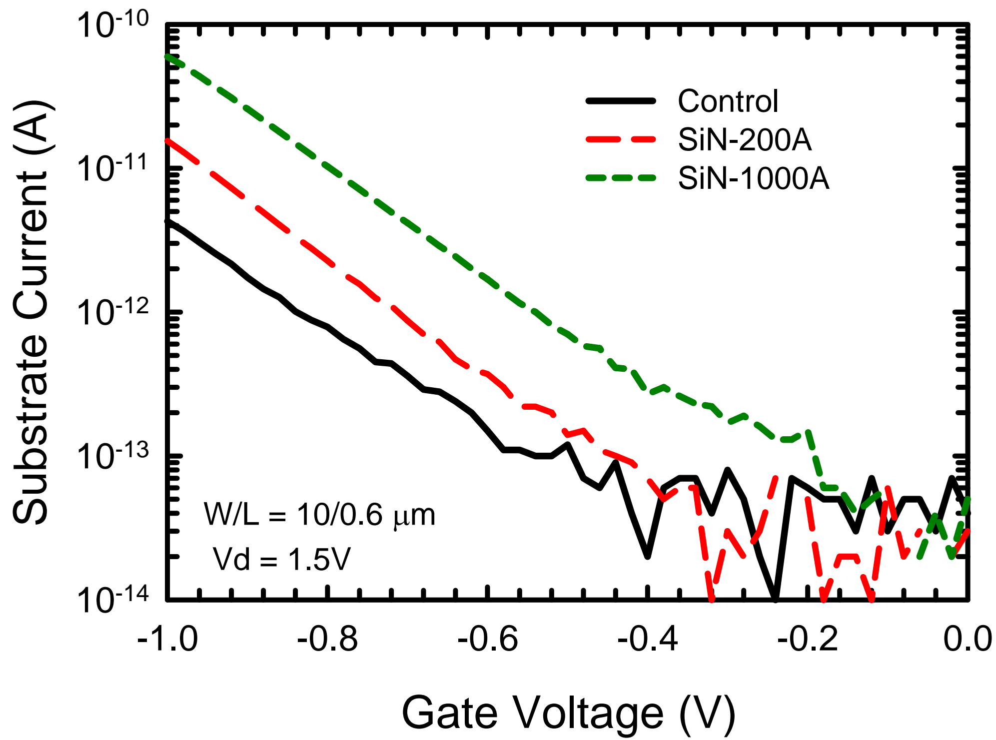


Fig. 4.9 Substrate currents for all splits of samples, showing that SiN-1000Å split depicts the largest Ib_off current among all splits.

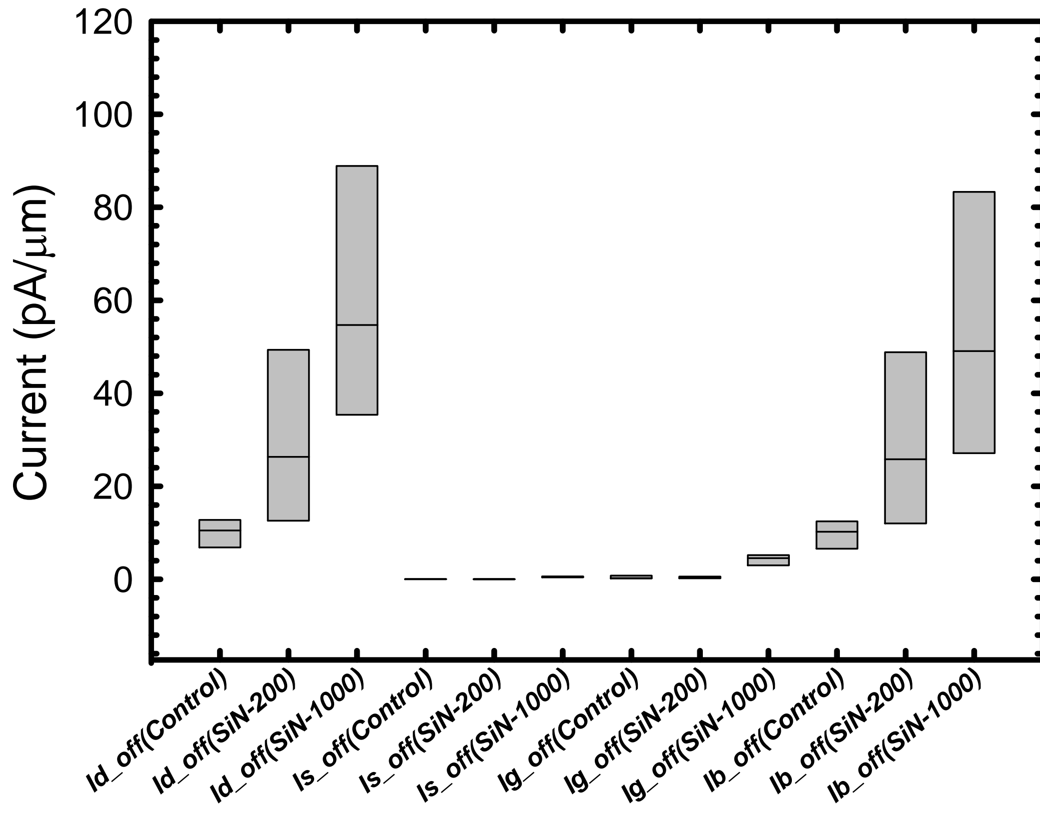


Fig. 4.10 Statistical box plot of off-state current for all splits. These data were measured from seven different die positions with Vd = 1.5 V and Vg = -0.9 V at W/L = 10/0.6 μm.

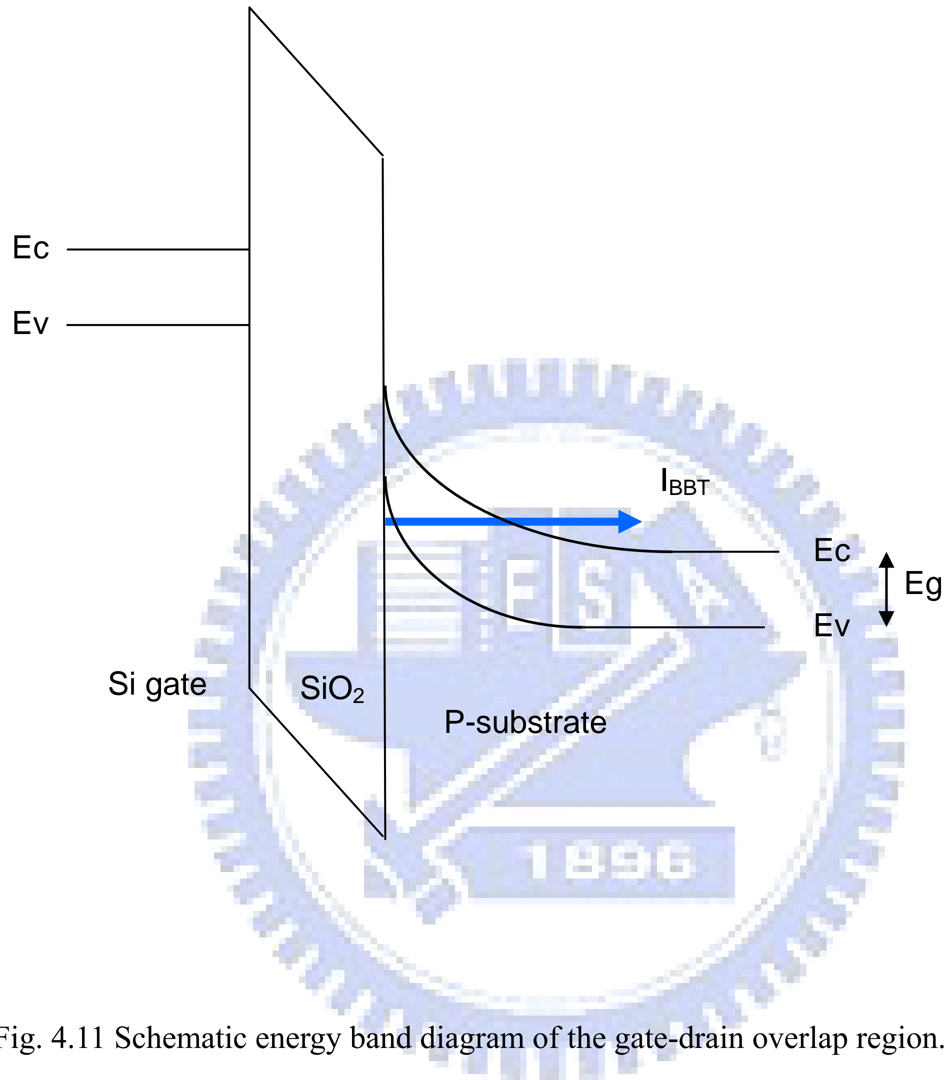


Fig. 4.11 Schematic energy band diagram of the gate-drain overlap region.

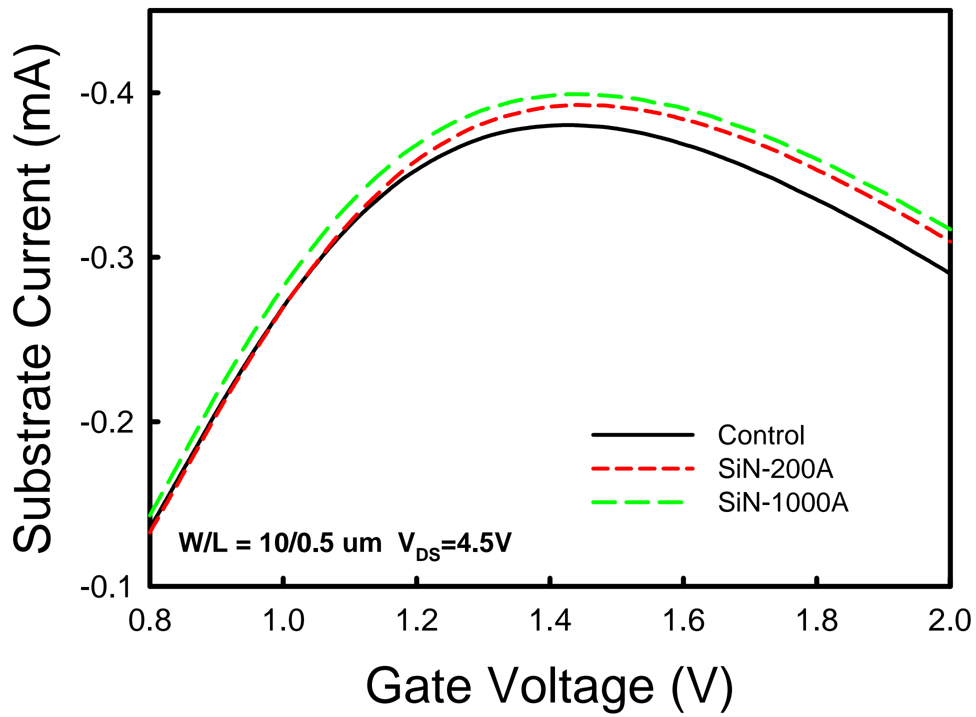


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Fig. 4.12 Substrate current (I_{sub}) versus gate voltage for all splits of devices with W/L = 10/0.5 μm at V_{DS} = 4.5 V. Substrate current increases with increasing SiN thickness.

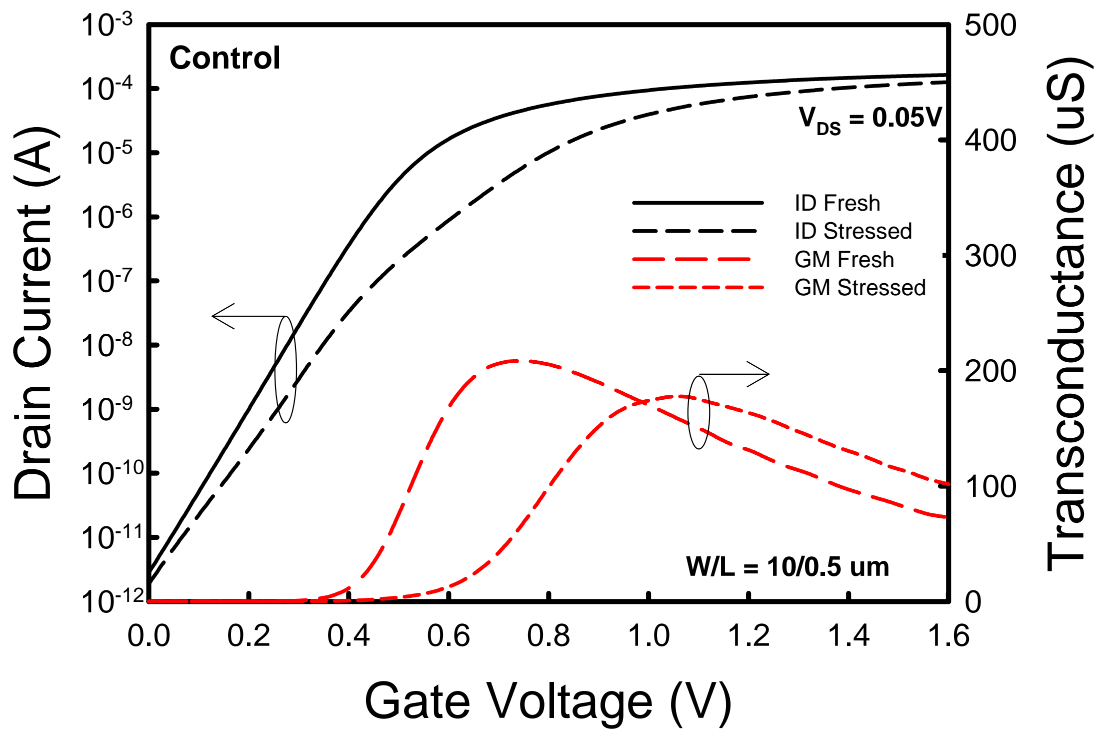

Fig. 4.13 (a) Subthreshold characteristics and transconductance before and after 5000 sec hot-carrier stress for control samples.

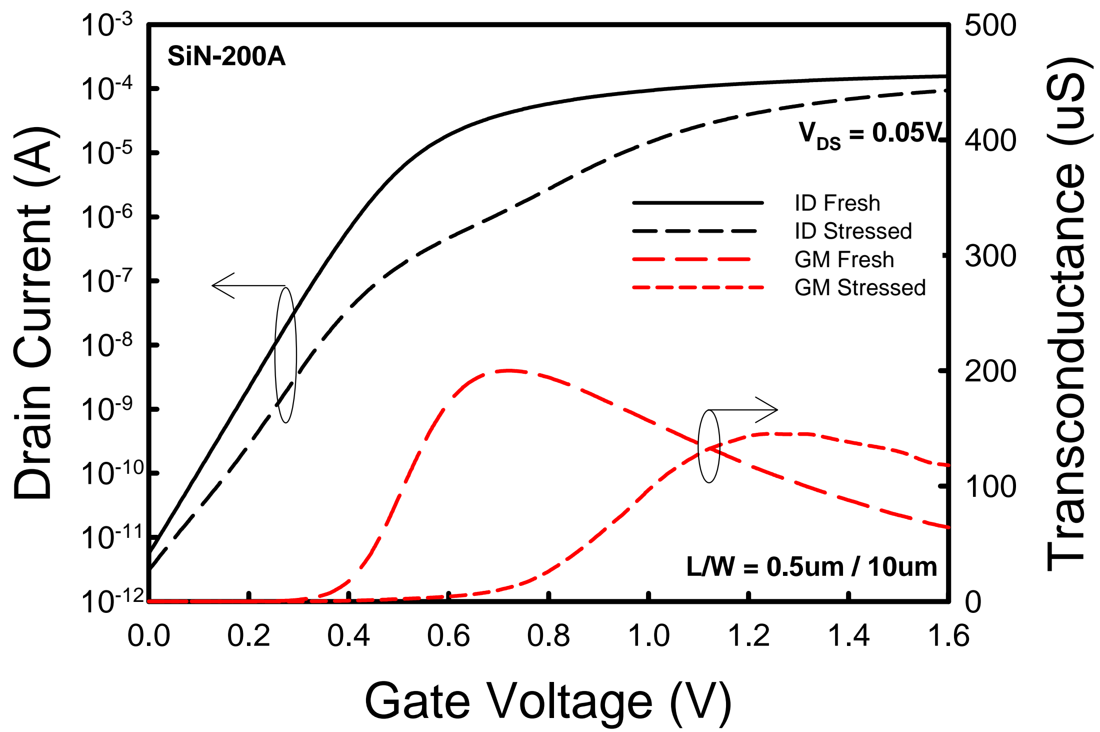

Fig. 4.13 (b) Subthreshold characteristics and transconductance before and after 5000 sec hot-carrier stress for SiN-200Å samples.

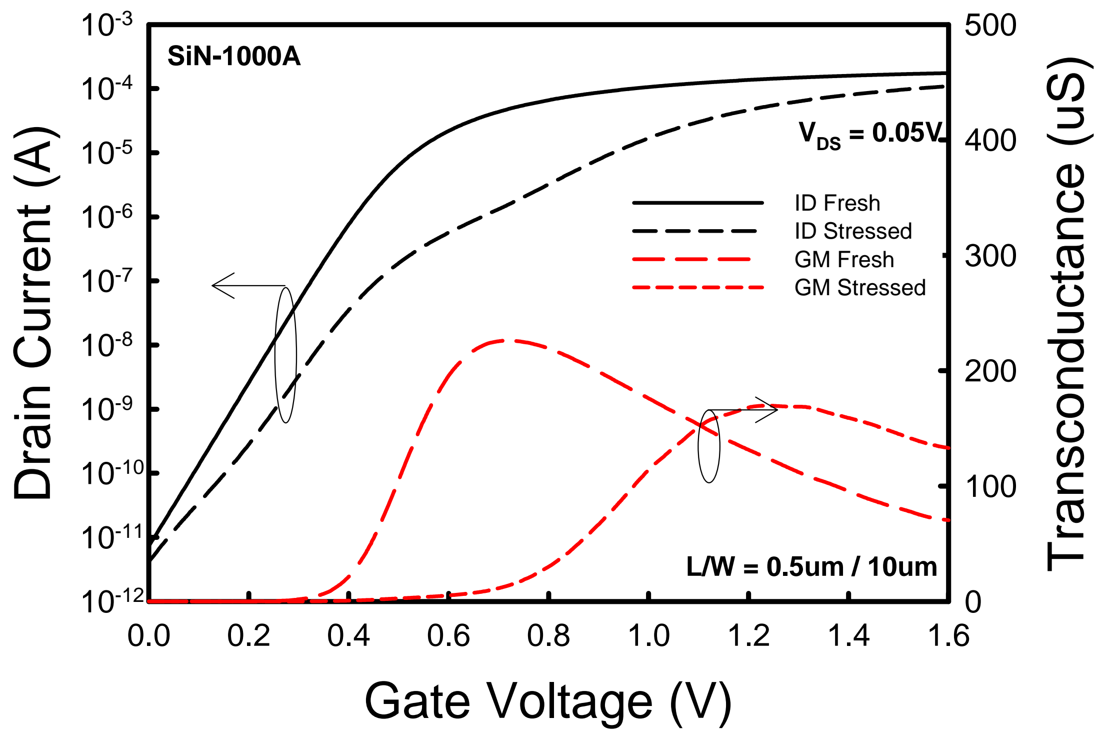

Fig. 4.13 (c) Subthreshold characteristics and transconductance before and after 5000 sec hot-carrier stress for SiN-1000Å samples.

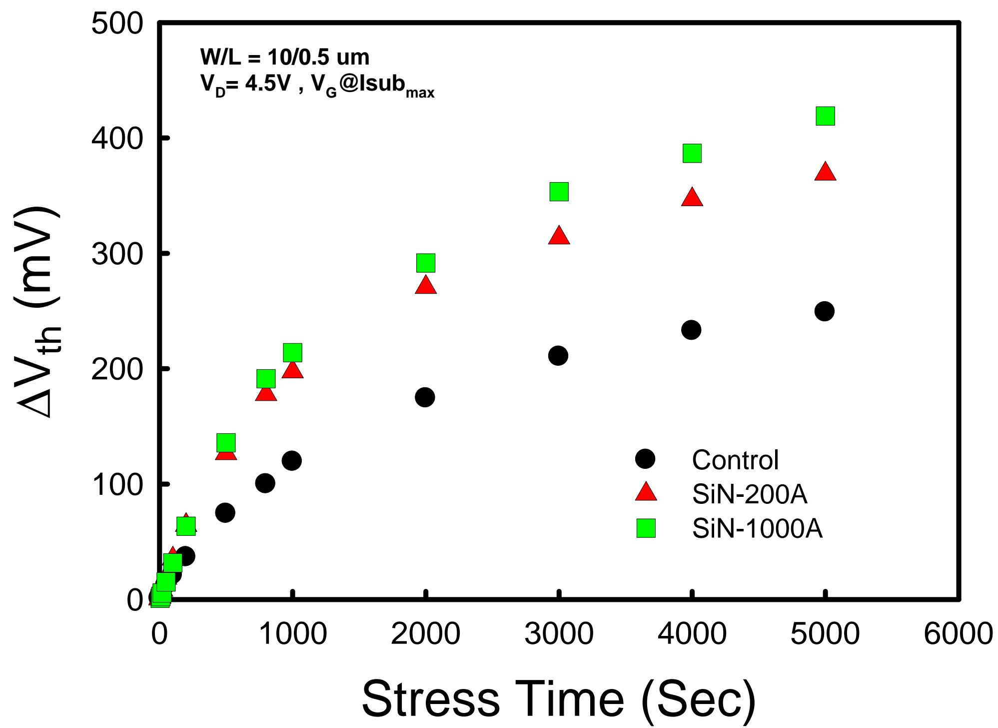

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Fig. 4.14 Threshold voltage shift as a function of stress time. Devices with W/L = 10/0.5 μm were stressed at V_{DS} = 4.5 V, and V_G of maximum substrate current.

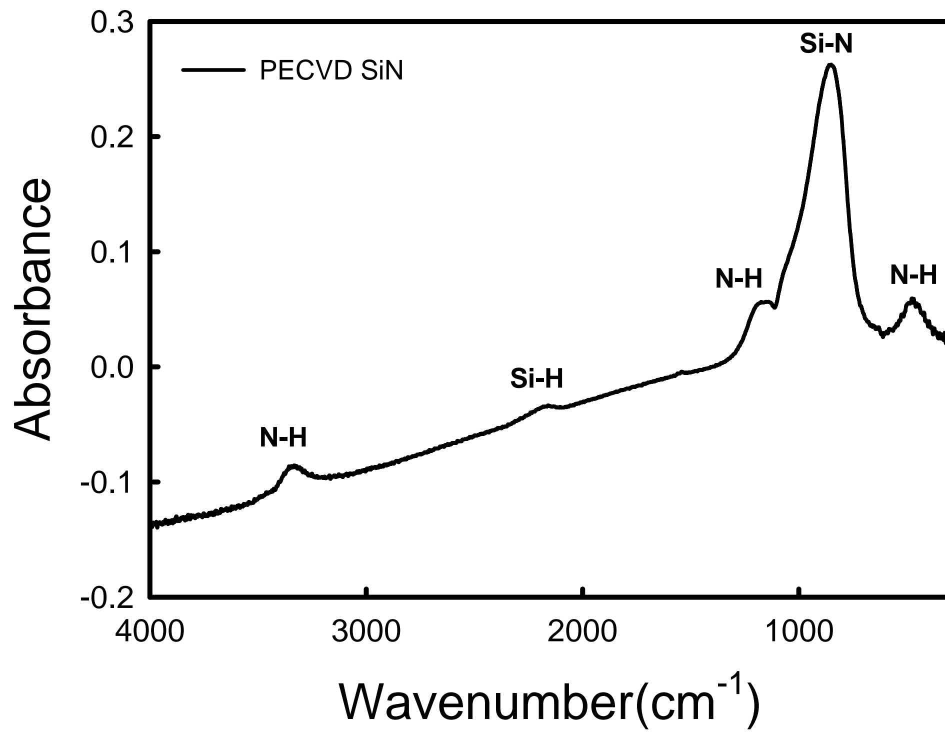

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Fig. 4.15 Bonding signals of PECVD SiN film measured by Fourier transform infrared spectrometer (FTIR). Extra Si-H bonding signals are observed, implying that SiN film indeed has higher hydrogen content.

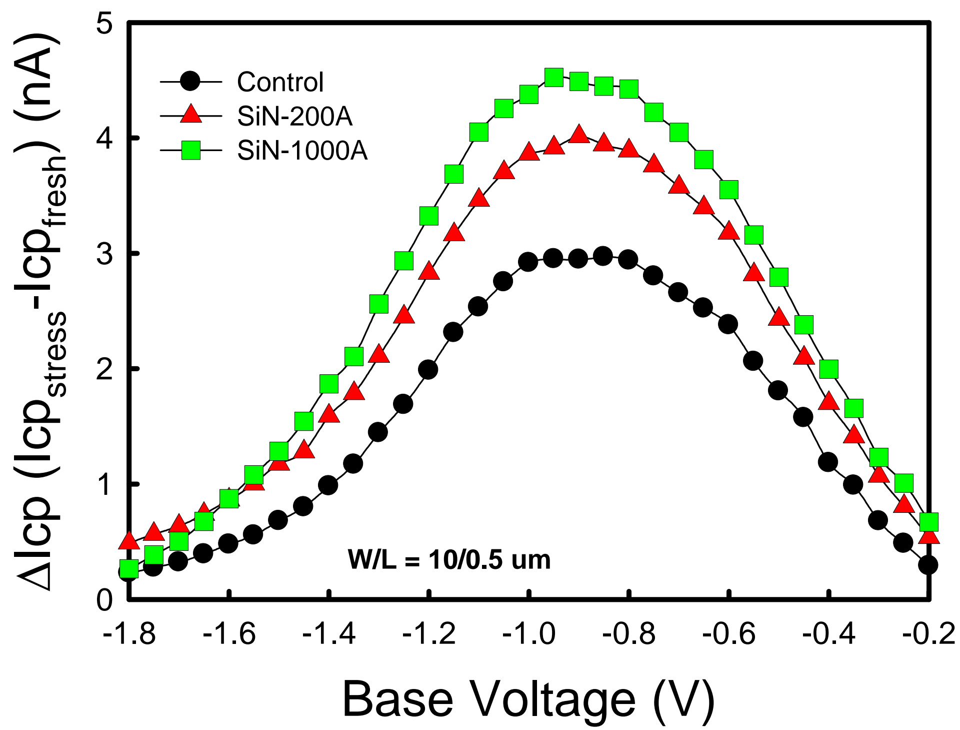

Fig. 4.16 The difference of charge pumping current before and after 5000 sec hot-carrier stress for all splits of samples. More interface states are generated during the hot-carrier stress for SiN-1000Å split.

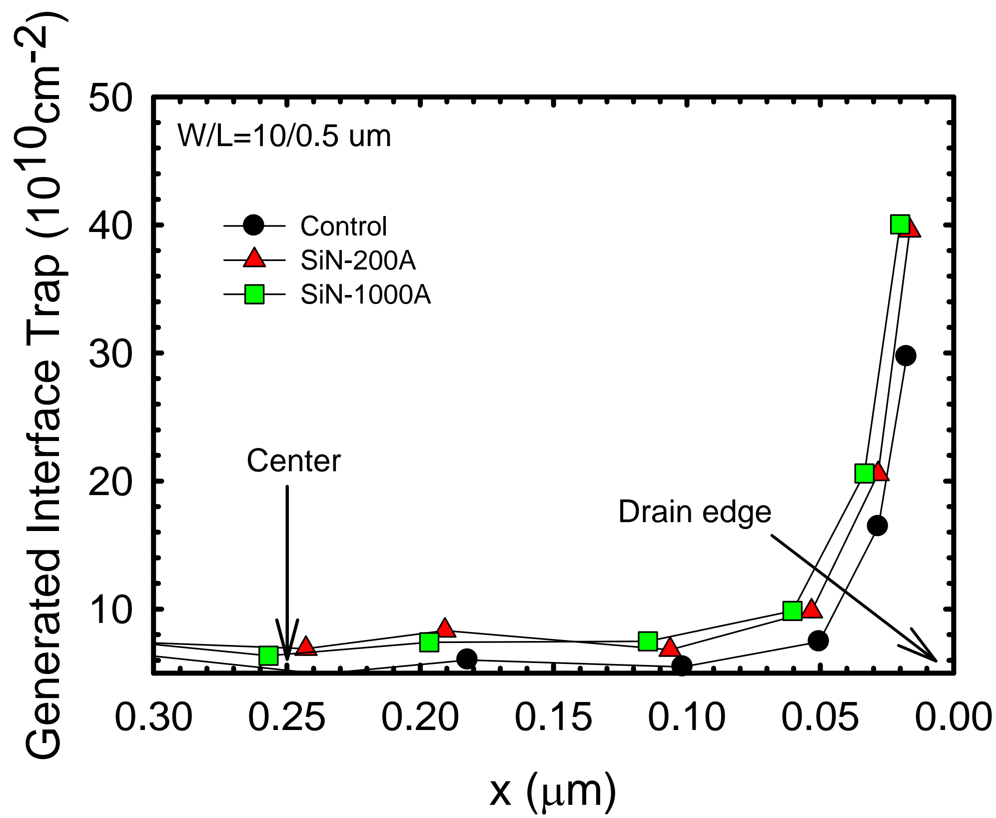

Fig. 4.17 Lateral profile of interface state generation after hot-carrier stress for all splits of devices. Hot-carrier degradation is highly localized and the major damage region is confined within 0.1 μm near the drain edge.

Chapter 5

Improvements of Negative-Bias-Temperature Instability in SiN-Capped p-Channel Metal-Oxide-Semiconductor Field-Effect Transistors Using Ultra-thin HfO_2 Buffer Layer

5.1 Introduction

Negative bias temperature instability (NBTI) is known to be a critical reliability concern and represents one of the major bottlenecks for product lifetime in nano-scale p-channel metal-oxide-semiconductor field-effect-transistors (PMOSFETs) [1-7]. Usually the creation of interface traps and positive fixed charges by the dissociation of Si-H bonds at the SiO_2/Si interface could cause a large threshold voltage shift, thus diminishing the current drive and transconductance of the device, and may eventually lead to circuit malfunction.

On the other hand, using process techniques to induce uniaxial strain in the channel for enhancing carrier mobility and thus drive current has recently received a lot of attention [8-16]. Several approaches have been reported to induce compressive channel strain beneficial for improving the hole mobility, including embedded SiGe in the source/drain (S/D) region [10,11] and the SiN contact etch-stop layer (CESL) [12-14]. The latter approach is typically carried out by depositing the SiN layer using plasma-enhanced chemical vapor deposition (PECVD). In contrast to the complex and costly SiGe refill scheme, the simplicity and maturity of the PECVD SiN (PE-SiN) process seem much more attractive and practical. Although strained channel could boost device performance, the strain energy stored in the channel and a high amount of hydrogen species contained in the PE-SiN layer could potentially worsen the NBTI

reliability [15,16]. To address this issue, in this chapter we present a new approach by inserting a thin buffer layer prior to SiN capping for suppressing hydrogen diffusion into the channel.

5.2 Devices Fabrication

The PMOSFETs in this study were fabricated on 6-inch n-type Si wafers with conventional local oxidation of silicon (LOCOS) isolation. Gate oxide with a thickness of 3 nm was grown in a vertical furnace in O_2 at 800°C. After gate oxide growth, a 200nm-thick polycrystalline silicon (poly-Si) was deposited by low-pressure chemical vapor deposition (LPCVD), followed by standard plasma gate-etch to form the patterned gate. Afterwards, standard procedures were applied to form tetraethoxysilane (TEOS) spacer and S/D junctions. Subsequently, a rapid thermal annealing at 900°C for 30 sec was performed to activate dopants in the gate and S/D regions. A 300nm-thick PE-SiN was then deposited onto the device surface, followed by the deposition of TEOS passivation by PECVD. For some SiN-capped samples, a 3nm-thick HfO_2 buffer layer deposited by metal-organic chemical vapor deposition (MOCVD) was capped prior to SiN deposition (denoted as HfO_2-buffered split). The thickness measured from cross-sectional transmission electron microscope (TEM) pictures for SiN and HfO_2 layer is about 310 nm and 3 nm, respectively, as shown in Figs.5.1 (a) and (b). Contact holes and metallization processes were subsequently performed. Finally, the processing steps were completed with a forming gas anneal at 400°C. Electrical characteristics were measured using an Agilent 4156 system. Interface traps were evaluated using charge pumping method with fixed amplitude of 1.5 V at 1MHz. NBTI stress measurements were performed using a temperature-regulated hot chuck at 125°C. We have also performed the measurements with applied frequencies ranging from 1 kHz to

1 MHz. These setups of measurement are shown in Figs.2 (a), (b), and (c), respectively.

5.3 Results and Discussion

5.3-1 Devices Characteristics

The stress of PE-SiN layer with and without an HfO_2 buffer layer (3 nm) was first examined by probing blanket monitor samples deposited on Si wafers. We confirmed that the stress was compressive in nature with a magnitude of around -700 MPa for all samples, irrespective of the HfO_2 presence. This indicates that the insertion of such an ultra-thin buffer layer would not relax the strain introduced by the SiN capping.

Figure 5.3 compares transconductance data for all splits with channel width/length (W/L) = 10/0.4 μm. It can be seen that the transconductance of all SiN-capped samples, with or without HfO_2 buffer layer, depicts significant and identical enhancement of around 26% with respect to that of the control counterparts without SiN capping. Output characteristics of PMOSFETs are shown and compared in Fig. 5.4. Similar enhancement trend in the drive current is also observed for the two SiN-capping splits. These findings confirm the results obtained in stress measurements that the insertion of an ultra-thin HfO_2 buffer layer does not compromise the performance enhancement induced by the SiN capping.

Figure 5.5 shows the percentage increase in transconductance for SiN-capped and HfO_2-buffered splits, compared with the control split, as a function of channel length. Each datum represents the mean measurement result performed on eight devices in this figure. As the channel length becomes shorter, the distance from the edge of spacer to the channel center becomes shorter, so the induced strain is stronger. Therefore, we can see that the transconductance enhancement increases with decreasing channel length. It is a unique feature for uniaxial strain by SiN capping [17,18]. Moreover, the induced

compressive strain is not relieved by the insertion of the buffer layer. Capacitance-voltage (*C-V*) characteristics of all splits of samples coincide altogether, as shown in Fig. 5.6. Negligible differences in oxide thickness among these devices are observed, indicating that the above-mentioned observations indeed are not caused by the oxide thickness difference among splits. The subthreshold characteristics of PMOSFETs for all splits of samples are shown in Fig. 5.7. We can see that the subthreshold characteristics are not affected by the presence of SiN and HfO_2-buffer layers. This is further convinced in Fig. 5.8, in which the mean value of the extracted subthreshold swing from ten devices is the same for the three splits of devices.

5.3-2 Negative Bias Temperature Instability Characterization

The setup of DC NBTI measurement is shown in Fig. 5.2(b). Figure 5.9 shows the results of NBTI stress performed at three different gate biases for HfO_2-buffered samples. It can be seen that larger gate bias leads to larger threshold voltage shift (ΔV_{th}), implying that more defects are being generated at higher bias. The shift curves show a fractional power-law dependence on time ($\Delta V_{th} \propto t^n$), and the values of the exponent (n) are roughly 0.3 for these samples. A comparison among the three splits of samples is given in Fig. 5.10, under the same stress condition, V_G-V_{th} = -3.5 V. It is seen that the SiN-capped split depicts much larger ΔV_{th} as compared with the control split. The enhanced degradation is partially relieved when the HfO_2 buffer layer is added. After 1000 sec stress, ΔV_{th} is 46.12 mV, 197.23 mV, and 274.72 mV for control, HfO_2-buffered, and SiN-capped splits, respectively. The results indicate that about 327% and 495% ΔV_{th} degradation are observed for HfO_2-buffered and SiN-capped samples compared with the control ones, where 168% improvement is obtained by adding HfO_2 buffer layer. Figure 5.11 compares the increase in interface state density

(ΔN_{it}) and subthreshold swing shift (ΔSwing) for all samples extracted using the charge pumping technique. Basically the trends are similar to those shown in Fig. 5.10. Figure 5.12 shows the transconductance degradation ratio as a function of stress time. The transconductance degradation ratio for SiN-capped split depicts the severest degradation among all three splits, reaching 16% after 1000 sec stress, implying that NBT stress grossly degrades the device performance and negates the benefit gained from the SiN capping, though the SiN capping can enhance carrier mobility in a fresh device. More importantly, the transconductance degradation is alleviated for HfO_2-buffered split. These results clearly indicate that the use of PE-SiN capping may aggravate NBTI, while the insertion of HfO_2 buffer layer can be helpful to mitigate the situation. In short, although the capping of SiN tends to worsen the device reliability characteristics, the insertion of a thin HfO_2 buffer layer between the gate and the SiN can effectively shield the device against the degradation.

These findings are postulated to be related to the hydrogen species contained in the PE-SiN layer. Actually, visible H-bonding signals from the PE-SiN layer can be detected by Fourier transform infrared spectrometer (FTIR), as shown in Fig. 5.13, indicating that the film indeed contains a substantial amount of hydrogen. Although hydrogen can effectively passivate the dangling bonds at the SiO_2/Si interface, the passivated Si-H bonds are more easily broken during subsequent stressing, so the voluminous hydrogen species could aggravate NBTI. The insertion of a thin HfO_2 buffer layer between the gate and SiN capping can effectively suppress the diffusion of hydrogen into the gate oxide and oxide/channel interface, resulting in less broken Si-H bonds and thus less newly-generated interface states during stressing as compared with the SiN-capped split. It is well known that the deposited HfO_2 layers typically contain a high density of structural defects [19,20]. We postulate that these defects tend to trap the

hydrogen species diffusing during the SiN deposition and subsequent thermal cycles.

To simulate real-life operation of CMOS circuits, the effect of AC NBTI stress was also investigated. The measurement setup was shown in Fig.5.2(c) with 50 % duty cycle and amplitude of AC signal ranging from V_G-V_{th} = -3.5 V to 0 V. The frequency dependence of NBTI degradation in HfO_2-buffered samples was measured and shown in Fig. 5.14. It can be seen that Vth depicts less shift with higher frequency. ΔV_{th} after 1000 sec stress is plotted as a function of stress frequency and compared for all samples of splits, as shown in Fig. 5.15. It is clear that ΔV_{th} is strongly dependent on frequency for SiN-capped and HfO_2-buffered samples, while control samples show weak frequency dependence. We can see that ΔV_{th} decreases from 274 mV to 43 mV for SiN-capped samples, from 197 mV to 36 mV for HfO_2-buffered ones, and from 45 mV to 18 mV for the control ones, when stress frequency increases from DC to 1 MHz. This observation can be explained by the postulation that excess hydrogen-related bonds due to SiN capping would be broken during the NBTI stressing, leading to larger Vth shift. However, the bond breaking process needs sufficient stress time to trigger, resulting in the significant frequency dependence. These results indicate that the aggravated NBTI degradation in the strained devices can be alleviated by high frequency operation while HfO_2-buffered samples still depict less degradation than SiN-capped samples.

In this thesis, the thickness of the HfO_2 buffer is fixed at 3 nm. Such a thin buffer layer would not compromise the performance gain obtained from the channel strain. In the meantime, the immunity against NBTI degradation is clearly demonstrated. However, it should be noted that the optimum thickness is yet to be determined. In this aspect more effort is in progress, and it is expected that further improvement in NBTI immunity is possible when the condition is optimized.

5.4 Summary

SiN-capped PMOSFETs with a thin HfO_2 buffer layer were fabricated and characterized in this thesis. Although the SiN layer tends to worsen the NBTI characteristics, our results demonstrate the usefulness of inserting a buffer layer in relieving the situation. Furthermore, no performance gain from the channel strain is compromised at all as the thin buffer layer is inserted. Such improvement is ascribed to the suppression of hydrogen diffusion from the SiN to the gate oxide and the oxide/channel interface with the insertion of the buffer layer.

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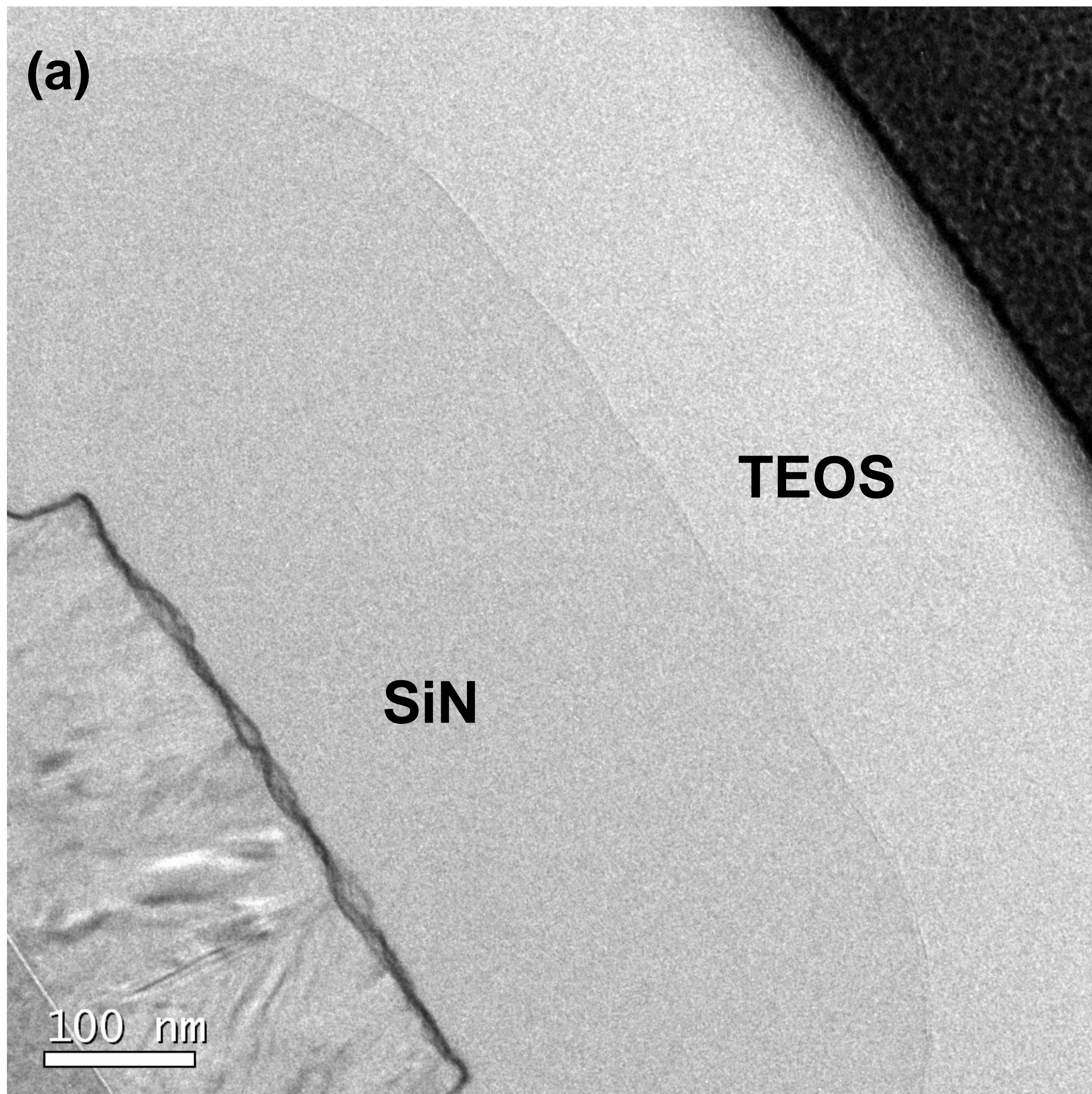


Fig. 5.1(a) Cross-sectional TEM pictures of HfO_2-buffered samples taken in passivation region.

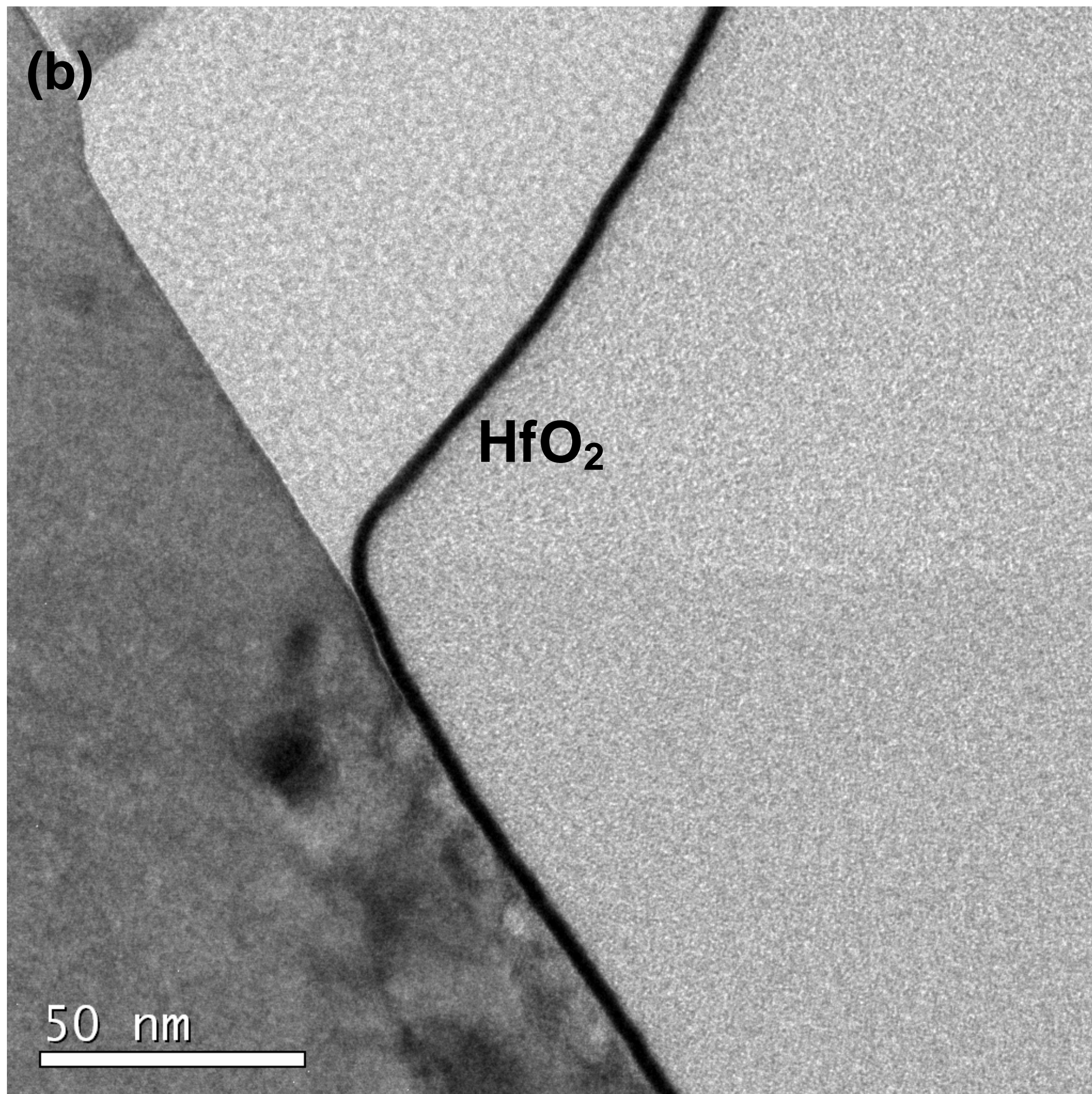


Fig. 5.1(b) Cross-sectional TEM pictures of HfO_2-buffered samples taken in spacer region. The thickness of SiN and HfO_2 buffer layer is roughly 310 nm and 3 nm, respectively.

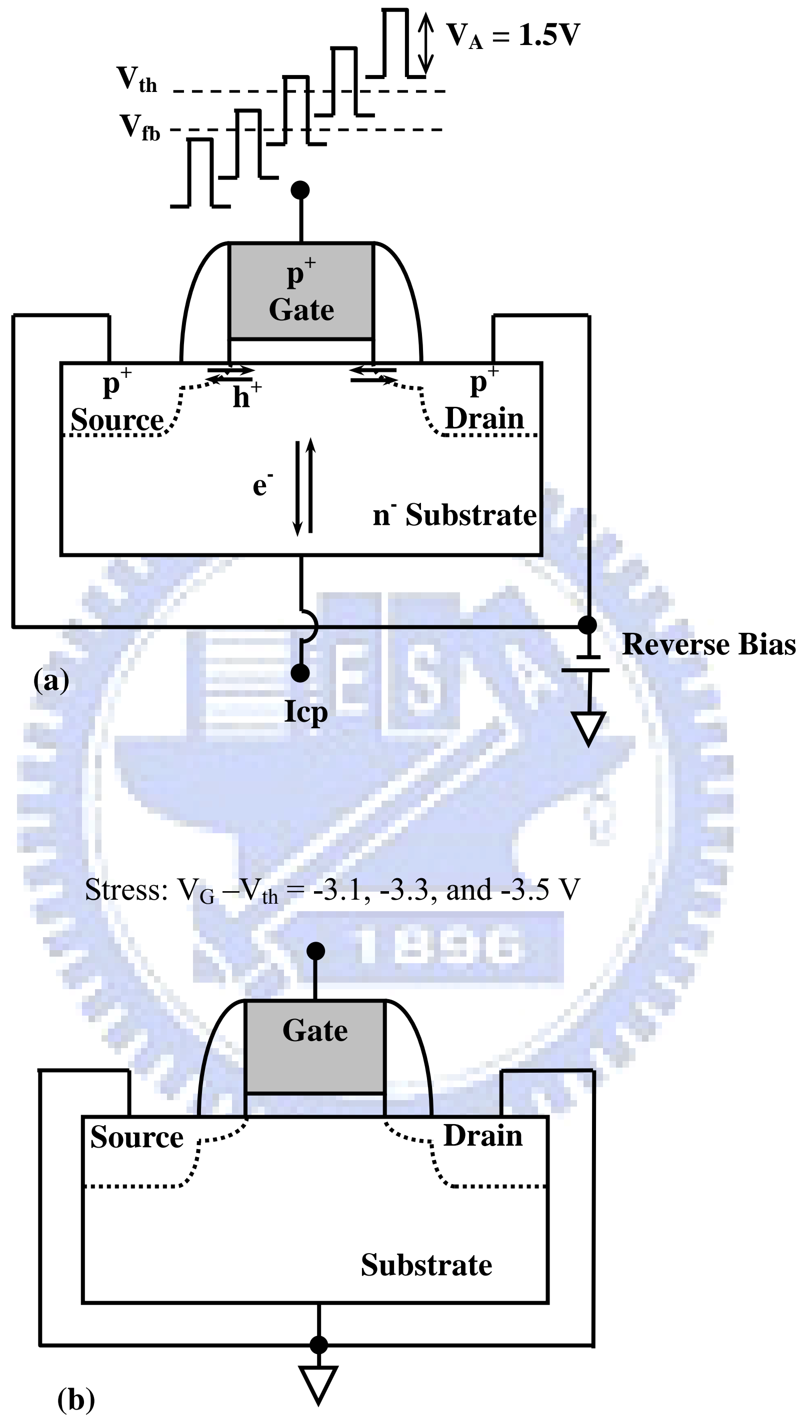
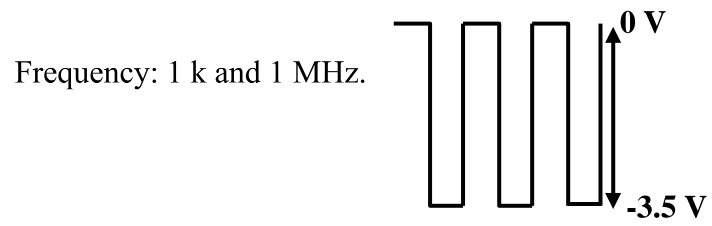


Fig. 5.2 (a) Setups of charge pumping measurement, and (b) setups of DC NBTI stress measurement,



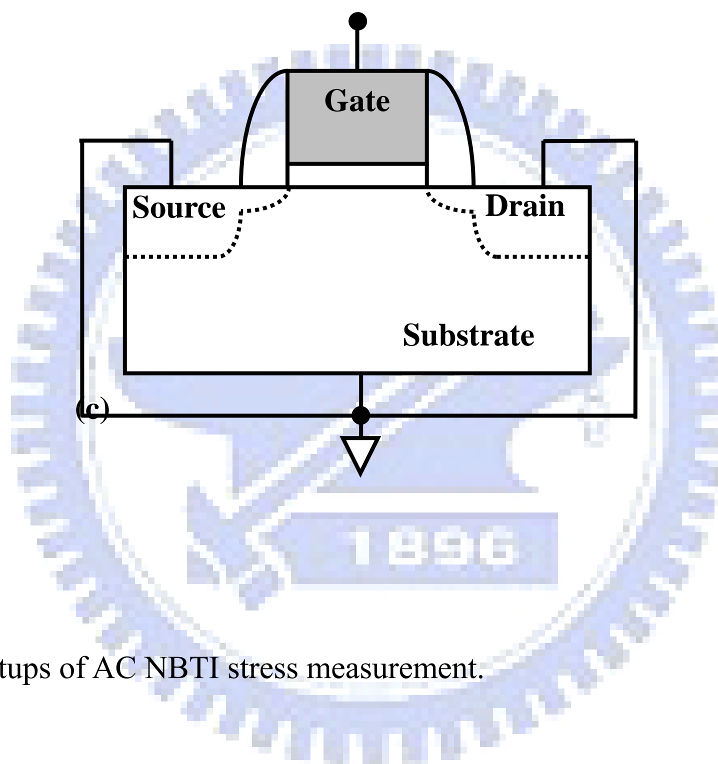


Fig. 5.2 (c) Setups of AC NBTI stress measurement.

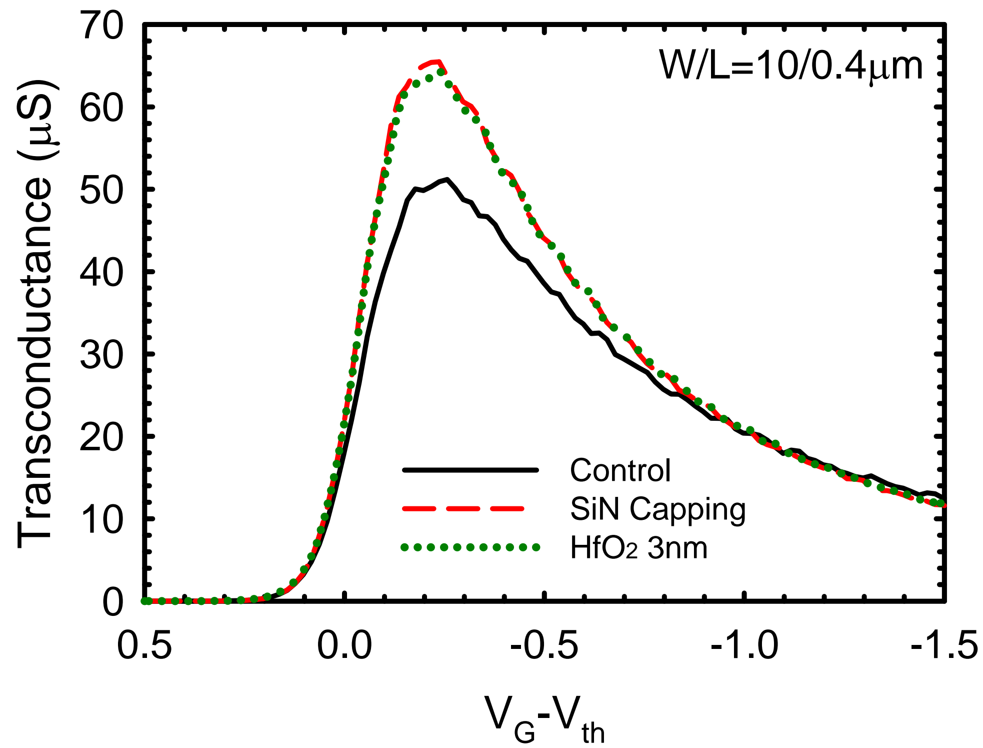


Fig. 5.3 Transconductance versus V_G-V_{th} for all splits of samples. For the SiN-capped devices, with or without inserting the buffer layer, the transconductance is clearly increased with respect to the control.

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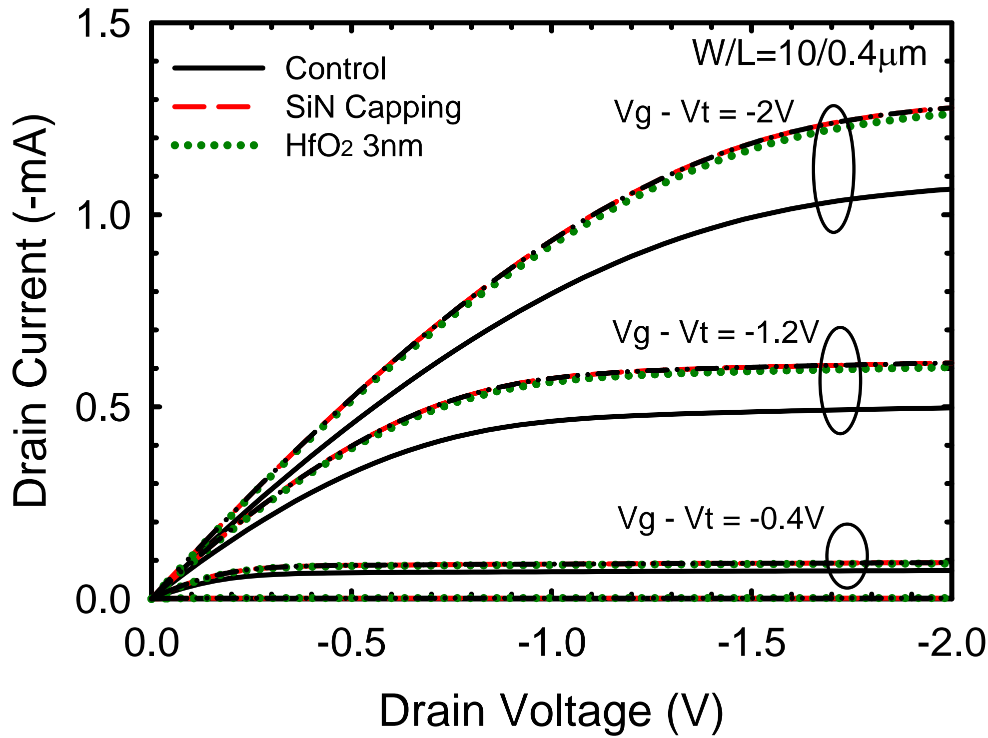

Fig. 5.4 Output characteristics of PMOSFETs for all splits. The insertion of the HfO_2 buffer in the SiN-capped device does not compromise the drive current enhancement with respect to the control.

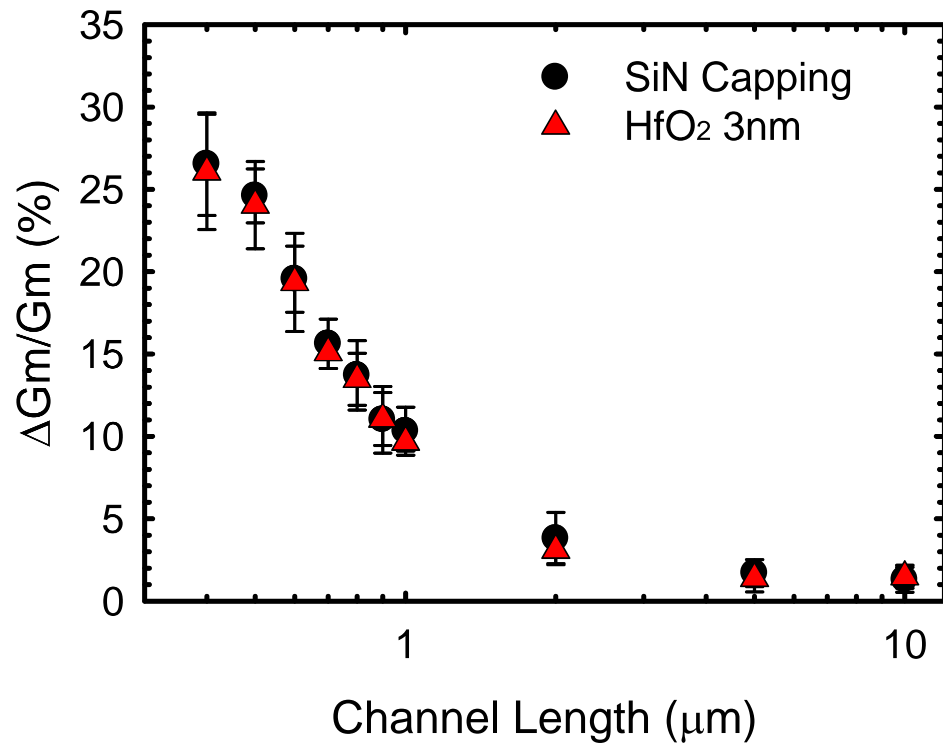

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Fig. 5.5 Transconductance increase versus channel length. Each datum point represents the mean measurement result performed on eight devices.

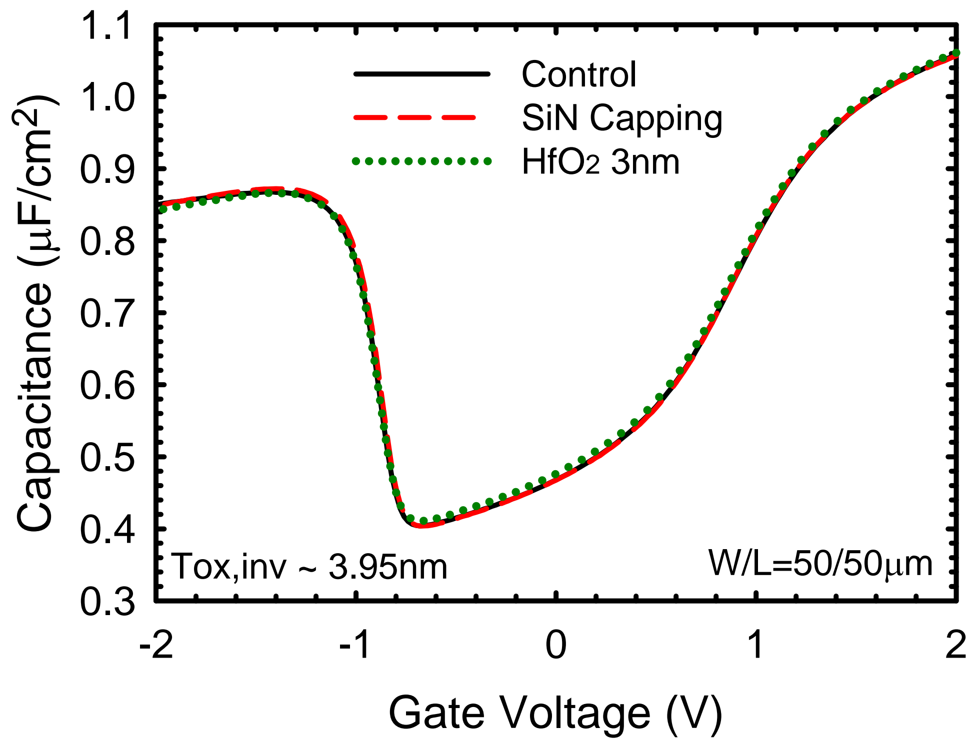

Fig. 5.6 Capacitance-Voltage (*C*-*V*) characteristics of all splits. The curves are almost coincided with each other, indicating that the oxide thickness difference among the three splits is negligible.

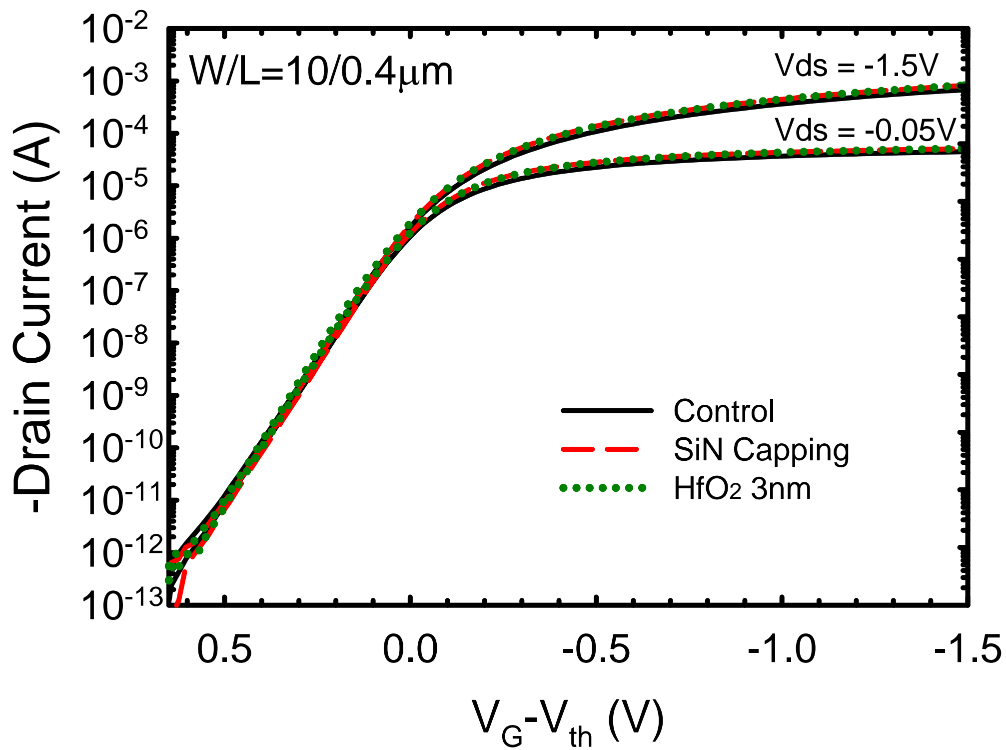

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Fig. 5.7 Subthreshold characteristics of all splits.

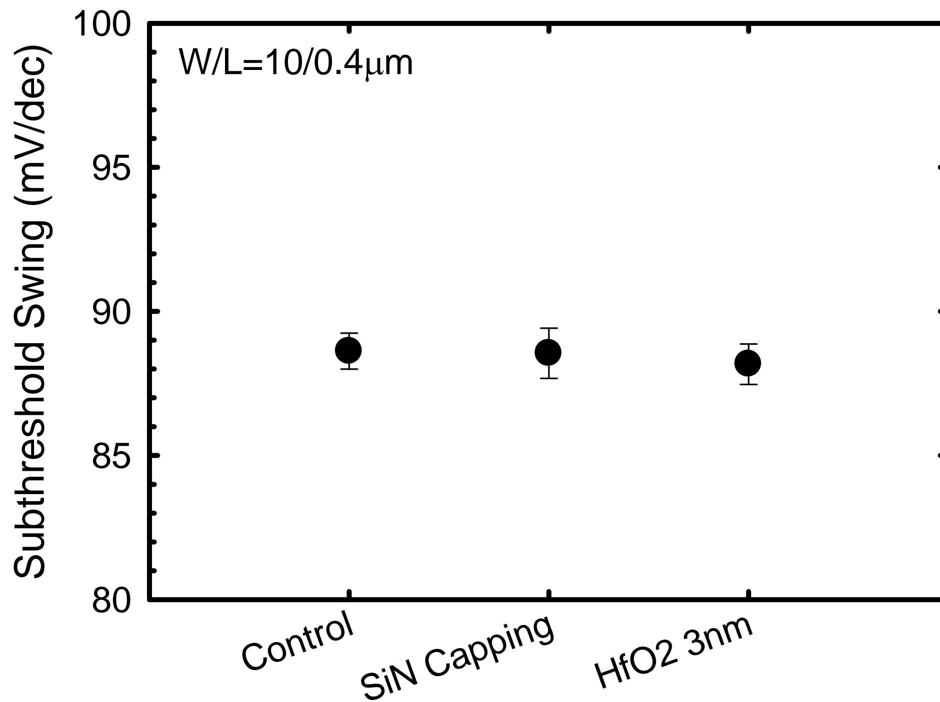

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Fig. 5.8 Subthreshold swing of all splits. We can see that the subthreshold characteristics are not affected by the presence of SiN and HfO_2-buffer layers.

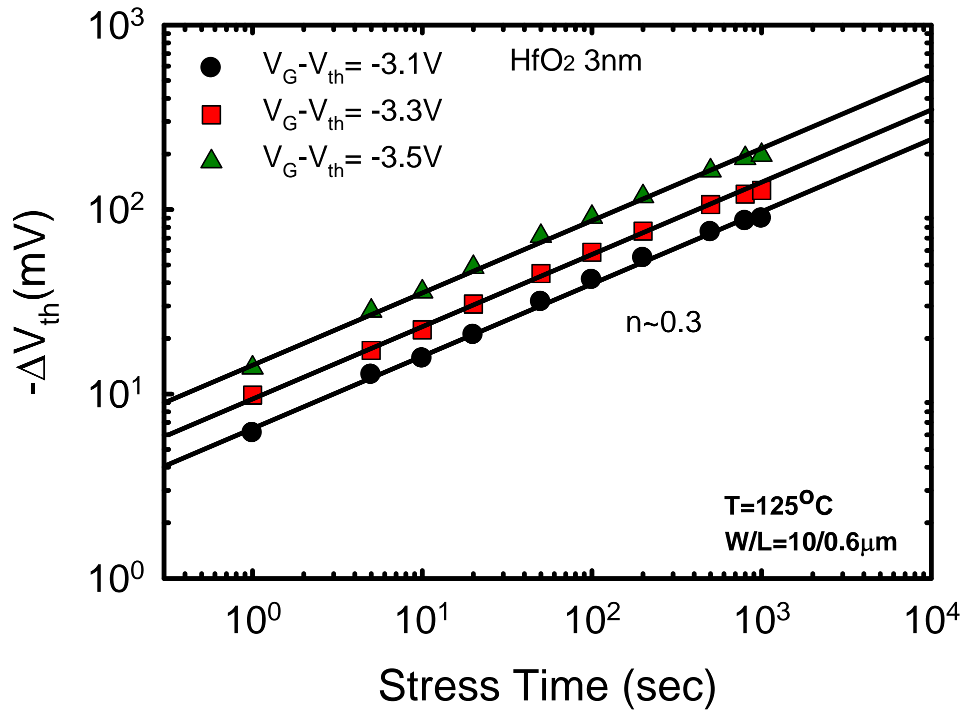

Fig. 5.9 Threshold voltage shift (ΔV_{th}) versus stress time for HfO_2-buffered split under three different gate biases at 125°C.

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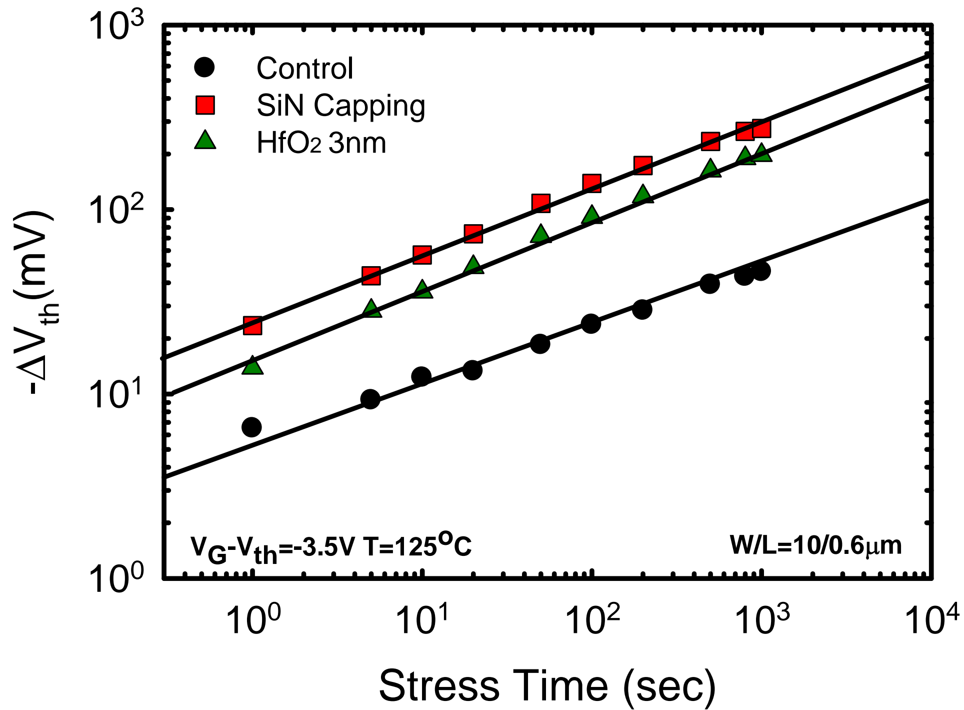

Fig. 5.10 Threshold voltage shift (ΔV_{th}) versus stress time for all three splits with V_G-V_{th} = -3.5 V at 125°C. It is seen that the SiN-capped split depicts much larger ΔV_{th} as compared with the control split. Such degradation is partially relieved when the HfO_2 buffer layer is added.

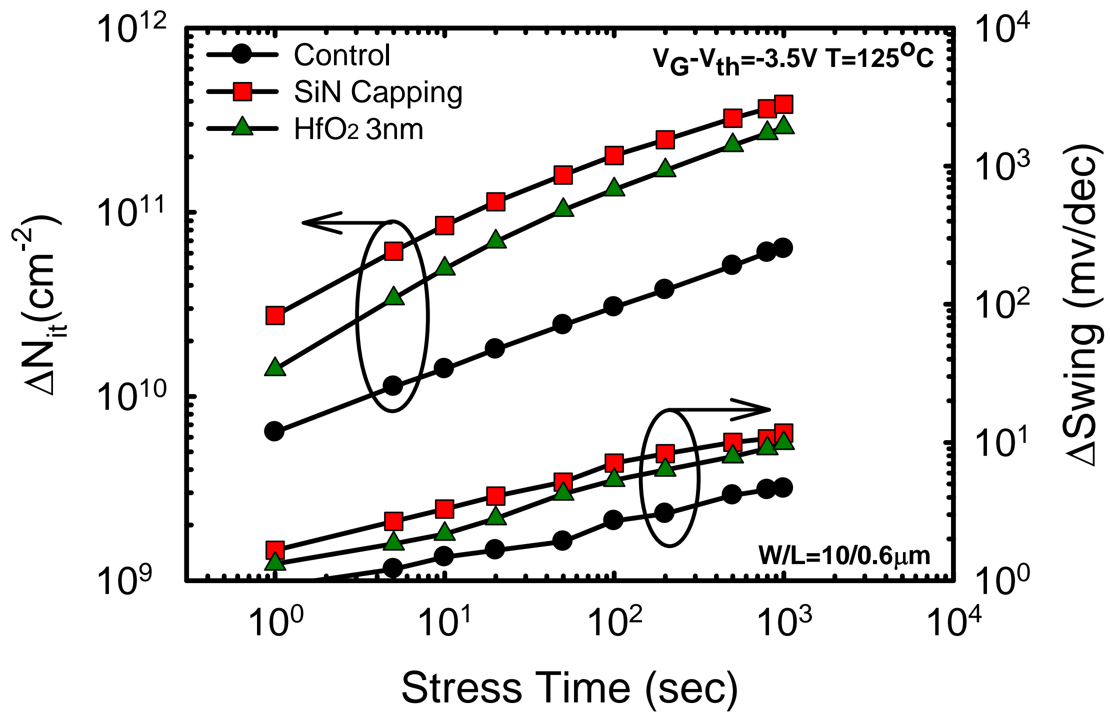

Fig. 5.11 Interface state generation (ΔN_{it}) and subthreshold swing degradation (ΔSwing) versus stress time for all three splits with V_G-V_{th} = -3.5 V at 125°C.

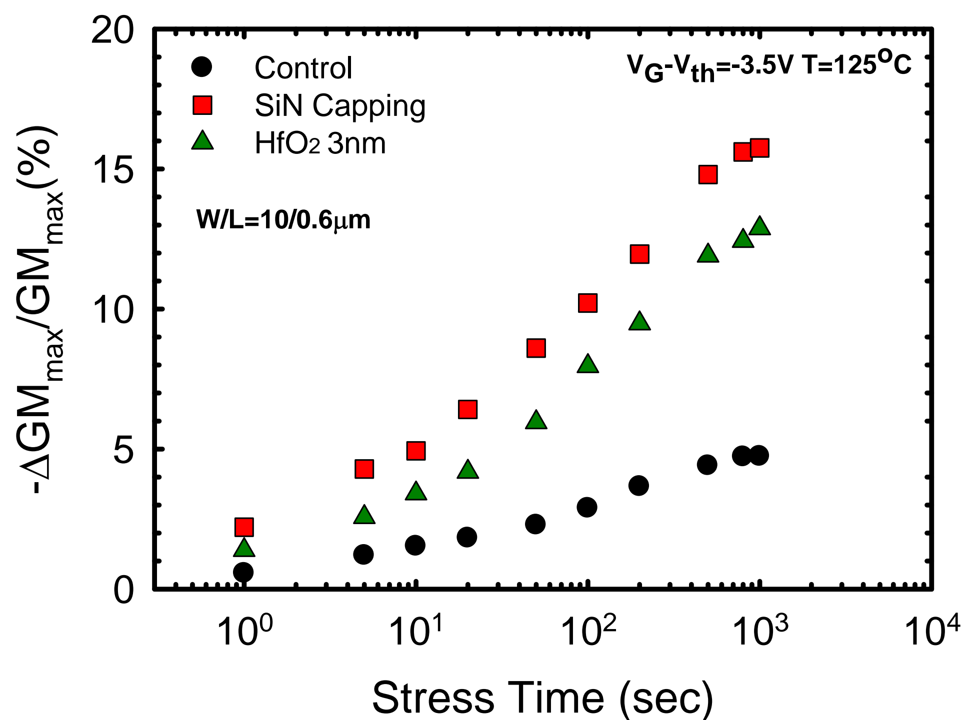

Fig. 5.12 Transconductance degradation versus stress time for all three splits with V_G-V_{th} = -3.5 V at 125°C. The transconductance degradation ratio for SiN-capped split depicts the severest degradation among all three splits, while this degradation is alleviated for HfO_2-buffered split.

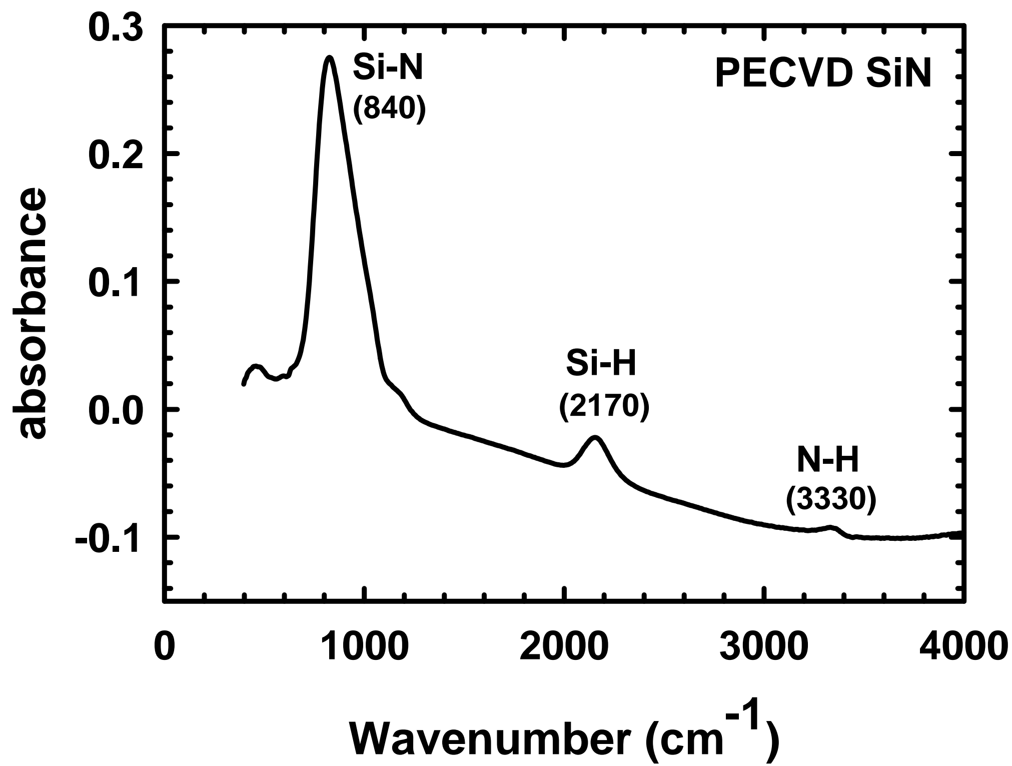

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Fig. 5.13 Bonding signals of PECVD-SiN layer by Fourier transform infrared spectrometer (FTIR). Visible H-bonding signals can be detected, indicating that the SiN film indeed contains a substantial amount of hydrogen.

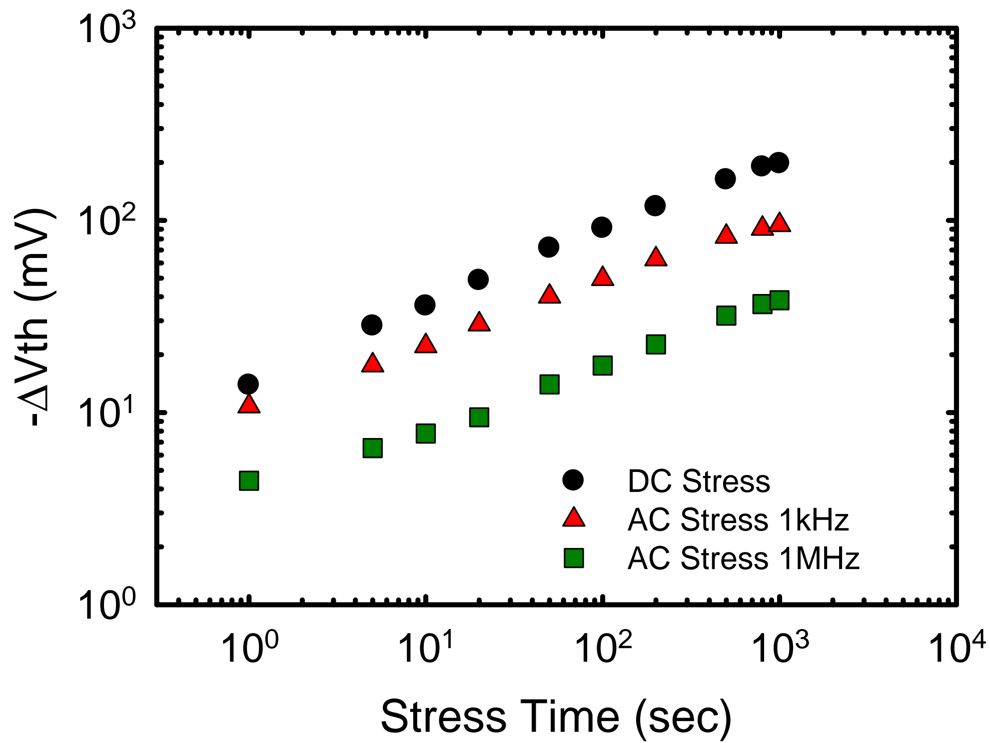


Fig. 5.14 Threshold voltage shift of devices with thin HfO_2 buffer layer, measured at different AC stress frequencies with V_G-V_{th} = -3.5 V at 125°C. It can be seen that Vth depicts less shift at higher frequency.

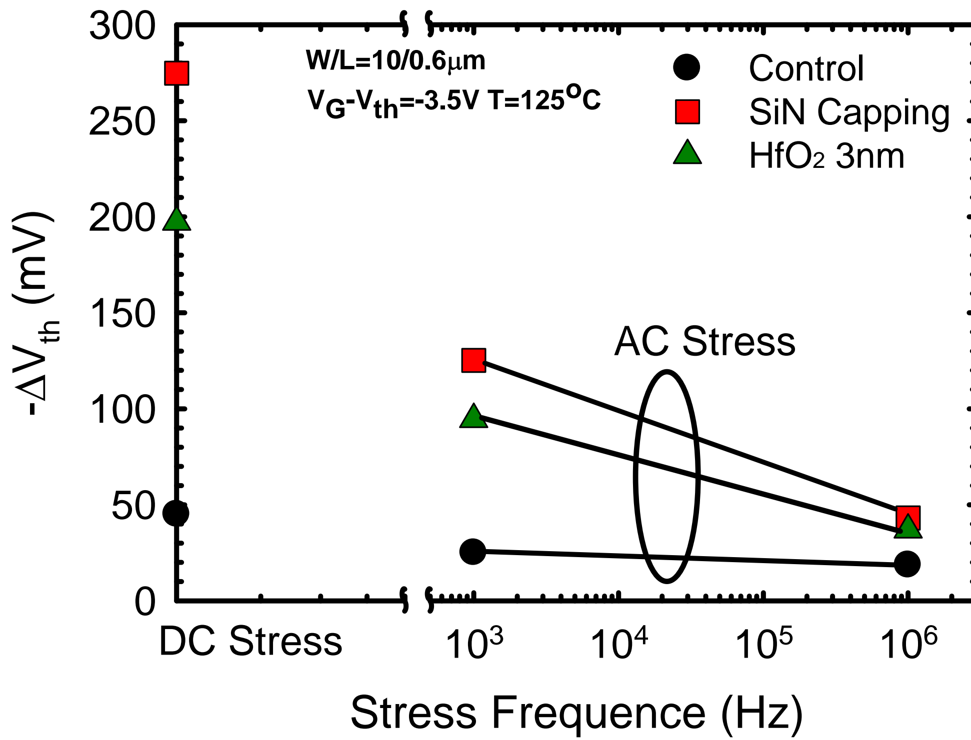


Fig. 5.15 Threshold voltage shift as a function of frequency for devices with different split conditions after V_G-V_{th} = -3.5 V, 1000 sec stress at 125°C.

Chapter 6

Impacts of SiN-Capped NMOSFETs on the Flicker Noise Characteristics

6.1 Introduction

Channel strain engineering with SiN capping technique has emerged as one of the most effective remedies for boosting mobility enhancement in scaled devices [1-10]. Its impacts on the device characteristics and related reliability issues have been demonstrated and investigated [7-10]. However, very few literatures have paid attention to the flicker noise characteristics, which is very important for low frequency analog circuits and rf applications.

The physical origin of flicker noise is described by the carrier number fluctuation theory known also as the trapping-detrapping model, originally proposed by McWhortor [11-13]. The low frequency noise is caused primarily by fluctuation of the number of inversion layer carriers as they are trapped and detrapped in the gate insulator. These fluctuations can also induce fluctuations in the channel mobility since these traps act as Coulomb scattering sites when they capture a carrier, which is also known as the mobility number fluctuation theory based on Hooge's hypothesis [14-16]. Therefore, the traps or interface states are believed to be the major culprits for flicker noise.

In this chapter, we evaluated three types of SiN film deposited with various gas flow conditions and confirm that the SiN deposition condition plays an important role in the flicker noise.

6.2 Devices Fabrication

The NMOSFETs characterized in this study were fabricated on 6-inch p-type (100) Si wafers with conventional local oxidation of silicon (LOCOS) isolation. The 3nm-thick thermal oxide was grown in a vertical furnace, followed by the deposition of a 150nm-thick polycrystalline-silicon (poly-Si) layer to serve as the gate electrode. After source/drain (S/D) doping and the formation of self-aligned spacers, rapid thermal anneal (RTA) was then carried out in a nitrogen ambient at 900°C for 30 sec to activate dopants in the gate and S/D junctions. Afterwards, a 300nm-thick SiN capping layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) system. The schematic structure of the fabricated device is shown in Fig. 6.1. In this chapter, we evaluated devices with three different types of SiN film using $SiH_4/NH_3/N_2$ gas mixtures at 300°C (denoted as SiN-1, SiN-2, SiN-3 splits, respectively). The detailed gas flow rates are listed in Table 6-I, and the major parameter adjusted is the N_2 gas flow rate. Deposition pressure and rf power were fixed at 1 Torr and 100W, respectively. In addition to SiN-capped samples, the control devices with 300nm-thick PECVD oxide were also fabricated for comparison purpose (denoted as oxide split). After contact hole and metallization processes, the processing steps were completed with a forming gas anneal at 400°C for 30 min.

6.3 Flicker Noise Measurement Setup

The experimental setup for measuring low frequency flicker noise is shown in Fig. 6.2. The transistor is coupled to the pre-amplifier and noise analyzer. The output of the pre-amplifier is connected to the dynamic signal analyzer (DSA), which performs sampling and Fast Fourier Transform of the incoming signal and calculates the density spectrum at the frequency of interest. The related setups of measurement parameters,

including the voltage for four terminals (i.e., gate, drain, source, and bulk) and the range of frequency, are controlled by a personal computer (PC), which can work for hours as required for the measurement. In this chapter, the noise measurement was performed in a range of 10 Hz to 1 kHz. In addition, I-V meter was also used to measure the fresh electrical characteristics and check if the test devices have failed during testing.

6.4 Results and Discussion

6.4-1 SiN Film Analysis

X-ray photoelectron spectroscopy (XPS), Fourier transform infrared spectrometer (FTIR) and stress measurement system (Tencor FLX-2320 system) were employed to investigate the material properties of the deposited SiN films. From XPS analysis (Fig. 6.3), we confirmed that SiN-3 split contains the highest nitrogen content among all splits. Obviously the use of higher N_2 flow rate in the deposition process is responsible for the phenomenon. From the analysis of FTIR measurement, an increase in N_2 flow rate would weaken the signal of Si-H bonds [19], as shown in Fig. 6.4. This result implies that SiN-3 split contains less hydrogen content among all splits. In addition, using stress measurement (by measuring the change in curvature of blanket wafer before and after 300nm-thick SiN capping), we confirmed that the stress levels are around 147, 344, and 556 MPa for SiN-1, SiN-2, and SiN-3 splits, respectively. Increasing N_2 flow rate (or nitrogen content in the SiN film) will increase the tensile stress. These results are also summarized in Table 6-I.

6.4-2 Basic Electrical Characteristics

Electrical characteristics were performed using Agilent 4156 system. Figure 6.5 shows the subthreshold characteristics and transconductance (Gm) of NMOSFETs for

all splits of devices with channel width/length (W/L) = 10/0.4 μm. It's well known that the tensile stress improves NMOSFETs performance [1-10], and thus SiN-3 split depicts the largest Gm among all splits. The enhancement ratio reaches about 16% compared with oxide split. Similar trend is also observed in the output characteristics, as shown in Fig. 6.6.

6.4-3 Flicker Noise Characteristics

As mentioned above, the SiN-induced tensile stress plays a major role in enhancing the carrier mobility and therefore changes the dc electrical characteristics. It is also interesting to investigate if these SiN films have any impact on the flicker noise characteristics. Drain current noise spectral density (S_{Id}) and input-referred gate voltage noise spectral density (S_{Vg}) for all splits with W/L = 10/0.6 μm under Vg = 1.5 V and Vd = 0.05 V are shown in Fig. 6.7 and Fig. 6.8, respectively. Based on the carrier number fluctuation theory, known as the trapping-detrapping model originated by McWhorter [11-13], S_{Vg} can be given by

$$S_{V_g} = \frac{S_{Id}}{g_m^2} = \frac{kTq^2}{\gamma C_{ox}^2} \frac{N_{ot}}{WL} \frac{1}{f} \tag{6.1}$$

where C_{ox} is the oxide capacitance per unit area;

γ is the McWhorter tunneling parameter;

f is frequency;

N_{ot} is the oxide trap density per unit volume and unit energy.

The extracted S_{Vg} and N_{ot} at f = 25 Hz for all splits are shown in Fig. 6.9 and Fig. 6.10, respectively. Each datum point represents the mean measurement result form five devices. We can see that all SiN-capping samples have lower S_{Vg} (or N_{ot}) than oxide split, even though SiN-3 split has the highest stress level. In addition, SiN-1 split, which possesses the highest hydrogen content, depicts the lowest S_{Vg}. We believe that

hydrogen content in the SiN film accounts for this result. Traps or interface states are considered to be the cause of the degradation of flicker noise. Extra hydrogen species contained in the SiN may diffuse into the channel region after later thermal cycles [8-10], and thus passivate the defects and dangling bonds near the interface, resulting in lower S_{Vg} for SiN-capped samples, especially for SiN-1 split. To further support this observation, conventional charge pumping measurement with a fixed pulse amplitude of 1.5V at 1 MHz was also performed, and the results are shown in Fig. 6.11. According to the conventional equation [20],

$$I_{cp,\max} = qfN_{it}WL \tag{6.2}$$

where $I_{cp.max}$ is the maximum charge pumping current; N_{it} is the interface state. The extracted N_{it} is shown in Fig. 6.12. It can be seen that indeed the charge pumping results are similar to that of the flicker noise, and the SiN-1 split still depicts the minimum N_{it}.

The S_{Vg} and the extracted N_{ot} at f = 25 Hz for devices with W/L = 10/0.6 μm as a function of Vg are shown in Fig. 6.13 and Fig. 6.14, respectively. We can see that S_{Vg} (or N_{ot}) is independent of Vg between Vg = 0.4 V to 0.7 V. Therefore, in this operation region, flicker noise characteristics can be modeled reasonably by only using carrier number fluctuation theory. However, when Vg is above 0.8 V, S_{Vg} exhibits pronounced dependence on Vg and increases with Vg. To model the noise in this gate-bias regime, the mobility fluctuation theory should be applied. The unified model proposed by K. K. Hung [17-18], taking into consideration of both carrier number fluctuation theory and mobility fluctuation theory, can be given by

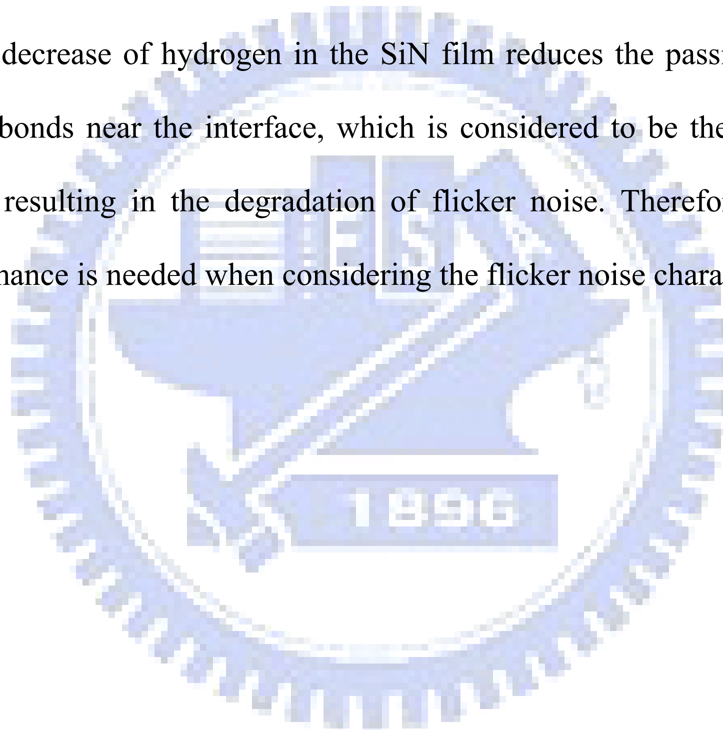
$$S_{Vg} = \frac{kTq^2 N_{ot}}{\gamma fWLC_{ox}^2}(1+\alpha\mu_0 C_{ox}(Vg - V_{th}))^2 \tag{6.3}$$

where α is the Coulomb scattering coefficient; μ_0 is the low-field carrier mobility.

In this operation region, the α, μ_0, and Vg need to be also taken into account.

6.5 Summary

In this chapter, we have fabricated strained-channel NMOSFETs with three types of SiN film, and the impacts of the SiN capping layer on the flicker noise characteristics were investigated. We found that increasing N_2 flow rate in the SiN deposition process will increase the tensile stress of SiN film and weaken the signal of Si-H bonds, which is beneficial for NMOSFETs' performance and hot-carrier reliability [10], respectively. However, the decrease of hydrogen in the SiN film reduces the passivation of defects and dangling bonds near the interface, which is considered to be the main culprit for flicker noise, resulting in the degradation of flicker noise. Therefore, a trade-off in device performance is needed when considering the flicker noise characteristics.



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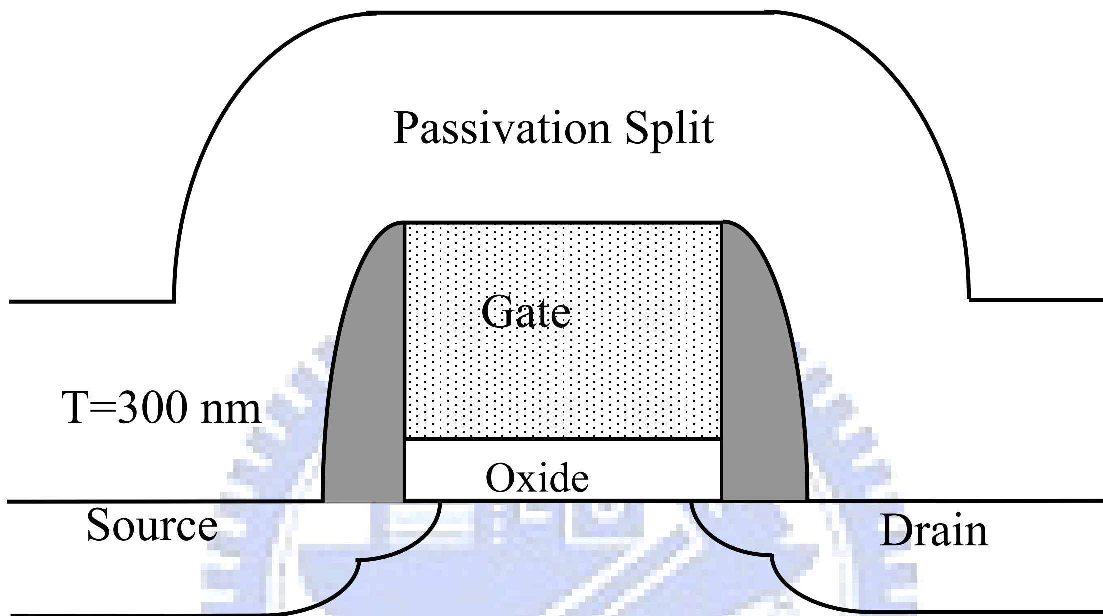
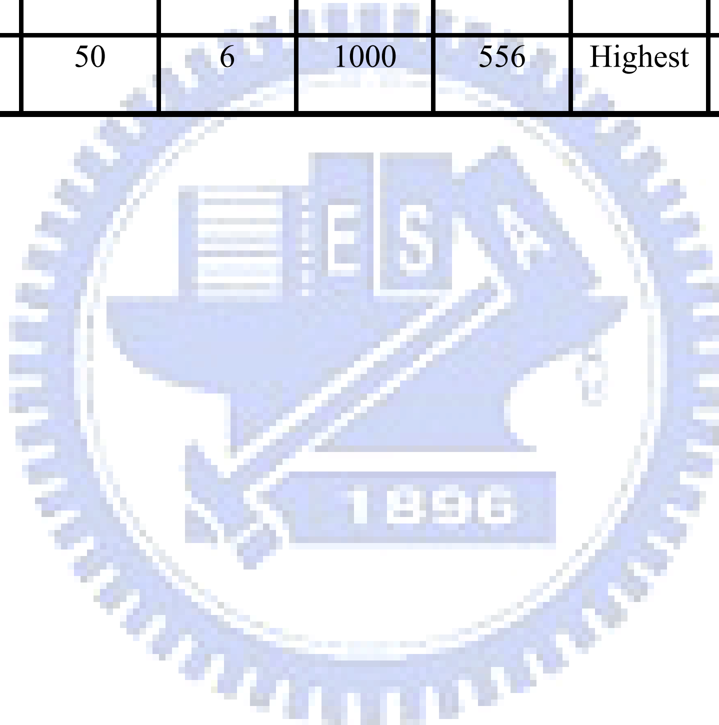


Fig. 6.1 Schematic structure of the fabricated device with different types of passivation. The thickness is fixed at 300 nm.

Table 6-I Precursor flow and SiN film properties. [1]Determined form the XPS results; [2]from the FTIR results

	SiH_4 (sccm)	NH_3 (sccm)	N_2 (sccm)	Stress (MPa)	N content[1]	Si-H signal[2]
SiN-1	50	6	50	147	Lowest	Highest
SiN-2	50	6	100	344	Medium	Medium
SiN-3	50	6	1000	556	Highest	Lowest



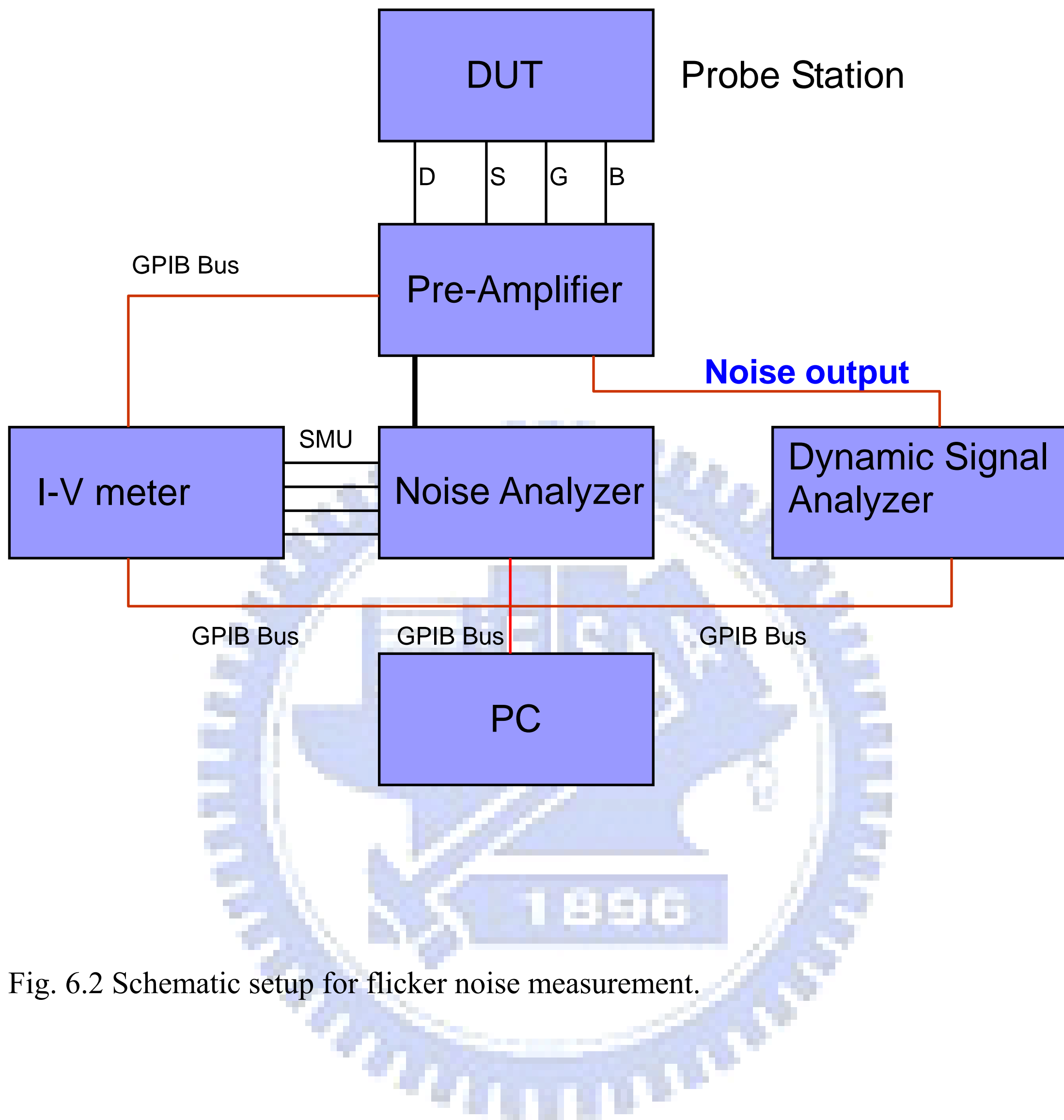


Fig. 6.2 Schematic setup for flicker noise measurement.

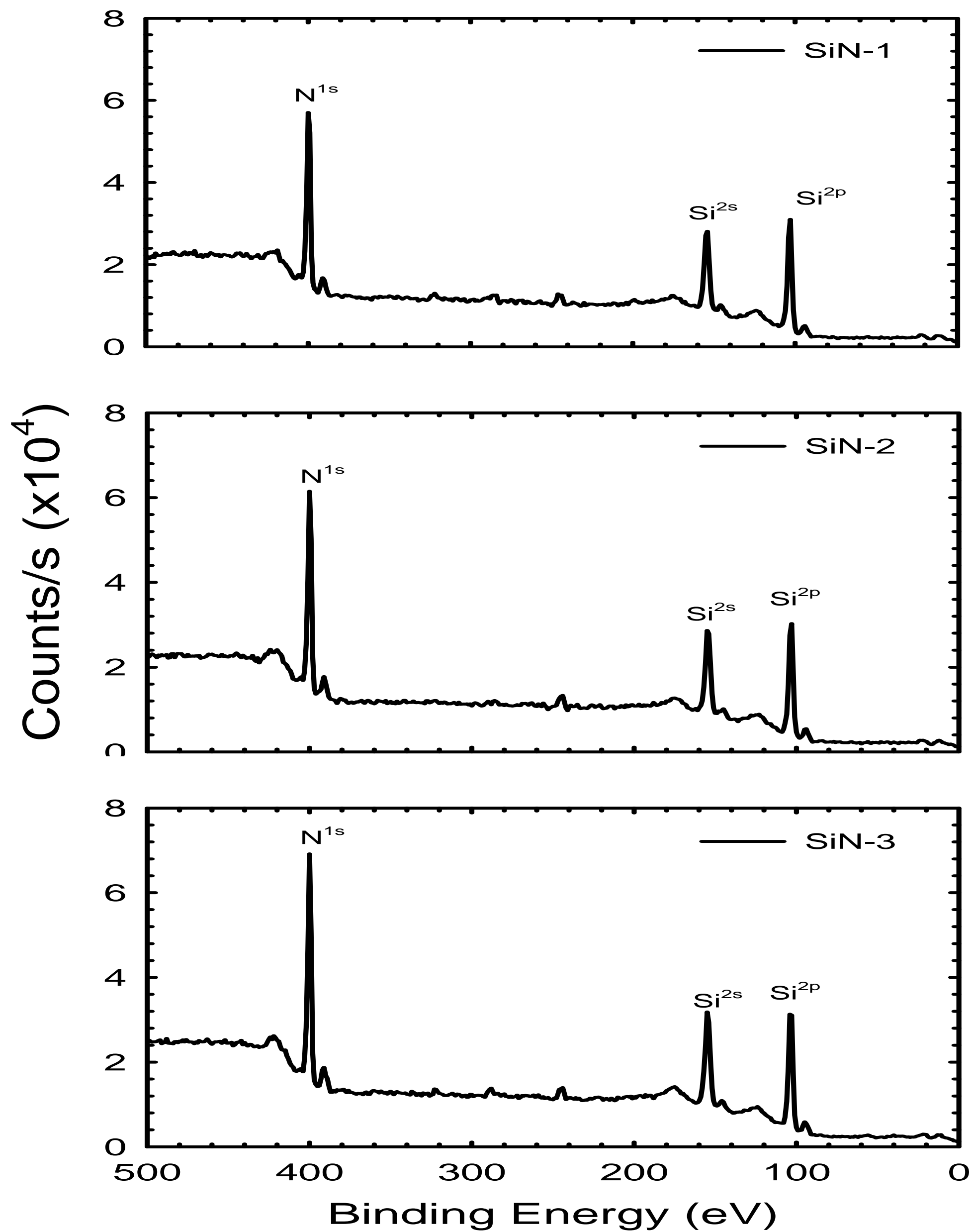


Fig. 6.3 Results of XPS analysis, indicating that the SiN-3 split contains the highest N content among all splits, owing to the use of the highest N_2 flow rate in the deposition process.

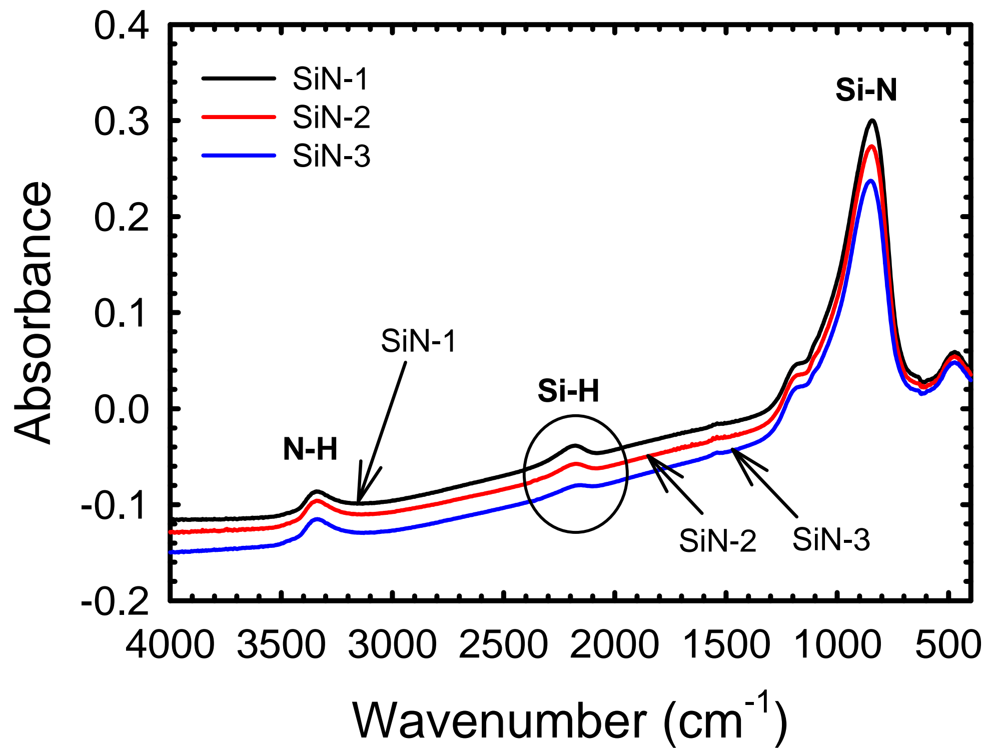


Fig. 6.4 Results of FTIR analysis, indicating that the SiN-1 split contains the highest number of Si-H bonds among all splits. Increase in N_2 flow rate tends to weaken the signal of Si-H bonds.

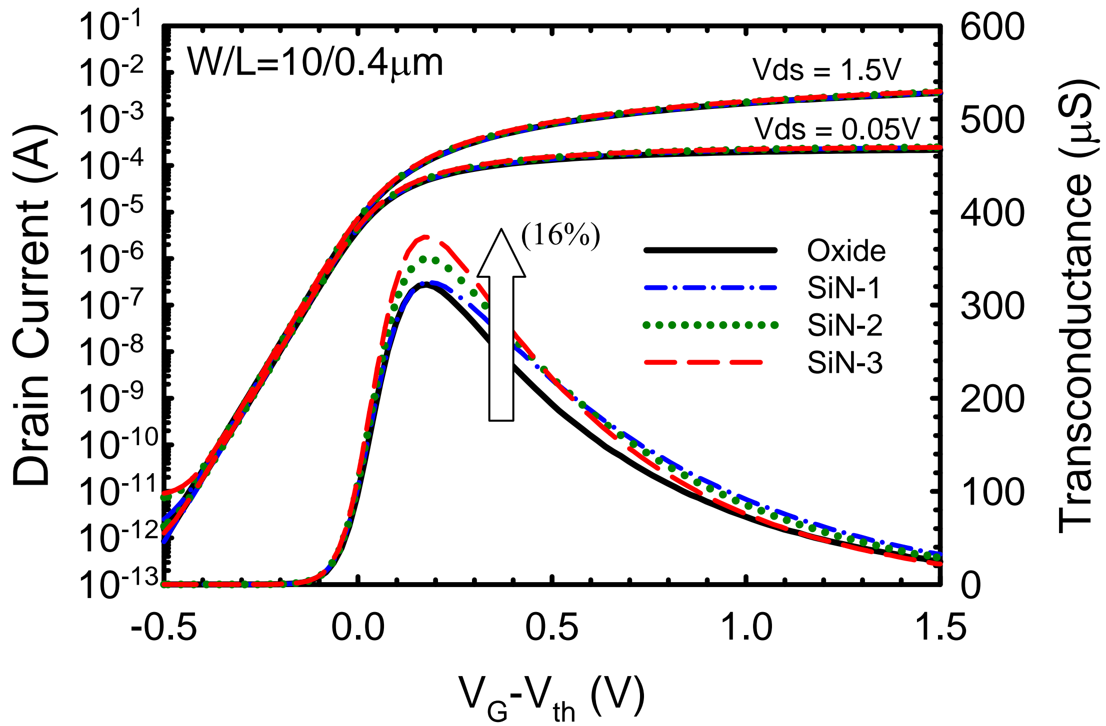


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Fig. 6.5 Subthreshold characteristics and transconductance (Gm) of the fabricated NMOSFETs for all splits.

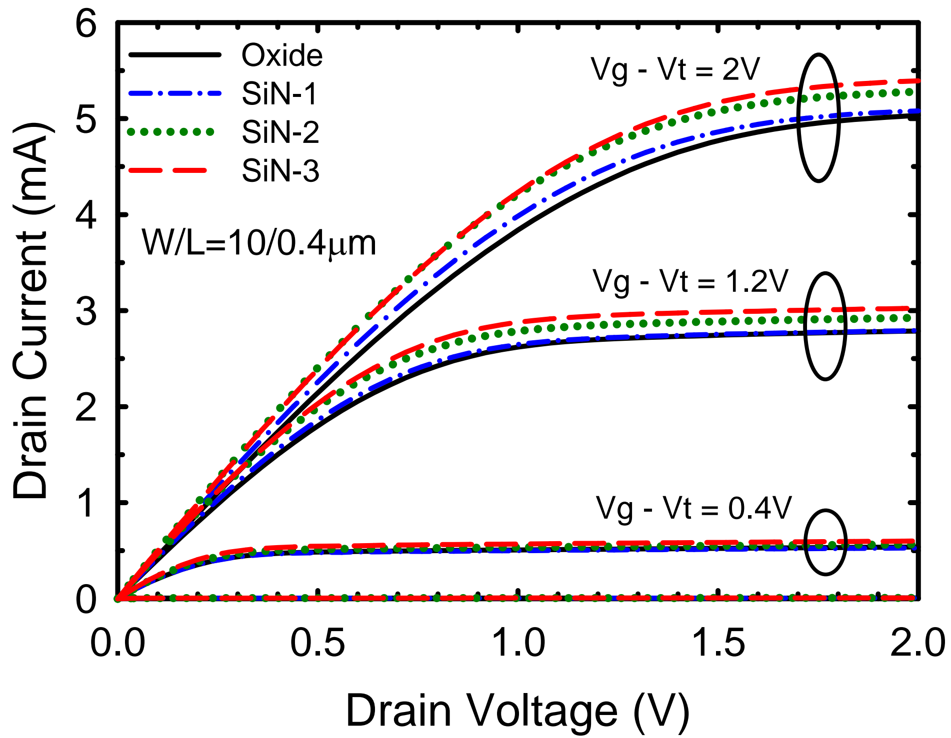

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Fig. 6.6 Output characteristics of NMOSFETs for all splits.

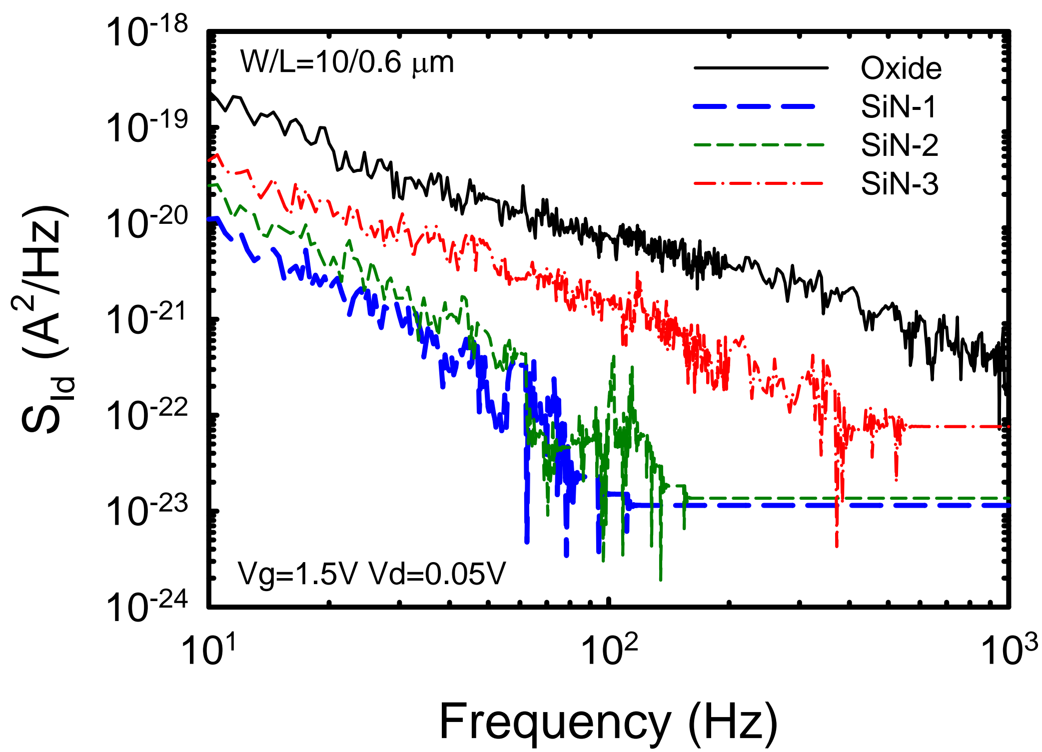

Fig. 6.7 Drain current noise spectral density (S_{Id}) for all splits with W/L = 10/0.6 μm under Vg = 1.5 V and Vd = 0.05 V.

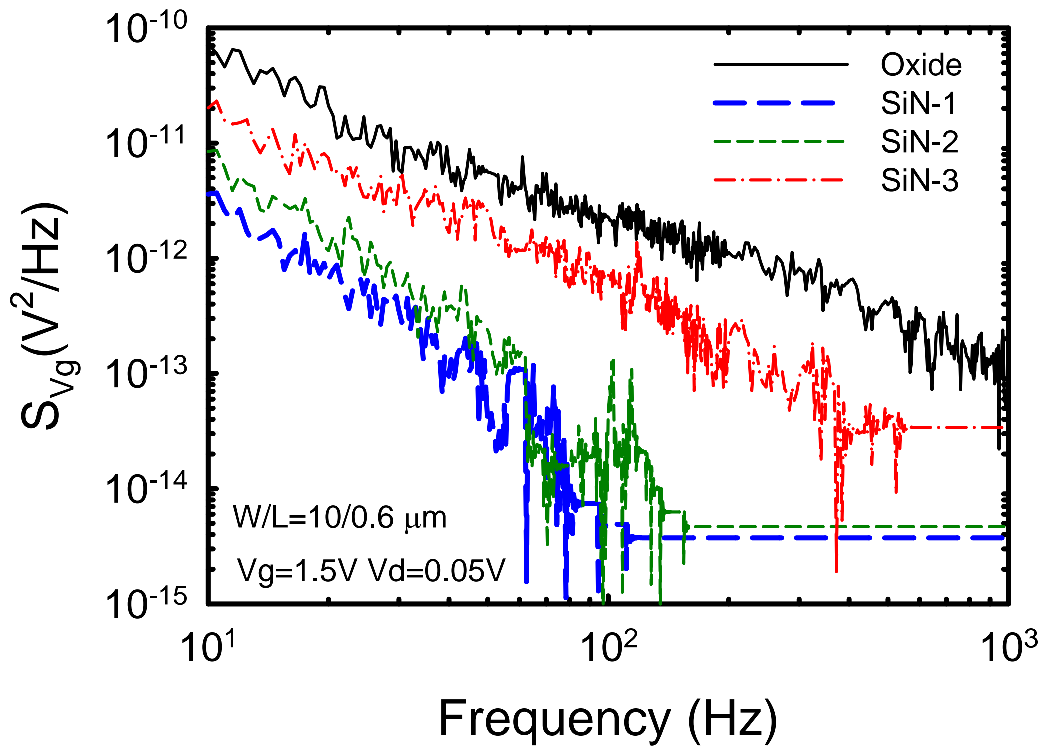

Fig. 6.8 Input-referred gate voltage noise spectral density (S_{Vg}) for all splits with W/L = 10/0.6 μm under Vg = 1.5 V and Vd = 0.05 V.

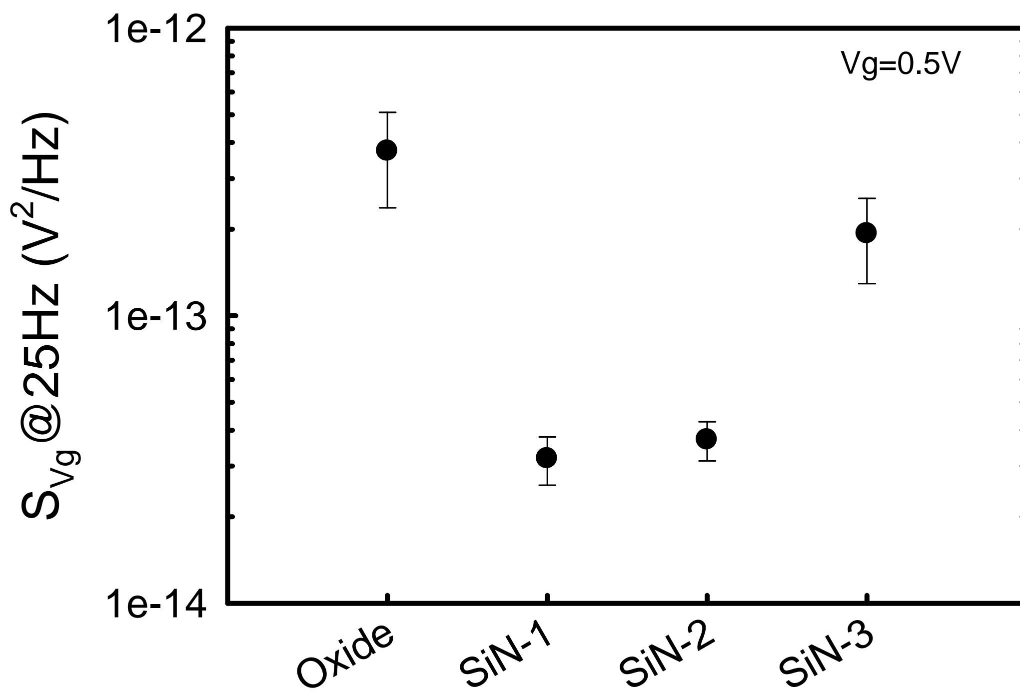

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Fig. 6.9 S_{Vg}@25 Hz for all splits under Vg = 0.5 V and Vd = 0.05 V. Each datum point represents the mean measurement result from five devices.

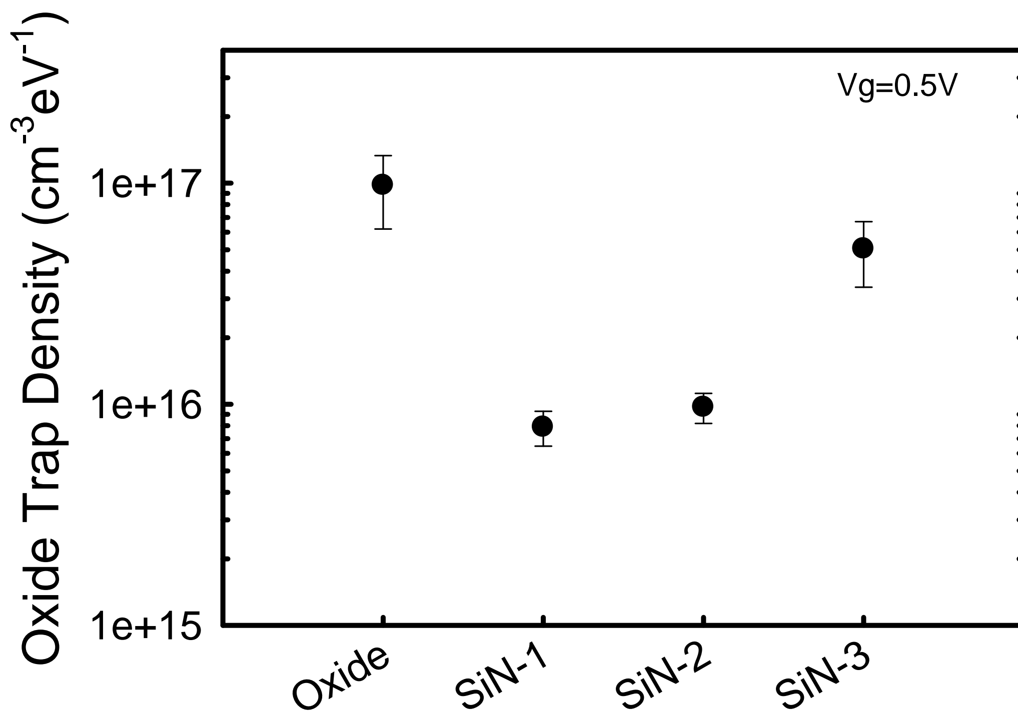


Fig. 6.10 Extracted oxide trap density (N_{ot}) for all splits. Each datum point represents the mean measurement result from five devices.

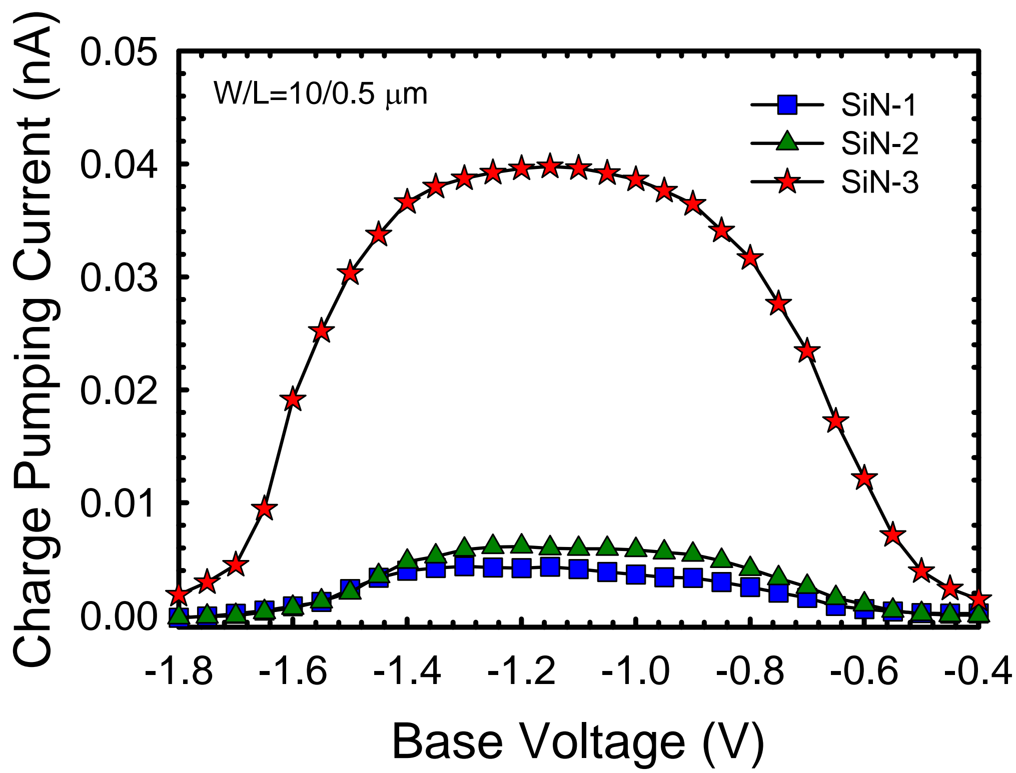
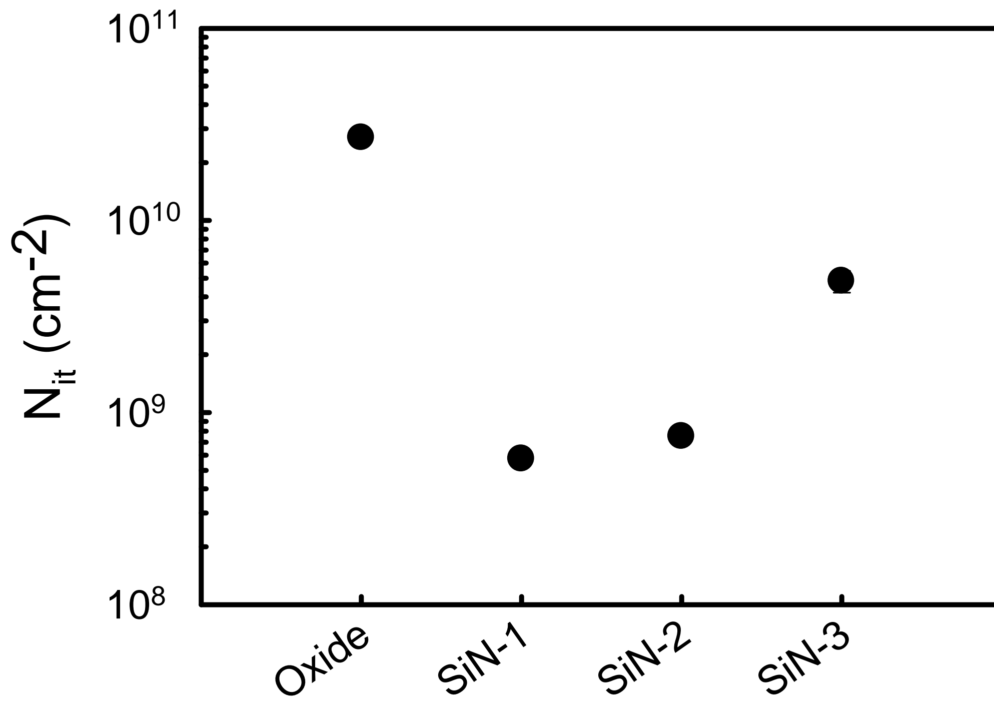


Fig. 6.11 Charge pumping current for SiN splits with pulse amplitude of 1.5V and f = 1 MHz.



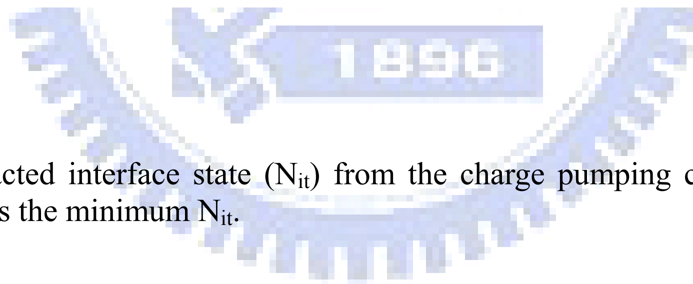


Fig. 6.12 Extracted interface state (N_{it}) from the charge pumping current. The SiN-1 split still depicts the minimum N_{it}.

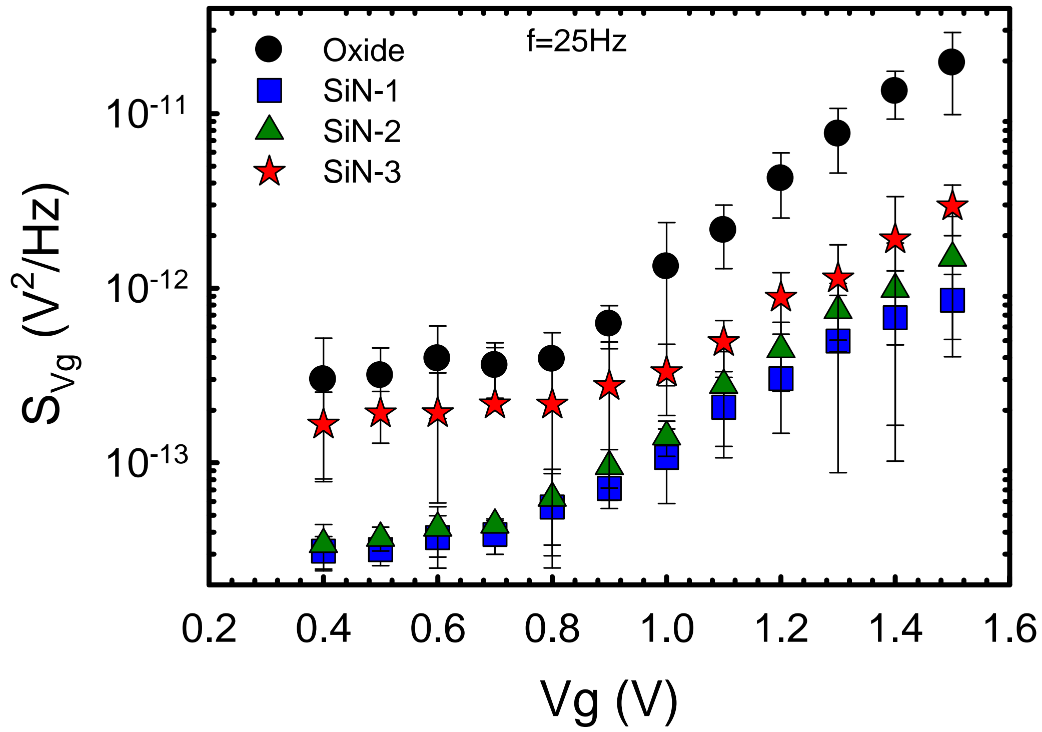


Fig. 6.13 Input-referred gate voltage noise spectral density (S_{Vg}) as a function of gate voltage at Vd = 0.05 V and f = 25 Hz.

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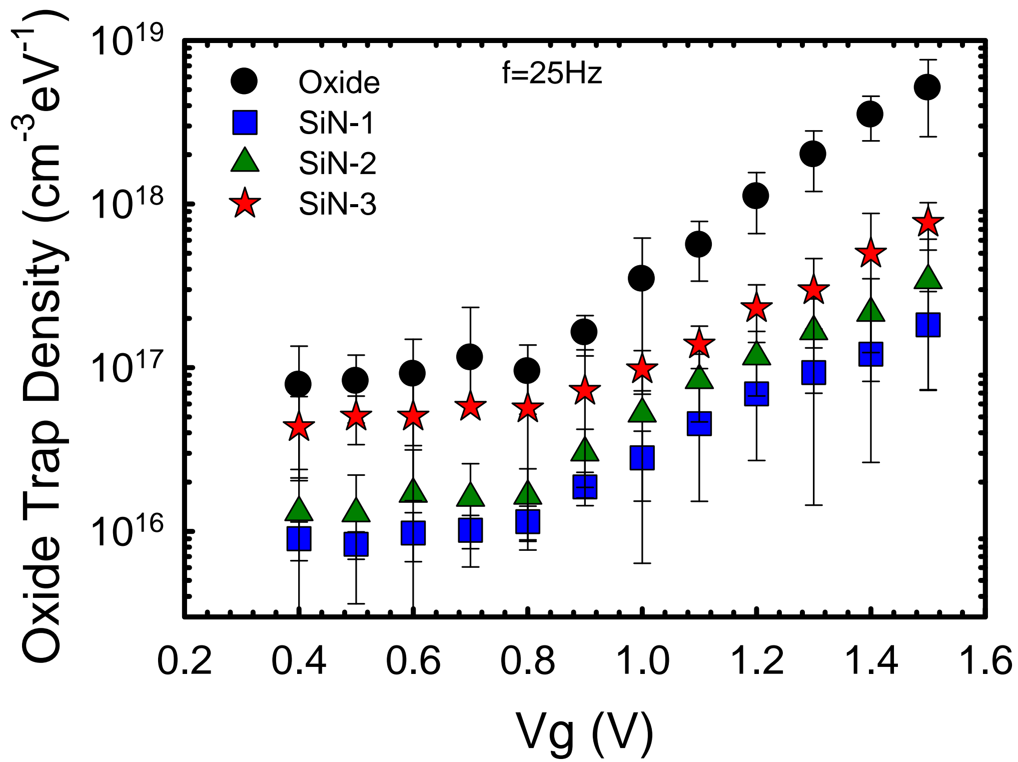

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Fig. 6.14 Extracted oxide trap density (N_{ot}) as a function of gate voltage at Vd = 0.05 V and f = 25 Hz.

Chapter 7

Conclusions and Suggested Future Works

7.1 Conclusions

In this dissertation, various strained n- and p-channel MOSFETs with SiN capping were fabricated successfully by using the novel scheme of buffer layer, adjusting SiN deposition conditions, and changing the thickness of SiN capping layer. The characteristics and related reliability issues were also investigated, including the mobility enhancement by SiN capping, bandgap narrowing effect, off-state leakage current mechanism, the improvement of hot-carrier and NBTI reliabilities, the lateral distribution of interface state after hot-carrier stress, and the impacts of AC stress on the NBTI reliability. Finally, we have also investigated the influence of low frequency flicker noise characteristics on the SiN-capped devices. Several important results were obtained and summarized as follows:

1. In Chapter 2, the effects of LPCVD SiN capping and the associated deposition process on the device performance and hot-carrier degradation were investigated in this work. A novel scheme involving the insertion of a buffer layer between the SiN and the gate for improving the device reliability was proposed and demonstrated. We found that the 20nm-thick buffer layer does not compromise the mobility enhancement due to the SiN capping, while the device performance enhancement starts to diminish if the thickness of the buffer layer exceeds 30nm. The accompanying bandgap narrowing effect and the increased carrier mobility tend to worsen the hot-carrier reliability. This work confirms that hot-carrier degradation is adversely affected when the SiN layer is deposited over the gate,

even if the SiN layer is removed later and the channel strain is relieved. Abundant hydrogen species incorporated into the channel region during the SiN deposition process, owing to the use of hydrogen-containing precursors, is the primary culprit for aggravated reliability. By blocking the diffusion of hydrogen species, the devices with 20nm-thick TEOS buffer layer can effectively improve the hot-carrier reliability without degrading the performance enhancement.

2. In Chapter 3, we have fabricated strained n- and p-channel MOSFETs with different types of SiN capping by varying the N_2 flow rate and deposition temperature during the deposition step. Tensile stress is found to increase with increasing N_2 flow rate, therefore boosting the NMOS device performance, especially for short-channel devices. However, the tensile stress would degrade PMOS device performance. On the other hand, we found that the robustness of the device to hot-carrier degradation and NBTI reliability is mainly affected by the hydrogen content, rather than the stress level. Therefore, SiN film with high tensile stress but low hydrogen content is ideally suitable for NMOSFETs, and nitrogen-rich film can fulfill the requirement.

3. In Chapter 4, we have fabricated strained-channel NMOSFETs with different tensile stress by adjusting the SiN thickness. Tensile stress is found to increase by increasing the SiN thickness, and thus enhancing the device performance, especially for short-channel devices. However, the off-state leakage current is also increased by the tensile stress. We demonstrate that GIDL current is the major reason for increased off-state leakage current. Bandgap narrowing induced by tensile stress would enhance the band-to-band tunneling process, thus resulting in

GIDL current increase. On the other hand, the hot-carrier reliability is also degraded owing to the increase in mobility and the use of hydrogen-containing precursors during the SiN deposition. How to deposit highly tensile SiN film but with low hydrogen content is therefore essential to the implementation of uniaxial channel strain in MOS devices.

4. In Chapter 5, SiN-capped PMOSFETs with a thin HfO_2 buffer layer were fabricated and characterized. Although the SiN layer tends to worsen the NBTI characteristics, our results demonstrate the usefulness of inserting a buffer layer in relieving the situation. Furthermore, no performance gain from the channel strain is compromised at all as the thin buffer layer is inserted. Such improvement is ascribed to the suppression of hydrogen diffusion from the SiN to the gate oxide and the oxide/channel interface with the insertion of the buffer layer.

5. In Chapter 6, we have fabricated strained-channel NMOSFETs with three types of SiN film, and the impacts of the SiN capping layer on the flicker noise characteristics were investigated. We found that increasing N_2 flow rate in the SiN deposition process will increase the tensile stress of SiN film and weaken the signal of Si-H bonds, which is beneficial for NMOSFETs' performance and hot-carrier reliability, respectively. However, the decrease of hydrogen in the SiN film reduces the passivation of defects and dangling bonds near the interface, which is considered to be the main culprit for flicker noise, resulting in the degradation of flicker noise. Therefore, a trade-off in device performance is needed when considering the flicker noise characteristics.

7.2 Suggestions for Future Work

There are some interesting and important topics that are valuable for the future research regarding the strained-channel devices with SiN capping:

1. In Chapter 2, hydrogen species generated during the SiN deposition process are the major culprit for the hot-carrier degradation. Several possible pathways, such as Path A1, A2, and A3, for hydrogen diffusion into the channel region have been proposed. How to identify the influence of these paths individually on the device reliability by designing experiments to develop device structure and process splits is suggested for future work. In addition, it is also suggested to develop new buffer-layer materials for further improving the device reliability.

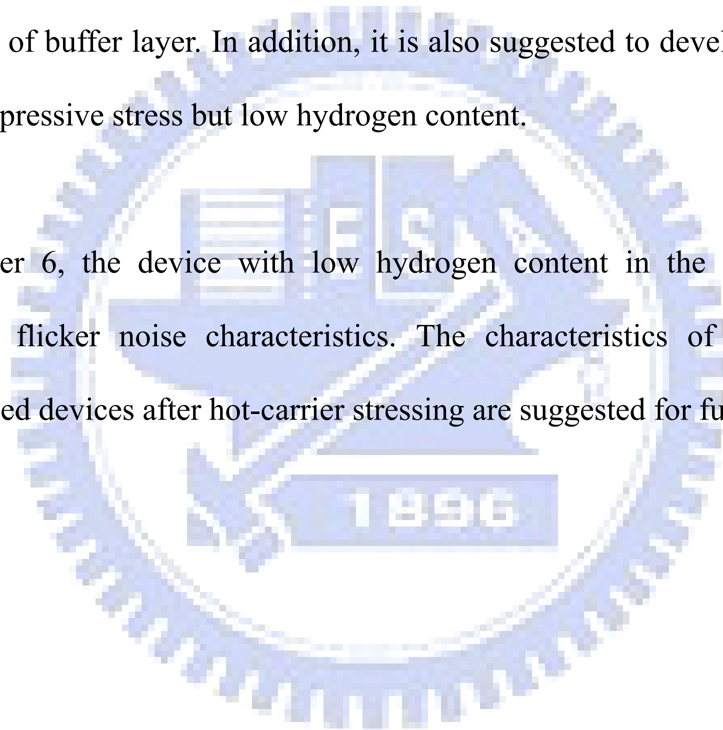
2. In Chapter 3, we found that SiN film with low hydrogen content is suitable for n- and p-channel MOSFETs. How to achieve large tensile stress while maintaining low hydrogen content by optimizing SiN deposition conditions is suggested for future work. However, SiN film with compressive stress is not studied in this chapter. Future research is suggested to develop SiN film with high compressive stress but low hydrogen content, which is beneficial for the performance and the NBTI reliability of PMOSFETs. Moreover, adding a thin buffer layer before capping the optimized SiN film may be the best solution for SiN-capped strained-channel MOSFETs.

3. In Chapter 4, the four leakage currents of source, drain, gate, and bulk terminals are individually analyzed, and we demonstrate qualitatively that the increase in GIDL current, which is enhanced by tensile stress owing to the bandgap narrowing

effect, is responsible for the increase in drain leakage current. Further, we need to analyze quantitatively the influence of stress on the leakage current. Simulating the distribution of stress in the channel region, and building a leakage current transport model, in which the local stress level is taken into consideration, are suggested for future work.

4. In Chapter 5, future research is suggested to use other buffer-layer materials, such as Al_2O_3, Hf-silicate film, as well as other insulators, and to find the optimum thickness of buffer layer. In addition, it is also suggested to develop SiN film with high compressive stress but low hydrogen content.

5. In Chapter 6, the device with low hydrogen content in the SiN film depicts degraded flicker noise characteristics. The characteristics of flicker noise of SiN-capped devices after hot-carrier stressing are suggested for future research.



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博士論文題目：

具有氮化矽覆蓋之形變通道金氧半場效電晶體特性與相關可靠性問題研究

A Study on Characteristics and Reliability Issues of Strained Channel MOSFETs with SiN Capping

著 作 目 錄

A. International Journal：

[1] **Ching-Sen Lu**, Horng-Chih Lin, Jian-Ming Huang, Chia-Yu Lu, Yao-Jen Lee, and Tiao-Yuan Huang, ”Impacts of LP-SiN Capping Layer and Lateral Distribution of Interface Trap on Hot Carrier Stress of NMOSFETs”, ***Jpn. J. Appl. Phys.***, vol. 46, no. 4B, pp. 2027-2031, 2007.

[2] **Ching-Sen Lu**, Horng-Chih Lin, and Yao-Jen Lee, “Improvement of Negative-Bias-Temperature Instability in SiN-Capped p-Channel Metal-Oxide-Semiconductor Field-Effect Transistors Using Ultra-thin HfO_2 Buffer Layer,” ***J. Electrochem. Soc.***, vol. 154, no. 12, pp. H1036-H1040, 2007.

[3] **Ching-Sen Lu**, Horng-Chih Lin, and Tiao-Yuan Huang, “Impacts of SiN Deposition Parameters on N-Channel Metal-Oxide-Semiconductor Field-Effect-Transistors,” ***Solid-State Electronics***, vol. 52, no. 10, pp. 1584-1588, 2008.

B. International Letter：

[1] **Ching-Sen Lu**, Horng-Chih Lin, Jian-Ming Huang, and Yao-Jen Lee, “Impacts of a Polycrystalline-Silicon Buffer Layer on the Performance and Reliability of Strained n-Channel Metal-Oxide-Semiconductor Field-Effect-Transistors with SiN Capping,” ***Appl. Phys. Lett.***, vol. 90, no. 12, pp. 122110, 2007.

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C. International Conference：

[1] **Ching-Sen Lu**, Chih-Cheng Chao, Chia-Yu Lu,Yao-Jen Lee, Horng-Chih Lin, and Tiao-Yuan Huang, “The Effect of Hydrogen Species on the Performance and Reliability of PMOS Transistors with $Si_{1-x}Ge_x$ Gate,” ***Int. Electron Devices and Materials Symp. (IEDMS)***, pp. 395-396, 2006.

[2] **Ching-Sen Lu**, Horng-Chih Lin, Yao-Jen Lee, and Tiao-Yuan Huang, “Improvement of Hot Carrier Reliability of Strained-Channel NMOSFETs with a TEOS Buffer Layer,” ***Proc. IEEE Int. Reliability Phys. Symp. (IRPS)***, pp. 670-671, 2007.

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[6] **Ching-Sen Lu**, Horng-Chih Lin, and Tiao-Yuan Huang, "Optimization of SiN Film by Varying Precursor Flow Conditions and its Impacts on Strained Channel MOSFETs," ***Proc. IEEE Int. Conf. on Electron Devices and Solid-State Circuits (EDSSC)***, pp. 117-120, 2007.

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[9] Chia-Yu Lu, Yu-Lin Hsieh, **Ching-Sen Lu**, Yao-Jen Lee, Horng-Chih Lin, and Tiao-Yuan Huang, "The Application and Impact of LPCVD SiN-Capping on NMOSFET's Performance and Reliability," ***Int. Electron Devices and Materials Symp.*** (***IEDMS***), pp. 290-291, 2006. **(Superior Award)**

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D. Local Conference：

[1] **Ching-Sen Lu**, Horng-Chih Lin, Yao-Jen Lee, and Tiao-Yuan Huang, "Improved Hot-Carrier Reliability in SiN-Capped NMOSFETs with Poly-Si Buffer Layer," ***Symp. on Nano Device Technology (SNDT)***, T6-4, pp. 78, 2007. **(Superior Award)**

[2] **Ching-Sen Lu**, Yu-Hang Chen, Horng-Chih Lin, Yao-Jen Lee, and Tiao-Yuan Huang, "Off-State Leakage Current Mechanisms of SiN-Capped NMOSFETs," ***Symp. on Nano Device Technology (SNDT)***, ND-08, pp. 27, 2008. **(Bonze Paper Award)**

E. Local Journal：

[1] **盧景森**, 林鴻志, "具有緩衝層之氮化矽覆蓋形變矽通道（Strained Si channel）互補式金氧半(CMOS)元件之特性影響與相關可靠度分析," ***電子月刊***, vol. 146, pp. 152-161, 2007.