不同前處理對二氧化鉿閘極介電層在電特性上的影響

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摘 要

在先進的互補金氧半技術中,元件尺寸快速的微縮使二氧化矽厚度縮小到不到 1.2 奈米。而極薄的二氧化矽介電層將伴隨著極大的直接穿遂漏電流，而這個直接穿遂漏電流將對元件的功率消耗有嚴重的影響。在閘極二氧化矽介電層薄到 10 奈米以下的情況之下，為了解決這嚴重的直接穿遂漏電流現象，我們將利用高介電係數材料來替換傳統的二氧化矽。我們利用高介電係數材料在相同的等效二氧化矽厚度之下，能擁有較大的實際物理厚度以抵擋直接穿遂漏電流，而且可以維持元件操作所須的閘極電容。

在眾多高介電係數材料之中，二氧化鉿是一種非常有潛力的高介

電係數材料。它有較高的介電係數，足夠高的載子能障（對電子而言為 1.6 電子伏特，對電洞而言為 3.2 電子伏特），以及在製程上能有著良好的穩定性。但是由於材料本身的基本特性，二氧化鉿中的氧氣容易和底下的矽基板產生介電常數較低的物質，這會對元件的微縮能力及電性有很大的影響。所以在實驗中，我們利用氨氣及一氧化二氮高密度電漿來處理矽基板表面，形成一層薄的含氮的界面層，來探討和一般傳統的二氧化矽界面層或直接沉積在矽基板上在電性以及可靠度上的差異，結果顯示經過高密度電漿處理過後的矽表面會有損害，漏電流仍然未達到我們要的標準，必須經由傳統的快速升溫回火來修補這些損害，所以修補後呈現出較小的漏電流、較小的磁滯、較小的頻率分散、較大的崩潰電壓。而就可靠度來說，經由氨氣電漿處理的試片會有最大的崩潰時間、崩潰電荷，以及最好的特性存活時間，所以用氨氣來作為表面處理的氣體是很好的選擇！

我們發現對於由氮化鈦作為電極的電容，在二氧化鉿薄膜裡面主要的捕捉電荷機制是電洞捕捉而不是電子捕捉。而這種行為可以用捕獲面積模型來適當敘述。特別的是，平帶電壓平移是由於陷阱填補而不是陷阱產生.而電洞捕捉為主要機制可以歸因於電洞由基板注入的機率遠大於電子由閘極注入的機率而這是因為氮化鈦電極的功函數造成電洞具有較短的穿透路徑。

我們也發現在二氧化鉿薄膜內的陷阱是「潛在的」，電流隨溫度的變化較小，但是經由一段時間的電壓壓迫，這些陷阱就會被活化而顯現出來，而表現出的電流機制主要以 Frankel-Poole 為主。而我們把這些陷阱再次填滿，電流隨溫度的變化又變小許多！

The Effects of Various Pre-treatments on the Electrical Properties of HfO_2 Gate Dielectrics

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Abstract

Aggressive device scaling has led to thin (i.e., not more than 1.2 nm) silicon dioxide (SiO_2) gate dielectric in state-of-the-art CMOS technologies. As a result, static leakage power due to direct tunneling through the gate oxide has been increasing at an exponential rate. As technology roadmaps call for sub-10Å gate oxides within the next five years, a variety of alternative high-*k* materials are being investigated as possible replacements for SiO_2. The higher dielectric constant in these materials allows the use of physically thicker films, potentially reducing the tunneling current while maintaining the gate capacitance needed for scaled device operation.

Hafnium oxide (HfO_2) is one of the most potential high-*k* materials. It has a high dielectric constant, high barrier height (1.6eV for electrons, and 3.2eV for holes), and excellent stability. But due to its material properties, the oxygen in HfO_2 easily reacts

with Si substrate and forms a low k interfacial layer. This has significant effects on scaling ability and electrical characteristics. In our experiment, we employ high density plasma (HDP) NH_3 and N_2O plasma surface pre-treatments on Si substrate to form an ultra-thin interfacial layer. Our results show that samples with HDP pre-treatment result in surface damage and the leakage current does not meet device criterion. An oxide RTA is found to be necessary to repair the damage. Samples with plasma pre-treatment and RTA anneal depict lower leakage current, smaller hysteresis and frequency dispersion, and higher breakdown voltage. In addition, NH_3 pre-treatment also results in longer time to breakdown, larger charge to breakdown and better characteristics life time.

We found that the dominant charge trapping mechanism in the high-k gate stack is hole trapping rather than electron trapping. This behavior can be well described by the distributed capture cross section model. In particular, the flatband voltage shift (ΔV_{fb}) is mainly caused by the trap filling instead of the trap creation. The dominant hole trapping can be ascribed to a higher probability for hole tunneling from the substrate, compared to electron tunneling from the gate, due to a shorter tunneling path over the barrier for holes due to the work function of the TiN gate electrode.

We also found that the traps in HfO_2 virgin films are "latent", so leakage current is essentially independent of temperature. After voltage stress, however, these traps are activated and the dominant current transport mechanism becomes Frenkel-Poole emission. If the existing hole traps are filled by proper voltage stress, the leakage is found to be essentially independent of temperature, similar to that of the virgin sample.

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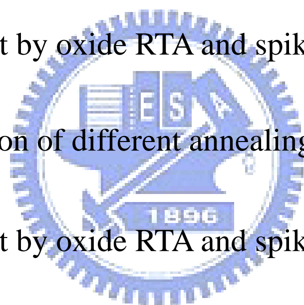

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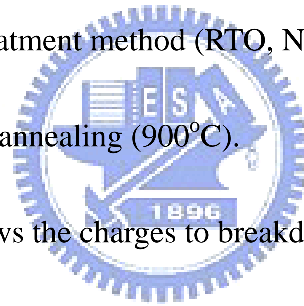

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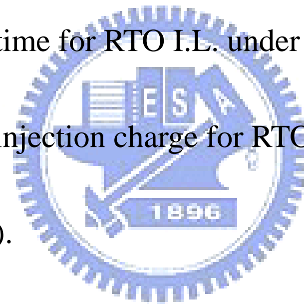

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