Chapter 1

Introduction

1-1 General Background

The rapid advancement of CMOS technology in the past decades has fueled the extraordinary progress in chip functionality, and dramatic lowering in the manufacturing cost. On the trace to the physical limit, the scaling of CMOS technology is reluctant to depart far away from the Moore's Law, which states that the number of transistors in a processor chip doubles every 18 months. For decades, this precept is regarded as a de facto roadmap for process technology in the semiconductor industry.

According to first order current-voltage relation, the drive current in a MOSFET can be given as

$$I_{ds} = 1/2C_g\mu_n(W/L_{eff})(V_{GS}-V_t)^2 \tag{1.1}$$

where V_{GS} is the applied gate-to-source voltage, L_{eff} is the effective channel length, W is the channel width, V_t is the threshold voltage, μ_n is the mobility for electrons and C_g is the gate capacitance; mainly governed by the permittivity and the thickness of the gate dielectric.

In an attempt to improve the current drivability of a MOSFET, all parameters contained in the above formula can be accordingly adjusted. However, some approaches will bring about serious drawbacks. For instance, the term (V_{GS}-V_t) is limited in a range due to the reliability and leakage concerns. Too large V_g will obviously create an undesirable high electric field across the gate oxide which in turn degrades the reliability. On the other hand, V_{th} cannot easily be reduced below about 200mV because of the induced statistical fluctuations in thermal energy at a typical operation circumstance of up to 100°C. Therefore, the more simple and liable tactics are the reduction in the channel length and the increase in the gate capacitance. Channel length reduction is a continuous solution to improve the performance and density of a chip and essentially depends on the progress of patterning technology including lithography and etching.

Currently, the full-fledged CMOS technology has been scaled into the nano-meter regime. According to the SIA roadmap [1], the equivalent oxide thickness (EOT) of gate dielectrics should be less than 1.3nm for 65nm technology node. Fig 1.1(a) and (b) depict the shrinking trend of gate dielectric thickness as a function of technology node for microprocessor and low-power devices. SiO_2 serving as the de facto gate dielectric since the inception of silicon-based IC technology has played a prominent role in determining the CMOS device performance. Unfortunately, the physical limit for the silicon dioxide gate dielectric is found to be around 1.2 nm, due to intolerable inversion charge loss, unwanted voltage drop along the gate electrode and the enhanced interface roughness scattering [2]. Since there exist two conflicting requirements in the scaling of CMOS devices: high speed operation and low power consumption. Both requirements are extremely desirable for the superior chip operation. Although the device speed is known to improve upon decreasing the gate oxide thickness, it is achieved at the expense of increased gate leakage current. Since the gate leakage current drastically soars to intolerable level as the gate oxide thickness is thinned down to this regime [3], this result, thus, poses a dilemma for further scaling of silicon dioxide as the gate dielectric. Apparently, the future of silicon dioxide appears to be somber and most likely doomed, and increasingly, the requirements outlined by the International Technology Roadmap for Semiconductors (ITRS) (see Table 1-1) [4] indicate that no known solutions exist for a variety of critical technologies, It is therefore essential to explore promising alternative gate dielectrics to replace SiO_2.

With increasing dielectric constant of the gate dielectric, the same equivalent oxide thickness can be obtained with a thicker physical thickness, thus reducing the leakage current. Oxynitride (SiON) and nitride/oxide stacked dielectrics [5-10] are considered to be potential candidates for 0.13 μm and 90 nm technology nodes due to its more controllable oxidation rate, lower interface state, higher rebellion against dopant diffusion, better dielectric integrity, lower stress induced leakage current, less charge trapping characteristic, and no contamination issues. They are expected to serve as near-term replacement for the gate dielectric. Unfortunately, their dielectric constants are not high enough to provide sufficient physical thickness for the gate leakage current suppression beyond the 65 nm technology node. Besides, as the nitrogen concentration increases in the oxynitride, it is difficult to achieve sufficient etching stop on the gate dielectric during poly-Si gate etching due to the degraded etching selectivity. It will result in pits on the active region after poly-Si gate etching. Thus, the suitability of oxynitride and nitride/oxide stack dielectrics is limited in future generations beyond 90 nm technology node.

Recently, gate dielectrics with higher dielectric constants than SiO_2 have attracted lots of research attention. Only the dielectrics that are thermodynamically stable in direct contact with Si are preferred [11], such as ZrO_2, HfO_2, $HfSiO_4$, Al_2O_3, Y_2O_3, and La_2O_3. Although these dielectrics are predicted to be stable with Si, there is still an interfacial layer, the Achilles' heel of further EOT reduction, since any deposition technique of interest usually operates under non-equilibrium condition. Among them, the most promising alternative gate dielectrics appear to be ZrO_2, HfO_2, and their silicates [12-30]. However, there are three major side effects of high-k dielectrics:

(a) the formation of polycrystalline phase at low deposition temperature,

(b) higher interface state density and charge trapping in high-k dielectrics,

(c) remote phonon scattering [31, 32].

These three side effects can result in additional leakage current paths, complicate leakage current mechanism, and cause mobility degradation. Unfortunately, these three side effects are ascribed to the inherent material properties. Compared to silicon dioxide, the high-k dielectrics can possess higher dielectric constant due to the greater degrees of ionic bonding contributing ionic polarization. On the other hand, the ionic bonding makes these high-k dielectrics not a good glass-former like SiO_2, i.e., polycrystalline phase is easily formed. In addition, ionic bonding enhances the remote phonon scattering arising from optical phonons associated with metal-oxygen bonds. In contrast, silicates are pseudo-binary alloys, intermediate between metal oxide and SiO_2. They can keep amorphous phase even after high-temperature annealing process. Therefore, silicate dielectrics show more preferable morphology, higher compatibility with the ULSI processing than metal oxide. However, these benefits are obtained at the price of lower dielectric constant.

Generally speaking, the energy gap is inversely proportional to the dielectric constant, as shown in Fig. 1.2. The offset of conduction and valance bands for several gate dielectrics are shown in Fig. 1.3. From Fig. 1.2＆Fig. 1.3, although the high-k dielectrics provide thicker physical thickness to suppress direct tunnelling current, the narrower energy gap and smaller band offsets can enhance Schottky emission of carriers. The trap-assisted leakage mechanisms, Frenkel-Poole emission or hopping effect, are also more significant than those in silicon dioxide. Thus, there are several requirements for high-k dielectrics aiming at replacing conventional SiO_2 or oxynitride [12, 13]:

(1) Thermodynamic stability in direct contact with Si.

(2) Higher energy bandgap with conduction band offset (ΔEc) > 1eV to reduce the thermal emission of carriers.

(3) Ultra-thin interfacial layer (if this layer can not be avoided).

(4) Low leakage current ($< 1mA/cm^2$ at $V_G-V_{FB} = 1$ V), (5) low interface state density ($D_{it} < 10^{11}$ /cm^2 eV^{-1}),

(6) Hysteresis < 20 mV,

(7) Film morphology (amorphous),

(8) Good gate compatibility,

(9) Stable process compatibility (especially high temperature source/drain anneal).

(10) Less mobility degradation.

1-2 Motivation-Why HfO_2 by MOCVD？

From section 1-1, we know that high-k materials are imperative to apply in semiconductor industry. But how to select a proper material to replace SiO_2 is a critical issue for engineers.

Currently, HfO_2 is the most promising candidate among all potential high-k dielectrics with many advantages as follows:

(1) Suitable permittivity,

(2) Acceptable band alignment,

(3) High free energy of reaction with Si,

(4) High heat of formation, and

(5) Superior thermal stability with poly-Si.

Table1-2 shows the preliminary material properties of HfO_2 [35]. Remarkably, this material almost meets all of the criteria and requirements for the high-k dielectrics to be used as the gate dielectric [36]. However, there are still many problems needed to be overcome such as crystallization, interfacial layer formation, lower mobility due to fixed charges (flat-band voltage shift), higher density of interface states, boron penetration, lateral oxidation at gate edge, and Hf contamination.

A comparison of sate-of-the-art high-k dielectrics is shown in Table 1.3 [18-30].

To reduce the interfacial layer, several approaches have been proposed and demonstrated. Unfortunately, irrespective of the pre-surface treatments, an interfacial layer with conceivable thickness still exists. It might be related to “catalytic oxidation effect” of metal oxide to enhance the oxidation rate at the interface [34]. To make this lower k-value material as thin as possible then becomes the goal in our study.

Many deposition methods, such as physical vapor deposition (PVD), metal-organic chemical vapor deposition (MOCVD), atomic layer deposition CVD (ALDCVD) [37, 38], and epitaxial method (MBE, etc.) have been employed to prepare HfO_2. The pros and cons of each deposition techniques are demonstrated in Table 1-4. For industrial application, PVD and MBE are not the appropriate tools for high-k film deposition. Because MOCVD has the advantage of superior step coverage, high deposition rate, good controllability of composition, excellent uniformity of film thickness over large area, we, therefore, chose the MOCVD technology as our tool to deposit thin hafnium oxide films.

1-3 Organization of the Thesis

In this thesis, we study the physical and electrical characteristics of HfO_2 with TiN metal gate electrode, its reliability issues, and the behavior of charge trapping.

In Chapter 2, we first describe the experimental procedure and, then, show the basic characteristics of HfO_2 gate dielectrics, including basic C-V and I-V characteristics of gate stacks with different post-nitridation annealing temperatures, EOT, hysteresis, and frequency dispersion.

In Chapter 3, the reliability and the characteristics of charge trapping in HfO_2 film are investigated. We compare the lifetimes of the gate stacks with different surface plasma treatment and show the hole trapping rather than electron trapping dominates in the HfO_2/SiO_2 gate stack during constant voltage stressing (CVS).

And the end of this thesis, conclusions are given in Chapter 4.

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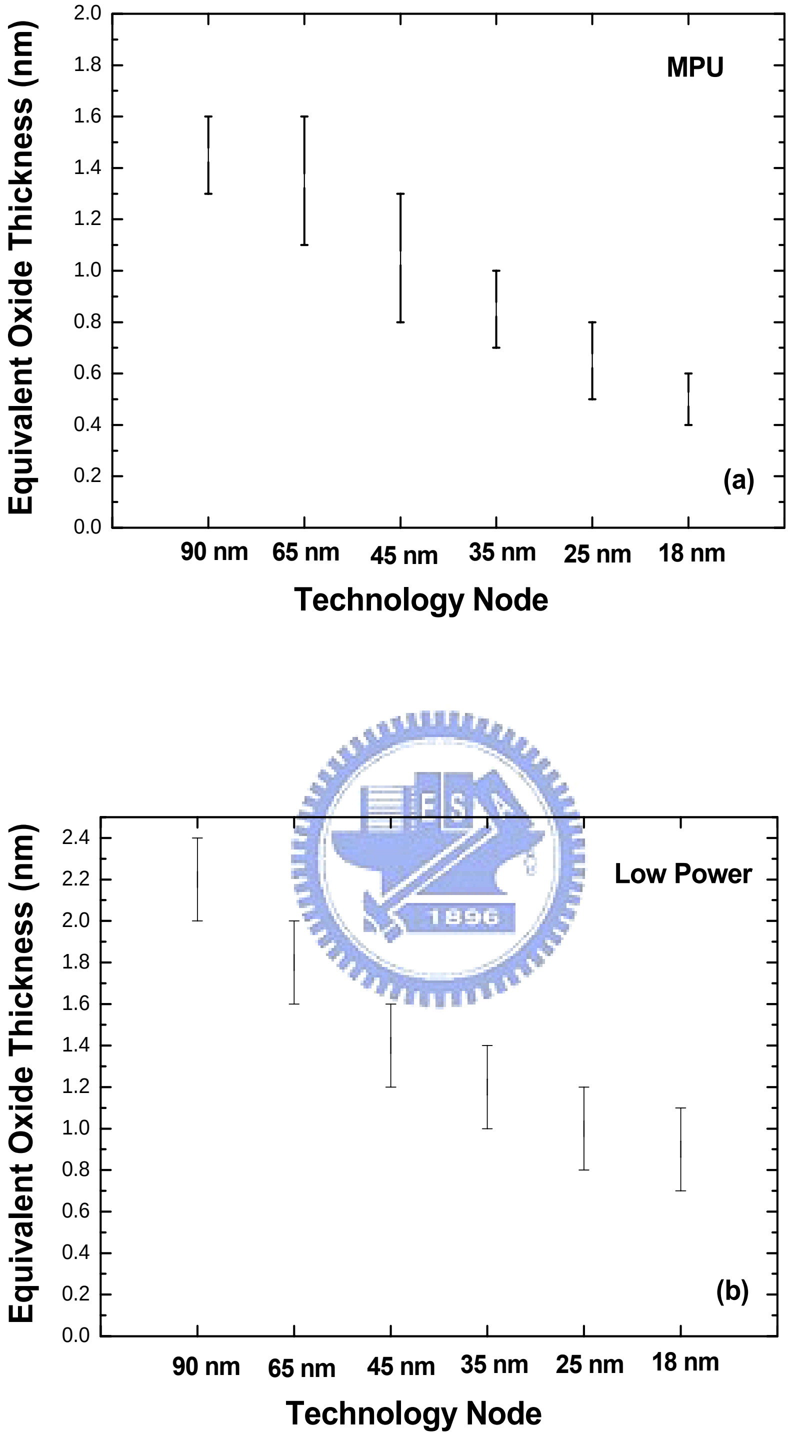
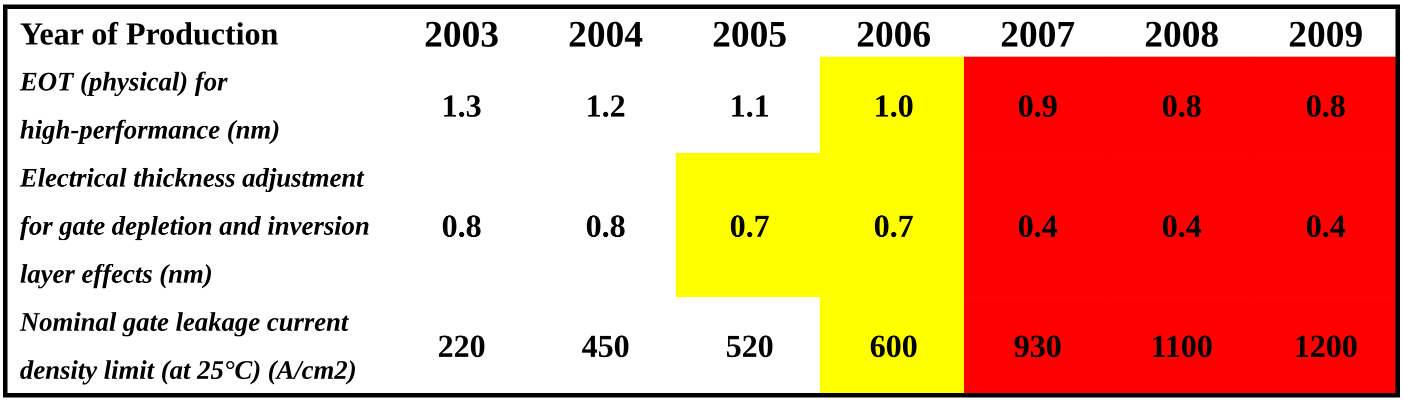


Fig. 1-1 The equivalent oxide thickness versus generation nodes for (a) microprocessor, and (b) low power.

ITRS 2003



Year of Production	2003	2004	2005	2006	2007	2008	2009
EOT (physical) for high-performance (nm)	1.3	1.2	1.1	🟨 1.0	🟥 0.9	🟥 0.8	🟥 0.8
Electrical thickness adjustment for gate depletion and inversion layer effects (nm)	0.8	0.8	🟨 0.7	🟨 0.7	🟥 0.4	🟥 0.4	🟥 0.4
Nominal gate leakage current density limit (at 25°C) (A/cm2)	220	450	520	🟨 600	🟥 930	🟥 1100	🟥 1200

🟨 *Manufacturable solutions are known*

🟥 *Manufacturable solutions are NOT known*

Table 1-1 2003 International Technology Roadmap for Semiconductors [1]
The color shade means the solution known and unknown for physical limit.

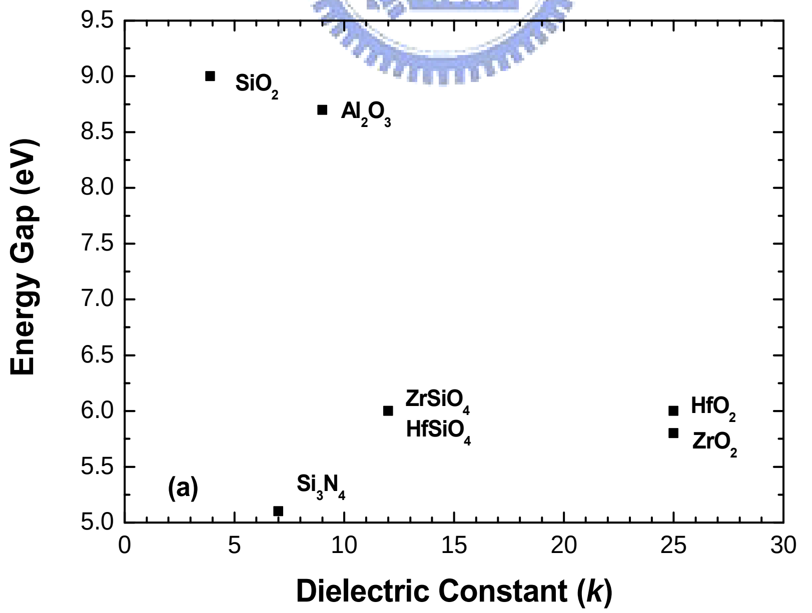


Fig. 1-2 Energy gap versus dielectric constant for
SiO$_2$, Si$_3$N$_4$, ZrO$_2$, HfO$_2$,ZrSiO$_4$, and HfSiO$_4$

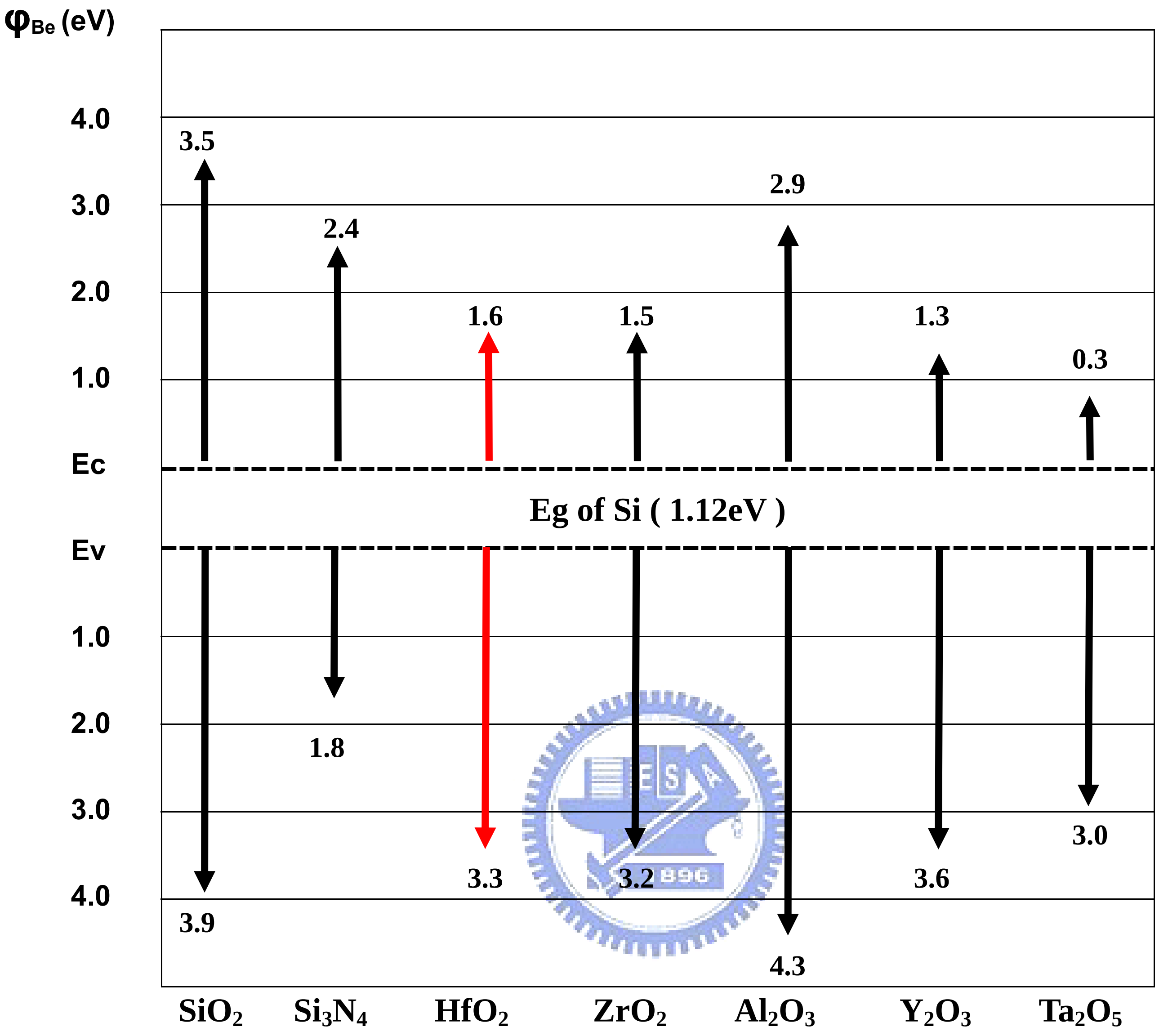


Fig. 1-3 Band alignments of topical high-k dielectrics [33]

Aspect	Property		
	HfO_2	ZrO_2	Al_2O_3
Band-gap(eV)	**5.68**	5.16	8.3
Barrier height to Si(eV)	**1.6**	1.5	2.9
Dielectric constant	**25~40**	~25	8~10
Dielectric strength (MV /cm)	**2~4.5**	>1.0	>1.0
Heat of formation (Kcal/mol)	**271**	261.9	399
ΔG for reduction (Si+Mox→M+SiOx)	**47.648**	42.326	64.39
Thermal expansion coefficient (10^{16}K-^{1})	**5.3**	7.01	6.7
Lattice constant (Å) (5.43 Å for Si)	**5.11**	5.1	4.7~5.2
Self diffusion coefficient @ 900℃	**2.8227×10^{-17}**	6.0009×10^{-10}	1.5048×10^{-7}

Table 1-2 Material properties of HfO_2, ZrO_2, and Al_2O_3.

	Fujitsu	**U.T., Austin**	**Sematech, IMEC**	**U.T., Austin**	**IBM**	**U.T., Austin**
Dielectrics	HfO_2	ZrO_xN_y	$ZrAl_xO_y$	HfO_2	HfO_2	HfO_2
Deposition Method	ALCVD	Sputtering	ALCVD	Sputtering	ALCVD	MOCVD
Substrate	Si	Si	Si	Si	Strained Si	Si
Surface Pre-Treatment	N/A	No	RTO	NH_3 or NO	oxynitride	RTP NH_3
Gate Electrode	Poly-Si	TaN (Sputtering)	Poly-Si	Poly-Si	Poly-Si	TaN (CVD)
EOT (nm)	1.4	1.03	1.0	1.3	2.8	1.1
Interfacial Layer (nm)	< 0.5	0.7	0.5	N/A	N/A	N/A

	Motorola	**U.T., Austin**	**U.C.,Berkeley U.T., Austin**	**Agere**	**Samsung**	**T.I.**
Dielectrics	HfO_2	HfO_xN_y	HfO_2	HfO_2, Hf-Al-O	Hf-Al-O	HfSiON
Deposition Method	MOCVD	Sputtering	Sputtering	ALCVD	ALCVD	Sputtering
Substrate	Si	Si	Si	Si	Si	Si
Surface Pre-Treatment	N/A	No	NH_3	Ozonated cleaning	No	N/A
Gate Electrode	TiN (PVD, CVD) TaSiN (PVD)	TaN (Sputtering)	Poly-SiGe	Poly-Si	Poly-Si	Poly-Si
EOT (nm)	1.7 (CET)	0.94	1.2	~1.7	1.46	1.1
Interfacial Layer (nm)	~1.5	N/A	~1.2	0.5	0.8	~0.9

Table 1-3 Comparison of state-of-the-art high-k dielectrics

Physics Vapor Deposition（PVD）	**Chemical Vapor Deposition（CVD）**		**Epitaxial Method**
	MOCVD	**ALDCVD**	
Pros： **1.Convenient for new materials screening.** **2.Easy to fabricate experimental data.** **3.Low cost for ownership.**	**Pros：** **1.Superier step coverage.** **2.High deposition rate.** **3.Good controllability of composition.** **4.Uniformality of film thickness over large area.**	**Pros：** **1.Better thin film quality than PVD and CVD.** **2.Excellent coverage and conformality.** **3.**	**Pros：** **1.Permit single crystal, high-k dielectric system.**
Cons： **1.Planar, line-of-sight process, damage.** **2.Not likely to be used in USLI gate Process.** **3.Poor co formality, especially for high aspect ratio.**	**Cons：** **1.Hard to deposit ultra thin films.** **2.Poorer conformity than ALD CVD.** **3. C-, H-, OH-impurity Contamination.**	**Cons：** **1.Low throughput.** **2.Mechanism-related surface sensitivity.** **3. Chemistry-limited final products (only binary materials are available now).**	**Cons：** **1.Requires submonlayer Control.** **2.Poor throughput for ULSI standard.** **3.UHV tool and the cost of maintenance.**

Table 1-4 Comparison of Deposition Techniques: Sputtering, ALD, MOCVD, and MBE.

Chapter 2

The Effects of Surface Pre-deposition Treatments on the Properties of HfO_2 Thin Films

2-1 Introduction

As the dimensions of complementary metal oxide semiconductor (CMOS) devices are scaled into the nanometer regime, the equivalent oxide thickness (EOT) of the gate dielectric decreases steadily to thinner than 1nm. In such thickness range, the mechanism responsible for the leakage current under normal operation bias falls into the direct tunneling regime. Due to their thicker physical thickness, high-k materials can have drastically reduced tunneling leakage current at the same EOT and gate capacitance compared to thermal oxide. Recently, high-k materials such as ZrO_2, HfO_2 and their silicates have been extensively studied [1,2]. Even though excellent characteristics in terms of interface state density, reliability and leakage current have been demonstrated, there are still many issues that need to be resolved before they can be used as the gate dielectrics in future device generations. Poly depletion is one of the challenging issues. To effectively solve the poly depletion problem, other gate electrodes such as metal gates must be used to replace the poly-Si gate electrode.

Considering the thermal stability of the new materials, metals that are rather inactive in contact with high-k materials such TiN, Pt, are often regarded as the potential candidates.

The unavoidable formation of interfacial low-k layer is another critical issue, which will place a limit on pursuing the lowest EOT value for high-k dielectrics. Previously, the composition of this interfacial layer is thought to be SiO_2-like [3, 4]. In order to suppress the oxygen diffusion through the high-k layer, we adopt an additional NH_3 treatment prior to the deposition of the HfO_2 films. According to the bonding strength comparisons as follows, Si-O(8.42eV) > Si-N(4.75eV) > Si-Si(3.38eV) > Si-H(3.18eV), the Si-N bonds have larger bonding strength than the Si-Si bonds or Si-H bonds. Therefore, we employ the stronger Si-N bonds to replace Si-H bonds in order to resist the oxygen diffusion during deposition, which could also help eliminate the defect generation, hot carrier injection effect, and boron penetration. Moreover, to reduce the leakage current is another major reason of using NH_3 treatment [5]. However, formation of thin Si_3N_4 on Si surface will result in higher interface charges [6], which may in turn lead to higher hysteresis and reduced channel mobility.

There are many methods to form a ultra-thin nitride film such as furnace growth or plasma deposition. Meanwhile, plasma deposition is preferred because of its low thermal budget and high throughputs. In this thesis, high density plasma (HDP) was used for the thin nitrided film formation. Conventional oxide RTA and spike oxide RTA with different temperatures were adopted to densify the nitrided film and hopefully to reduce the hysterisis effect.

MOCVD system was used in this thesis, and its pros and cons were mentioned in chapter one. A detail schematic structure is shown in Fig. 2-1. The MOCVD chamber is equipped with a turbomolecular pump and a liquid injection system (which has four independent-controlled injectors). The latter is consisted of a liquid pump to pump the precursors through a hot nickel frit with a proper rate, because the pump is unreliable at low pump rates. The vapors are carried with a 200 sccm flow of Ar to a gas distribution ring which is located at a proper distance from the substrate. In contrast to the conventional bubbler system, the liquid injection system is with sufficient temperature window to alleviate the thermal aging of the precursor. This is because the precursor remains in liquid state at room temperature until it is pumped into the vaporizer and injected into the deposition chamber. However, the precursor should be kept at long-term chemical stability in solvent and non-reactive with other precursors in solvent [7, 8]. The components of the vaporizer, the gas ring and the connecting tube are maintained at a temperature of 190 ºC with heating tapes and blankets, while the substrate temperature is controlled at 500 ºC with quartz-halogen lamps and a thermocouple. A rotating susceptor is used for uniform heating during processing. A flow of 100 sccm N_2 is maintained throughout the deposition cycle. The base pressure of the MOCVD chamber is ~ 10^{-8} Torr. The deposition pressure of the deposition is at the 5 mTorr where the gas-phase collisions are scarce.

2-2 Experimental Procedure

In this thesis, we use LOCOS isolation to fabricate capacitors. The cross-sectional views and kep processing steps are shown in Fig. 2-2. MOS capacitors were fabricated on 6-inch p-type Si with (1 0 0)-oriention and 5~8Ω-cm resistivity. After the sacrificial oxide about 300Å was removed, RCA clean was performed, followed by dilute HF dip to remove native oxide. After that, wafers were processed to receive various surface treatments to form an ultra-thin interfacial layer before HfO_2 deposition (i.e. pre-treatment). Specifically, we used NH_3 and N_2O plasma to nitridate silicon surface, immediately followed by conventional N_2 RTA or spike N_2 RTA at three different temperatures (900℃, 950℃, 1000℃), and we also used spike RTA at 800℃ in O_2 ambient to form about 10Å interfacial oxide. After surface pre-treatment, HfO_2 film of approximately 5 nm was deposited by atomic vapor deposition (AVD^{TM}) in an AIXTRON Tricent® system at a substrate temperature of 500 °C, followed by 500℃ N_2 RTA for 30sec. The MOCVD system was designed for

8-inch wafers, so a 6-inch quartz was used as wafer carrier for film deposition. A 5000 Å TiN electrode was sputtered and patterned to form gate electrodes, followed by 600℃ post-mteal deposition anneal for 30 sec. Then, wafers were sputtered with aluminum on the backside, and received a forming gas anneal at 400 °C for 30 min.

For physical analysis, high resolution transmission electron microscopy (HRTEM) was employed. For electrical analysis, a precision impedance meter of HP 4284 was used for C-V measurement and a semiconductor parameter analyzer of HP 4156C was used for I-V measurement. High frequency C-V measurement was performed at 100 kHz, with a small ac signal of V_{rms}=25mV. In general, forward C-V sweep indicated that the bias voltage was swept from inversion mode to accumulation mode. In some case, forward and backward sweeps were performed to monitor the hysteresis phenomenon. For C-V measurement, parallel circuit model was employed due to the high leakage current of most of the thin gate dielectric and flatband voltage, equivalent oxide thickness (EOT) were extracted by UCLA CVC method.

2-3 Physical and Electrical Characteristics

In this section, some physical and electrical characteristics were discussed to analysis NH_3 and N_2O plasma with various annealing temperatures by oxide RTA or spike RTA.

2-3-1 C-V and I-V characteristics

Figure 2-3 (a) shows the high frequency C-V curves (100 KHz) of the samples with N_2O pre-treatment followed by N_2 RTA at 900°C, 950°C and 1000°C, respectively. The C-V measurement was swept from inversion to accumulation and Fig. 2-3 (b) shows the corresponding I-V curves. The capacitance of the sample with post-nitridation annealing decreases compared to that of the as-deposited sample. With only pre-treatment, i.e., without RTA, the distortion in the C-V curve hump disappears, indicating that leakage current in the film is significantly suppressed with surface pre-treatment. From I-V curves, we clearly observe that the gate current density (at –1V) in the samples with N_2O pre-treatment alone (i.e., without any RTA anneal) dramatically improves by about 3 orders of magnitude, albeit this current is still too large for practical application. Therefore, post-nitridation annealing is essential to further reduce leakage current to 10^{-7} A/cm^2 level.

Figure 2-4 (a) shows the high frequency C-V curves (100 KHz) of the samples with N_2O pre-treatment followed by N_2 spike RTA at 900°C, 950°C and 1000°C, respectively. The measurement was swept from inversion to accumulation. Fig. 2-3 (b) shows the corresponding I-V curves. It can be seen that although N_2 spike RTA at moderate temperatures (i.e., 900 and 950 ^{o}C) does result in moderate improvement, N_2 spike RTA at higher temperature (i.e., 1000 ^{o}C) results in performance degradation.

The leakage current is worse than that of the as-deposited sample with such a high N_2 spike RTA temperature, and the C-V curves are also severely distorted. We attribute these results to the thermal stress induced in the interfacial layer and the presence of this stress will degrade subsequently deposited film's quality.

As shown in Figs. 2-5 (a) and (b), the NH_3 pre-treatment followed by oxide RTA at different temperatures show similar trends compared to their N_2O pre-treatment counterparts shown in previous figures, albeit that the EOT increases faster. Fig. 2-6 (a) displays C-V curves with NH_3 pre-treatment followed by N_2 spike RTA at 900°C, 950°C and 1000°C, and the corresponding I-V curves are shown in Fig. 2-6(b). From the results in I-V characteristics, the spike RTA induces serious thermal stress because current density increases up to 10^{-2} A/cm^2 level even with a moderate annealing temperature 950°C, a current level seen at 1000°C N_2 spike RTA for the sample with N_2O pre-treatment.

Fig. 2-7 shows C-V and I-V characteristics of the samples with NH_3 and N_2O plasma pre-treatment with conventional and spike RTA at 900℃. Irrespective of N_2O or NH_3 treatment, the leakage current for the samples with conventional N_2 RTA is nearly 3 orders of magnitude lower than those with spike N_2 RTA.

2-3-2 Frequency Dispersion for HfO_2 Gate Dielectric

Ideally the capacitance determined from C-V measurements should not be frequency dependent at the high frequency range (i.e., above 100 kHz). In a typical capacitor, two mechanisms result in frequency dispersion. The first one is series resistance effect and the other is interface traps. The former effect mainly shows up in the accumulation region while the latter affects the transition in the depletion region. For radio frequency (RF) application of MIM capacitor with high-k dielectrics, frequency dispersion is an index for quality. Therefore, we discuss frequency dispersion below.

First, we need to determine the proper sweeping range for the C-V measurement, as we don’t want to introduce measurement artifacts such as stress induced traps into our results. Fig. 2-8(a) shows the C-V curves with RTO interfacial layer (I. L.). The sweeping range is (+1.5V, -1V), i.e., from inversion to accumulation. We start at 1 MHz, follow by 500 KHz, 100 KHz, 50KHz, 10 KHz, and then repeat for 1 MHz, 500 KHz and 100 KHz. For any given frequency, three sweeping cycles are performed. It is found that, irrespective of the measurement frequency, the subsequent sweeping cycles trace exactly the first cycle. This indicates that no defects and charge trappings are created during the C-V measurement. Next, we increase the sweeping range at accumulation regime to -2V, and repeat the experiment again. As shown in Fig. 2-9, the curves shift toward the left for the second sweep. This shift in C-V curves indicate that charge trappings are being introduced during the C-V sweeping, so the difference among different frequency measurements are not entirely due to frequency dispersion alone.

We repeat the same measuring sequence for every frequency by only sweeping from accumulation to inversion, and the results are shown in Fig. 2-10 and Fig. 2-11. For small sweep range, the curves with the same frequency overlap completely no matter how many times the measurements were performed. However, for larger range (-2V, 1.5V) the high-field stress does cause permanent change on the C-V charcateristics.

The dispersion percentage is defined as below:

$$\text{Frequency Dispersion} \equiv \frac{\text{C (@10 KHz)-C (@1 MHz)}}{\text{C (@10 KHz)}} \times 100\,\% \qquad (2\text{-}1)$$

Table 2-1 shows frequency dispersion percentage for all conditions. From Table 2-1 it can be seen that conventional oxide RTA can improve frequency dispersion, and the improvement becomes even more significant with increasing temperature. In contrast, spike RTA does not improve frequency dispersion at all.

2-3-3 Proper Sweep Range for C-V Measurement

Since improper sweep range will introduce uncertainties in our analyses, and affect the accuracy of flatband voltage extraction, we discuss the proper sweep range for the C-V measurement in this section.

First, the sweep range is set between -0.5V and +0.5V to ensure that C-V curve does not change regardless of the sweep direction, as shown in Fig. 2-13. Then we fix the accumulation voltage at -0.5V, and increase the inversion voltage from +0.5V to +2.0V with a step of 0.5V, as shown in Fig. 2-14. This reveals that increasing the inversion voltage has no effects on the extraction of flatband voltage. Next, if we fix the inversion voltage at +0.5V, and increase accumulation voltage form -0.5V to -2.0V with a step of -0.5 V, as shown in Fig. 2-15, it is clear that the curves shift left due to hole trapping. The amount of shift is in proportion to the increase of the initial voltage of reverse sweep.

2-3-4 Hysteresis for C-V measurement

One of the important features in the C-V characteristics of MOS devices is hysteresis, which can be employed to evaluate the electrical quality of the dielectrics. The requirement for the high-k gate dielectric applications is that the hysteresis width must be less 20 mV. Detailed mechanisms of the hysteresis in the high-k films are not fully understood. Interface traps is common suspected to contribute to the hysteresis [9].

First of all, the C-V hysteresis is measured by sweeping the gate voltage from inversion to accumulation (i.e., forward sweeping) and then back from accumulation to inversion (i.e., reverse sweeping). We fix the inversion voltage at +1.5V and change the accumulation voltage to observe the change of hysteresis width. Fig. 2-16(a) shows the zoom-in figure of C-V curve, and Fig. 2-16(b) is the plot of the relationship between the flatband voltage and accumulation voltage. It can be seen that the flatband voltage shifts toward left. The hysteresis width increases monotonically with increasing accumulation voltage. This result indicates that the amount of trapped charges is linearly dependent on the accumulation voltage but rather independent of the inversion voltage. Table 2-2 shows the hysteresis widths for all conditions in our experiment. Again it can be seen that N_2 RTA reduces the hysteresis, while spike RTA does not.

2-3-5 High Resolution Transmission Electron Microscopy (HRTEM)

Fig. 2-17 to Fig. 2-20 show HRTEM images of as-deposited samples which received NH_3 pre-treatment and N_2 RTA annealing at 900°, 950°, 1000°C, respectively. We found that the interfacial layer thickness increases with the increasing temperature. As a result, EOT increases with the grown interfacial layer while the leakage current decreases. From the HRTEM, we can see that owing to RTA treatment, interfacial layers become thicker and must be carefully controlled to maintain a thin EOT.

2-4 Summary

In this chapter, the characteristics of the MOCVD-deposited HfO_2 films with pre-treatment by NH_3 or N_2O and RTA at temperature ranging from 900 to 1000°C for 30 sec by either conventional N_2 RTA or spike N_2 RTA are presented. The samples with conventional RTA show much lower leakage current, lower frequency dispersion, and smaller hysteresis than as-deposited, spike RTA and no RTA samples because of a thicker interfacial layers. Therefore, RTA is still an essential process after pre-treatment to densify nitrided film although the EOT inevitably becomes larger. In contrast, spike RTA does not seem to be a proper method to densify nitride film because of large thermal stress.

Proper C-V voltage sweeping range is discussed here. From the points of frequency dispersion and the extraction of flatband voltage, the proper range is found to be between +1.5V and -1V for the capacitors used in this study. Hysteresis width in the high-k film becomes smaller with post-nitrded oxide RTA annealing. There is a linear relationship between the amount of trapped charges and the accumulation stress voltage, but independent of the inversion stress voltage.

Finally, HRTEM images reveal that even though oxide N_2 RTA can effectively decrease the leakage current, the formation of an interfacial layer could defeat the whole purpose of achieving thin EOT.

2-5 Reference

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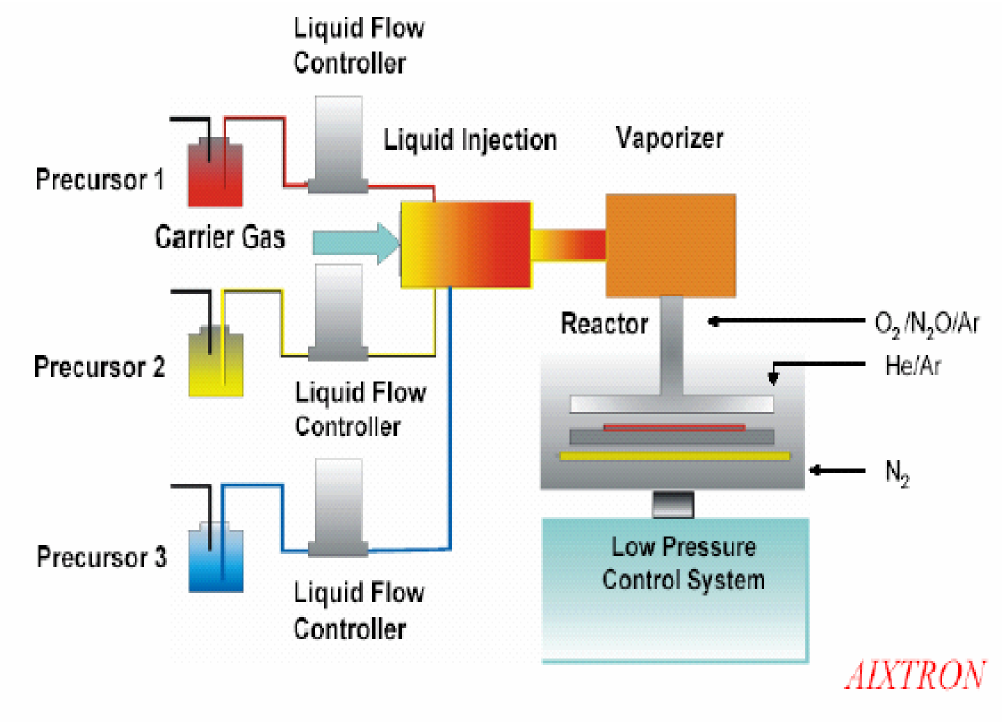
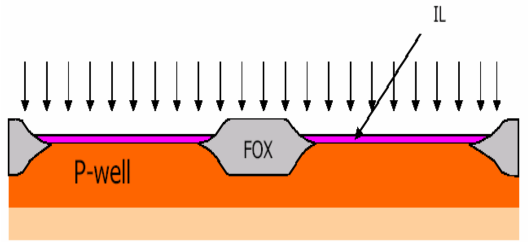


Fig. 2-1 A diagram of typical MOCVD system structure.

1. LOCOS structure, RCA clean, HF dip to remove native oxide.
2. HDP Pre-treatment to form a ultra-thin interfacial layer.

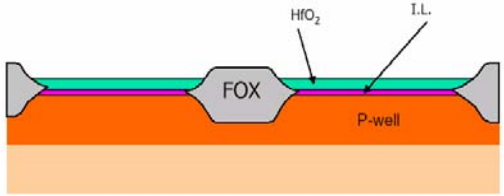
Spilt condition： a：N_2O plasma (250℃, 300W, 10 sec)
b：N_2O plasma (250℃, 300W, 10 sec)
c：Spike RTO (Rapid thermal oxide, 800℃ in O_2 ambient)
d：As-deposition



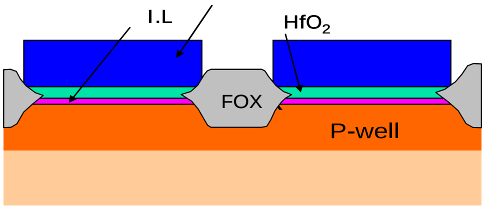
3. RTA in N_2 ambient to density plasma thin film.

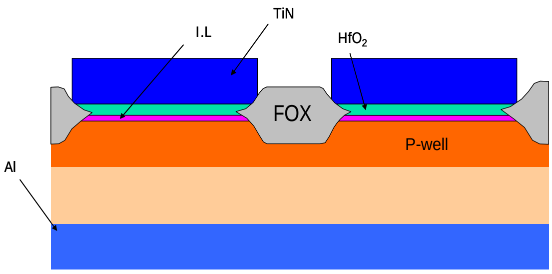
Spilt condition：
a：Oxide RTA with different temperature (900℃, 950℃, 1000℃)
b：Spike RTA with different temperature (900℃, 950℃, 1000℃)
c：No RTA

4. MOCVD HfO2 deposition.
(500℃, ~48Å, pressure~5mbar, carrier gas Ar~80 sccm, O_2~80 sccm).



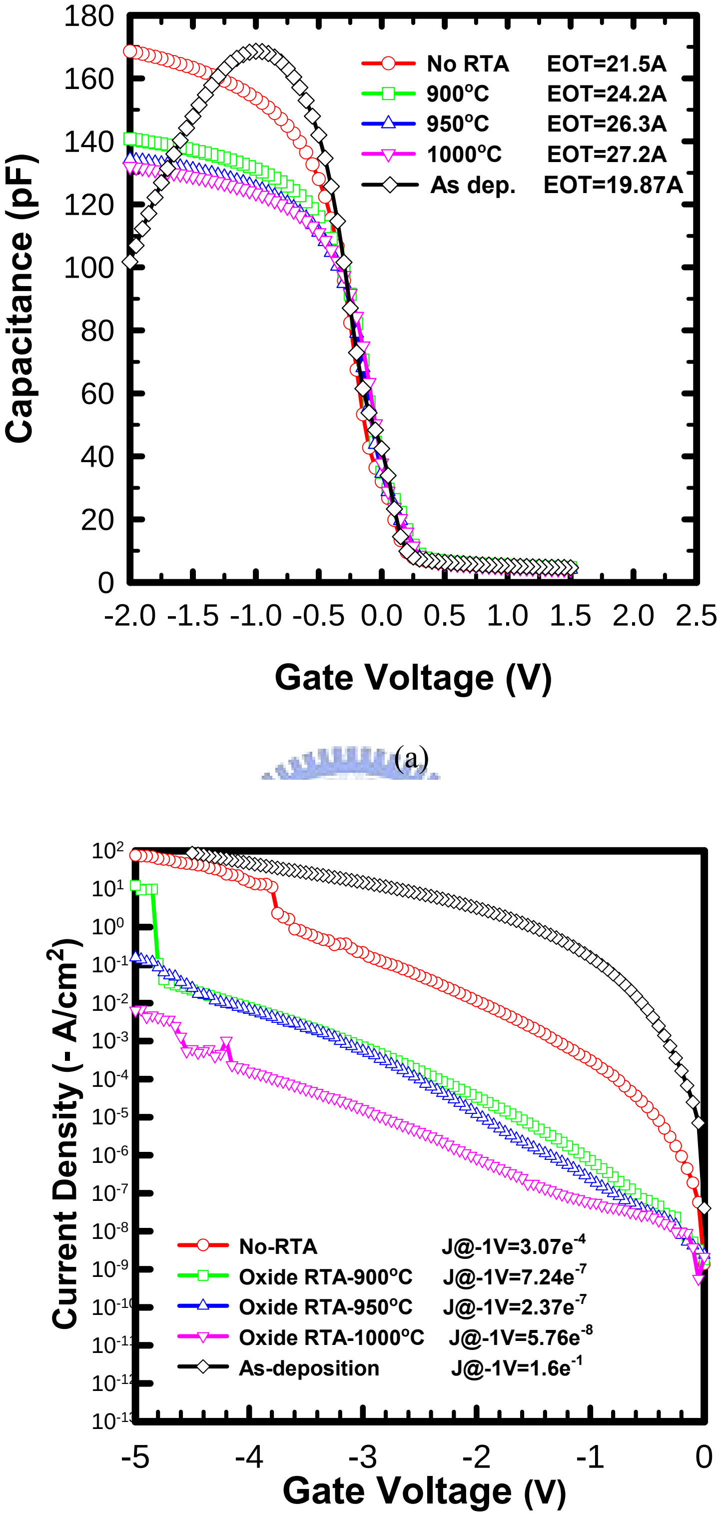
5. Post-deposition annealing, PDA (500℃, N_2, 30 sec).
6. TiN metal gate deposition (5000Å).
7. Post-metal deposition annealing, PMA (600℃, N_2, 30 sec).
8. Gate definition.





9. Backside Al sputtering.
10. 400℃ 30min H2 forming gas annealing.

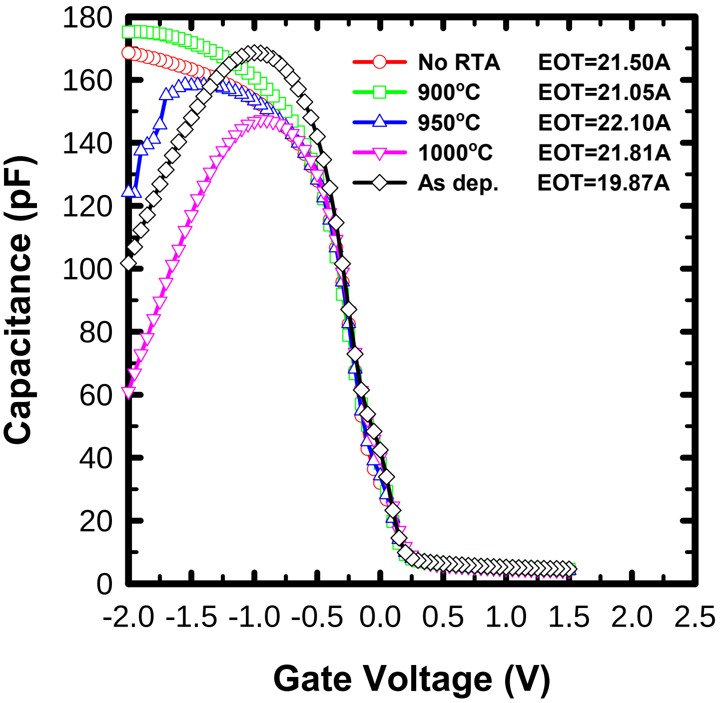
Fig. 2-2 The cross-section views of capacitor show LOCOS structure process flow.



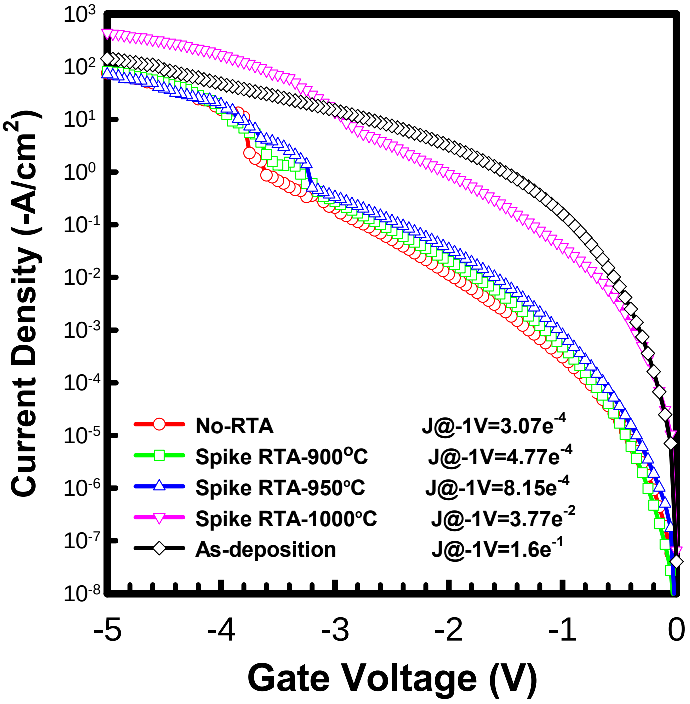
(a)

(b)

Fig. 2-3 The (a) C-V and (b) I-V curves of N_2O pre-treatment with different N_2 RTA temperature.

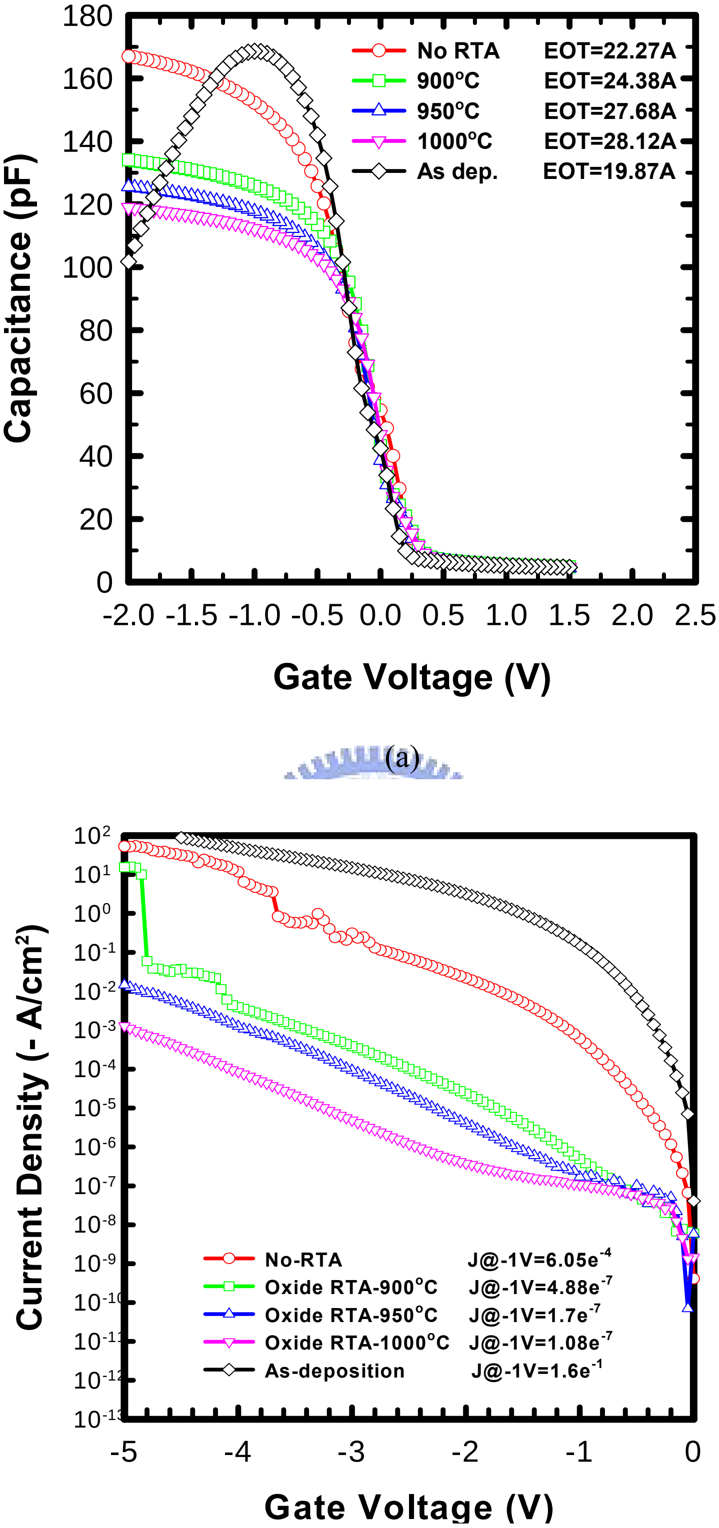


(a)



(b)

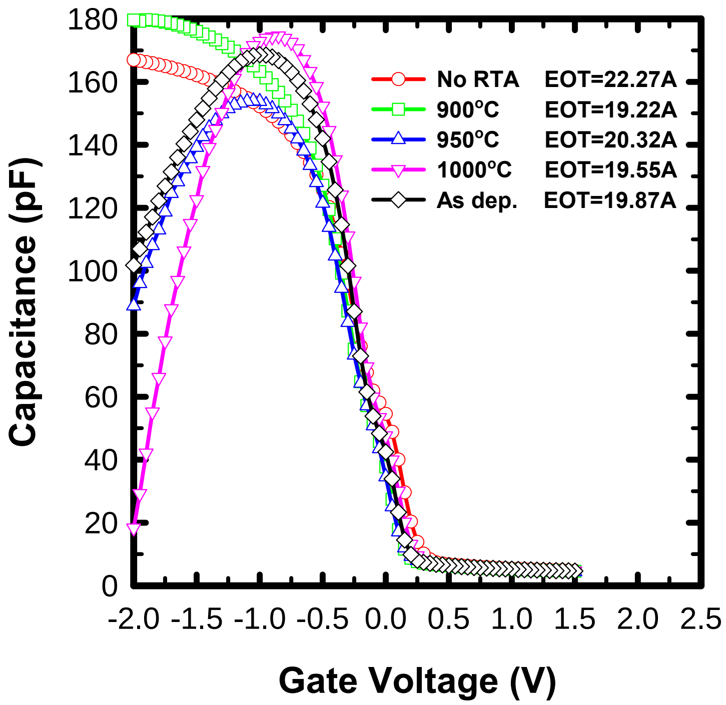
Fig. 2-4 The (a) C-V and (b) I-V curves of N_2O pre-treatment with different N_2 spike RTA temperature.



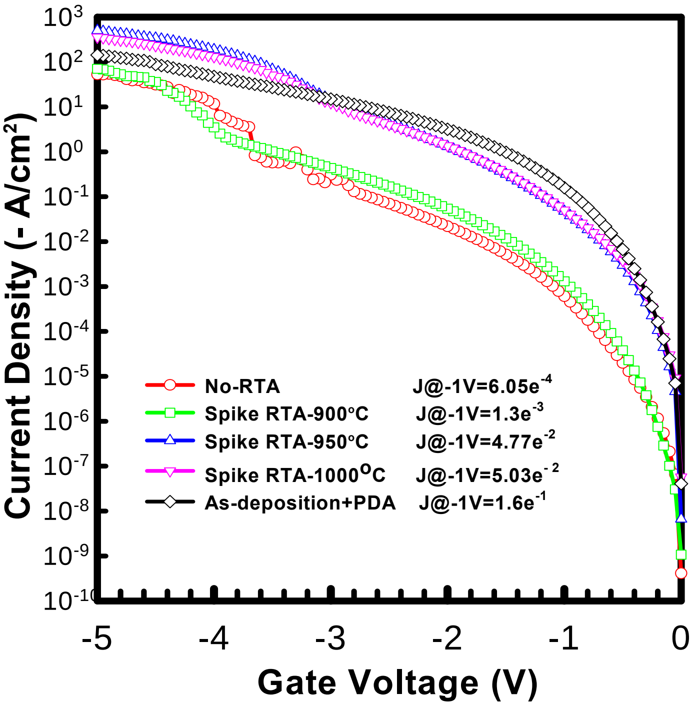
(a)

(b)

Fig. 2-5 The (a) C-V and (b) I-V curves of NH_3 pre-treatment with different N_2 RTA temperature.

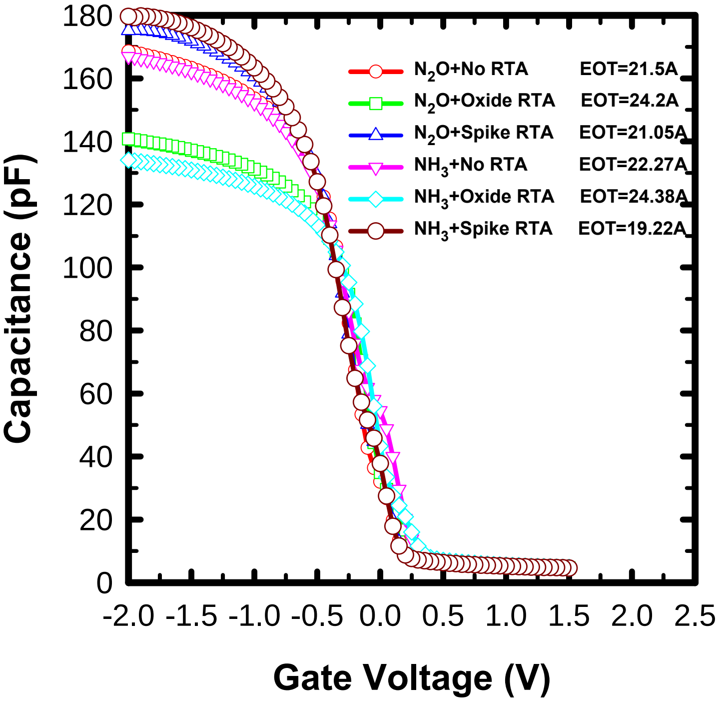


(a)

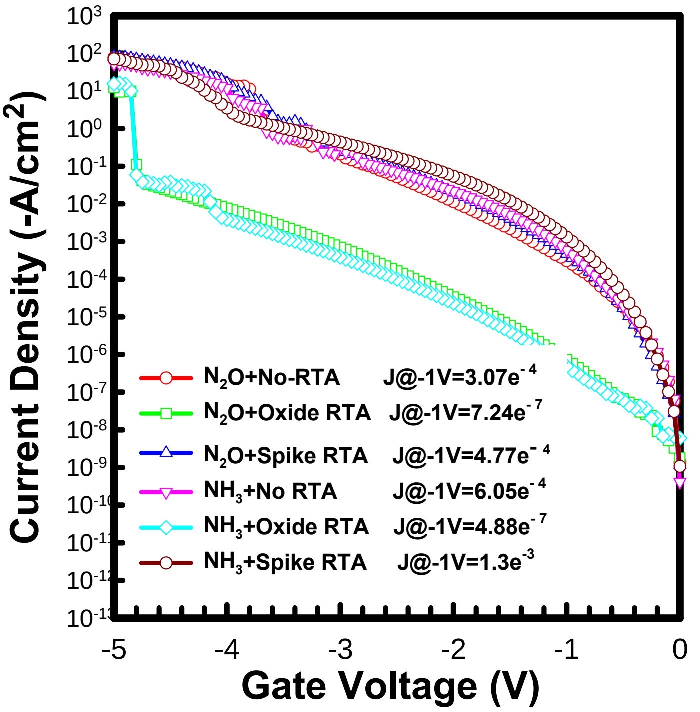


(b)

Fig. 2-6 The (a) C-V and (b) I-V curves of NH_3 pre-treatment with different N_2 RTA spike temperature.

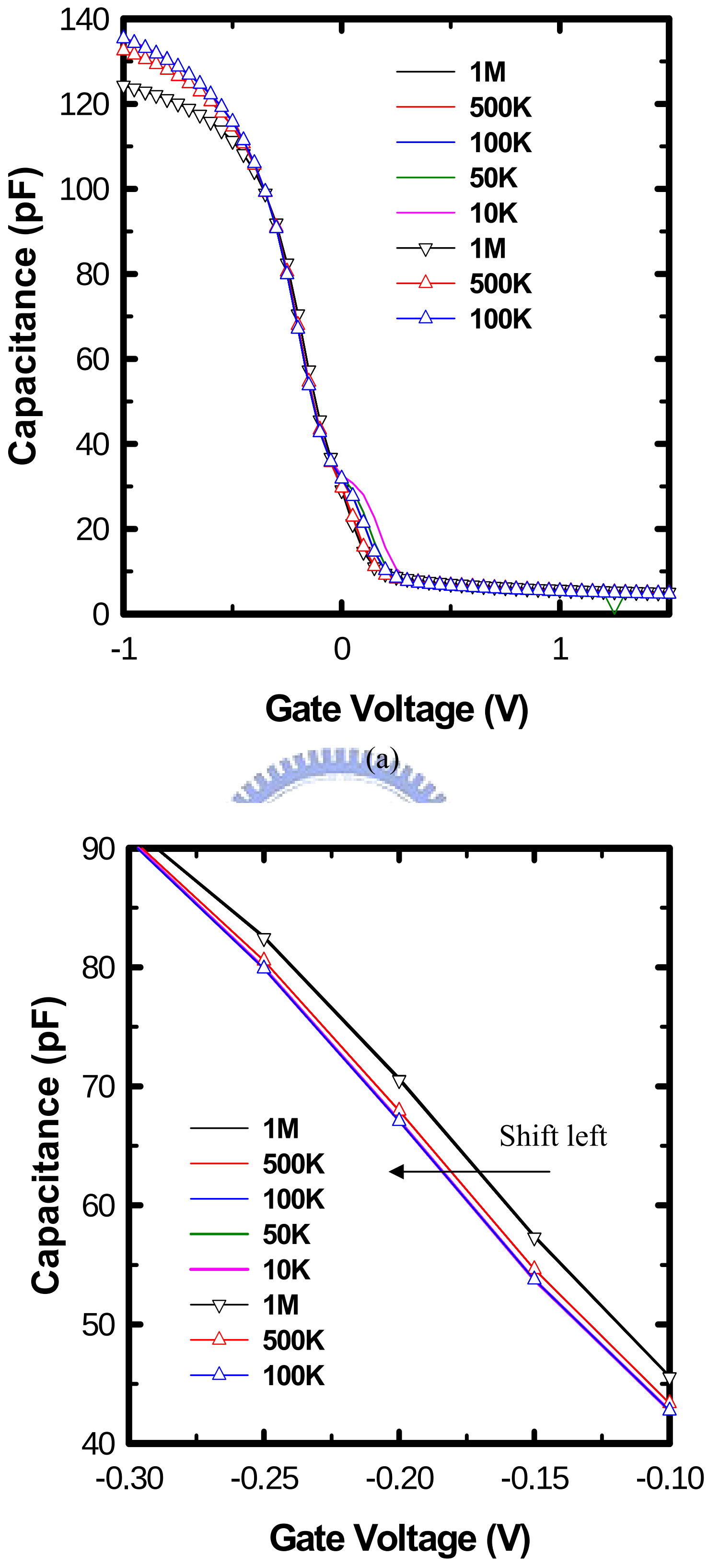


(a)



(b)

Fig. 2-7 The (a) C-V and (b) I-V curves of 900℃ N_2 annealing with N_2O/NH_3 plasma pre-treatment by oxide RTA and spike RTA.

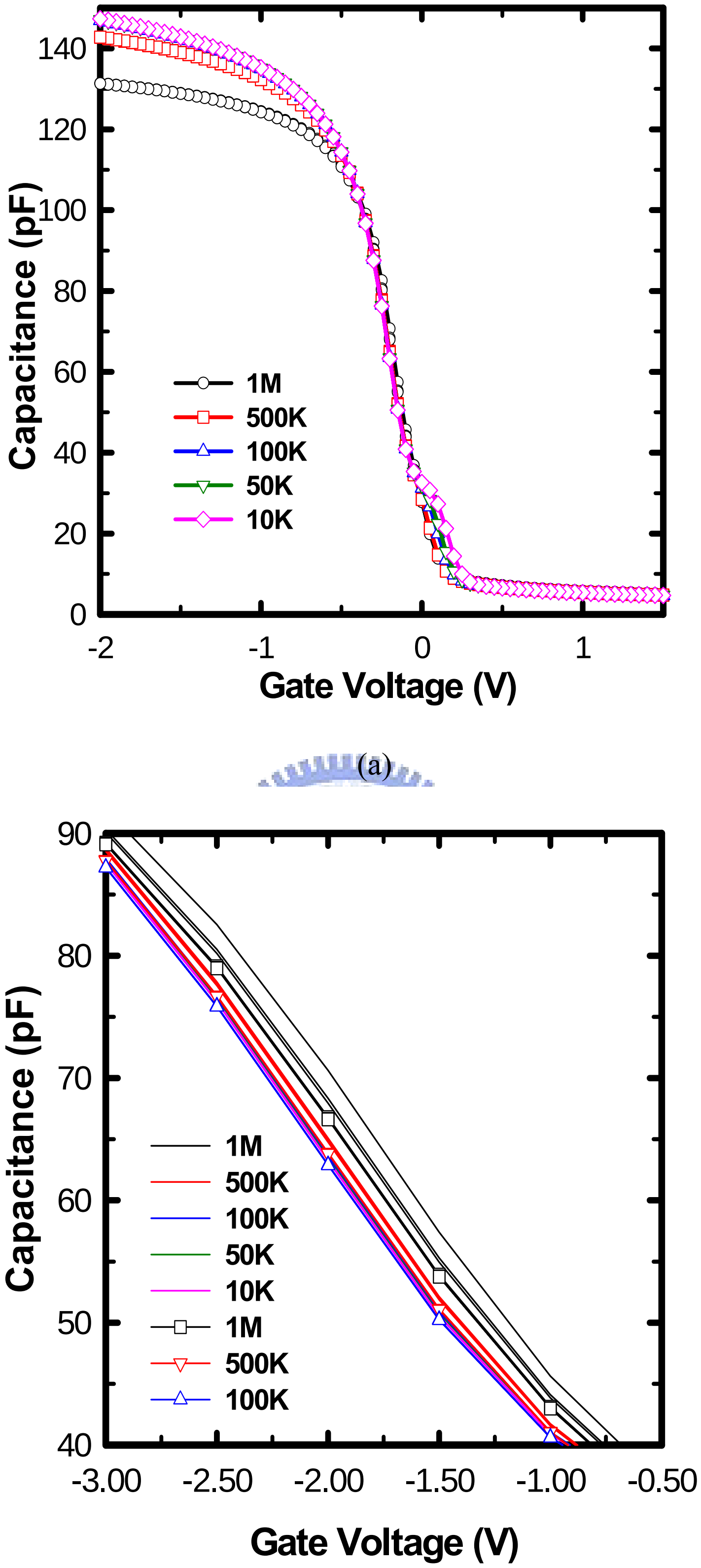


(a)

(b)

Fig. 2-8 The (a) C-V curve and (b) Zoom in figure of (a) with RTO I.L.

Sweep range is (+1.5V, -1V) form inversion to accumulation.

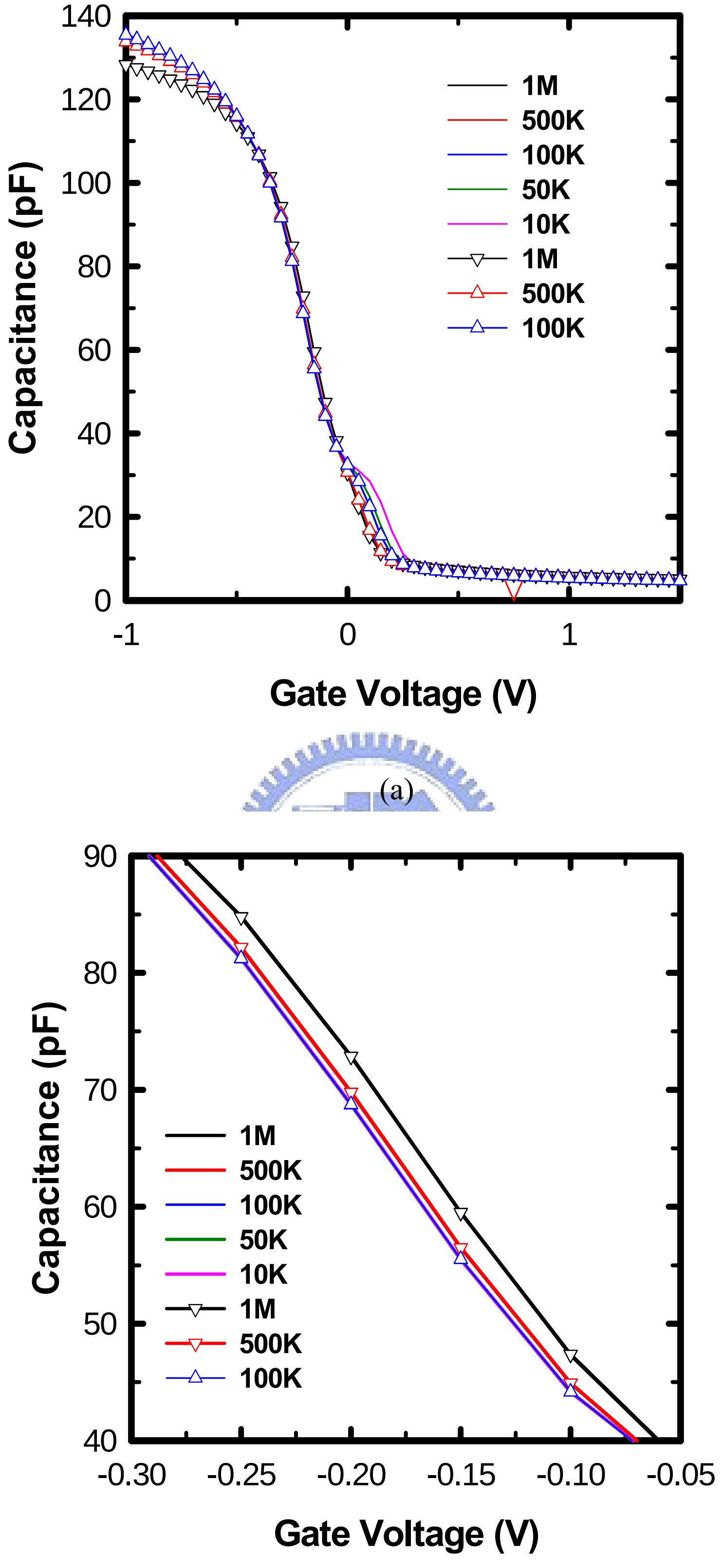


(a)

(b)

Fig. 2-9 The (a) C-V curve and (b) Zoom in figure of (a) with RTO I.L.

Sweep range is (+1.5V, -2V) form inversion to accumulation.

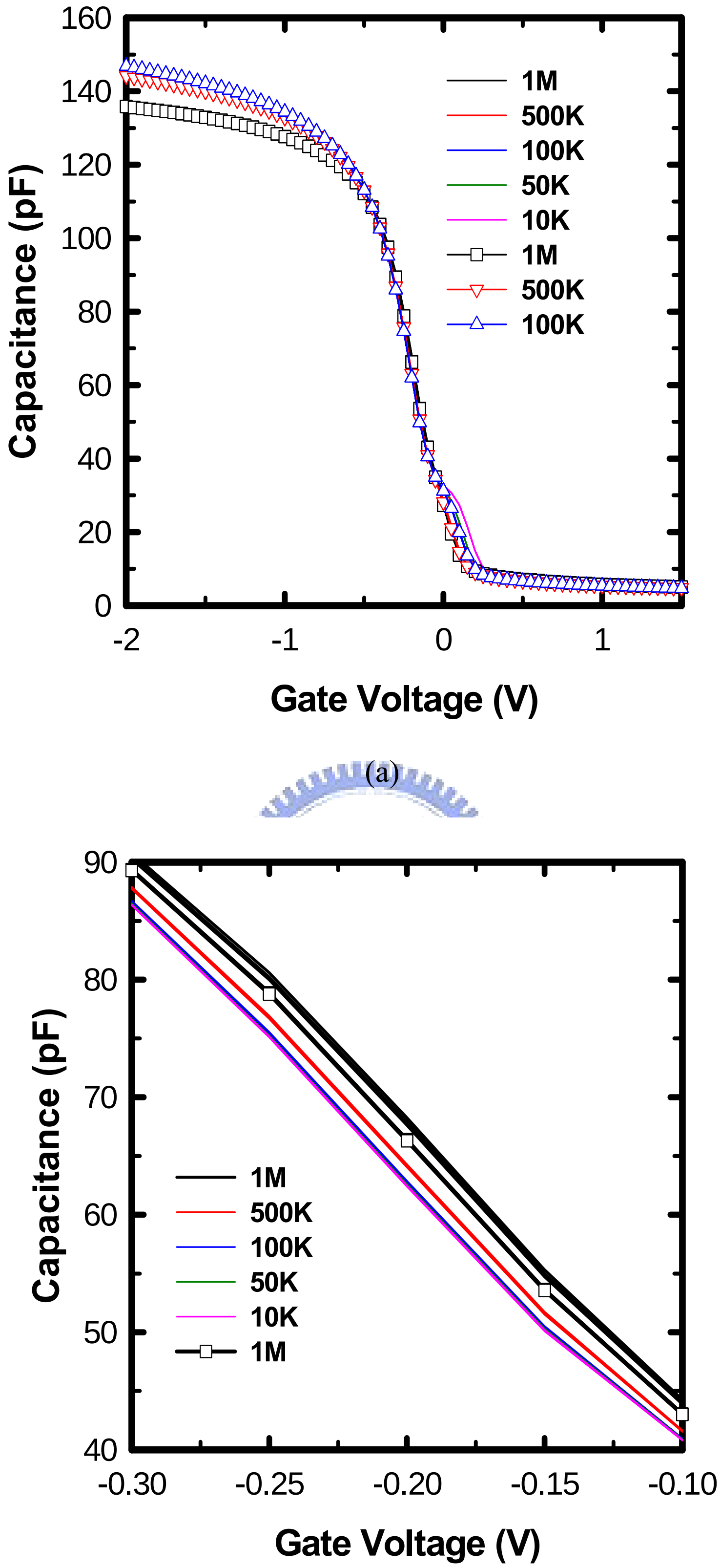


(a)

(b)

Fig. 2-10 The (a) C-V curve and (b) Zoom in figure of (a) with RTO I.L.

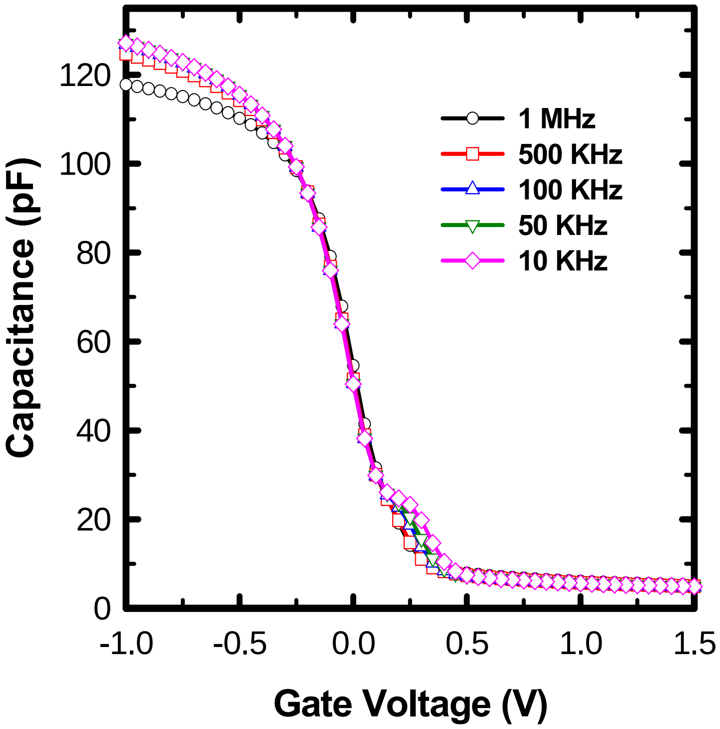
Sweep range is (+1.5V, -1V) form accumulation to inversion.



(a)

(b)

Fig. 2-11 The (a) C-V curve and (b) Zoom in figure of (a) with RTO I.L. Sweep range is (+1.5V, -1V) form accumulation to inversion.

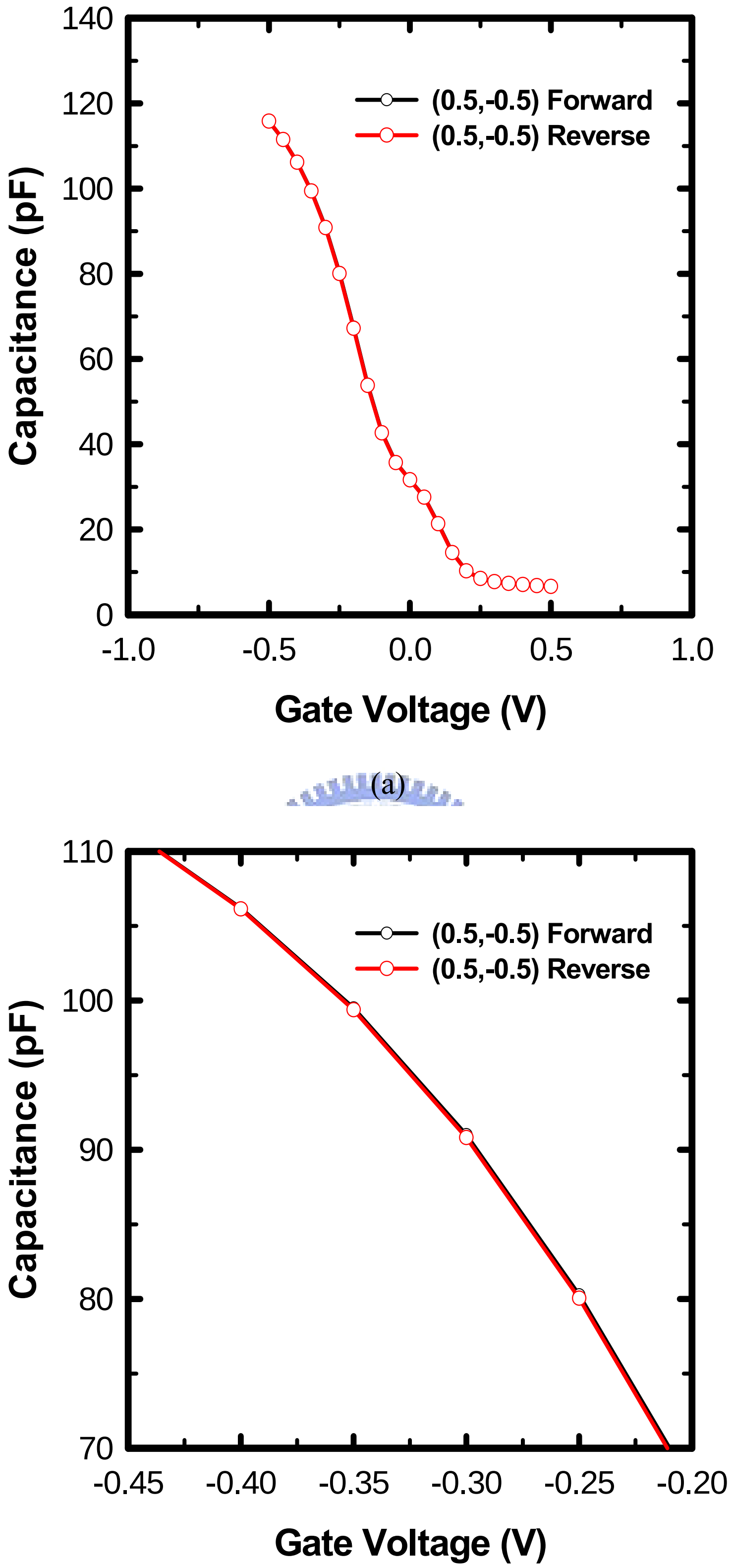


$$\text{Frequency Dispersion} \equiv \frac{\text{C (@10 KHz)-C (@1 MHz)}}{\text{C (@10 KHz)}} \times 100\,\%$$

Fig. 2-12 The C-V curve with different frequency sweep and the equation shows the definition of frequency dispersion percentage.

N_2O Pre-treatment	Dispersion (%)	NH_3 Pre-treatment	Dispersion (%)
No RTA	21.45	No RTA	19.73
Oxide RTA-900oC-10s	14.79	Oxide RTA-900oC-10s	8.386
Oxide RTA-950oC-10s	6.341	Oxide RTA-950oC-10s	7.259
Oxide RTA-1000oC-10s	4.552	Oxide RTA-1000oC-10s	1.016
Spike RTA-900oC	17.93	Spike RTA-900oC	18.14
Spike RTA-950oC	18.83	Spike RTA-950oC	18.77
Spike RTA-1000oC	18.09	Spike RTA-1000oC	20.52

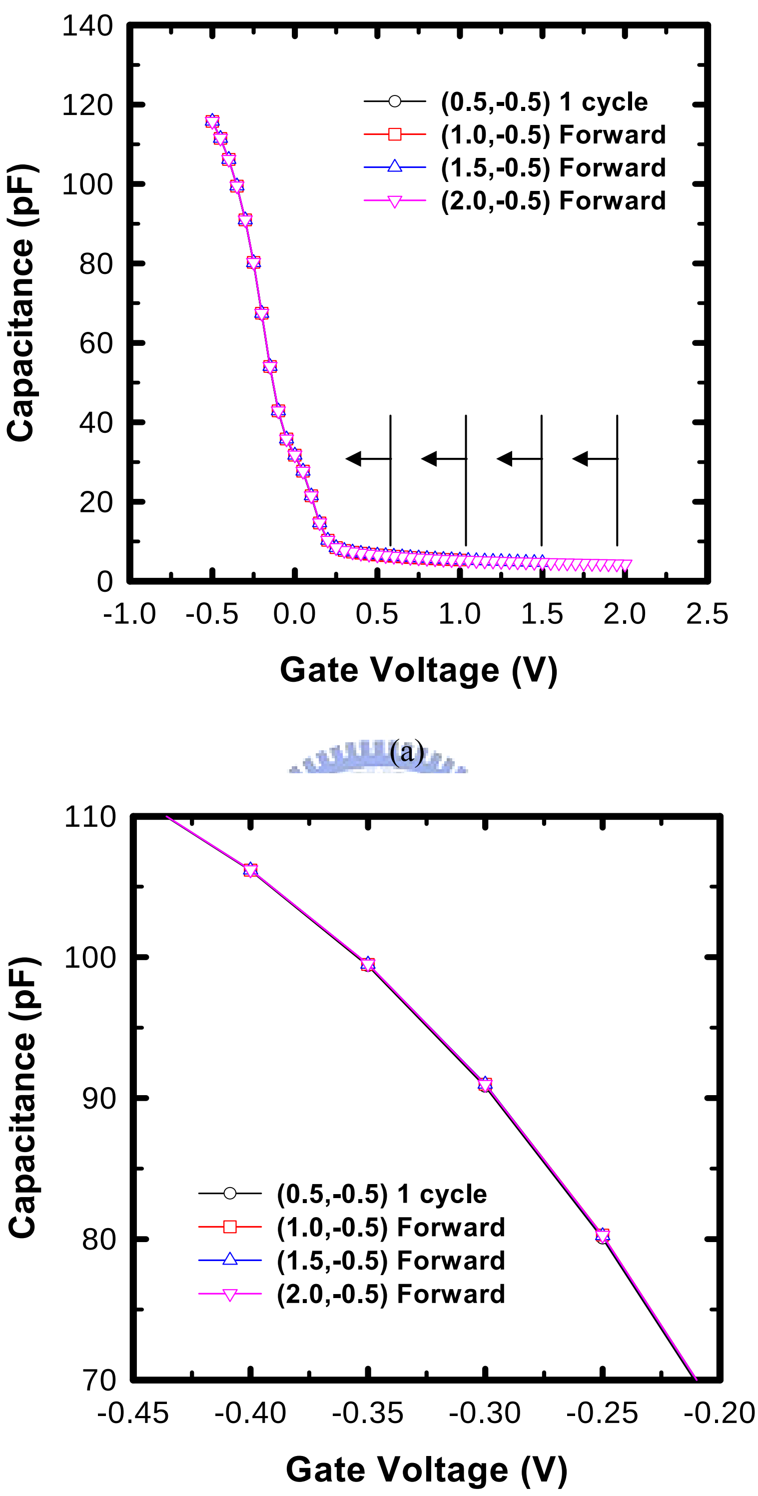
Table 2-1 Hysteresis comparison of different annealing temperature with N_2O/NH_3 plasma pre-treatment by oxide RTA and spike RTA



(a)

(b)

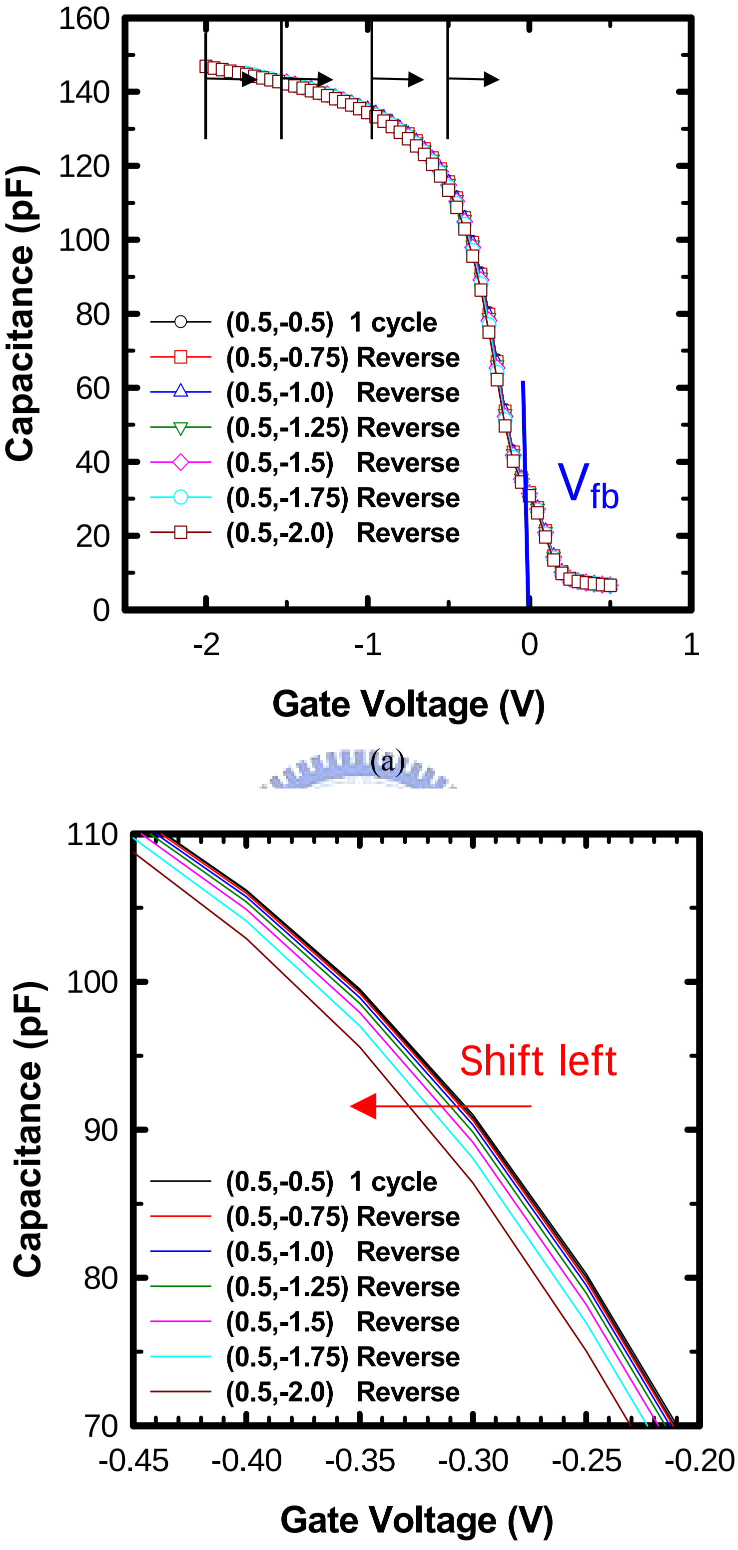
Fig. 2-13 The (a) C-V curve and (b) Zoom in figure of (a) with RTO I.L. Sweep range is (+0.5V, -0.5V) for one cycle sweep (first from inversion to accumulation and then from accumulation to inversion).



(a)

(b)

Fig. 2-14 The (a) C-V curve and (b) Zoom in figure of (a) with RTO I.L. Inversion sweep range is increasing form 0.5 V to 2V with a step of 0.5.



(a)

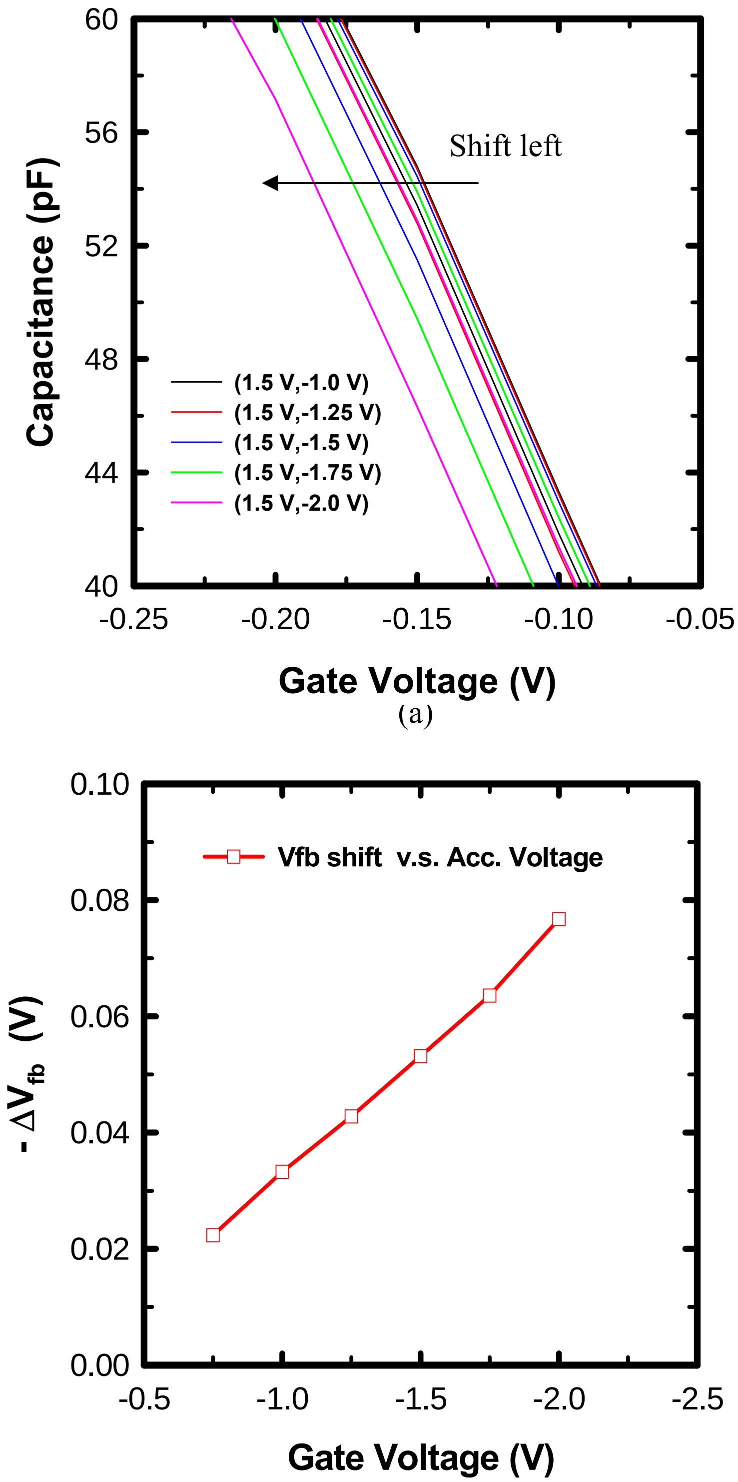
(b)

Fig. 2-15 The (a) C-V curve and (b) Zoom in figure of (a) with RTO I.L. Accumulation sweep range is increasing form -0.5 V to -2V with a step of 0.5.

N_2O Pre-treatment	**Hysteresis**	**NH_3 Pre-treatment**	**Hysteresis**
No RTA	**-60.1mV**	No RTA	**-50.3mV**
Oxide RTA-900℃-10s	**-55.2mV**	Oxide RTA-900℃-10s	**-46.8mV**
Oxide RTA-950℃-10s	**-53.3mV**	Oxide RTA-950℃-10s	**-45.5mV**
Oxide RTA-1000℃-10s	**-52.0mV**	Oxide RTA-1000℃-10s	**-45.3mV**
Spike RTA-900℃	**-57.8mV**	Spike RTA-900℃	**-56.3mV**
Spike RTA-950℃	**-56.9mV**	Spike RTA-950℃	**-55.9mV**
Spike RTA-1000℃	**-56.3mV**	Spike RTA-1000℃	**-56.1mV**

- As deposition sample, hysteresis ~ 67.5mV
- RTO I.L., hysteresis ~ 50.13mV

Table 2-2 Hysteresis comparison of different annealing temperature with N_2O/NH_3 plasma pre-treatment by oxide RTA and spike RTA.



(a)

(b)

Fig. 2-16 (a) The zoom in plot of the hysteresis of C-V curve with fixed inversion voltage and various accumulation. (b) shows the relationship between flatband shift and accumulation voltage.

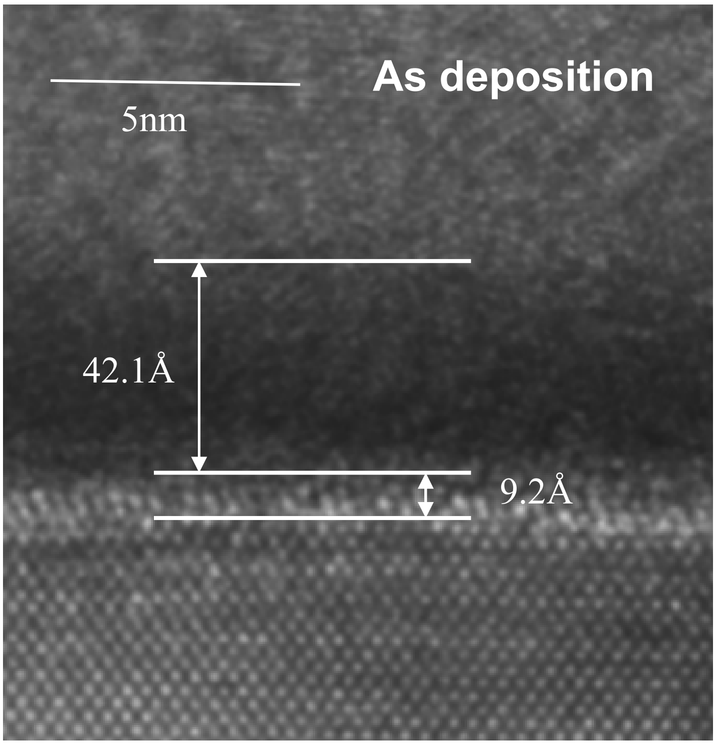
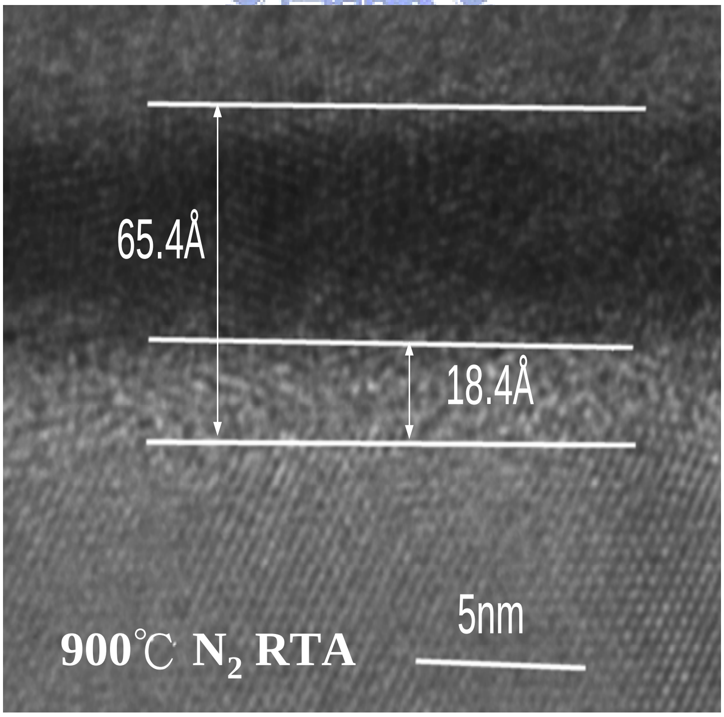


Fig. 2-17 The HRTEM image shows the as-deposited sample.



(b)

Fig. 2-18 The HRTEM image shows the sample with NH_3 pre-treatment and oxide RTA N_2 900℃ annealing.

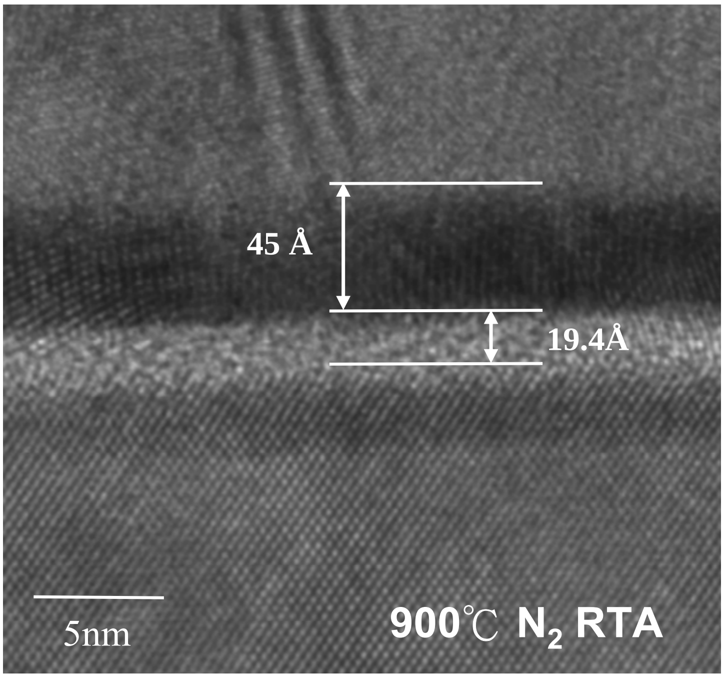
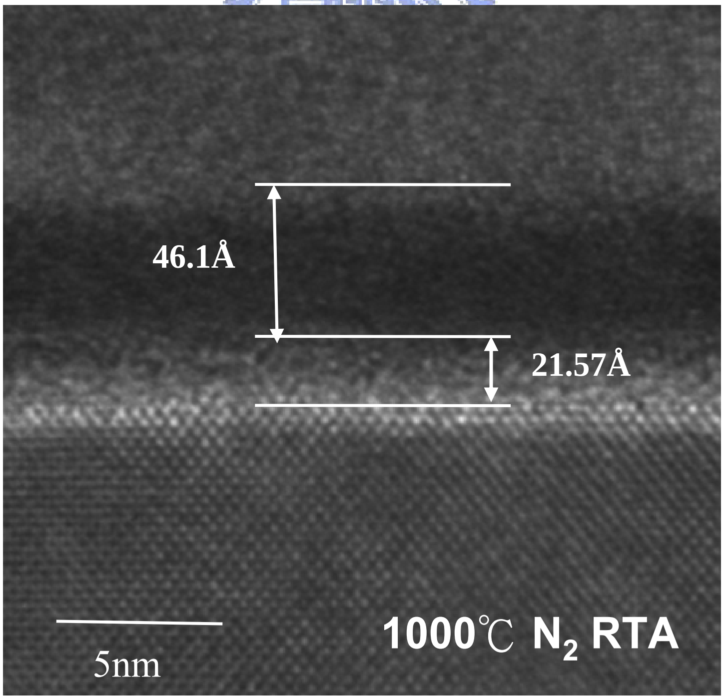


Fig. 2-19 The HRTEM image shows the sample with NH_3 pre-treatment and oxide RTA N_2 950℃ annealing.



(d)

Fig. 2-20 The HRTEM image shows the sample with NH_3 pre-treatment and oxide RTA N_2 1000℃ annealing.

Chapter 3

Reliability Issues and Charge Trapping Characteristics of HfO_2 Gate Dielectrics

3-1 Introduction

As CMOS devices are scaled aggressively into nanometer regime, SiO_2 gate dielectric is approaching its physical and electrical limits. One of the primary scaling issues is the intolerably huge leakage current caused by the direct quantum tunneling of carriers through these ultra thin oxides.

To alleviate this problem, alternative gate insulators with higher permittivity than SiO_2 are currently extensively investigated for future generations of metal oxide semiconductor (MOS) transistors [1]–[6]. The use of dielectric layers with higher permittivity as the gate dielectric layer should allow the use of thicker films to achieve the same equivalent electrical thickness (as far as gate capacitance is concerned), and therefore reduced tunneling leakage current and improved reliability.

Among high-k materials under investigation, HfO_2 has been demonstrated to be highly attractive because of its relatively high dielectric constant (~25), sufficiently large band gap (~ 5.9 eV), suitable tunneling barrier height for both electrons and holes (>1 eV), and thermal compatibility with contemporary CMOS processes.

Even though HfO_2 films have been shown to be scalable to below 1nm, [7] there still exists several issues that need to be tackled before they can eventually replace SiO_2 dielectric in ULSI production. One of the most important issues for HfO_2 is the charge trapping, which leads to threshold voltage instability [8]-[12]. While the other is reliability, which is crucial for any practical electronic product.

In this work, we first discuss the reliability issues for HfO_2 films with three different processing conditions, including N_2O pre-treatment followed by 900℃ N_2 RTA, NH_3 pre-treatment followed by 900℃ N_2 RTA, and spike rapid thermal oxide (~11Å) as interfacial layer. All samples have approximate equivalent oxide thickness (EOT). We find that the samples with NH_3 pre-treatment or N_2O pre-treatment depict improved leakage current and breakdown voltage (or $E_{BD(eff)}$) over the RTO control. While the sample with NH_3 pre-treatment show the best charge to breakdown (Q_{BD}), and characteristic life time.

Then, we investigate the characteristics of charge trapping in the HfO_2/SiO_2 gate stack with TiN gate electrode. Contrary to most previous reports [8]-[12], we found that hole trapping, rather than electron trapping, prevails in the HfO_2/SiO_2 gate stack during constant voltage stressing (CVS). By employing the distributed capture cross section model, [8]-[9] the behavior of hole trapping can be well predicted over several decades of stress time, i.e., charge trapping is caused by the hole filling of as-fabricated traps with distributed capture cross section. This phenomenon is consistent with the work function level of TiN that results in a band structure with asymmetric barriers for holes and electrons. With resultant shorter tunneling path, holes become the dominant component in the current flow and, therefore, lead to the prevalence of hole trapping.

Finally, we propose pre-existing trap precursors (or latent traps) in HfO_2 high-k dielectrics to explain the observed current transport mechanisms. When we measure I-V characteristics on virgin samples under various temperatures, the current density is insensitive to temperature. However, when we first stress the sample under constant voltage stress (CVS) for certain duration (-4.0V, 600s), the gate current density becomes strongly temperature dependent at low voltage, albeit much less dependent on temperature at higher voltage. These results are consistent with Frenkel-Poole emission. And if we perform CVS with a duration of 2300 seconds at -4.0V (a condition known to fill all the existing hole traps), I-V curves again become insensitive to temperature. This can prove again that flatband voltage shift (ΔV_{fb}) is mainly caused by the trap filling instead of the trap creation

3-2 Experimental Procedure

Metal-oxide-semiconductor (MOS) capacitors with HfO_2 high-k dielectric were fabricated on p-type (100)-oriented silicon wafers with local oxidation of silicon (LOCOS) isolation. After HF-last dipping, three samples were processed with different pre-treatment conditions. The first split is high density plasma (HDP) N_2O pre-treatment followed by 900°C N_2 RTA. The second split is HDP NH_3 pre-treatment followed by 900℃ N_2 RTA. While the last split is an ultrathin spike rapid thermal anneal (RTA) at 800 °C in an O_2 ambient (RTO interfacial layer). Subsequently, an HfO_2 film of approximately 5 nm was deposited by atomic vapor deposition (AVD^{TM}) in an AIXTRON Tricent® system at a substrate temperature of 500 °C, followed by N_2 RTA at 500 °C for 30 sec. A 5000 Å TiN electrode was sputtered and patterned to form gate electrodes. Then, wafers were sputtered with aluminum on the backside, and received a forming gas anneal at 400 °C for 30 min. The physical thickness of the interfacial oxide layer and HfO_2 film as determined from transmission electron microscopy (TEM) are 11 Å and 49 Å, respectively. The equivalent oxide thickness (EOT) of the stack and initial flatband voltage before stressing are estimated to be 24 Å and -0.005 V from the high-frequency (100 kHz) C-V curves using UCLA CVC method without considering quantum effect [13].

3-3 Results and Discussions

3-3-1 Reliability Results

Figs. 3-1(a) & (b) show typical J-V curves and Weibull plots for samples with three different pre-treatments, respectively. All samples have similar EOT values. It can be seen that samples with either N_2O or NH_3 pre-treatment show comparable leakage characteristics, which are much lower than the RTO interfacial layer sample. This can be explained by HRTEM images shown in Fig. 3-2. As shown in Fig.3-2, N_2O pre-treatment results in a thicker interfacial layer than the RTO control (i.e., 1.5nm vs. 1.1 nm). The samples with plasma pre-treatments may incorporate N atoms into the interfacial layer and result in a higher k value. However, with a thicker interfacial layer, the leakage current is reduced. Fig. 3-3 shows the effective breakdown field ($E_{BD\ (eff)}$) after subtracting V_{fb} voltage. The samples with plasma pre-treatments indeed have higher $E_{BD\ (eff)}$ than the RTO control, duo to a thicker interfacial layer.

Fig. 3-4 exhibits the time-to-breakdown characteristics for three samples. We can see that the sample with NH_3 pre-treatment has the longest breakdown time, while the sample with N_2O pre-treatment the shortest, as illustrated in Fig. 3-5 plotted under the same stress voltage (-4.6 V).

Fig. 3-6 shows the charge-to-breakdown (Q_{BD}) of the samples under -4.8V stress voltage. NH_3 pre-treatment has higher charge-to-breakdown than RTO and N_2O pre-treatment.

Therefore, from reliability concern, NH_3 pre-treatment is better than N_2O pre-treatment. A possible reason may be due to the NH_3 plasma being more uniform in HDP system than N_2O plasma.

3-3-2 Characteristics of Hole Trapping in HfO_2/SiO_2 Gate Stack with TiN Electrode

Figure 3-7 (a) shows a set of C-V curves of a MOS capacitor measured after different CVS times. The stress voltage was – 3.5 V, i.e., gate injection polarity. It is clearly observed that the C-V curve gradually shifts toward negative voltage with increasing stress time. This tendency indicates that hole trapping, rather than electron trapping, is the predominant process in the gate stack during stressing. However, the negative flatband voltage shift (ΔV_{fb}) may arise from the emergence of positive bulk trapped charges and/or interface charges. In order to clarify the mechanism responsible for the hole trapping, the conductance of the capacitor is plotted against measuring voltage over several decades of stress time, as shown in Fig. 3-7 (b). It is found that the conductance peak value only changes slightly with stress time. This suggests that charge trapping at the interface states does not play any significant role in flatband voltage shift for the HfO_2/SiO_2 gate stack during CVS [14]. Thus, we conclude that the flatband voltage shift is mainly caused by hole trappings in the bulk of HfO_2 layer, rather than at the SiO_2/Si interface. This result seems to contradict with most previous works, in which electron trappings in the high-k stacks were shown to be the dominant mechanism responsible for the threshold and flatband voltage shifts [9]-[12].

To gain further insight into the trapping mechanism, we assume that the hole trapping is attributed to filling of pre-existing traps in the high-k dielectrics without the creation of additional trap centers, and employ the so-called distributed capture cross section model or stretched exponential model [8]-[9] to describe the trapping behavior in our high-k gate stacks. The stretched exponential equation is given by

$$|\Delta V_{fb}| = |\Delta V_{max}|\bullet(1-\exp(-t/\tau_0)^{\beta}), \qquad (3\text{-}1)$$

where $|\Delta V_{max}|$, τ_0, β are fitting parameters which are related to the total trap density. Here, τ_0 represents the characteristic time constant of the distribution, and $|\Delta V_{max}|$ denotes the maximum shift in $|\Delta V_{fb}|$ that occurs after prolonged stressing. Fig. 3-8 shows the dependence of ΔV_{fb} on stress time. It can be clearly seen that the fitting curves (i.e., solid curves) match very well with experimental data (i.e., symbols) over several decades of stress time. In addition, $|\Delta V_{fb}|$ saturates at longer stress time when the magnitude of the stress voltage is higher than |-3.5V|. These features support our assumption of filling existing hole traps in the high-k gate stacks. Since the parameter β is a measure of the distribution width, the value of around 0.184 for all stressing conditions indicates that hole traps in the high-k gate stacks possess larger distributed capture cross section than that of electron traps (c.f., $\beta\sim 0.32$) [12]. Moreover, it is worthy to note that $|\Delta V_{fb}|$ increases again as the stress time is longer than 10000 s at $V_g = -4.2$ V. This phenomenon is thought to be due to additional traps creation. Therefore, we would like to conclude that trap filling model in the high-k gate stack is only suitable within certain specific voltage range, which may strongly depend on the quality of the high-k film.

Not disregarding the success of the distributed capture cross section model in describing the flatband voltage shift during CVS, it is still necessary to explain why the hole trapping is more likely to take place in our high-k gate stacks. We believe this can be explained by the resultant band diagram of the TiN/HfO_2/SiO_2 gate stack system under $V_g = -4.2$ V stress, as illustrated in Fig. 3-9. The parameters, including physical thickness, band offsets and voltage drops across the individual insulators were determined based on our TEM analyses (not shown) and the work function of TiN (~ 4.8 eV) was adopted from previous researches [15]-[16]. From the band diagram, it can be seen that the probability of hole tunneling from the substrate is much higher than that of electron tunneling from the gate because of the shorter tunnel distance. Therefore, the leakage current is dominated by hole injection. To reinforce this argument, the characteristics of the gate current density (J_g) as a function of injected charge density (Q_{inj}) for different CVS conditions were monitored and shown in Fig. 3-10. It can be seen that the leakage current decreases with increasing stress time for various applied voltages. This is consistent with hole dominance in the gate stack because only the trapped holes can cause leakage increase if the hole current is the dominant component.

Fig. 3-11 shows the flatband voltage shift versus injection charge. Similar trend to Fig. 3-8 is observed, and flatband voltage shift will eventually saturate if the injection charge continue to increase. Fig.3-12 shows the injection charge as a function of time. Fig. 3-13 shows the trapped charge versus time. The amount of trapped charges increases with stress voltage and time. At higher voltage (- 4.0V), the saturation phenomenon is observed at about 2300 s.

Fig. 3-14 shows the trapped charge as a function of injection charge. The slope of the curve is defined as the trapping efficiency. Form the plot, the slope of curves is different for different stress voltages. This indicates that the trapping efficiency is dependent on stress voltage, as shown in Fig. 3-15.

In Fig. 3-16 we first apply a -3.6 V on capacitor for 1000s, causing some charges to be trapped in HfO_2 film. Then, we apply a +3.6 V for 1000s in an effort to de-trap the charges. From 3-16 (a), it can be seen that positive voltage does not change the flatband voltage. From Fig. 3-16 (b), it is found the trapped charges can not be totally detrapped even after a duration of 1000 s by positive voltage.

3-3-3 Pre-Existing Charges and Current Transport Mechanism

In Fig. 3-17 (a), the I-V curves are measured under various temperatures from 25 to 150 °C. The current remains essentially constant with increasing temperature. However, from previous sections, we know that flatband voltage shifts toward left and the leakage current reduces under constant voltage stress. Therefore, we first stress the sample under -4 V, 600 s stress and measure the I-V curves. It can be obviously seen that the current now increases with temperature. This again proves that the traps are latent and can be activated by applying a stress. Furthermore, traps which are passivated during processing are activated; meanwhile, the amount of holes which filled the traps is dependent on the stressing time.

Then we investigate the current transport mechanism. The current from Frenkel-Poole emission is of the form:

$$J=B*E\exp\left[\frac{-q(\phi_B-\sqrt{qE/\pi\varepsilon_i\varepsilon_{HfO_2}})}{k_BT}\right] \tag{3-2}$$

where B is a constant in terms of the trapping density in the HfO_2 film, φ_B is barrier height , E is the electric field in HfO_2 film, ε_i is free space permittivity, ε_{HfO2} is HfO_2 dielectric constant, k_B is Boltzmann constant, T is the temperature measured in Kelvin.

First, we define a parameter Z as below:

$$Z=\phi_B-\sqrt{\frac{qE}{\pi\varepsilon_i\,\varepsilon_{HfO_2}}} \tag{3-3}$$

Fig.3-18 (a) shows ln (J/E) as a function of 1000/T with different V_{stack} (=$Vg-V_{fb}-\psi s$), and the slope of these curves are defined in (3-3). Next, we plot Z versus $E^{1/2}$, as shown in Fig. 3-18(b), and the slope of the curve is

$$\sqrt{\frac{q}{\pi\varepsilon_i\varepsilon_{HfO_2}}}, \tag{3-4}$$

where q, π, ε_i, are known, the dielectric constant of HfO_2 can be calculated and the value is found to be 15.6. The value is very close to the estimated value from HRTEM image, which is 14.7. This result demonstrates that Frenkle-Poole emission of holes is dominant in HfO_2 film, and the energy band diagram is shown in Fig. 3-19. In this figure, traps can be classified into two types, shallow traps and deep traps, and both of them followed the distributed capture cross section model from prior section. The holes trapped by deep traps cause the flatband voltage shift and the holes trapped by shallow traps can easily hop over the barrier through the HfO_2 film and cause the leakage current [14].

Since from Fig. 3-8, flatband voltage shift becomes saturated under -4.0 V stress voltage of about 2000 s, and we have proposed that the holes are trapped in pre-existing traps and eventually fully filled after a certain stress of time. To validate this point, we measure the I-V characteristics of a sample that was previously stressed at -4.0 V for 2300 s (i.e., the existing hole traps in the sample are activated and presumably filled), and the current is again less dependent on temperature. This can be also explained by Fig. 3-19. The deep traps are now activated and filled with holes and the trapped holes cause the barrier height of shallow traps to become “more shallower”. Therefore, the holes can easily go through at room temperature, and the leakage current becomes less dependent on the temperature.

3-4 Summary

In this chapter, we first investigated the reliability issues for HfO_2 samples subjected to NH_3 or N_2O HDP plasma surface pre-treatments, and compared with those on HfO_2 control samples with conventional oxide interfacial layer. The samples with plasma surface pre-treatment show much lower leakage current, higher breakdown voltage and higher effective breakdown field, due to incorporated nitrogen in interfacial layer. For time-to-breakdown and charge-to-breakdown characteristics, NH_3 and N_2O plasma pre-treatments show improved and degraded performance over RTO control, respectively.

Next, we studied hole trapping in HfO_2/SiO_x gate dielectrics stack. We proposed that hole trapping occurs through filling of pre-existing hole traps in HfO_2 film, and we employed continuous capture cross section model to fit our experimental data. The fitting results match well with experimental data, and the fitting parameter β possesses larger distributed capture cross section than that of electron traps. We also used energy band diagram to illustrate our viewpoint.

Finally, we studied the current transport mechanism responsible for the leakage current in HfO_2 films. Since the pre-existing (latent) traps were passivated during processing so the leakage current in the virgin sample is almost independent of the measuring temperature. When we applied a stress to the thin film, these traps will be activated and the samples depict leakage characteristic of Frenkel-Poole emission.

3-5 Reference

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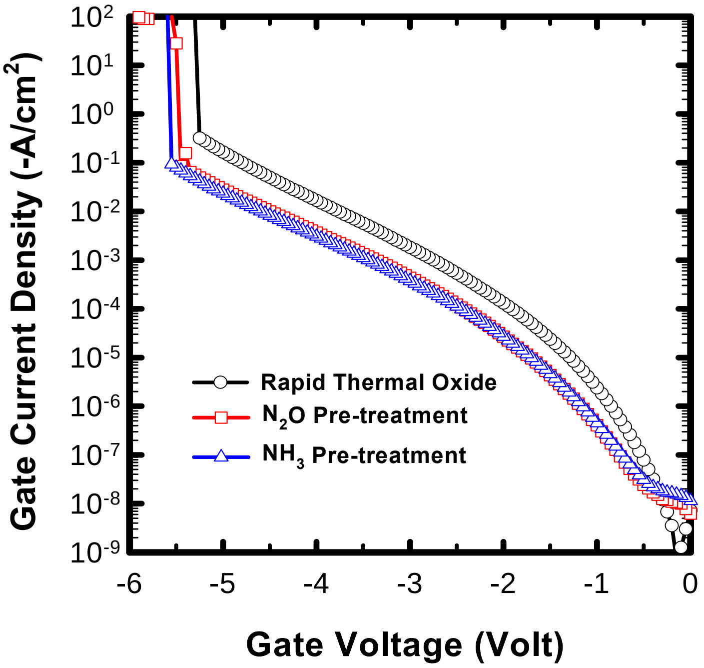


Fig. 3-1(a) The J-V characteristics with different I.L. treatment method (RTO, N_2O, NH_3) at same post-treatment annealing (900°C).

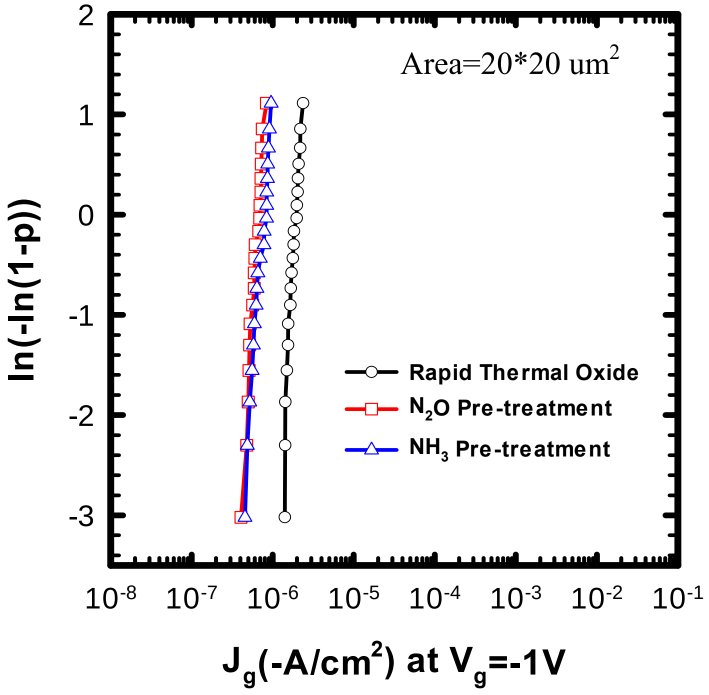


Fig. 3-1(b) The Weibull plot shows the gate current densities at Vg=-1V with different I.L. treatment method (RTO, N_2O, NH_3).

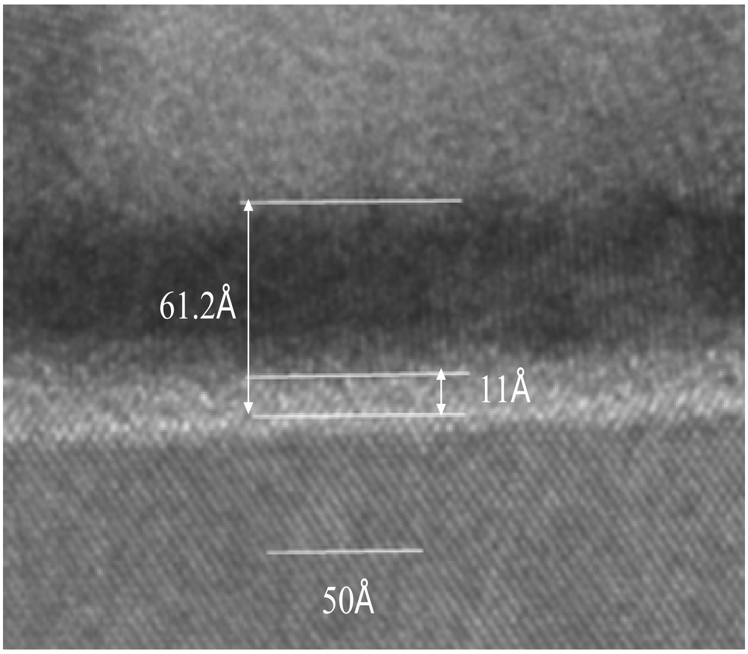


Fig. 3-2 (a) The TEM image of the HfO_2 with RTO I.L.

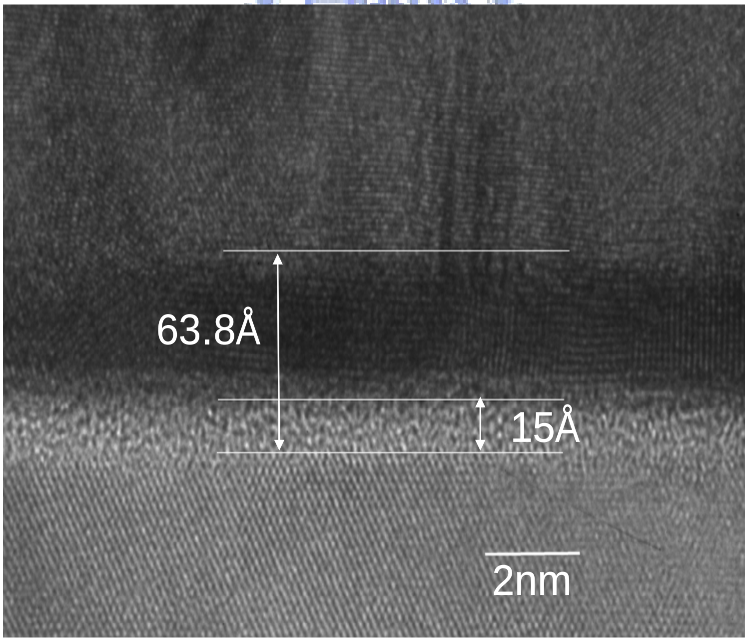


Fig. 3-2(b) The HRTEM image of the HfO_2 with N_2O

pre-treatment and 900℃ N_2 RTA annealing.

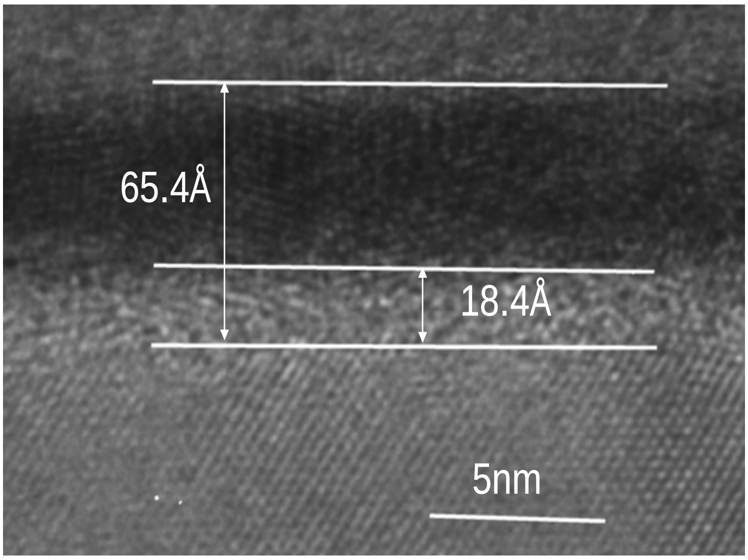


Fig. 3-2(c) The HRTEM image of the HfO$_2$ with NH$_3$ pre-treatment and 900℃ N$_2$ RTA annealing.

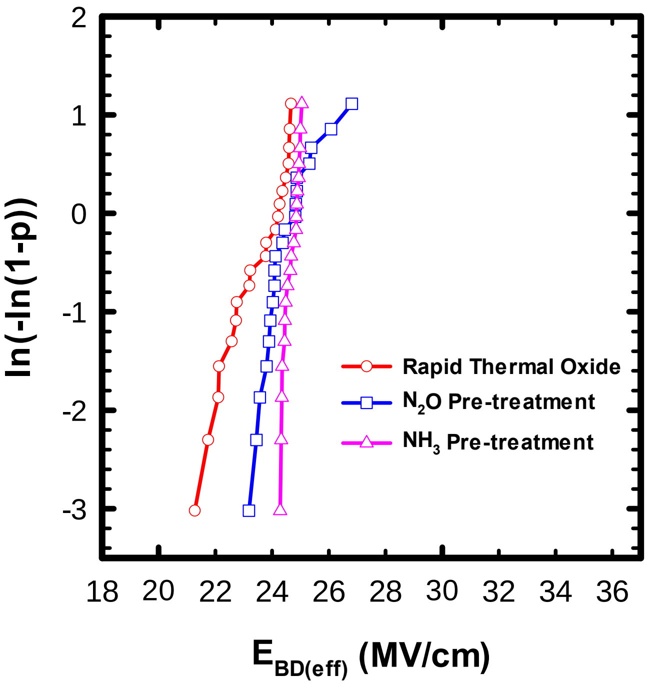
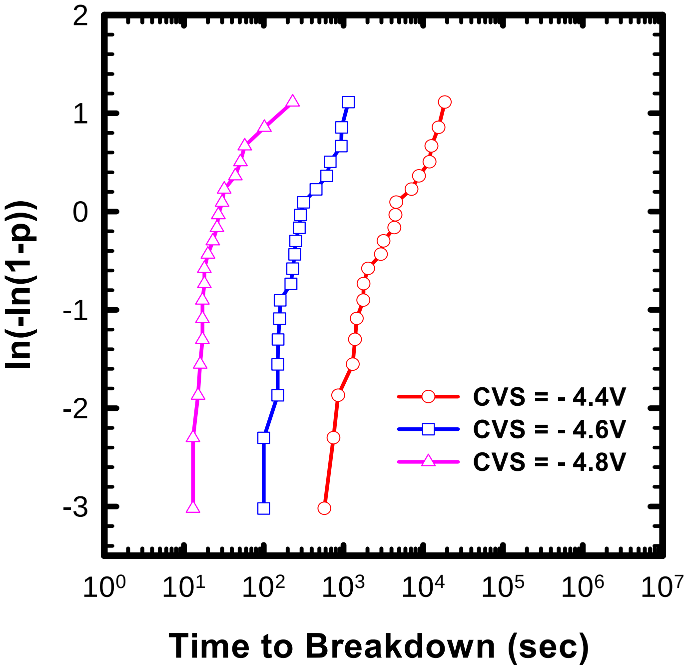
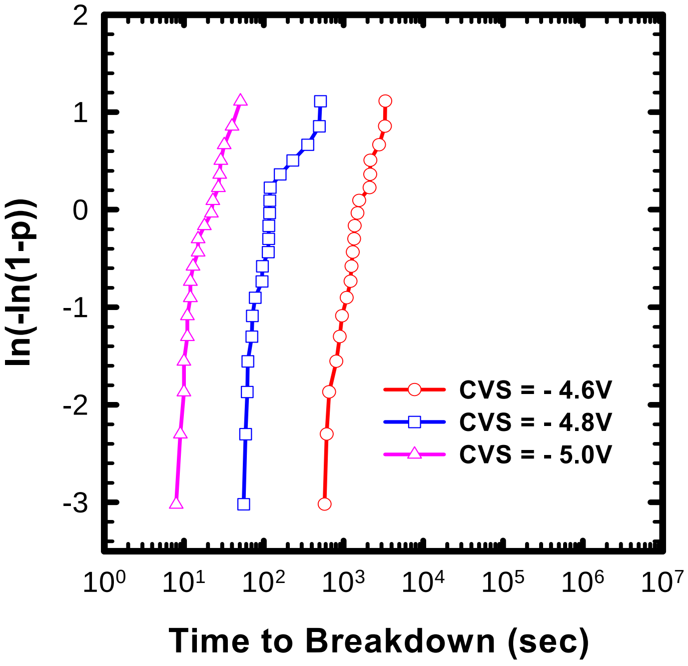


Fig. 3-3 The Weibull plot shows the effective breakdown field with different I.L. treatment method (RTO, N$_2$O, NH$_3$) at same post-treatment annealing (900°C).



(a)



(b)

Fig. 3-4 The Weibull plot shows the time to breakdown under three constant stresses voltages with (a)NH_3 (b)N_2O pre-treatment followed by 900°C post-nitridation annealing.

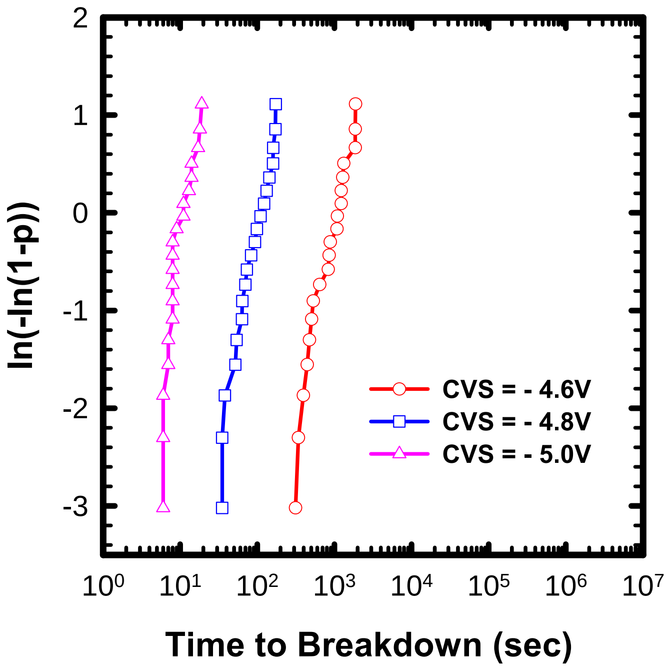


Fig. 3-4 (c) The Weibull plot shows the time to breakdown under three constant stress voltages with RTO interfacial layer.

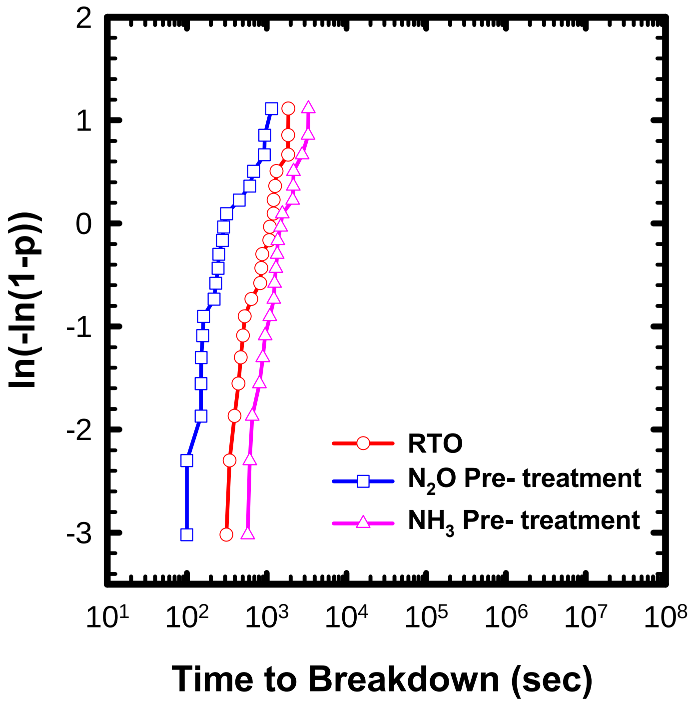


Fig. 3-5 The Weibull plot shows the time to breakdown under -4.6V stress voltage with different I.L. treatment method (RTO, N_2O, NH_3).

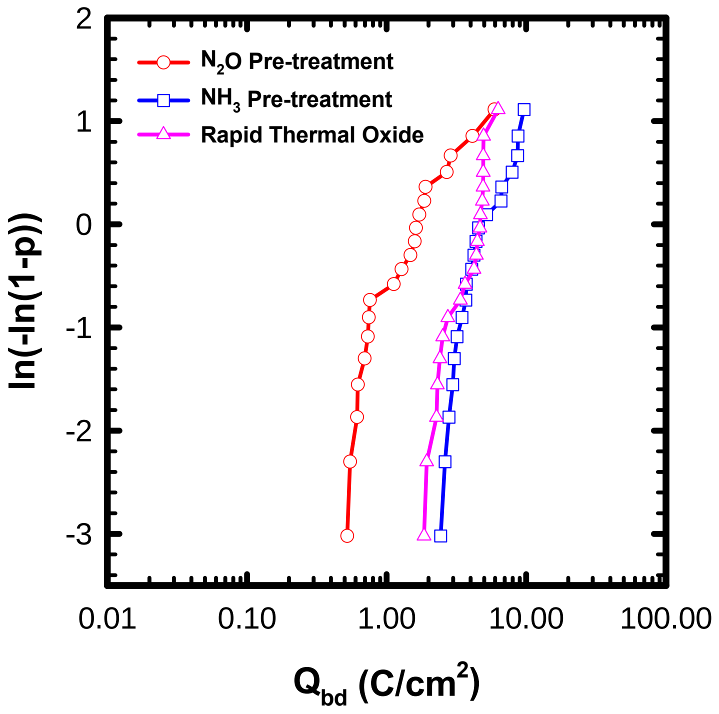


Fig. 3-6 The Weibull plot shows the charges to breakdown under -4.8V stress voltage with different I.L. treatment method (RTO, N_2O, NH_3).

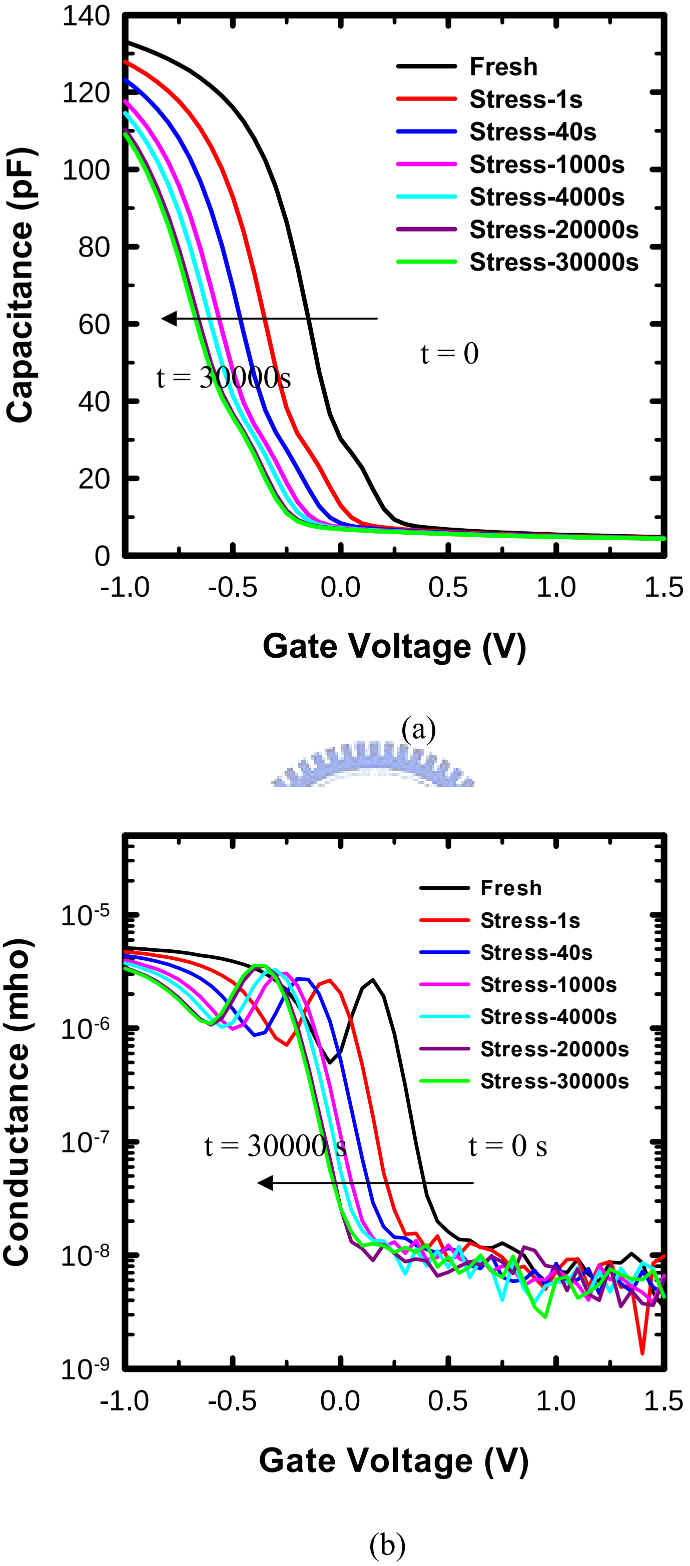


Fig. 3-7 (a) C-V curves and (b) G-V curves measured at 100 kHz with increasing stress time as a parameter. The stress voltage (V_g) was– 3.5 V. The curve labeled t = 0 s corresponds to the data before stressing.

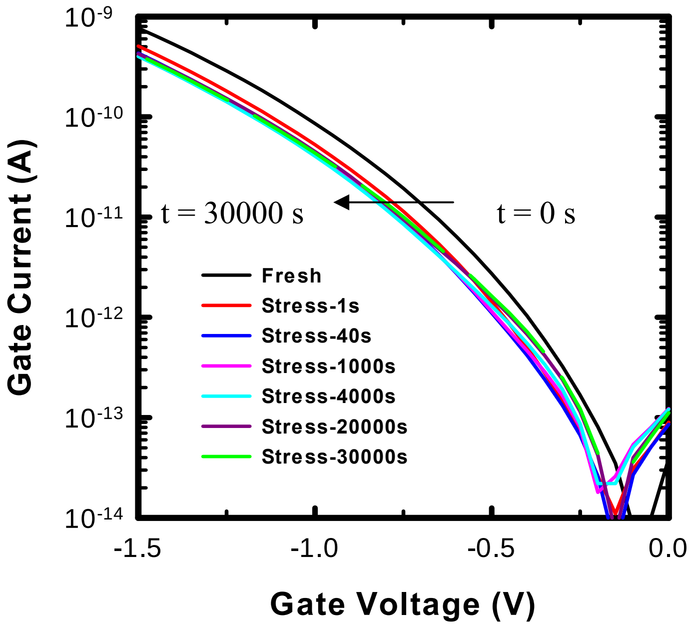


Fig. 3-7 (c) I-V curves measured with increasing stress time. The stress voltage (V_g) was– 3.5 V. The curve labeled t = 0 s corresponds to the data before stressing.

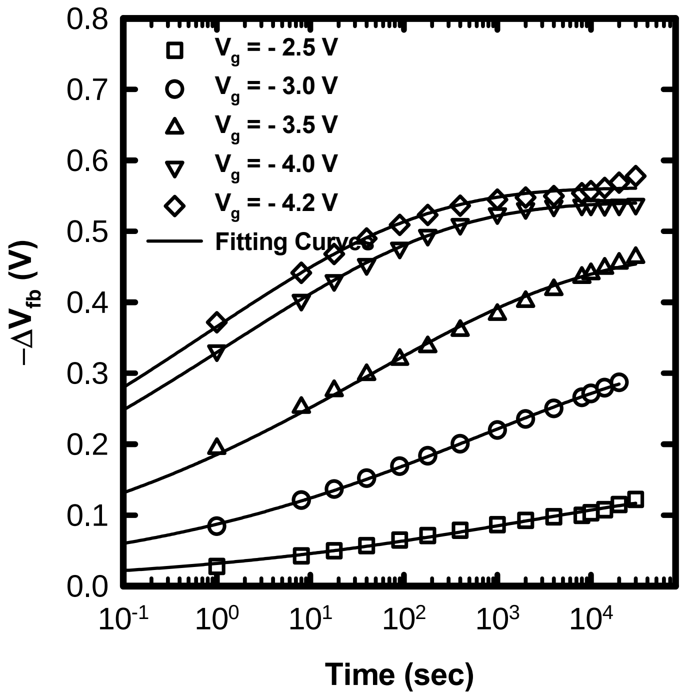


Fig. 3-8 Flatband voltage shift v.s. time for RTO I.L. under different constant voltage stress (CVS). Symbols are experimental data, and solid lines are fitting curves.

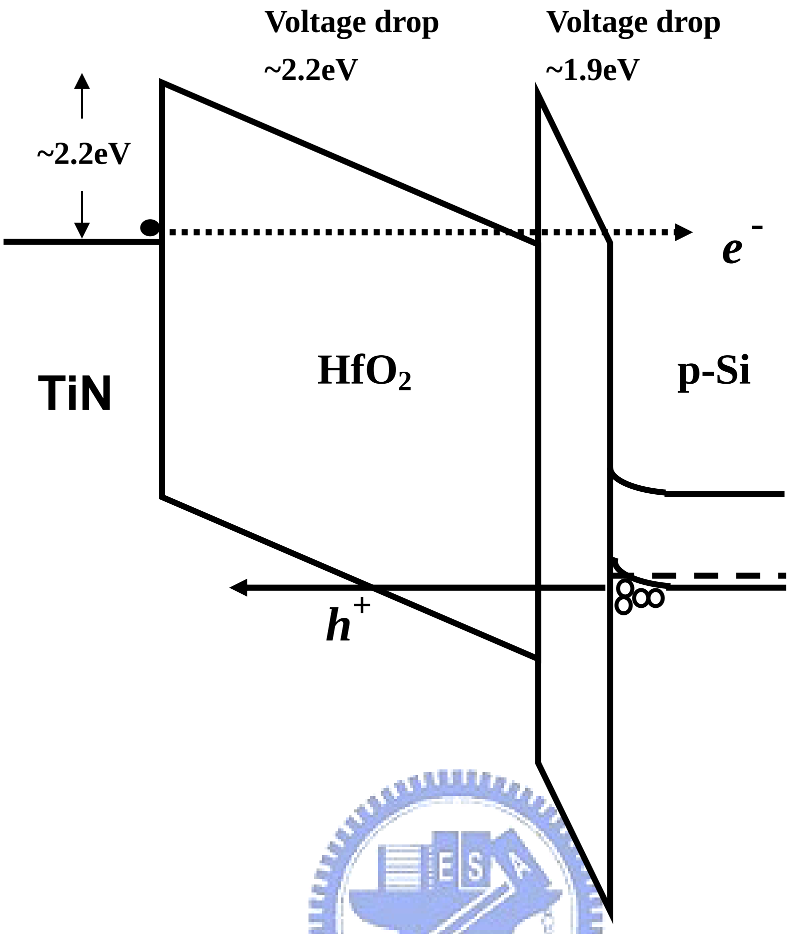


Fig. 3-9 Energy diagram of HfO_2/SiO_2 gate stack capacitor with mid-gap TiN metal gate electrode under constant voltage stress (V_G = – 4.2V).

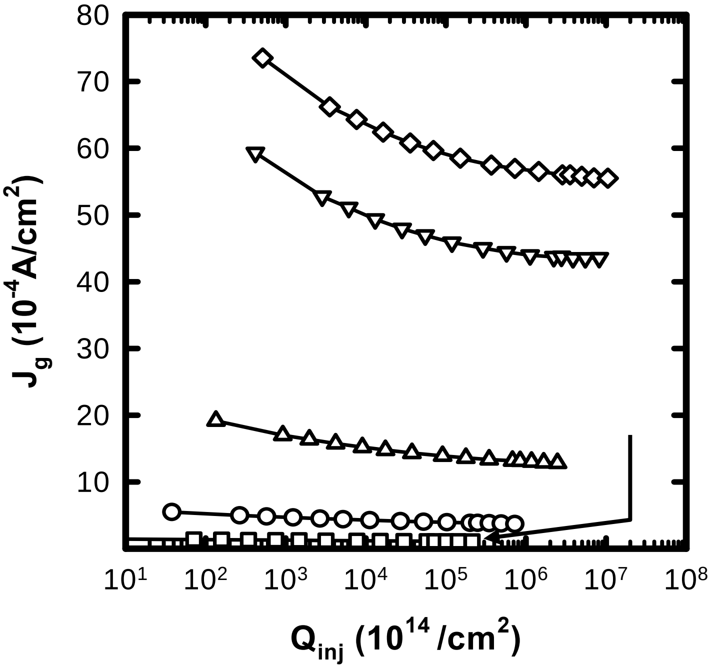


Fig. 3-10 Gate current density as a function of injection charge density for various stress voltages.

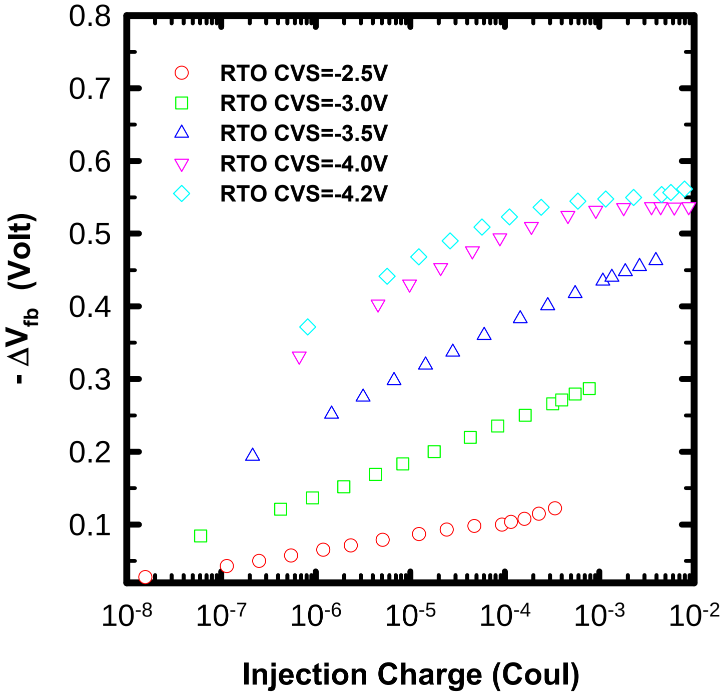


Fig. 3-11 Flat band voltage shift v.s. injection charge for RTO Interfacial layer under different Constant voltage stress

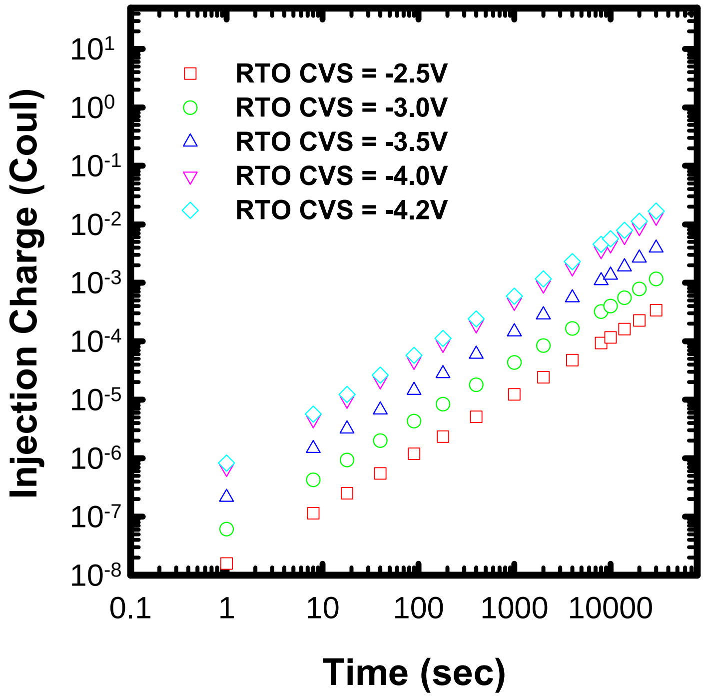


Fig. 3-12 Injection charge v.s. Time for RTO interfacial layer

under different Constant voltage stress (CVS).

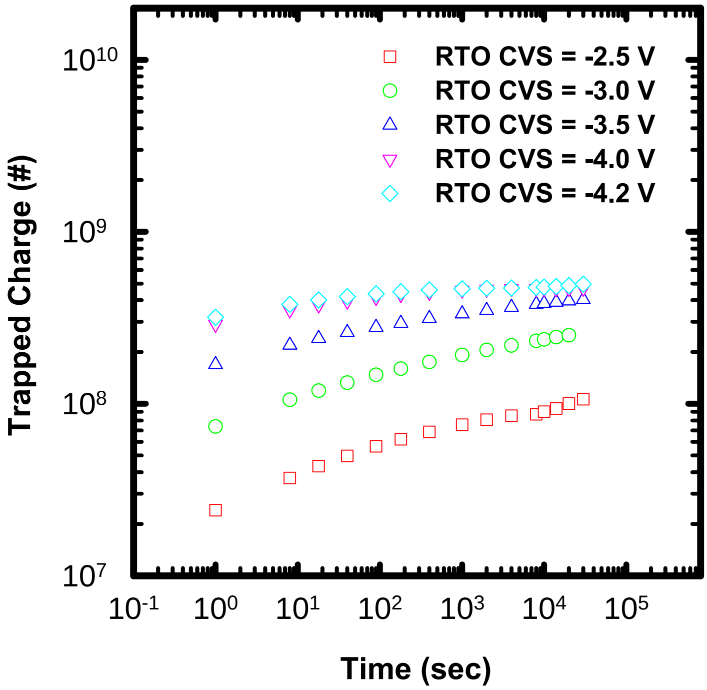


Fig. 3-13 Trapped charge v.s. time for RTO interfacial layer

under different constant voltage stress (CVS).

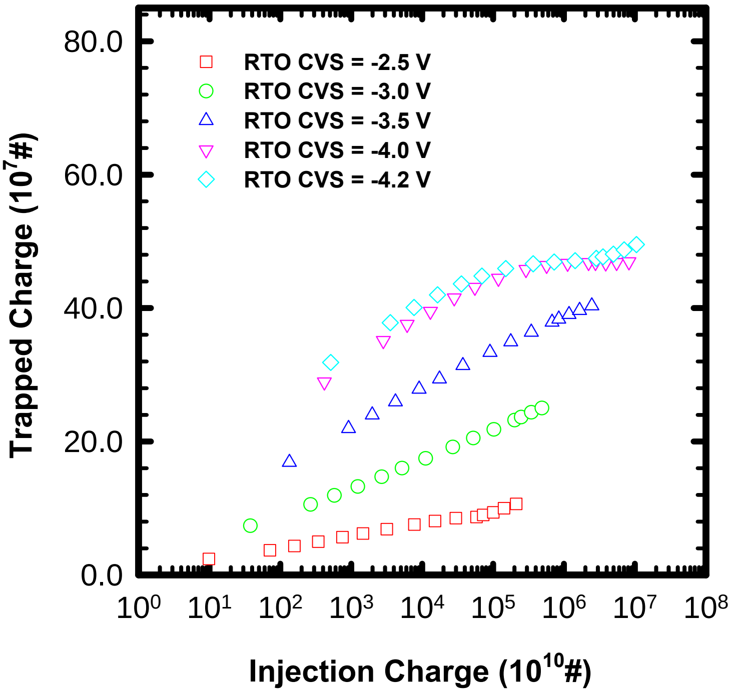


Fig. 3-14 Trapped charge v.s. injection charge for RTO interfacial layer under different constant voltage stress (CVS)

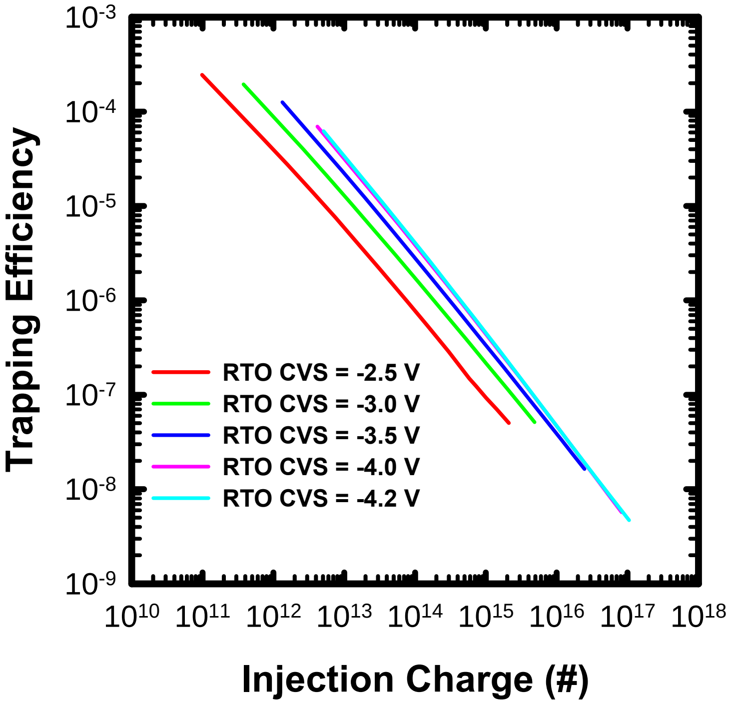
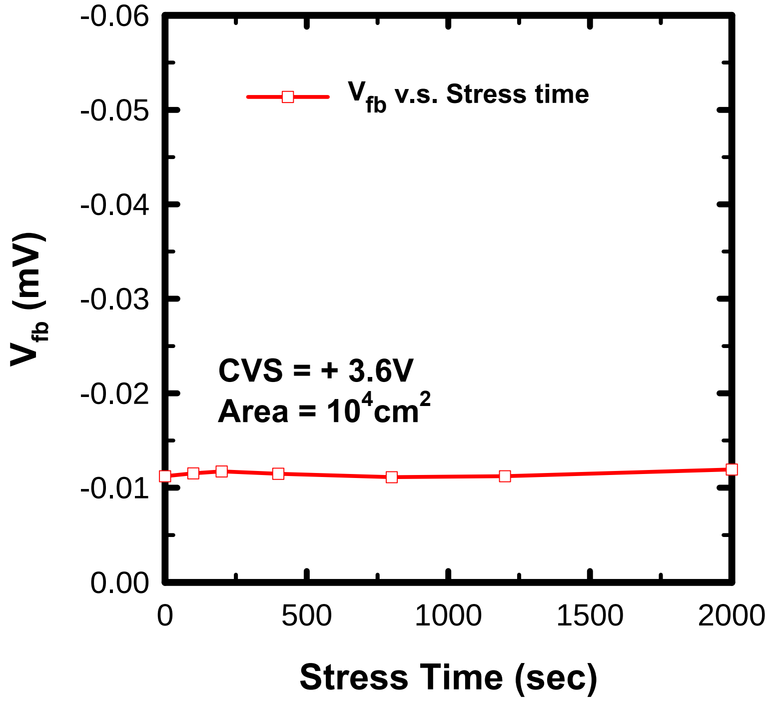
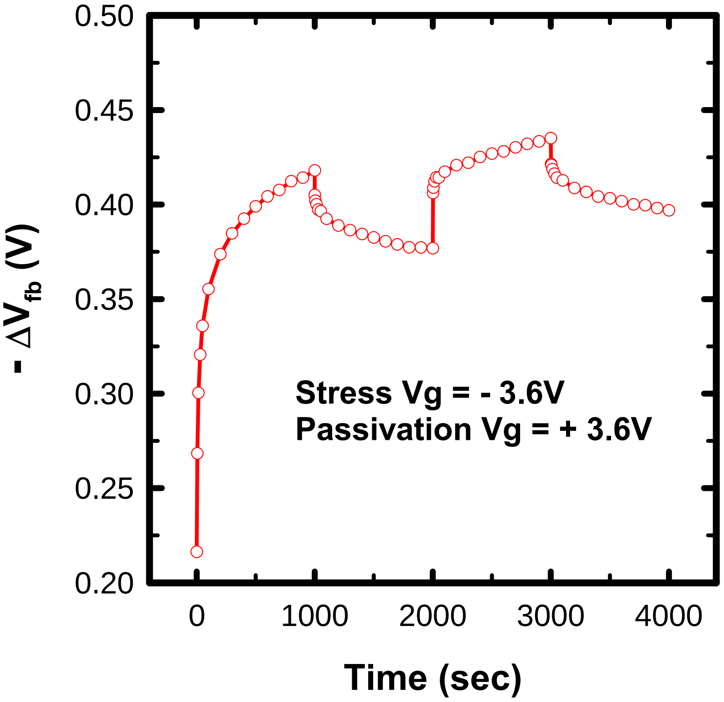


Fig. 3-15 Trapping efficiency v.s. Injection Charge for RTO interfacial layer under different constant voltage stress (CVS).

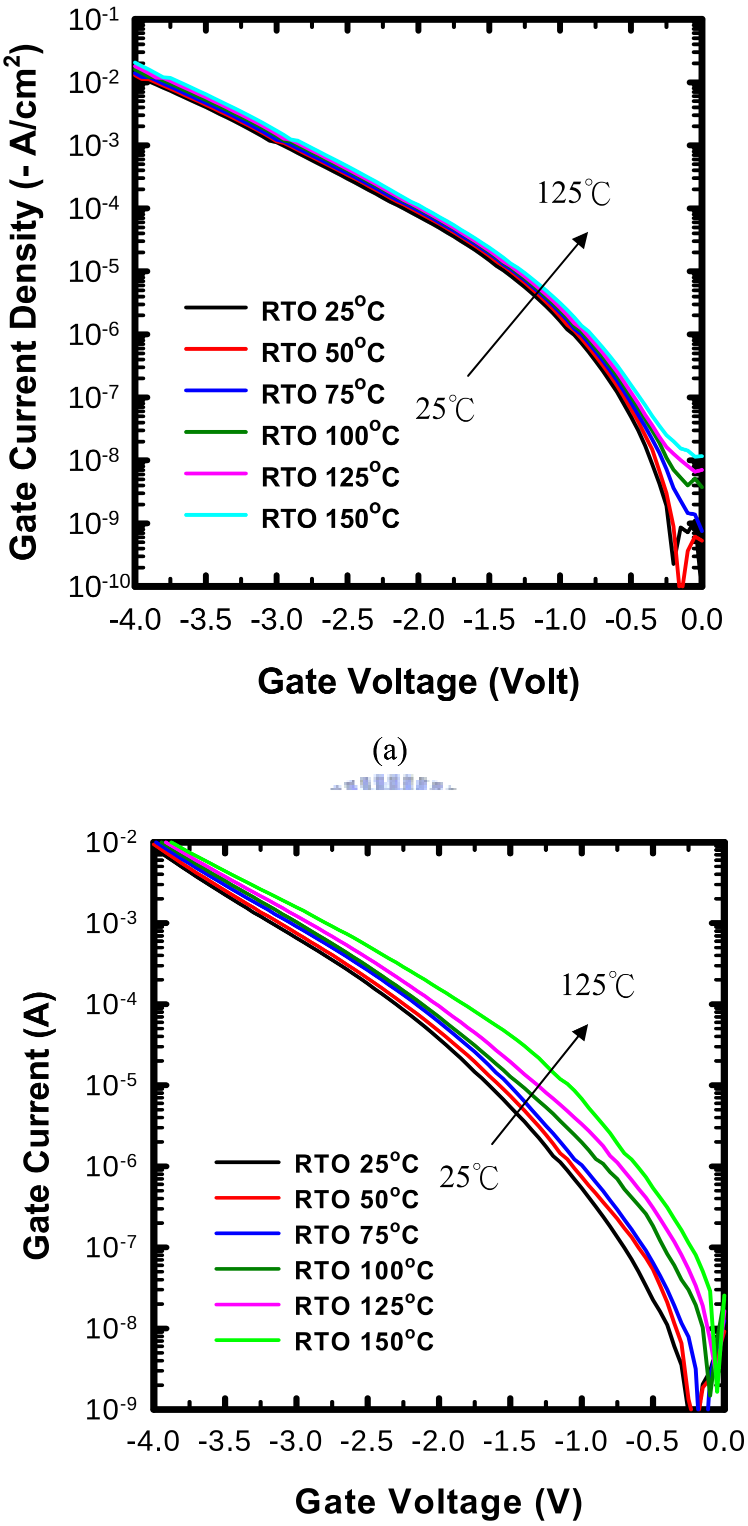


(a)



(b)

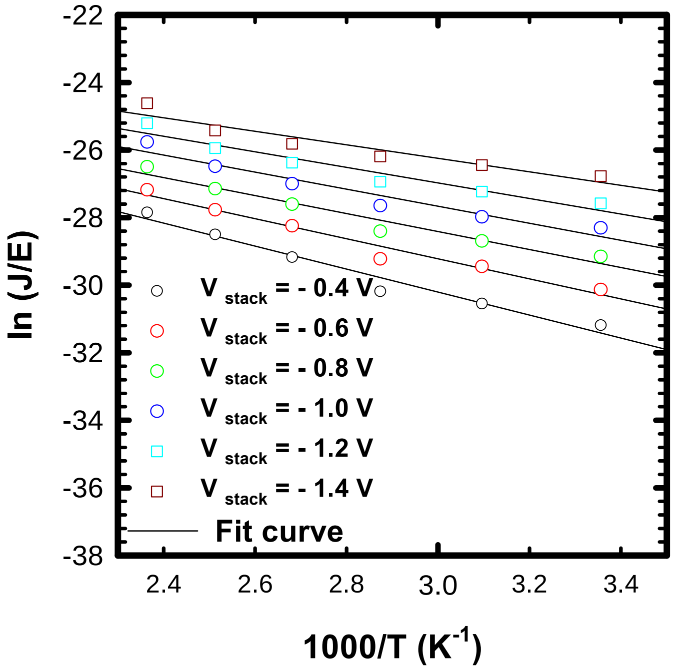
Fig. 3-16 (a) Flat band voltage versus stress time under positive constant voltage stress, and (b) Flat band voltage shift versus stress time under dynamic stressing with stress and passivation duration both 1000 sec.



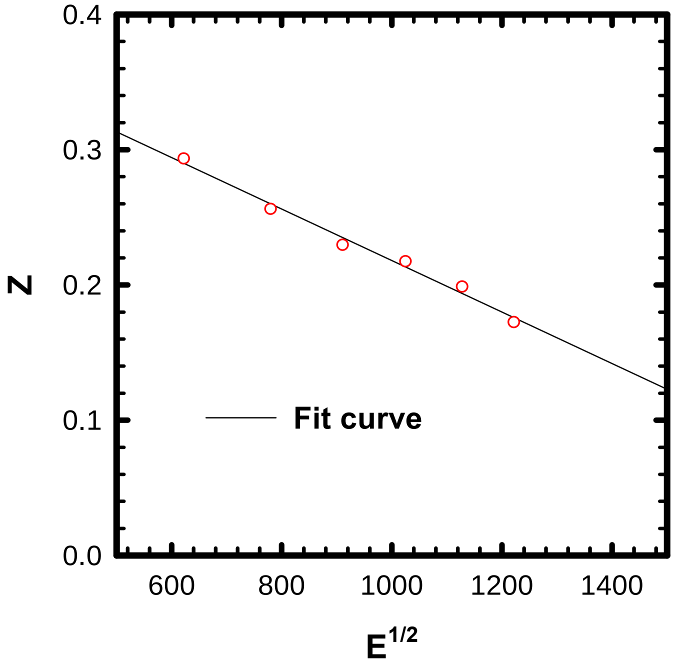
(a)

(b)

Fig. 3-17 (a) The J-V curves measurement under various temperatures from 25℃ to 150℃ before stress and (b) is after -4.0V 600s stress.



(a)



(b)

Fig. 3-18 (a) ln (J/E) v.s. 1000/T under different HfO_2/ SiO_x stack voltage, and the symbols are experiment data and the solid line are fit curve. (b) Z v.s. $E^{1/2}$, Z is the slopes of the curves of (a) and solid curve is fitting line.

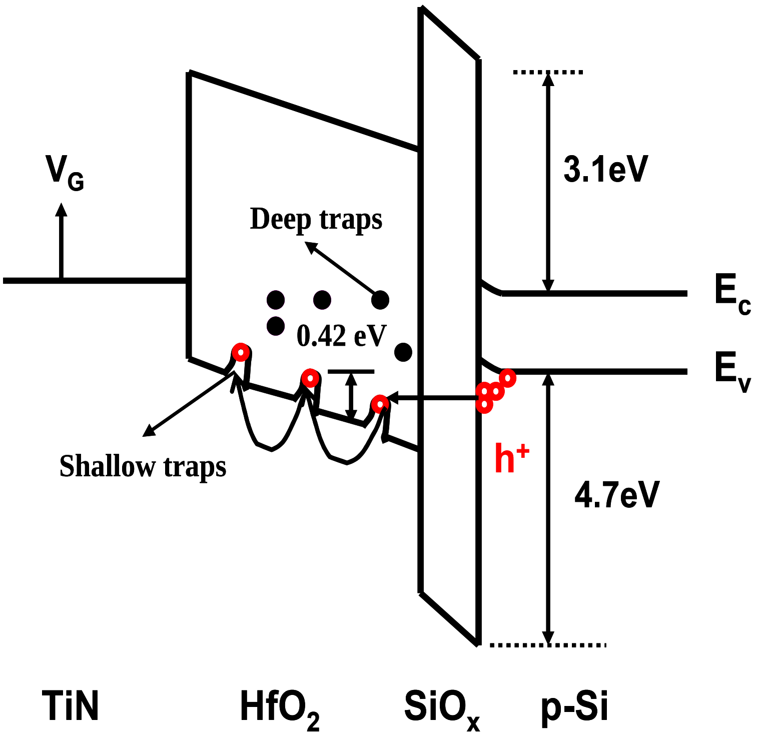


Fig. 3-19 Energy band diagram of HfO$_2$/SiO$_x$ stack to illustrate the conduction mechanism of Frankel-Poole emission.

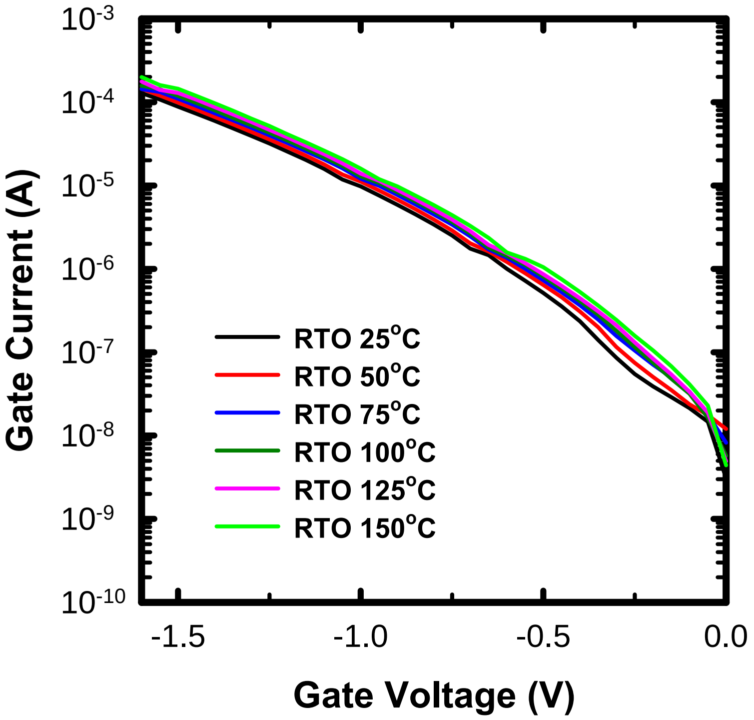


Fig. 3-20 The I-V curves measurement under various temperatures from 25℃ to 150℃ after -4.0V 2300s stress.

Chapter 4

Conclusions and Suggestions for Future Work

4-1 Conclusions

In the first part of this thesis, the effects of surface pre-deposition treatments on the prosperities of HfO_2 thin films were investigated. Several important phenomena were observed and summarized follows.

Firstly, oxygen in HfO_2 easily reacts with Si substrate if hafnium oxide is directly deposited on silicon, and during subsequent thermal processing HfO_2 film easily becomes crystalline. To alleviate this problem, we used a high density N_2O or NH_3 plasma to form a thin nitrided interfacial film. Plasma pre-treatment alone without post-nitridation annealing can decrease leakage current by about three orders of magnitude, however, the resultant leakage current still does not satisfy stringent ULSI demands. Post-nitridation annealing is therefore needed to further reduce the leakage current. The post-nitridation annealing, however, also results in EOT increase, especially at higher annealing temperature. The use of spike N_2 RTA to anneal nitrided film, however, results in degraded leakage current.

Secondly, proper sweeping range for C-V measurement is important for evaluating a new material's quality. Other elements that affect our results must be excluded in these measurement. In this thesis, (+1.5V, -1V) is found to be proper for the investigation of frequency dispersion and hysteresis. Our results on reliability show that NH_3 pre-treatment is better than N_2O pre-deposition in terms of time-to-breakdown, charges to breakdown and characteristics lifetime.

Thirdly, hole trappings are observed in the HfO_2/SiO_2 gate stack with TiN metal gate electrode. The flatband voltage shift (ΔV_{fb}) caused by the trapped holes can be well described by adopting distributed capture cross section model over several decades of stress time during CVS. This phenomenon is attributed to the resultant asymmetric band structure, which favors hole tunneling from the substrate and, in turn, makes the gate stack more susceptible to the hole trapping.

Finally, we proposed that latent traps exist in the bulk of HfO_2 virgin films. These latent traps were classified into deep and shallow traps that can be activated by stress. The trapped holes result in an effectively smaller barrier height for Frenkel-Poole emission so the leakage current become less dependent on temperature.

4-2 Suggestions for Future Work

The major potential showstoppers for high-k gate dielectrics are considered to be (a) interfacial layer thickness and quality, (b) film morphology after the entire thermal process, (c) mobility degradation, and (d) reliability issues. Mobility is the first concern for device performance. Interfacial layer thickness and quality are related to mobility degradation and scaling limit. The interfacial layer thus represents a stumbling block and remains a tough challenge for high-k dielectrics. For the potential use of MOCVD system for high k material deposition, the precursor plays a dominant role in determining the thickness and quality of interfacial layer. More efforts on the synthesis of new precursor and the optimization of deposition condition and post deposition processes to reduce interfacial layer thickness and to improve interface quality are necessary.

From HRTEM images, HfO_2 film is crystalline after high temperature annealing. Without an interfacial layer under the high-k film, the leakage current must be intolerably high. Therefore, raising the crystallization temperature thus represents an urgent and important task. Adding nitrogen is generally used to increase thin film crystallization temperature. How to effectively incorporate nitrogen into HfO_2 film is currently being actively investigated.

For electrical properties, C-V and I-V characteristics were studied in this thesis, however, a complete reliability study has not been carried out, and should be actively pursued. In this thesis, only LOCOS capacitor structure was fabricated. Many important issues such as channel carrier mobility can not be studied using this simple test structure. To fabricate MOSFET structure is necessary to perform complete evaluation of the HfO_2 films.

In this study, hole trappings are found to be dominant in HfO_2 film due to the use of mid-gap metal gate in our experiment. The use of different metal gates may results in different trapping mechanisms. This is also an interesting topic for research but the process stability between the chosen metal and HfO_2 film must be taken into consideration.

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