國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

高介電常數材料氧化鋁在矽基板上之介面特性研究

The Interface Investigation of High-K Material Al_2O_3 on Si Substrate

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中 華 民 國 九 十 三 年 六 月

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摘 要

根據半導體的微縮定律，隨著半導體製造逐漸的微小化，極薄的二氧化矽介電層將伴隨著極大的直接穿遂漏電流，而這個直接穿遂漏電流將對元件的功率消耗有嚴重的影響。在閘極二氧化矽介電層薄到10 奈米以下的情況之下，為了解決這嚴重的直接穿遂漏電流現象，我們將利用高介電係數材料來替換傳統的二氧化矽。我們利用高介電係數材料在相同的等效二氧化矽厚度之下，能擁有較大的實際物理厚度以抵擋直接穿遂漏電流。

在眾多高介電係數材料之中，氧化鋁是一種非常有潛力的高介電係數材料。它有較高的介電係數（約 8～10），足夠高的載子能障（對

電子約 2.9 電子伏特，對電洞約 4.3 電子伏特)，以及與矽有著良好的熱穩定性。在論文中，我們研究氧化鋁經由 NH_3 表面處理與在氧氣與氮氣環境下進行沈積後退火（ＰＤＡ）在物性，電性，及可靠度分析。沈積後退火（ＰＤＡ）可以有效的降低表面粗糙度。我們發現 NH_3 表面處理與沈積後退火（ＰＤＡ）都能改善試片在電容-電壓電性分析上的平台現象，其中氨氣表面處理更可以降低試片的漏電流。

有先經過NH_3 表面處理與在氮氣環境下進行沈積後退火（ＰＤＡ）的話，其介電質的可靠度將會變得較佳。在氧化鋁薄膜內的漏電傳導機制是由Schottky發射所主導的。綜上所述，氧化鋁介電層的特性在 NH_3 表面處理配合後續沈積後退火處理後得到了有效的改善。這種新穎的NH_3 表面處理與沈積後退火提供了未來奈米元件應用在金氧半沈積處理上一個極佳的選擇。

The Interface Investigation of High-K Material Al_2O_3 on Si Substrate

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Abstract

According to the scalling rules, aggressive scaling has led to silicon dioxide (SiO_2) gate dielectrics as ultra thin in state-of-the-art CMOS technologies. As a consequence, static leakage power due to direct tunneling through the gate oxide has been increasing at an exponential rate. As technology roadmaps call for sub-10Å gate oxides within the next five years, a variety of alternative high-*k* materials are being investigated as possible replacements for SiO_2. The higher dielectric constants in these materials allow the use of physically thicker films, potentially reducing the tunneling current while maintaining the gate capacitance needed for scaled device operation.

Aluminum oxide (Al_2O_3) is one of the potential high-*k* materials. It has the higher dielectric constant (8~10), higher barrier height (2.9eV for electrons , and 4.3eV for holes), and excellent thermal stability. In the thesis, physical, electrical and reliability characteristics of Al_2O_3 film with NH_3 surface treatment and Post Deposition Annealing (PDA) in the O_2 and N_2 ambient were studied. The PDA can effectively reduce surface roughness. The PDA and NH_3 surface treatments both can improve the C-V curves. Moreover, the lower leakage current is observed in NH_3 surface treatment samples.

The reliabilities can be improved by the NH_3 surface treatment after PDA in a N_2 ambient. The conduction mechanism in the Al_2O_3 thin film is dominated by the Schottky emission. To sum up, the characteristics of Al_2O_3 gate dielectrics with NH_3 surface treatment and subsequent PDA treatment described above are effectively improved. This novel NH_3 and PDA treatment provides an alternative for post metal-oxide deposition treatment in nanoscale device application.

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Chapter 1

Introduction

1.1 General Background

Silicon technology has been the basic of microelectronic and electronics systems for more than thirty years. The density of devices on silicon chip has been following the “Moore’s law”, doubling about every two or three years since about 1980.The density improvement combines not only the progress in lithography but also the innovation in device fabrication technology. Therefore , a steady path of constantly shrinking device dimensions , increasing speed , increasing chip size ,and decreasing cost has been found from the Si integrate circuit (I C) industry.

Over the years , there have been several major evolutions in silicon digital logic technology. CMOS technology has become the most popular digital logic technology for all IC industry, owing to its low standby power dissipation and scaling properties. Oxide thickness scaling has long been recognized as one of major keys for devices scaling. High drive current and thereby improved device performance can be achieved by reducing oxide thickness. Figure 1.1 shows the expected equivalent oxide thickness (EOT) trends from the published 2003-ITRS roadmap.[1] It suggests that at the current rate of progress , we will need EOT of less than 2 nm by 2004 and after 2006 oxy-nitride can’t meet the limit on

gate leakage current density. Such thin gate oxide can not suffer much from extrinsic factors such as defect density, surface roughness and uniformity control. Moreover, the physical limitation of oxide thickness is caused by the quantum mechanical tunneling of carriers. Besides, the direct tunneling current increases exponentially by about one order of magnitude for every 0.2 ~ 0.3nm reduction in oxide thickness. This additional leakage current not only causes increased power dissipation but also may affect the circuit functionality due to the decreased operation margins. For this reason , some of the effective replacement materials for silicon dioxide that are currently being investigated to replace silicon dioxide include Al_2O_3 , HfO_2,ZrO_2,Ta_2O_5,TiO_2 .Table 1.1 illustrates basic properties of current high-k material.[2] The alternative high-k material should be thermodynamically stable on Si upon high temperature anneals (needed for dopant activation for polysilicon gates).Unstable dielectric materials will form interfacial layers, which are between the high-k dielectrics and silicon substrate. The high-k film and it's interfacial films would affect various device parameters like effective oxide thickness(EOT),flatband voltage(Vfb),gate leakage current, and channel mobility ,and thus significantly affect the transistor behavior. Some of the metal oxides like Ta_2O_5,TiO_2,and BST are known to degrade when annealed at temperature as low as 600℃and have poor electrical properties for MOS devices.[3] The newer high-k materials including Al_2O_3, HfO_2, ZrO_2 have generated a lot of interest primarily due to their potential thermal stability in the presence of Si based on thermodynamic considerations.[4][5]

1.2 Motivation

The purpose of CMOS scaling is to enhance the performance of circuit and increase the packing density in a chip. However, when scaling down, thinning gate dielectrics inevitably accompany with larger direct tunneling current. The more recent high-*k* approach is to increase the physical thickness to reduce the direct tunneling current, yet at the same time obtain higher values of gate capacitance by using a dielectric material with a higher dielectric constant (high-κ) relative to SiO_2[6]

$$\frac{k_{ox}}{t_{ox}} = \frac{k_{high-k}}{t_{high-k}} \qquad \textbf{[eq-1]}$$

Electrical result on various candidates such as Al_2O_3 and HfO_2 have shown the leakage reduction by order of magnitude, but have encountered the integration challenges such as charge trapping-related threshold voltage instability and mobility degradation.

Many high-k materials have emerged as the most promising gate dielectric candidates for sub 100nm technology due to its superior thermal stability, longer tunneling distance than SiO_2 at the same EOT and large band gap with a favorable Band alignment .However, the formation of interfacial layer between Al_2O_3 and SiO_2 is still an important issue. Fortunately, as reported, we find adding a nitride layer between oxide/silicon substrate interface can improve reliability.[7][8]

1.3 Characterization of Al_2O_3

Recently, Al_2O_3 has gained much attention as promising insulator. The reasons are briefly listed as follows.

(1) Suitable high dielectric constant：

The reported dielectric constant κ of Al_2O_3 is about 8 ~10. This magnitude of κ-value is higher than that of SiO2(κ~4) and Si_3N_4 (κ~7). It is not high enough to induce severe FIBL effect.[9]

(2) Wide bandgap：

In general, as the dielectric constant increases, the bandgap decreases. The narrower bandgap would increase leakage current. The energy band gap of Al_2O_3 is about 8.3 eV, which is higher than the other high-κ materials such as ZrO_2, HfO_2 , Ta_2O_5.[10][11]

(3) Acceptable band alignment：

Band alignment determines the barrier height for electron and hole tunneling from gate or Si substrate. For SiO_2, the band offset of conduction band and valence band is ~9eV, and the barrier height for electrons is 3.5eV and the barrier height for holes is 4.4eV. The high band offset for both electron and hole has the benefit of low leakage current. Figure 1-2 shows the calculated band offsets for most high-k dielectrics.[3] For Al_2O_3, barrier height for electron and hole is 2.9ev and 4.3eV, respectively. This band alignment is acceptable and better than other high-k materials such as Ta_2O_5 and HfO_2

(4) High free energy of reaction with Si：

For Al_2O_3, the free energy of reaction with Si is about 64.4 Kal/mole (see Table 1-2).which is higher than that of TiO_2 and Ta_2O_5[3]. Therefore, Al_2O_3 is a more stable material on Si substrate as compared to ZrO_2,and HfO_2. [12]-[14]

(5) High heat of formation:

Al_2O_3 has higher heat of formation (399 kcal/mole). That means that Al is easy to be oxidized to form Al_2O_3 and the oxide of Al is usually stable on Si substrate.

According to these profits above discussions, we choose Al_2O_3 as the major high-k material and in our investigation. The measurement is performed by MIS capacitor structures.

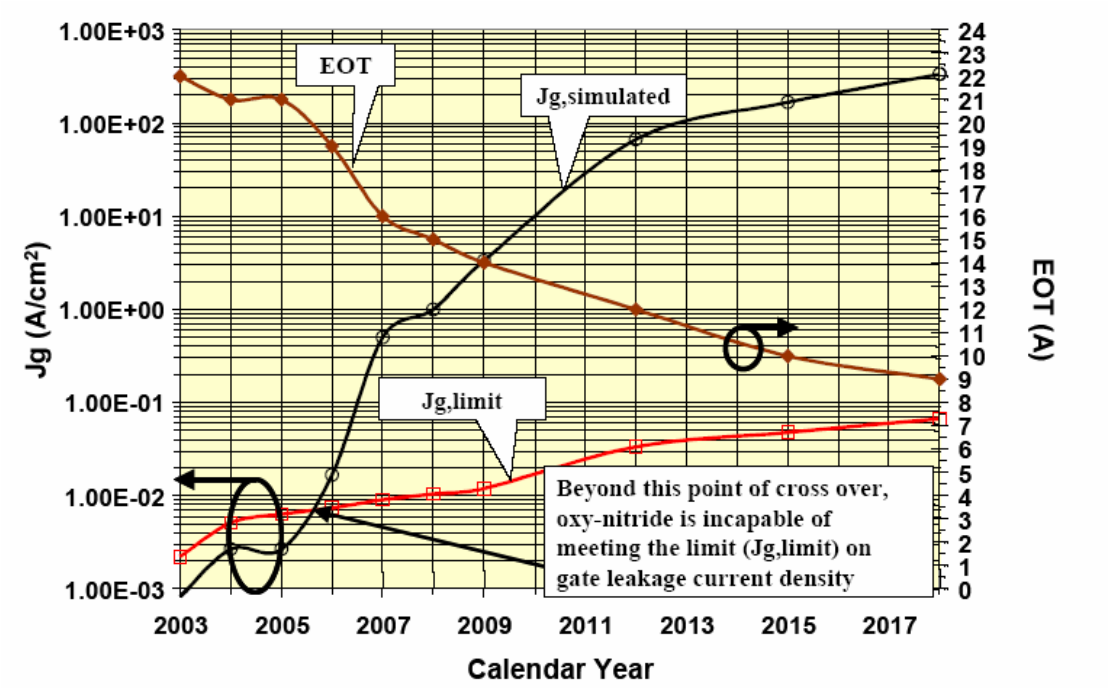


Fig 1.1 the expected equivalent oxide thickness (EOT) trends from the published 2003- ITRS roadmap

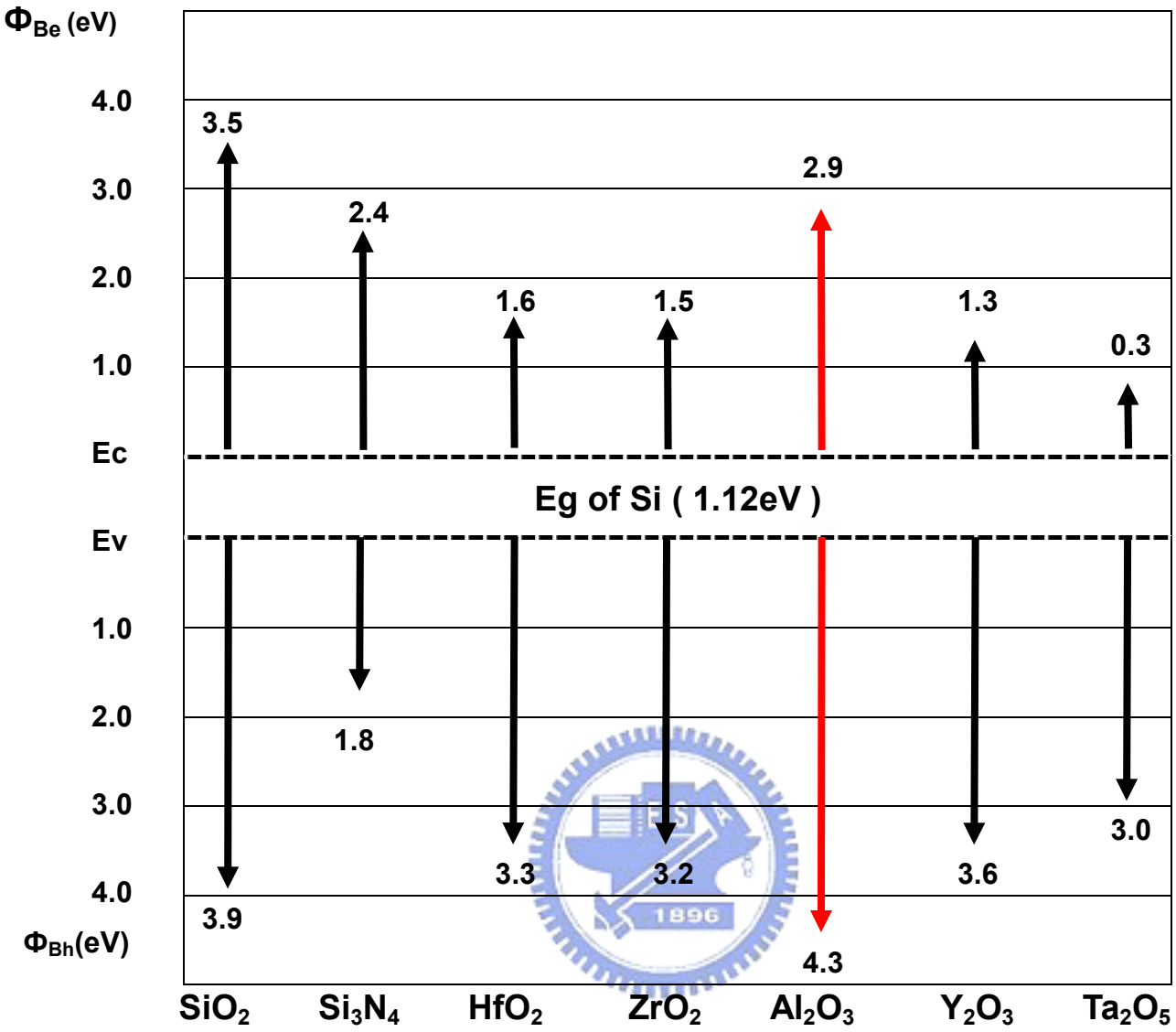


Fig 1-2 Band alignment of topical high-k dielectrics

Material	Dielectric Constsnt(k)	Band gap Eg(eV)	△Ec(eV) to Si	Crystal Structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8	Amorphous
Ta_2O_5	26	4.5	1-1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.
HfO_2	25	5.7	1.5	Mono.,Tetrag.,Cubic
ZrO_2	25	7.8	1.4	Mono.,Tetrag.,Cubic

Table 1.1 Basic properties of current high-k candidates[2]

Aspect	Property		
	Al_2O_3	ZrO_2	HfO_2
Bandgap (eV)	8.3	5.82	6.02
Barrier Height to Si (eV)	2.9	1.5	1.6
Dielectric Constant	8-11.5	~25	~30
Dielectric Strength (MV/cm)	>1.0		2-4.5
Heat of Formation (Kcal/mol)	399	261.9	271
ΔG for Reduction (Kcal/mol) ($MO_x + Si \rightarrow M + SiO_x$)	64.39	42.326	47.648
Thermal expansion coefficient ($10^{-6}K^{-1}$)	6.7	7.01	5.3
Lattice Constant (Å) (5.43 Å for Si)	4.7-5.2	5.1	5.11
Self Diffusion Coefficient @ 900℃	1.5048×10^{-7}	6.0009×10^{-10}	2.8227×10^{-17}

Table 1-2 Material properties of Al_2O_3, ZrO_2 ,HfO_2[3]

Chapter 2

Basic Characteristics of Al_2O_3 Gate Dielectrics Using Rapid Thermal Annealing Technology

2.1 Introduction

Recently, MOSFETs with high-k gate dielectrics such as Al_2O_3, ZrO_2, and HfO_2 have been studied intensively. However, investigation of these materials shows that oxygen or dopant penetration through dielectrics is a significant problem due to the low crystallization temperature.[15] In addition, in crystallized gate dielectric films, grain boundaries may act as high oxygen or dopant diffusivity paths, causing device failure with high leakage. For this reason, the high-k materials are expected to have higher crystalline temperature. Among these materials, Al_2O_3 is a promising candidate because of its compatibility with the poly-silicon gate process and relatively superior scalability. In additional, Al_2O_3 offers the possibility of pushing the CMOS technology to 10nm feature sizes. As the dielectric constant of Al_2O_3 is higher than SiO_2, it will provide a significant increase in capacitance without scaling down the oxide thickness. Rapid thermal Annealing (RTA) is a short time processing technique that can contribute to reduce the thermal budget, low levels of surface roughness, and improve film qualities[16]. It is also very important that RTA is capable of meeting the process integration and manufacturing needs in the currently used CMOS fabrication sequence.

2.2 Experiment

The 6-inch P-type Si(100) wafers are after the RCA clean. The high-k material Al_2O_3 was then deposited by reactive sputtering in Ar/O ambient. After Al_2O_3 deposition, a high temperature post deposition annealing is performed at 750℃、850℃、and 950℃ respectively for 30 sec by RTA Rapid Thermal Annealing (RTA). In our experiment, the gate electrode formations were used the Physical Vapor Deposition (PVD) systems. We deposit the TiN film (2000Å) as the top gate electrode and the thermal evaporation system to deposit the Al film(5000Å) as the backside contact. The cross-sectional view and total experimental procedures of the structure were shown in Fig2-1.At last the Capacitance-Voltage (C-V) and Current-Voltage(I-V) characteristics were measured by HP-4284 and HP-4156C systems. The capacitance equivalent thickness (CET) were extracted from C-V curve.

2.3 Results and discussion

2.3-1 Capacitance-Voltage characteristic

After the Al_2O_3 deposition, the following processes may go through many high temperature treatments during the VLSI fabrication. Such high-temperature treatments are likely to change the morphology and properties of thin films. Fig 2- 2 2-3 shows the high frequency(100kHz) capacitance-voltage(C-V) ,and Figure 2-4 shows the CET of Al_2O_3 samples (without surface treatment) after various post

deposition annealing (PDA) temperature at 750℃, 850℃, 950℃ in the O_2 or N_2 ambient. The capacitance of Al_2O_3 samples annealing in an O_2 ambient decreases with the increasing annealing temperature.[17] Therefore, the CET increases after annealing in an O_2 ambient. This is because an O_2 penetration will induce the increasing of the interfacial layer at Al_2O_3/Si-substrate and higher annealing temperature increasing will speed up interface layer growth rate.[18] The exact composition of such interfacial layer is still not known, it is believed its dielectric constant is much lower than Al_2O_3. On the contrary, the capacitance of Al_2O_3 samples annealing in a N_2 ambient is increasing when annealing temperature increases. Therefore, the CET decreases after annealing in a N_2 ambient. The void-defects generated after the sputtered Al_2O_3 formation and it could be densified followed a RTA process in a N_2 ambient.[19]. A hump is clearly observed in the depletion region of the C-V curve for the 750℃ annealing sample. This hump is speculated due to the poor interface quality, and it can be eliminated after a high temperature annealing.

2.3-2 Current density-Electric field characteristic

The current density (J) in the J-E curve was defined by J = I / A, where A is the area of capacitor. The CET determined by the C-V measurement. Fig. 2-5 shows the J-E characteristics of Al_2O_3 film with RTA process in an O_2 ambient. It shows that the thicker Al_2O_3 film will resist large leakage current, and the lower leakage current was observed.[20] However, the thicker dielectric thickness will reduce capacitance and the driving current. Fig 2-6 shows the J-V characteristics of the fabricated Al_2O_3 film with RTA in a N_2 ambient. The capacitor can have a lower leakage current with

thinner CET. This is due to RTA process in a N_2 ambient can improve Al_2O_3 film by eliminating void-defect [21][22]. Fig 2-7 shows J versus PDA temperature in the O_2 and N_2 ambient. Obviously, higher PDA temperature can reduce leakage for both annealing ambient. Consequentially, the sputtered Al_2O_3 film can be improved after a N_2 RTA process.

2.3-3 Time Dependent Dielectric Breakdown

If the leakage current density in the oxide (J_{ox}) is kept constant during the stress test (implying that the applied current is held constant), the stress time to breakdown becomes the variable. The length of stress time t_{BD} elapsed until dielectric breakdown occurred. The time-to-breakdown behavior of a group of oxide samples under such test conditions is referred to as time-dependent dielectric breakdown (TDDB). Gate oxide failure is reported to be a limiting factor for scaling of oxide thickness, since time-to-breakdown decreases with rising gate current .The weibull plot of charge to breakdown for Al_2O_3 samples with various PDA temperature in an O_2 ambient is shown in Fig 2-8. Obviously, distribution of the samples with thinner CET is better than others. However, the level of the charge to breakdown is lower than we expect. Fig 2-9 shows the weibull plot of charge to breakdown for Al_2O_3 samples with various PDA temperature in a N_2 ambient. For various PDA temperature, their distribution and charge to breakdown are almost the same and they are not dependent on Al_2O_3 thickness. This means that the interfacial layer determines the breakdown of the whole stack.[23]

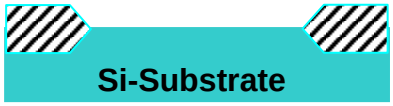
2.3-4 Surface morphology

Surface morphology of Al_2O_3 films which were deposited and followed by different post annealing conditions were shown in AFM analysis. The thickness of the Al_2O_3 films was about 15nm. According to the published literature[24], smooth surface is desired since roughness will enhance local electric field, which is believed to be detrimental to the gate dielectric integrity. Fig.2-10(a), (b), and (c) show the AFM images of Al_2O_3 films as deposited with as-deposition , 900 ℃ PDA in an O_2 ambient, and 900 ℃ PDA in a N_2 ambient, respectively. The corresponded root-mean-square roughness (R_{ms}) values were 0.823 nm, 0.593 nm, and 0.560 nm. The as deposited Al_2O_3 film show larger roughness. After a PDA process, the roughness of Al_2O_3 film was improved. Fig.2-11 and Fig 2-12 show the leakage current density at -1V and the R_{ms} values of these samples. It was observed that the surface roughness increases when the PDA temperature increases.

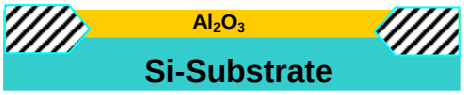
2.4 Summary

In this chapter, characteristics of the sputtering Al_2O_3 films with PDA at temperature ranging at 750℃ to 950℃ for 30 sec are shown, respectively. Higher PDA temperature can effectively reduce leakage current. For the samples with PDA in an O_2 ambient, it will induce extra interface growth to increase CET.[25][26] In a N_2 ambient, the phenomenon won't find. We believe additional RTA in a N_2 ambient technique could suppress the interface growth and improve the gate dielectrics

reliability. The dielectric is shown to be a potential candidate for next generation high-k gate dielectric applications.

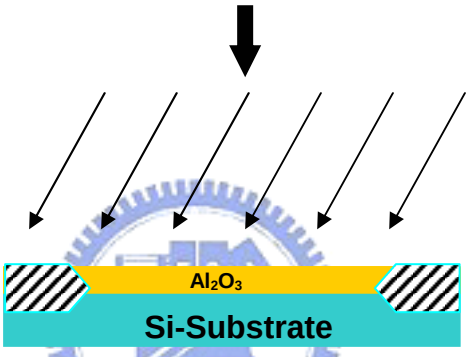


1. RCA clean and LOCOS



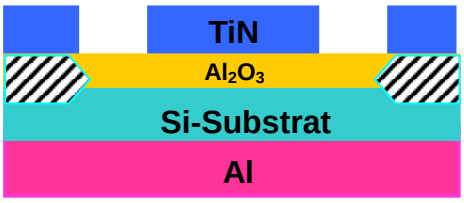
2. Al_2O_3 deposition (60Å)

by Reactive Sputter



3. RTA treatment N_2/ 5 slm/30 sec or

O_2/ 5 slm/30 sec 750℃ , 850℃ ,950℃



4. Top electrode formation TiN-2000 Å &

Backside contact formation Al -5000Å

Fig.2-1 Process flows of experimental samples

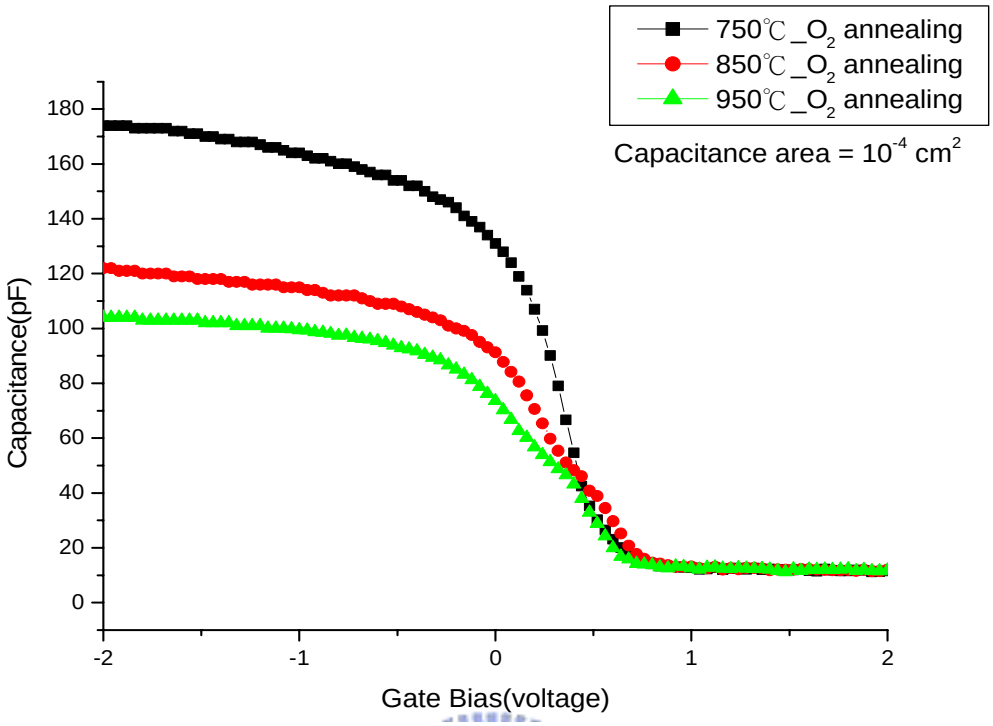


Fig.2-2 The C-V curves of Al_2O_3 samples annealing in an O_2 ambient

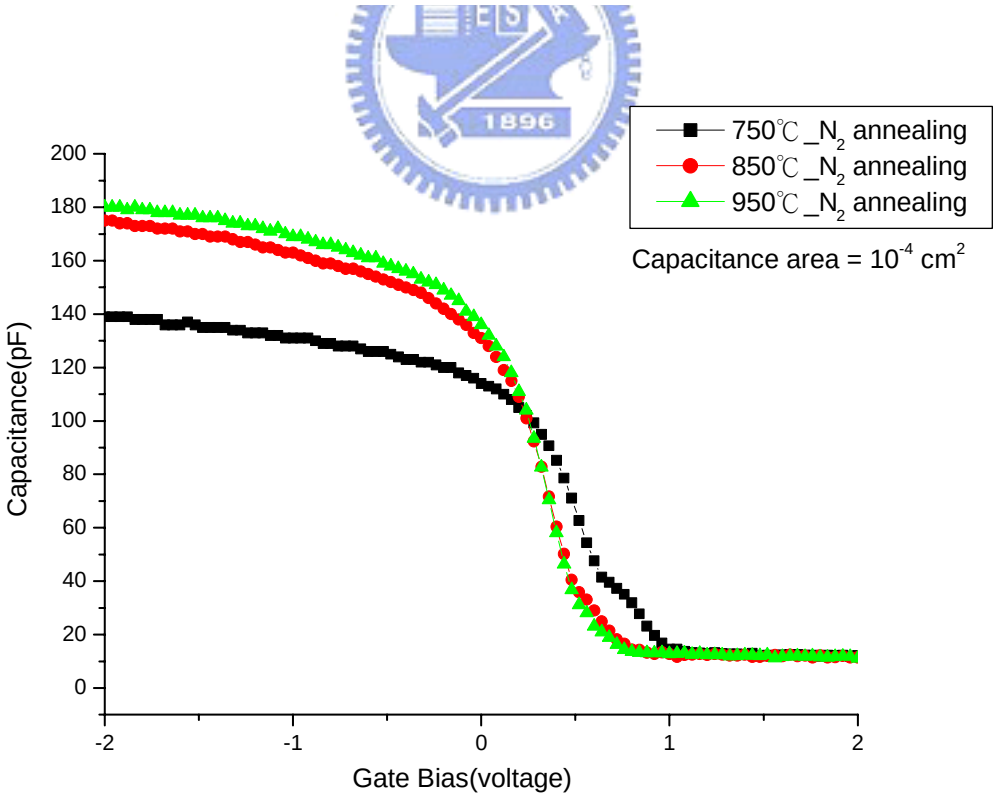


Fig.2-3 The C-V curves of Al_2O_3 samples annealing in a N_2 ambient

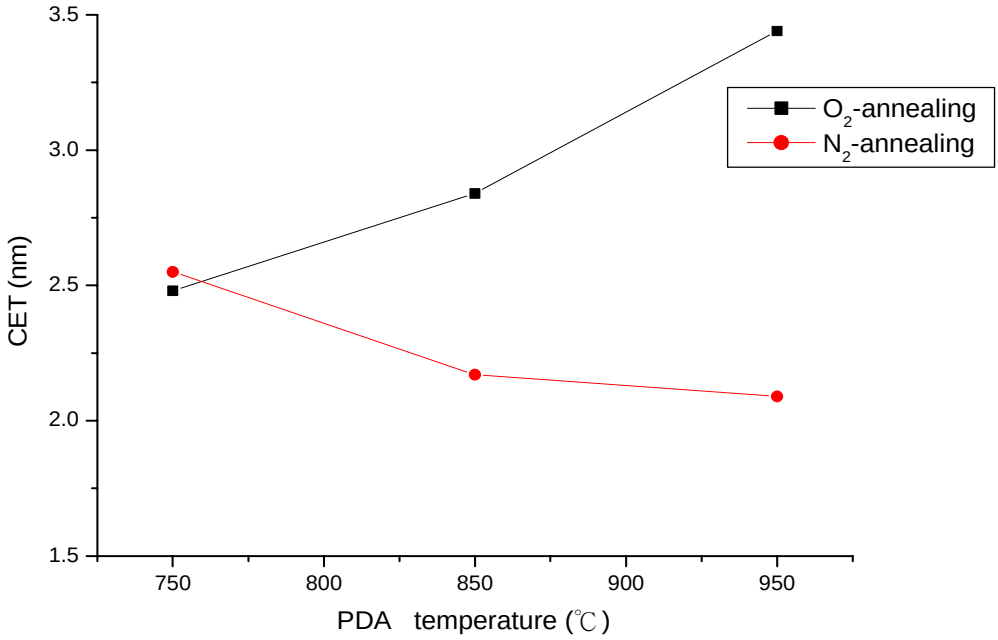


Fig.2-4 The CET of Al_2O_3 samples after various post annealing temperature 750℃, 850℃, 950℃

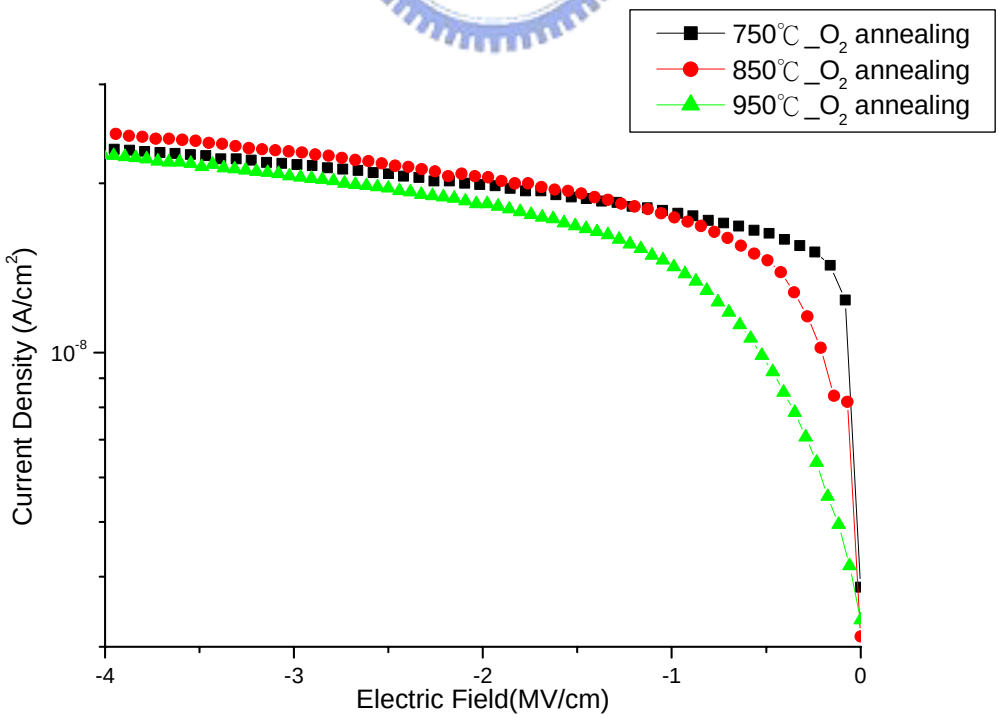


Fig.2-5 The J-E curves of Al_2O_3 samples with various PDA temperature in an O_2 ambient.

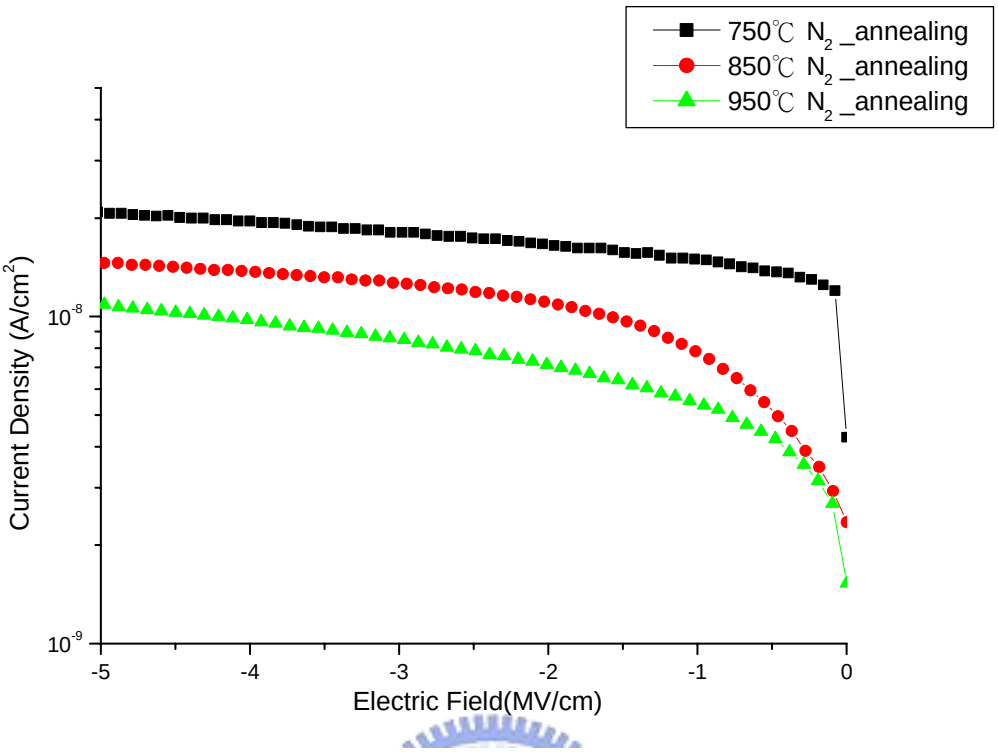


Fig.2-6 The J-E curves of Al_2O_3 samples with various PDA temperature in a N_2 ambient.

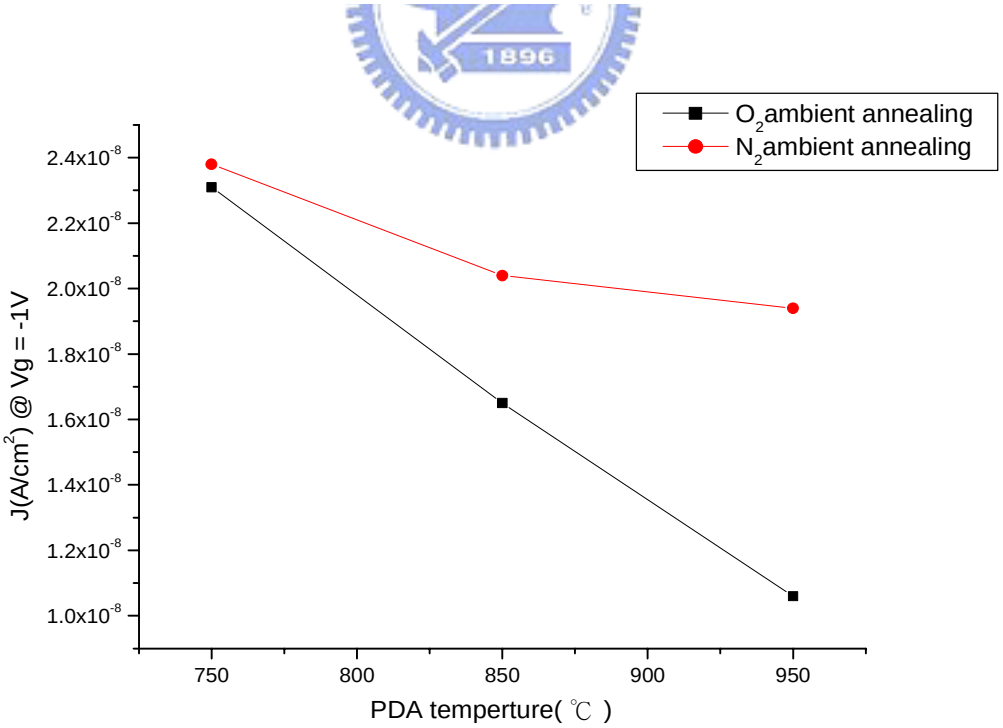


Fig.2- 7 The J at Vg= -1 V of Al_2O_3 samples with various PDA temperature

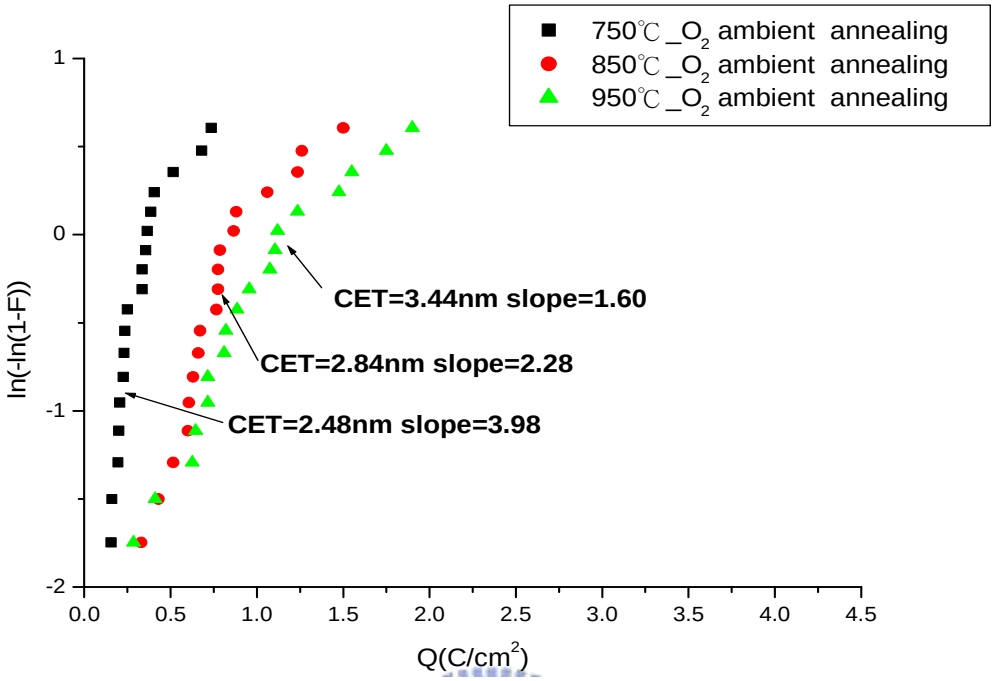


Fig.2- 8 The Weibull plot versus the charge to breakdown Q (C/cm^2) of Al_2O_3 samples with various PDA temperature in an O_2 ambient.

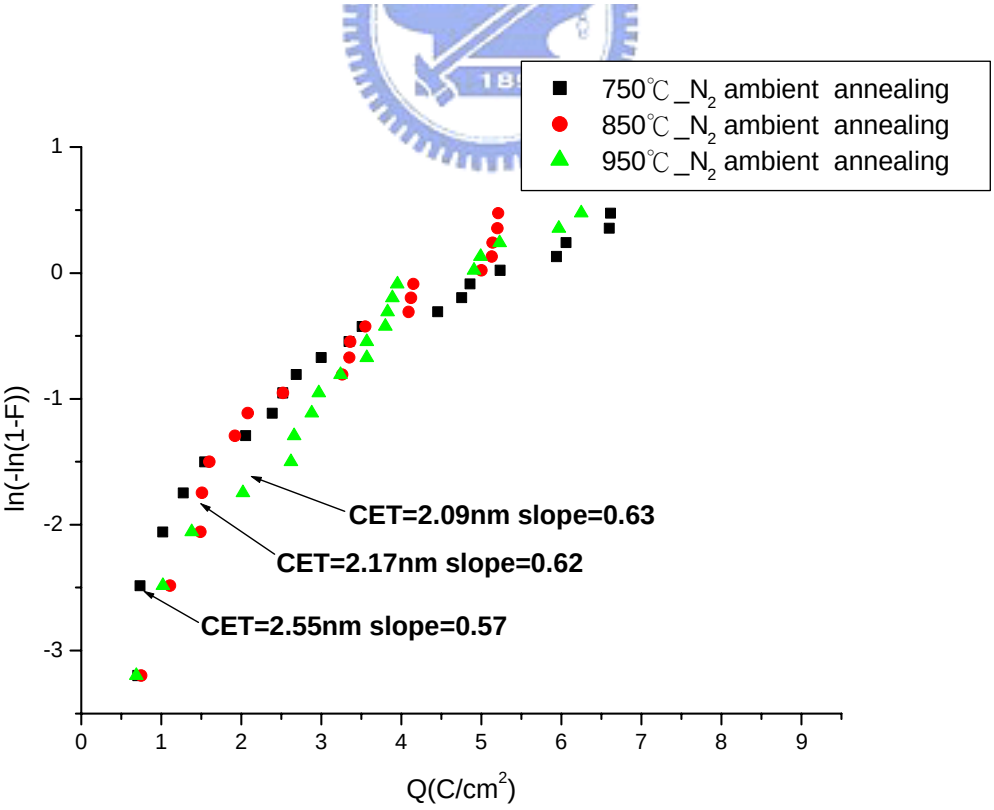


Fig.2- 9 The Weibull plot shows the charge to breakdown Q (C/cm^2) of Al_2O_3 samples with various PDA temperature in a N_2 ambient.

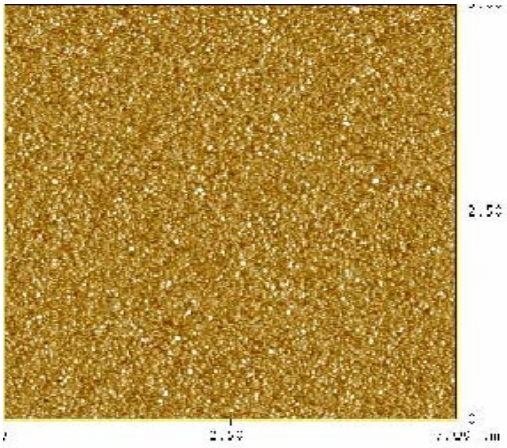


Image Statistics

Img. Z range	11.187 nm
Img. Mean	-0.000000 nm
Img. Raw mean	485.03 nm
Img. Rms (Rq)	0.823 nm
Img. Ra	0.628 nm

(a) As deposition

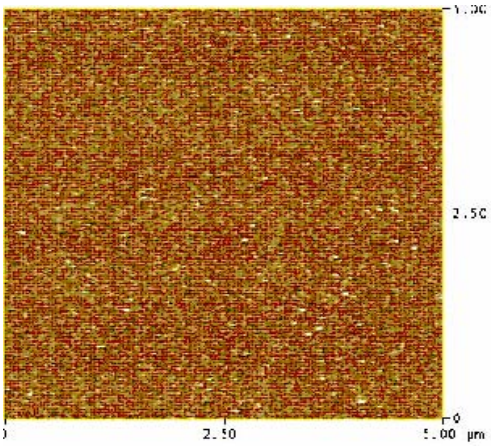


Image Statistics

Img. Z range	8.053 nm
Img. Mean	-0.000000 nm
Img. Raw mean	533.79 nm
Img. Rms (Rq)	0.593 nm
Img. Ra	0.454 nm

(b) O_2-800℃

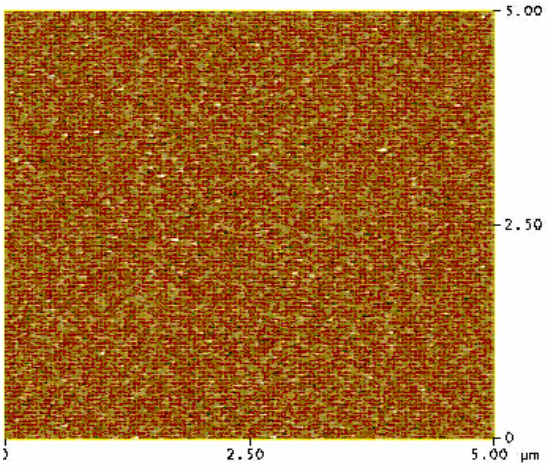


Image Statistics

Img. Z range	6.460 nm
Img. Mean	-0.000000 nm
Img. Raw mean	233.10 nm
Img. Rms (Rq)	0.560 nm
Img. Ra	0.437 nm

(c) N_2-800℃

Fig.2-10 AFM images of Al_2O_3 with various PDA: (a) As deposition, (b) O_2-900℃, and (c)N_2-900℃

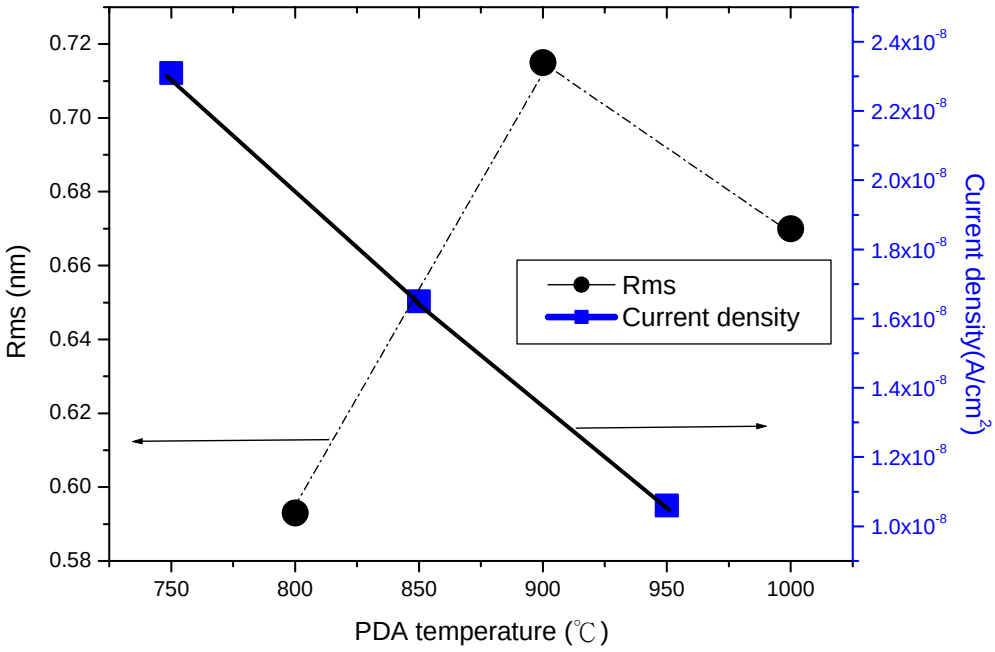


Fig.2-11 Leakage current density,R_{ms} values versus PDA temperature in an O_2 ambient

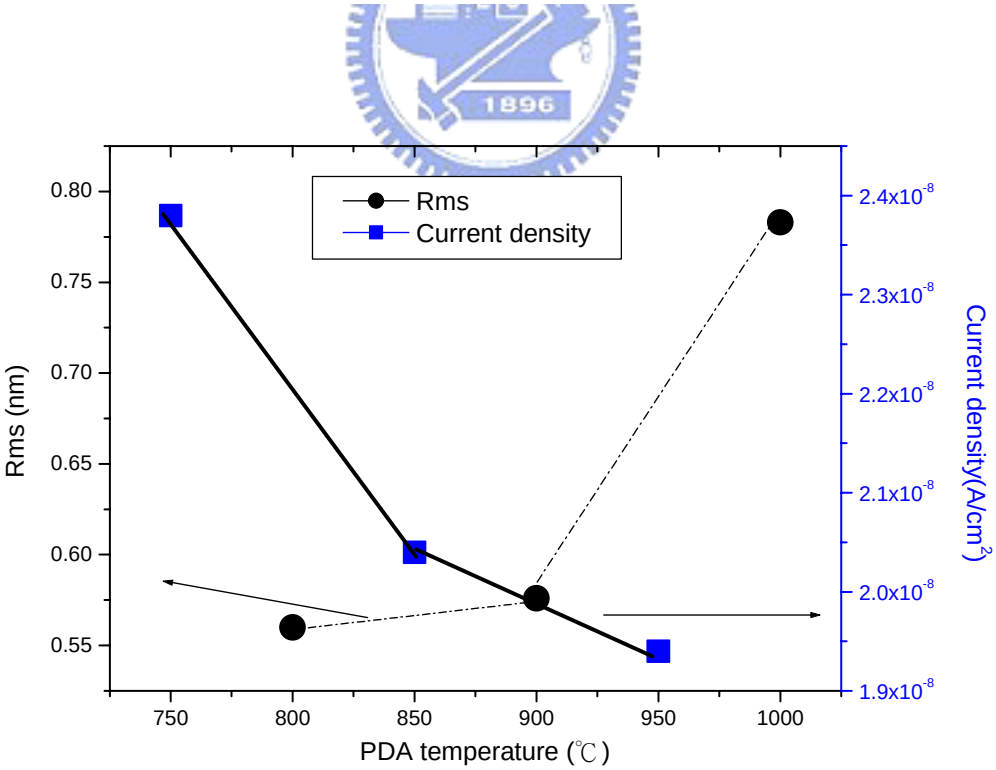


Fig.2-12 Leakage current density, CET and R_{ms} values versus PDA temperature in a N_2 ambient

Chapter 3

Characteristics of Al_2O_3 Gate Dielectrics Using NH_3 Surface Nitridation Technology

3.1 Introduction

As many reports, the direct contact of high-k materials and Si-substrate will be imperfect and have many issues. The dominance of the Si MOSFET over competing technologies has largely been attributed to the high quality of thermally grown SiO_2 and the resulting Si/ SiO_2 interface.[27] The Si/SiO_2 interface is known to have a very low density of interface states (D_{it}~$2x10^{10}$ states/cm^2) arising from unsaturated surface bonds and other electrically active imperfections.[27] Interface states lead to degradation of on-current, since carrier mobility is limited by scattering at the interface due to the strong vertical electric fields present in the channel. For maintaining the excellent transport properties at the Si interface, a possible method to suppress the interfacial layer thickness is to passivate the Si surface before Al_2O_3 deposition. Generally, there are many methods to passivate the Si surface such as surface nitridation, nitrogen-contained ambient annealing, or nitride deposition as the bottom layer. Nitridation of the Si surface using NH_3 treatment before the deposition of high-k materials has been shown to be effective in achieving the low EOT and preventing the boron penetration [28][29] However, this technique results in higher interface charges [30] which leads to higher hysteresis and

reduced channel mobility. In this chapter, we studied the effect of suppressing interfacial layer growth by NH_3 surface treatments. The NH_3 treatment would nitridize the Si surface to form a silicon nitride layer. [31]-[33] Silicon nitride is a superior barrier for H_2O and oxygen, and it can suppress oxygen to diffuse into Si substrate.[34] After the NH_3 treatment, a thin silicon nitride (SiN_x) layer (~10Å) was deposited and measured by optical measurement system (Ellipsometer). As reports, Nitridation of the Si surface is prior to the deposition of high-k gate dielectrics and it shows the result to achieve the low EOT and increase reliability by making the interface smoother.[35] In this study, the effect of post thermal annealing was studied in the O_2 and N_2 ambient, respectively.

3.2 Experiment

First, the 6-inch P-type Si(100) wafers were cleaned with standand RCA clean. The samples were divided into two groups. One was without any surface treatment before Al_2O_3 deposition, and the other was with a NH_3 surface treatment before Al_2O_3 deposition. The NH_3-treatment is performed in high temperature furnace, 800℃ for 1 hour. After NH_3-treatment, a SiN_X layer(~10 Å) was deposited. Al_2O_3 dielectric was then deposited various thickness (30Å, 40Å, and 50Å) by reactive sputtering in the Ar/O (ratio = 24/1) ambient. After Al_2O_3 deposition, a high temperature post deposition annealing was performed at 900℃ in the O_2 or N_2 ambient. Finally, the gate electrode formation was performed by the Physical Vapor Deposition (PVD) systems. We deposited the TiN film (2000Å) as the top gate electrode and the thermal evaporation system to deposit the

Al film (5000Å) as the backside contact. The cross-sectional view and total process flow were shown in Fig 3-1. The Capacitance-Voltage (C-V) and Current-Voltage (I-V) characteristics were measured by HP-4284 and HP-4156C systems, respectively. The capacitance equivalent thickness (CET) were extracted from C-V curve. In order to study the conduction mechanism in the Al_2O_3 film. The current-voltage characteristics with various temperature were measured at room temperature (RT), 50℃ , 75℃ , 100℃ , 125℃ , respectively.

3.3 Results and discussion

3.3-1 Capacitance-Voltage characteristic

Figure 3-2 shows the comparisons of the C-V curves of the samples with and without surface treatment after PDA 900℃ in an O_2 ambient. Both sample shows less hysteresis and hump phenomenon. It is clear that samples with a NH_3 treatment had higher capacitance at strong accumulation than samples without a NH_3 treatment. The CET of Al_2O_3 film is effectively reduced after NH_3 nitridation since NH_3 surface can suppress the growth of interfacial layer.[36] In Fig 3-2, we can also found the C-V curves shift negatively after NH_3 nitridation can be observed due to the nitridation-induced fixed positive charges[37]. Since positive fixed charges in conventional NH_3 nitridation film is due to N–H bonds at the interface [38]-[40]. Fig 3-3 shows the comparisons of the C-V curves of the samples with or without surface treatment after PDA 900℃ in a N_2 ambient. We still can find that the CET of Al_2O_3 film is effectively reduced after NH_3 treatment.

However, the amount of the C-V curves shift negatively after NH_3 nitridation is decreasing. The reason is due to that PDA in a N_2 ambient will enhance the magnitude of fixed charge in Al_2O_3 film Fig 3-4 shows the variation of deposited thickness (measured by ellipsometer) versus CET after PDA 900℃ in an O_2 ambient. the NH_3 treatment can effectively reduce the CET despite the initial oxide thickness, which shows the excellent CET scalibility of this nitridation process. Because presence of Si_3N_4 layer can effectively suppress the diffusion of oxygen species into the high-k/Si substrate interface[41]. Without surface nitridation, Al and O atoms are easier to react with Si and are likely to form additional silicon dioxide and/or aluminum silicate layer with relatively lower k value.[42] As the result, the NH_3 nitridation treatment can effectively suppress the interface growth to lower the CET and increases the effective dielectric constant. [43] Fig 3-5 shows the variation of Al_2O_3 thickness versus capacitance equivalent thickness (CET) after PDA 900℃ in a N_2 ambient. We can see almost the same result in an O_2 ambient as in a N_2 ambient, except in a N_2 ambient with higher k value. So the PDA in a N_2 ambient exhibits superior behavior than PDA in an O_2 ambient.

3.3-2 Current density-Electric field characteristic

Figure 3-6 (a) and (b) show the relationship of gate leakage current versus gate bias after PDA 900℃ in the O_2 and N_2 ambient, respectively. The NH_3 –treatment samples show lower leakage current even with thinner CET. It is postulated that the NH_3-treatment can improve the quality of interface between high-k and silicon substrate and effectively

reduce the leakage current.[44] Fig. 3-7 shows the curve of Current density versus CET curves at Vg = -1V with NH_3 treatment and without NH_3 treatment. It is clear that NH_3 treatment can effectively reduce leakage current. According to the bonding strength comparisons as follow, Si-O(8.42eV) > Si-N(4.75eV) > Si-Si(3.38eV) > Si-H(3.18eV) The Si-N bonds have larger bonding strength than the Si-Si bonds or Si-H bonds. Therefore, we preferred to use the stronger Si-N bonds to replace Si-H bonds, subsequently resist the oxygen diffusion and reduce defect-generation.[45] We also suspect that surface nitridation may effectively reduce the concentration of oxygen vacancies during PDA due to its capability to suppress oxygen diffusion.[42] Therefore, the leakage current will be reduced large. However, as the requirement of the gate dielectric thickness shrinks to below 2nm, the excessive direct tunneling current dominates the gate leakage characteristics and limits scalability of the conventional SiO_2 gate dielectrics. As the result, NH_3 treatment process become potentially to reduce the gate leakage current to meet the request for deep sub-micron CMOS applications.

3.3-3 Time Dependent Dielectric Breakdown

In this study, the dielectric reliability was also investigated with the behavior of time dependent dielectric breakdown (TDDB). The gate dielectric failure occurred when the significant gate leakage was observed. The magnitude of charge to breakdown (Q_{BD}) can be calculated in TDDB measure. Fig 3-8(a) and (b) show the weibull plots of the charge to breakdown (Q_{BD}) of Al_2O_3 samples with nearly the same CET after PDA 900℃ in

theO_2 and N_2 ambient , respectively. The samples with NH_3 treatment shows more charge to breakdown (Q_{BD}). Thus, we suspect that surface nitridation may effectively reduce the concentration of oxygen vacancies during PDA due to its capability to suppress oxygen diffusion.[42] On the other hand, the stronger Si-N bonds bring a stronger interface layer.[35] When part of voltage drop across the Si_3N_4 interfacial layer in samples, the voltage drop across the Al_2O_3 film is lower than expectance, and the influence of the electric field stress is not as severe as the un-NH_3 treatment Al_2O_3 samples. As the result, it will enhance the Q_{BD} for NH_3 treated Al_2O_3 samples. Besides, the slope of the Weibull distribution is an important factor in reliability calculations, where it is used for scaling to total oxide area on chip and low percentiles. A low Weibull slope results in a strong reduction of the Q_{BD}. A value of slope of 0.9~1.5 is very low for a gate dielectric layer. For thermally grown SiO_2 with a physical thickness of 9 nm, is expected slope = 12 for intrinsic breakdown.[46] Similarly low values below 2 (dotted line) are measured for the other ALCVD high-k layers grown at IMEC as well as for layers reported by other research groups, as citation in Fig.3-9. Breakdown is determined by sputter-induced defects causing weak spots in the Al_2O_3 film. The percolation model is not applicable and the slope values are always low.[47] The sputtered Al_2O_3 film seems to produce a lot of initial defects during a PVD process. Therefore, other deposition technology should be considered such as MOCVD and ALCVD..

3.3-4 Conduction Mechanism

It is important to study the conduction mechanisms of leakage current in Al_2O_3 film to

improve its electrical and dielectric properties. Comparing the conduction mechanism reported, the current transport mechanism in Al_2O_3 is still unclear and seems to be strongly process dependent.[48] There may be different conduction mechanisms in the insulator thin film. Typically, two possible effects are in the metal-insulator interface, one is Schottky effect ,the other is Frenkel-Poole effect. The Schottky-Richardson emission generated by the thermionic effect is caused by the electron transport across the potential energy barrier via field-assisted lowering at a metal-insulator interface. The leakage current equation is:

$$J = A^* T^2 \exp\left(\frac{\beta_s E^{1/2} - \phi_s}{k_B T}\right)$$

where $\beta_s = (e^3 / 4\pi\varepsilon_0\varepsilon)^{1/2}$,A^* effective Richardson constant,ϕ_s the contact potential barrier. We can find the slope of the leakage current equation.

$$\ln J = \frac{\beta_s}{k_B T}\sqrt{E} + \left[\ln(A^* T^2) - \frac{\phi_s}{k_B T}\right]$$

$$\text{slope} = \frac{\beta_s}{k_B T}$$

The Frenkel- Poole (F-P) emission is due to field-enhanced thermal excitation of trapped electrons in the insulator into the conduction band. The leakage current equation is:

$$J = J_0 \exp\left(\frac{\beta_{FP} E^{1/2} - \phi_{PF}}{k_B T}\right)$$

where $J_0 = \sigma_0 E$ is the low-field current density, σ_0 the low-field conductivity,

$\beta_{FP} = (e^3 / \pi\varepsilon_0\varepsilon)^{1/2}$,*e* the electronic charge,ε_0 the permittivity of free space,ε the high frequency relative dielectric constant, *T* absolute temperature ,*E* the applied electric filed, K_B the Boltzmann constant,ϕ_{PF} the contact potential barrier. We can find the slope of the leakage current equation.

$$\ln J = \frac{\beta_{FP}}{k_B T}\sqrt{E} + \left[\ln(J_0) - \frac{\phi_{PF}}{k_B T}\right]$$

$$\text{slope} = \frac{\beta_{FP}}{k_B T}$$

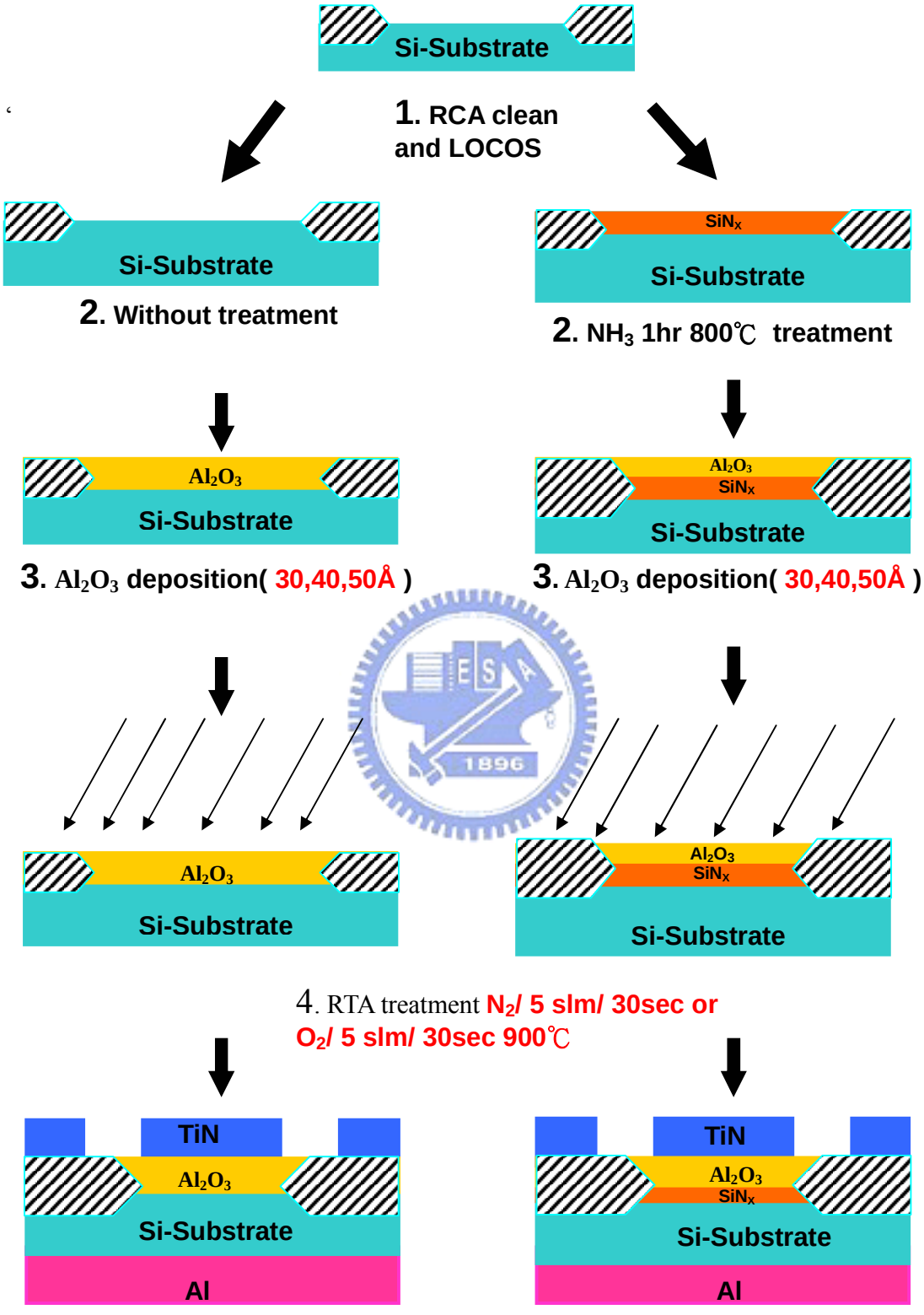
From the equations as shown above, leakage current behaviors of insulate films can be investigated further on the leakage current density (*J*)-electric field (*E*) characteristics such as ln *J* vs. $E^{1/2}$ plots. The plot of the nature log of leakage current density versus the square root of the applied electric field was observed. It is found that the leakage current density is linearly related to square root of the applied electric field. The linear variations of the current correspond either to Schottky emission or to Frenkel-Poole conduction mechanism. For trap states with coulomb potentials, the expression is virtually identical to that of the Schottky emission. The barrier height, however, is the depth of the trap potential well, and the quantity β_{FP} is larger than in the case of Schottky emission by a factor of 2. Distinction between the two processes can be done by comparing the theoretical value of β with the experimental one obtained by calculating the slope of the curve ln J-$E^{1/2}$. The dielectric constant of Al $_2O_3$ is 7.63 at PDA O_2 ambient and 8.29 at PDA N_2 ambient extracted by Fig 3-4 and-5, the theory β values are 4.40×10^{-23} for Frenkel-Poole and 2.20×10^{-23} for Schottky after PDA in an O_2 ambient and the theory β

values are 4.22×10^{-23} for Frenkel-Poole and 2.11×10^{-23} for Schottky after PDA in a N_2 ambient. Table 3-1 (a) and (b) shown the experimental β and Schottky barrier high of Al_2O_3 samples with NH_3 and without NH_3 treatment after PDA 900℃ in an O_2 ambient and after PDA 900℃ in a N_2 ambient ,respectively .Fig 3-10 (a) and (b) show the conduction mechanism fitting of Al_2O_3 samples with NH_3 and w/o NH_3 treatment after PDA 900℃ in an O_2 ambient and after PDA 900℃ in a N_2 ambient, respectively. We find the conduction mechanism in Al_2O_3 thin film is dominated by Schottky conduction. However, Schottky conduction depends strongly on the barrier between metal and insulator and has the inclination to occur for insulators with fewer defects and a more perfect metal-insulator interface.[49] Samples after NH_3 treatment will have higher barrier high and it is clear that the NH_3 treatment is very effective for improving the interface properties like the barrier height and Al_2O_3 film to reduce the leakage current.[50]

3.4 Summery

In this chapter, characteristics of the fabricated Al_2O_3 samples with NH_3 and without NH_3 treatment after PDA 900℃ in an O_2 ambient and at PDA 900℃ in a N_2 ambient are present, respectively. With surface NH_3 treatment, the CET of Al_2O_3 film can be reduced due to the suppression of interfacial layer growth. In samples with a NH_3 pre-treatment had lower leakage current and better dielectric reliability. Therefore, the NH_3 pre-treatment is a potential technique to improve the performance in high-k gate

dielectric applications.



5. Top electrode formation TiN -2000 Å pattern contact & Backside contact formation Al -5000Å contact

Fig.3-1 Process flows of experimental samples

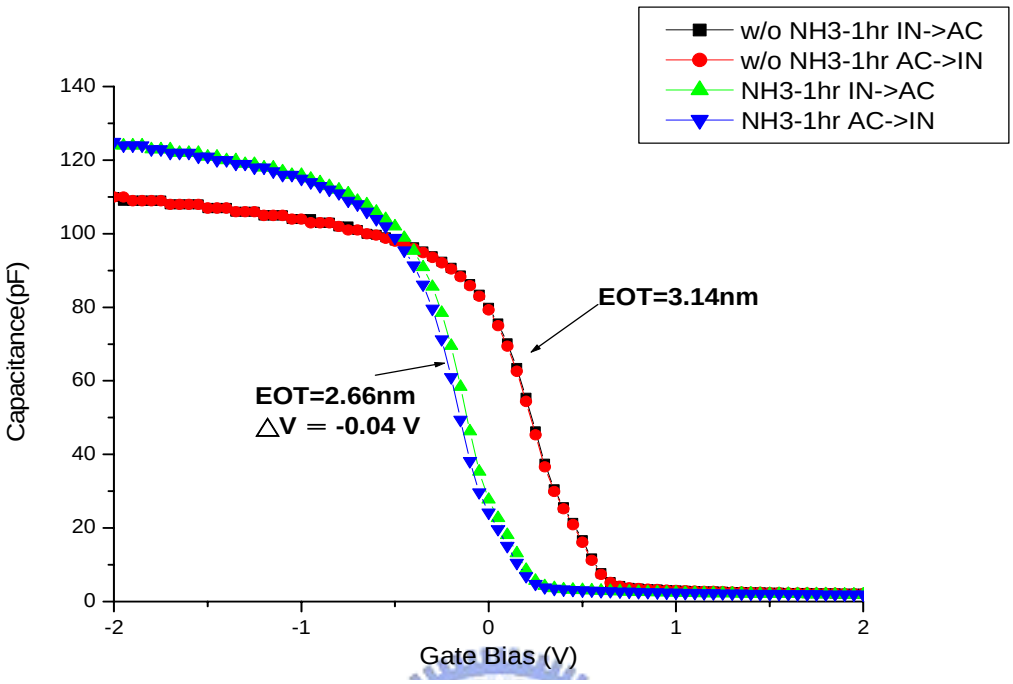


Fig. 3-2: C-V curve of Al_2O_3 sample with surface treatment compare to Al_2O_3 sample without surface treatment after PDA 900℃ in an O_2 ambient

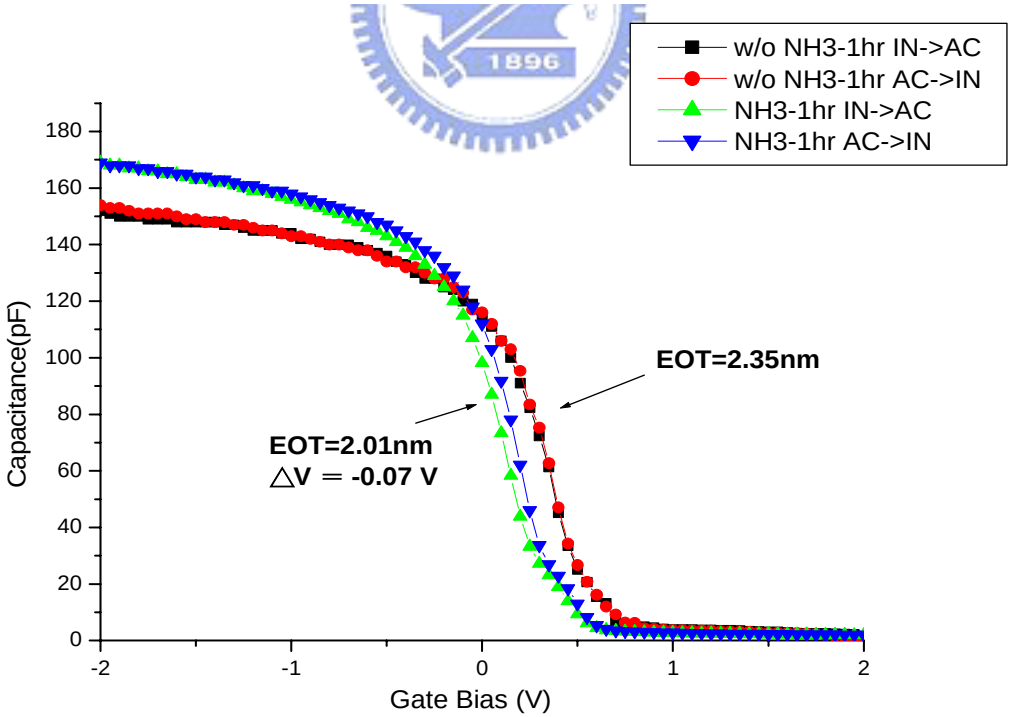


Fig. 3-3: C-V curve of Al_2O_3 sample with surface treatment compare to Al_2O_3 sample without surface treatment after PDA 900℃ in a N_2 ambient

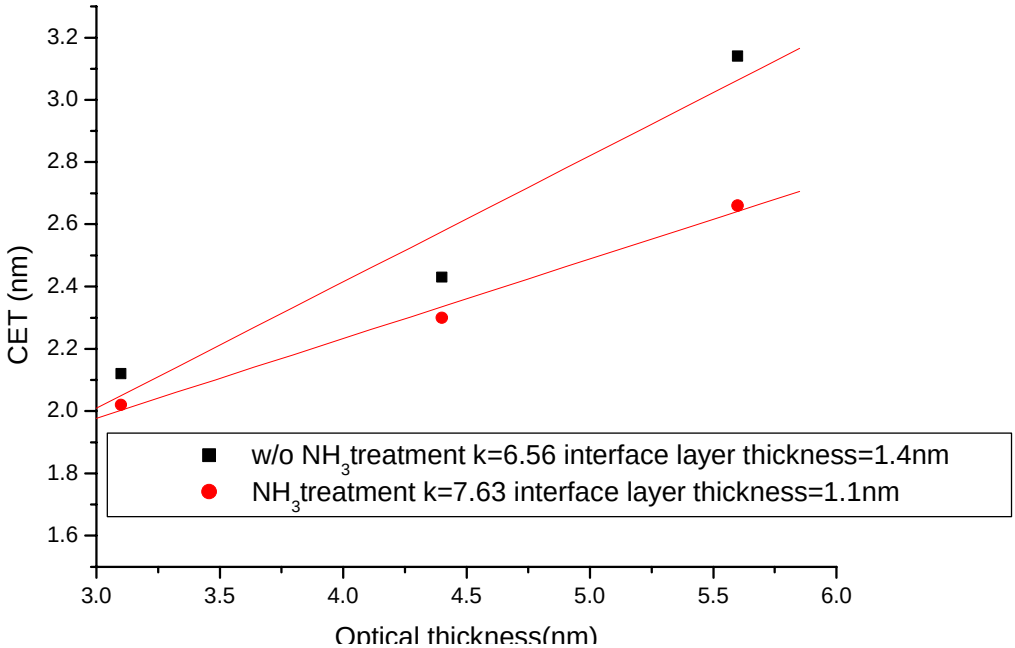


Fig. 3-4: CET versus Optical thickness of Al_2O_3 sample with surface treatment compare to Al_2O_3 sample without surface treatment after PDA 900℃ in an O_2 ambient

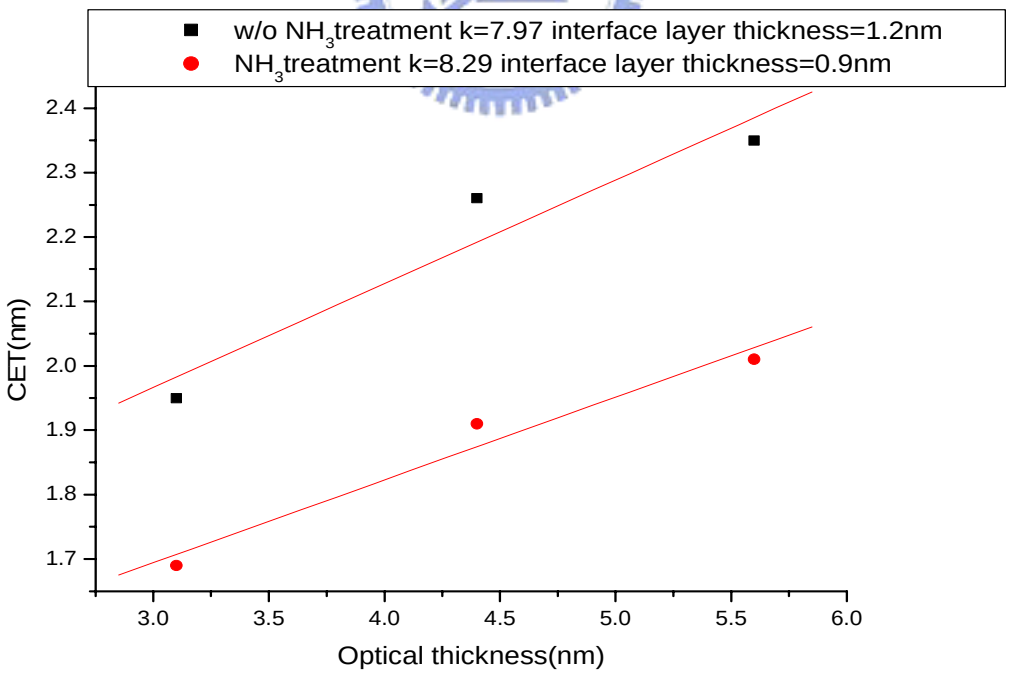


Fig. 3-5: CET versus Optical thickness of Al_2O_3 sample with surface treatment compare to Al_2O_3 sample without surface treatment after PDA 900℃ in a N_2 ambient

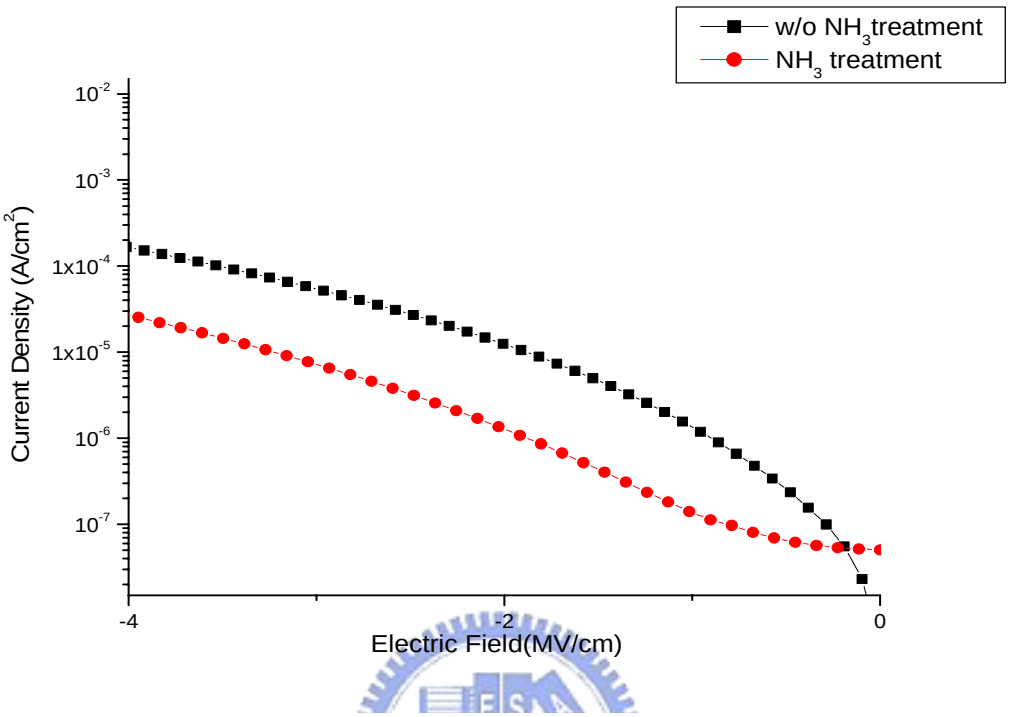


Fig. 3-6-(a): The gate leakage current density (J) versus electric field (E) curves for NH_3 nitrided and w/o NH_3 nitrided after PDA 900℃ in an O_2 ambient

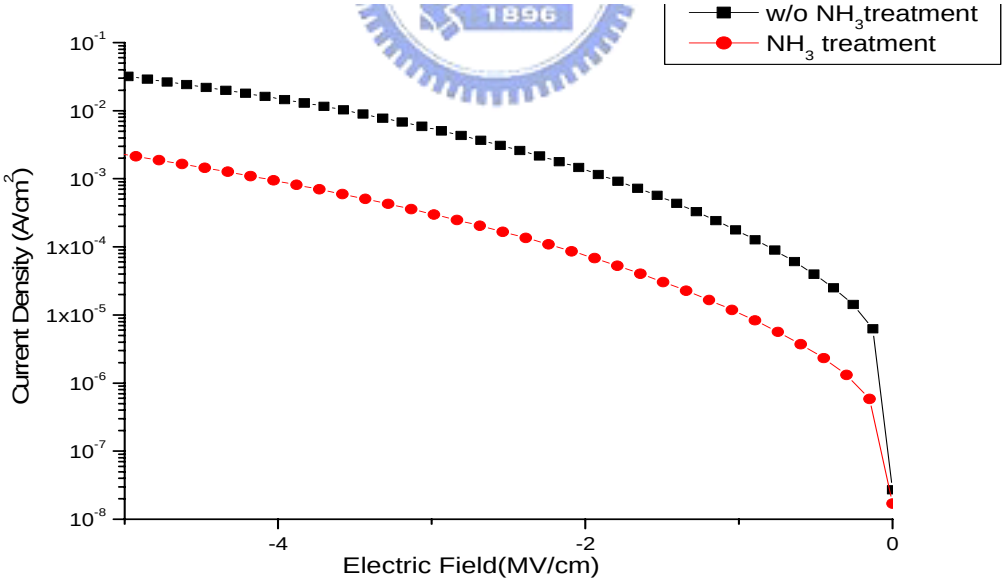


Fig. 3-6-(b): The gate leakage current density (J) versus electric field (E) curves for NH_3 nitrided and w/o NH_3 nitrided after PDA 900℃ in a N_2 ambient

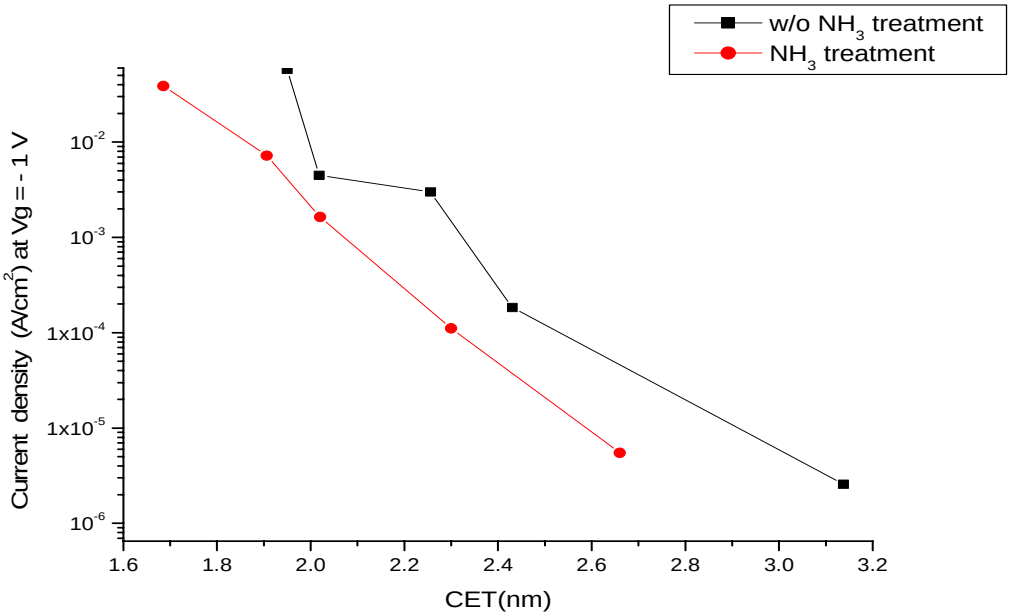


Fig. 3-7 Current density at Vg = -1Vversus CET curves for NH3 treatment and without NH3 treatment.

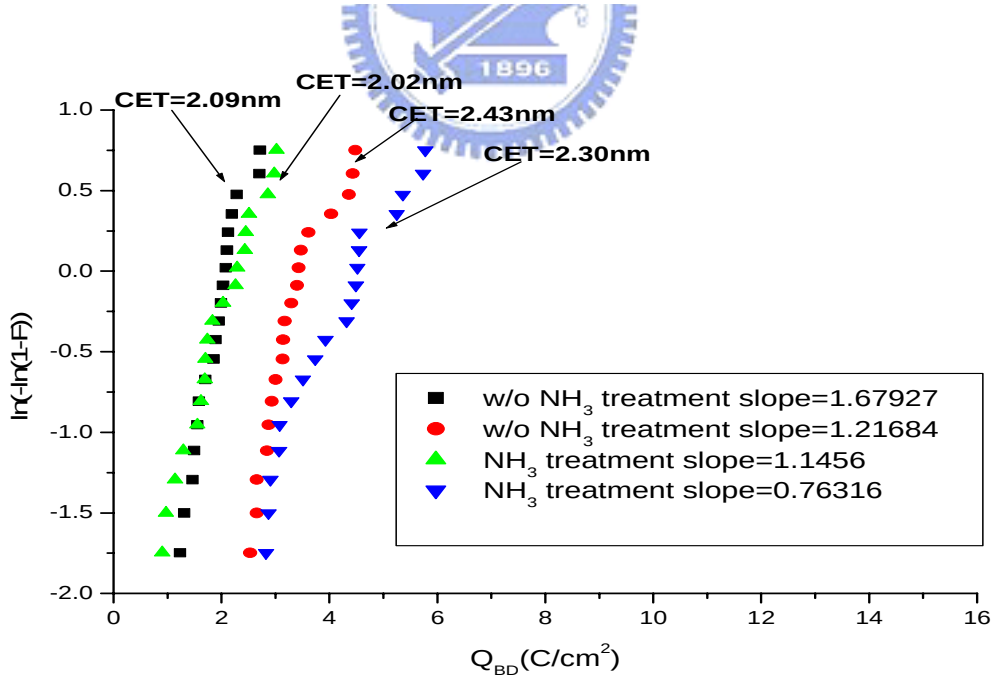


Fig. 3-8 –(a)The weibull plot shows charge to breakdown for Al_2O_3 samples with NH_3 and w/o NH_3 treatment at PDA after PDA 900℃ in an O_2 ambient

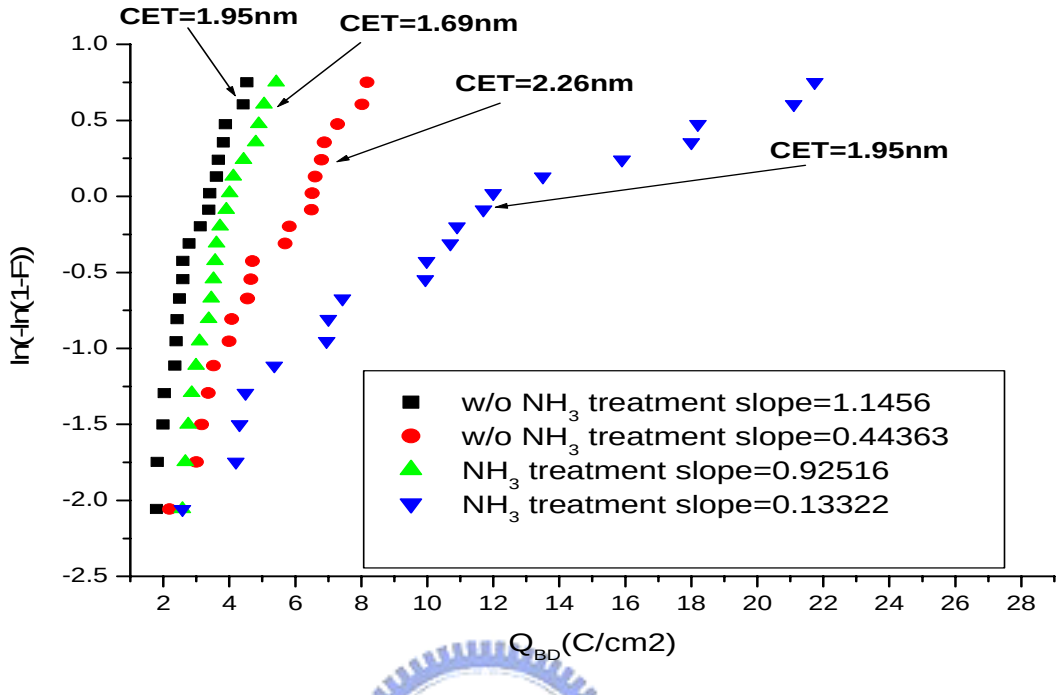


Fig. 3-8 –(b)The weibull plot shows charge to breakdown for Al_2O_3 samples with NH_3 and w/o NH_3 treatment at PDA after PDA 900℃ in a N_2 ambient

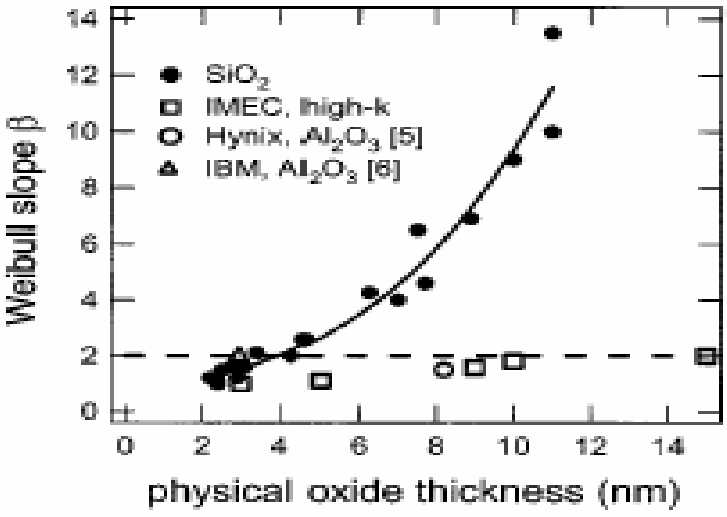


Fig. 3-9. Measured Weibull slopes are plotted versus the physical layer thickness, and a clear gap between the slopes for SiO_2 and the high-k layers can be observed.[20]

	w/o NH_3 treatment		With NH_3 treatment	
	βexp	Schottky barrier high	βexp	Schottky barrier high
25℃	$1.88*10^{-23}$	0.71ev	$2.25*10^{-23}$	0.97ev
50℃	$2.18*10^{-23}$	0.72 ev	$2.37*10^{-23}$	1.06ev
75℃	$2.48*10^{-23}$	0.70 ev	$2.49*10^{-23}$	1.13ev
100℃	$2.59*10^{-23}$	0.74 ev	$2.59*10^{-23}$	1.20ev
125℃	$2.71*10^{-23}$	0.70 ev	$2.71*10^{-23}$	1.28ev

Table.3-1(a) The experimental β and Schottky barrier high of Al_2O_3 samples with NH_3 and w/o NH_3 treatment after PDA 900℃ in a O_2 ambient

	w/o NH_3 treatment		With NH_3 treatment	
	βexp	Schottky barrier high	βexp	Schottky barrier high
25℃	$1.93*10^{-23}$	0.73 ev	$1.98*10^{-23}$	0.83ev
50℃	$1.83*10^{-23}$	0.65 ev	$2.15*10^{-23}$	0.89ev
75℃	$2.04*10^{-23}$	0.69 ev	$2.32*10^{-23}$	0.96ev
100℃	$2.13*10^{-23}$	0.72 ev	$2.45*10^{-23}$	1.03ev
125℃	$2.01*10^{-23}$	0.77 ev	$2.61*10^{-23}$	1.10ev

Table.3-1(a) The experimental β and Schottky barrier high of Al_2O_3 samples with NH_3 and w/o NH_3 treatment after PDA 900℃ in a N_2 ambient

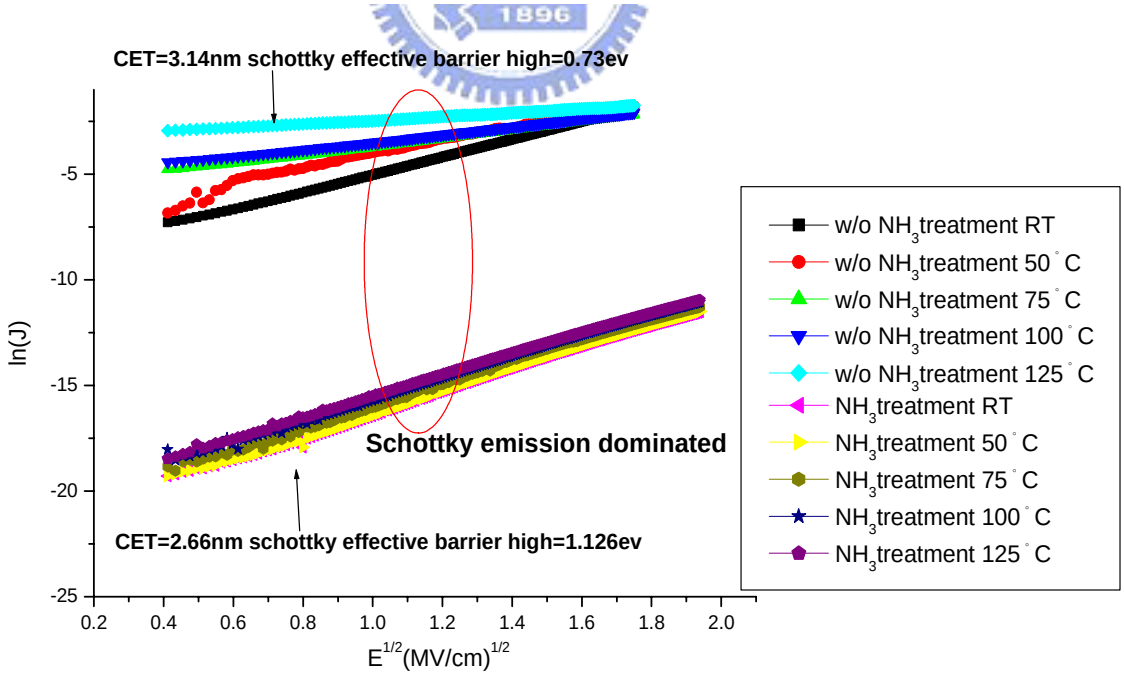


Fig.3-10(a) The conduction mechanism fitting of Al_2O_3 samples with NH_3 and w/o NH_3 treatment after PDA 900℃ in an O_2 ambient

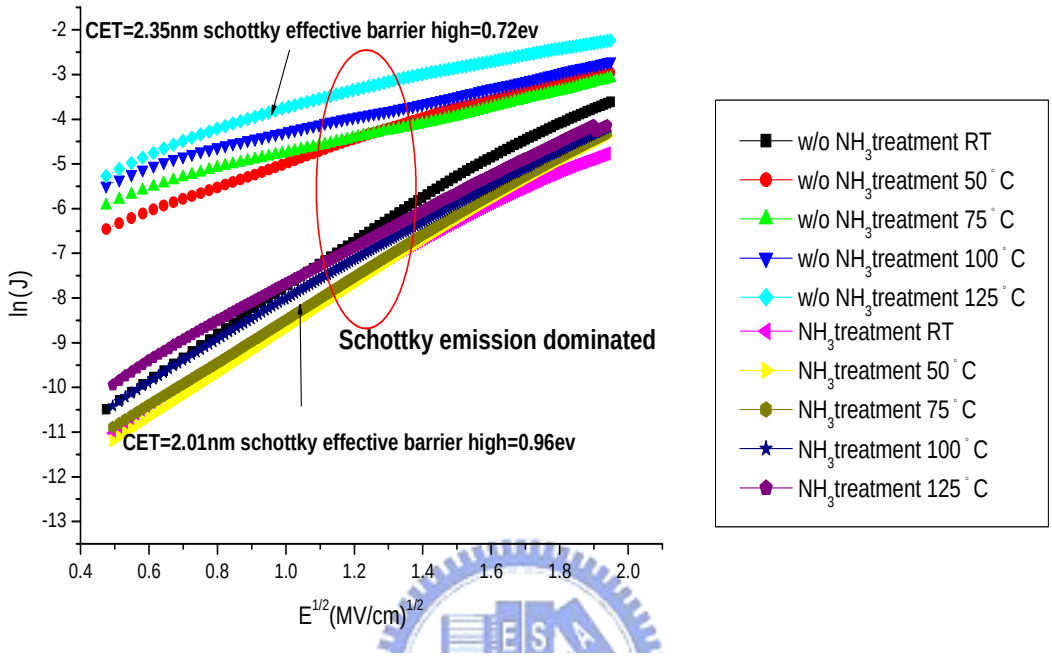


Fig.3-10(b) The conduction mechanism fitting of Al_2O_3 samples with NH_3 and w/o NH_3 treatment after PDA 900℃ in a N_2 ambient

Chapter 4

Conclusions and Suggestions for Future Work

4.1 Conclusions

In this thesis, characteristics and reliability of Al_2O_3 gate dielectrics with pre-deposition NH3 treatment and rapid thermal annealing in O_2 and N_2 ambient have been investigated. Several important phenomena were observed and summarized as follows. PDA can effectively reduce leakage current. For the samples with PDA at O_2 ambient, the interfacial layer increases with the higher PDA temperature. It is obviously that O_2 penetration will induce the increasing of the interfacial layer at Al_2O_3/Si-substrate and higher annealing temperature will speed up interface layer growth rate. For samples with PDA in a N_2 ambient, the void–defect of sputtered Al_2O_3 film will be eliminated. The as deposited Al_2O_3 film shows larger roughness, and after PDA it will become smoother. However, with higher PDA temperature, surface rough will slightly increase. The surface NH_3 treatment, can lower the CET value, and reduce the leakage current. In additional, the dielectric reliability was enhanced with NH_3 treatment. The low Weibull slope of Al_2O_3 film may result from sputter-induced defects causing weak spots. Significant process improvements are necessary to enhance dielectric quality ,such as MOCVD, ALCVD. The conduction mechanism in Al_2O_3 film was investigated by the various temperature measurement

and fitting. The conduction mechanism in Al_2O_3 thin film is dominated by Schottky conduction which occured for insulators with fewer defects and a more perfect metal-insulator interface. Samples after NH_3 treatment will have higher barrier high to reduce the leakage current.

4.2 Suggestions for Future Work

From recent reports, the major potential show-stoppers for high-k gate dielectrics are considered to be (a) interfacial layer thickness and quality, (b) film morphology after the whole thermal process, (c) reliability issues. Base on the above results, Al_2O_3 gate dielectrics with pre-deposition NH3 treatment and rapid thermal annealing can have very notable improvement. But still several works are worthy to do in the future and are recommended here.

(1). MOSFET devices fabrication with the above results：

The issues in the integration of Al_2O_3, and it's performances can be investigated with the device structures. Mobility is the first concern for considering device performance. Interfacial layer thickness and quality are related to mobility degradation and scaling limit.

(2). More potential interfacial layer investigation：

It is difficult to make a balance between the low leakage current tunneling and the low EOT. The quality of the NH_3 treatment interfacial layer still could be improved. Moreover, in order to improve the quality at high-k/Si-substrate interafce, how to determine the composition of nano-crystals and the boundary layer around crystals is

a key to answer this question.

(3). More potential surface treatment investigation：

For the NH_3 surface treatment, the excellent improvement of properties are observed. However, the large traps are still existence in NH_3 surface treatment samples. Other more potential interfacial treatments maybe can be developed to minimize the defects. For example：N_2O gas treatments.

(4). More potential deposition method investigation：

For reactive sputtering in Ar/O ambient to deposit Al_2O_3 film, it can not avoid with sputter damages. These damages will become leakage path and can not be accepted to nanometer CMOS fabrication. Other potential manufacturing system like MOCVD maybe can be developed to deposit high quality Al_2O_3 film.

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碩士論文題目 ：

高介電常數材料氧化鋁在矽基板上之介面特性研究

The Interface Investigation of High-K Material Al_2O_3 on Si Substrate