國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

射頻CMOS主動電感器的研究與應用

The Study of Radio Frequency CMOS Active Inductors and Applications

研 究 生 ：楊 鎮 澤

指導教授 ：李 鎮 宜

中華民國 九十五 年 二 月

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推薦函

本人所指導之博士班學生楊鎮澤先生，業已完成博士班之學科課程及相關研究。楊君主要從事於CMOS射頻主動電感器的研究與其應用於射頻電路的研究工作，其論文題目『射頻CMOS主動電感器的研究與應用』（The Study of Radio Frequency CMOS Active Inductors and Applications）針對主動電感器於射頻電路的應用、改善主動電感的特性提出理論探討、模擬結果及晶片實現的驗證與改善後的主動電感器應用於寬頻放大器及電壓控制振盪器的電路設計，相關成果如下：

[1] **Jyh-Neng Yang**, Chen-Yi Lee, Terng-Yin Hsu, Terng-Ren Hsu, and Chung-Cheng Wang, "A 1.5-V, 2.4GHz CMOS low-noise amplifier," *Proc. of the 43rd IEEE Midwest Symposium on Circuits and Systems*, Vol. 2, pp. 1010–1012, 2000.

[2] **Jyh-Neng Yang**, Chen-Yi Lee, Yi-Chang Cheng, Terng-Yin Hsu, and Terng-Ren Hsu, "A Tunable Low Power 2.06GHz CMOS LNA with Inductor-less and Negative Conductance Generator," *International Symposium Signal on Signals Circuits and Systems*, pp. 393–396, 2001.

[3] **Jyh-Neng Yang**, Chen-Yi Lee, Yi-Chang Cheng, Terng-Yin Hsu, and Terng-Ren Hsu, "A Low-Power 2GHz CMOS LNA with Active Inductor and Negative Conductance Generator," *the 5th WSEAS/IEEE CSCC, MCP, MCME*, pp.8-15, July 2001.

[4] **Jyh-Neng Yang**, Yi-Chang Cheng, Terng-Yin Hsu, Terng-Ren Hsu, and Chen-Yi Lee, "A 1.75GHz Inductor-less CMOS Low Noise Amplifier With High-Q Active Inductor Load," *Proc. of the 44th IEEE Midwest Symposium on Circuit and Systems*, 2001.

[5] **Jyh-Neng Yang**, Yi-Chang Cheng, Tsung-Kuel Kang, and Chen-Yi Lee, "A novel Inductor-Less 2.4 GHz CMOS Band-Pass Amplifier," *Cross Strait Tri-Regional Radio Science and Wireless Technology Conference*, vol. 8, pp. 220-222, Sep. 2002.

[6] **Jyh-Neng Yang**, Yi-Chang Cheng, and Chen-Yi Lee, "A Design of CMOS Broadband Amplifier with High-Q Active Inductor," *Proc. of the 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications*, pp. 86-89, June 2003.

[7] **Jyh-Neng Yang**, Yi-Chang Cheng, and Chen-Yi Lee, "A Novel RF CMOS Active Inductor," *IEICE Transaction Communication*, Vol. E86-B, No.7, pp. 2190-2192, July 2003.

[8] Ming-Juei Wu, **Jyh-Neng Yang**, and Chen-Yi Lee, "A Constant Power Consumption CMOS LC Oscillator Using Improved High-Q Active Inductor with Wide Tuning-Range," *Proc. of the 47th IEEE Midwest Symposium on Circuit and Systems*, July 2004.

[9] Chen-Yi Lee, **Jyh-Neng Yang**, and Yi-Chang Cheng, "Improving RF CMOS Active Inductor by Simple Loss Compensation Network," *IEICE Transaction Communication*, Vol. E87-B, No. 6, pp. 2195-2198, June 2004.

[10] **Jyh-Neng Yang**, Ming-Jeui Wu, and Chen-Yi Lee, "Loss Compensation in RF CMOS Active Inductor Using a Capacitor," *IEICE Transaction Electronic*, Vol. E87-C, No. 12, pp. 2198-2201, December 2004.

[11] **Jyh-Neng Yang**, Ming-Jeui Wu, and Chen-Yi Lee, "An Improving Active Inductor Using a Compensation Resistor," *WSEAS Transactions on Circuits and Systems*, Issue 11, Vol. 4, pp. 1529-1532, December 2005.

[12] **Jyh-Neng Yang**, Ming-Jeui Wu, Zen-Chi Hu, Terng-Ren Hsu, and Chen-Yi Lee, "CMOS LC Oscillators Using High-Q Active Inductors with Constant-Power Consumption," *WSEAS Transactions on Circuits and Systems*, Issue 12, Vol. 4, pp. 1834-1841, December 2005.

目前尚有兩篇期刊論文正在審查中，除此之外，楊君近幾年來連續通過申請國科會的相關研究計畫繼續進行此領域的相關研究，目前也於明新科技大學電子系任教，正帶領學生從事射頻IC方面的研究工作。

總言之，楊君於過去幾年的研究期間，已滿足本所在課業及研究上的要求，並在團隊研究方面，獲得肯定，因此特以推薦之。

推薦人：

中華民國 九十五 年 二 月

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論文口試委員會審定書

本校電子工程學系電子研究所博士班 楊鎮澤 君

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合於博士資格標準、業經本委員會評審認可。

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中 華 民 國　九十五　年　二　月　二十四　日

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Date : 2006-02-24

We have carefully read the dissertation entitled The Study of Radio Frequency CMOS Active Inductors and Applications

submitted by Jenn-Tzer Yang in partial fulfillment of the requirements of the degree of DOCTOR OF PHILOSOPHY and recommend its acceptance.

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摘要

在本論文中，我們首先針對各種不同的CMOS主動式電感器(Active Inductor)與負電導產生器(Negative Conductance Generator)的組合應用於不同工作頻率的射頻放大器設計研究，並且對各種不同的主動式電感器使用不同的損失補償技術來改進此電感器特性的設計。接著將此改進的主動式電感器應用於寬頻放大器(Wideband Amplifier)與電壓控制震盪器(Voltage-Controlled Oscillator)電路，以證實射頻電路中使用主動電感器能得到比使用平面螺旋型電感器(Planar Spiral Inductor)有更好的優點。如，可得到很高的品質因數(Quality Factor)、高的電感量(Inductance)等特性；並且使用主動式電感器的射頻電路於晶片製作時的面積將比使用平面螺旋型電感器的射頻電路所佔的晶片面積小很多的優點。

本論文首先描述使用平面式螺線型電感器元件應用於射頻放大器設計，雖能得到良好的特性結果，但仍有些缺點產生。如，平面式螺線型電感器佔用的晶片面積太大、品質因數很低、不容易準確控制電感的特性等缺點。而這些缺點可以使用主動式的電感器來給予改善。應用目前已經存的主動電式感器結合改進電感器特性的負電導產生器技術設計工作於不同頻帶的射頻放大器。經由模擬結果得到輸出的增益可達到17dB以上、雜訊指數低於6dB，此結果與使用平面式螺線型電感器相近，而面積為使用平面式螺線型電

感器的四分之一及使用主動電感器的功率消耗也有明顯的降低。所以，得知使用主動式電感器將優於使用平面式螺線型電感器。

然而，為降低改善主動電感器特性的電路複雜度，提出各種不同的簡單補償電路對各種不同的電感器作改良設計，得到高效能的主動電感器，且能得到電路非常簡單的電感器。經由數學的分析、電路的模擬及實際的測量結果，此改良後的電感器可得到很高的品質因數（約10^4以上）。最後，將此改良後的主動式電感器應用於寬頻放大器及電壓控制振盪器的電路中。於寬頻放大器可以得到頻帶寬度由0Hz到1GHz有平坦的增益（約18dB）特性。對於電壓控制振盪器得到寬的調整範圍（1GHz到3GHz）、-98dBc/Hz的相位雜訊及10mW的固定功率消耗。因此，經由以上的研究結果證實使用主動電感器於射頻電路為一種可行的方法，此種方法可使設計射頻電路時可以大幅的降低所佔的晶片面積的成本。

The Study of Radio Frequency CMOS Active Inductors and Applications

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Abstract

In this thesis, we will focus on the research illustration and design comparison on combing several different CMOS active inductor with negative conductance generator (NCG) applied in RF amplifier on different operating frequency. And we will apply various loss compensation techniques on several different active inductors to improve the characteristics of the inductors. Furthermore, we applied the improved active inductor on the wideband amplifier and the voltage-controlled oscillator to prove that using the active inductors in RF can have more advantages than using the planar spiral inductor. For example, the active inductor can have a higher quality factor, a higher operating frequency, and a higher inductance etc. On the other hand, in radio frequency circuit design, the size of the chip used in an active inductor will be much smaller than the one used in a planar spiral inductor.

The design of the use of the planar spiral inductor applied on the radiofrequency amplifier will be described at the beginning of the thesis. Though the above design shows the result of performing good characteristics, some disadvantages of this design also exist. For example, the size of the chip of the circuits using planar spiral inductor too large, quality factor is too low, and the characteristics of the inductor cannot be controlled easily and accurately. We presented the use of the active inductor to improve the disadvantages mentioned above. We applied the techniques of the negative conductance generator, which

combines the existing active inductor and the characteristics of the improved inductor, to work on the different bandwidth radio frequency. From the simulation results, we found that the output power gain is over 17dB, and the noise figure is lower than 6dB. The simulation also shows that the results are very close to those using the planar spiral inductor, and the size of circuit using the active inductor design is one forth of that using planar spiral inductor. Moreover, the power consumption decreases dramatically when using active inductor. So, we can conclude that using active inductor generates more benefits than using planar spiral inductor.

For minimizing the complexity of the active inductor circuits, we present several simple compensated circuits for each different active inductor to reach the goals of performing higher performance and an easy design circuit. From the mathematical analysis, simulated results, and measured results, the improved active inductor can obtain a very high quality factor, which is above 10^4. Finally, we present the results of applying the improved active inductor in the circuits of wideband amplifier and voltage-controlled oscillator. From the wideband amplifier's point of view, the amplifier can generate a flat gain, which is about 18dB, in the bandwidth from 0Hz to 1GHz. From the voltage-controlled oscillator's point of view, the voltage-controlled oscillator can generate a wide tuning range from 1GHz to 3GHz, -98dBc/Hz phase noise and steady 10mW power consumption. As the result, we can conclude that using active inductor in the radio frequency is a workable solution via the approach mention above. This solution also saves us a lot of cost taken by the size of the chip during the design stage of the radio frequency.

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Chapter 1

Introduction

1.1 Motivation

In recent years, wireless telecommunication systems are expanding in many directions. The rapid growth of wireless systems has led to an increasing demand of light, inexpensive, low power, handheld terminal, and high-performance communication systems. The operational frequency bands of the wireless system are from 900MHz to several GHz, or even above. For example, advanced mobile phone service (AMPS), group special mobile (GSM), intelligent transport system (ITS), and wireless local area network (WLAN) are 900MHz, 1.9GHz, and over 5GHz for the personal communication network (PCN), digital European cordless telephone (DECT), and IEEE 802.11a, respectively [1-3]. In such a high-frequency band, the complete systems often contain many IC's and discrete components to obtain the maximum performance/cost ratio. Thanks to recent advances in CMOS technology, a cut-off frequency f_T is competitive with that of BJT, BiCMOS, and GaAs technology. Therefore, all-CMOS implementation is one of the most attractive solutions to obtain a low-cost and a high-integration wireless system [4, 5].

In a CMOS wireless transceiver, the key factor of obtaining an all-CMOS system is availability of high-performance CMOS RF front-end circuits, which include the low noise

amplifiers (LNAs), the band pass filters (BPFs), the mixer, the voltage-controlled oscillators (VCOs), and the power amplifiers (PAs). Recently, much effort has been devoted to the design of RF circuits in CMOS technology. With the special techniques developed to overcome some of the limiting factors, the proposed CMOS LNA [6-8], the mixer [9-11], VCO [12-14], the BPF [15], and the PA [16, 17] have good high-frequency performances.

In the CMOS RF front-end circuits, the inductors are fundamental components for the design of all RF circuits. Most inductors of the published RF circuits are implemented by using on-chip planar spiral inductor [18-22]. Planar spiral inductors are used in an extensive range of applications in monolithic microwave integrated circuits (MMICs), including biasing and matching impedance circuitry, filters, VCOs, analog phase shifts, and others. However, the utilization of these planar spiral inductors presents many drawbacks: the large occupied area, the difficulty to obtain high inductance values, and the low quality factor, typically in the range of 10-30 [23]. In fact, the large area involved in the realization of these spiral inductors, when compared with the normally area occupied by others lumped components utilized in integrated circuits (ICs), such as capacitors, resistors, and field effect transistors (FETs). It essentially determines the physical size of the integrated circuits [24].

In addition, the physical dimensions of the planar spiral inductors directly relate to the desired inductance value. The higher inductance values will require the larger physical dimensions. Furthermore, the operational frequency of the planar spiral inductor is usually limited, particularly in the case of relatively high inductance values (above 5nH), by the stray capacitances associated to these components [25, 26]. Besides, owing to the variations in the fabricated process, the accurate inductance and the required characteristics are difficultly achieved.

As an attempt to overcome these limitations, an alternative technique, called active inductor, is presented. The active inductor is implemented by means of circuit configurations

using active devices (FETs), called the gyrator. Specifically, a convenient association of transistors, capacitors, and resistors can combine into a circuit that will be equivalent to inductance impedance. In turn, depending on biasing conditions of the gyrator circuit, this inductance impedance can be taken as a series/parallel L-R-C circuit. The inductance values obtained by means of this active technique can be high enough to overcome the values exhibited by the conventional planar spiral inductors. In addition, the stray capacitances associated to gyrator circuits may be almost completely cancelled, which permits to extend the useful operating frequency of these circuits [27-30].

Also, the obtained inductance and series/parallel resistance values can be independently varied, within a narrow frequency range, by applying an external voltage control [31, 32]. The external control voltage can also correct the variations due to the changing in fabricated process. Finally, depending on the chosen topology, the insertion loss associated to these active inductors can be made very small. As a result, higher quality factors (Q-value) can be obtained. In fact, some configurations can reach quality factors in the range of thousands, widely exceeding the conventional planar spiral inductors. Moreover, the area of active inductors is much smaller than other components and their area is totally independent of the desired inductance values.

In recently years, CMOS active inductors and their applications have been explored in some literatures [33- 37]. However, in RF CMOS technology, a constant internal loss exists in active devices. The loss is caused by the conductance between drain and source of a MOSFET, DC bias circuits [38, 39], etc. As a result, in RF CMOS active inductor applications, these losses limit the Q-value, the inductance and the operating frequency. To obtain the higher Q value, the higher inductance, and the higher operating frequency, the Q-enhancement techniques of the active inductor circuit to compensate these internal losses are proposed [34, 38, 39]. Although, remarkable improvement is obtained in the

Q-enhancement design, the complexity and power consumption of the active inductor becomes increasing, and hence the cost/performance ratio will be significantly increased. Therefore, in order to explicate the advantages and improve the characteristics of active inductor, the studies and the applications of the CMOS active indictors are presented.

First, in this work, a low noise amplifier based on inductors is presented. Although, the amplifier achieved good performances, the passive spiral inductors occupied larger die area than other components. To reduce the die area, a design based on an active inductor is proposed. Second, a principle for the characteristics of inductance impedance is described. Based on the principle, several different active inductors are proposed. And various RF amplifiers, which use the original active inductors, are designed to operate in different frequency bands. As a result, these circuits can obtain similar characteristics obtained from using a planar spiral inductor. Moreover the die area is much smaller than that of the circuits with planar spiral inductors. Third, we present the RF CMOS high Q-value active inductors, which adopt a simple cascode RC feedback, a gain-boosting and current-reused circuit, a capacitor, and a resistor loss compensated techniques to overcome the loss of the active inductor. In addition, mathematic analysis, simulation results, and measured results show that the performances of the proposed active inductor can achieve better characteristics, such as Q value, inductance, and operating frequency, than those published in the previous literatures. Finally, RF circuit applications of the wideband amplifier and the LC oscillator based on the improved active inductors are designed. As a result, these application circuits can meet a required performance. Therefore, a CMOS RF front-end circuit using active inductor can be a good candidate to replace the circuit using planar spiral inductors.

1.2 Thesis Organization

In this dissertation, we first focus on the design of a low noise amplifier using planar spiral inductor. And then, the principles and the characteristics of the active inductor are described. We proceed with the RF amplifier circuit designs with the original active inductors to verify that die area using an active inductor is smaller than that of the die area using a planar spiral inductor. To improve the performance and reduce the complexity of the active inductor, we concentrate on the circuit design of the active inductors. By means of mathematical analysis, the simulated verification, and the measured results show that the active inductors based on several compensated methods can significantly improve quality factor (Q), inductance (L), and operating frequency of the RF CMOS active inductors. And for the CMOS RF circuit applications, the wideband amplifier and the LC oscillator applying with the improved active inductors are proposed. As a result, the proposed RF front-end circuits obtain competitive performances compared with the circuit based on planar spiral inductors and used active inductor published previous literatures. Consequently, die area of the circuits using the active inductor is much smaller than that of the conventional circuits using planar spiral inductors.

In chapter 2, we present a low noise amplifier with planar spiral inductors for discussing the related problems caused by using passive inductors within RF circuits. Although, the amplifier based on the planar spiral inductors obtains good performances, the amplifier results in many drawbacks. Especially, the passive spiral inductors are main components that occupy larger die area than other components such as resistors, capacitors, and transistors. Furthermore, due to process variation, to obtain an accurate passive spiral inductor is very difficult. Therefore, we propose a solution of applying active inductors for overcoming the disadvantages caused by using planar spiral inductors. We present an overview of a CMOS active inductor. The principle of the active inductor for the inductance

impedance is caused by the feedback configuration of back-to-back connection of transistors. The inductance impedance includes both of the inductance and the internal loss. The internal loss is a main factor, which affects the performance of the active inductor. The performances of the active inductor will depend on the various circuit topologies. In recent years, various CMOS active inductors have been explored in some literatures. We survey some CMOS active inductor circuits and applications in this chapter.

In chapter 3, using the active inductors of the previously published literatures to design the availability for the inductor-less RF amplifier is proposed. According to the simulation results, the performances of the RF amplifiers based on an active inductor are similar with that using planar spiral inductor. But the die area of the RF amplifiers with active inductor is much smaller than that with planar spiral inductor. Moreover, the performance of these ordinary active inductors can be improved by compensation techniques to obtain a higher performance. Although compensation such as negative impedance converter has been presented, the active inductor circuits are very complicated. Therefore, in this work, we present simple compensated techniques to achieve a simpler active inductor circuit than those designs published in the literatures. Besides, the proposed active inductor circuits are very simple and the active inductors achieve higher Q, higher operating frequency, and higher inductance.

In chapter 4, the improved active inductor circuit designs using four simple distinct loss compensated techniques to obtain higher performance and reduce circuit complexity are presented. To improve Q-value, operating frequency, and inductance of the active inductor, four different loss-compensated techniques such as cascode RC feedback, gain-boosting and current-reused, using a capacitor, and only using a resistor to aim at different circuits of the active inductor are described. According to the measured results, the proposed active inductors can achieve higher Q-value, higher inductance, higher operating frequency, and less

circuit complexity. As a result, the performance of the proposed active inductors is better than those from previous designs [34, 36, 37, 38, 41].

In chapter 5, the designs for wideband amplifier and LC oscillator using the proposed active inductor with distinct loss compensated techniques are presented. In these applications, the wideband amplifier is designed with the proposed active inductor based on cascode RC feedback loss compensated circuit to obtain wide frequency response, high enough power gain, and reasonable noise figure. The LC oscillator circuit is implemented by using the improved active inductor based on a resistor loss compensated technique to achieve wide tuning range, low phase noise, constant power consumption, and frequency-independent phase noise. According to the simulated and measured results, we've got an 18dB wideband amplifier gain and 1GHz bandwidth with the requirements of 8dB noise figure and a reasonable linearity (-16dBm of IIP3). Moreover, the VCO circuits presented a reasonable output voltage, wide tuning range (1GHz to 3GHz), and without changing the phase noise (-98dBc/Hz) and the power consumption (10mW) due to the change of output frequency. So, the sub-circuit of the RF front-end based on the active inductor can be realized.

In chapter 6, we make some conclusions and outline future research directions. In the active inductor designs, the characteristics are better than the planar spiral inductor such as Q-value, inductance, operating frequency, and die area. In RF front-end applications, the main keys to complete high performance CMOS active inductor and wideband amplifier and LC oscillator, are briefly summarized. And performances of the RF front-end circuit can compete with the circuits using the planar spiral inductor. Although higher Q-value, higher inductance, and higher operating frequency CMOS active inductor can be obtained, other design issues such as noise, power consumption, and dynamic range of the active inductor need to be further improved. Furthermore, sub-circuits of the RF front-end in this research can be integrated together to reach a single chip solution.

Chapter 2

An Overview of Active Inductors

This chapter starts with the discussion of using planar spiral inductors to design CMOS RF amplifier. And a discussion about the related problem after using planar spiral inductors applied in an amplifier will also be presented later. We can use active inductors to minimize the disadvantages caused by using planar spiral inductors. So, we will start from the introduction of the principle of an active inductor, and the discussion about the characters of an active inductor will be introduced afterwards. The CMOS active inductor related circuit architectures and its applied designs would be presented at the end of this chapter.

The organization of this chapter is as follows. In section 2.1, we will describe the methodologies using passive inductors to design a RF amplifier, and the discussion of the disadvantages will also be presented. In section 2.2 the basic principle and the characteristics of an RF CMOS active inductor for inductance impedance is presented. The generated inductance impedance includes both the real term and the imaginary term. They are used to describe the characteristics of the active inductor. In section 2.3, we describe some research of the published RF CMOS active inductors and the applications that exist in present research. Finally, a brief summary is given in section 2.4.

2.1 Design of 2.4GHz CMOS RF Amplifier Using Planar Spiral Inductors

As we know, the first stage of a receiver is commonly a low-noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of the subsequent stages (such as mixers) without inducing overload in mixer. Secondly, an LNA should induce as little noise as possible to minimize the impact on overall noise performance. Thirdly, an LNA should accommodate large signals without distortion, i.e., acceptable linearity. Frequently, an LNA must also provide specific impedance, such as 50 Ohms, to the input source and the output load, which are particularly important to reduce energy loss. In addition, an LNA should provide low power consumption especially in portable systems. The design of an LNA involves trade-offs among optimum gain, lowest noise figure, optimum input and output matching, high linearity and lower power consumption. Recently, advances in CMOS technology, a cut-off frequency f_T is competitive with that of BJT, BiCMOS, and GaAs technology. Therefore, all-CMOS implementation is one of the most attractive solutions to provide the possibility of the integration of complete communication systems.

2.1.1 Circuit Design

Following the circuit design given in [19], and with details presented in another reference [20], the complete circuit is shown in Fig. 2.1. It was found that a two-stage amplifier is required to achieve the desired gain and to provide a good isolation between input and output. The first stage is a cascode amplifier consisting of M2 and M3. L1 and L2 are for input matching. L3 and CL form a tank circuit to tune the LNA to 2.4GHz. M4 is the output stage with a matching network of L4 and C3. M1, R1, and RD form a bias circuit. M1

is a current mirror with RD, while R1 prevents the bias circuit from shunting the RF input signal. C1, C2, and C3 are used as a DC blocking capacitor. Vin and Vout are input/output source voltage ports respectively.

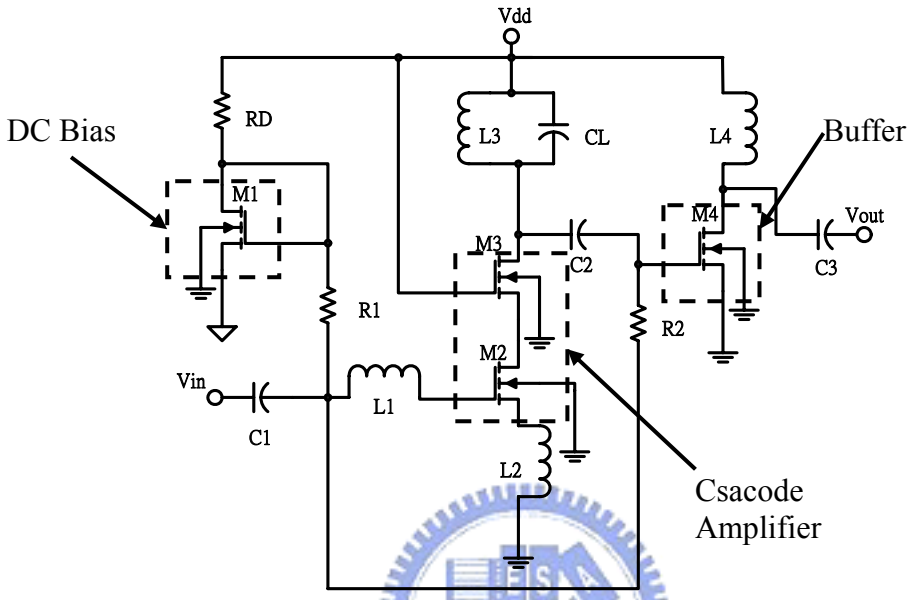


Fig. 2.1 Low noise amplifier using planar spiral inductors

2.1.2 Simulation Results

The proposed circuit was simulated using Serenade 8.5 simulator. All transistor models are Bsim3v3 for TSMC 0.35 um process. Fig. 2.2 shows the forward gain of LNA. The amplifier provides a forward gain of 33dB at 2.4GHz. Noise Figure (NF) is obtained and shown in Fig. 2.3. Simulation results show that this LNA achieves a noise figure of 1dB at 2.4GHz. Both S11 and S22 parameters of LNA are illustrated in Fig 2.4. The simulated S11 and S22 are –23dB, -9dB respectively. The linearity of this LNA, which is normally evaluated by the input referred third-order intercept point (IIP3), is plotted in Fig. 2.5. The simulated IIP3 is around 0dBm. Fig. 2.6 shows the response of input power versus output power, which indicates the 1dB compression point. The simulated 1dB compression point

is –26dBm. The complete layout of the LNA circuit, shown in Fig. 2.7, was realized by TSMC 0.35um CMOS technology with a die size of 850um×600um. The LNA drains 10.8mA from a 3.3V supply and the power dissipates 35.6mW at 2.4GHz frequency.

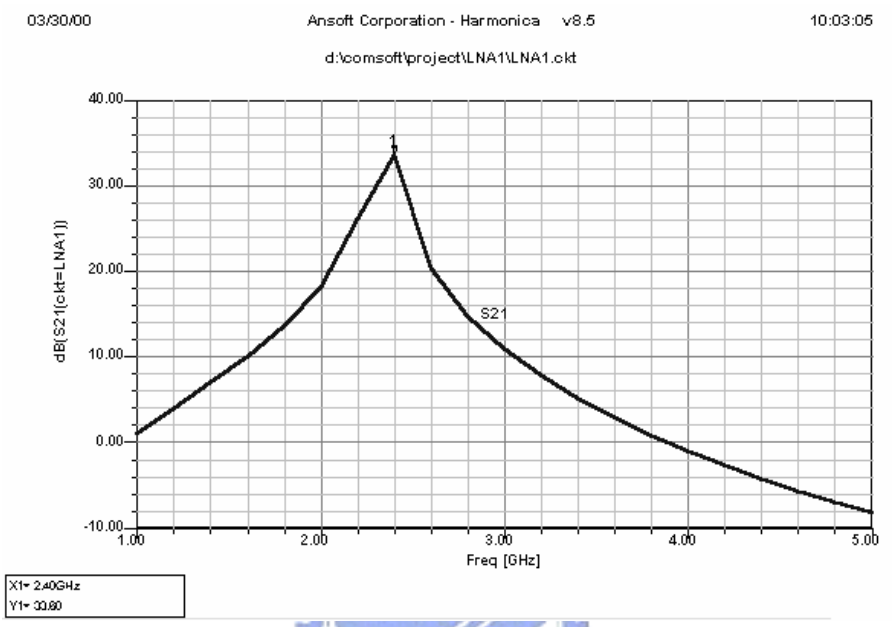


Fig. 2.2 Forward Gain S21 of LNA

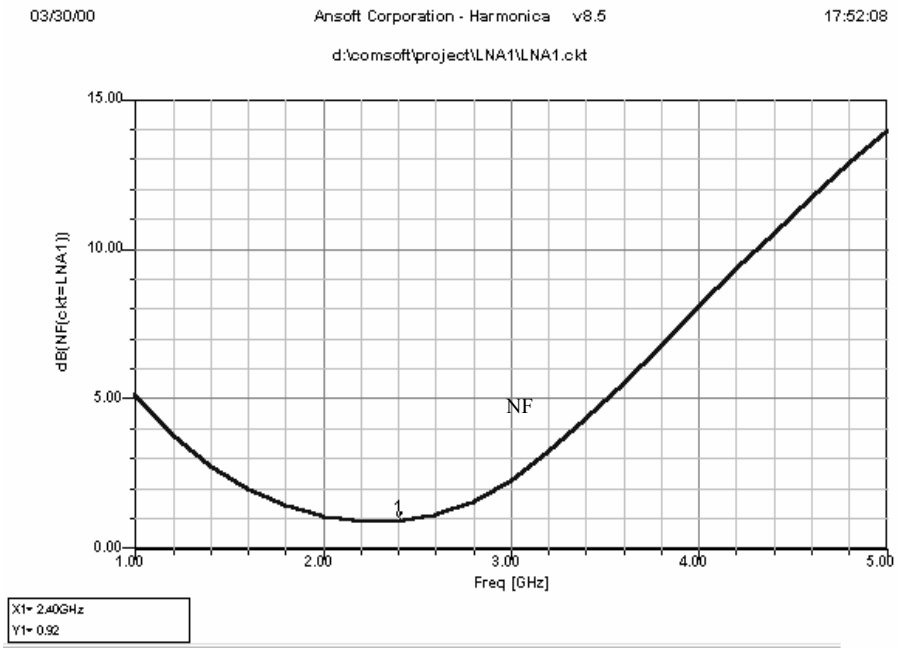


Fig. 2.3 Noise Figure (NF)

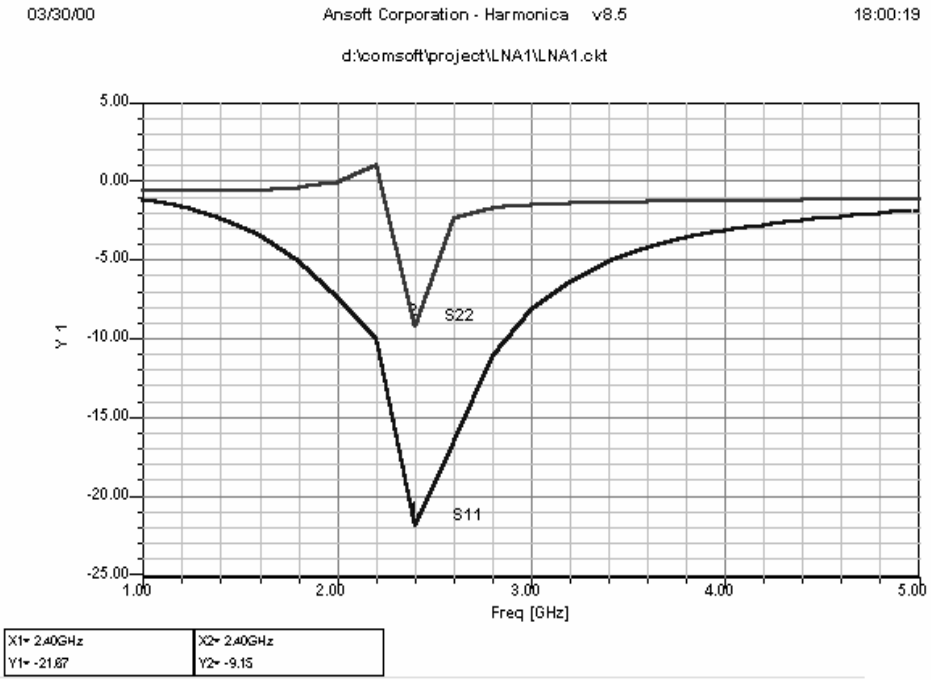


Fig. 2.4 S-parameter (S11, S22)

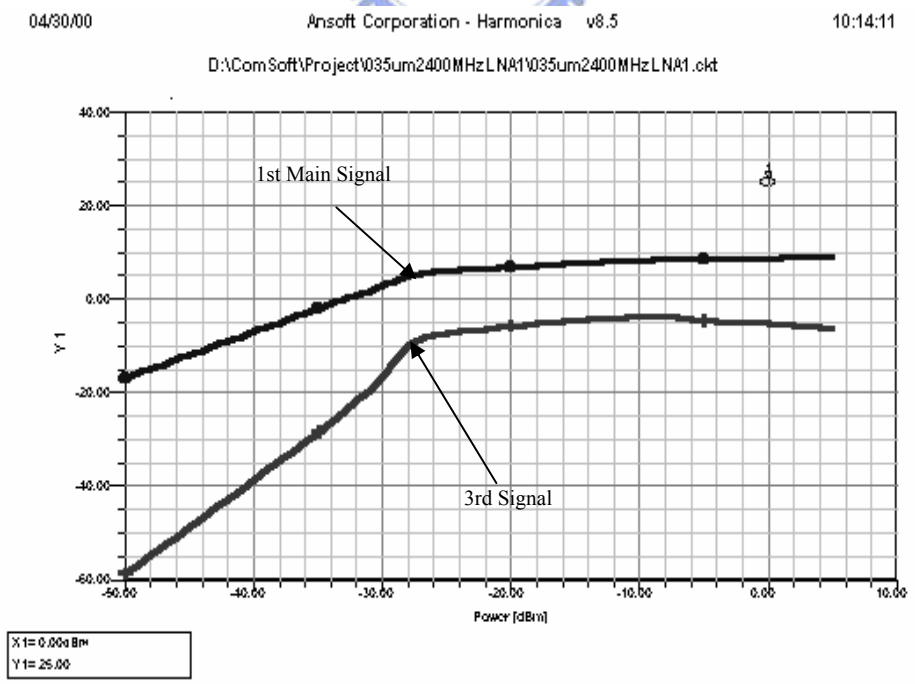


Fig. 2.5 The response of IIP3

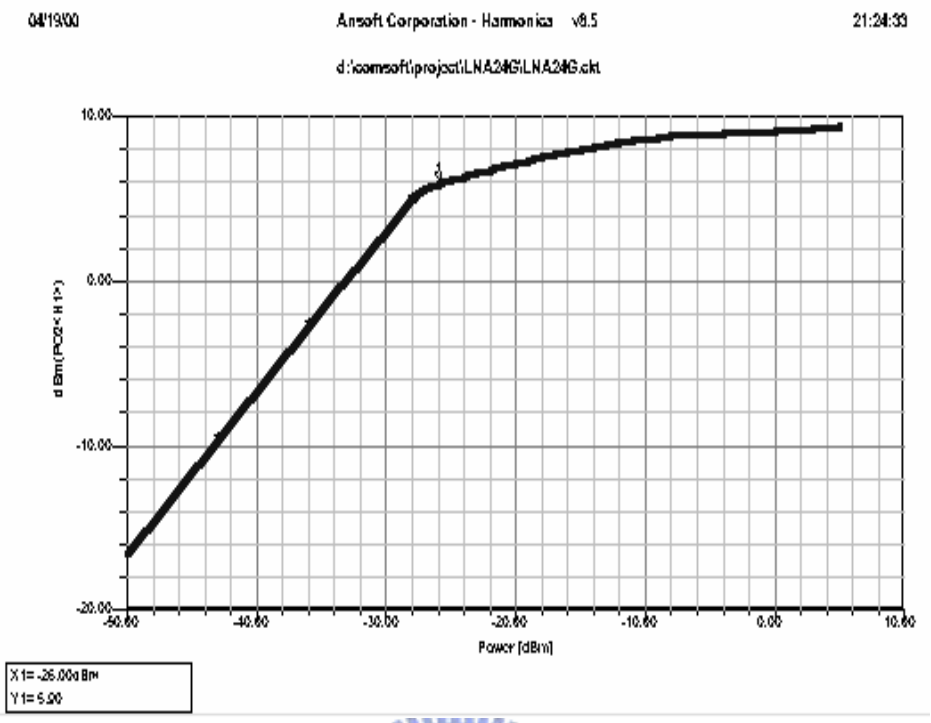


Fig. 2.61dB compression

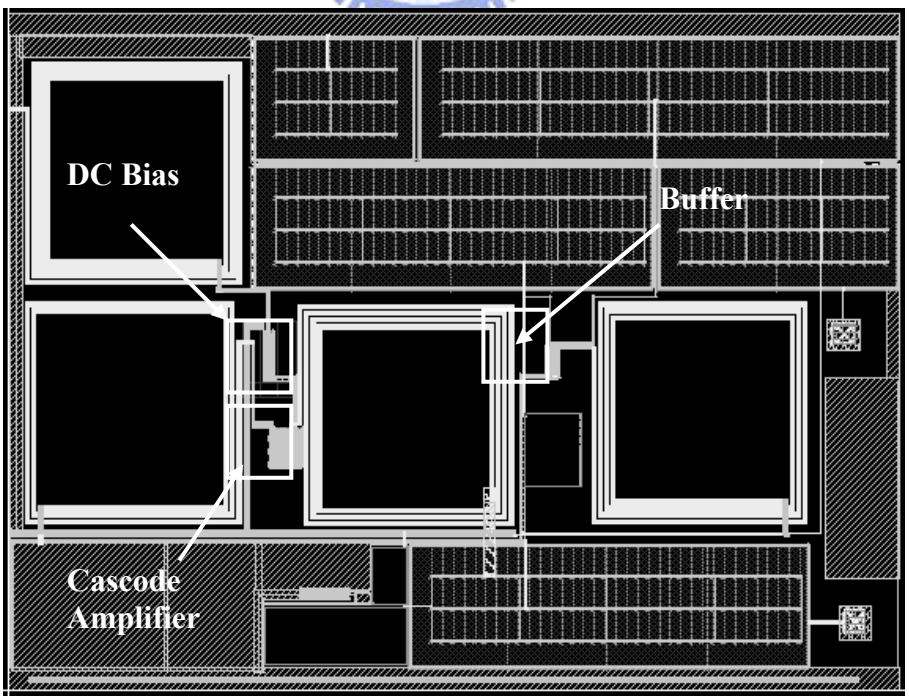


Fig. 2.7 Layout of proposed LNA

2.1.3 Discussion

In this section, we have demonstrated a low noise amplifier in a standard TSMC CMOS 0.35um process. The amplifier was applied with planar spiral inductors. Based on the simulation results, we believe that CMOS is a suitable technology for wireless transceiver design and will provide the integration of a complete communication system on a single chip. Although the amplifier reaches acceptable performance, many of the drawbacks exist in the amplifier. Especially, the area of the planar spiral inductors is much larger than the others components, such as active devices (MOSFET). In additional, to obtain an accurate passive spiral inductor is very difficult. During the process of IC manufacturing, any change within the processing stage will affect the characters of the inductor. Moreover, the characters changed would also generate certain character change within the whole circuits. Meanwhile, the Q-value of a planar spiral inductor is very low, in which its range is from 12 to 15. So, for obtaining a higher power gain, we must raise the circuit bias current. However once we raise the bias current, the power consumption will also increase at the same time. For improving the disadvantages mentioned above, we applied the advantages of using active inductors. This solution of using an active inductor not only lowers the die size and provides higher Q-value but also decreases the power consumption of the circuits. Moreover, we can use the external bias voltage to revise the unpredictable effects caused by the processing change during the IC manufacturing stage, and this solution also helps to minimize the change of the circuit characters. Therefore, an active inductor is the best alternative to improve drawbacks using the planar spiral inductor.

2.2 Characteristics of Active Inductors

Based on the principle, the characteristics of an active inductor circuit can be obtained and operated in the radio frequency range. The active inductor circuit produces characteristics of inductance impedance. The inductance impedance includes both the real term and the imaginary term. These terms can be also called the loss and the inductance, respectively. The real term and the imaginary term of the inductance impedance are fundamental factors to describe the characteristics of the active inductor. Therefore, the important parameters of an active inductor can be defined by the real term and the imaginary term of the inductance impedance, such as the quality-factor (Q), the inductance (L), and the resonant frequency (ω_0). In addition, these parameters can be used to analyze the performance of an active inductor circuit as well.

Traditionally, active inductors are typically created by using high gain operational amplifiers with negative feedback, and are thus unsuitable for frequencies close to the f_T of the transistors. An alternative strategy, which has been proposed, was using GaAs, MESFET and bipolar technologies [27, 40] to exploit capacitance with the transistors to implement the require inductance impedance. Since these techniques make use of the parasitic within the devices, the circuits can operate close to the technology limits. These parasitic methods seem promising for the implementation of high frequency active inductors in CMOS technology.

The basic principle of forming the active inductor circuit is based on a well-known gyrator theory [30]. The gyrator topology is a two-port network that can be realized by connecting in parallel and back-to-back two voltage-controlled current source of opposite polarities. Fig. 2.8 shows an arrangement of an active inductor implementation based on a capacitive load gyrator topology.

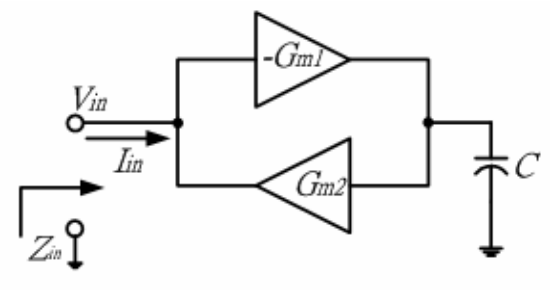


Fig. 2.8 Gyrator topology

From the input terminal in Fig. 2.8, this architecture of the gyrator simulates inductance impedance (Z_{in}), expressed as Eq. (2.1).

$$Z_{in} = \frac{V_{in}}{I_{in}} \approx \frac{sC}{G_{m1}G_{m2}} \tag{2.1}$$

where G_{m1} and G_{m2} are the transconductor of the amplifier.

In order to obtain a CMOS active inductor, the active inductor can be operated in the radio frequency band. The simplest active inductor based on a gyrator topology can be realized by using a single MOS transistor as the transconductance (G_m) element, as shown in Fig. 2.9. The active inductor exploits the intrinsic capacitances within the transistors to achieve the require poles and zeros. As a result, the active inductor is capable of operating up to the cut off frequency (f_t) of the transistors.

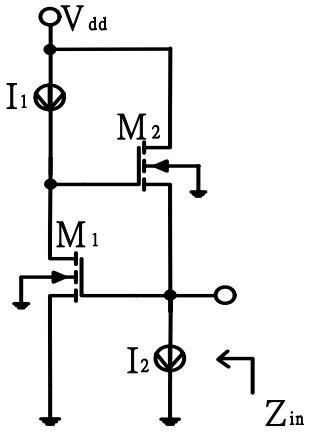


Fig. 2.9 A simple gyrator in MOS implementation

In the Fig. 2.9, if each transistor is modeled by c_{gs}, c_{gd}, g_m, and g_{ds}, the model is shown in Fig. 2.10, and then the input impedance (Z_{in}) of the circuit of the Fig. 2.9 can be derived in Eq. (2.2).

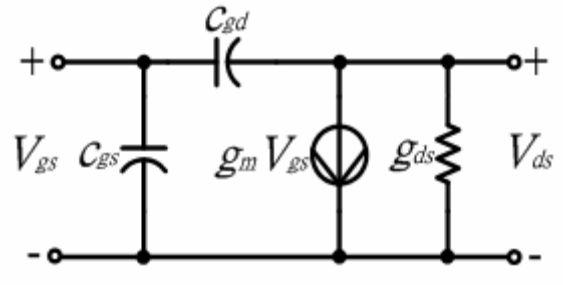


Fig. 2.10 A small-signal model of the MOS transistor

$$Z_{in} \approx \frac{s(C_{gs2}+C_{gd1}+C_{gd2})+g_{ds1}}{(sC_{gd2}+g_{ds1}+g_{m1})(s(C_{gs2}+C_{gd1})+g_{m2})} \tag{2.2}$$

where $s=j\omega$, based on a first order small signal analysis and the assumption of the $C_{gdi} << C_{gsi}$, the Eq. (2) can be simplified in Eq. (2.3).

$$Z_{in} \approx \frac{sC_{gs2}+g_{ds1}}{(sC_{gd2}+g_{ds2}+g_{m1})(sC_{gs2}+g_{m2})} = \mathrm{Re}(Z_{in}) + j\,\mathrm{Im}(Z_{in}) \tag{2.3}$$

or can be expressed as input conductance (Y_{in}).

$$\begin{aligned} Y_{in} &\approx [\frac{sC_{gs2}+g_{ds1}}{(sC_{gd2}+g_{ds2}+g_{m1})(sC_{gs2}+g_{m2})}]^{-1} \\ &= g_{ds2}+g_{m2}+sC_{gs1}+\frac{g_{m1}g_{m2}}{sC_{gs2}+g_{ds1}} \\ &= \mathrm{Re}(Y_{in}) + j\,\mathrm{Im}(Y_{in}) \end{aligned} \tag{2.4}$$

From Eq. (2.3), the input impedance, Z_{in}, is equivalent to the input conductance Y_{in}. The input impedance Z_{in} can be formed with the real term and the imaginary term, and Z_{in} is the

equivalent RLC network for the active inductor, shown in Fig.2.11. The values of all components in the Fig. 2.11 can be derived by Eq. (2.3) or Eq. (2.4), and be expressed as Eq. (2.5) to Eq. (2.8).

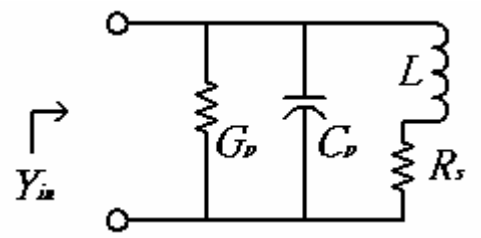


Fig. 2.11 Equivalent RLC model of active inductor

$$G_p = g_{ds2} + g_{m2} \approx g_{m2} \tag{2.5}$$

$$C_p = C_{gs1} \tag{2.6}$$

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}} \tag{2.7}$$

$$R_s = \frac{g_{ds1}}{g_{m1}g_{m2}} \tag{2.8}$$

In additional, the self-resonant frequency for the active inductor is expressed in Eq. (2.9) and the Q-value at the self-resonant frequency ω_0 can be written as Eq. (2.10).

$$\omega_0^{\,2} = \frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}} \tag{2.9}$$

$$Q_L = \frac{\omega_0 C_{gs2}}{g_{ds1}} = \sqrt{\frac{g_{m1}g_{m2}C_{gs2}}{g_{ds1}^{\,2}C_{gs1}}} \tag{2.10}$$

Therefore, based on the gyrator configuration, the circuit can obtain the equivalent input inductance impedance (Z_{in}), which produces the required parameters and includes both the real term and the imagine term to simulate an inductor. Then the equivalent input inductance impedance can be defined as the characteristics of an inductor.

In CMOS RF front-end circuits, the inductors are the fundamental component for filtering, tuning, phase shifting and matching. To achieve the required specifications in RF application circuits, a high performance inductor must be obtained. The characteristics of the inductor should basically possess a high quality factor (high Q-value), a wide inductance range, and a high operating frequency. Because a higher Q-value will obtain a higher selection, a higher gain, and a lower phase noise in RF circuit applications. A wider inductance range and a higher operating frequency will achieve more an effective inductor and a higher frequency circuit. Therefore, in CMOS RF active inductor designs, a higher Q value, a wider inductance range, and a higher operating frequency are expected.

An inductor is a component of storage energy. To store the energy for a long period of time in the inductor, the loss of the inductor should be as small as possible. Similarly, an active inductor simulates the characteristic of inductance based on active devices. The characteristic of a high-Q value CMOS active inductor implies the loss of the inductor circuit must be as small as possible.

The equivalent impedance of an inductor can be expressed as a combination of the resistance and the inductance, shown in Fig.2.12. According to the definition of the Q-value of the inductor, the Q-value can be defined as Eq. (2.11).

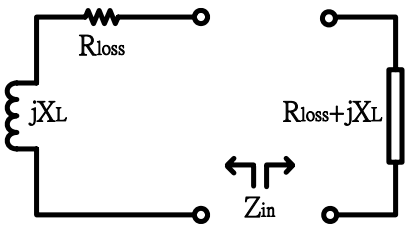


Fig. 2.12 The equivalent circuit of inductor

$$Q = \frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})} = \frac{X_L}{R_{loss}} \tag{2.11}$$

From Eq. (2.3) and Fig. 2.12, the input equivalent impedance of the active inductor combines both the real term and the imaginary term. It is called loss and inductance, respectively. The equivalent input impedance of the active inductor can also be expressed as the combination of the resistance and the inductance, shown in Fig. 2.12. And the Q value of the active inductor can be defined in Eq. (2.11) as well.

Therefore, the Q-value of the active inductor will be affected by the loss (the real term) and the inductance (the imaginary term). In order to obtain a higher Q-value, a higher inductance and a lower loss are required.

2.3 CMOS Active Inductors and Applications

Recently, CMOS active inductors and their applications have been published in the literature [33-37]. The topologies of the active inductors were implemented by using the gyrator configuration. The circuit type of the published active inductors was constructed with the common source (CS) and the common drain (CD), shown in Fig.2.9, and was connected with the common gate (CG) and the common source, which shows in Fig. 2. 13. These circuits formed the basic configurations of the active inductors.

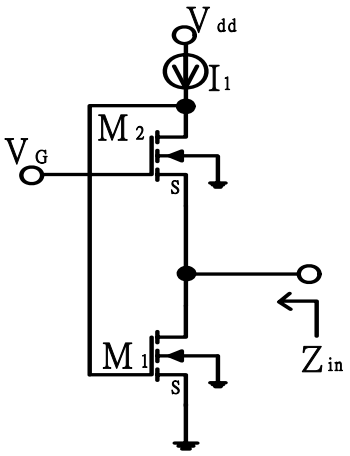


Fig. 2.13 CG-CS configuration active inductor

For the active inductor research, improving the Q value and the low operating voltage have been the trends [36-39]. The techniques of improving the characteristics of active inductors using the gain boosting, the current-reused, the double feedback, and the negative conductance compensated techniques, shown in Fig. 2.14 to Fig.2.16 have been described, respectively. Fig. 2.17 is the architecture of the negative impedance technique used to improve the Q value of the active inductor.

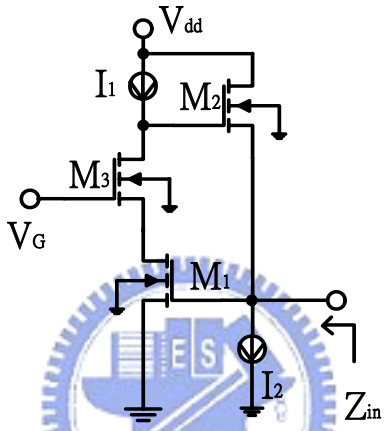


Fig. 2.14 Gain boosting compensated active inductor

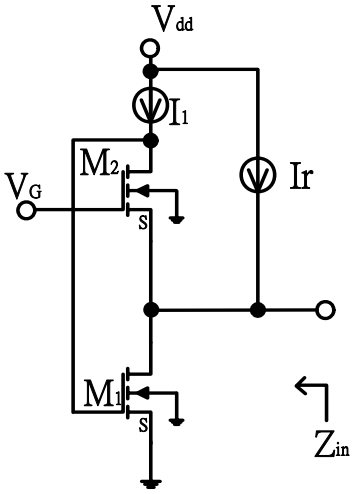


Fig. 2.15 Current-reused compensated active inductor

Although the proposed techniques can improve the Q value of the active inductor, the inductor circuits posses some drawbacks such as the complexity and power consumption. In addition, in order to operate on a low voltage, the active inductor circuit used the PMOS transistor, shown in Fig. 2.18, was proposed.

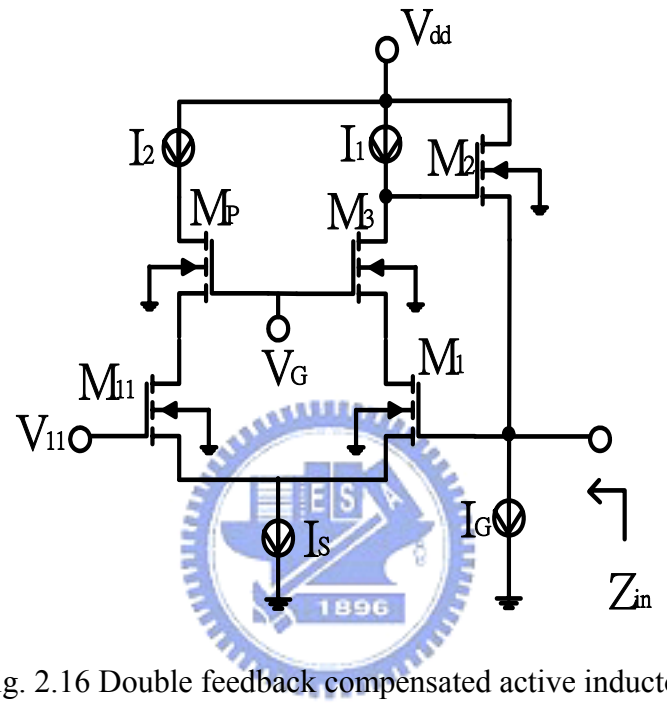


Fig. 2.16 Double feedback compensated active inductor

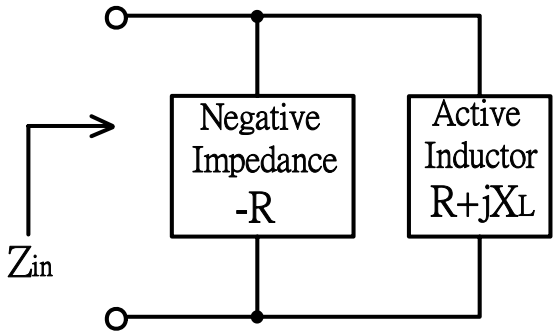


Fig. 2.17 Negative impedance compensated active inductor

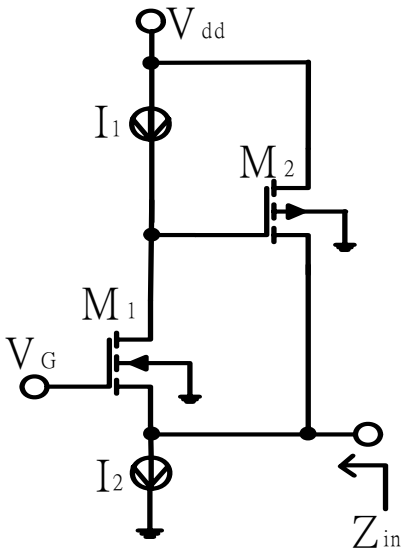


Fig. 2.18 Low voltage active inductor

For the applications of active inductors, the bandpass filters [36, 39], the low noise amplifier [32], the bandpass amplifier [24, 31], and the voltage-controlled oscillators [35, 37] based on previous research have been published [33-37]. Although, these applications have good performances, the performances can further be improved by improving the characteristics of the active inductor.

2.4 Summary

In this chapter, we will summarize the disadvantages of using planar spiral inductors to design the amplifier. The disadvantages are listed as the following: causing a larger die size and a lower Q-value, requiring more power consumption, and producing the revising difficulties. The above disadvantages can be overcome by using active inductor. The principle operation methodologies of an active inductor are based on the application of the gyrator. The gyrator configuration of using active devices can be used to simulate the active inductor to obtain the inductance impedance. The Q value and the inductance of the active inductor will

be affected by the transconductance and the capacitance of the MOSFETs. The external bias voltage will tune the transconductance of the MOSFETs. Therefore, the external bias voltage can vary the characteristics of the active inductor.

Though there are several successful solutions for enhancing the characters of the active inductors and have proposed in the literatures, there are still some other simpler ideas that have stronger capabilities to improve the characters of the active inductor. So, we will propose those simpler approaches in chapter 4.

Chapter 3

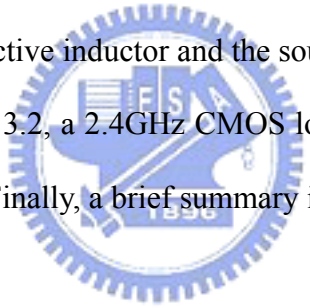
Designs of the RF Amplifiers Using CMOS Active Inductors

Motivated by the growing market of RF communications system, much effort has been devoted to the implementation of RF circuits in a CMOS technology. A low noise amplifier is the most demanding block in a RF system. The specifications of a low noise amplifier must be satisfied the following requirements which include larger power gain, lower noise figure, better impedance matching, good linearity, lower power consumption, and lower manufacturing cost. These demanded requirements have been traditionally led to the implementation of the discrete components or the use of exotic processes. Inductors are fundamental for the design of low noise amplifiers. Most of the published low noise amplifiers are implemented by using chip passive spiral or bond wire inductors. The quality factor of an integrated planar spiral inductor is normally low. For producing a higher quality factor, an integrated inductor requires additional processing steps. By applying techniques proposed in [6], it is possible to compensate the quality factor of these inductors for reducing extra manufacturing cost. Moreover, the un-tunable inductor value is dependent on the size of the inductor [24]. Thus the additional tuning circuitry is required to modify the required characteristics in our applications and it is also the main problem when we consider

minimizing the size of an inductor. For reducing the size of a traditional integrated passive inductor, an active inductor will be introduced to achieve the goals of downsizing the chips.

In this chapter, the design of the low noise radio frequency amplifiers, which are called the active inductors, are presented. Several low noise amplifier simulations using different active inductors and a negative conductance generator were performed and the simulation results showed that the characteristics of the low noise amplifiers are improving and various frequencies are operated via different combining designs of active inductors and a negative conductance generator. Especially, the occupied chip area of the low noise amplifier is significantly reduced and the characteristics of the low noise amplifiers can directly tune by using external voltage.

The organization of this chapter is as the following. In section 3.1, a 2GHz CMOS LNA with the regulated cascade active inductor and the source follower negative conductance generator is illustrated. In section 3.2, a 2.4GHz CMOS low noise amplifier with the high-Q active inductor load is proposed. Finally, a brief summary is made in section 3.3.



3.1 A 2GHz CMOS LNA with Active Inductor and Source Follower Negative Conductance Generator

In this RF low noise amplifier, the regulated cascode active inductor and the source follower negative conductance generator (NIC) are used to design the amplifier. The regulated cascode active inductor is described in section 3.1.1. The source follower negative conductance generator circuit based on a common drain with common gate is given in section 3.1.2. The design methodology of the low noise amplifier is given in section 3.1.3. The simulation results of the low noise amplifier are shown in section 3.1.4. Finally, the discussion is given in section 3.1.5.

3.1.1 Regulated Cascode Active Inductor

An often-used way to produce an active inductor is to combine a gyrator and capacitor. The circuits proposed in Fig. 3.1 exploit the parasitic within the devices and the active inductors proposed can operate in the GHz range. In order to increase the quality factor Q, the Q-enhancement technology are proposed to increase the quality factor of the active inductor. The technique is used to exploit the regulated cascode technology, which reduces the inductor loss and increases the cascode gain. Based on the first small signal analysis, the equivalent RLC network of the inductor is shown in Fig. 3.2.

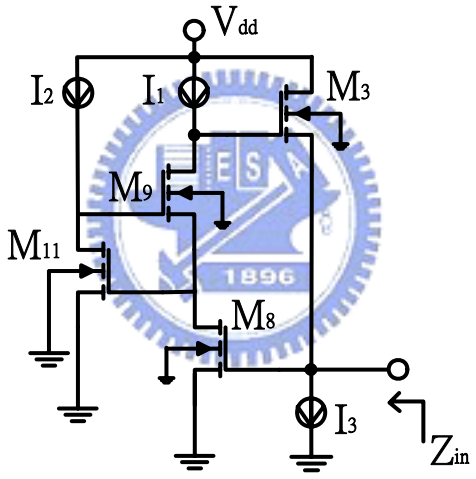


Fig. 3.1 Regulated cascode active inductor

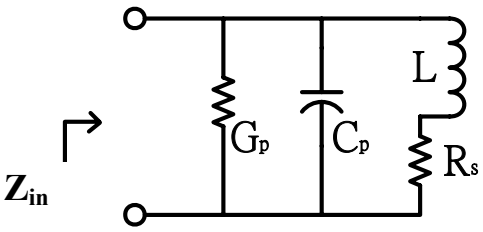


Fig. 3.2 Equivalent RLC model of active inductor

3.1.2 The Source Follower Negative Conductance Generator

A negative conductance generator is proposed to enhance the quality factors of the active inductor. A common drain stage combines with a common gate stage to generate the source follower negative conductance generator as depicted in Fig. 3.3. The main idea of this design is to generate an out-of-phase output current respected to the input current and feed it back to the applied input voltage at the same node, which is called the positive feedback configuration. Transistor M6 is a transistor providing transconductance gain g_{m6}. Transistor M5 forms a simple current mirror, providing the out-of-phase function and the voltage gain. Transistor M4 provides a required DC current through the negative conductance generator. Based on the combining configuration of M4 to M6, the equivalent negative conductance will be generated.

Assuming $g_{mi} >> g_{dsi}$ for all transistors and ignoring all non-dominant higher-order-terms, the conductance of the negative conductance generator can be expressed as:

$$-G_n = -\frac{g_{m5}g_{m6}}{g_{m5}+g_{m6}}$$

The idea of reducing the loss is to add a source follower negative conductance generator to the active inductor so that the loss of the active inductor can be compensated. The negative conductance generator produces the negative conductance $-G_n$ to connect in parallel with the active inductor. Thus the active inductor quality will be increased.

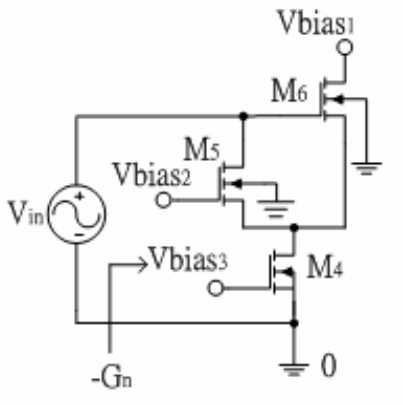


Fig. 3.3 The negative conductance generator

3.1.3 Low Noise Amplifier Design Methodology

A common gate CMOS low noise amplifier with a regulated cascode active inductor load and a source follower negative conductance generator will be presented in this section. In order to improve the power gain of the low noise amplifier, a large impedance of the load is required. Thus, the current running on the impedance should be minimized for obtaining a large impedance load, and the size of transistor can also be minimized. Moreover, the dimension of transistors should be increased to generate a large bias current for obtaining good linearity. Therefore, trade-offs between the power gain and linearity should be taken into account. An alternate configuration, combining with the regulated cascode active inductor and the source follower negative conductance generator are used to increase the impedance load. In other words, increasing the Q-value of the active inductor can obtain the large impedance load. In order to increase the Q-value, the loss of the active inductor should be reduced. The source follower negative conductance generator generates the negative conductance ($-G_n$) connected in parallel with the active inductor. The loss of the active inductor can be reduced.

Therefore, a low noise amplifier, which has the features of higher gain, smaller chip size, and lower power consumption, is proposed. The configuration of the proposed low noise

amplifier consisting with four signal-processing stages is illustrated in Fig. 3.4.

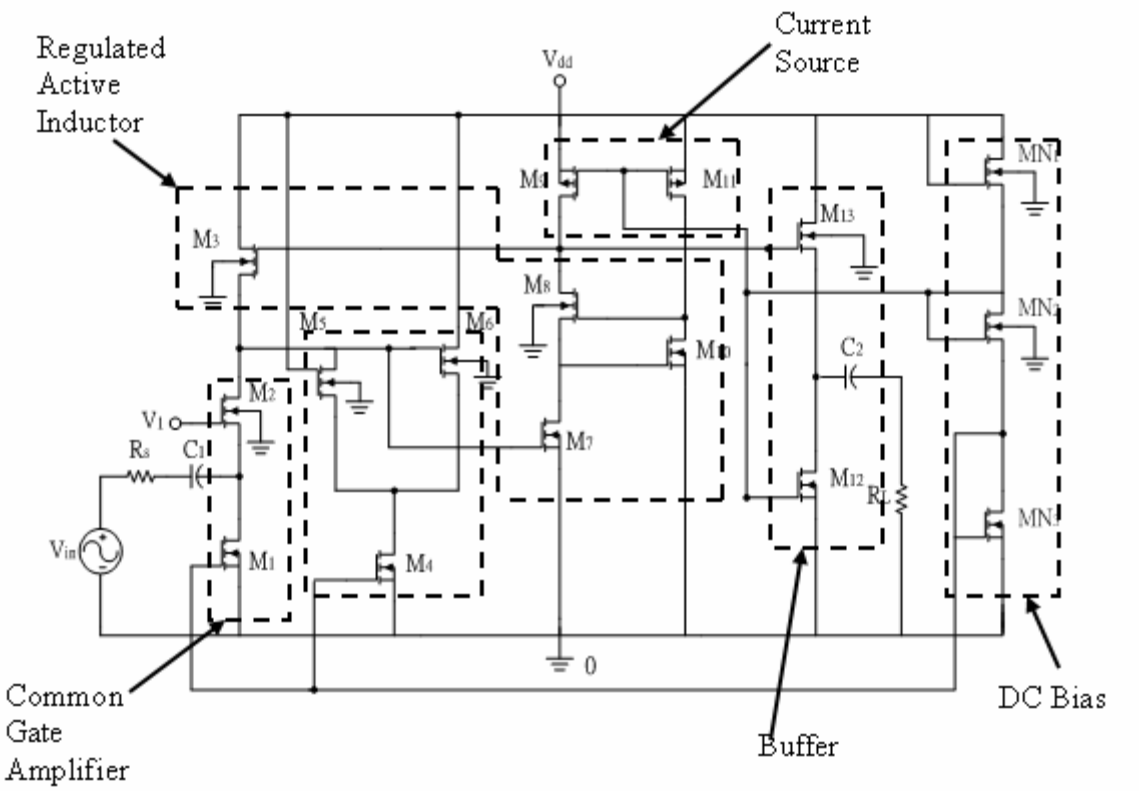


Fig. 3.4 The proposed low noise amplifier

In Fig. 3.4, the first stage, transistors M_1 and M_2 comprise the input amplifier stage. This common-gate configuration provides a simple 50-Ohm input impedance matching and higher linearity in contrast to a common-source configuration without source degeneration. This common-gate configuration also helps to increase the effective reverse isolation in heterodyne architectures due to the signal leakage of the local oscillator from the mixer to the antenna. The second stage, a regulated cascode active inductor is constructed by transistorsM_3, and M_7~M_{11}. The regulated cascode active inductor acts as the load of the low noise amplifier. The equivalent circuit model of the active inductor is shown in Fig. 3.2. The source follower negative conductance can help reduce the inductor loss of the regulated cascode active inductor and increase the Q-value of the active inductor. Transistors M_9 and

M_{11} are formed the active inductor constant current source. The third stage, a source follower negative conductance generator is constructed by transistors M_4~M_6. The main idea of this stage is to generate an out-of-phase current respected to the input current and feed it back to the input voltage at the same node called the negative conductance generator, which compensates the loss of the active inductor. Therefore, it is possible to improve the quality factor of the active inductor. The final stage, the output voltage buffer is built up by transistors M_{12} and M_{13}. A voltage buffer follows the designed amplifier in order to drive a 50-Ohm resistive load and it also requires a large drain current to drive a low resistance load. The transistors of M_{N1} to M_{N3} produce the bias voltage to provide the voltage the transistors M_1, M_4, M_9, M_{11}, and M_{12}. The capacitors of the C_1 and the C_2 are the dc coupling to block the dc voltage so that the external bias voltage will not affect the bias of the amplifier.

3.1.4 Simulation Results

The low noise amplifier was simulated by parameters from a standard CMOS 0.35-um digital process technology using HSPICE simulator. The normal supply voltage is 3.3V. Figs. 3.5, 3.6 and 3.7 show the simulation results of S21, S11, S12, S22, and noise figure where the amplifier is tuned around 2GHz. It can be seen that S21 is 17.6dB and S11, S22, and S12 are –11.2dB, -11.9dB, –39.4dB, and 5.05dB around 2GHz, respectively.

In RF amplifier, the conditions (necessary and sufficient) for unconditional stability are expressed in following:

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|D|^2}{2|S_{12}||S_{21}|} > 1, \text{ where } D = S_{11}S_{22} - S_{12}S_{21}$$

$$|S_{12}S_{21}| < 1-|S_{11}|^2$$

$$|S_{12}S_{21}| < 1 - |S_{22}|^2$$

From Fig. 3.5 and 3.6, at f = 2GHz, we find that K = 1.31 and D = $0.174 \angle 160^\circ$. Since K > 1 and |D| <1, the amplifier is unconditional stable. Furthermore, in the frequency range between 1.6GHz and 2.4GHz shows the K > 1 and |D| <1, the amplifier will be unconditional stable.

The 1dB compression and the IIP3 are -26dBm and -13dBm, respectively, and are shown in Fig. 3.8 and Fig. 3.9. From Fig. 3.8 and 3.8, the linearity of the proposed amplifier can achieve reasonable requirements. The layout of the low noise amplifier is shown in Fig. 3.10. From Fig. 3.10, the area of the proposed circuit is 108um×104um, which is smaller than that of the amplifiers use the passive spiral inductor of the previous work. Furthermore, the power consumption of the low noise amplifier is 21.4mW, which is smaller than that others design. A comparison between our design using the regulated cascode active inductor with the negative conductance generator of source follower configuration and other designs reported in the literature is presented in TABLE 3.1.

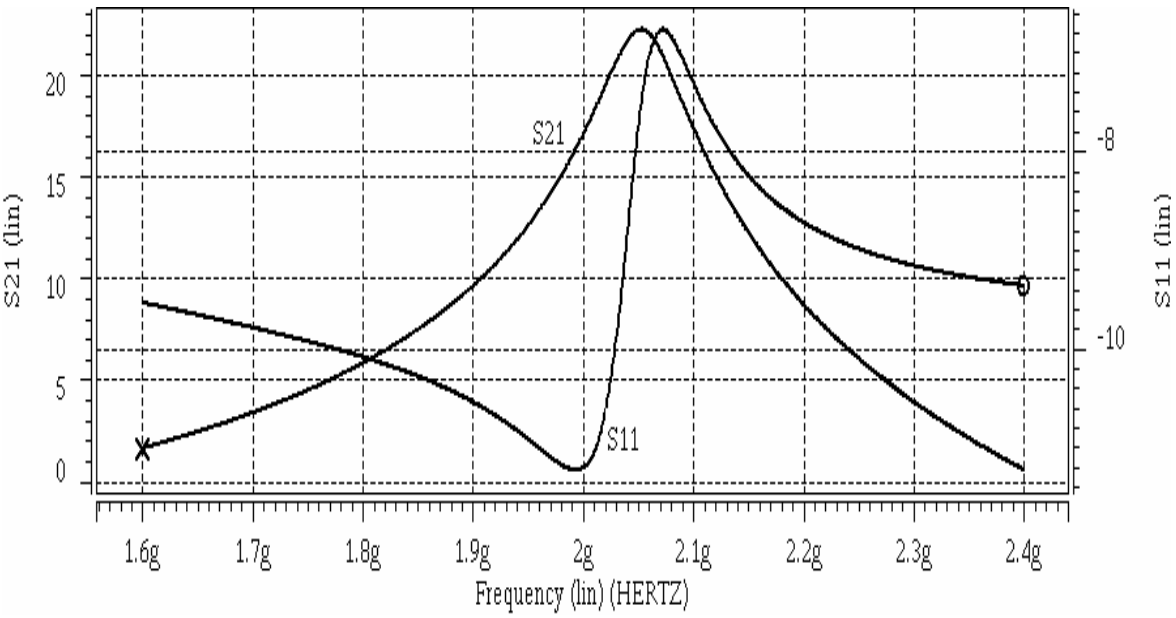


Fig. 3.5 S21 and S11 of the low noise amplifier

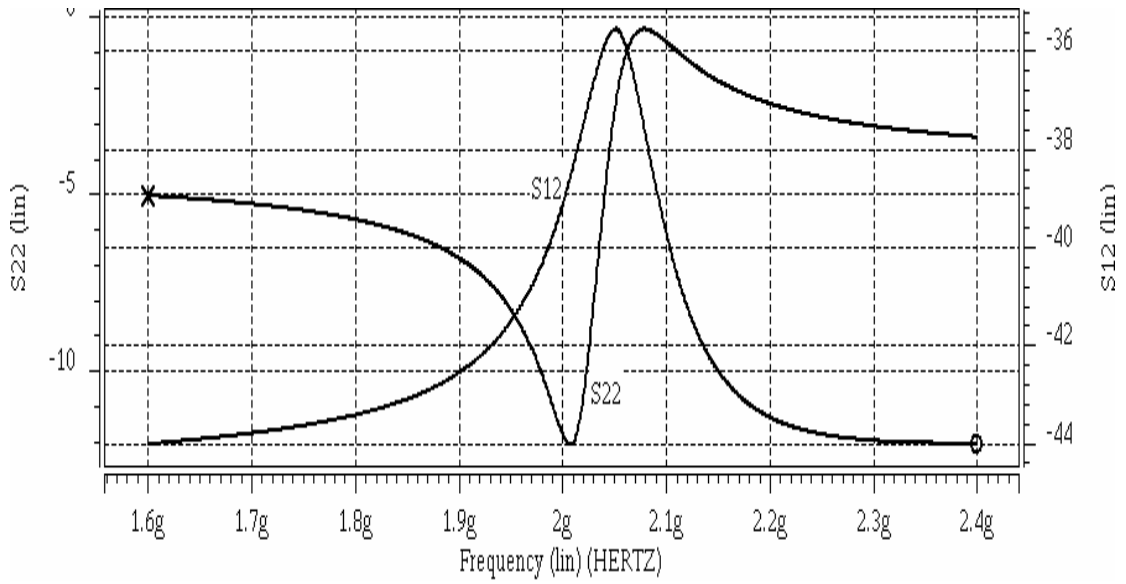


Fig. 3.6 S22 and S12 of the low noise amplifier

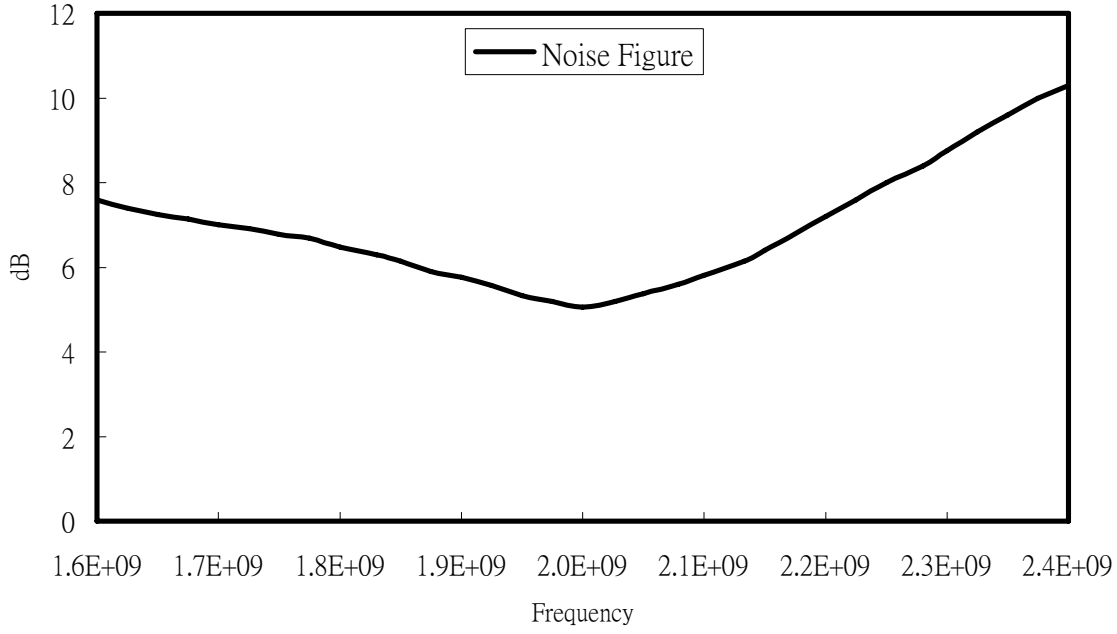


Fig. 3.7 Noise figure of the low noise amplifier

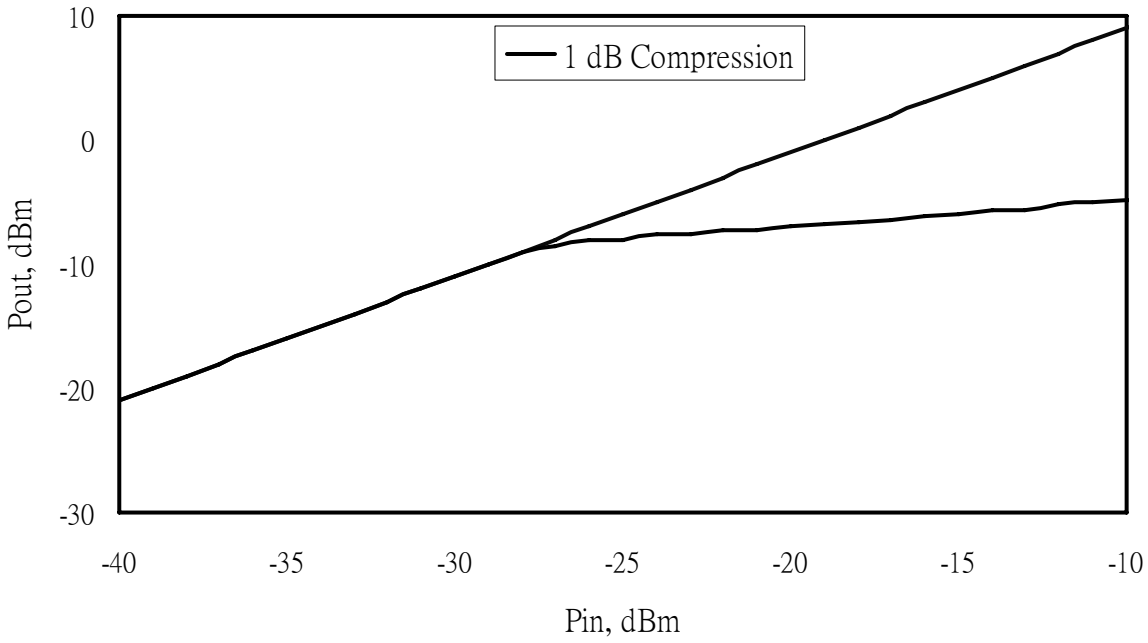


Fig. 3.8 1dB compression of the low noise amplifier

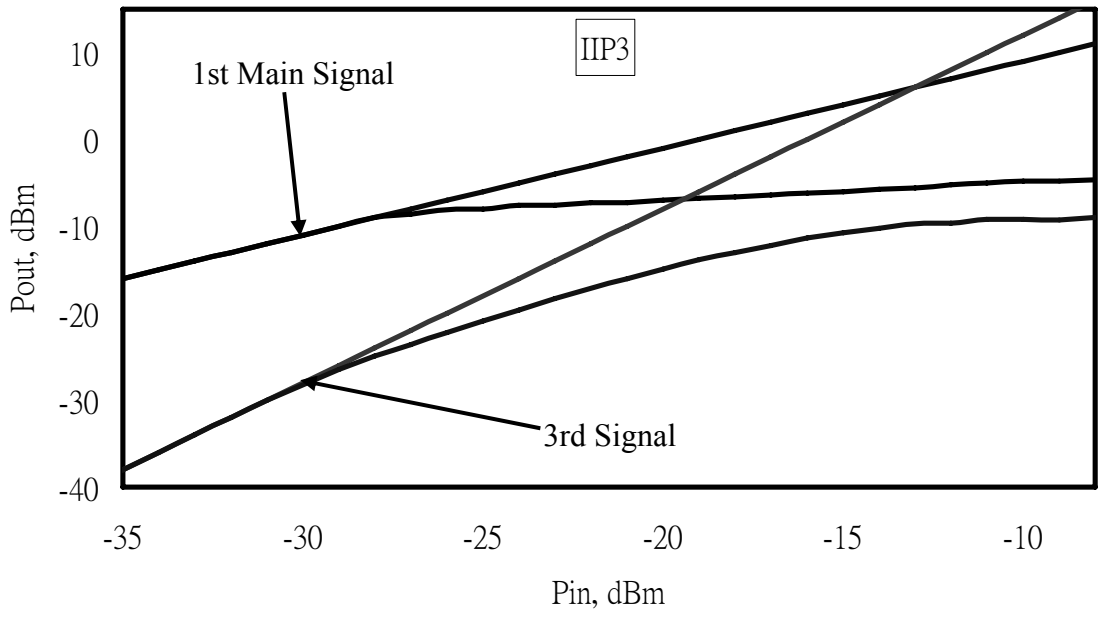


Fig. 3.9 IIP3 of the low noise amplifier

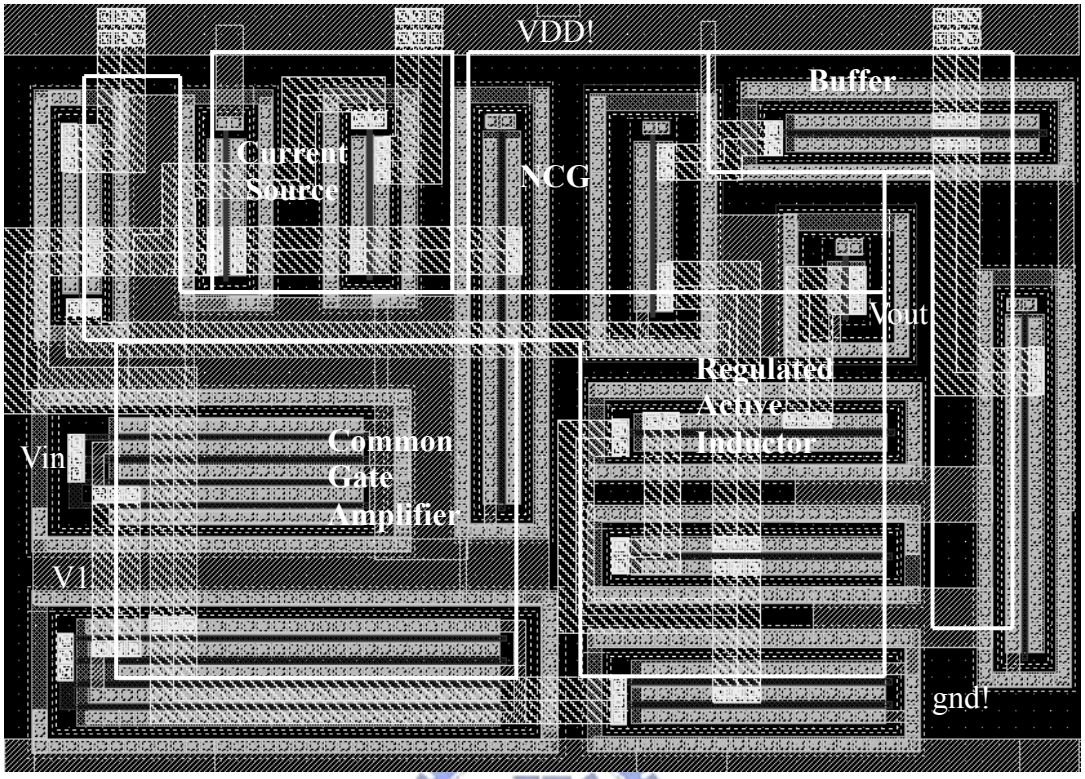


Fig. 3.10 Layout of the low noise amplifier

3.1.5 Discussion

This work presents the design of a CMOS low noise amplifier using the regulated cascade active inductor and the source follower negative conductance generator as the frequency selective element and the Q-enhancement. The proposed circuit is verified by HSPICE simulation and the results show that the center frequency and the power gain of the low noise amplifier are electronically tunable. The performance of the low noise amplifier is better than that of the integrated passive inductor. The achievement of this work is to reduce the size of the chip to 108um×104um.

TABLE 3.1 COMPARISONS OF 2 GHZ LOW NOISE AMPLIFIERS

	Karanicolas(20)	Texas A&M(32)	Thanachayanont(34)	This work
Technology	0.5um CMOS	0.5um CMOS	0.8um BiCMOS	0.35um
Gain (dB)	15.6	20.5	23	17.6
Frequency (Hz)	900M	1G	900M	2G
Power (mW)	20	14	50	21.4
1 dB (dBm)	NA	NA	-24.3	-26
IIP3 (dBm)	-3.2	-12.4	-27	-13
NF (dB)	2.8	3.65	4.3	5.05
Inductor	On chip spiral	Active	Active	Active
Area (mm^2)	0.28	0.08	NA	0.012

3.2 A 2.4GHz CMOS Low Noise Amplifier with High-Q Active Inductor Load

In this RF low noise amplifier, a double feedback cascode active inductor is used to design the amplifier. The double feedback cascode active inductor acts as the load of the low noise amplifier to obtain reasonable requirements. In this work, the cascode active inductor is introduced in section 3.2.1. In section 3.2.2, the double feedback technique is presented to improve the Q-value of the cascode active inductor. The design methodology of the low noise amplifier is given section 3.2.3. Simulation results of the low noise amplifier are shown in section 3.2.4. Finally, the discussion is given in section 3.2.5.

3.2.1 Cascode Active Inductor

An often-used way to produce active inductors is by combining a gyrator with two transconductors connected in back-to-back configuration and a capacitor. The cascode active inductor shown in Fig. 3.11 exploits the parasitic within the devices.

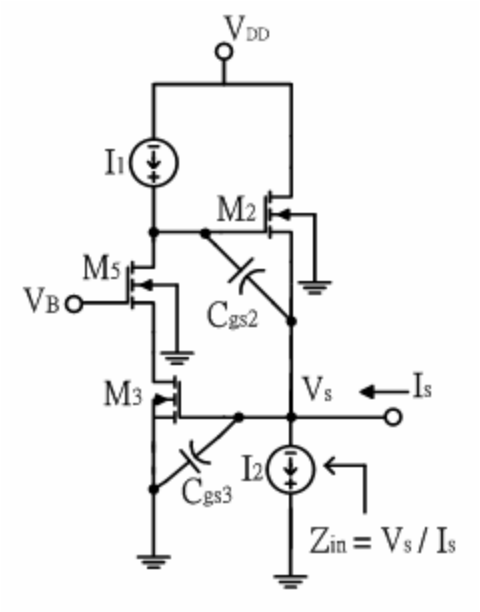


Fig. 3.11 The cascode active inductor

As shown in Fig. 3.11, transistor M_3 is used to convert the input voltage V_s, into a current for charging the integrating capacitor C_{gs3}, whereas M_2 is used to convert the voltage across C_{gs2} into an input current I_s. Base on a small signal analysis, the equivalent circuit for this inductor is also shown in Fig. 3.2.

Where,

$$R=\frac{1}{g_{m2}}$$

$$C=c_{gs3}$$

$$r_L=\frac{g_{ds3}g_{ds5}}{g_{m2}g_{m3}g_{m5}}$$

$$L=\frac{c_{gs2}}{g_{m2}g_{m3}}$$

In this configuration, the gain boosting is the utilization of negative feedback around the cascode common-source amplifier comprising of M_3 and I_1 to reduce the series resistive loss.

Hence, gain-boosting techniques have been applied to M_3 in order for increasing its voltage gain, $g_{ds3}g_{ds5}/g_{m3}g_{m5}$ for cascode configuration. However, referring to Fig. 3.2, the gain boosting technical operation does not affect the parallel resistive loss and its value left to be finite (about $1/g_{m2}$) so that an important characteristic on Q enhancement is limited. Intuitively, this effect arises from the existence of undesirable coupling path formed by c_{gs2} and c_{gs3}, which spoil the current, I_s, from M_2 and M_3 at high frequency. In order to diminish the parallel resistive loss, positive feedback has been placed around the first transconductor (M_3) in the active inductor for compensating the excessive currents in c_{gs2} and c_{gs3}.

3.2.2 Q-Enhancement Active Inductor

The Q-value of the cascode active inductor in Fig. 3.11 can be improved by removing the parallel resistive loss and series resistive loss. Thus the cascode common source configuration in Fig. 3.11 can be replaced with a pair cascode common source around the cascade common source as illustrated in Fig. 3.12.

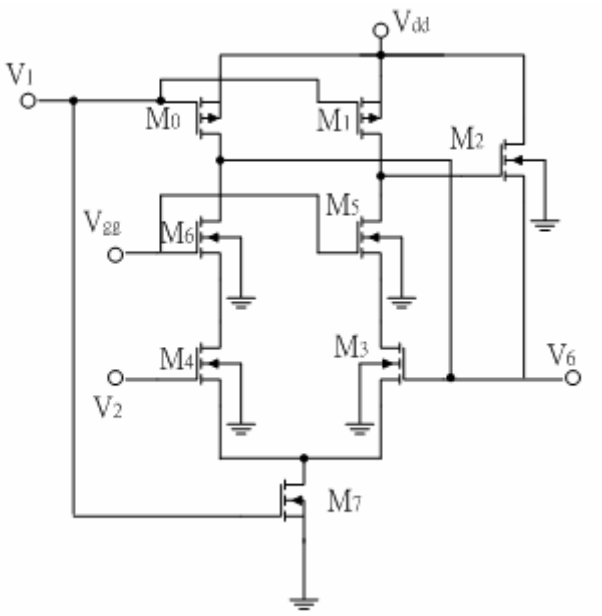


Fig. 3.12 Q enhancement active inductor

This operation of the high-Q active inductor uses positive feedback to compensate the undesirable coupling path formed by c_{gs2} and c_{gs3}, which spoil the input current, I_s, through M_2 and M_3 for reducing the parallel resistive loss and exploiting the gain boosting of cascade configuration for reducing the series resistive loss. According to the proposed topology in Fig. 3.12, transistors M_0, M_1 and M_7 comprise constant current source. The cascode active inductor consists of M_2, M_3 and M_5. Transistors M_4 and M_6 construct the positive feedback to compensate the parallel resistive loss. The currents in the undesirable coupling paths have been compensated. If there is an input voltage V_s, applied to the inductor, the current I_s, flowing through c_{gs2} and c_{gs3} are summed at the common source terminals of M_3 and M_4, which exhibit virtual ground potential. This current will then flow out of the drain terminal of M_6 and feedback to the input, because the current in c_{gs4} is negligible since the signal voltage across it is close to zero. As a result, the current in the undesirable coupling paths have been compensated hence the drain current of M_2 is equal to the input current and the inductor parallel resistive loss is now removed. Therefore, the Q-factor of the active inductor will be enhanced.

3.2.3 LNA Using Q Enhancement Active Inductor Design

A common gate configuration CMOS low noise amplifier using high-Q active inductor load is shown in Fig. 3.13. This circuit consists of three different stages. Transistors M_8 and M_9 comprise the input amplifier stage. This common-gate configuration provides a simple 50 Ω input matching and higher linearity without source degeneration. This common-gate approach also helps to increase the effective reverse isolation in heterodyne architecture due to the signal leakage arises from the local oscillator within the mixer to the antenna.

The high-Q active inductor is constructed by transistors M_2~M_6. It generates the load of the common gate configuration, the input stage. The key factor to obtain high circuit gain

is to increase the Q value of active inductor. Therefore, the high-Q active inductor uses positive feedback to compensate the parallel resistive loss and uses cascode configuration to improve the series resistive loss so that the Q factor of the active inductor is increased and the gain of low noise amplifier can be increased. Transistors M_{10} and M_{11} comprise the output buffer stage. This common drain configuration minimizes the loading effect and a simple 50 Ω output impedance matching. Transistors M_0, M_1 and M_7 comprise the constant current source. This current source provides the constant current, which tunes the Q factor and inductance of the high-Q active inductor. This LNA is sensitive to the parasitic capacitance, and any following stage loading. This will be modified the overall circuit response by tuning the biases of V_1, V_2, V_3 and V_{gg}. Therefore, it is easily to tune the variation due to the process and other factors. Capacitors C_1 and C_2 are used as a DC blocking capacitor of the input and output to isolate DC voltage of the previous stage and the following stages.

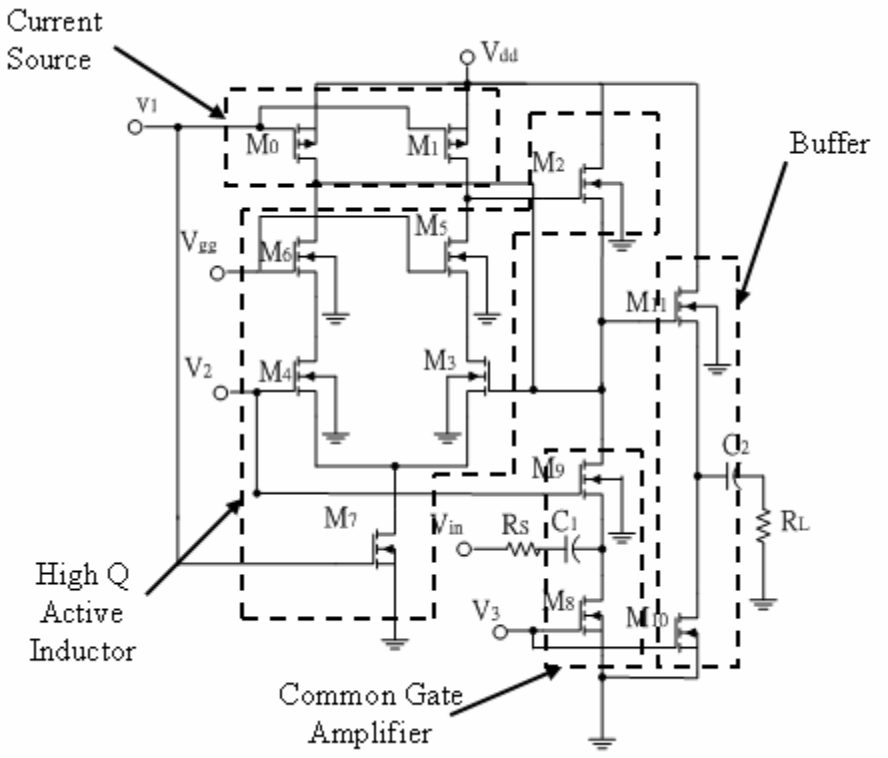


Fig. 3.13 LNA using Q enhancement active inductor

3.2.4 Simulation Results

The low noise amplifier was simulated with parameters from a standard CMOS 0.35-um digital process technology using HSPICE simulator. According to the circuit Fig. 3.13, the used transistors width and capacitors are shown in Fig. 3.14 and the minimum lengths of 0.35um. The biasing values are shown as the following: V_1=2V, V_2=1V, V_3=1.5V, V_{gg}=2.3V and the normal supply voltage is 3.3V. Figs. 3.15, 3.16, and 3.17 show the simulated results of S21, S11, S12, S22, and noise figure when the amplifier is tuned around 2.4GHz. It can be seen that S21 is 21dB and S11, S22, S12, and noise figure are –21dB, -38.8dB, –37.6dB, and 4.4dB, respectively.

PARAMETERS	VALUE
$(W/L)_{M0, M1, M7}$	10u
$(W/L)_{M3, M4, M8}$	80u
$(W/L)_{M5, M6}$	25u
$(W/L)_{M2}$	60u
$(W/L)_{M9}$	88u
$(W/L)_{M10}$	20u
$(W/L)_{M11}$	18u
C1, C2	5pF

Fig. 3.14 Component values and device dimensions

In RF amplifier, the conditions (necessary and sufficient) for unconditional stability are expressed in following:

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|D|^2}{2|S_{12}||S_{21}|} > 1, \text{ where } D = S_{11}S_{22} - S_{12}S_{21}$$

$$|S_{12}S_{21}| < 1-|S_{11}|^2$$

$$|S_{12}S_{21}| < 1 - |S_{22}|^2$$

From Fig. 3.15 and 3.16, at f = 2.4GHz, we find that K = 1.535 and D = $0.226 \angle 121^\circ$. Since K > 1 and |D| <1, the amplifier is unconditional stable. Furthermore, in the frequency range between 2GHz and 2.8GHz shows the K > 1 and |D| <1, the amplifier will be unconditional stable.

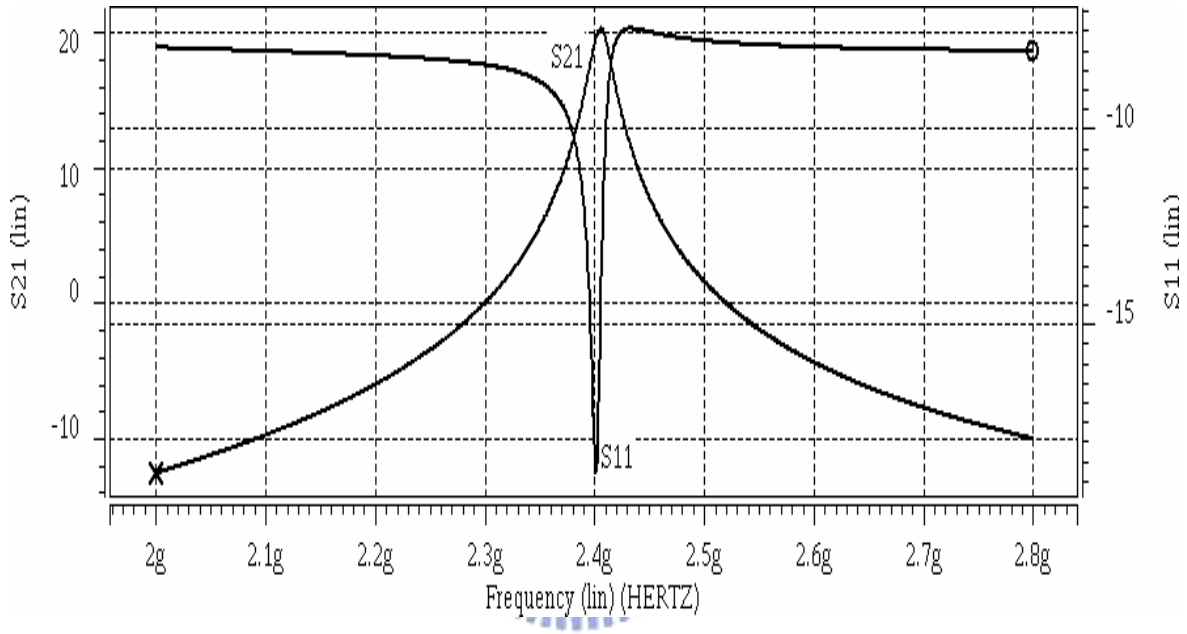


Fig. 3.15 S21 and S11 of the proposed amplifier

For the linearity, the 1dB compression and the IIP3 are -28dBm and -12dBm, respectively, and shown in Fig. 3.18 and Fig. 3.19. The layout of the low noise amplifier is shown in Fig. 3.20. The chip layout plays an important role in the high frequency circuits design. The unsuitable circuit layout may drastically degrade the circuit performance due to the increasing inductor or coupled noise. To obtain the desire performance, all interconnections are made by metal layer to minimize parasitic resistance and all active devices are surrounded by guard ring to minimize the substrate noise and reduce the coupling among the devices. The size of the proposed circuit is 56.8um×56um, and is smaller than that

using the passive component. The power consumption of the low noise amplifier is 17.8mW. A comparison between our low noise amplifier design using the high-Q cascode active inductor load and other designs reported in the literature is presented in TABLE 3.2.

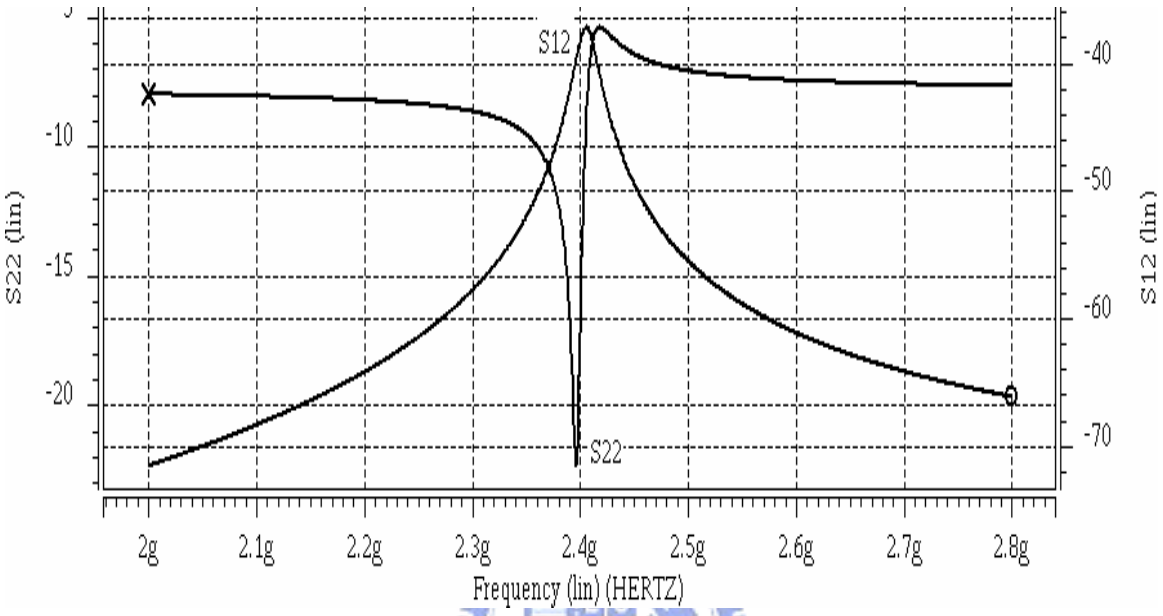


Fig. 3.16 S22 and S12 of the proposed amplifier

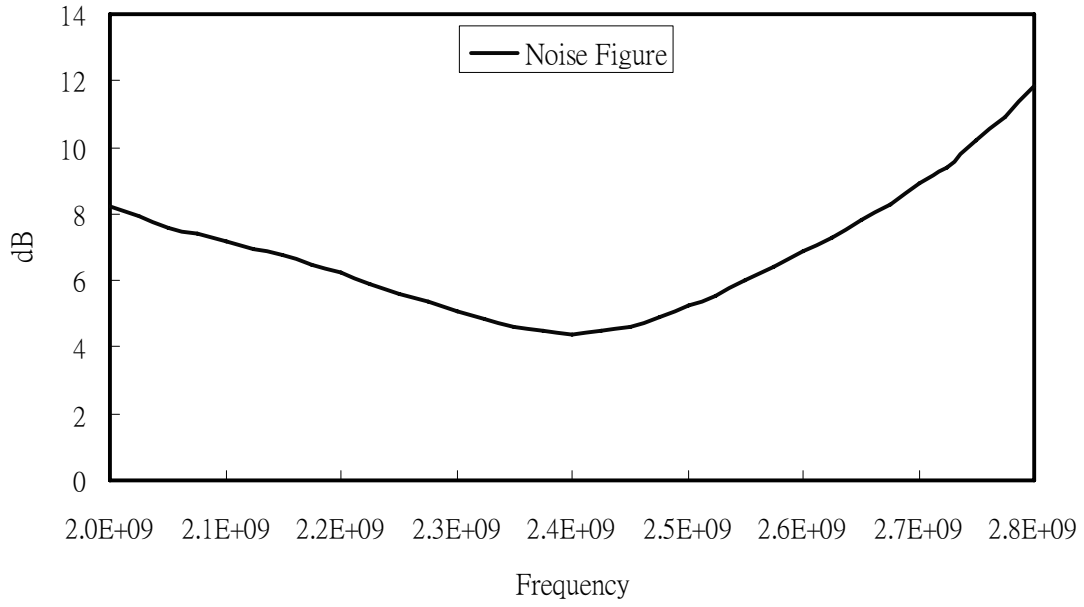


Fig. 3.17 Noise figure of the proposed amplifier

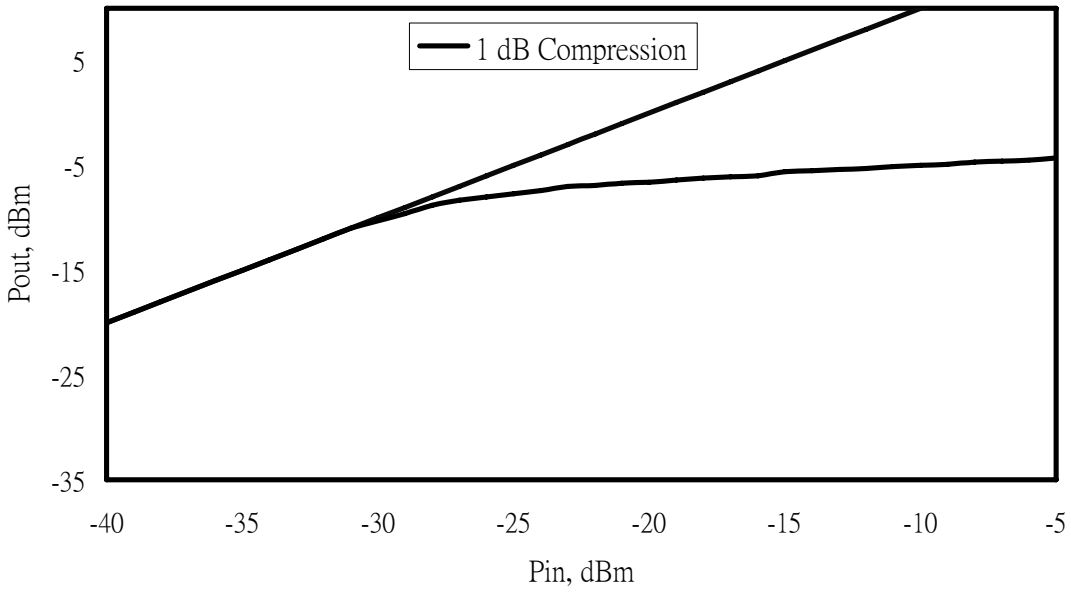


Fig. 3.18 1dB compression of the proposed amplifier

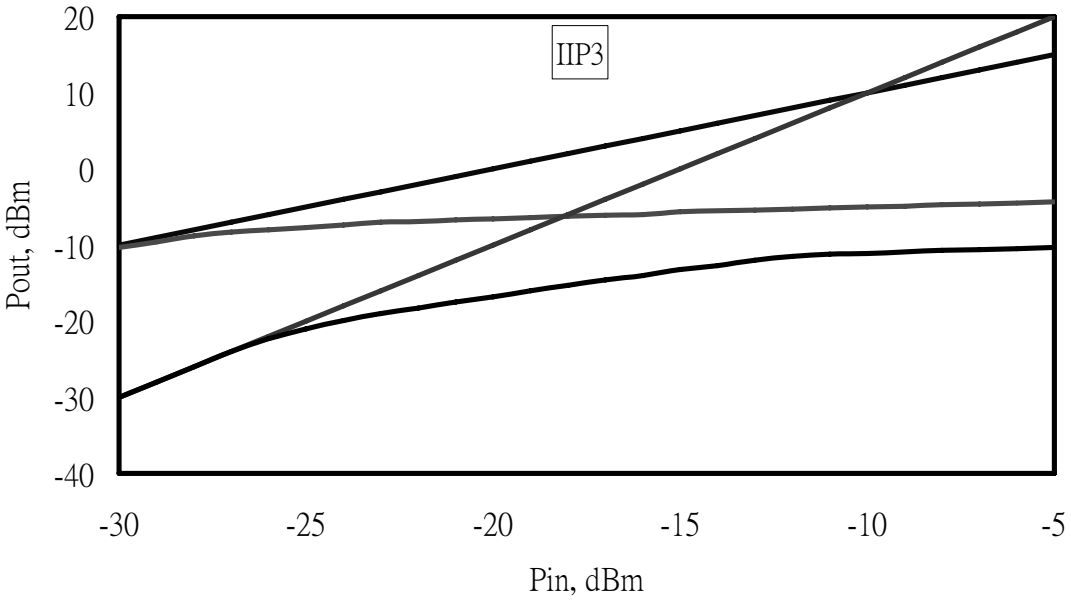


Fig. 3.19 IIP3 of the proposed amplifier

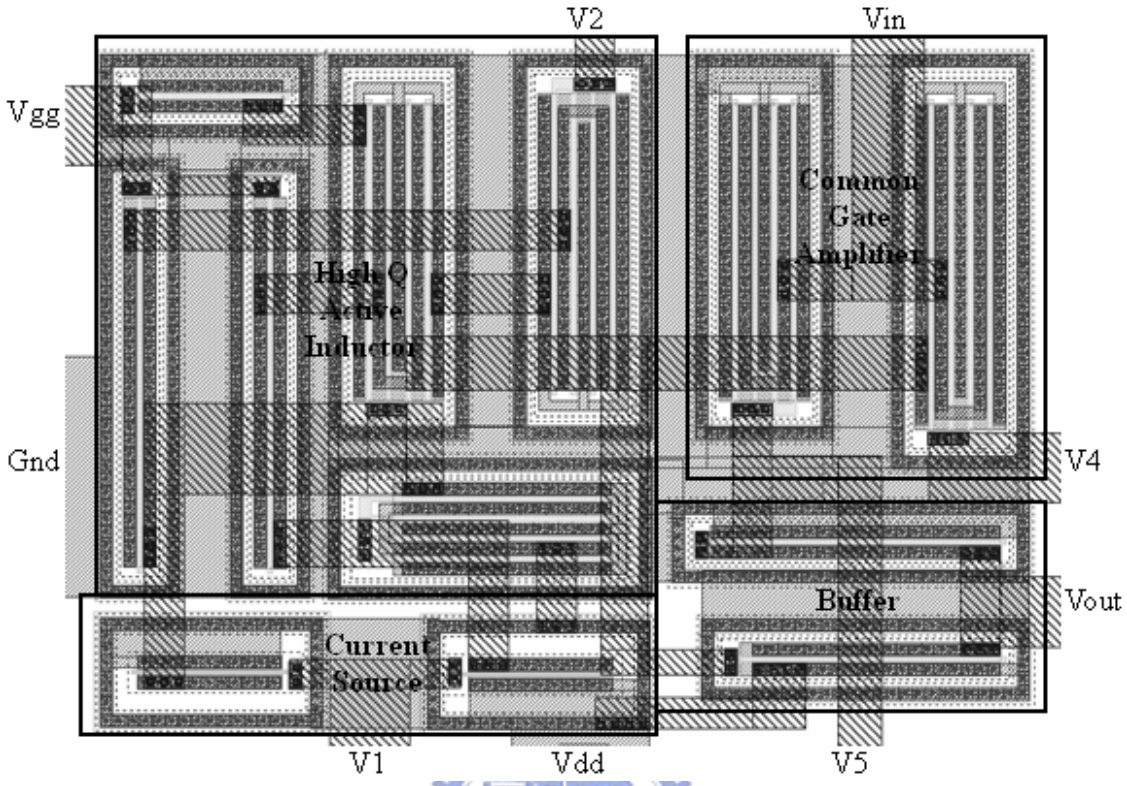


Fig. 3.20 Layout of the proposed amplifier

3.2.5 Discussion

This work presents the design of a CMOS low noise amplifier using a high-Q active inductor load as a frequency selective element. The proposed circuit was verified by HSPICE simulation and the results show that the center frequency and Q-factor of the low noise amplifier are electronically tunable. The performance, power gain and matching of the low noise amplifier are better than those employed integrated passive inductor and other active inductor. The achievement of this work is to reduce the size of the chip.

TABLE 3.2 COMPARISON OF 2.4GHZ LOW NOISE AMPLIFIER

	Karanicolas(30)	Texas A&M(32)	Thanachayanont(34)	This work
Technology	0.5um CMOS	0.5um CMOS	0.8um BiCMOS	0.35um CMOS
Gain (dB)	15.6	20.5	23	21.4
Frequency (Hz)	900M	1G	900M	2.4G
Power (mW)	20	14	50	17.8
1 dB (dBm)	NA	NA	-24.3	-28
IIP3 (dBm)	-3.2	-12.4	-27	-12
NF (dB)	2.8	3.65	4.3	4.4
Inductor	On chip spiral	Active	Active	Active
Area (mm^2)	0.28	0.08	NA	0.03

3.3 Summary

In this chapter, the various RF amplifiers are presented. The amplifier designs are obtained by combining the active inductor and negative conductance generator to operate in different frequency band. Exploring the negative conductance generator can compensate the loss of the active inductor, and then the Q-value of the inductor is increased. The increasing Q-value of the active can improve the characteristics of the RF amplifiers. Using the external bias voltage can change the characteristics of the active inductor, the negative conductance, and the RF amplifiers. All works are simulated with parameters from a standard CMOS 0.35-um digital process technology using HSPICE. The simulation results show that the performance of the RF amplifiers can achieve better performance than that of the previous literatures, which were implemented based on the planar spiral inductor. In addition, the size of the RF amplifiers, which use the active inductor, is smaller than that using the planar spiral inductor. Therefore, applying an active inductor in RF circuit is an alternative approach to obtain the characteristics of a smaller size, electric tunable, high Q-value etc. Although, applying a negative conductance generator can compensate the loss of the active inductor, the complexity of the active inductor circuit is significantly increased. Therefore, it is possible

that a simple technique is proposed to improve the loss compensation and obtain a simple configuration of the active inductor.

Chapter 4

Designs of Improving CMOS Active Inductors

In a RF CMOS active inductor, internal losses always exist in some components such as the conductance between drain and source of a MOSFET, in the parasitic capacitance, and in the DC bias circuits. These elements result in series, parallel, and parasitic capacitance losses in active inductors. Therefore, quality factor (Q), inductance (L), and operating frequency are limited [38, 39]. A gain-boosting technique had been employed to reduce the loss and hence to enhance Q [34]. In this technique, the series loss was reduced only around 100 at 1GHz, but the maximum Q value was not obviously promoted. A Q-enhancing approach based on the double-feedback compensation has also been proposed [38]. This technique is developed to reduce the parallel loss, and hence the maximum Q value approximates 12,000 at 1GHz. Furthermore, current-reused and negative conductance generator techniques were adopted to improve the optimally expected Q value of active inductor [39]. Though the internal loss is compensated, both circuit complexity and power consumption are increasing.

In this chapter, the designs for improving active inductors are presented. We carry out a design of active inductor using different loss compensation techniques to improve the

performance of the active inductors. The improved active inductors are verified that the performance can be improved by applying the mathematic analysis, the simulation results, and the measurement results.

The organization of this chapter is as the following. In section 4.1, an improving active inductor using a cascode RC feedback compensation technique is presented. In section 4.2, an improving active inductor using gain-boosting and current-reused techniques is described. An improving active inductor using a capacitor is depicted in section 4.3. An improving active inductor using a resistor is expressed in section 4.4. Finally, a brief summary is made in section 4.5.

4.1 An Improved Active Inductor Using a Cascode RC Feedback Compensation Technique

In RF CMOS active inductor applications, losses limit the Q-value, the inductance and the operating frequency. A conventional Q-enhancement active inductor circuit required a circuit to compensate these internal losses. In the Q-enhancement design, compensation circuits are constructed with active devices. The complexity, the power consumption, and the noise figure of the active inductor are increasing.

Figure 4.1 shows an active inductor based on CMOS generalized impedance converter (GIC) proposed in [33], where the inductor loss was reduced by cascode technique of enhancement DC gain [34]. Nevertheless, the Q-value, the inductance, and the operating frequency of this active inductor are seriously degraded when CMOS current source devices replace the ideal current sources. This is caused by the conductance of the MOSFET used in CMOS current sources.

In this work, we propose a novel CMOS high Q-value RF active inductor by a simple

cascode RC feedback loss compensation circuit to overcome the loss caused by the active devices. The improved circuit design of the active inductor is described in section 4.1.1. The simulation results and the layout of the active inductor are expressed in section 4.1.2. The measured results are displayed in section 4.1.3. Finally, the discussion is given in section 4.1.4.

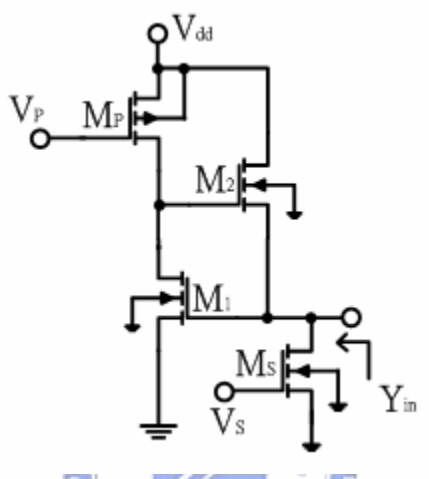


Fig. 4.1 The simple active inductor

4.1.1 Circuit Design

Including the current source, the equivalent input conductance (Y_{in}) of the general impedance converter (GIC) circuit shown in Fig. 4.1 is derived as below.

$$Y_{in} \approx \left[\frac{s(C_{gs2}+C_{gd1}+C_{gd2})+g_{ds1}+g_{dsp}}{(sC_{gd2}+g_{dsp}+g_{ds1}+g_{mp})(s(C_{gs2}+C_{gd1})+g_{m2})}\right]^{-1} \quad (C_{gd} << C_{gs}) \qquad (4.1)$$

$$\approx g_{ds1}+g_{dsp}+g_{mp}+sC_{gs1}+\frac{g_{m1}g_{m2}}{sC_{gs2}+g_{ds1}}$$

From Eq. (4.1), the conductance loss of g_{ds1}, g_{dsp}, and g_{mp} can significantly reduce the performance of the active inductor. In order to improve the performance of the active

inductor, the conductance loss of g_{dsp} and g_{ds1} should be reduced. Fig. 4.2 shows the proposed CMOS active inductor circuit, which is based on the CMOS GIC circuit design in [33].

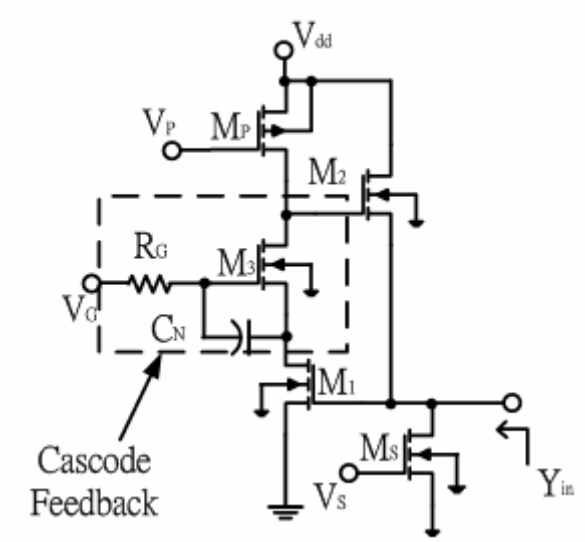


Fig. 4.2 The proposed active inductor circuit

In Fig. 4.2 the feedback RC network is designed for compensating the conductance loss caused by CMOS current source implementation. Capacitor C_N, resistor R_G, and transistor M_3 construct a RC feedback cascode compensation circuit. The RC feedback network operation includes negative feedback and positive feedback. The M_1, M_2 and M_3 components construct the negative feedback operation path for converting the input voltage back to the input current. This mechanism realizes input impedance of the active inductor, in which the transistor M_3 is used for reducing the output conductance of M_1 in cascode configuration [34]. Therefore, the loss of g_{ds1} can be reduced. Nevertheless, loss of the g_{dsp}, caused by current source cannot be reduced. In order to reduce the loss of g_{dsp}, the positive feedback can be exploited. The positive feedback path is passed through M_1, C_N, R_G, M_3 and M_2. The C_N, R_G and M_3 are organized to build up a common source configuration in the positive feedback

path for achieving negative conductance and for compensating the loss of current source, g_{dsp}. The negative conductance is generated by C_N, R_G and M_3 and is interacting with M_1 and M_2. Based on the assumption of $\omega << g_{m3}/(C_{gs3} - C_N)$, the negative conductance (G_N) can be derived as

$$-G_N \approx -\frac{(g_{m1}g_{m3}/g_{dsp})+g_{m3}-SC_N}{g_{m3}-SC_N}g_{m2} = -g_{m2} + \frac{1}{\frac{sC_N g_{dsp}}{g_{m1}g_{m2}g_{m3}} - \frac{g_{dsp}}{g_{m1}g_{m2}}} \qquad (4.2)$$

From Eq. (4.2), the input negative conductance ($-G_N$) is produced using positive feedback circuit. The negative conductance parallels with the active inductor. The equivalent circuit of active inductor is shown in Fig. 4.3. The total loss of active inductor can be reduced by the negative conductance. Therefore, if the circuit components and biases are properly chosen, the Q-value, inductance L, and operating frequency can be improved.

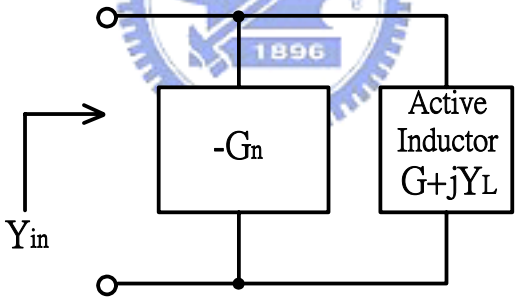


Fig. 4.3 The equivalent circuit of loss compensation

4.1.2 Simulation Results

All simulations are implemented via Agilent-ADS simulator and the active inductor circuit is produced by TSMC 0.25um CMOS process and biased at 2.5V. All transistors have the same dimensions and the length and width of each MOSFET are 0.24um and 40um respectively. The RC feedback circuit is designed to have R_G=650Ω and C_N=0.7PF. The

scattering parameter S11 performance of the active inductor is shown in Fig. 4.4. It can be seen that the curve is inclined to the outside of circle between 1.2GHz and 2GHz and this result also indicates that the loss is decreased. Thus the Q-value is improved.

The inductance, the equivalent loss, and the Q-value of the inductor are shown in Figs. 4.5, 4.6, and 4.7 respectively. It can be seen that in the range of 1.2GHz to 2GHz, the inductance value changing is very small. When ranging from 3.5nH to 4.5nH, the inductance's minimum equivalent loss is about 3E-5Ω and maximum Q-value is about 1.2E6. The power consumption is only about 4.3mW under 2.5 V supply voltage. The layout of the improved active inductor is shown in Fig. 4.8. The comparisons of the characteristics between the original active inductor and the proposed active inductor are shown in TABLE 4.1.

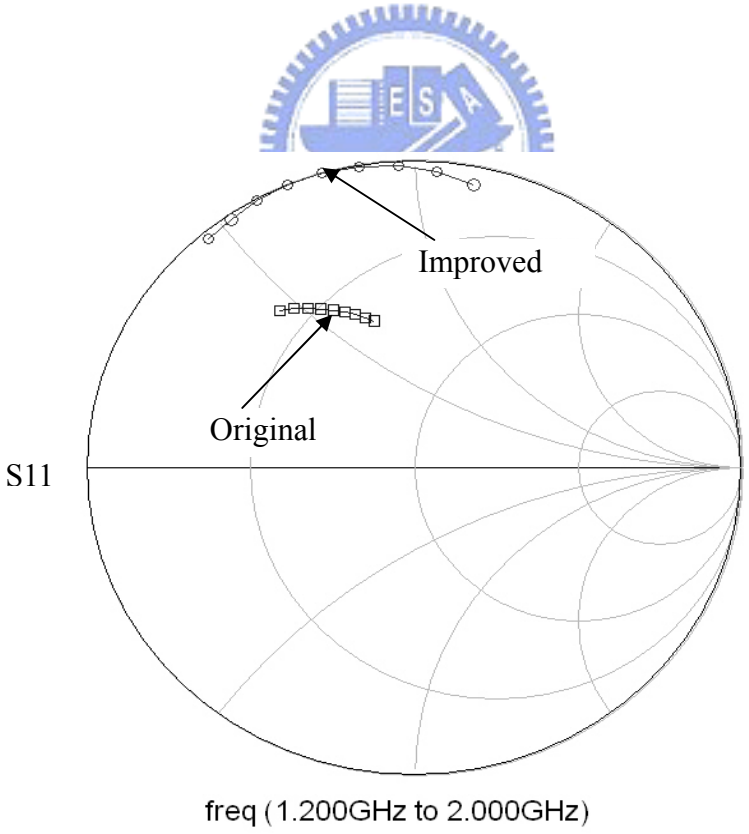


Fig. 4.4 S11 of the proposed active inductor circuit

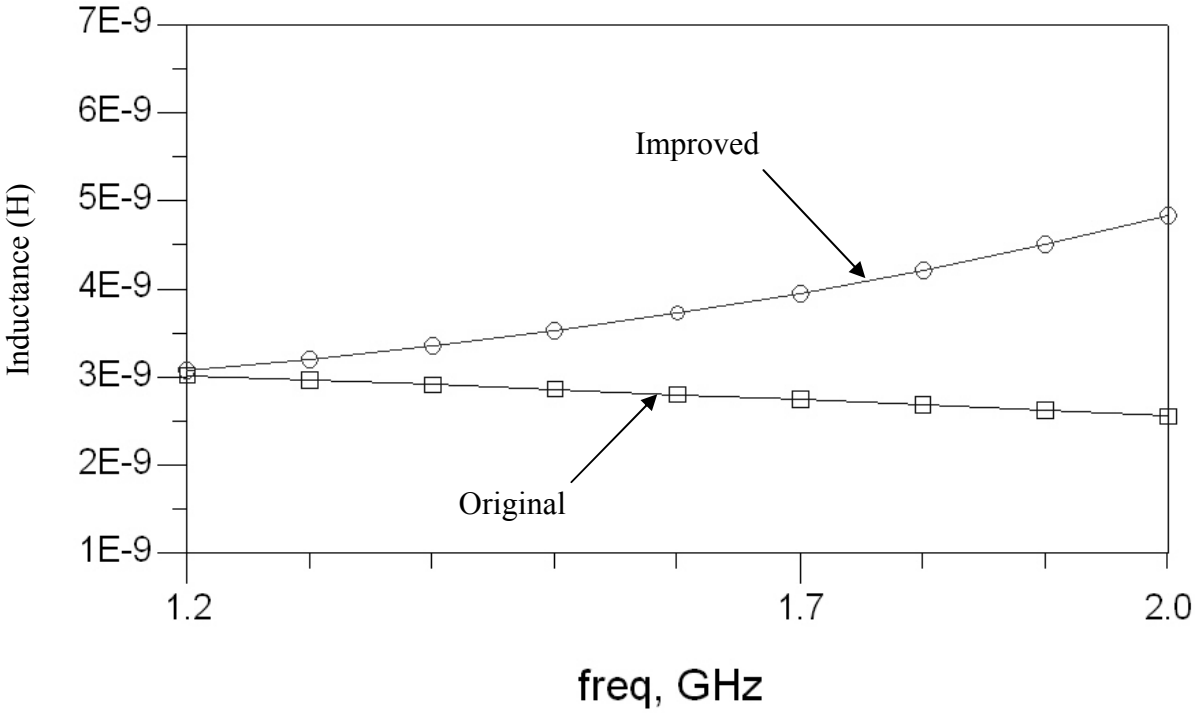


Fig. 4.5 Inductance of the proposed active inductor circuit

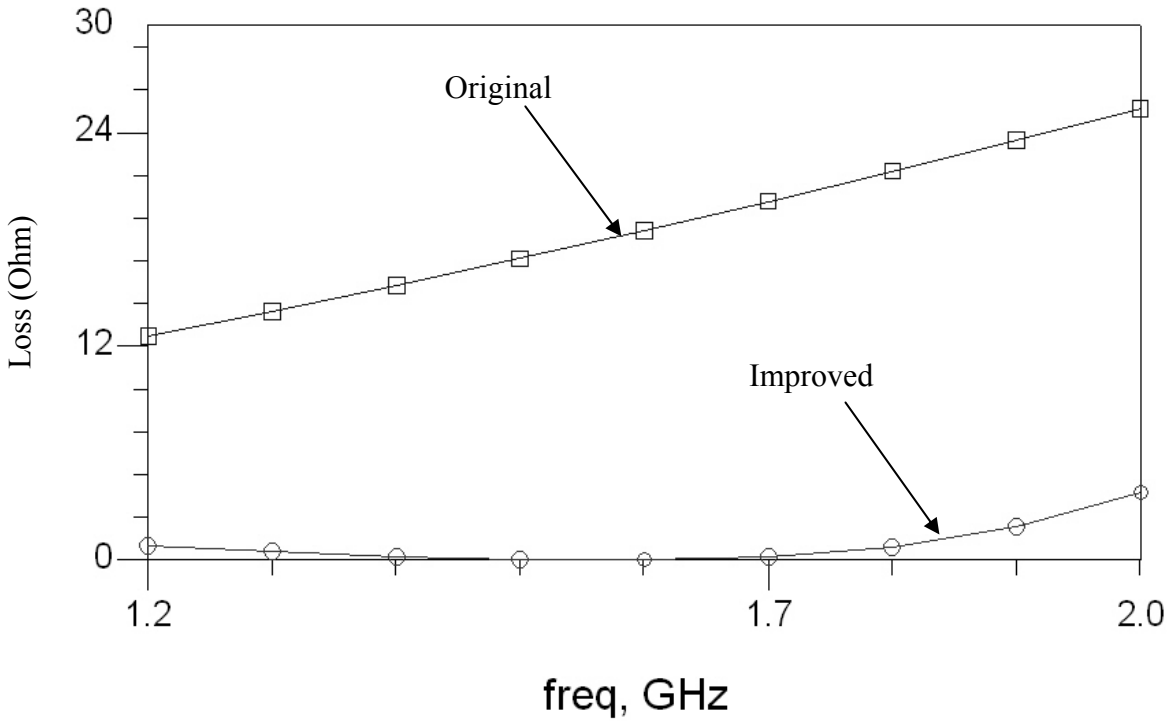


Fig. 4.6 Equivalent loss of the proposed active inductor circuit

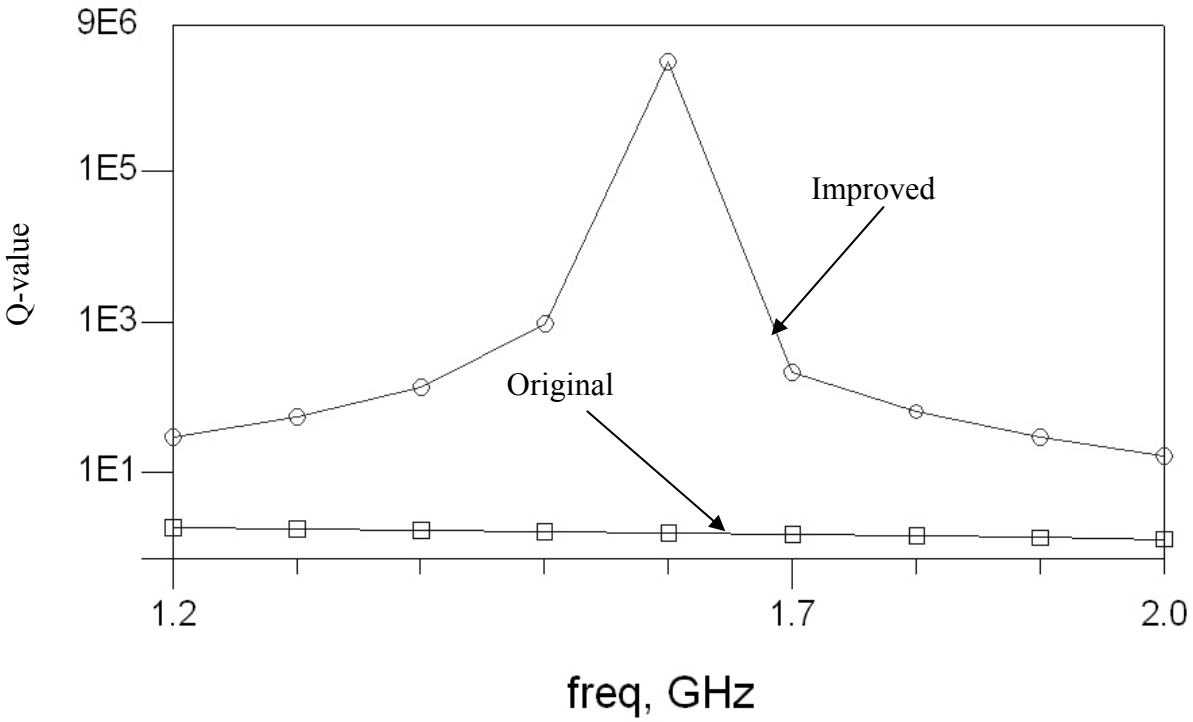


Fig. 4.7 Q-value of the proposed active inductor circuit

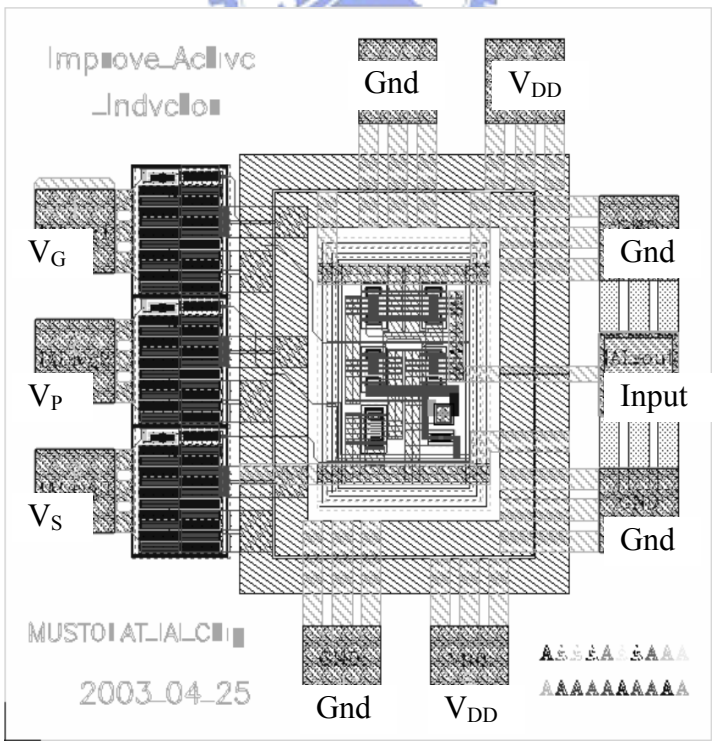


Fig. 4.8 Layout of the proposed active inductor circuit

TABLE 4.1 COMPARISONS BETWEEN IMPROVED AND ORIGINAL @ 1.6GHZ

	Improved	Original
Q	1.2E6	3
Loss (Ω)	3E-5	17
Inductance (nH)	3.6	2.7
Power Consumption (mW)	4.3	4.5

4.1.3 Measurement Results

The proposed active inductor is fabricated by using TSMC 0.25um CMOS process. The photo-die and the bonding on the PCB of the proposed active inductor circuit are displayed in Fig. 4.9 and Fig. 4.10. In CIC, a network analyzer, a probe station, and a Tek P6217 probe carried out the measured S-parameter and this measure demonstrates the same trend as the simulated results. According to the measure results, the improved quality-factor can be easily obtained from the S-parameter. Fig. 4.11 shows the S-parameter of the simulated, the measured, and the original results. The improved performance can be obtained by adding the RC feedback compensated network.

The comparisons of the inductance, the equivalent loss, and the Q-value in the simulated result, the measured result, and the original result are shown in Figs. 4.12, 4.13, and 4.14 respectively. The supplied voltage VDD of this active inductor is 2.5 V with a 2.1mA dc current, and the total power consumption is 5.25mW. The maximum Q-value is about 1.1E5 at 1.6 GHz with a 3.2nH inductance. The comparisons between simulation and measurement at 1.6GHz are shown in TABLE 4.2. The additional parasitic effects, such as the resistance and the capacitance, cause the measured results of the inductance and the Q-value to be smaller than those of the simulation results in realistic fabrication. From the curve of the Smith chart, it is slightly inward than that of simulated curve and the loss is imperceptible increased.

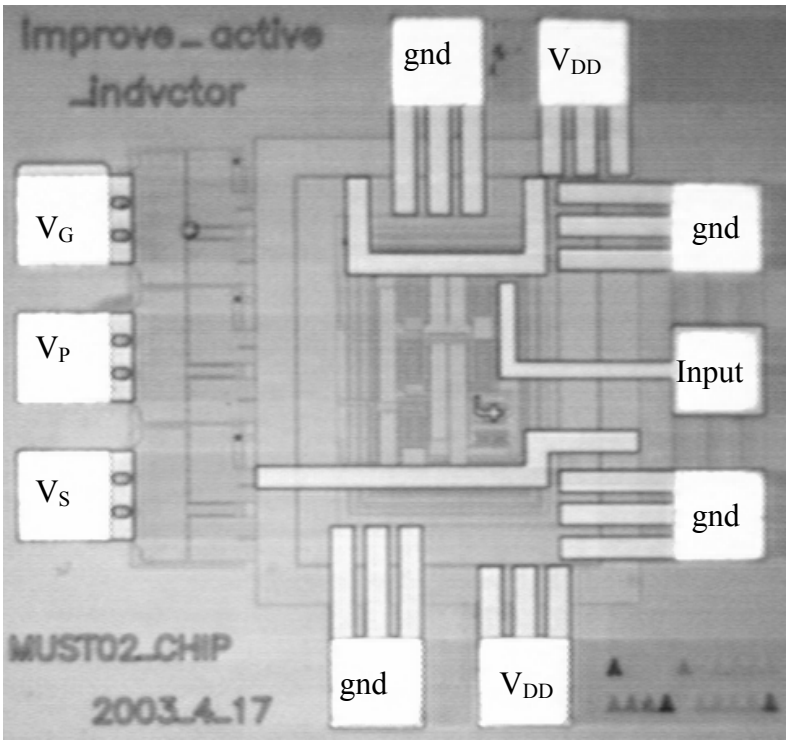


Fig. 4.9 Photo-die of the proposed active inductor circuit

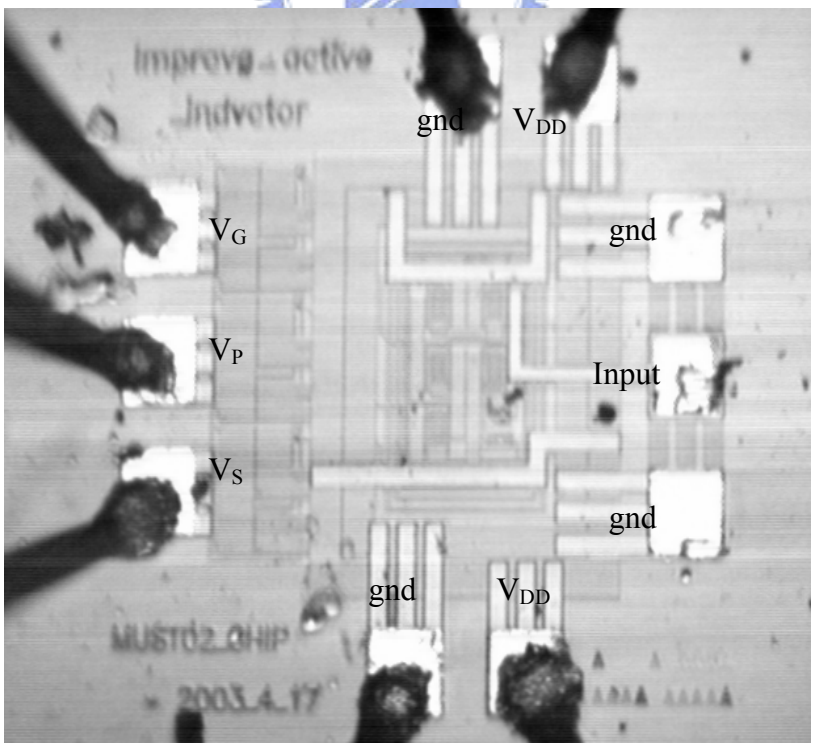


Fig. 4.10 (a) Bonding to PCB of the proposed active inductor circuit

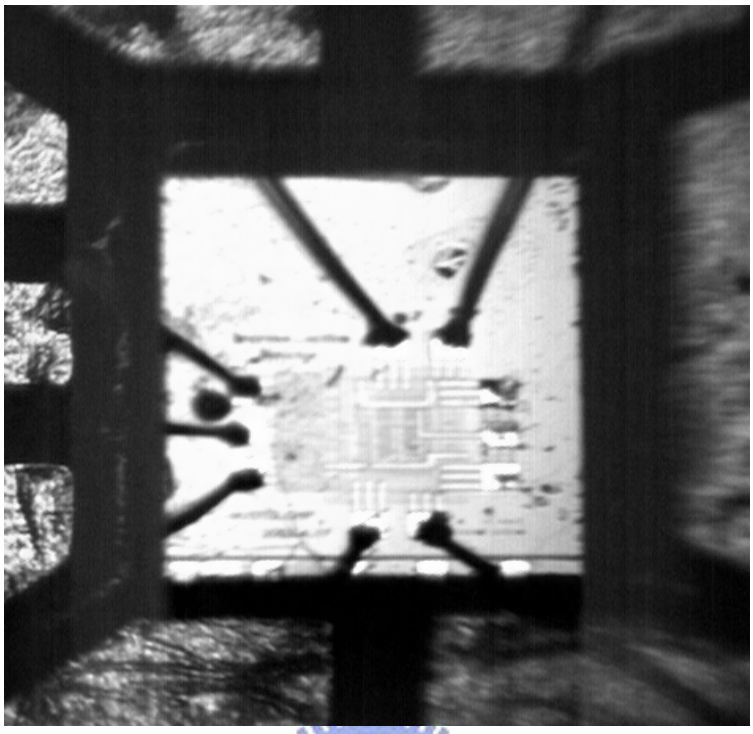


Fig. 4.10 (b) Bonding to PCB of the proposed active inductor circuit

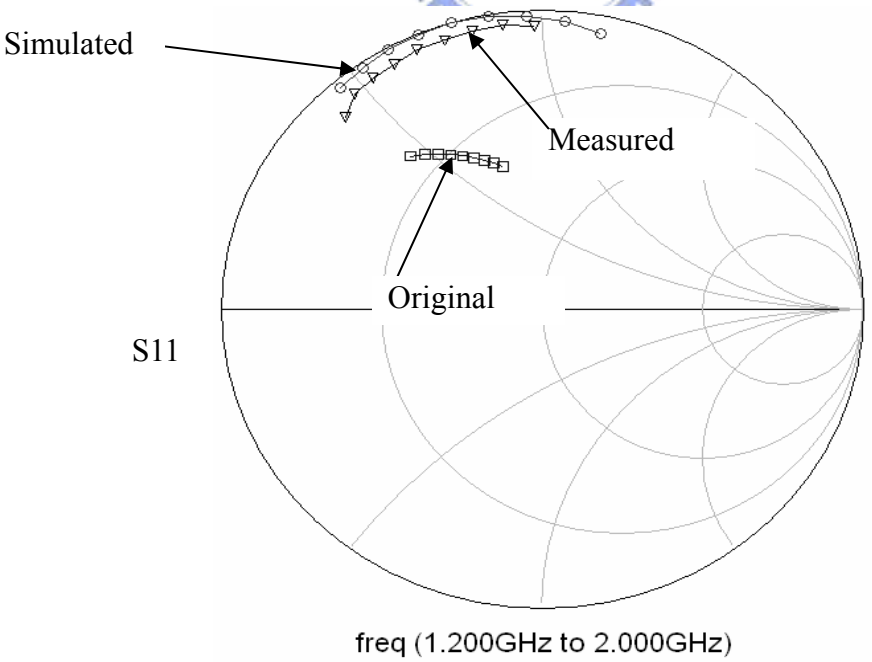


Fig. 4.11 S11 measurement of the proposed active inductor circuit

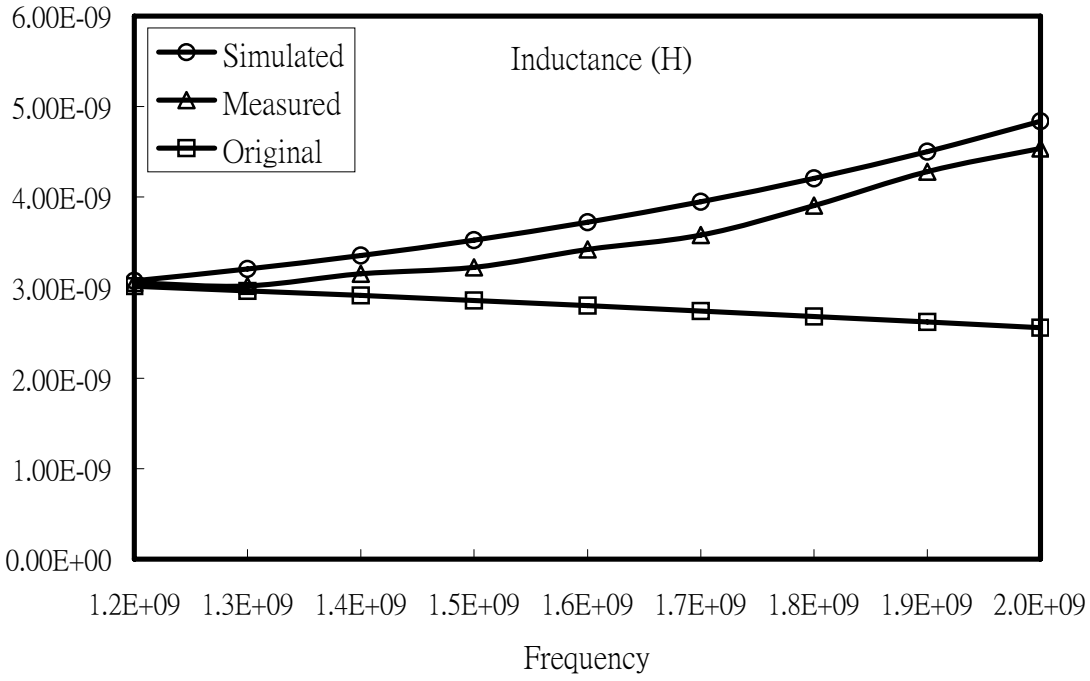


Fig. 4.12 Inductance of the measured result

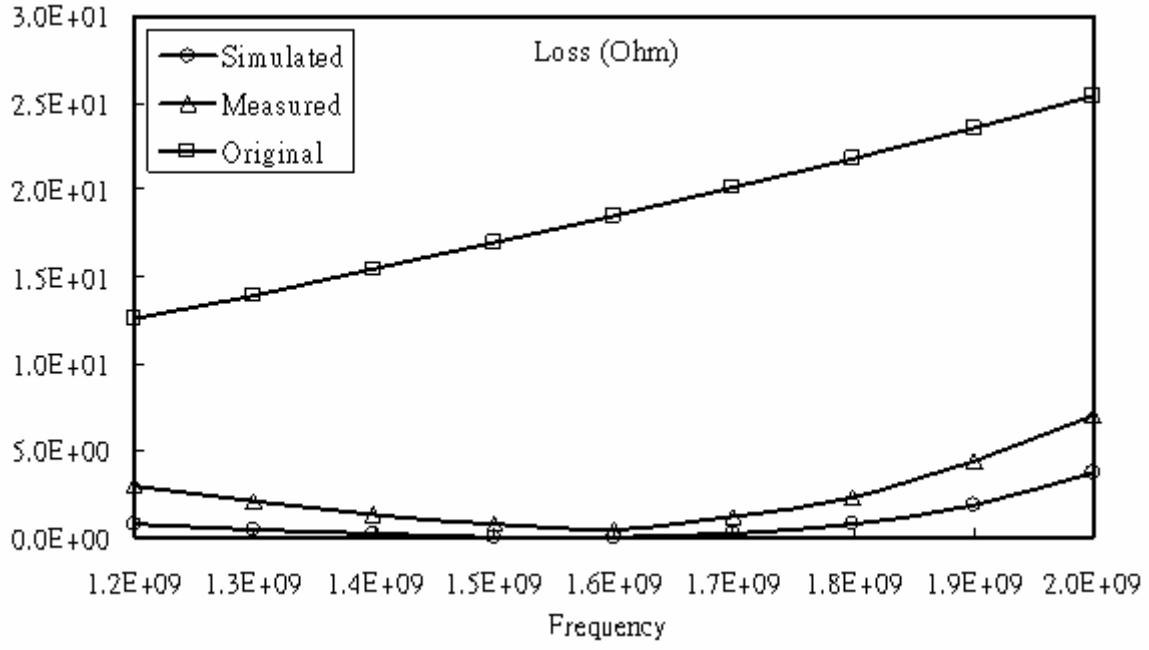


Fig. 4.13 Loss of the measured result

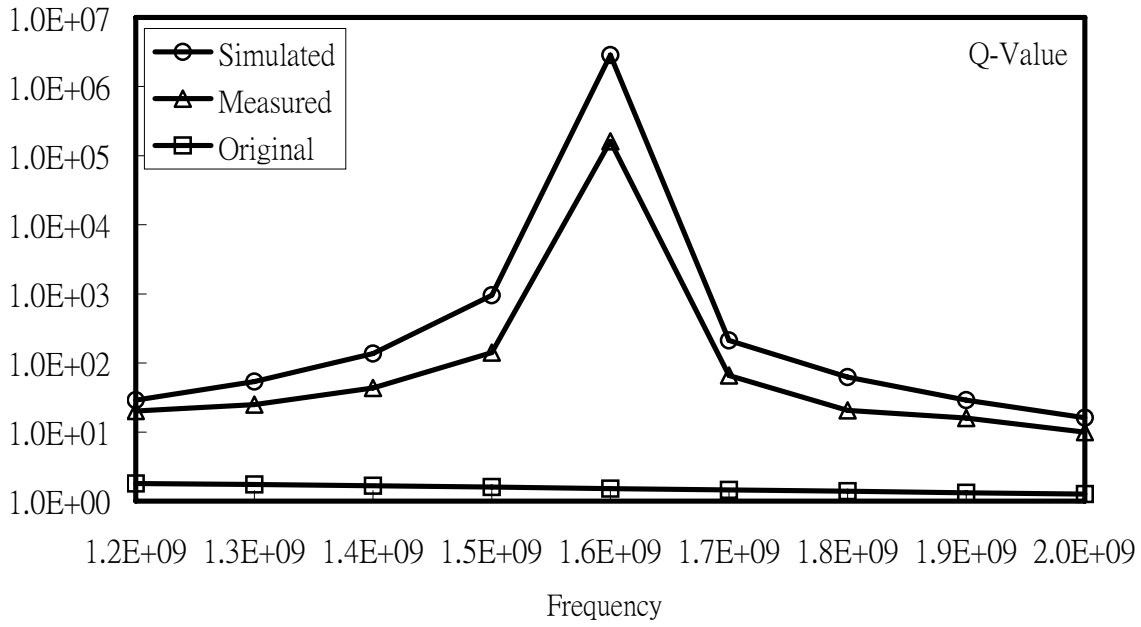


Fig. 4.14 Q-value of the measured result

TABLE 4.2 COMPARISONS BETWEEN SIMULATION AND MEASUREMENT @ 1.6GHZ

	Simulated	Measured
Q	1.2E6	1.1E5
Loss (Ohm)	3E-5	2E-4
Inductance (H)	3.6n	3.2n
Power Consumption (mW)	4.3	5.25

4.1.4 Discussion

A novel CMOS high Q-value RF active inductor by using simple cascode RC feedback loss compensation circuit has been proposed in this work. We use passive RC components in the feedback loop to compensate the loss of CMOS active devices. As a result, a better Q's value (1.1E5) is achieved with total equivalent resistance loss of 2E-4Ω, power consumption of 5.25 mW under 2.5V supply voltage, and inductance value of 3.1nH to 4.3nH in the frequency range of 1.2GHz to 2GHz. These results show that this proposal achieves better

performance indices compared to those having the same active inductor structure published earlier.

4.2 An Improving Active Inductor Using Gain-Boosting and Current-Reused Technique

A gain-boosting technique has been employed to reduce the loss and hence to enhance Q [27]. In this technique, the series loss was reduced only around 100 at1GHz, but the maximum Q value was not obviously promoted. A Q-enhancing approach based on the double-feedback compensation has also been proposed [38]. This technique is developed to reduce the parallel loss, and hence the maximum Q value approximates 12,000 at 1GHz. Furthermore, the current-reused and negative impedance converter techniques were adopted to improve the optimally expected Q value of active inductor [39]. Though the internal loss is compensated, both circuit complexity and power consumption are increasing.

In this work, we propose an effective active inductor to reduce series and parallel losses simultaneously without increasing circuit complexity and power consumption. The design methodology of the improved active inductor circuit and the mathematical analysis are described in section 4.2.1. The simulation results of the proposed active inductor are expressed in section 4.2.2. Finally, the discussion is given in section 4.2.3.

4.2.1 Circuit Design

This novel loss compensation RF CMOS active inductor circuit is derived from a basic model shown in Fig. 4.15 [39]. The circuit is applied with a simple loss compensation circuit

by combining the compensation techniques of a gain-boosting, current-reused, and a double-feedback to reduce the series loss, parallel loss and the parasitic capacitance loss simultaneously. As a result, the total equivalent loss and the Q value can be significantly improved. Furthermore, the power consumption is reduced and the circuit complexity is obviously simplified when comparing with the previously mentioned results [39].

Figure 4.15 is the original active inductor. The equivalent input conductance (Y_{in}) of this active inductor circuit, shown in Fig. 4.16, is expressed as below [39].

$$Y_{in} \approx (g_{dsN1} + g_{mN2}) + SC_{gsN2} + \frac{g_{mN1}(g_{mN2} + g_{dsN2})}{(SC_{gsN1} + g_{dsN2})} \tag{4.3}$$

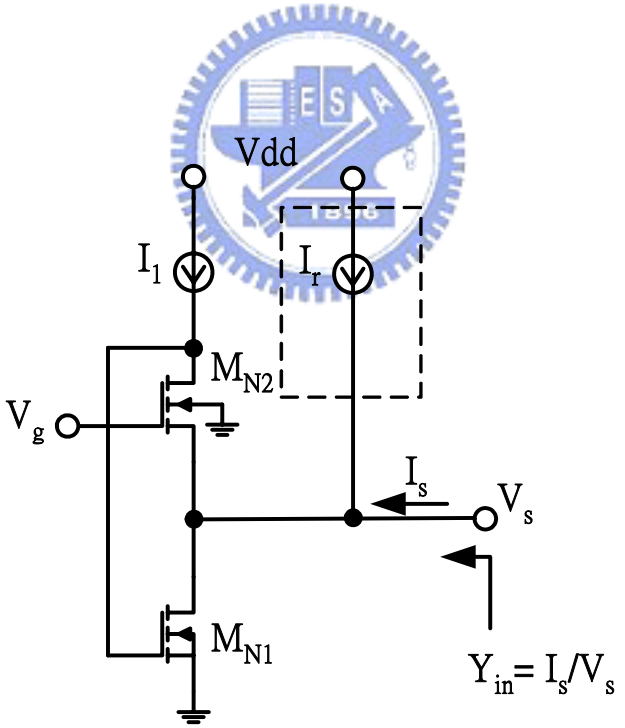


Fig. 4.15 Original circuit of active inductor

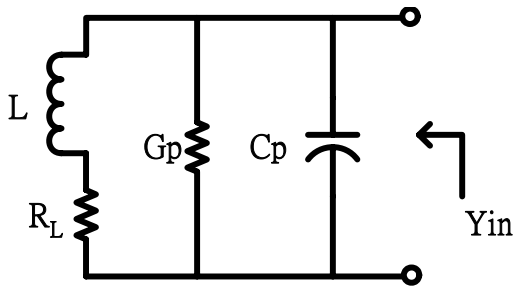


Fig. 4.16 The equivalent circuit of active inductor

From Eq. (4.3), the parallel conductance of (g_{dsN1} + g_{mN2}) and the series resistance $g_{dsN2}/(g_{mN1}g_{mN2})$ are the parallel loss and the series loss of the active inductor respectively. Both of them reduce the performance of the active inductor. In order to improve the performance, it is expected to reduce the series resistance $g_{dsN2}/(g_{mN1}g_{mN2})$ and the parallel conductance (g_{dsN1} + g_{mN2}). In this case, the negative impedance converter is added to improve these losses, but it requires the extra cost and power of complexity circuit.

Therefore, Fig. 4.17 shows the proposed CMOS active inductor circuit based on the CMOS GIC circuit in [39]. The simple loss compensation circuit is composed of current source I_2, transistor M_{P3}, and resistor R_g to improve performance of the active inductor. The loss compensation circuit is designed by combining the current-reused, the gain-boosting, and the double-feedback compensation techniques to simultaneously reduce series/parallel and parasitic capacitance loss. The I_2, R_g, and M_{P3} construct current-reused and gain-boosting techniques, which increase the g_{mN1} and enhance the gain of M_{N1}. Therefore, the series loss resistance (R_L) can be reduced. The parallel loss resistance will be decreased because the negative conductance is created by the double-feedback of M_{P3} and R_G. As the parasitic capacitance loss (C_{gsN2}) is reduced with double-feedback of M_{P3}, this feedback compensates the parasitic capacitance loss and increases the operating frequency. The simple loss

compensation circuit provides an additional inductance reactance of the impedance from the input terminal's point of view. Therefore, the increased Q value also results in an increased inductance and higher operating frequency.

In this analysis, we use C_{gs}, g_{ds}, and g_m to analyze the proposed circuit, and the equivalent input conductance Y_{in} can be expressed below.

$$Y_{in} \approx (g_{dsN1} + g_{dsN2}) + \frac{SC_{gsp1}(g_{dsp1} + g_{mN2}) + S^2 C_{gsN2} C_{gsp1} + g_{mN2} g_{mp1}}{(SC_{gsp1} + g_{mp1}) + (1 + SC_{gsp1} R_g)(SC_{gsN2} + g_{dsp1})} + \frac{g_{mN1} g_{dsN2}}{SC_{gsN1} + g_{dsN2}} + \frac{g_{mN1} g_{mN2}(SC_{gsp1} + g_{mp1})}{(SC_{gsp1} + g_{mp1}) + (1 + SC_{gsp1} R_g)(SC_{gsN2} + g_{dsp1})} \frac{1}{SC_{gsN1} + g_{dsN2}} \quad (4.4)$$

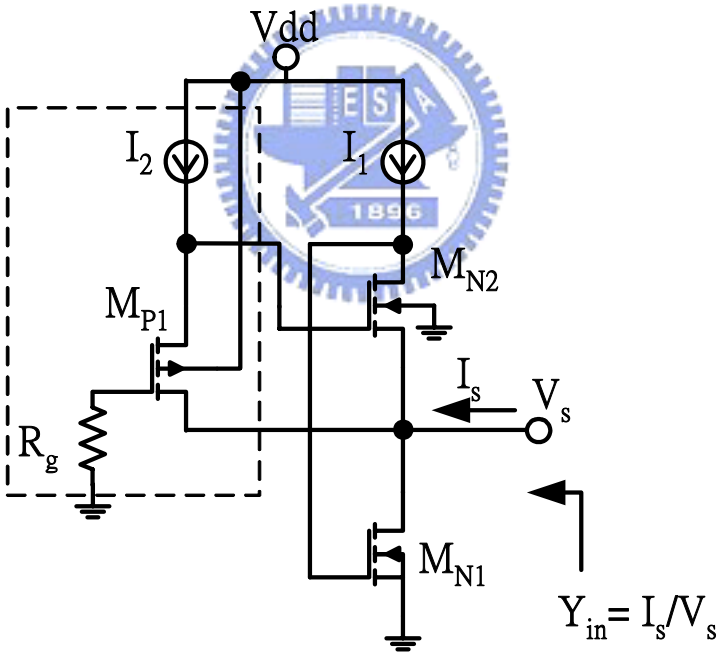


Fig. 4.17 Proposed active inductor with loss compensation

Based on these assumptions of $\omega R_g C_{gsp} << 1$, $g_{mi} >> g_{dsi}$, and all identical MOSFETs dimensions, $C_{gsN1}=C_{gsN2}=C_{gsP1}=C_{gs}$, Y_{in} can be rewritten as Eq. (4.5).

$$Y_{in} \approx (g_{dsN1} + g_{dsN2}) + \frac{SC_{gs}}{2}$$

$$+ \frac{g_{mN1} g_{mN2}{}^2 g_{mp1} (g_{mN1} g_{mN2} + g_{mp1} g_{dsN2})}{S[C_{gs}(2g_{mN1} g_{mN2} + g_{mN2} g_{mp1})](g_{mN1} g_{mN2} + g_{dsp1} g_{dsN2}) + g_{mp1} g_{dsN2} g_{mN1} g_{mN2}{}^2} \quad (4.5)$$

In Eq. (4.5), the equivalent circuit model of using the loss compensation circuit active inductor is also shown in Fig. 4.16. The values of each component are expressed below.

$$G_p = g_{dsN1} + g_{dsN2} \quad (4.6)$$

$$C_p = \frac{C_{gs}}{2} \quad (4.7)$$

$$L = \frac{C_{gs}}{g_{mN1} g_{mN2}} + \frac{C_{gs}}{g_{mN2} g_{mp1}} \quad (4.8)$$

$$R_L = \frac{g_{dsN2}}{g_{mN1} g_{mN2} + g_{mp1} g_{dsN2}} \approx \frac{g_{dsN2}}{g_{mN1} g_{mN2} g_{mp1}} \quad (4.9)$$

In Eq. (4.6), the parallel conductance is changed from ($g_{dsN1} + g_{mN2}$) to ($g_{dsN1}+g_{dsN2}$) so that the parallel loss is reduced. In Eq. (4.7), the capacitance $C_{gs}/2$ is reduced so that the operating frequency is increased. In Eq. (4.8), the equivalent inductance can also be increased. In Eq. (4.9), the numerator (g_{ds2}) of the R_L is divided by a factor of $g_{mN1}g_{mN2}g_{mp1}$, and then the series loss can be reduced. Therefore, the performance of the active inductor can be improved by in consequence, by using the simple loss compensation circuit. If the circuit components are properly chosen, a high Q value, a suitable inductance L, and the desired operating frequency can be implemented.