國立交通大學

電子工程學系電子研究所

博士論文

低電壓互補式金氧半製程下可相容高工作電壓之靜電放電防護設計

HIGH-VOLTAGE-TOLERANT ESD PROTECTION DESIGN IN LOW-VOLTAGE CMOS PROCESSES

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指導教授：柯明道（Ming-Dou Ker)

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摘要

隨著半導體製程的進步與發展，積體電路產品已經成為民生用品般地大量製造與使用，許多整合多功能的系統晶片(SoC)已經成為各電子公司的產品研發主力，電子產業也在這個領域有長足的進步與發展。但由於半導體製造技術的日新月異，使得積體電路對靜電放電防護的能力下降很多，同時由於操作電壓一直在下降，但是週邊電路的電壓卻未隨半導體製程的進步而降低，所以在扮演晶片輸入輸出媒介的混合電壓界面(Mixed-Voltage I/O Interface)上將會產生許多問題，尤其在電子系統訊號整合上。因此要在此混合電壓電路加上其靜電放電保護電路，需要考量界面電壓轉換、混合電壓界面間的漏電流 (Leakage Current)、混合電壓界面電路的可靠度(Reliability)等問題。因此，在混合電壓界面上，如何仔細評估這些問題進而設計出具有高的靜電放電防護能力的電路將是當今以及未來積體電路設計上的重要課題，這個主題隨著半導體製程進入 0.13 微米 以及 90 奈米之後，對積體電路設計產業更加重要。另外，隨著高壓金氧半製程在面版驅動電路(LCD Driver ICs)、電源供應器(Power Supplies)、電源管理(Power Management)，以及汽車電子(Automotive Electronics)等使用的普及化，對

於使用在這些應用的輸出端以及當作靜電放電保護元件的高壓電晶體來說，靜電放電的可靠度問題將比在一般低壓製程的元件來得嚴重，因此如何有效改善靜電放電耐壓能力，將是這些高壓積體電路設計上很重要的課題，這個主題也隨著這些產業應用上的多元化而更趨重要。所以本論文分別針對了混合電壓界面電路以及高壓金氧半製程應用上的限制與困難作討論，並進一步設計出有效的靜電放電防護電路以適用在各相關應用之積體電路晶片。

首先，本論文提出了一種新型的低電壓驅動雙載子接面電晶體(Low-Voltage-Triggered PNP, LVTPNP)來當作混合電壓輸入輸出界面（Mixed-Voltage I/O Interfaces）之靜電放電保護元件。此新型靜電放電保護元件是在CMOS製程中寄生的雙載子接面電晶體的N型井（N-Well）以及P型基板（P-Substrate）接面上，額外植入N型或是P型的擴散離子所構成，以降低N型井以及P型基板接面的崩潰電壓，當輸入電壓比VDD高（Over-VDD）或比VSS低（Under-VSS）時，不會有漏電以及閘極氧化層的可靠度問題。在0.35微米互補式金氧半製程，已經驗證了此低電壓驅動雙載子接面電晶體會比傳統寄生的雙載子接面電晶體的靜電放電耐受程度來得高，而該元件的最佳化佈局方式（Layout Style）也在0.35微米以及0.25微米互補式金氧半製程中驗證來提升元件本身的靜電放電耐受程度，經由實驗證明，具有多指狀（Multi-Finger）佈局方式的元件靜電放電耐受程度會比單指狀（Single Finger）的要來得高。除此之外，在0.25微米製程的晶片驗證下，具有多指狀佈局方式的低電壓驅動雙載子接面電晶體搭配電源間的靜電放電箝制電路(Power-Rail ESD Clamp Circuit)成功地提升了非同步數位用戶專線（Asymmetric Digital Subscriber Line, ADSL）輸入級的靜電放電耐受程度，此輸入級的訊號界於5V到-1V之間，此電壓同時超過了該IC之VDD（2.5V）和低過了該IC之VSS（0V）。

本論文研究的第二部分，為了提供有效的靜電放電防護於 1.2/2.5V 混合電壓輸入輸出界面，本論文提出了新型的靜電放電保護架構並在 0.13 微米製程中成功驗證，此架構同時利用了靜電放電匯流排（ESD BUS）以及可耐高工作電壓之靜電放電箝制電路（High-Voltage-Tolerant ESD Clamp Circuit）來實現。當混合電壓輸入輸出界面的銲墊（Pad）對 VDD（或 VSS）之間遭受靜電轟擊或是輸入輸出腳對腳（Pin-to-Pin）之間遭受靜電轟擊時，此靜電放電保護架構都可以提供相對應的放電路徑來避免內部電路遭受靜電損壞。在此靜電放電防護電路中，可耐高工作電壓之靜電放電箝制電路都是利用 1.2V 低壓元件來實現，並可安全地在 2.5V 的電壓偏壓下工作而不會有閘極氧化層的可靠度問題。由實驗可知，比起一般的堆疊式電晶體（Stacked-NMOS）而言，基板觸發（Substrate Triggered）技術可以有效提升該可耐高工作電壓之靜電放電箝制電路的導通速度以及靜電放電耐受程度。在堆疊式電晶體的元件尺寸為 480μm/0.2μm 的大小之下，1.2/2.5V 的混合電壓輸入輸出界面之人體放電模式靜電放電耐壓能力(HBM ESD levels)可以從原本的 5kV 增加到 6.5kV;同時，機械放電模式靜電放電耐壓能力(MM ESD levels)可以從原本的 275V 增加到 400V。

本論文研究的第三部份，為了提升應用在車用電子（Automotive Electronics）中的真空螢光顯示器（Vacuum-Fluorescent-Display, VFD）驅動 IC 的靜電放電耐受程度，本論文提出一種新型的靜電放電保護的元件結構。此元件結構是在高壓 P 型的金氧半電晶體（HVPMOS）的汲極當中植入一個 N 型離子佈植來形成一個嵌入式高壓 P 型矽控整流器（High-Voltage P-Type Silicon Controlled Rectifier, HVPSCR）路徑，此結構只需要加入額外的 N 型離子局部佈局面積即可實現。在 0.5 微米的互補式金氧半製程中，成功驗證了具有此嵌入式高壓 P 型矽控整流器的真空螢光顯示器驅動積體電路的人體放電模式靜電放電耐壓能力可以從不到 500V 增加到 8kV;同

時，當元件尺寸為 500μm/2μm、600μm/2μm 以及 800μm/2μm 時，機械放電模式之靜電放電耐壓能力可以通過 1100V、1300V 以及 1900V 的靜電測試。此外，此嵌入式高壓 P 型矽控整流器的真空螢光顯示器驅動積體電路可成功通過 ±200mA 的閂鎖（Latchup）測試。

本論文研究的第四部分，觀察到使用在輸出端以及當作靜電放電保護元件的高壓電晶體，靜電放電的可靠度問題比在一般製程的元件來得嚴重，因此本論文利用 40-V 金氧半製程對於不同元件結構以及汲極到閘極的距離（Layout Spacing from Drain to Polygate）做一深入探討。實驗結果成功驗證了汲極下端沒有植入的飄移摻雜（Drift Implant）佈局的高壓金氧半電晶體比起汲極下端有加入移摻雜的高壓金氧半電晶體有較高的二次崩潰電流（Secondary Breakdown Current, It2）以及較好的靜電放電防護能力。在所有元件結構當中，嵌入在高壓 N 型的金氧半電晶體中的高壓 N 型矽控整流器（HVNSCR）並在汲極下端移除了飄移摻雜的結構，具有最高的二次崩潰電流以及靜電放電耐受度。此外，元件模擬技巧也成功地分析了有無飄移摻雜對於元件內電流分佈的影響。

本論文分別針對了混合電壓界面電路以及高壓金氧半製程應用上的限制與困難作討論，並進一步設計出有效的靜電放電防護電路應用在各相關之積體電路晶片。本博士論文所提出電路已經有相對應的國際期刊與會議論文發表以及專利申請。

HIGH-VOLTAGE-TOLERANT ESD PROTECTION DESIGN IN LOW-VOLTAGE CMOS PROCESSES

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ABSTRACT

The scaling trend of the CMOS technology is toward the nanometer region to increase the speed and density of the transistors in integrated circuits. Due to the reliability issue, the power supply voltage is also decreased with the advanced technologies. However, in an electronic system, some circuits could be still operated at high voltage levels. If the circuits realized with low-voltage devices are operated at high voltage levels, the gate-oxide breakdown and leakage issues will occur. Therefore, for the CMOS integrated circuits (ICs) with the mixed-voltage I/O interfaces, the on-chip electrostatic discharge (ESD) protection circuits will meet more design constraints and difficulties. The on-chip ESD protection circuit for mixed-voltage I/O interfaces should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths during normal circuit operating operation. During ESD stress condition, the on-chip ESD protection circuit should provide effective ESD protection for the internal circuits. In high-voltage CMOS technology, high-voltage transistors have been widely used for display driver ICs, power supplies, power management, and automotive electronics. The high-voltage MOSFET was often used as the ESD protection device in the high-voltage CMOS ICs, because it can work as both of output driver and ESD protection device simultaneously. With an ultra-high operating voltage, the ESD robustness of high-voltage MOSFET is quite weaker than that of low-voltage MOSFET. Hence, how to improve the ESD robustness of HV NMOS with a reasonable silicon area is indeed an important reliability issue in HV CMOS technology. In this thesis, some new ESD protection structures are proposed to improve ESD robustness of the high-voltage IC products fabricated in CMOS technology.

To protect the mixed-voltage I/O interfaces for signals with voltage levels higher than VDD (over-VDD) and lower than VSS (under-VSS), ESD protection design with the low-voltage-triggered PNP (LVTPNP) device in CMOS technology is proposed. The LVTPNP is realized by inserting N+ or P+ diffusion across the junction between N-well and P-substrate of the PNP device. The LVTPNP devices with different structures have been investigated and compared in CMOS processes. The experimental results in a 0.35-μm CMOS process have proven that the ESD level of the proposed LVTPNP is higher than that of the traditional PNP device. Furthermore, layout on LVTPNP device for ESD protection in mixed-voltage I/O interfaces is also optimized in this work. The experimental results verified in both 0.35-μm and 0.25-μm CMOS processes have proven that the ESD levels of the LVTPNP drawn in the multi-finger layout style are higher than that drawn in the single finger layout style. Moreover, one of the LVTPNP devices drawn with the multi-finger layout style has been used to successfully protect the input stage of an ADSL IC in a 0.25-μm salicided CMOS process.

To increase the system-on-chip ESD immunity of micro-electronic products against system-level ESD stress, the chip-level ESD/EMC protection design should be enhanced. Considering gate-oxide reliability, a new ESD protection scheme with ESD_BUS and high-voltage-tolerant ESD clamp circuit for 1.2/2.5 V mixed-voltage I/O interfaces is proposed in this chapter. The devices used in the high-voltage-tolerant ESD clamp circuit are all 1.2 V low-voltage NMOS/PMOS devices which can be safely operated under the 2.5 V bias conditions without suffering from the gate-oxide reliability issue. The four-mode (PS, NS, PD, and ND) ESD stresses on the mixed-voltage I/O pad and pin-to-pin ESD stresses can be effectively discharged by the proposed ESD protection scheme. The experimental results verified in a 0.13 μm CMOS process have confirmed that the proposed new ESD protection scheme has high human-body-model (HBM) and machine-model (MM) ESD robustness with a fast turn-on speed. The proposed new ESD protection scheme, which is designed with only low-voltage devices, is an excellent and cost-efficient solution to protect mixed-voltage I/O interfaces.

To greatly improve ESD robustness of the vacuum-fluorescent-display (VFD) driver IC for automotive electronics applications, a new electrostatic discharge protection structure of

high-voltage P-type silicon controlled rectifier (HVPSCR) embedded into the high-voltage PMOS device is proposed. By only adding the additional N+ diffusion into the drain region of high-voltage PMOS, the TLP-measured secondary breakdown current (It2) of output driver has been greatly improved greater than 6A in a 0.5-µm high-voltage CMOS process. Such ESD-enhanced VFD driver IC, which can sustain HBM ESD stress of up to 8kV, has been in mass production for automotive applications in car without latchup problem. Moreover, with device widths of 500µm, 600µm, and 800µm, the MM ESD levels of the HVPSCR are as high as 1100V, 1300V, and 1900V, respectively.

The dependences of drift implant and layout parameters on ESD robustness in a 40-V CMOS process have been investigated in silicon chips. From the experimental results, the HV MOSFETs without drift implant in the drain region have better TLP-measured It2 and ESD robustness than those with drift implant in the drain region. Furthermore, the It2 and ESD level of HV MOSFETs can be increased as the layout spacing from the drain diffusion to polygate is increased. It was also demonstrated that a specific test structure of HV n-type silicon controlled rectifier (HVNSCR) embedded into HV NMOS without N-drift implant in the drain region has the excellent TLP-measured It2 and ESD robustness. Moreover, due to the different current distributions in HV NMOS and HVNSCR, the dependences of the TLP-measured It2 and HBM ESD levels on the spacing from the drain diffusion to polygate are different.

In this thesis, the novel ESD protection circuits have been developed for mixed-voltage I/O interfaces and high-voltage CMOS process with high ESD robustness. Each of the ESD protection circuits has been successfully verified in the testchips.

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謹誌於竹塹交大
96年 秋

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INTRODUCTION

1.1 Background

Electrostatic Discharge (ESD) has become the main reliability concern on semiconductor products, especially for the system-on-a-chip (SOC) implementation in nanoscale CMOS processes. The ESD specifications of commercial IC products are generally required to be higher than 2kV in human-body-model (HBM) [1] ESD stress. Therefore, on-chip ESD protection circuits have to be added between the input/output (I/O) pad and VDD/VSS to provide the desired ESD robustness in CMOS integrated circuits (ICs) [2]–[4]. ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode), as shown in Figs. 1.1(a) ~ 1.1(d), respectively. The typical design of on-chip ESD protection circuits in a CMOS IC is illustrated in Fig. 1.2. To avoid the unexpected ESD damage in the internal circuits of CMOS ICs [5]–[7], the turn-on-efficient power-rail ESD clamp circuit was placed between VDD and VSS power lines [8]. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of PMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground. Consequently, the traditional I/O circuits cooperating with the VDD-to-VSS ESD clamp circuit can achieve a much higher ESD level [8].

1.2 Issue of Mixed-Voltage I/O Interface

To improve circuit operating speed and performance, the device dimension of MOSFET has been shrunk in the advanced CMOS ICs. With the scaled-down device dimension in advanced CMOS technology, the power supply voltage is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. However, most microelectronic systems nowadays consist of mix semiconductor chips fabricated in different CMOS technologies. Therefore, the microelectronic systems often require the interfaces between semiconductor chips or sub-systems which have different internal power supply voltages. With the different power supply voltages in a microelectronic system, chip-to-chip I/O interface circuits must be designed to avoid electrical overstress across the gate oxide [9], to avoid hot-carrier degradation [10] on the output devices, and to prevent the undesired leakage current paths between the chips [11], [12]. For example, a chip which operates with internal power supply voltage of 1.2V may have the I/O signals of 2.5V. The traditional CMOS I/O buffer with VDD of 1.2V and 1.2-V gate oxide devices is shown in Fig. 1.3(a) with both input and output stages. When an external 2.5-V signal is applied to the I/O pad, the channel of the pull-up PMOS and the parasitic drain-to-well junction diode in the pull-up PMOS will cause the leakage current paths from I/O pad to VDD, as the dashed lines shown in Fig. 1(a). Moreover, the 1.2-V gate oxides of the pull-down NMOS and the input inverter will be over-stressed by the 2.5-V input signal to suffer the gate-oxide reliability issue. By using the additional thick gate-oxide process (or called as dual gate-oxide CMOS process [13], [14]), the gate-oxide reliability issue can be avoided. However, the process complexity and fabrication cost are increased.

To solve the gate-oxide reliability issue without using the additional thick gate-oxide process, the stacked-NMOS configuration has been widely used in the mixed-voltage I/O circuits [15]–[21]. The typical 1.2V/2.5V-tolerant mixed-voltage I/O circuit is shown in Fig. 1.3(b). The independent control on the top and bottom gates of stacked-NMOS device allows the devices to meet reliability limitations during normal circuit operation. Therefore, the stacked-NMOS can be operated within the safe range for both dielectric and hot-carrier reliability limitations. The pull-up PMOS, connected from the I/O pad to the VDD power line, has the gate tracking circuits for tracking the gate voltage and the N-well self-biased circuits for tracking N-well voltage, which are designed to ensure that the pull-up PMOS does not conduct current when the 2.5-V input signals enter the I/O pad. In such mixed-voltage I/O circuits, the on-chip ESD protection circuits will meet more design constraints and difficulty.

The ESD protection design of I/O pad cooperating with power-rail ESD clamp circuit is shown in Fig. 1.4(a), where a PS-mode ESD pulse is applied to the I/O pad. The ESD current paths (I_{ESD}), including I_{ESD1} and I_{ESD2}, along the traditional CMOS output buffer are also illustrated by the dashed lines in Fig. 1.4(a), where most of ESD current (I_{ESD1}) is discharged through the parasitic diode of the PMOS and the VDD-to-VSS ESD camp circuit to ground. Therefore, the traditional CMOS output buffer can sustain a higher ESD stress with cooperation of active power-rail ESD clamp circuit. But, due to the leakage current issue in the mixed-voltage I/O circuits, there is no diode connected from the I/O pad to VDD power line in the mixed-voltage I/O circuits. Without the diode connected from the I/O pad to VDD in the mixed-voltage I/O circuits, the ESD current at I/O pad under PS-mode ESD stress cannot be discharged from the I/O pad to VDD power line, and cannot be discharged through the additional VDD-to-VSS ESD clamp circuit. Therefore, the power-rail ESD clamp circuit did not help to pull up ESD level of the mixed-voltage I/O pad under the PS-mode ESD stress. The ESD current path in the mixed-voltage I/O circuits with power-rail ESD clamp circuit under PS-mode ESD stress in illustrated in Fig. 1.4(b). Such ESD current at the I/O pad is mainly discharged through the stacked-NMOS by snapback breakdown. Besides, comparing the single NMOS and the stacked-NMOS in the high-current snapback region, the stacked-NMOS will have a higher trigger voltage (Vt1), a higher snapback holding voltage (Vsb), slower turn-on speed, and a lower secondary breakdown current (It2), as shown in Fig. 1.5. Therefore, such mixed-voltage I/O circuits with stacked-NMOS often have much lower ESD level under the PS-mode ESD stress, as compared to the traditional I/O circuits with a single NMOS [22], [23]. In addition, without the diode connected from the I/O pad to VDD, the mixed-voltage I/O circuit also has a lower ESD level for I/O pad under PD-mode ESD stress. The absence of the diode between I/O pad and VDD power line in the mixed-voltage I/O circuits will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses. By using extra process modification such as ESD implantation, the ESD robustness of stacked-NMOS device can be further improved [24], [25], but the process complexity and fabrication cost are increased. In addition, the induced high voltage on the gate of top NMOS transistor under ESD stress will cause high-current crowding effect in the channel region to seriously degrade ESD robustness of stacked-NMOS device in the mixed-voltage I/O circuits [26]. Therefore, effective ESD protection design without increasing process complexity is strongly requested by the mixed-voltage I/O circuits in the scaled-down CMOS processes.

One of the mixed-voltage circuit applications, such as the interface in ADSL which has input signals with voltage levels higher than VDD and lower than VSS, is shown in Fig. 1.6 The traditional on-chip ESD protection circuits are not suitable for such mixed-voltage interfaces. The ESD diode D_p (D_n) will be forward biased when the input signal levels are higher than VDD (lower than VSS). This ESD protection circuit will cause current leakage between the chips of the mixed-voltage I/O interface. Moreover, traditional on-chip ESD protection with NMOS/PMOS will also cause the same leakage issue and suffer the gate-oxide reliability issue when the over-VDD or under-VSS external signals reach to the input pad. To meet such mixed-voltage I/O interface, the SCR device with floating P-well structure in an N-substrate CMOS process had been used as on-chip ESD protection device [27]. However, the SCR device with a floating well structure is very sensitive to latchup [28], [29]. The mixed-voltage I/O interfaces in the system applications often have serious overshooting or undershooting signal transition, which could trigger on the SCR device in the ESD protection circuit of I/O pad to induce latchup troubles to the chip [27].

1.3 Issue of High-Voltage CMOS ICs

High-voltage (HV) CMOS process has been widely used in LCD driver circuits, telecommunication, power switch, motor control systems, etc [30]. In the smart-power technology, high-voltage MOSFET, silicon controlled rectifier (SCR) device, or bipolar junction transistor were used as on-chip electrostatic discharge (ESD) protection devices [31]–[38]. Some ESD protection designs used the lateral or vertical bipolar transistors as ESD protection devices in smart power technology [36], [37]. However, fabrication cost and process complexity are increased by adding bipolar modules into the high-voltage CMOS process. The high-voltage MOSFET was often used as the ESD protection device because it can work as both of output driver and ESD protection device simultaneously in the high-voltage CMOS ICs. With an ultra-high operating voltage, the ESD robustness of high-voltage MOSFET is quite weaker than that of low-voltage MOSFET [31]–[38]. To increase ESD robustness, the conventional design with large device dimension still suffers the non-uniform current distribution among the device. The HV NMOS has the extremely strong snapback phenomenon during ESD stress, which often results in non-uniform turn-on variation among the multi-fingers of HV NMOS [39]. To overcome the problem of non-uniform turn-on phenomenon, the gate-coupling technique was applied to the HV NMOS [32], [33]. However, the gate of HV NMOS must be in series with a large resistor, which occupies a large layout area. Hence, how to improve the ESD robustness of HV NMOS with a reasonable silicon area is indeed an important reliability issue in HV CMOS technology.

In some specific applications, such as the driver IC for vacuum fluorescent display (VFD) [40] in automotive instrumentation [41], only high-voltage PMOS (HVPMOS) is provided in a given CMOS process which is developed by adding a few additional masks and process steps into the low-cost low-voltage CMOS process. To reduce the fabrication cost, no high-voltage NMOS is used in such specific VFD driver IC. For safety concerns in automotive electronics, the ESD robustness was often requested much higher than that of consumer electronics products. Thus, an additional protection device is necessary in the high-voltage I/O pin to sustain a high enough ESD robustness of the VFD driver IC for safe automotive applications.

1.4 Thesis Organization

To overcome the ESD design constraints in mixed-voltage I/O interfaces, and high-voltage CMOS process, the novel on-chip ESD protection designs are developed and verified in this thesis.

This thesis contains seven chapters. Chapter 1 presents the basic design concept of ESD protection design for commercial IC products in CMOS technology. Moreover, ESD protection design for mixed-voltage I/O interfaces should be concerned about the gate-oxide reliability issue and leakage current path. ESD protection design for high-voltage CMOS process should be concerned about the quite weak ESD robustness due to the ultra-high operating voltage.

In chapter 2, presents an overview on the design concept and circuit implementations of the ESD protection designs for mixed-voltage I/O interfaces without using the additional thick gate-oxide process. To improve ESD level of the mixed-voltage I/O circuits, the ESD protection design without increasing the process complexity is strongly requested by the mixed-voltage I/O circuits in consumer IC products. Such ESD protection design in the mixed-voltage I/O circuits still meets the gate-oxide reliability constraints, and needs to prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current.

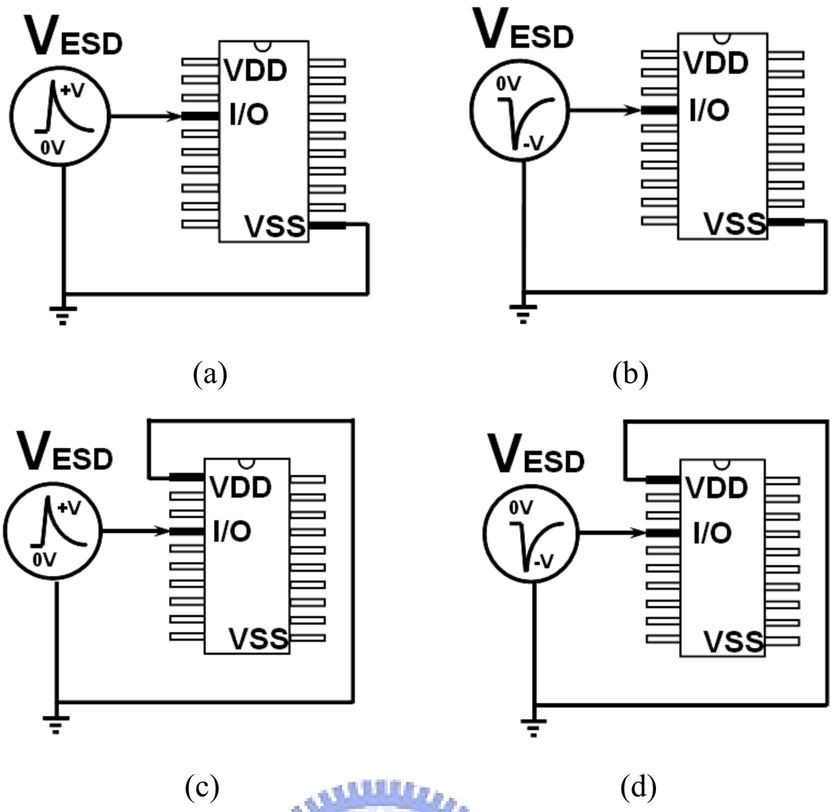
In chapter 3, presents a new ESD protection design with the low-voltage-triggered PNP (called as LVTPNP) device to protect the I/O interfaces with input voltage levels higher than VDD or lower than VSS. Comparing to the traditional PNP device in CMOS process, the new proposed LVTPNP with a low breakdown voltage, by avalanche breakdown across the P+/N-well or N+/P-sub junctions, provides effective discharging path to protect the mixed-voltage I/O interfaces against ESD stresses. Under normal circuit operation conditions, the LVTPNP device is kept off without causing current leakage between the chips. Furthermore, layout optimization on the LVTPNP device to increase its ESD robustness per silicon area has been also studied. The multi-finger layout style is used to improve ESD robustness of the LVTPNP device. Moreover, the input stage of ADSL protected by the LVTPNP device has been practically implemented in a 0.25-μm salicided CMOS process to achieve a better ESD robustness.

In chapter 4, presents a new ESD protection scheme with an ESD_BUS and a high-voltage-tolerant ESD clamp circuit, which is designed to protect the mixed-voltage I/O interfaces against ESD stresses without suffering the gate-oxide reliability issue. The proposed high-voltage-tolerant ESD clamp circuit, which combines the stacked-NMOS of 1.2-V gate oxide with the substrate-triggered technique, is designed to protect the 1.2/2.5 V mixed-voltage I/O interfaces. This high-voltage-tolerant ESD clamp circuit has higher ESD robustness and a faster turn-on speed, which has been successfully verified in a 0.13-μm 1.2-V CMOS process.

In chapter 5, presents a new ESD protection structure with the embedded high-voltage p-type SCR (HVPSCR) into the high-voltage PMOS device to protect the vacuum fluorescent display (VFD) in automotive instrumentation. Only an additional N+ diffusion is added into the HVPMOS to form the HVPSCR for ESD protection. The HVPSCR device structure can greatly improve HBM ESD robustness of the VFD driver IC up to 8kV in the specific 0.5-μm high-voltage CMOS process for automotive electronics applications without suffering latchup issue.

In chapter 6, presents ESD robustness of MOSFETs in a 40-V CMOS process with or without drift implant. In addition, the layout spacing from the drain diffusion to polygate is split to find its dependence on ESD robustness. To improve ESD robustness of HV NMOS in a limit layout area, a specific structure of HV n-type SCR (HVNSCR) can be built in the HV NMOS by replacing part of the drain region with P+ diffusion. ESD robustness of HVNSCR is also verified with or without the N-drift implant under different layout spacings from the drain region to polygate. All test chips have been fabricated in a 0.35-μm 40-V CMOS technology.

Finally, the main results of this thesis are summarized in chapter 7. Some suggestions for the future works are also addressed in this chapter.



(a) (b)

(c) (d)

Fig. 1.1 The four pin-combination modes for ESD test on an IC product: (a) positive-to-VSS (PS-mode), (b) negative-to-VSS (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode).

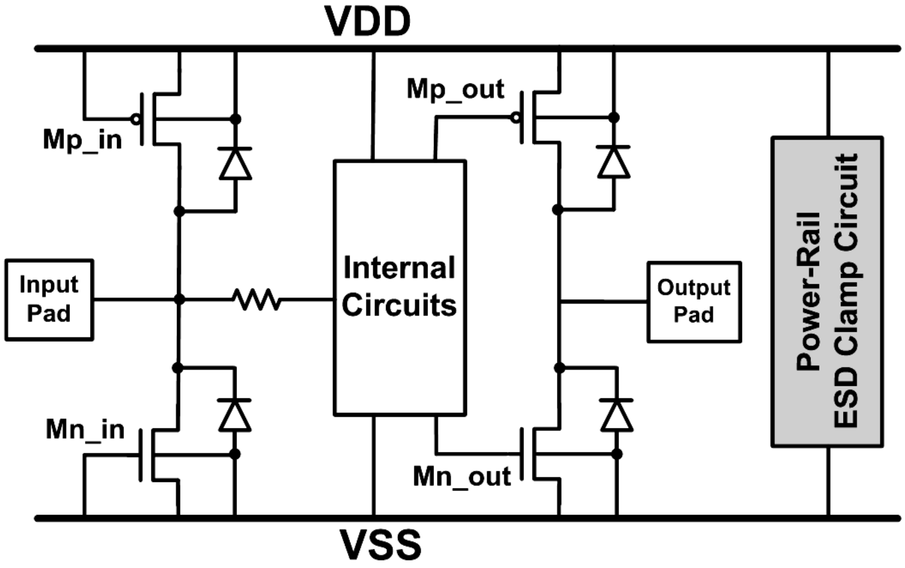
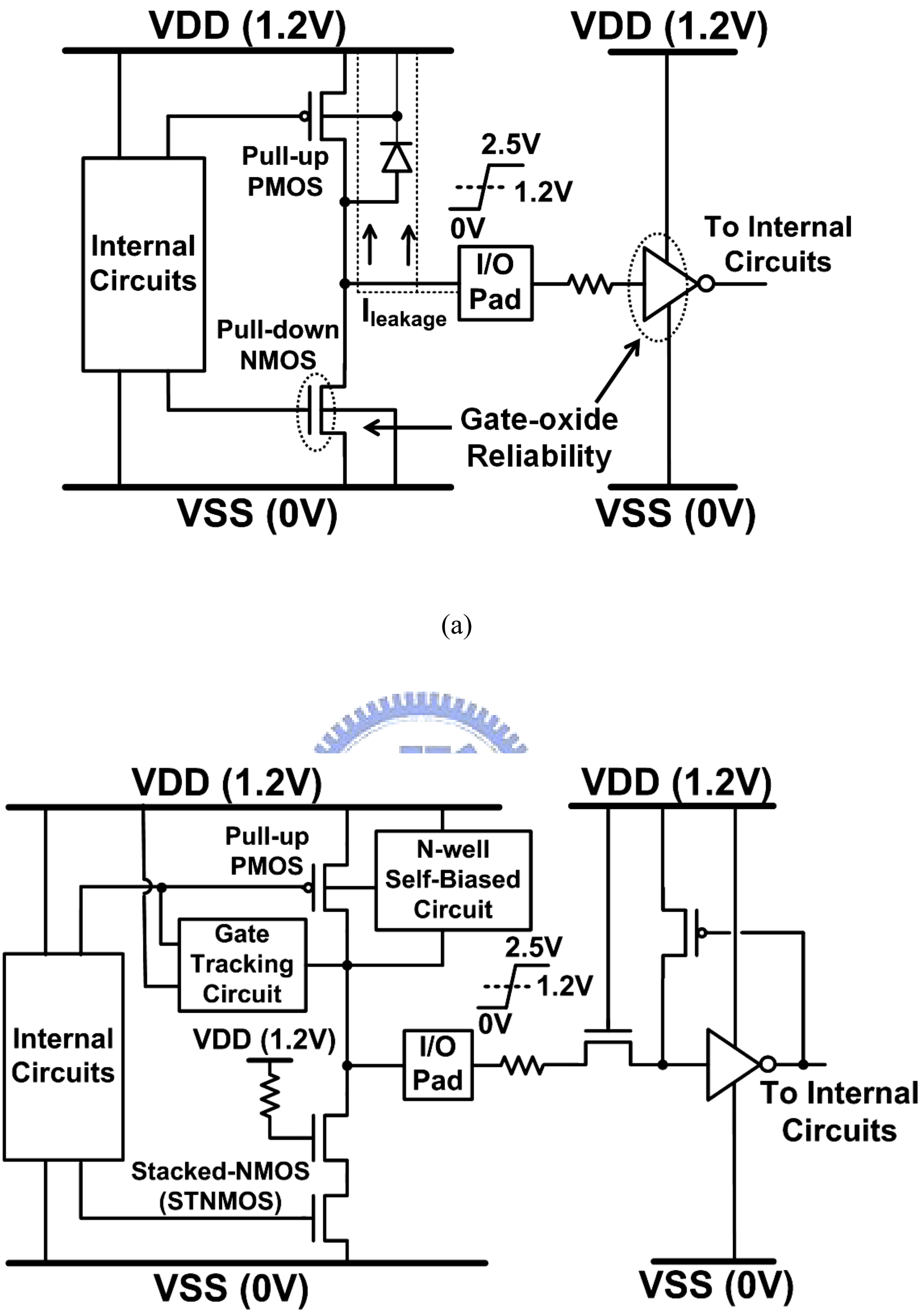


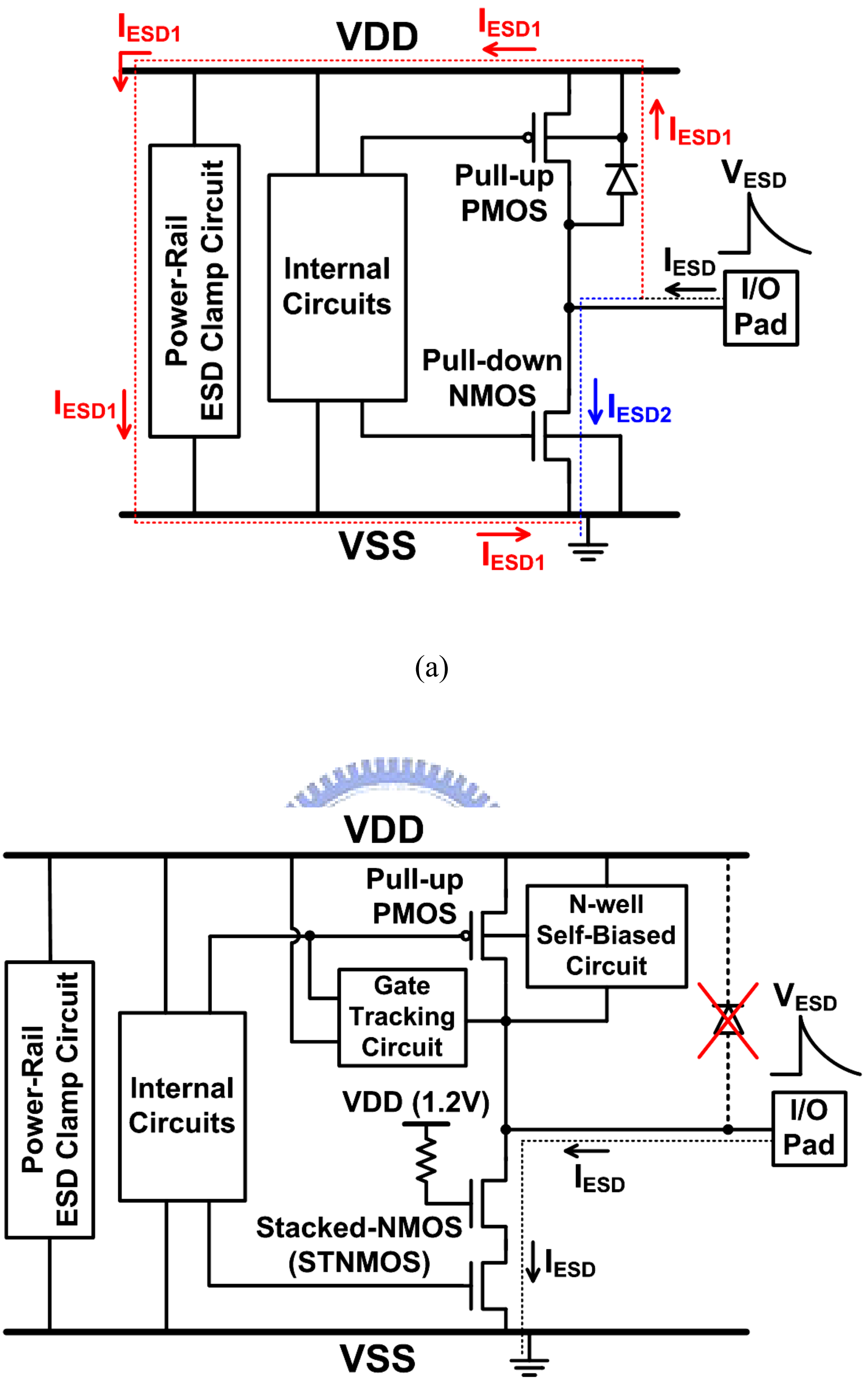
Fig. 1.2 Typical on-chip ESD protection circuits in a CMOS IC.



(a)

(b)

Fig. 1.3 Typical circuit diagrams for (a) the traditional CMOS I/O buffer, and (b) the mixed-voltage I/O circuits with the stacked-NMOS and the N-well self-biased PMOS.



(a)

(b)

Fig. 1.4 The ESD current paths of (a) the traditional I/O pad with power-rail ESD clamp circuit, and (b) the mixed-voltage I/O pad with power-rail ESD clamp circuit, under the positive-to-VSS (PS-mode) ESD stress. The ESD current paths are indicated by the dashed lines.

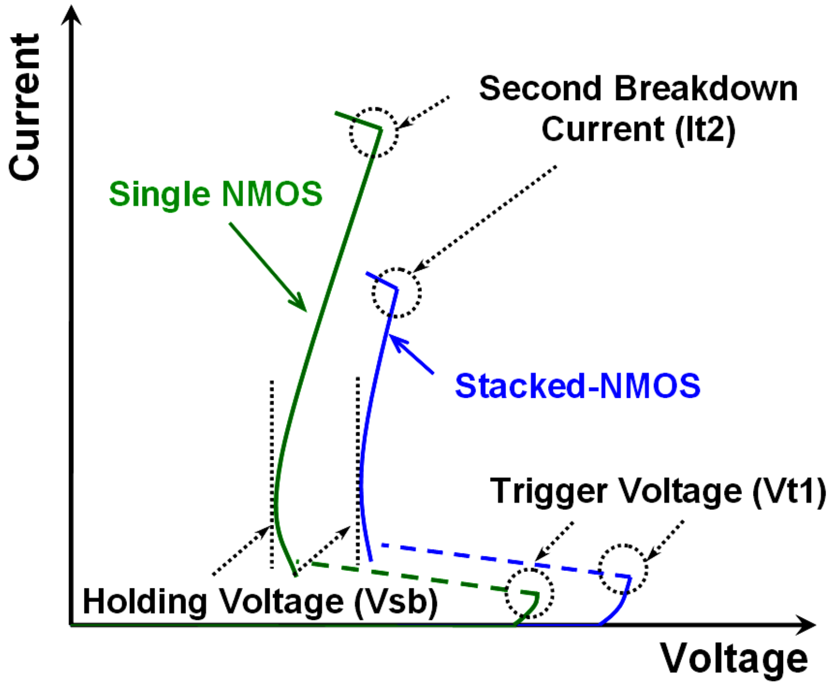


Fig. 1.5 The I-V curves in high-current region of single NMOS and stacked-NMOS.

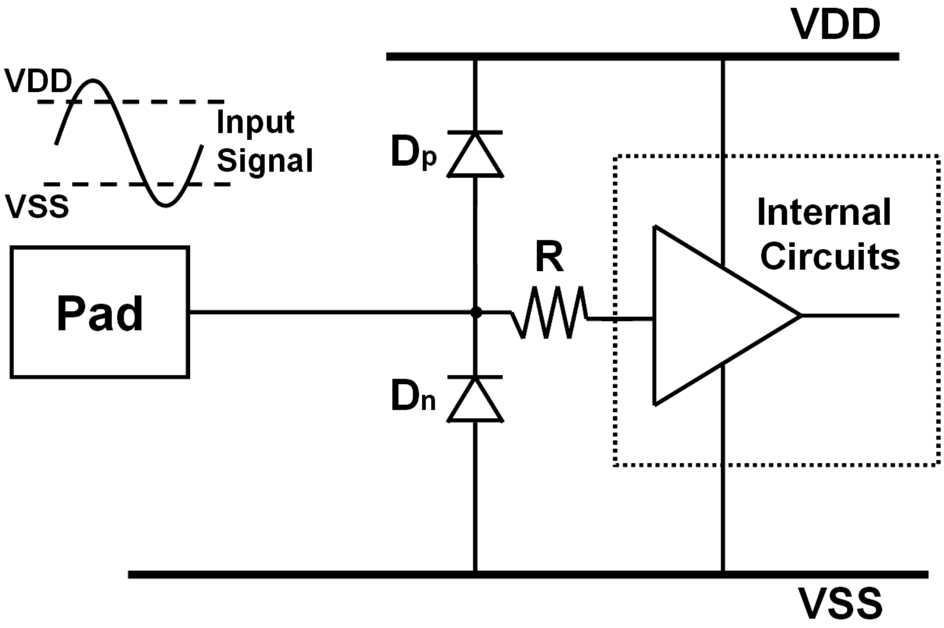


Fig. 1.6 The input signals with voltage levels higher than VDD and lower than VSS in some mixed-voltage I/O interfaces.

CHAPTER 2

OVERVIEW ON ESD PROTECTION DESIGN FOR MIXED-VOLTAGE I/O CIRCUITS

ESD protection design for mixed-voltage I/O interfaces has been one of the key challenges of SOC implementation in nanoscale CMOS processes. The on-chip ESD protection circuit for mixed-voltage I/O interfaces should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths. In this chapter, an overview on the design concept and circuit implementations of ESD protection designs is presented for mixed-voltage I/O interfaces with only low-voltage thin-oxide CMOS transistors. The ESD design constraints in mixed-voltage I/O interfaces, the classification, and analysis of ESD protection designs for mixed-voltage I/O interfaces are presented and discussed.

2.1 Substrate-Triggered Stacked-NMOS Device

The snapback operation of the parasitic n-p-n BJT in the stacked-NMOS structure can be controlled by its substrate potential. The substrate-triggered technique [42] can be used to generate the substrate current (I_{sub}) in ESD protection circuits. With the substrate-triggered current (I_{trig}), the trigger voltage of the stacked-NMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection.

The finger-type layout pattern and the corresponding cross-sectional view of the substrate-triggered stacked-NMOS device are shown in Figs. 2.1(a) and 2.1(b), respectively. As shown in the layout top view, an additional p+ diffusion is inserted into the center drain region of stacked-NMOS device as the substrate-triggered node. The trigger current is provided by the substrate-triggered circuit. An n-well structure is further diffused under the source region, which is also surrounding the whole device, to form a higher equivalent substrate resistance (R_{sub}) for improving turn-on efficiency of the parasitic lateral BJT in the stacked-NMOS device. The substrate-triggered circuit should be designed to avoid electrical overstress on the gate oxide and to prevent the undesired leakage current paths during normal circuit operating condition. During ESD stress condition, the substrate-triggered circuit should generate large enough trigger current to effectively improve the turn-on efficiency of parasitic n-p-n BJT in stacked-NMOS device.

The substrate-triggered circuit I for stacked-NMOS device in the mixed-voltage I/O circuits is shown in Fig. 2.2 [43]. The substrate-triggered circuit I is composed of the diode string, a PMOS Mp1, and an NMOS Mn1, to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-NMOS device during ESD stress. Under normal circuit operating condition, the turn-on voltage of the substrate-triggered circuit roughly equals to Vpad $\geqq V_{string}(I)+|Vtp|+VDD$, where $V_{string}(I)$ is the total voltage drop across the diodes and Vtp is the threshold voltage of the PMOS. To satisfy the requirement in the 2.5V/3.3V mixed-voltage application, the number of the diodes in the diode string should be adjusted to make the turn-on voltage greater than 3.3V. When a 3.3-V input voltage is applied at I/O pad, Mp1 is kept off, and the local substrate of the stacked NMOS is biased at VSS by the turned-on Mn1. With the diode string to block the 3.3-V input voltage at the I/O pad, the Mp1 with thin gate oxide has no gate-oxide reliability issue under normal circuit operating condition. The Mp1 in conjunction with the diode string is used to reduce the leakage current through the substrate-triggered circuit in normal operating condition. If a lower input leakage is desired, the numbers of the diodes in the diode string should be increased. Under PS-mode ESD stress condition, the gate of the Mp1 has an initial voltage level of ~0V, while the VSS pin is grounded but the VDD pin is floating. The substrate-triggered circuit will provide the trigger current flowing through the diode string and the Mp1 into the p-substrate, when Vpad $\geqq V_{string}(I)+ |Vtp|$. The trigger current provided by the substrate-triggered circuit is determined by the diode string and the size of Mp1. Once the parasitic n-p-n BJT in the stacked-NMOS device is triggered on, the ESD current will be discharged from the I/O pad to VSS.

Another substrate-triggered circuit II for stacked-NMOS device in the mixed-voltage I/O circuits is shown in Fig. 2.3 [44]. The substrate-triggered circuit II is composed of the PMOS Mp1, PMOS Mp2, NMOS Mn1, and NMOS Mn2, to provide the substrate current for triggering on the parasitic n-p-n BJT in the stacked-NMOS device during ESD stress. In the 2.5V/3.3V mixed-voltage IC application, the gates of Mp1 and Mp2 are biased at 2.5-V VDD supply through a resistor Rd under normal circuit operating condition. When the input voltage transfers from 0V to 3.3V at the I/O pad, the gate voltage of Mn1 could be increased through the coupling capacitor C. However, the Mn2 and Mp2 can clamp the gate voltage of

Mn1 between VDD-Vtn and VDD+|Vtp|, where Vtn is the threshold voltage of NMOS. Once the gate voltage of Mn1 is over VDD+|Vtp|, the Mp2 will turn on to discharge the over-coupled voltage and to keep the gate voltage within VDD+|Vtp|. Since the upper boundary on the gate voltage of Mn1 is within VDD+|Vtp|, the source voltage of Mp1 is clamping below VDD, which keeps the Mp1 always off under normal circuit operation condition. The Mn2 and Mp2 can further clamp the gate voltage of Mn1 to avoid gate-oxide reliability issue in the substrate-triggered circuit, even if the I/O pad has a high input voltage level. Under PS-mode ESD-stress condition, the gates of Mp1 and Mp2 have an initial voltage level of ~0V, while the VSS pin is grounded but the VDD pin is floating. The positive ESD transient voltage on the I/O pad is coupled through the capacitor C to the gate of Mn1. In this situation, both of the Mn1 and Mp1 are operated in the turned-on state. Therefore, the substrate-triggered circuit II will conduct some ESD current flowing from I/O pad through Mn1 and Mp1 into the p-substrate. The trigger current provided by the substrate-triggered circuit II is determined by the size of Mn1, Mp1, and the capacitor C. Once the parasitic n-p-n BJT in the stacked-NMOS device is triggered on, the ESD current can be mainly discharged from the I/O pad to VSS.

Both two substrate-triggered designs can significantly reduce the trigger voltage and ensure effective ESD protection for the mixed-voltage I/O circuits. By using such substrate-triggered designs, the gates of stacked-NMOS in the mixed-voltage I/O circuits can be fully controlled by the pre-driver of I/O circuits without conflict to the ESD protection circuits. The main ESD discharge device is the parasitic n-p-n BJT in the stacked-NMOS device. Therefore, the ESD robustness of mixed-voltage I/O circuits can be effectively improved without occupying extra silicon area to realize the additional stand-alone ESD protection device into the mixed-voltage I/O cells.

2.2 Extra ESD Protection Device Between I/O Pad and VSS

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and VSS power line [45], [46]. The ESD current at the I/O pad under PS-mode ESD stress is designed to be directly discharged through this additional ESD device to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through this ESD device to VSS power line, and then through the parasitic diode of power-rail ESD clamp circuit to the grounded VDD.

One ESD protection design with the additional substrate-triggered lateral n-p-n BJT device has been used to protect the mixed-voltage I/O circuits in a fully salicided, 0.35-μm, thin-epi CMOS process [45]. The ESD protection design with substrate-triggered circuit and the lateral n-p-n BJT device for the mixed-voltage I/O circuits is re-drawn in Fig. 2.4(a). The substrate-triggered circuit should meet the design constraints for providing effective ESD protection to the mixed-voltage I/O circuits, but without suffering the gate-oxide reliability issue. In this design, the substrate-triggered circuit is mainly composed of the diode string and a PMOS Mp1 to provide the substrate current for triggering on the lateral n-p-n BJT during ESD stress. A positive feedback network is formed with Mp2, Mn1, and R1, which maintains Mp1 in a highly conductive state to provide the substrate current during ESD stress. Moreover, to improve the turn-on efficiency of lateral n-p-n BJT device in a thin-epi CMOS process with much smaller substrate resistance (Rsub), the device structure of lateral n-p-n BJT is specifically designed in Fig. 2.4(b). The lateral n-p-n BJT device consists of an n+ diffusion (emitter), an n-well (collector), and a p+ diffusion as its base. A dummy gate is formed between the p+ base and n+ emitter regions. The collector n-well encloses a portion of the p+ base region. In this design, the HBM ESD level of the mixed-voltage I/O circuits has been verified greater than 2kV in a fully-salicided thin-epi CMOS process.

Another ESD protection design, by using the additional stacked-NMOS triggered silicon controlled rectifier (SNTSCR), has been reported to protect the mixed-voltage I/O circuits [46]. The ESD protection design with the additional SNTSCR device for protecting the mixed-voltage I/O circuits is shown in Fig. 2.5(a). The device structure of SNTSCR and the corresponding ESD detection circuit are shown in Fig. 2.5(b). The ESD detection circuit, designed by using the gate-coupled technique with consideration of the gate-oxide reliability issue, is used to provide suitable gate bias to trigger on the SNTSCR device under ESD stress condition. On the contrary, this ESD detection circuit must keep the SNTSCR off when the IC is under normal circuit operating condition. During normal circuit operating condition, the Mn3 in Fig. 2.5(b) acts as a resistor to bias the gate voltage (Vg1) of Mn1 at VDD. But, the gate of Mn2 is grounded through the resistor R2 and Mn4. So, all the devices in the ESD protection circuit can meet the electrical-field constraint of gate-oxide reliability under normal circuit operating condition. Under PS-mode ESD stress condition, the Mp1 is turned on but Mn3 is off since the initial voltage level on the floating VDD line is ~0V. The capacitors C1 and C2 are designed to couple ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed greater than the threshold voltage of NMOS to turn on Mn1 and Mn2 for triggering on the SNTSCR device, before the devices in the mixed-voltage I/O circuit are damaged by ESD stress. With the gate-coupled circuit technique, the trigger voltage of SNTSCR can be significantly reduced, so the SNTSCR can be quickly triggered on to discharge ESD current. By changing the connection of the ESD protection circuit from the I/O pad to the floating n-well of the pull-up PMOS in the mixed-voltage I/O circuit, the SNTSCR device can have a high enough noise margin to the overshooting glitch on the I/O pad, during the normal circuit operating condition. From the experimental results in a 0.35-μm CMOS process, the HBM ESD level of the mixed-voltage I/O circuits with this ESD protection design has been greatly improved up to 8kV, as compared with that (~2kV) of the original mixed-voltage I/O circuits with only stacked NMOS device.

2.3 Extra ESD Protection Device Between I/O Pad and VDD

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and VDD power line [47]–[49]. The ESD current at the I/O pad under PS-mode ESD stress is designed to be discharged through this additional ESD device to VDD power line, and then through the power-rail ESD clamp circuit to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be directly discharged through this additional ESD device to the grounded VDD.

Because the diode in forward-biased condition can sustain much higher ESD current, the diode string has been used for protecting the mixed-voltage I/O circuits [47], [48], or used to realize the power-rail ESD clamp circuit [50]. The ESD protection design with the diode string connected between the I/O pad and VDD power line for the mixed-voltage I/O circuits is shown in Fig. 2.6. The number of diodes in the diode string is determined by the voltage difference between the maximum input voltage at I/O pad and the VDD supply voltage. To reduce the turn-on resistance from I/O pad to VDD during ESD stress, the area of such diodes has to be scaled up by the number of the diodes in stacked configuration. The major concern of using the diode string for ESD protection in the mixed-voltage I/O circuits is the leakage current. While the mixed-voltage I/O circuit is operating at a high-temperature environment with a high-voltage input signal, the forward-biased leakage current from the I/O pad to VDD through the stacked diodes could trigger on the parasitic vertical p-n-p BJT devices in the diode string. The Darlington bipolar amplification of these parasitic p-n-p BJT devices in the diode string will induce a large leakage current into the substrate. In Fig. 2.6, an additional snubber diode (SD) was used to reduce the leakage current due to the Darlington bipolar amplification in the diode string [47], [48].

Another ESD protection design, by using the gated p-n-p BJT as the additional ESD device connected between I/O pad and VDD, has been designed to protect the mixed-voltage I/O circuits [49], as that shown in Fig. 2.7. In this ESD protection design, the PMOS Mp1 acting as ESD clamp device should be kept off to avoid the leakage current path during normal circuit operating condition. Under PD-mode ESD stress condition, the parasitic lateral p-n-p BJT in the device structure of Mp1 is turned on to discharge ESD current. In the 3.6V/5V mixed-voltage IC application, when the input voltage at I/O pad is 0V, the n-well voltage and gate voltage of Mp1 is clamped at VDD (3.6V) through the turn-on of Mp2 and Mp4. When the input voltage at I/O pad is 5V, the n-well voltage of Mp1 is maintained at 5-Vd (where Vd is the cut-in voltage of the parasitic drain-to-well diode), and the gate voltage of Mp1 is clamped at 5V through the turn-on of Mp3. Therefore, this design can meet the gate-oxide reliability constraints without leakage current path from I/O pad to VDD during normal circuit operating condition. Under ESD stress condition, the parasitic lateral p-n-p BJT in Mp1 is turned on to discharge ESD current by avalanche breakdown. Such a gated p-n-p BJT should be designed to effectively clamp the overstress ESD pulse without causing ESD damage in the mixed-voltage I/O circuits.

2.4 ESD Protection Design with ESD Bus

The ESD protection scheme by using the additional ESD bus for the IC with power-down-mode application has been reported in [51]. Such design concept with ESD bus can be used to form the ESD protection network for the mixed-voltage I/O circuits, as shown in Fig. 2.8. The additional ESD bus line is realized by a wide metal line in CMOS IC [51], [52]. To save layout area, the ESD bus can be realized by the different metal layer, which overlaps the VDD power line. The ESD bus is not directly connected to an external power pin, but initially biased to VDD through the diode D1 in Fig. 2.8. The diode D1 connected between the VDD power line and ESD bus is also used to block the leakage current path from the I/O pad to VDD during normal circuit operating condition with a high-voltage input signal. The diode Dp is connected between I/O pad and ESD bus, whereas the diode Dn is connected between VSS power line and I/O pad. One (the first) power-rail ESD clamp circuit is connected between VDD power line and VSS power line. Another (the second) power-rail

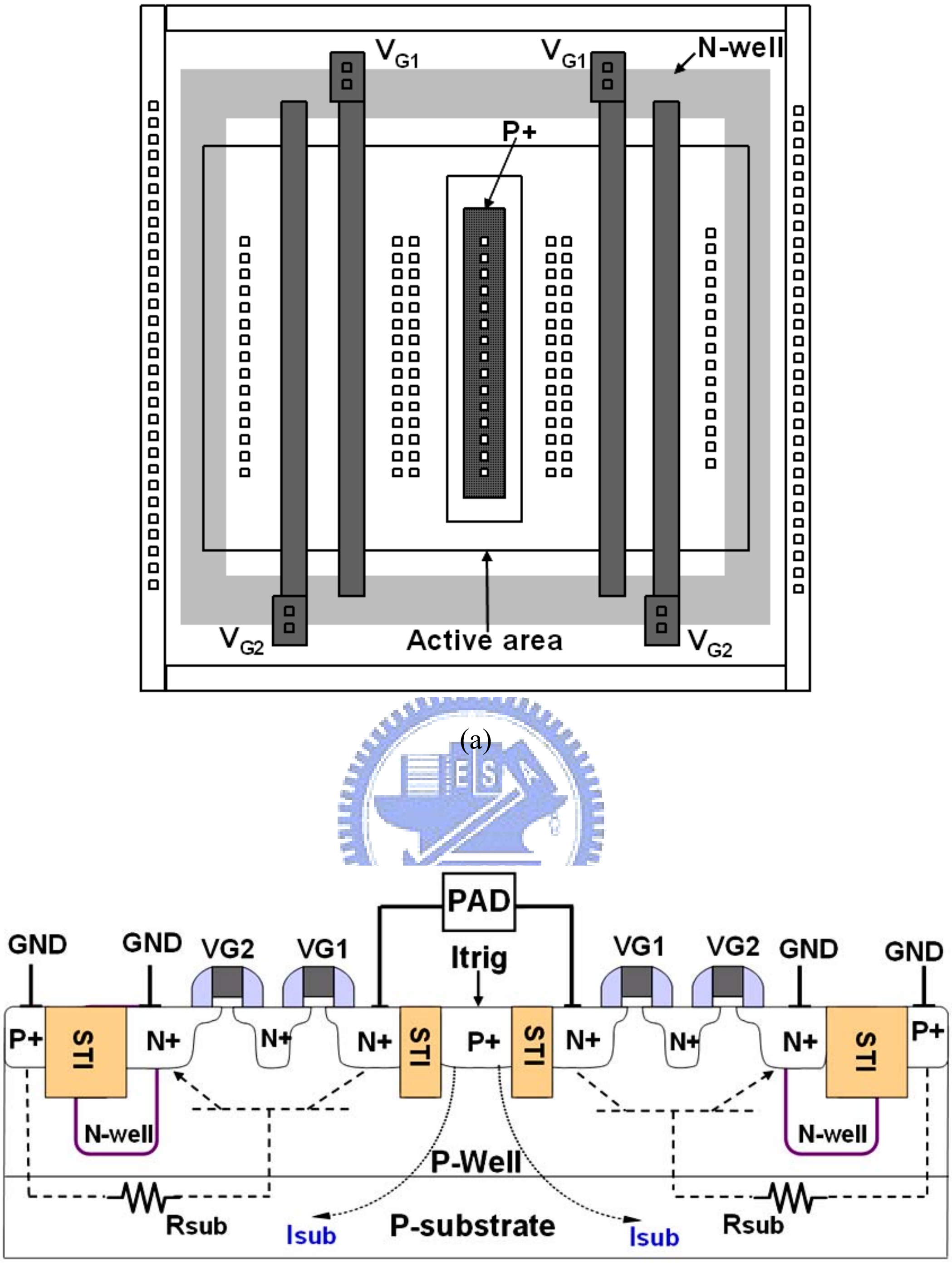
ESD clamp circuit is connected between the ESD bus and VSS power line. The second power-rail ESD clamp circuit connected between ESD bus and VSS power line should be designed with high-voltage-tolerant constraints without suffering the gate-oxide reliability issue. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode Dp to the ESD bus, and then through the second power-rail ESD clamp circuit to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through the diode Dp to the ESD bus, the second power-rail ESD clamp circuit to VSS power line, and then through the parasitic diode of the first power-rail ESD clamp circuit to the grounded VDD. With the turn-on-efficient power-rail ESD clamp circuits, high ESD level for the mixed-voltage I/O circuits can be achieved by this ESD protection scheme with ESD bus. Here, the design key point is how to design such a high-voltage-tolerant power-rail ESD clamp circuit with only low-voltage thin-oxide CMOS devices.

2.5 Special Applications

For high-frequency and analog circuit applications, the high-voltage-tolerant ESD protection design should meet the constraint of low parasitic capacitance. The traditional analog ESD protection with double diodes connected between I/O pad and VDD/VSS power lines [53] cannot meet the high-voltage tolerant requirement. A high-voltage-tolerant ESD protection design, by using the forward-biased diode in series with the stacked-NMOS device, has been reported for analog ESD protection to reduce the input parasitic capacitance [54], as shown in Fig. 2.9. The equivalent capacitance of analog pin in this design is approximate the junction capacitance of D1 plus the junction capacitance of D2. The diodes D1 and D2 can be drawn with small layout area, because the ESD current is discharged through these diodes under forward-biased condition. Therefore, the total parasitic input capacitance seen by the analog pin was reduced. The gates of Mn1 and Mn3 are connected to VDD to meet the gate-oxide reliability. The gates of Mn2 and Mn4 are grounded by the dynamic-floating-gate technique [55] to improve turn-on uniformity among the multiple fingers of the stacked NMOS device. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode D1 and the parasitic n-p-n BJT of stacked-NMOS (Mn3 and Mn4) to the grounded VSS. The ESD current at the I/O pad under PD-mode ESD stress can be discharged through the diode D1 and the parasitic n-p-n BJT of stacked-NMOS (Mn1 and Mn2) to the grounded VDD. Because the ESD current is discharged through the stacked-NMOS device by snapback breakdown in this design, the turn-on efficiency and ESD robustness of stacked-NMOS devices (Mn1–Mn4) need to be further improved by the additional ESD-implantation process [56].

2.6 Summary

A comprehensive overview on the ESD protection designs have been discussed for the mixed-voltage I/O circuits without suffering the gate-oxide reliability issue. To improve ESD level of the mixed-voltage I/O circuits, the ESD protection design without increasing the process complexity is strongly requested by the mixed-voltage I/O circuits in consumer IC products. Such ESD protection design in the mixed-voltage I/O circuits still meets the gate-oxide reliability constraints, and needs to prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current. To design the efficient ESD protection circuit for the mixed-voltage I/O circuits with low parasitic capacitance for high-speed I/O applications and low standby leakage current for low-power applications will continually be an important challenge to SOC implementation in the nanoscale CMOS technology.



(a)

(b)

Fig. 2.1 (a) Finger-type layout pattern, and (b) the corresponding cross-sectional view, of the substrate-triggered stacked-NMOS device for mixed-voltage I/O circuits.

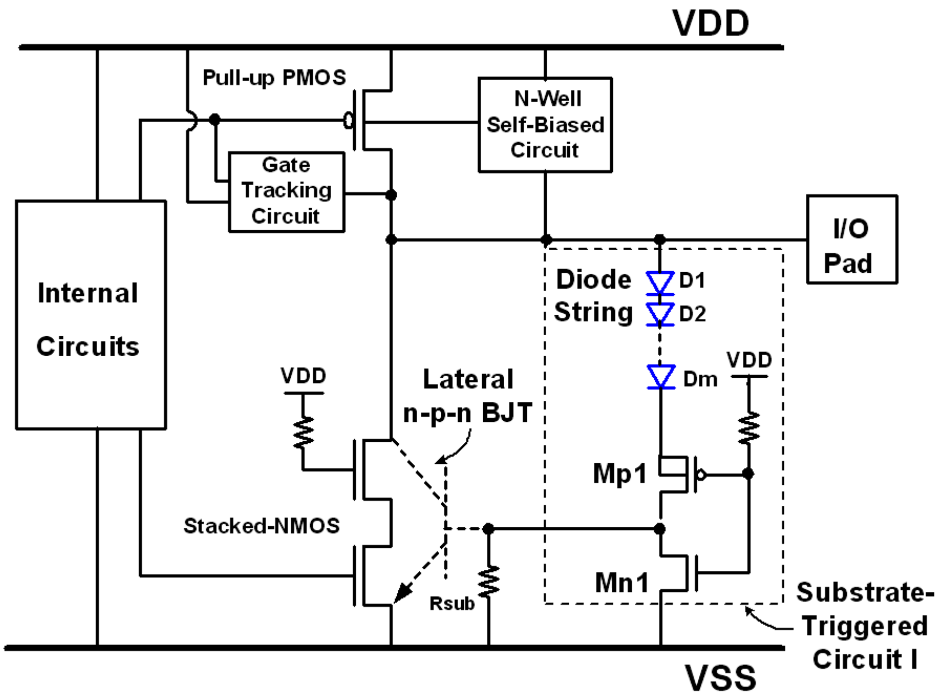


Fig. 2.2 Schematic circuit diagram of the substrate-triggered stacked-NMOS device with substrate-triggered circuit I for the mixed-voltage I/O circuits.

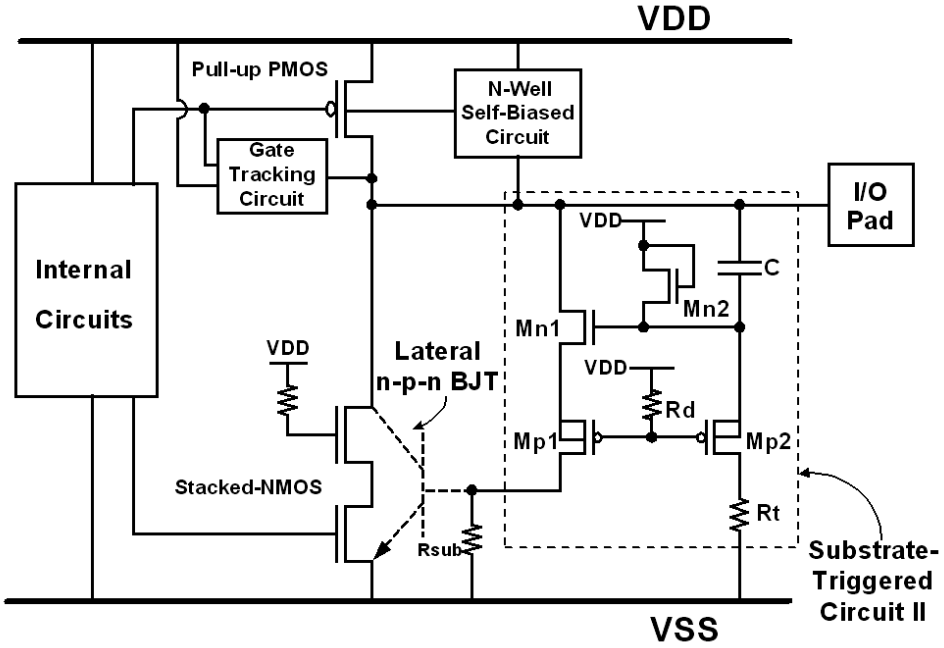


Fig. 2.3 Schematic circuit diagram of the substrate-triggered stacked-NMOS device with substrate-triggered circuit II for the mixed-voltage I/O circuits.

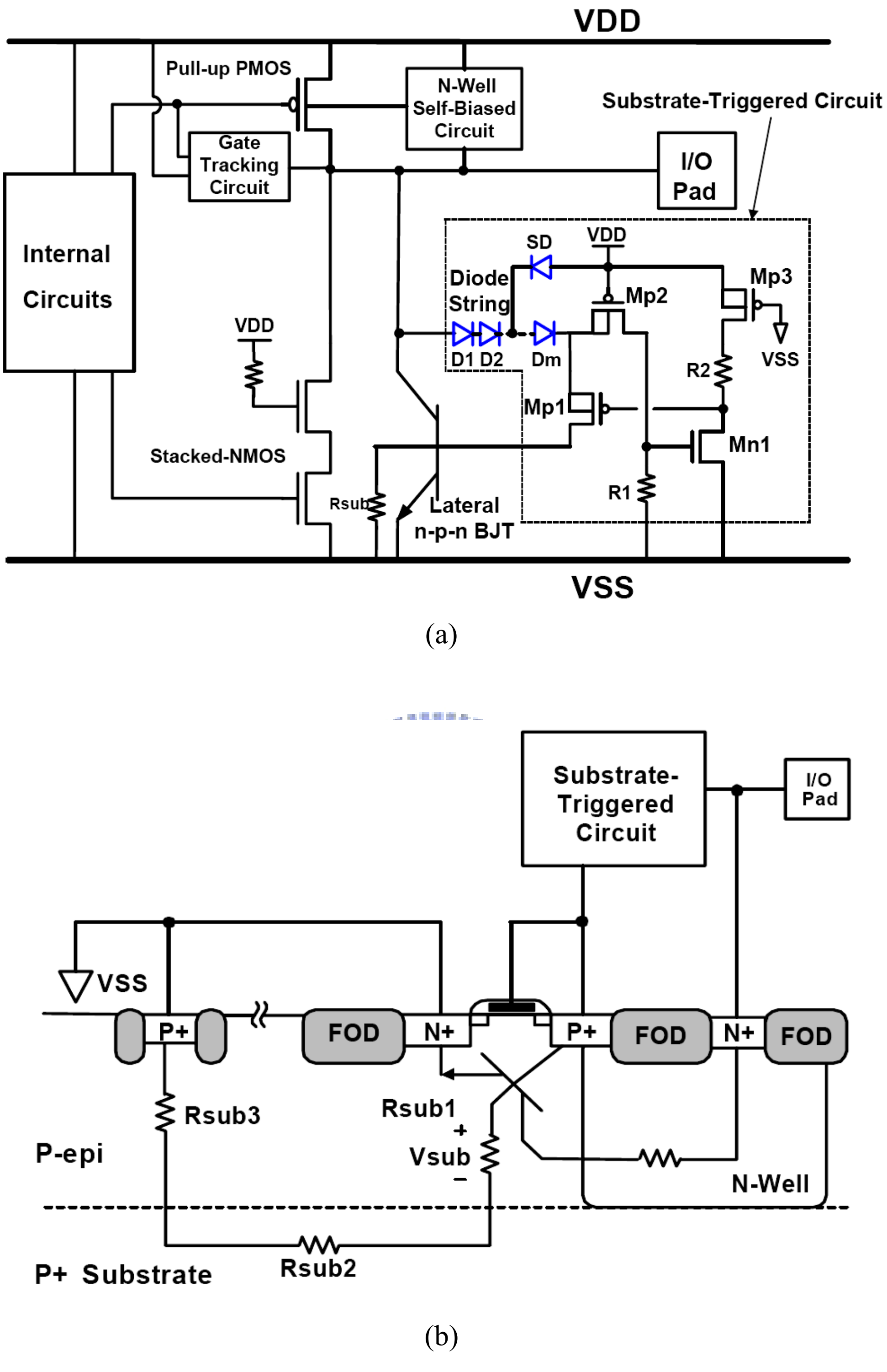


Fig. 2.4 (a) ESD protection design with substrate-triggered lateral n-p-n BJT device to protect the mixed-voltage I/O circuits. (b) Cross-sectional view of the lateral n-p-n BJT device in a thin-epi CMOS process.

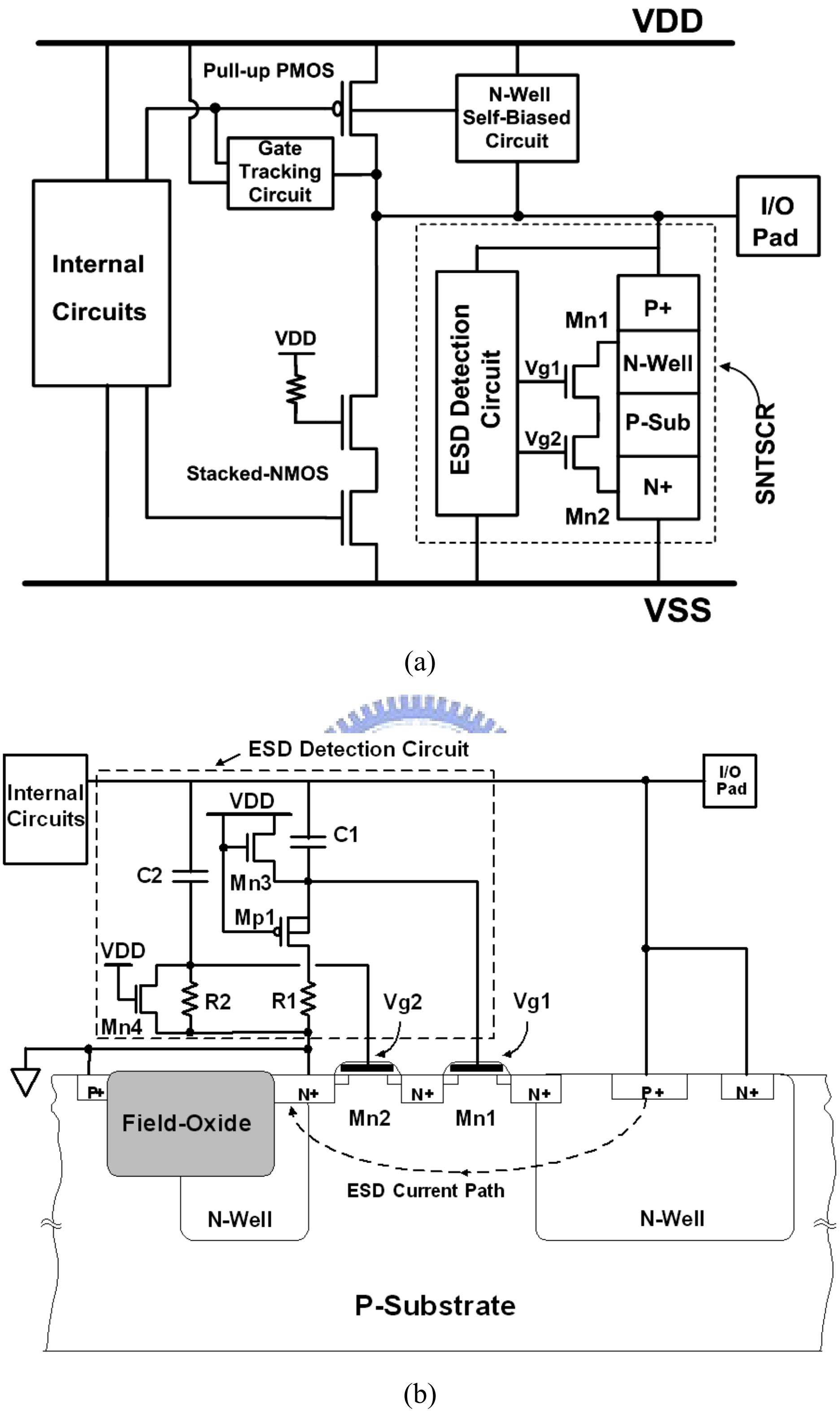


Fig. 2.5 (a) ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O circuits. (b) Realizations of the SNTSCR device and the ESD detection circuit with the gate-coupling technique to trigger on the SNTSCR device.

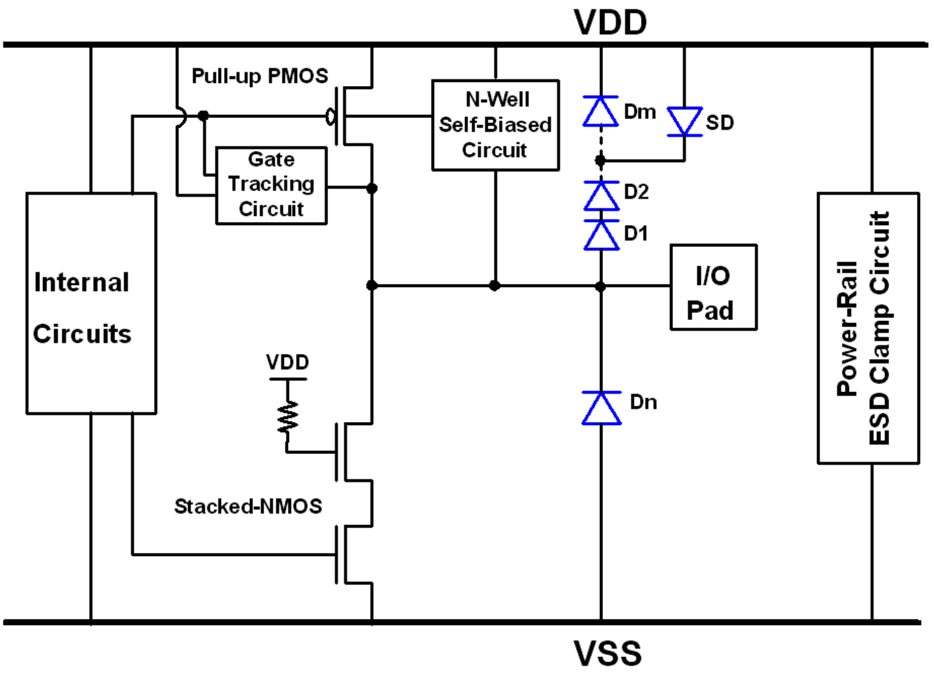


Fig. 2.6 ESD protection design with the diode string connected between the I/O pad and VDD power line to protect the mixed-voltage I/O circuits.

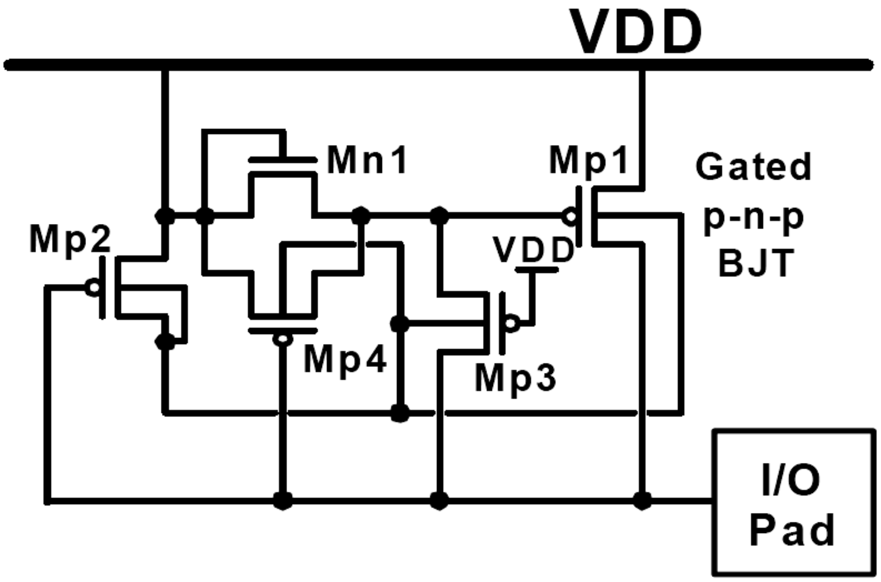


Fig. 2.7 ESD protection design with gated p-n-p BJT as the ESD clamp device connected between I/O pad and VDD to protect the mixed-voltage I/O circuits.

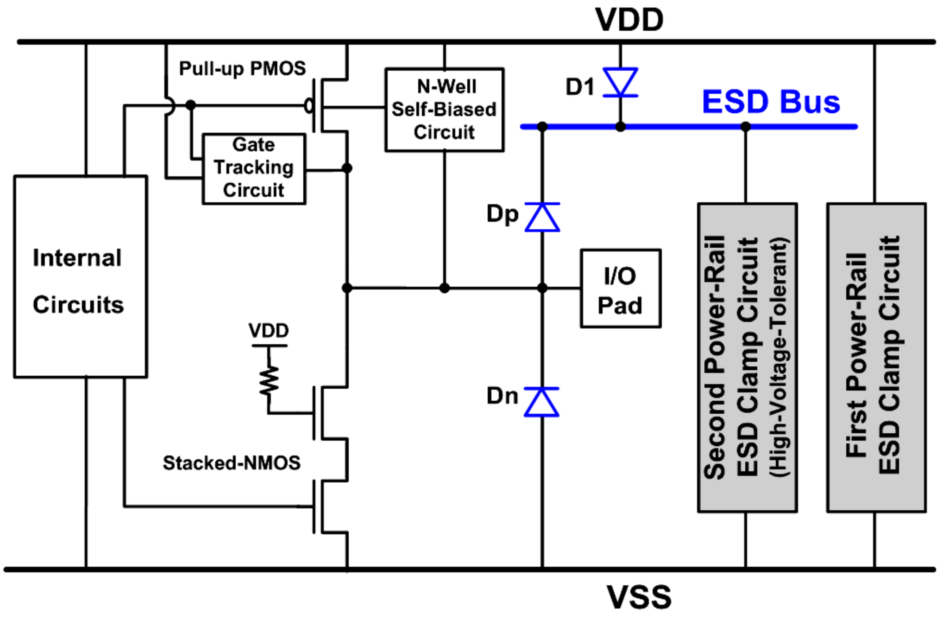


Fig. 2.8 The ESD protection network with the additional ESD bus line for the mixed-voltage I/O circuits. One power-rail ESD clamp circuit is connected between VDD power line and VSS power line. A second power-rail ESD clamp circuit is connected between ESD bus line and VSS power line.

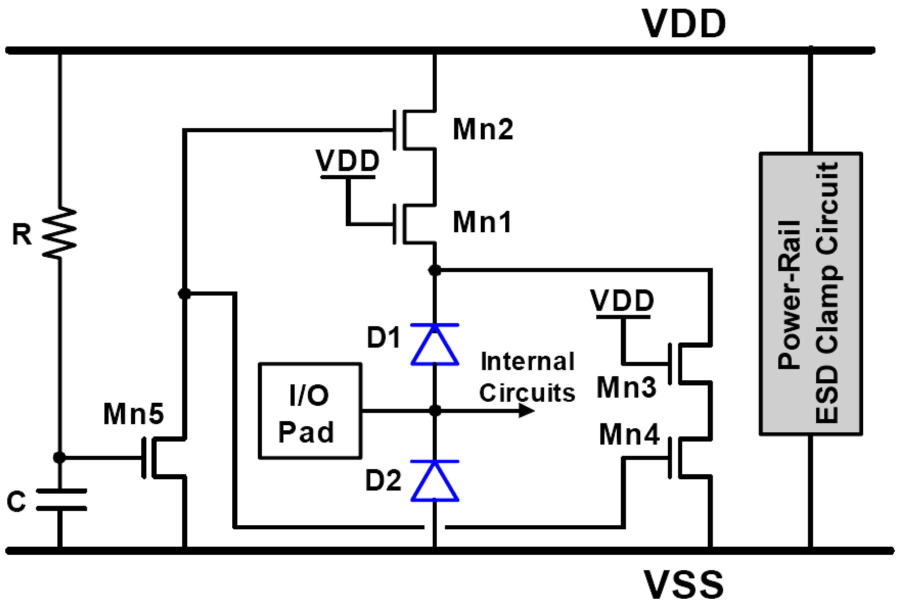


Fig. 2.9 High-voltage-tolerant ESD protection design with the forward-biased diode in series with one stacked NMOS for analog ESD protection to reduce the input parasitic capacitance.

CHAPTER 3

ESD PROTECTION DESIGN WITH LOW-VOLTAGE-TRIGGERED PNP (LVTPNP) DEVICES FOR MIXED-VOLTAGE I/O INTERFACE

In this chapter, ESD protection design for mixed-voltage I/O interfaces with the low-voltage-triggered PNP (LVTPNP) device in CMOS technology is proposed [57]. The LVTPNP, by inserting N+ or P+ diffusion across the junction between N-well and P-substrate of the PNP device, is designed to protect the mixed-voltage I/O interfaces for signals with voltage levels higher than VDD (over-VDD) and lower than VSS (under-VSS). The LVTPNP devices with different structures have been investigated and compared in CMOS processes. The experimental results in a 0.35-μm CMOS process have proven that the ESD level of the proposed LVTPNP is higher than that of the traditional PNP device. Furthermore, layout on LVTPNP device for ESD protection in mixed-voltage I/O interfaces is also optimized in this work. The experimental results verified in both 0.35-μm and 0.25-μm CMOS processes have proven that the ESD levels of the LVTPNP drawn in the multi-finger layout style are higher than that drawn in the single finger layout style. Moreover, one of the LVTPNP devices drawn with the multi-finger layout style has been used to successfully protect the input stage of an ADSL IC in a 0.25-μm salicided CMOS process [57].

3.1 ESD Protection with LVTPNP Device

Due to the limitation on placing ESD diode between the input pad and VDD/VSS power lines for the mixed-voltage I/O interface with over-VDD and under-VSS signal levels, a new ESD protection design with LVTPNP device is shown in Fig. 3.1. The LVTPNP device is connected between the input pad and VSS power line, which provides ESD protection for such mixed-voltage I/O interface. With the help of power-rail ESD clamp circuit [8], the positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) ESD stresses on the input pin can be discharged through the LVTPNP to VSS or VDD with the cooperation of power-rail ESD clamp circuit.

3.1.1 Device Structures and TLP-Measured I-V Characteristics

The cross-sectional view of the traditional PNP device in N-well/P-substrate CMOS process is shown in Fig. 3.2(a), where the N-well is floating in this structure to avoid the leakage path from the pad to grounded P-substrate. The P+ diffusion (emitter) in the floating N-well is connected to the I/O pad for ESD protection. By inserting N+ or P+ diffusion across the junction between N-well and P-substrate of the traditional PNP device, five new different structures of LVTPNP devices in Figs. 3.2(b) ~ 3.2(f) are proposed and investigated to find the optimized design for ESD protection [57]–[59].

Compared to the breakdown voltage of gate oxide, the junction between P+ diffusion and N-well in the traditional PNP device has a low breakdown voltage since the P+ diffusion region is heavily doped. But, the junction between N-well and P-substrate has high breakdown voltage since both of them are lightly doped. The junction between N-well and P-substrate with high breakdown voltage is disadvantageous to ESD protection. In Fig. 3.2(b), an N+ diffusion is inserted across the junction between the N-well and P-substrate. This structure is similar to the traditional PNP device but with a lower breakdown voltage across the base-collector junction, which is called as the type1 LVTPNP. The inserted N+ diffusion is floated to avoid the leakage current paths from the pad to VSS or VDD for application in the mixed-voltage I/O interfaces. Thus, under the normal circuit operation condition, only one of the P/N or N/P junctions in the LVTPNP device could be forward biased to eliminate current leakage path. The inserted N+ diffusion with n-type heavily doped region to the P-substrate has a lower breakdown voltage, which avalanches earlier than the junction between N-well and P-substrate to discharge ESD current.

In Fig. 3.2(c), the P+ diffusion instead of N+ diffusion is inserted in the PNP structure to become the type2 LVTPNP, where the P+ diffusion across the N-well/P-substrate junction is used to reduce the breakdown voltage across the base-collector junction of the LVTPNP. Because of the floating base (N-well), the two separated P+ diffusions in Fig. 3.2(c) can be further merged into one single P+ diffusion to form the type3 LVTPNP in Fig. 3.2(d). The heavily doped P+ diffusion across the N-well/P-substrate junction in Fig. 3.2(d) is also used as the contact region for P-substrate.

In Fig. 3.2(e), compared with the type1 LVTPNP in Fig. 3.2(b), the field-oxide region between N+ diffusion and P+ diffusion in P-substrate is replaced by a floating polygate to become the gated1 LVTPNP. In general CMOS process, the minimum design rule of the polygate is shorter than that of the field oxide isolation. With the dummy polygate, the clearance (marked as L_1) between the N+ and P+ diffusions can be realized with the minimum design rule. Moreover, the replacement of field oxide with polygate can change the current path from the bottom of field oxide to the surface of the channel under the polygate. This will result in a smaller turn-on resistance to quickly discharge ESD current. In Fig. 3.2(f), compared with the gated1 LVTPNP in Fig. 3.2(e), the field oxide between N+ diffusion and P+ diffusion in N-well is replaced by another floating polygate (marked with a gate length of L_2) to become the gated2 LVTPNP. The replacement of field oxide with polygate between the base and emitter will obtain a smaller turn-on resistance for ESD protection.

With the same device dimension of 30μm×30μm (the width is defined as 30μm) for all devices, the corresponding TLP-measured I-V curves among those devices under PS-mode and NS-mode ESD-stress conditions are shown in Fig. 3.3(a) and 3.3(b), respectively. The first breakdown voltage (Vt1), the first breakdown current (It1), the second breakdown voltage (Vt2), and the second breakdown current (It2) of these devices are summary at Table 3.1. Under PS-mode ESD-stress condition, the Vt1 of the LVTPNP devices is indeed lower than that of the traditional PNP device. The It2 of LVTPNP devices is indeed higher than that of the traditional PNP device. Under NS-mode ESD-stress condition, the Vt1 of the LVTPNP devices and the traditional PNP device are almost the same because the breakdown region of all the devices occurs at the E-B junction (P+/N-well). The It2 among theses devices are somewhat different, which could be caused from the different current distribution along the devices of different structures during ESD stress. Basically, the device with the more effective device width will present a higher ESD robustness. To further improve ESD level of such LVTPNP devices, the layout to increase effective device width will be studied and optimized in the next section.

3.1.2 Layout Parameters of LVTPNP Devices on HBM ESD Levels

Under 0.35-μm CMOS process without any extra mask layer, the ESD levels among the proposed LVTPNP devices with different layout parameters are compared in Figs. 3.4(a) ~ 3.4(g). The layout parameters include the width or spacing, L_E, L_C, X, Y, S, L_1, and L_2, which have been indicated in Figs. 3.2(a) ~ 3.2(f). For the gated2 LVTPNP device, the L_1 and L_2 are changed simultaneously in the layout.

In Figs. 3.4(a) and 3.4(b), as the width of the LVTPNP devices increasing, the HBM ESD levels are improved under both positive-to-VSS and negative-to-VSS ESD-stress conditions. This confirms that when the area of effective ESD current flow from emitter to collector is increased, the heat will be dissipated through the larger region. Therefore, the device can sustain a higher ESD level.

In Fig. 3.4(c), as the spacing X of the type1 LVTPNP or the spacing Y of the type2 LVTPNP increasing, the HBM ESD level is improved under the positive-to-VSS ESD-stress condition. Here, the LVTPNP devices with the increase of X or Y will have a wider field oxide region in the device structures, but the N+ or P+ diffusion across the N-well/P-substrate junction is kept to have the same diffusion layout spacing of 1.2 μm. The TLP-measured I-V curves of the type1 LVTPNP with different X spacings and the type2 LVTPNP with different Y spacings are shown in Figs. 3.5(a) and 3.5(b), respectively. As these spacings increase, the clamped voltage across the devices will be increased due to the increased turn-on resistances. The voltage drop across the base-collector (B-C) junction will increase to cause the emitter-base (E-B) potential barrier to be lowered. The lowering potential barrier at the E-B junction produces a large increase in current with a very small increase in B-C voltage. This effect is the so-called punch-through breakdown phenomenon [60], which will occur before the avalanche breakdown. In Fig. 3.4(d), as the spacing S of the LVTPNP increasing, the HBM ESD level is improved under the negative-to-VSS ESD-stress condition. In this ESD-stress condition, however, the parameters S play the same role as parameters X and Y in positive-to-VSS ESD-stress condition. Because these spacings increase, the voltage drop across the base-emitter (B-E) junction will increase to cause the collector-base (C-B) potential barrier to be lowered. Therefore, the lowering potential barrier at the C-B junction produces a large increase in current but with a very small increase in B-E voltage. From such results, these spacings in LVTPNP devices can be further optimized in layout to improve ESD robustness for applications in such mixed-voltage I/O interfaces.

In Fig. 3.4(e), as the L_E of the LVTPNP devices increasing, the HBM ESD level is improved under negative-to-VSS ESD-stress condition. Because the heat will be located around the B-E junction, as the emitter junction area is increased, the heat will be dissipated through the larger region. However, under positive-to-VSS ESD-stress condition, this parameter has no influence to ESD level, because the heat will be located around the B-C junction with the same area in the test chips.

The parameter L_C of the LVTPNP devices almost has no influences to HBM ESD level. Under both positive-to-VSS and negative-to-VSS ESD-stress conditions, the heat will be located around B-C junction and B-E junction, respectively. However, the heat will not be located around the P+ diffusion in P-substrate.

In Fig. 3.4(f), as L_1 of the gated1 LVTPNP (L_1 and L_2 of the gated2 LVTPNP) increasing, the ESD level is improved under the positive-to-VSS ESD-stress condition. In Fig. 3.4(g), as L_1 and L_2 of the gated2 LVTPNP increasing, the ESD level is improved under the negative-to-VSS ESD-stress condition. However, in such ESD stress mode, the L_1 has no influence to ESD level of both gated1 LVTPNP and gated2 LVTPNP. Such layout parameters L_1 (L_2) in the gated LVTPNP play the same role as that of the parameters X (S) in the type1 LVTPNP, so as the parameters Y (S) in the type2 LVTPNP. By correctly adjusting the layout parameters, the desired ESD level of the mixed-voltage I/O interface can be achieved by the proposed LVTPNP devices with the optimized layout parameters.

3.1.3 Multi-Finger Layout Style for LVTPNP

The ESD robustness of LVTPNP device with the single finger layout style, which is shown in Fig. 3.6(a) and its cross-sectional view shown in Fig. 3.6(b), can't meet the ESD specification of 2-kV HBM ESD level in a limited silicon area. Therefore, based on the dependence of ESD levels on the layout parameters (including the width, L_E, L_C, X, Y, and S) of LVTPNP devices, the ESD level mainly depends on the effective device width from its emitter to its collector in both PS- and NS- mode ESD stresses. On the other hand, L_E affects only NS-mode ESD level and L_C doesn't affect the ESD level. However, comparing the PS- and NS-mode ESD levels, the PS-mode ESD level is critical. Considering the parameters of effective device width, L_E, and L_C, L_E and L_C are less sensitive to ESD level than the effective device width. Therefore, a more compact realization of the LVTPNP can be implemented by using the minimum spacing of the design rules for L_E and L_C in each finger layout. The LVTPNP realized by the multi-finger layout style is shown in Fig. 3.7(a), and its cross-sectional view is shown in Fig. 3.7(b), which will have more effective current flow for ESD protection. Here, due to complicated layout structure, the gated1 and gated2 LVTPNP devices are difficult to realize with multi-finger layout style. Hence, only the type 1, 2, and 3 LVTPNP devices were chosen to realize the multi-finger layout style

The LVTPNP devices drawn with the single finger layout style and the new proposed multi-finger layout style have been fabricated in both 0.35-μm polycided and 0.25-μm salicided CMOS processes without any extra additional mask layer. Under the positive-to-VSS ESD-stress condition, the HBM ESD levels of the LVTPNP devices with the singer finger layout style and the multi-finger layout style are compared in Table 3.2. In almost the same layout area (36μm×32μm v.s. 33.6μm×36.5μm), the LVTPNP devices with the multi-finger layout style have much higher ESD robustness than those with the single finger layout style in both 0.35-μm polycided and 0.25-μm salicided CMOS processes. Especially, the type3 LVTPNP with multi-finger layout has the highest ESD robustness, which can sustain HBM ESD stress of 3.6kV in the 0.35-μm polycided CMOS process and 1.4kV in the 0.25-μm salicided CMOS process. Furthermore, within unit layout area, the ESD robustness of type3 LVTPNP is increased from 0.5 V/μm^2 to 2.94V/μm^2 in the 0.35-μm polycided CMOS process and from 0.68 V/μm^2 to 1.14 V/μm^2 in the 0.25-μm salicided CMOS process.

Under the negative-to-VSS ESD-stress condition, the HBM ESD levels of the LVTPNP devices with the single finger layout style and the new multi-finger layout style are compared in Table 3.3. In almost the same layout area, the LVTPNP devices with the multi-finger layout style have much higher ESD robustness than those with the single finger layout style in both 0.35-μm polycided and 0.25-μm salicided CMOS processes. Especially, the type3 LVTPNP with multi-finger layout has the highest ESD robustness, which can sustain HBM ESD stress of a 3.3kV in the 0.35-μm polycided CMOS process and 3.8kV in the 0.25-μm salicided CMOS process. Furthermore, within unit layout area, the ESD robustness of type3 LVTPNP is increased from 0.59 V/μm^2 to 2.69V/μm^2 in the 0.35-μm polycided CMOS process and from 1.71 V/μm^2 to 3.10 V/μm^2 in the salicided 0.25-μm CMOS process. With suitable selection on the LVTPNP devices and layout style, the overall ESD robustness of the mixed-voltage I/O interfaces can be designed to meet the ESD specification of 2-kV HBM ESD level within a smaller silicon area. Especially, the LVTPNP in the type3 device structure with multi-finger layout style has the excellent ESD performance.

Because the doping concentration in the 0.25-μm salicided CMOS process is higher than that in the 0.35-μm polycided CMOS process, the junctions have slightly lower breakdown voltages in the 0.25-μm CMOS process than that in the 0.35-μm CMOS process. With the single finger layout style, HBM ESD levels of the LVTPNP devices in the 0.25-μm CMOS process are higher than those of the LVTPNP devices in the 0.35-μm CMOS process under both positive-to-VSS and negative-to-VSS ESD-stress conditions. Moreover, HBM

ESD levels of the LVTPNP devices in the 0.25-μm CMOS process are higher than those of the LVTPNP devices in the 0.35-μm CMOS process under negative-to-VSS ESD-stress condition, when they are drawn with the multi-finger layout style. However, HBM ESD levels of the LVTPNP devices in the 0.25-μm salicided CMOS process are lower than those of the LVTPNP devices in the 0.35-μm polycided CMOS process under positive-to-VSS ESD-stress condition for the multi-finger layout style. The silicided diffusion in the 0.25-μm salicided CMOS process causes degradation on ESD robustness of the LVTPNP device drawn in multi-finger layout style [61]. Under ESD stress condition, the silicide diffusion on the device will cause the current crowded on the surface of the device and the heat will be located in the local area. To further increase ESD level of the LVTPNP device in the 0.25-μm salicided CMOS process, the optional silicide-blocking mask layer can be used to block the silicide formation around the perimeter of emitter region of the LVTPNP device.

Moreover, the TLP-measured I-V curves of LVTPNP devices with the single finger layout style and the multi-finger layout style in 0.25-μm salicided CMOS process under PS-mode and NS-mode stress conditions are compared in Figs. 3.8(a) and 3.8(b), respectively. Due to the increase of total effective device width and the decrease of the length from its emitter to its collector, the LVTPNP devices with the multi-finger layout style have lower turn-on resistances than those with the single finger layout style in the same layout area. Hence, the It2 of LVTPNP devices with multi-finger layout style is higher than those with single finger layout style. For single finger layout style, however, because the turn-on resistance of the type3 LVTPNP is lower than those of the type1 and type2 LVTPNP, there will be a factor differences in the improved ESD levels of different types of LVTPNP in multi-finger layout. Hence, correlating with the same increase of effective device fingers will result in different increase factors of It2 of the type1 (type2) LVTPNP and type3 LVTPNP.

3.2 Application in ADSL Interface

3.2.1 ESD Protection Design with the LVTPNP for the Input Stage of ADSL

The LVTPNP devices are used in the input ESD protection circuit for the ADSL interface, which has a high-voltage signal level of 5V and a low-voltage signal level of -1V. The ESD protection design for such ADSL input stage is shown in Fig. 3.9(a), where the single-ended operational amplifier (opamp) with divider resistors is the input stage of ADSL.

The schematic of the single-ended opamp is shown in Fig. 3.9(b), which is composed with input differential stage (M_1~M_4), output stage (M_6, M_7, R_C, and C_C), and bias circuit (M_8~M_{10} and R_{bias}). In the 0.25-μm CMOS process with VDD of 2.5V, the voltage divider (R and R_f) with a ratio of thirty to one is used to scale down the ADSL input signals, when the input signals (between 5V and -1V) transmitted into ADSL IC. The V_{i2} is biased at the common reference voltage of 1.25V, which is half of VDD. The voltage divider is formed by R and R_f, which are designed to keep V_{i1} at the scaled-down voltage level and to make the single-ended opamp correct operation.

The TLP measurement of gate oxide breakdown voltage of NMOS is about 13V in the 0.25μm CMOS process. On the other hand, for LVTPNP devices, the breakdown voltages are about 7~9V. During TLP testing, no snapback characteristics are found due to the inefficient parasitic p-n-p bipolar gain, and the Vt2 will be higher than the gate oxide breakdown voltage, especially the type1 and type2 LVTPNP, shown in Fig. 3.8. In Fig. 3.9, for ADSL input stage, because the input signal will flow from R and R_f to V_o, the voltage level at the differential input will be divided by R and R_f. During ESD stress, if the divided voltage level on the differential input is larger than the gate oxide breakdown voltage of the input NMOS, the ESD stress will damage the gate oxide of the input NMOS. By using the proposed ESD protection design with LVTPNP, the ESD current will discharge through the LVTPNP device to VSS. Because the Vt2 of the LVTPNP is lower than the voltage drop on R pulsing the gate oxide breakdown voltage of NMOS, the gate oxide of the input NMOS can be successfully protected in this ADSL interface. By the way, the input node (V_{i1}) of the opamp in Fig. 3.9(a) is also connected to its output (V_o) through the feedback resistor R_f, which will also help to clamp the overshooting voltage on the gate oxide of the input stage. To reduce the Vt2 at a given current level, the device width should be further increased to have a lower turn-on resistance. Among the LVTPNP devices, the type3 LVTPNP is selected for input ESD protection design in ADSL interface due to its highest HBM ESD level. In Fig. 10, the type3 LVTPNP device is connected between input pad and VSS power line, and the power-rail ESD clamp circuit is realized by the RC-inverter-NMOS circuit [8]. The layout views of the ADSL input stage without and with ESD protection circuit are shown in Figs. 3.10(a) and 3.10(b), respectively. When ESD stress occurs to the input pin, the type3 LVTPNP will break down with a lower trigger voltage to discharge ESD current. With power-rail ESD clamp circuit, the PS, NS, PD, and ND ESD stresses can be discharged through the type3 LVTPNP to VSS or VDD. Under PS-mode ESD-stress condition, the ESD current will flow from input pad through LVTPNP to VSS. Under NS-mode ESD-stress condition, the ESD current will flow from VSS through LVTPNP to the input pad. Under PD-mode ESD-stress condition, the ESD current will flow from input pad through LVTPNP to VSS, and then through power-rail ESD clamp circuit to VDD. Under ND-mode ESD-stress condition, the ESD current will flow from VDD through power-rail ESD clamp circuit to VSS, and then through LVTPNP to the input pad. Therefore, under PS-mode and PD-mode ESD-stress conditions, HBM ESD levels will mainly determined by the LVTPNP in PS-mode ESD-stress condition. Under NS-mode and ND-mode ESD-stress conditions, HBM ESD levels will mainly determined by the LVTPNP in NS-mode ESD-stress condition.

3.2.2 HBM ESD Levels of ADSL with the Type3 LVTPNP

When applying a positive bias (with VSS grounded and VDD floating) to the input pad of ADSL, the current will flow from R and R_f to V_o, and then from V_o through the parasitic diode (drain-Nwell PN junction) of M_6 in the single-ended opamp to VDD, finally from the VDD through the path of M_3-M_1-M_5 to VSS or through the bias circuit to VSS. Due to the turn-on bias circuit, M_7 will turn on. Therefore, before ESD stress, there is current flow from input through the internal circuits to VSS when applying a signal to the input pad. Due to the reason of initial current, to compare the ESD protection ability, the input stage of ADSL without and with the ESD protection circuit has been tested in HBM ESD stress with the failure criterion of 30% shifting on the voltage at 1-μA current bias from its original I-V curve [62]–[64]. The typical I-V curves of the input stage of ADSL with ESD protection circuit before and after the HBM PS-mode ESD stress of 1.5kV are shown in Fig. 3.11, which was measured by applying a swept voltage from -1 to 5V on the input pad with VSS grounded and VDD floating. Before ESD stress, while the input pad is swept from 0 to 5V with grounded VSS (VDD floating), the signal paths will flow into the opamp circuit. Therefore, the I-V curve will become a straight line with a slope of reciprocal of R+R_f, which starts at the voltage drop of internal circuits. Moreover, before ESD stress, while the input pad is swept from 0 to -1V with grounded VSS (VDD floating), the input current will flow from VSS through the parasitic diode of M_7 in the single-ended opamp, and then through R_f and R to input pad. Therefore, the I-V curve will become a straight line with a slope of reciprocal of R+R_f, which starts at the cut-in voltage of the parasitic diode of M_7. However, after HBM ESD stress of 1.5kV, the type3 LVTPNP is burned out to cause a short circuit line in the I-V curve.

The input stage of ADSL protected by the type3 LVTPNP devices in the single finger layout style or the multi-finger layout style and the power-rail ESD clamp circuit has been fabricated in a 0.25-µm salicided CMOS process. The HBM ESD levels of ADSL input stage under PS-mode, NS-mode, PD-mode, and ND-mode ESD-stress conditions are shown in Table 3.4. The LVTPNP in single finger layout style is drawn with a device size of 36µm×32µm, whereas the LVTPNP in the multi-finger layout style is drawn with a device size of 33.6µm×36.5µm. As seen in Table 3.4, with the type3 LVTPNP and the power-rail ESD clamp circuit, the input stage of ADSL indeed can be protected from ESD stress. Moreover, HBM ESD levels of input stage of ADSL protected by the LVTPNP in multi-finger layout style are higher than those of input stage of ADSL protected by the LVTPNP in single finger layout style. To further increase ESD level, the layout area of LVTPNP should be increased with the multi-finger layout style. Or, the silicide-blocking mask layer should be used to block the silicide formation around the perimeter of emitter region of the LVTPNP device.

3.2.3 Failure Analysis

The EMMI (photon emission microscope) picture of ADSL input stage without ESD protection circuit after HBM PS-mode ESD stress of 500V is shown in Fig. 3.12. The ESD damage, indicated by the arrow, is located on the opamp of ADSL input stage.

In the layout of ADSL input stage protected by LVTPNP, the type3 LVTPNP is fully covered by the metal layers on the top. The ESD damage on the device junction can't be observed by the EMMI picture. Here, the OBIRCH (optical beam induced resistance change) [65], [66] is used to find the ESD damage location on the input stage of ADSL with ESD protection circuit after HBM PS-mode ESD stress. The OBIRCH picture shown in Fig. 3.13 indicates the ESD damage located on the type3 LVTPNP device after 1.5-kV HBM PS-mode ESD stress. From the failure location in Fig. 3.13, the type3 LVTPNP indeed is triggered on to conduct ESD current to effectively protect the mixed-voltage I/O interface of ADSL input stage.

3.3 Summary

ESD protection design for the mixed-voltage I/O interfaces with new proposed

LVTPNP devices has been successfully verified to achieve a good ESD protection in a 0.35-μm CMOS process. The proposed LVTPNP devices have the higher ESD level than that of the traditional PNP device. Moreover, the multi-finger layout style has been used to increase the effective device width among the LVTPNP device for improving ESD robustness in both 0.35-μm and 0.25-μm CMOS processes. Comparing among these LVTPNP devices, the type3 LVTPNP in the multi-finger layout style can sustain the highest ESD stress for application in the mixed-voltage I/O interfaces. ESD protection co-designed with the LVTPNP device and the power-rail ESD clamp circuit has been successfully implemented to protect the ADSL input stage in a 0.25-μm salicided CMOS process.

Table 3.1

Breakdown voltage and breakdown current of the LVTPNP devices under both positive-to-VSS and negative-to-VSS ESD-stress conditions.

Device Type	PS-mode (positive-to-VSS)				NS-mode (negative-to-VSS)			
	Vt1 (V)	It1 (A)	Vt2 (V)	It2 (A)	Vt1 (V)	It1 (A)	Vt2 (V)	It2 (A)
PNP	31	0.01	80	0.08	10	0.01	27	0.65
Type1	10	0.02	24	0.14	10	0.01	24	0.6
Type2	9	0.03	24	0.17	9	0.02	16	0.46
Type3	9	0.02	12	0.24	8	0.01	12	0.33
Gated1	10	0.03	20	0.18	8	0.02	22	0.56
Gated2	10	0.02	21	0.21	8	0.01	21	0.55

Table 3.2

HBM ESD Levels of the LVTPNP devices with different layout styles under positive-to-VSS ESD-stress condition.

Device Layout Style	**Type1 Single Finger Layout**	**Type2 Single Finger Layout**	**Type3 Single Finger Layout**	**Type1 Multi-Finger Layout**	**Type2 Multi-Finger Layout**	**Type3 Multi-Finger Layout**
Layout Area (µm×µm)	**36×32**	**36×32**	**36×32**	**33.6×36.5**	**33.6×36.5**	**33.6×36.5**
HBM ESD Level (V) in a 0.35-µm CMOS Process	**250**	**350**	**550**	**950**	**1050**	**3.6k**
HBM ESD Level (V) in a 0.25-µm CMOS Process	**350**	**350**	**750**	**850**	**900**	**1.4k**
V_{ESD}/Area ($V/\mu m^2$) in a 0.35-µm CMOS Process	**0.22**	**0.3**	**0.5**	**0.77**	**0.86**	**2.94**
V_{ESD}/Area ($V/\mu m^2$) in a 0.25-µm CMOS Process	**0.3**	**0.3**	**0.68**	**0.69**	**0.73**	**1.14**

Table 3.3

HBM ESD Levels of the LVTPNP devices with different layout styles under negative-to-VSS ESD-stress condition.

Device Layout Style	**Type1 Single Finger Layout**	**Type2 Single Finger Layout**	**Type3 Single Finger Layout**	**Type1 Multi-Finger Layout**	**Type2 Multi-Finger Layout**	**Type3 Multi-Finger Layout**
Layout Area (μm×μm)	**36×32**	**36×32**	**36×32**	**33.6×36.5**	**33.6×36.5**	**33.6×36.5**
HBM ESD Level (V) in a 0.35-μm CMOS Process	**1.2k**	**700**	**650**	**2.6k**	**2.4k**	**3.3k**
HBM ESD Level (V) in a 0.25-μm CMOS Process	**2.4k**	**2.2k**	**1.9k**	**2.7k**	**2.8k**	**3.8k**
V_{ESD}/Area (V/μm^2) in a 0.35-μm CMOS Process	**1.04**	**0.61**	**0.59**	**2.12**	**1.96**	**2.69**
V_{ESD}/Area (V/μm^2) in a 0.25-μm CMOS Process	**2.08**	**1.91**	**1.71**	**2.20**	**2.28**	**3.10**

Table 3.4

HBM ESD Levels of ADSL input stage with different ESD protection designs under PS-mode, NS-mode, PD-mode, and ND-mode ESD-stress conditions.

	PS-Mode (Positive-to-VSS)	**NS-Mode** (Negative-to-VSS)	**PD-Mode** (Positive-to-VDD)	**ND-Mode** (Negative-to-VDD)
ADSL Only	**450V**	**350V**	**450V**	**400V**
ADSL Including the Type3 LVTPNP with Single Finger Layout Style	**750V**	**1.9kV**	**750V**	**1.9kV**
ADSL Including the Type3 LVTPNP with Multi-Finger Layout Style	**1.4kV**	**3.8kV**	**1.3kV**	**3.8kV**

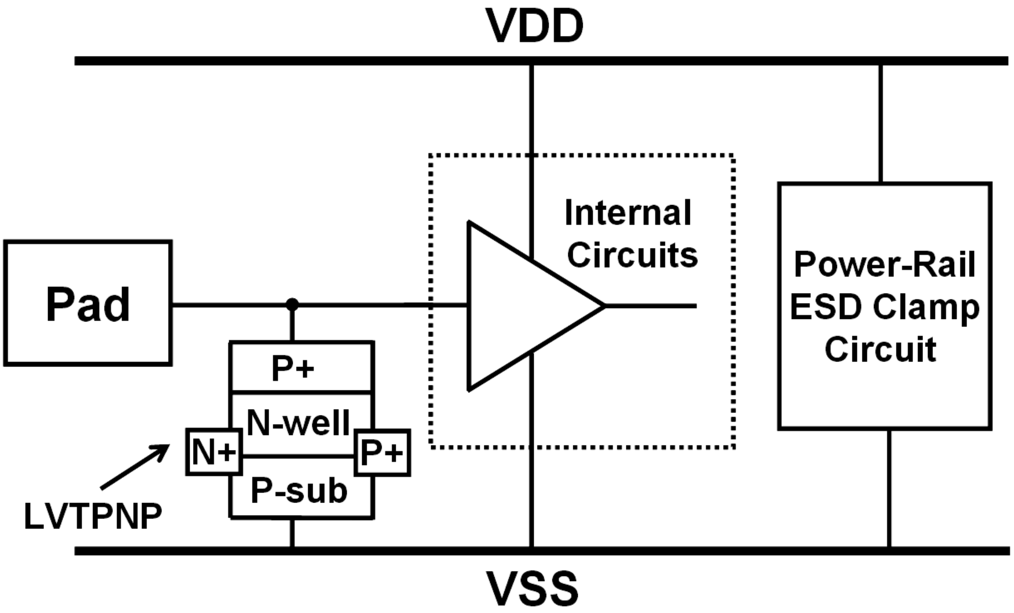
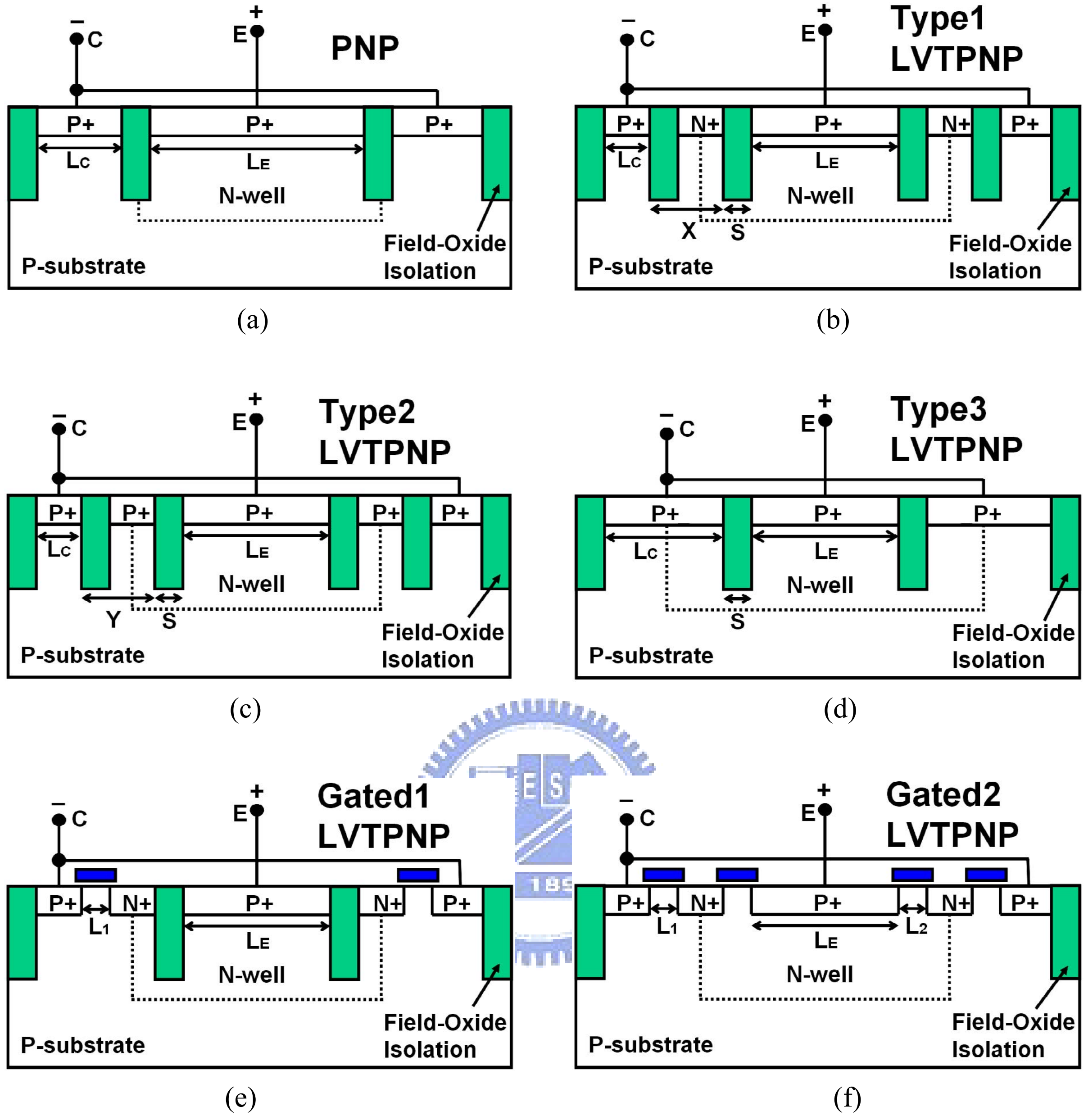
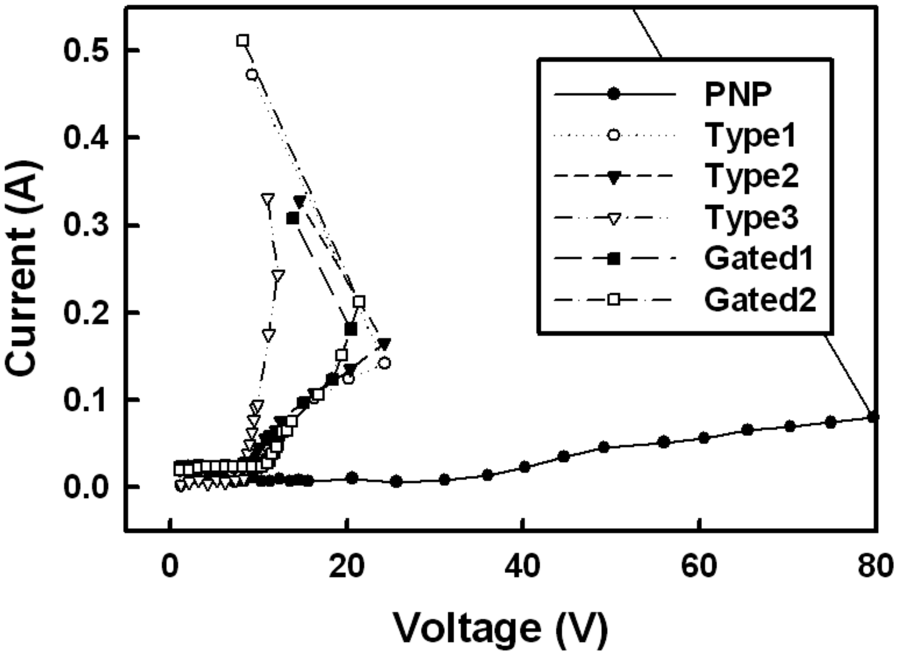


Fig. 3.1 The new proposed ESD protection design with LVTPNP device for the mixed-voltage I/O interface with input voltage levels higher than VDD and lower than VSS.

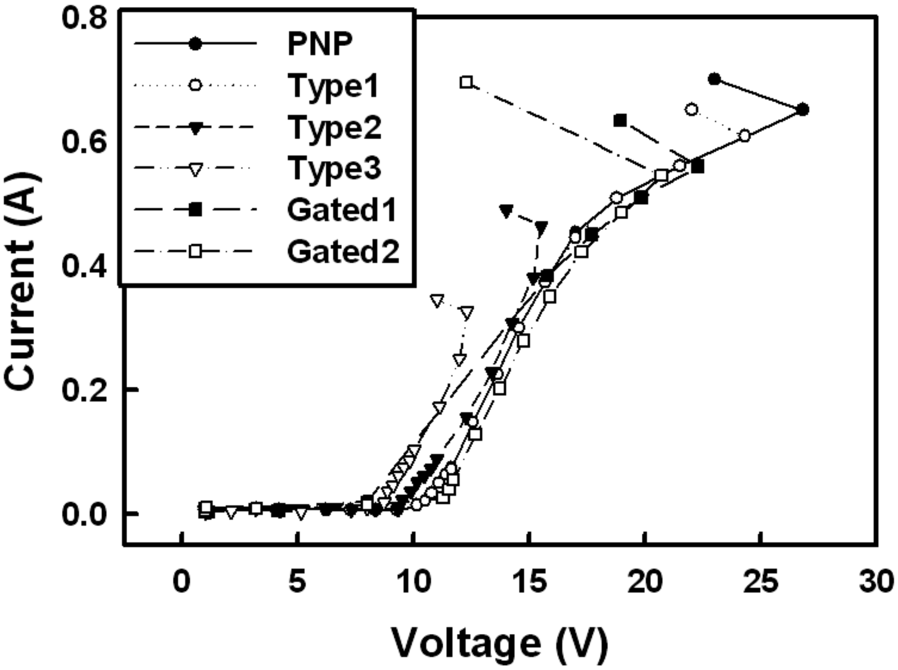


(a) (b) (c) (d) (e) (f)

Fig. 3.2 The device structures of (a) the traditional PNP, (b) the type1 LVTPNP, (c) the type2 LVTPNP, (d) the type3 LVTPNP, (e) the gated1 LVTPNP, and (f) the gated2 LVTPNP.

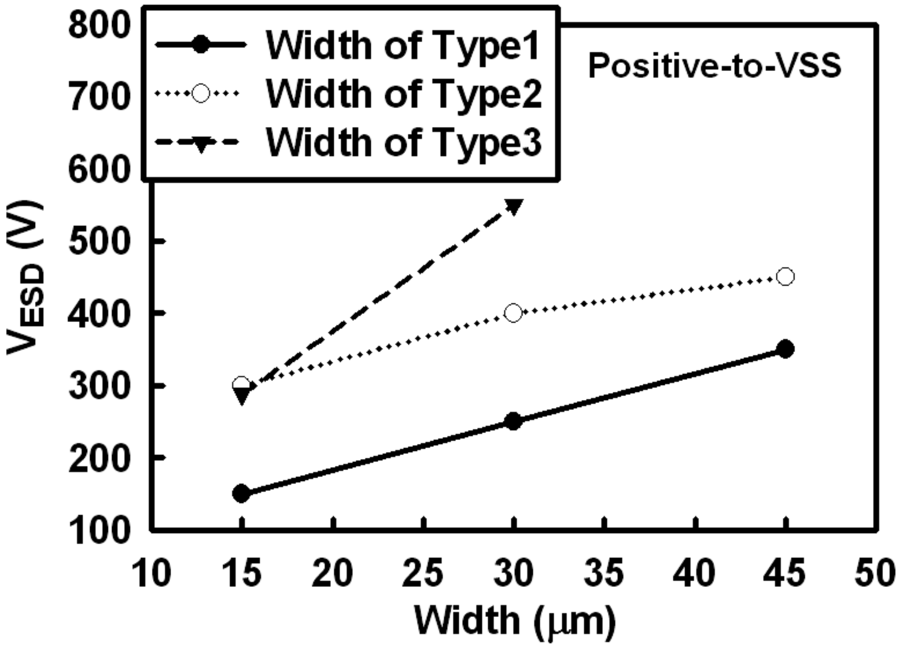


(a)

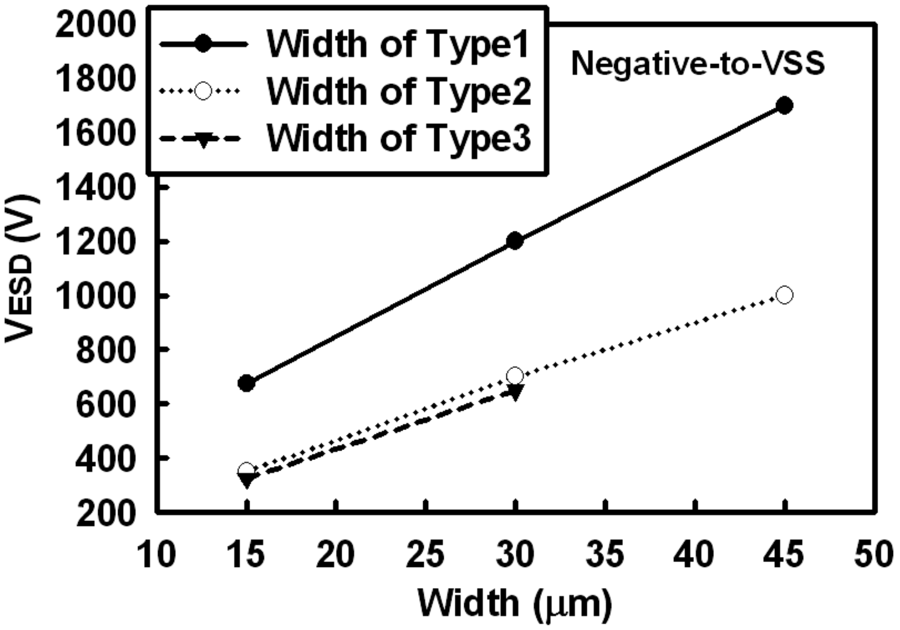


(b)

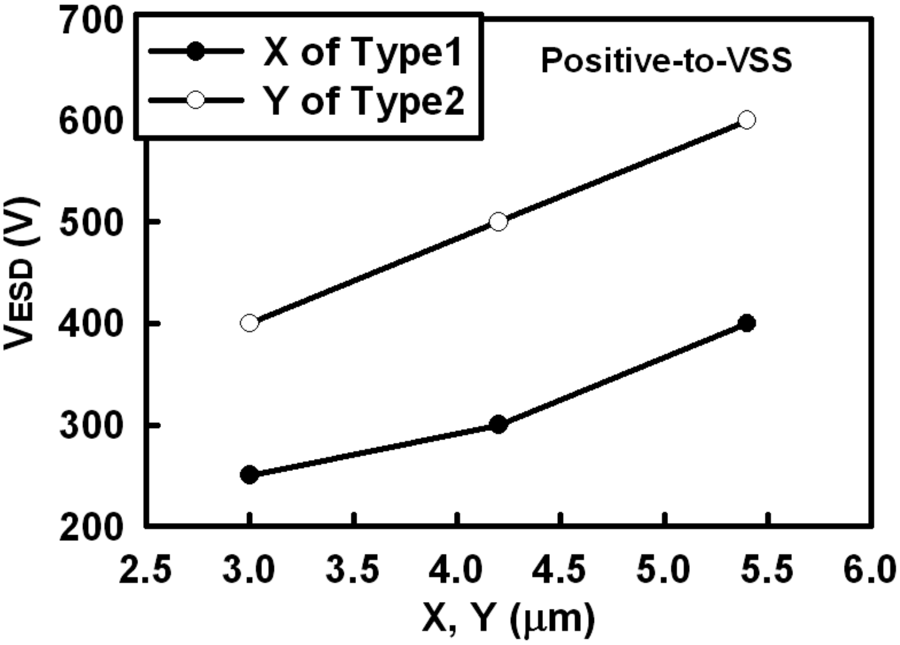
Fig. 3.3 The TLP-measured I-V curves among traditional PNP and different LVTPNP devices under (a) the positive-to-VSS (PS-mode), and (b) the negative-to-VSS (NS-mode), stress conditions.


Width of Type1
Width of Type2
Width of Type3
Positive-to-VSS
V_{ESD} (V)
800
700
600
500
400
300
200
100
10
15
20
25
30
35
40
45
50
Width (μm)

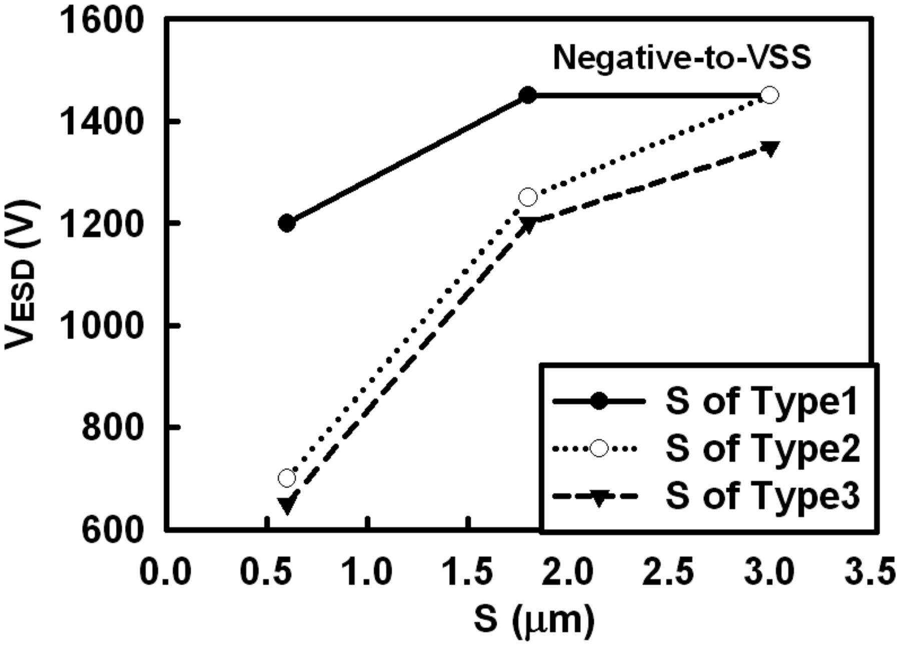
(a)


Width of Type1
Width of Type2
Width of Type3
Negative-to-VSS
V_{ESD} (V)
2000
1800
1600
1400
1200
1000
800
600
400
200
10
15
20
25
30
35
40
45
50
Width (μm)

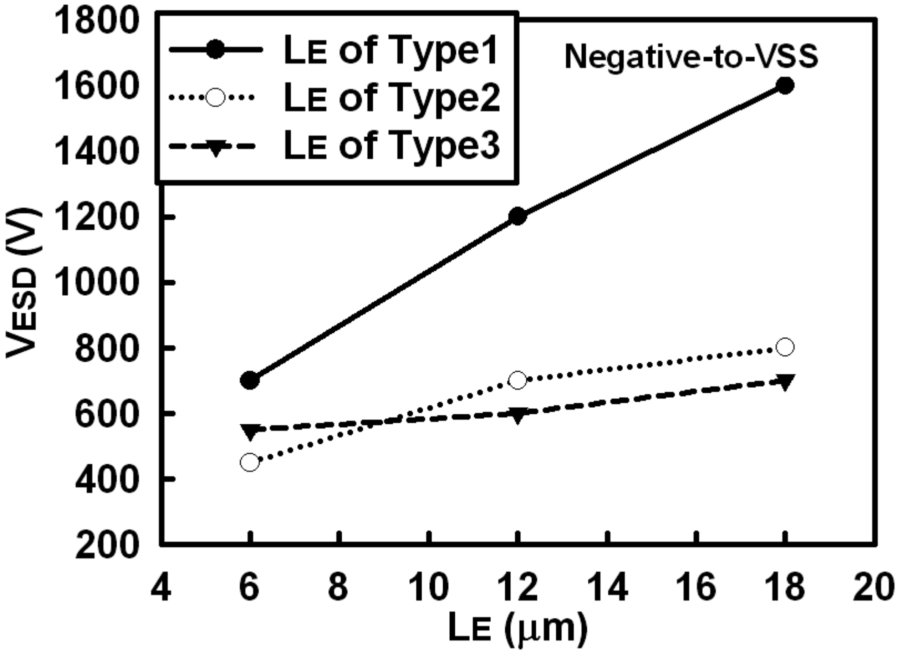
(b)


X of Type1
Y of Type2
Positive-to-VSS
VESD (V)
700
600
500
400
300
200
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
X, Y (μm)

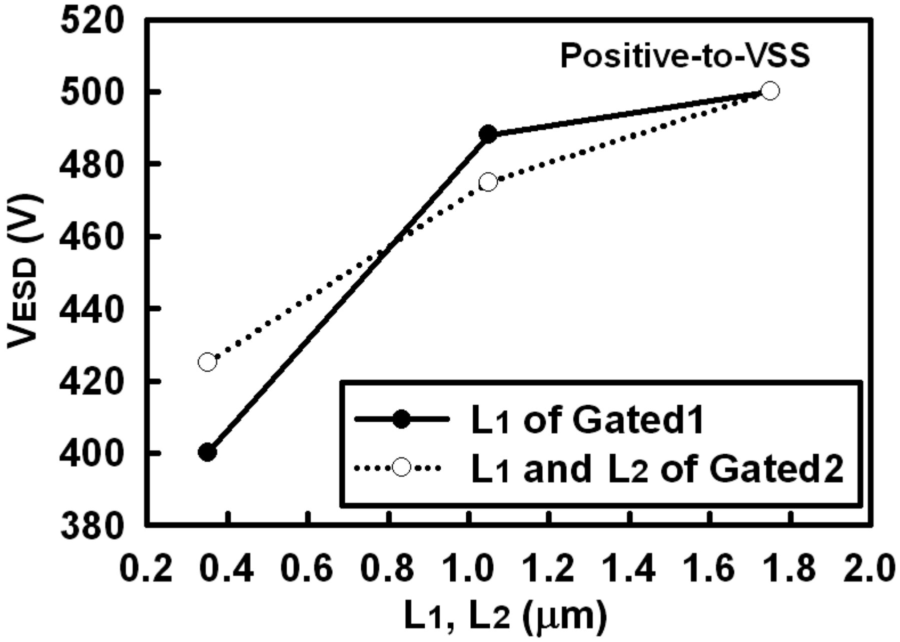
(c)


Negative-to-VSS
S of Type1
S of Type2
S of Type3
VESD (V)
1600
1400
1200
1000
800
600
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
S (μm)

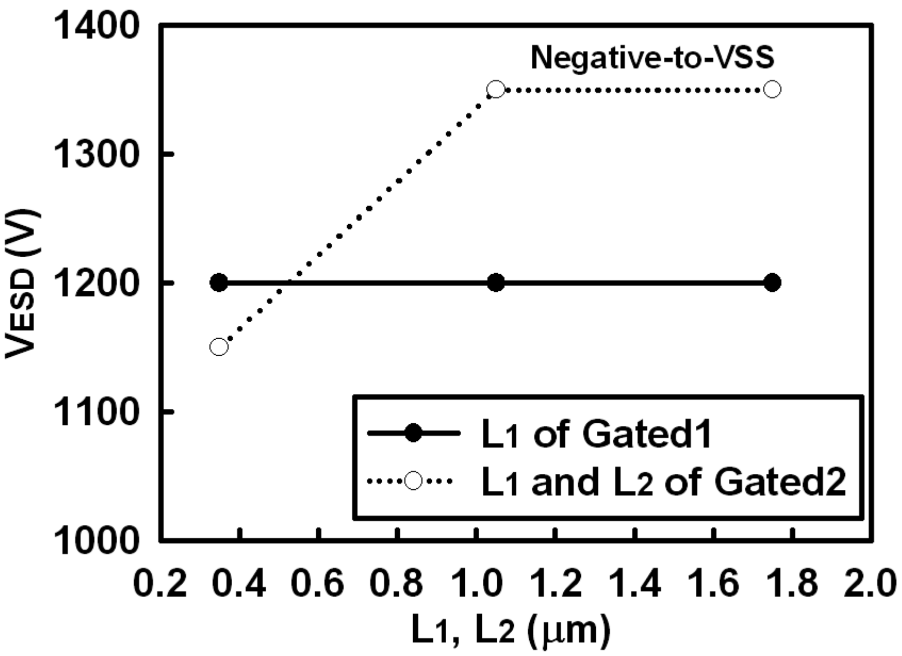
(d)


1800
1600
1400
1200
1000
800
600
400
200
VESD (V)
4
6
8
10
12
14
16
18
20
LE (μm)
LE of Type1
LE of Type2
LE of Type3
Negative-to-VSS

(e)

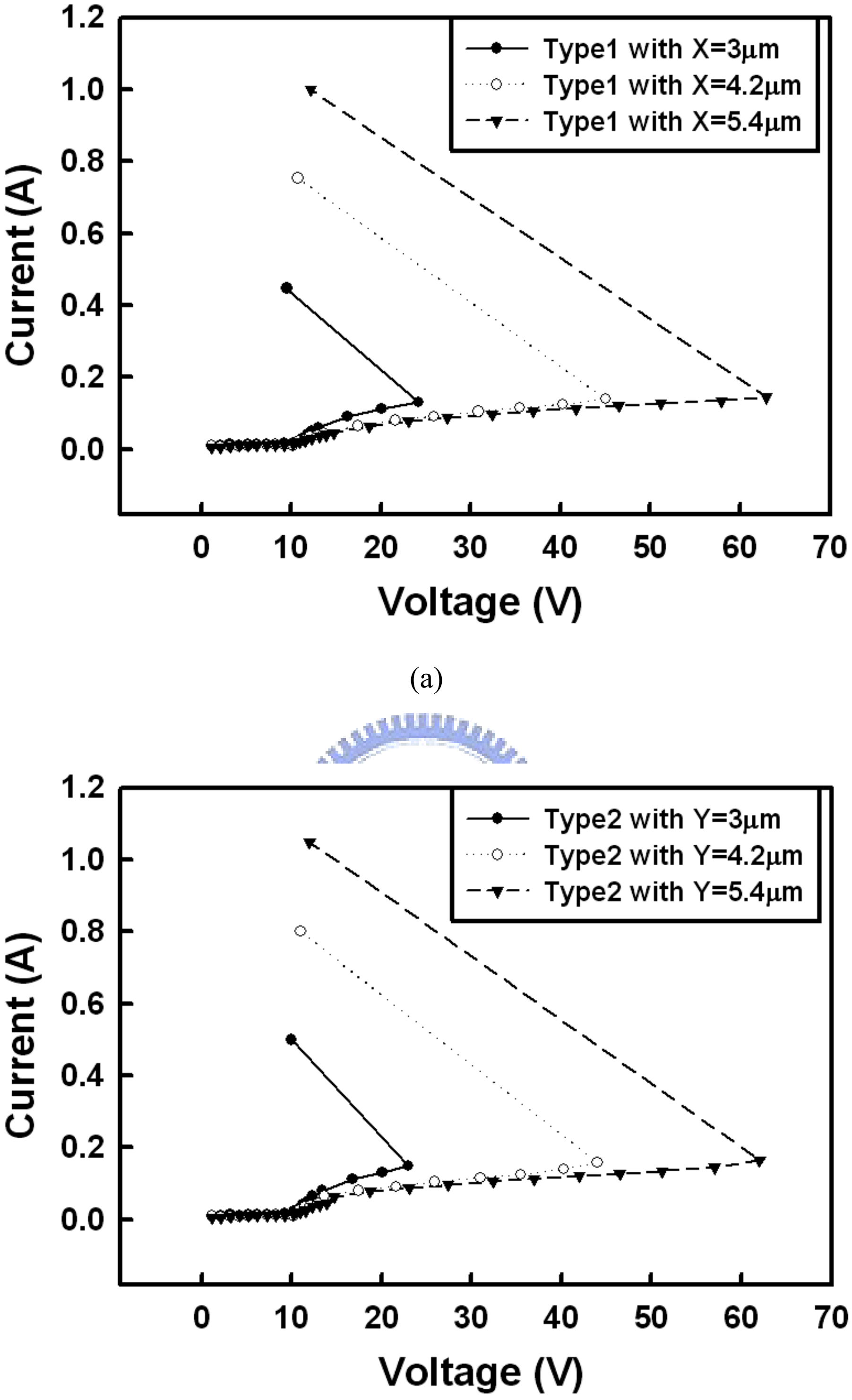

520
500
480
460
440
420
400
380
VESD (V)
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
L1, L2 (μm)
Positive-to-VSS
L1 of Gated1
L1 and L2 of Gated2

(f)



(g)

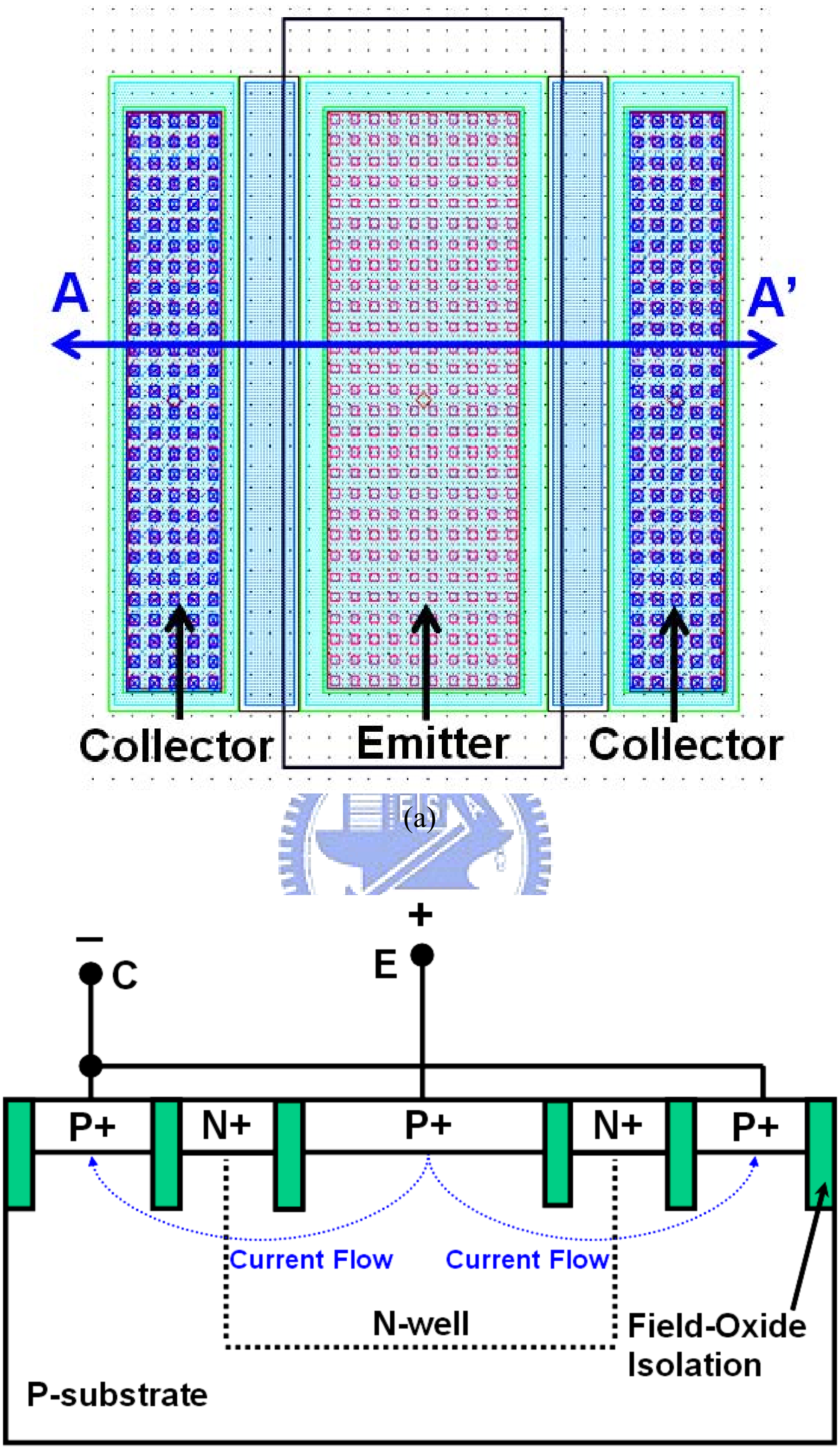
Fig. 3.4 (a) The ESD level v.s. device width under the positive-to-VSS ESD-stress condition. (b) The ESD level v.s. device width under the negative-to-VSS ESD-stress condition. (c) The ESD level v.s. the spacing X of the type1 LVTPNP or the spacing Y of the type2 LVTPNP under the positive-to-VSS ESD-stress condition. (d) The ESD level v.s. the spacing S under the negative-to-VSS ESD-stress condition, respectively. (e) The ESD level v.s. device LE under the negative-to-VSS ESD-stress condition. (f) The ESD level v.s. L1 or L2 of the gated1 LVTPNP and the gated2 LVTPNP under the positive-to-VSS ESD-stress condition. (g) The ESD level v.s. L1 or L2 the gated1 LVTPNP and the gated2 LVTPNP under the negative-to-VSS ESD-stress condition.



(a)

(b)

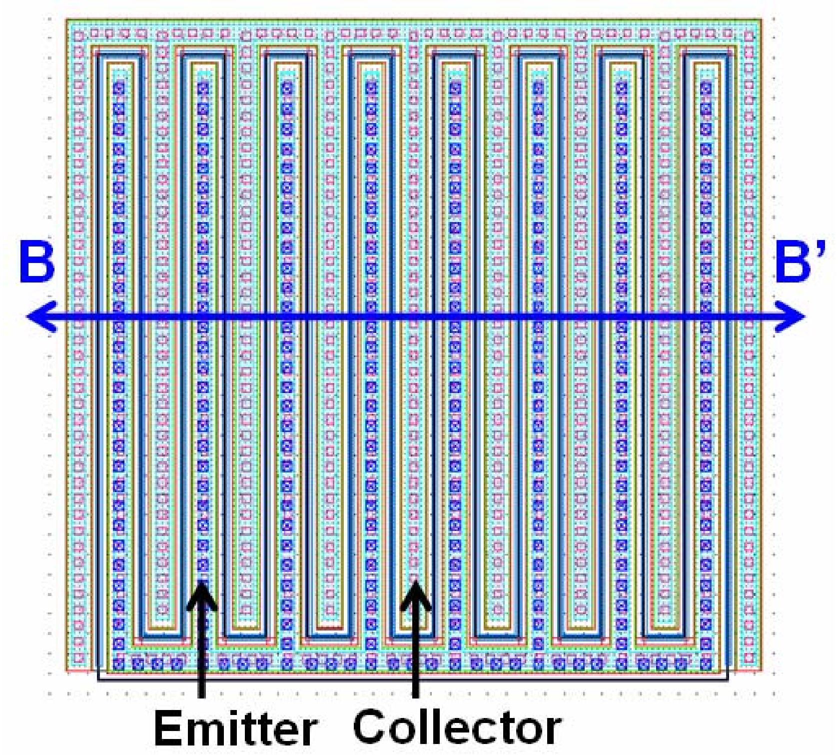
Fig. 3.5 The TLP-measured I-V curves of (a) the type1 LVTPNP with different X spacings, and (b) the type2 LVTPNP with different Y spacings, under the positive-to-VSS stress condition.



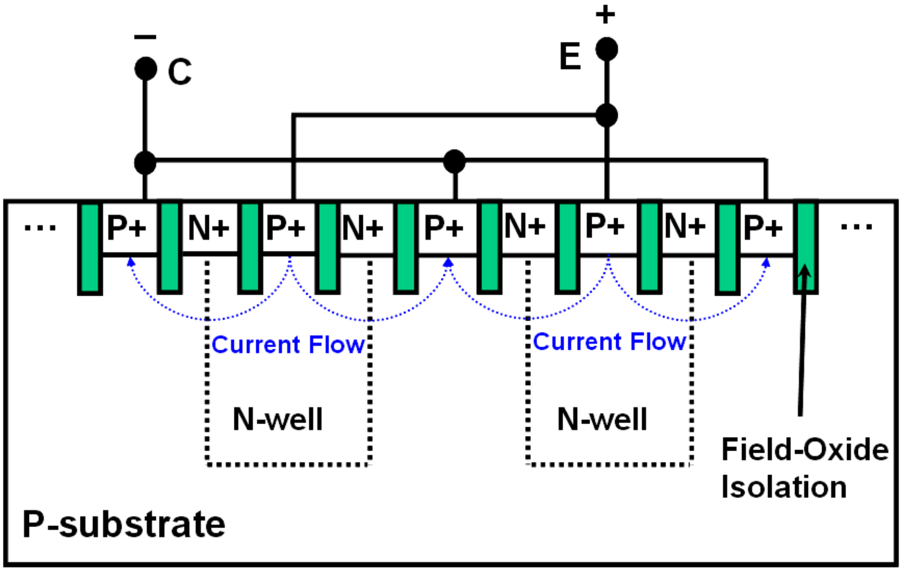
(a)

(b)

Fig. 3.6 (a) The single finger layout style of the LVTPNP, and (b) the cross-sectional view along the line AA' in the single finger layout of LVTPNP.

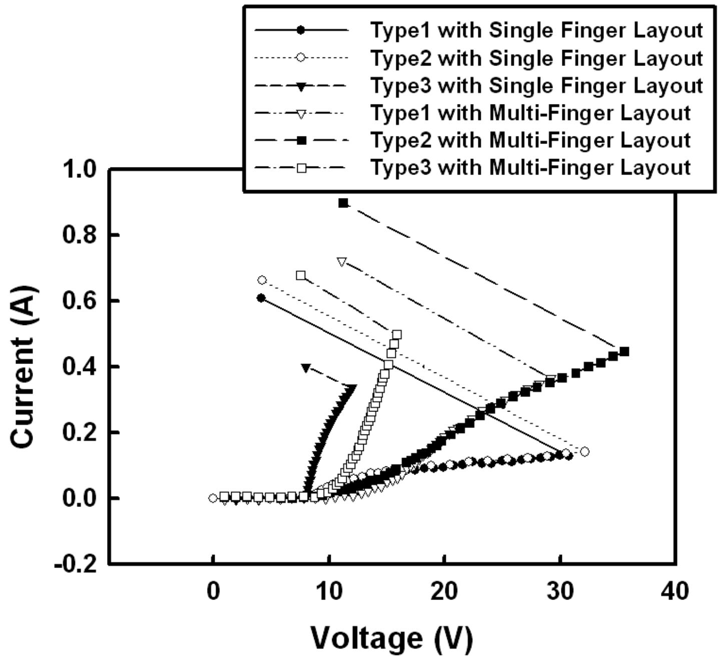


(a)

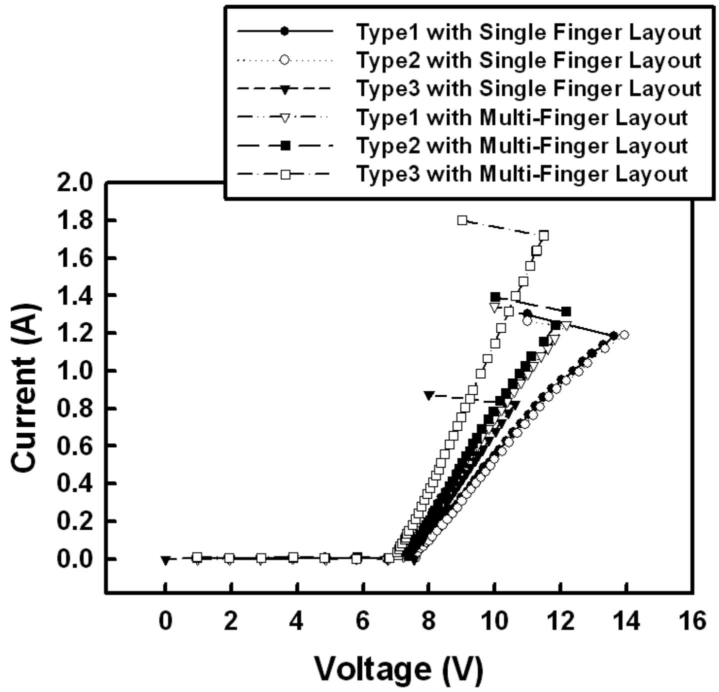


(b)

Fig. 3.7 (a) The multi-finger layout style of the LVTPNP, and (b) the cross-sectional view along the line BB' in the multi-finger layout of LVTPNP.



(a)



(b)

Fig. 3.8 The TLP-measured I-V curves of the LVTPNP devices realized with the single finger layout style or the multi-finger layout style in a 0.25-μm salicided CMOS process under (a) the positive-to-VSS, and (b) the negative-to-VSS, stress conditions.

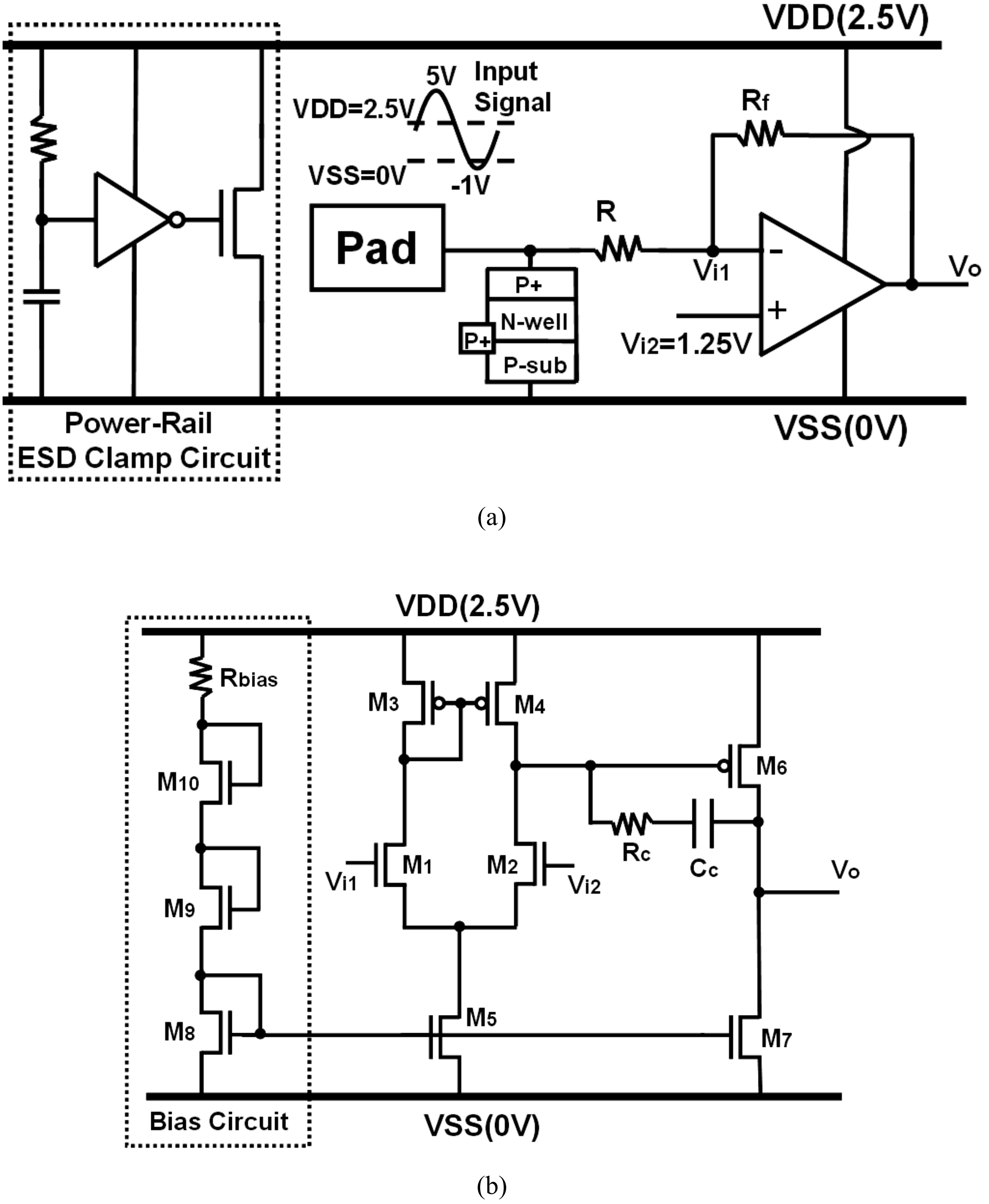


Fig. 3.9 (a) ESD protection design for the ADSL input stage with single-ended operational amplifier and voltage divider in a 0.25-μm salicided CMOS process. (b) The schematic of the two-stage operational amplifier.

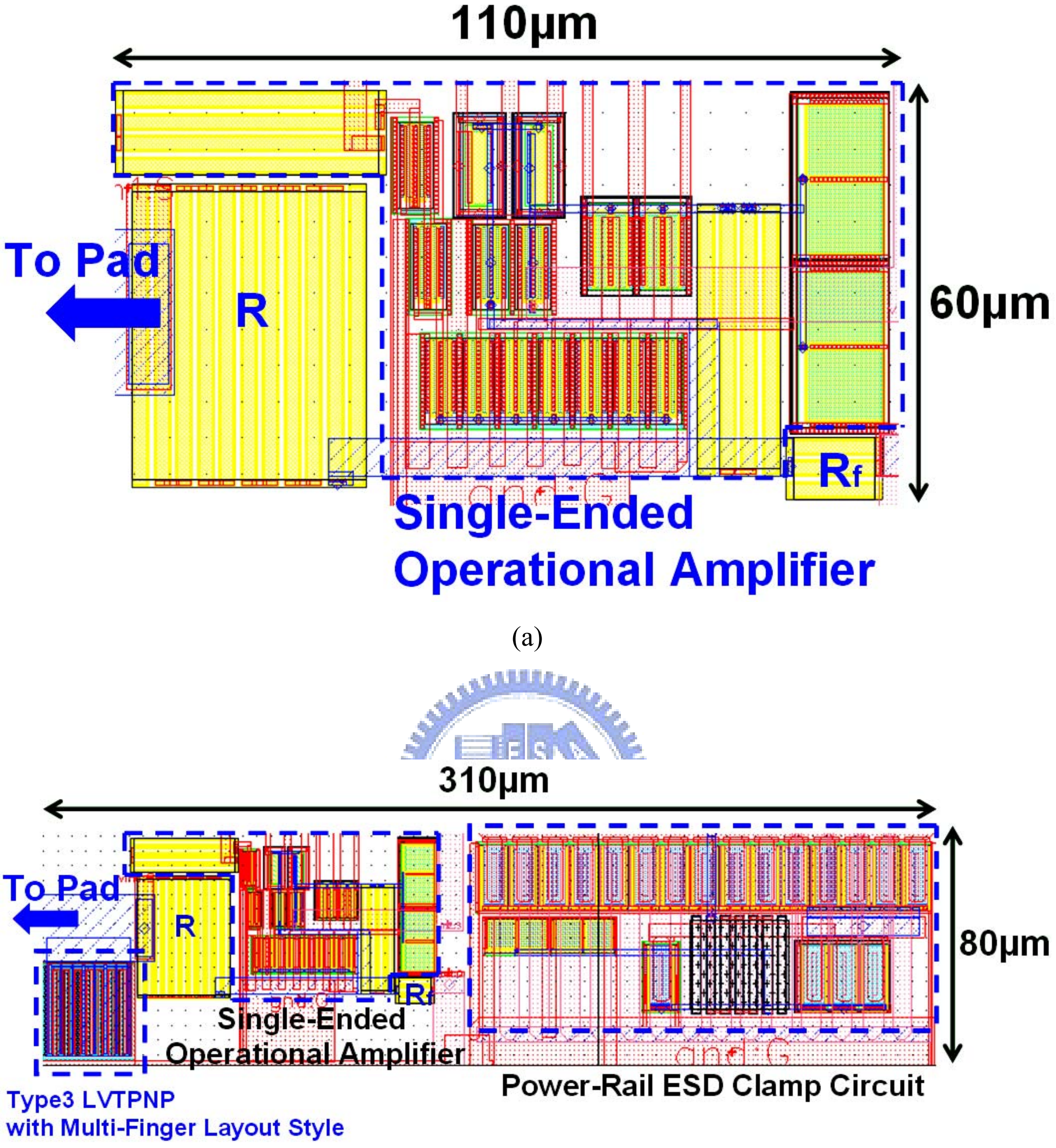


Fig. 3.10 The layout views of the ADSL input stage (a) without ESD protection, and (b) with ESD protection circuit.

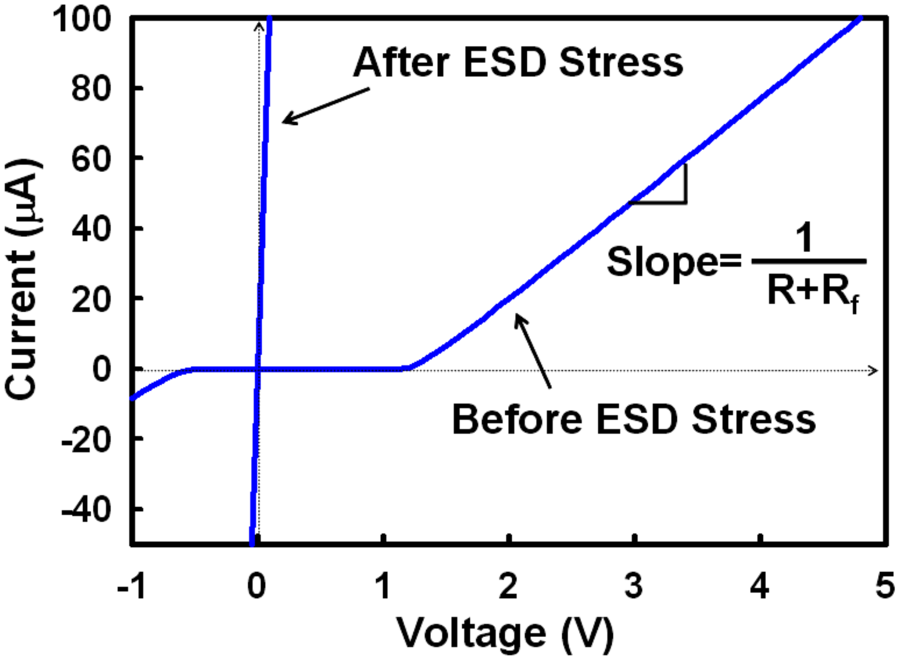


Fig. 3.11 The I-V curves of the ADSL input stage with ESD protection circuit before and after PS-mode HBM ESD stress of 1.5kV, which was measured by applying a swept voltage from -1 to 5 V on the input pad with VSS grounded and VDD floating.

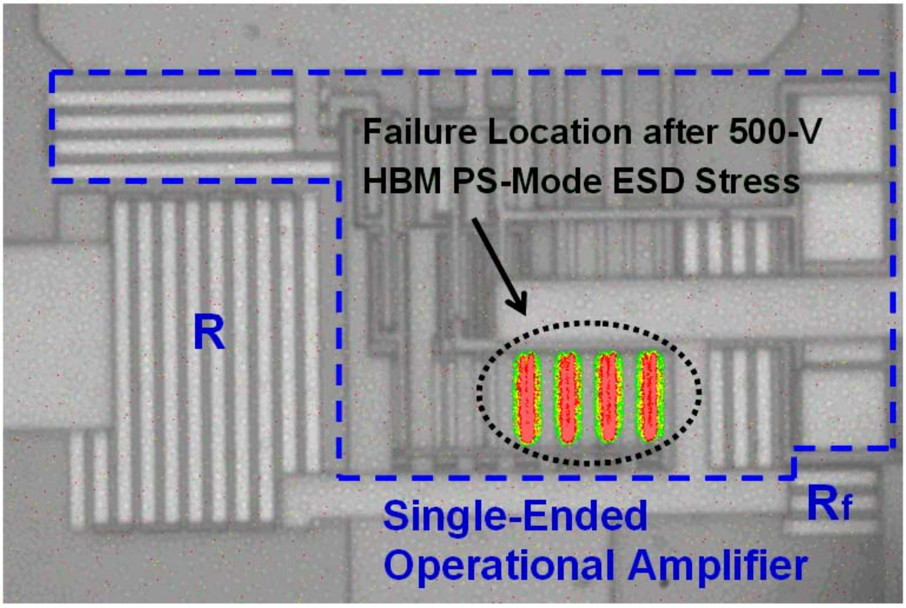


Fig. 3.12 The EMMI picture on the ADSL input stage without ESD protection circuit after HBM PS-mode ESD stress of 500V.

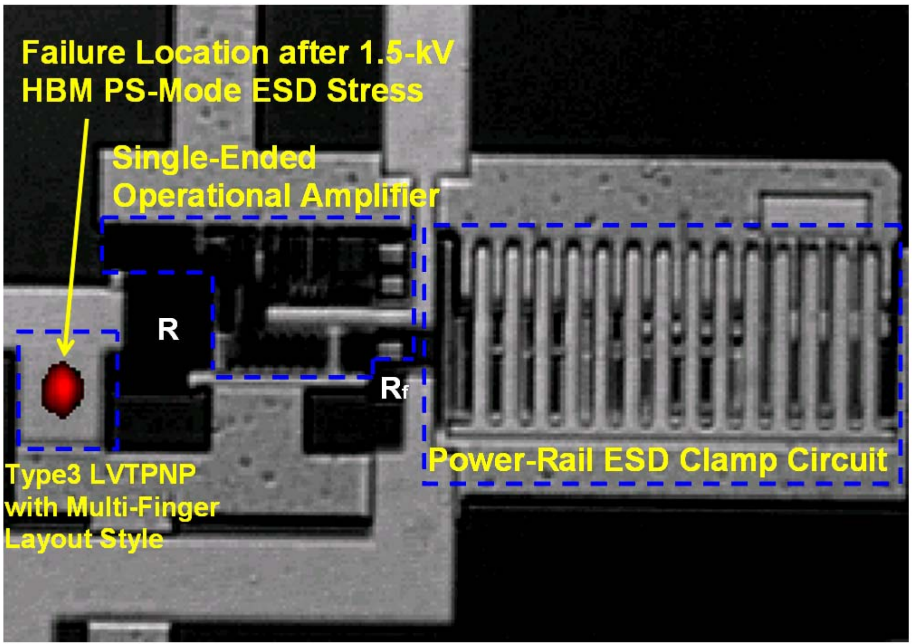


Fig. 3.13 The OBIRCH picture on the ADSL input stage with ESD protection circuit after 1.5-kV HBM PS-mode ESD stress. The failure location is on the type3 LVTPNP device of ESD protection circuit.

CHAPTER 4

HIGH-VOLTAGE-TOLERANT ESD CLAMP CIRCUIT IN LOW-VOLTAGE THIN-OXIDE TECHNOLOGY

To increase the system-on-chip ESD immunity of micro-electronic products against system-level ESD stress, the chip-level ESD/EMC protection design should be enhanced. Considering gate-oxide reliability, a new electrostatic discharge (ESD) protection scheme with ESD_BUS and high-voltage-tolerant ESD clamp circuit for 1.2/2.5 V mixed-voltage I/O interfaces is proposed in this chapter. The devices used in the high-voltage-tolerant ESD clamp circuit are all 1.2 V low-voltage NMOS/PMOS devices which can be safely operated under the 2.5 V bias conditions without suffering from the gate-oxide reliability issue. The four-mode (PS, NS, PD, and ND) ESD stresses on the mixed-voltage I/O pad and pin-to-pin ESD stresses can be effectively discharged by the proposed ESD protection scheme. The experimental results verified in a 0.13 μm CMOS process have confirmed that the proposed new ESD protection scheme has high human-body-model (HBM) and machine-model (MM) ESD robustness with a fast turn-on speed. The proposed new ESD protection scheme, which is designed with only low-voltage devices, is an excellent and cost-efficient solution to protect mixed-voltage I/O interfaces [67].

4.1 New ESD Protection Scheme for Mixed-Voltage I/O Interfaces

Giving consideration to gate-oxide reliability, the proposed ESD protection scheme with an ESD_BUS and a high-voltage-tolerant ESD clamp circuit for 1.2/2.5 V mixed-voltage I/O interfaces [67]–[70] is shown in Fig. 4.1. To receive the input signals with 2.5 V voltage level, the direct diode connection from the I/O pad to the VDD of 1.2 V is forbidden. Hence, to avoid the leakage current path from the I/O pad to the VDD, the new ESD scheme is realized with the diodes Dp, Dn, D1, the ESD_BUS line, and the high-voltage-tolerant ESD clamp circuit, as shown in Fig. 4.1.

The additional ESD_BUS line is realized by a wide metal line in the CMOS IC [51], [52]. To save layout area, the ESD_BUS can be realized by a different metal layer, which overlaps the VDD power line. The ESD_BUS is not directly connected to an external power pin, but is initially biased at VDD of 1.2 V through the diode D1 after the chip has been powered on. When the input signals of 2.5 V reach to the I/O pad, the ESD_BUS line will be charged up to 2.5 V through the diode Dp. Therefore, during normal circuit operating conditions with 2.5 V input signals, the diode D1 connected between the VDD power line and ESD_BUS line is used to block the leakage current path from the I/O pad to VDD.

The PS-mode, NS-mode, PD-mode, and ND-mode ESD stresses on the mixed-voltage I/O pad have the corresponding ESD discharge paths in the proposed ESD protection scheme. The R_{ESD} is used to avoid damage on the stacked-NMOS before the ESD current is discharged through the proposed ESD protection scheme. Under the PS-mode ESD stress condition, the ESD current will flow from the I/O pad through the diode Dp to the ESD_BUS, and then from the ESD_BUS through the high-voltage-tolerant ESD clamp circuit to VSS. Under the NS-mode ESD stress condition, the ESD current will flow from VSS through the diode Dn in the forward-biased condition to the I/O pad. Under the PD-mode ESD stress condition, the ESD current will flow from the I/O pad through the diode Dp to the ESD_BUS, and then from the ESD_BUS through the high-voltage-tolerant ESD clamp circuit to the VSS line, and then through the power-rail ESD clamp circuit to VDD. Under the ND-mode ESD stress condition, the ESD current will flow from VDD through the power-rail ESD clamp circuit to the VSS line, and then from VSS through the diode Dn in the forward-biased condition to the I/O pad.

Usually, the ESD detection circuit was directly added between the I/O pad and VSS to enhance the ESD robustness of STNMOS in the I/O cell [43], [44]. However, an ESD detection circuit is needed for each I/O cell, which increases the additional loading capacitance to the I/O pad. In order to save the layout area of the chip and to decrease the loading capacitance on the I/O pad, such an ESD_BUS and a high-voltage-voltage ESD clamp circuit can be shared with other mixed-voltage I/O cells which have the same input/output voltage levels. Moreover, the shared ESD_BUS and high-voltage-tolerant ESD clamp circuit can provide efficient pin-to-pin ESD protection. In the pin-to-pin ESD test, the ESD pulse is applied to some I/O pin with other I/O pins grounded, whereas the VDD and

VSS are floating. During pin-to-pin ESD stress, as shown in Fig. 4.2, the ESD current will flow from one I/O pad through the diode Dp to the common ESD_BUS, and then from ESD_BUS through high-voltage-tolerant ESD clamp circuit to the VSS line, and finally from VSS through the diode Dn to another grounded I/O pad.

In this ESD protection scheme, the high-voltage-tolerant ESD clamp circuit must sustain the high-voltage (2.5 V) stress in the mixed-voltage I/O circuit during normal circuit operating conditions. Hence, how to design a turn-on efficient high-voltage-tolerant ESD clamp circuit with only 1.2 V devices for 2.5 V application is the key design issue in the proposed ESD protection scheme for 1.2/2.5 V mixed-voltage I/O interfaces.

4.2 High-Voltage-Tolerant ESD Clamp Circuit

The high-voltage-tolerant ESD clamp circuit realized with only 1.2 V devices is shown in Fig. 4.3, which contains the ESD detection circuit and the ESD clamp device. The ESD clamp device is realized with stacked-NMOS (STNMOS) with the substrate-triggered technique [42]. The STNMOS is formed by two stacked NMOS transistors (Mn1 and Mn2) with 1.2 V gate oxide in a 0.13 μm CMOS process. The gate of Mn1 (V_{g1}) is biased at VDD of 1.2 V through a resistor to avoid the gate-oxide reliability issue, and the gate of Mn2 (V_{g2}) is connected to VSS (grounded) to ensure the off state of the STNMOS during normal circuit operating conditions. Therefore, the STNMOS will be kept off without gate-oxide reliability during normal circuit operating conditions with an ESD_BUS of 2.5 V.

The ESD detection circuit is inactive during normal circuit operating conditions, but it becomes active to provide the substrate-triggered current to trigger on an ESD clamp device under an ESD stress event. The gate voltage of PMOS Mp1 is decided by the RC delay caused by an N-well resistor R2 and a capacitor (realized by Mp3 in a stand-alone N-well). Here, the time constant of R2 and C (Mp3) is designed around the order of ~ 1 μs to distinguish the power-on transition (the supply voltage with a rise time of several milliseconds) from the ESD transition (the ESD voltage with a rise time of several nanoseconds).

4.2.1 Substrate-Triggered STNMOS

The snapback breakdown of STNMOS device depends on the substrate current (I_{sub}), which is created by the reverse-biased drain/substrate junction in breakdown condition, to forward bias the source/substrate junction. The substrate current (I_{sub}) drifting through the effective substrate resistance (R_{sub}) to ground, will elevate the substrate potential (V_{sub}) of the emitter-base junction in the parasitic lateral n-p-n BJT. When the emitter-base junction begins to weakly forward bias due to the increase of the local substrate potential, the lateral n-p-n BJT will be turned on to discharge the ESD current. Hence, the substrate resistance (R_{sub}) and the substrate current (I_{sub}) are the important parameters to turn-on efficiency [71], [72]. The substrate-triggered technique [42] can be applied to generate the necessary substrate current (I_{sub}) without causing drain/substrate junction breakdown. With the applied substrate-triggered current (I_{trig}), the trigger voltage (Vt1) of the STNMOS can be reduced for more effective ESD protection.

The finger-type layout pattern and the corresponding cross-sectional view of the substrate-triggered STNMOS device are shown in Figs. 4.4(a) and 4.4(b), respectively. Here, the drain of Mn2 and the source of Mn1 share a common N+ diffusion region. An additional P+ diffusion is inserted into the center region of STNMOS device structure as the substrate-triggered point. An N-well structure is further diffused under the source region to form a higher equivalent substrate resistance (R_{sub}) to improve turn-on efficiency of the parasitic lateral n-p-n BJT in the STNMOS.

4.2.2 Operation Principles

The operation of the high-voltage-tolerant ESD clamp circuit during normal circuit operating conditions is shown in Fig. 4.5. With a 1.2 V VDD power supply voltage, the ESD_BUS could be charged up to (maximum) 2.5 V by the 2.5 V input signals at the I/O pad. With a maximum voltage level of 2.5 V on the ESD_BUS, the gate of Mp1 (node a) will be biased at 2.5 V through resistor R2, and the gate of Mp2 and Mn3 (node b) will be biased at 1.2 V through resistor R1. Hence, Mp1 and Mp2 are kept off and Mn3 is turned on to bias the substrate of STNMOS at VSS. There is no trigger current generated from the ESD detection circuit into the STNMOS, so the STNMOS is guaranteed to be kept off under normal circuit operating conditions. The source-gate voltage of Mp2 is less than the threshold voltage of the 1.2 V PMOS transistor (|Vtp|), so the source voltage of Mp2 (node c) is kept between VDD and VDD+|Vtp|. In this situation, all 1.2 V devices are free from the gate-oxide reliability issue under normal circuit operating conditions with a 2.5 V ESD_BUS in the mixed-voltage I/O interfaces.

The operation of the high-voltage-tolerant ESD clamp circuit during a PS-mode ESD stress event is shown in Fig. 4.6, where the ESD transition voltage is applied to the I/O pad with VSS relatively grounded and VDD floating. The ESD transient voltage will be conducted from the I/O pad through the diode Dp to the ESD_BUS. The gate of Mp1 (node a) will be kept at a relatively low voltage for a long time due to the RC delay of R2 and Mp3 in the ESD detection circuit. The VDD is initially floating with an initial voltage of 0 V before the ESD transition voltage is applied across the I/O pad and VSS. Some ESD transient voltage would be coupled to VDD through parasitic capacitance during ESD discharging, but R1 and the parasitic capacitance at the gates of Mp2 and Mn3 will hold the gate of Mp2 at a low voltage level for a long time to keep Mp2 at on state. Therefore, Mp1 and Mp2 (whose initial gate voltages are at a low voltage level of ~0V) can be quickly turned on by ESD energy to generate the substrate-triggered current (I_{trig}) into the substrate of STNMOS. After the base-emitter voltage of the lateral n-p-n BJT in the STNMOS is greater than its cut-in voltage, the STNMOS will be triggered into its snapback region. Hence, the PS-mode ESD current will be conducted from the I/O pad through the diode Dp to the ESD_BUS, and then through the lateral n-p-n BJT in the STNMOS to VSS.

4.2.3 Hspice-Simulated Results

The device dimensions of Mp1, Mp2, Mp3, and Mn3 in the ESD detection circuit are 40 μm/0.2 μm, 40 μm/0.2 μm, 10 μm/7.5 μm, and 5 μm/0.2 μm, respectively. R1 and R2 in the detection circuit are 1 kΩ and 50 kΩ, respectively. The Hspice-simulated voltage waveforms of the ESD detection circuit during power-on transition are shown in Fig. 4.7. The ESD_BUS and VDD are respectively powered on to 2.5 V and 1.2 V with a simultaneous rise time of 1 ms. The gate voltage of Mp1 (node a) in the ESD detection circuit with the selected R2-Mp3 value (1 μs) can be validated to follow up the power-on transition of the ESD_BUS, therefore, to keep the PMOS Mp1 off. Moreover, from the Hspice-simulated voltage waveforms, the voltages across the gate-drain, gate-source, and gate-bulk terminations of every device in the proposed high-voltage-tolerant ESD clamp circuit do not exceed the process limitation (~ 1.32 V in a given 1.2 V CMOS process).

The transient simulation of the ESD detection circuit under an ESD stress event is shown in Fig. 4.8. When a 0 to 5.5V ESD-like voltage pulse with a rise time of 10 ns is applied to the ESD_BUS with VSS relatively grounded and VDD floating, the gate voltage of Mp1 (node a) is kept at a low voltage level due to the time delay of R2-Mp3. Therefore, substrate-triggered current (I_{trig}) can be conducted through Mp1 and Mp2 in the ESD detection circuit to trigger on STNMOS. By selecting suitable device dimensions for R2, Mp1, Mp2, and Mp3, the peak current and period of the substrate-triggered current can be designed to meet different applications or specifications.

4.3 Experimental Results

4.3.1 *Characteristics of Substrate-Triggered STNMOS*

The measured DC current-voltage (I-V) characteristics of STNMOS with a device dimension (W/L) of 360 μm/0.2 μm under different substrate-triggered currents (measured by a Tek370 curve tracer) are shown in Fig. 4.9(a). The trigger voltage of the parasitic lateral n-p-n BJT in the STNMOS device decreases when the substrate-triggered current (I_{trig}) increases. Moreover, the relation of common-emitter current gain (β_F) to collector current (I_C) in the STNMOS is also shown in Fig. 4.9(b). β_F increases as I_C increases when I_C is lower than ~ 10 mA. But, β_F decreases as I_C increases when I_C is larger than ~ 10 mA. The peak value of β_F is about 1.3 when I_C is about ~ 10 mA.

To investigate the device behavior during high ESD current stress, the transmission line pulsing (TLP) technique has been widely used to measure the second breakdown characteristics (secondary breakdown current (It2) and secondary breakdown voltage (Vt2)) of ESD devices. The TLP generator (TLPG) with a pulse width of 100 ns and rise time of 10 ns is used to find the It2 of STNMOS devices under different substrate-triggered currents. The TLP-measured I-V characteristics of the substrate-triggered STNMOS with the device dimension (W/L) of 360 μm/0.2 μm under substrate-triggered currents of 0, 2, and 4 mA are shown in Fig. 4.10. With the substrate-triggered current of 4 mA, the STNMOS can be triggered on with a trigger voltage below 4 V, as comparing to an original drain breakdown voltage of ~ 6 V. In addition, the turn-on uniformity among the multiple fingers of STNMOS can be improved by the substrate-triggered effect [42]. The It2 level of the substrate-triggered STNMOS device can be improved from 2 A to 2.4 A, when the substrate-triggered current is increased from 0 to 4 mA. With a higher It2, the STNMOS can sustain a higher ESD level.

Based on the experimental results, the high-voltage-tolerant ESD clamp circuit can be designed with a lower trigger voltage and higher ESD robustness. The TLP-measured I-V curves of STNMOS with or without the ESD detection circuit under device dimension (W/L) of 360 μm/0.2 μm are shown in Fig. 4.11. Compared to the stand-alone STNMOS, the secondary breakdown current (It2) of the STNMOS with the proposed ESD detection circuit can be increased from 2 A to 2.6 A. The R_{ESD} in Fig. 4.1 should be designed a little larger than some critical value (~ 10 Ω), such that STNMOS in the mixed-voltage I/O interface will not be damaged before the ESD current is discharged through the diode Dp, the ESD_BUS, and the high-voltage-tolerant ESD clamp circuit to the grounded VSS under the PS-mode ESD stress. The Vt2 of STNMOS in the mixed-voltage I/O interface ($Vt2_{I/O}$) plus the voltage drop of the R_{ESD} ($It2_{I/O} \times R_{ESD}$) should be larger than the Vt2 of STNMOS in the high-voltage-tolerant ESD clamp circuit ($Vt2_{ESD}$) plus the turn-on voltage of the diode Dp ($V_{D,on}$), as seen in the following equation,

$$Vt2_{ESD} + V_{D,on} \leq (It2_{I/O} \times R_{ESD}) + Vt2_{I/O}. \qquad (1)$$

Here, $Vt2_{ESD}$ and $Vt2_{I/O}$ can be derived from the secondary breakdown voltage of the STNMOS with and without the ESD detection circuit in Fig. 4.11, respectively. The $It2_{I/O}$ can be derived from the secondary breakdown current of the STNMOS without the ESD detection circuit in Fig. 4.11.

Moreover, the It2 of STNMOS with or without the ESD detection circuit under different device dimensions are also measured in Fig. 4.12. The STNMOS device with an ESD detection circuit has a higher It2 than that without an ESD detection circuit. For the device dimension (W/L) of 240 μm/0.2 μm, the It2 can be increased from 1.4 A to 2.4 A, which is a ~70% improvement.

4.3.2 Turn-on Speed

In order to verify the turn-on efficiency of the proposed high-voltage-tolerant ESD clamp circuit, a 0 to 20V voltage pulse with a rise time of 10 ns is applied to the ESD_BUS with VSS grounded and VDD floating, as shown in Fig. 4.13. The overshooting peak voltage clamped by the STNMOS without the ESD detection circuit is about 10 V, which could cause damage to the gate oxide of the low-voltage devices. On the contrary, the 20 V voltage pulse can be quickly clamped by the STNMOS with the ESD detection circuit to a low voltage level (~ 5 V). The measured voltage waveforms in Fig. 4.13 have successfully verified the excellent turn-on efficiency of the proposed new high-voltage-tolerant ESD clamp circuit. Hence, during a PS-mode ESD stress condition, the ESD current can be quickly discharged from the I/O pad through the diode Dp, ESD_BUS, and the high-voltage-tolerant ESD clamp circuit to VSS, instead of through STNMOS in the mixed-voltage I/O interface to VSS.

4.3.3 ESD Robustness of STNMOS Devices

The human-body-model (HBM) and machine-model (MM) ESD level of STNMOS devices with different device dimensions are shown in Table 4.1. In these ESD verifications, the HBM and MM levels are measured by a *KeyTek ZapMaster* and the failure criterion is defined as the I-V characteristic curve shifting over 30% from its original curve after three continuous ESD discharges at every ESD test level. With the substrate-triggered current generated from the proposed ESD detection circuit, the turn-on uniformity of STNMOS can be effectively improved. The HBM (MM) ESD levels of the STNMOS with the ESD detection circuit in the high-voltage-tolerant ESD clamp circuit under channel widths of 240, 360, and 480 μm with a channel length of 0.2 μm are improved from 3, 4, 5 kV (175, 250, and 275 V) to 4, 5, 6.5 kV (225, 300, 400 V), respectively, as compared with the stand-alone STNMOS. As a result, the ESD levels of these 1.2/2.5 V mixed-voltage I/O interfaces can be effectively improved by the proposed new ESD protection scheme with the ESD_BUS and the high-voltage-tolerant ESD clamp circuit.

4.4 Summary

To enhance chip-level ESD/EMC immunity, a new ESD protection scheme with an ESD_BUS and a high-voltage-tolerant ESD clamp circuit for system-on-chip with 1.2/2.5 V mixed-voltage I/O interfaces has been successfully designed and verified in a 0.13 μm CMOS process. The ESD stresses on the mixed-voltage I/O pad and the pin-to-pin ESD stresses can be effectively discharged by the proposed ESD protection scheme. With the substrate-triggered current generated from the ESD detection circuit, the turn-on speed and ESD robustness of the high-voltage-tolerant ESD clamp circuit can be significantly increased as compared with a stand-alone STNMOS. For STNMOS with a device dimension (W/L) of 480 μm/0.2 μm, the HBM (MM) ESD level of the 1.2/2.5 V mixed-voltage I/O interfaces can be improved from 5 kV (275 V) to 6.5 kV (400 V) by the ESD detection circuit in the proposed ESD protection scheme.

Table 4.1

HBM and MM ESD levels of STNMOS with or without ESD detection circuit.

STNMOS W/L (μm/μm)	HBM ESD Level (kV)		MM ESD Level (V)	
	without Detection Circuit	with Detection Circuit	without Detection Circuit	with Detection Circuit
240/0.2	3	4	175	225
360/0.2	4	5	250	300
480/0.2	5	6.5	275	400

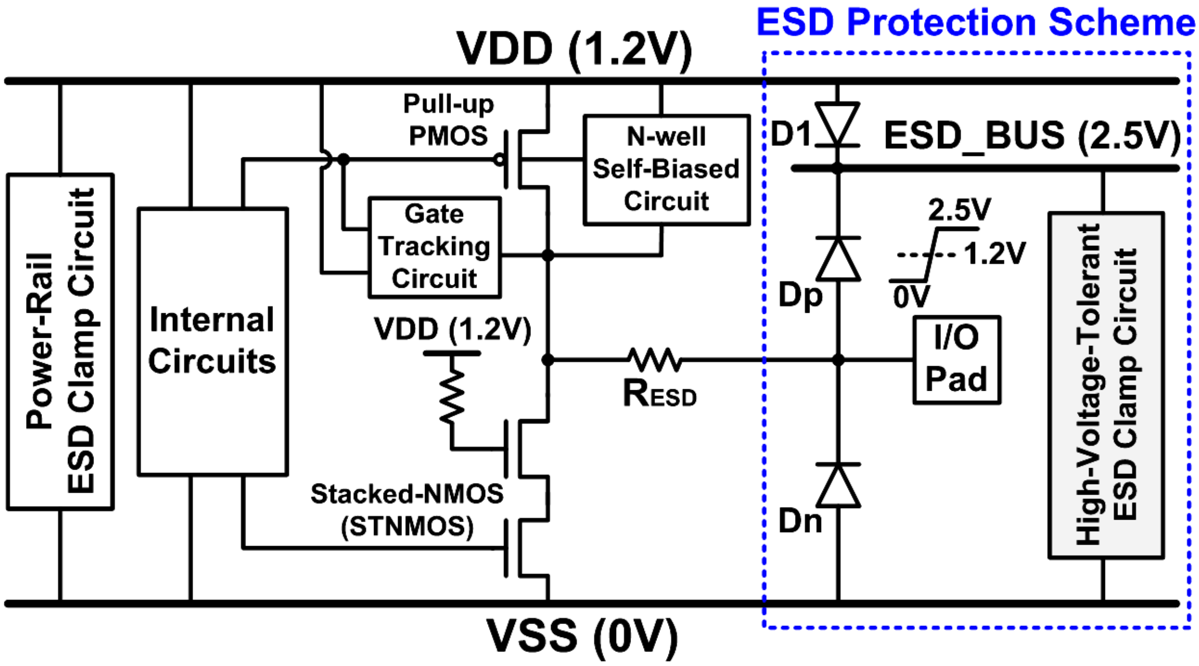


Fig. 4.1 The proposed new ESD protection scheme for 1.2 V/2.5 V mixed-voltage I/O interfaces with a high-voltage-tolerant ESD clamp circuit.

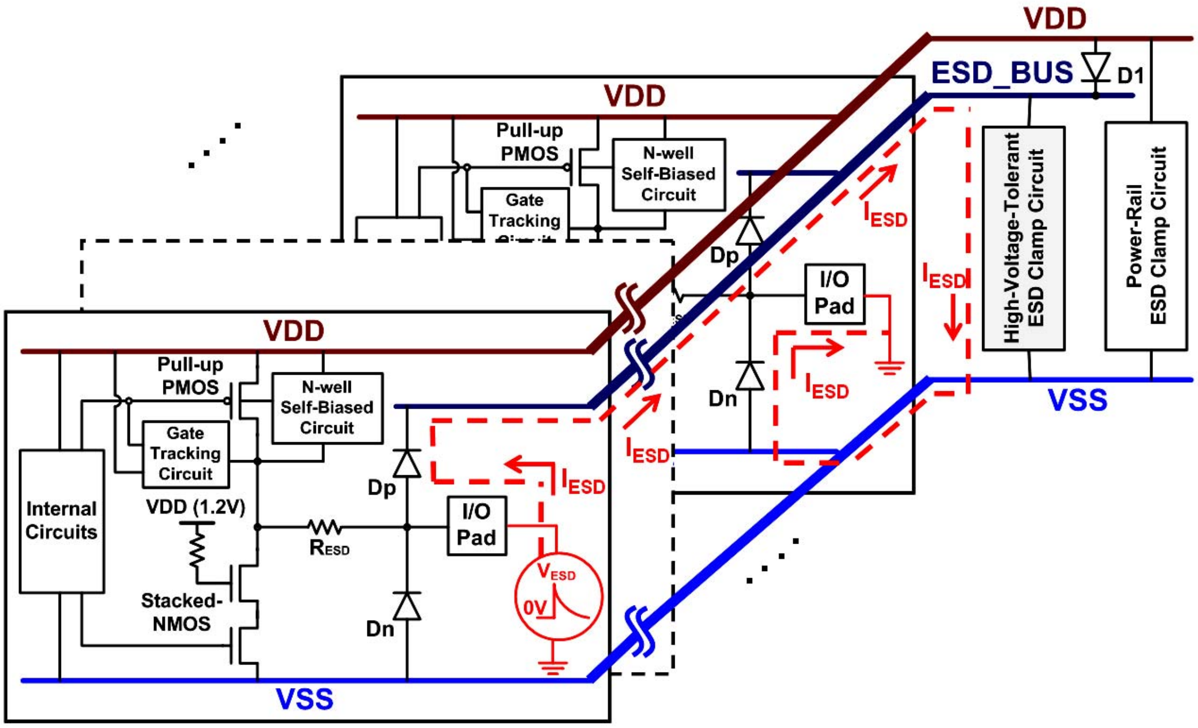


Fig. 4.2 The shared ESD_BUS and high-voltage-tolerant ESD clamp circuit for the whole set of I/O cells to achieve pin-to-pin ESD protection.

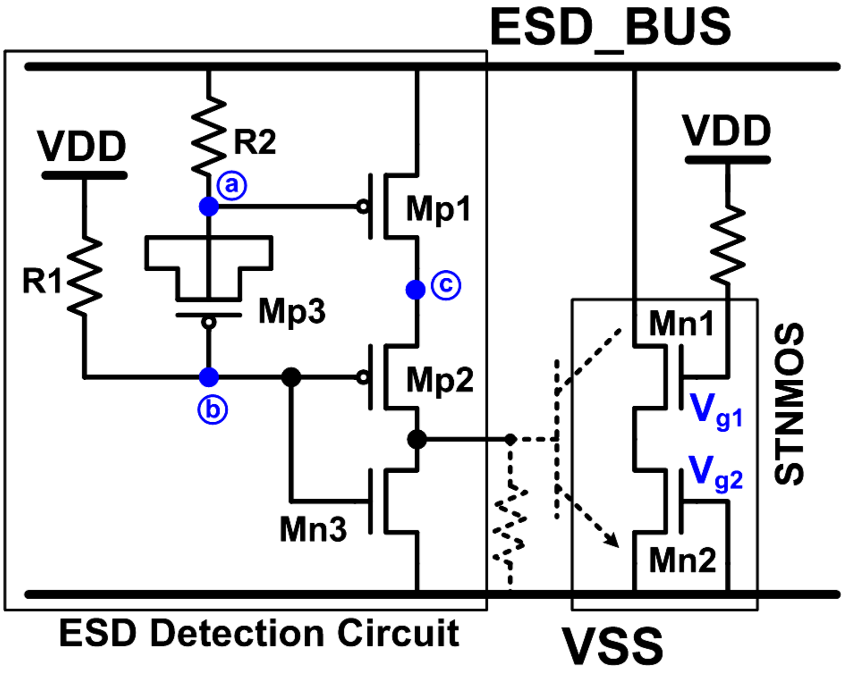
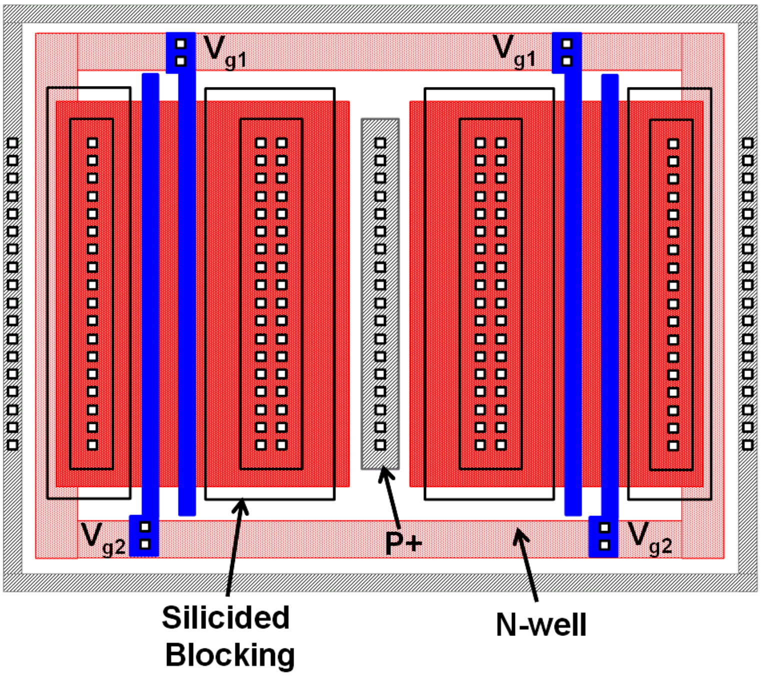
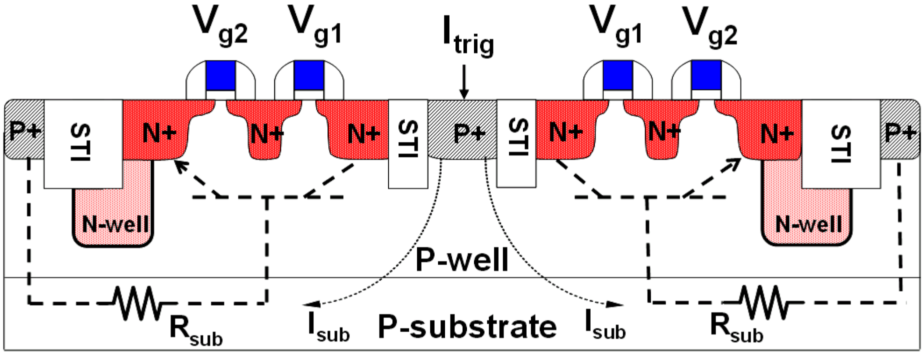


Fig. 4.3 The proposed high-voltage-tolerant ESD clamp circuit.



(a)



(b)

Fig. 4.4 (a) The finger-type layout pattern and (b) the corresponding cross-sectional view of the substrate-triggered STNMOS device.

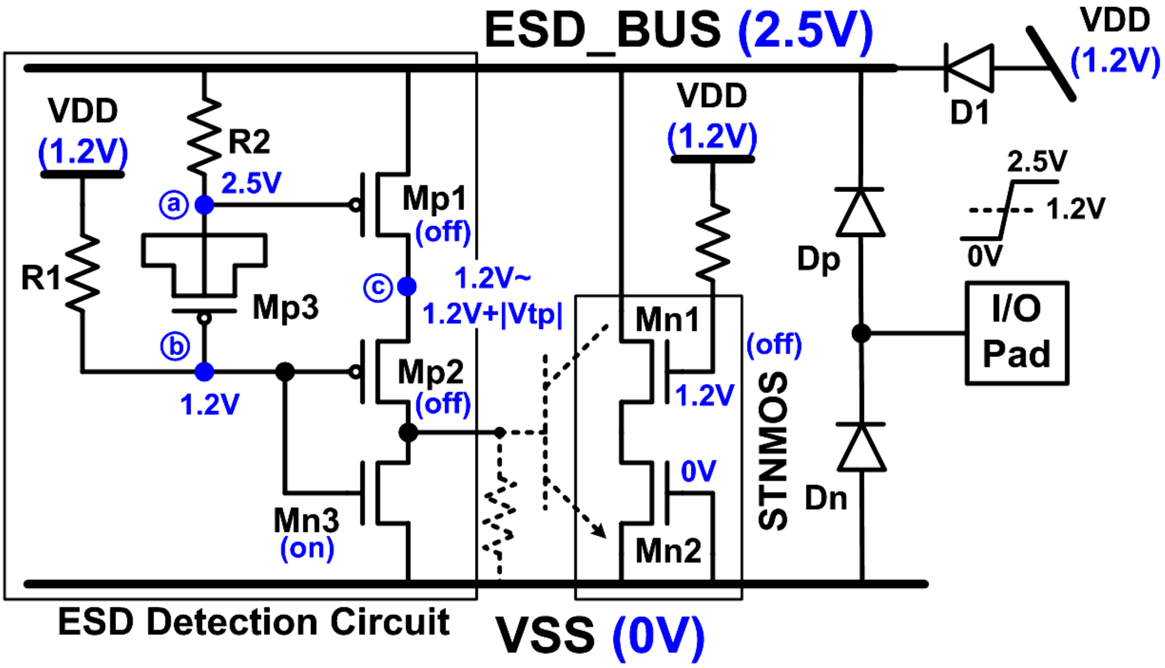


Fig. 4.5 The operation of the high-voltage-tolerant ESD clamp circuit during normal circuit operating conditions.

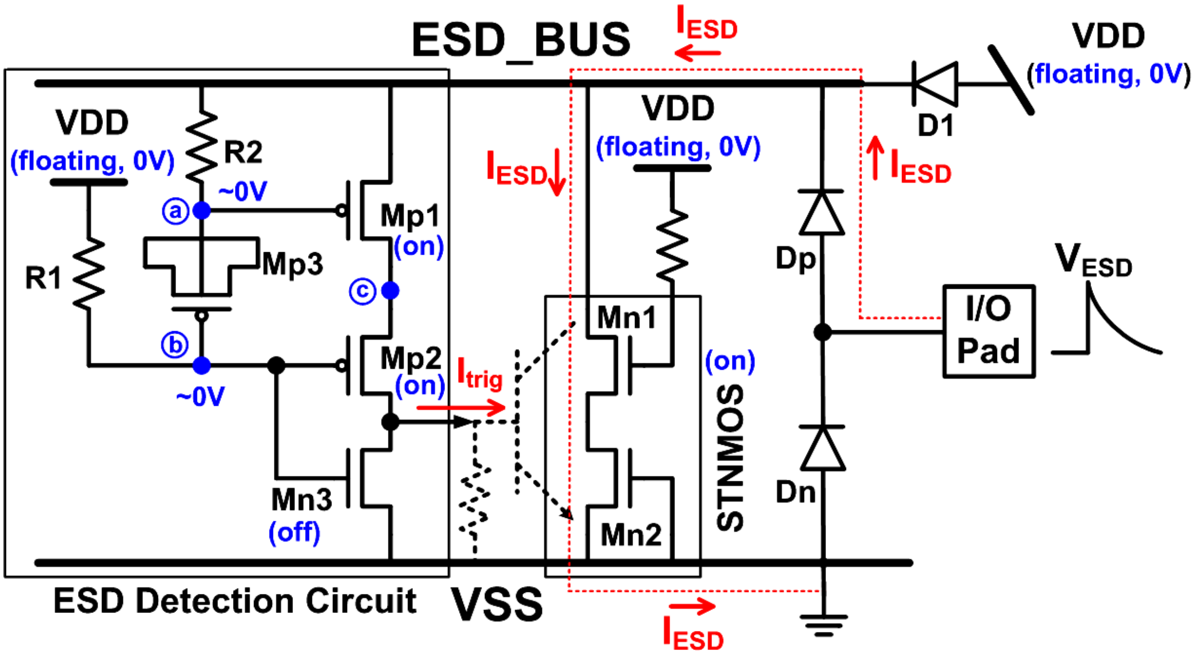


Fig. 4.6 The operation of the high-voltage-tolerant ESD clamp circuit during a PS-mode ESD stress event.

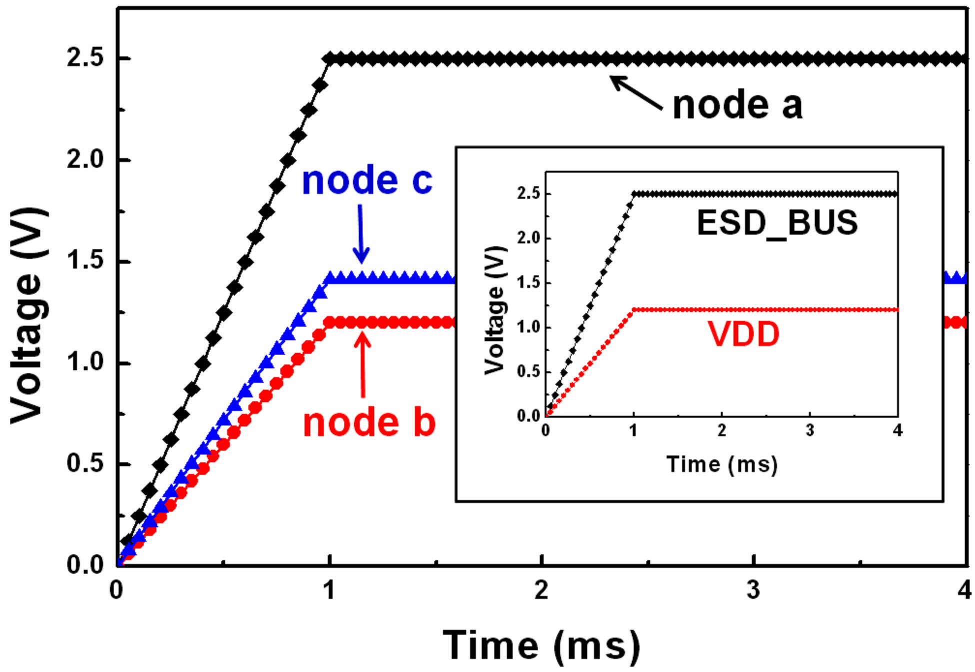


Fig. 4.7 The Hspice-simulated voltage waveforms of the ESD detection circuit during normal power-on transition.

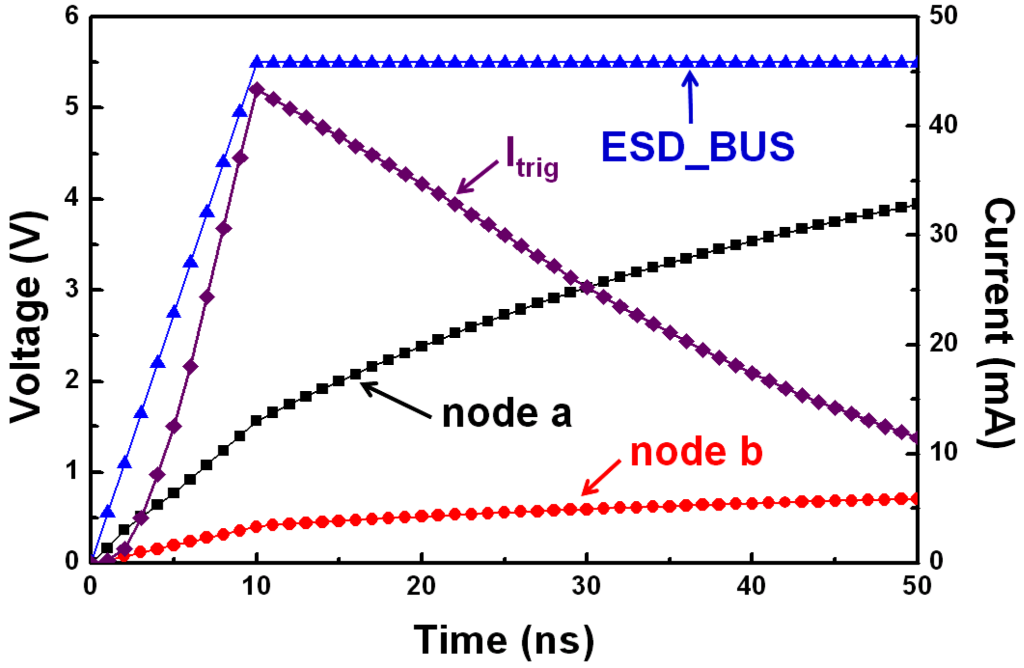
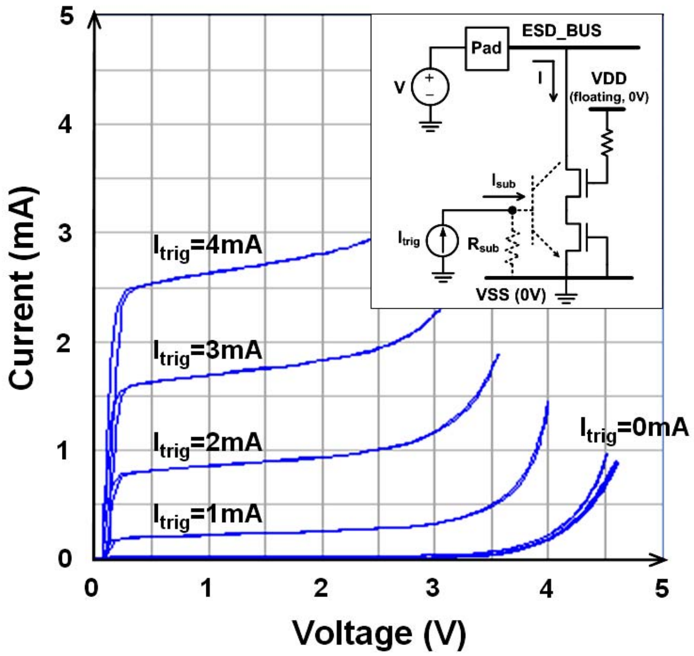
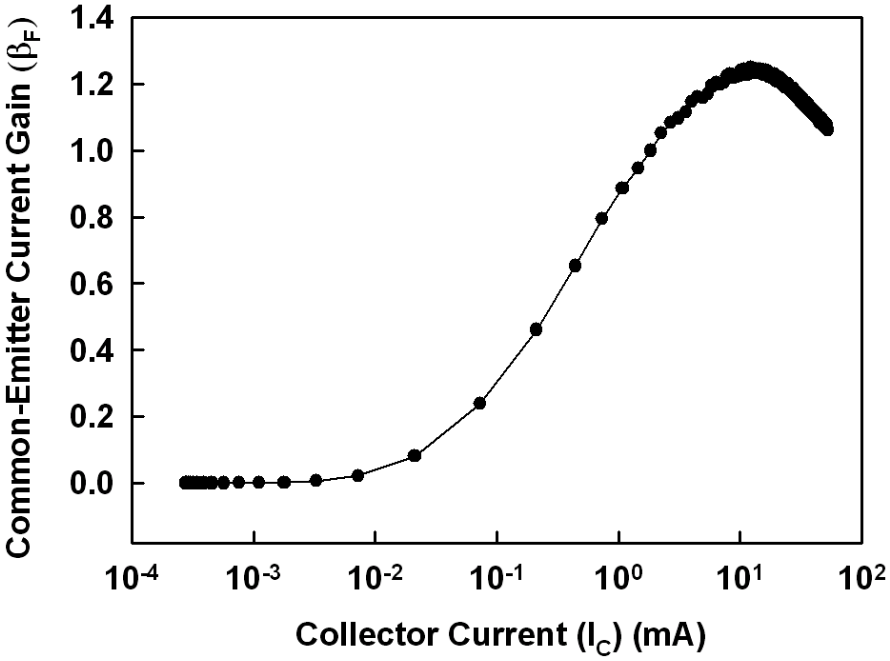


Fig. 4.8 The Hspice-simulated voltage waveforms of the ESD detection circuit during ESD stress event.



(a)



(b)

Fig. 4.9 (a) The measured DC I-V curves of the STNMOS device under different substrate-triggered currents. (b) The measured β_F-I_C relation of the STNMOS device.

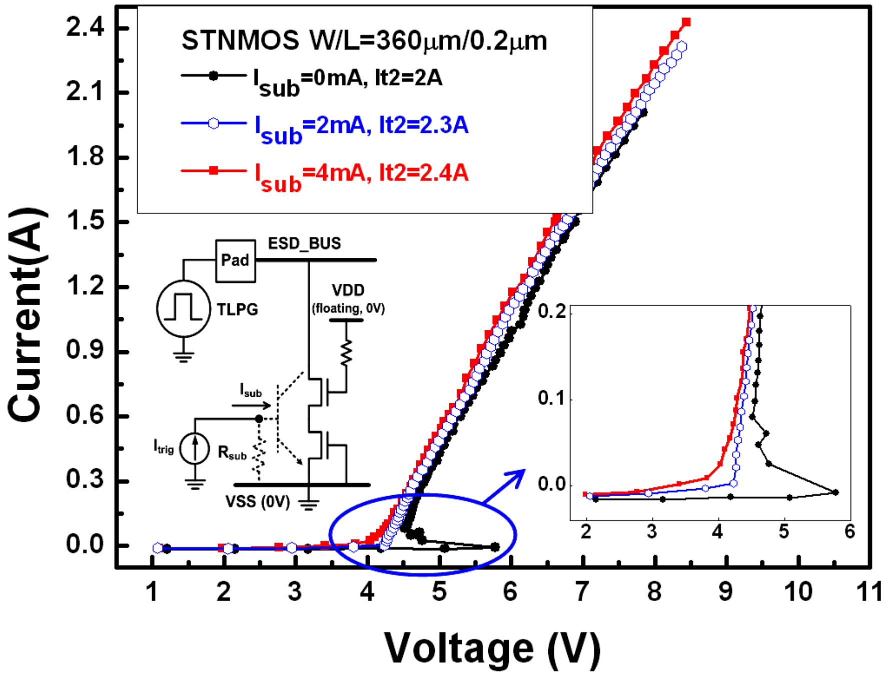


Fig. 4.10 The TLP-measured I-V curves of the STNMOS device with the device dimension (W/L) of 360 μm/0.2 μm under different substrate-triggered currents.

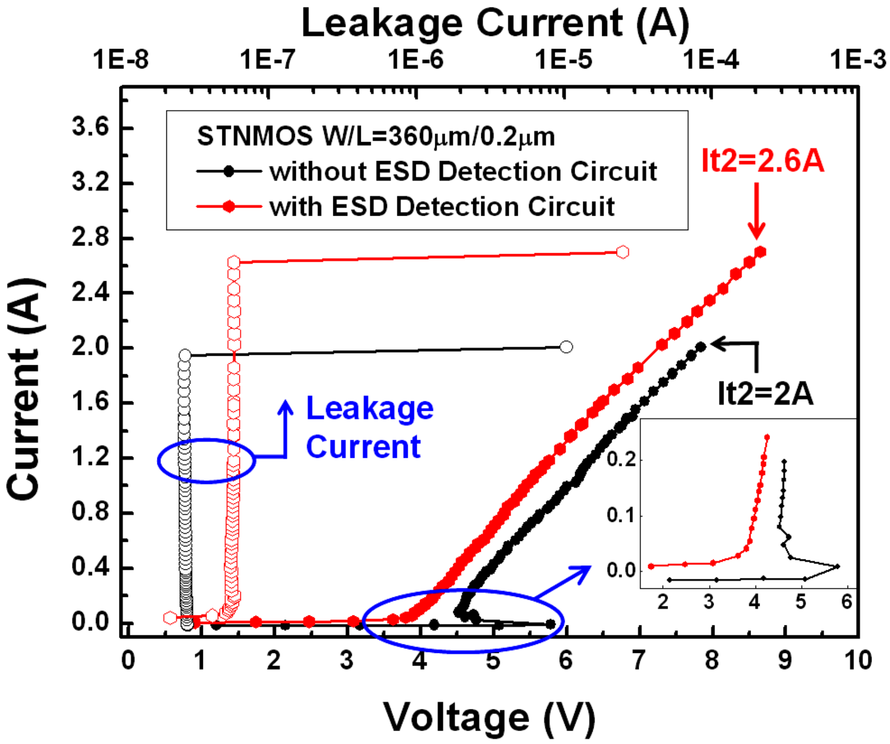


Fig. 4.11 The TLP-measured I-V curve of the STNMOS with or without ESD detection circuit under device dimension (W/L) of 360 μm/0.2 μm.

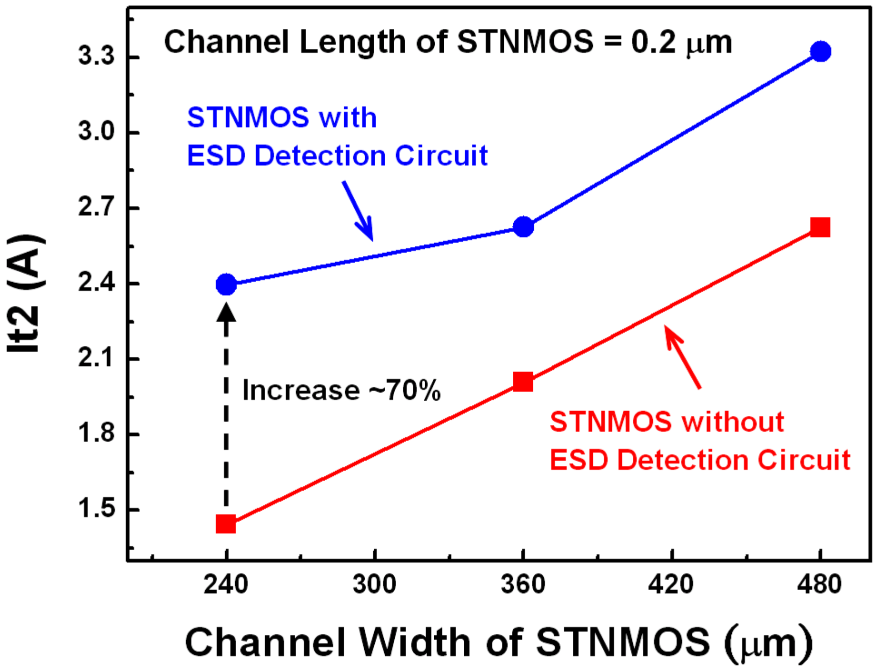


Fig. 4.12 The TLP-measured It2 of the STNMOS device with or without the ESD detection circuit under different channel widths.

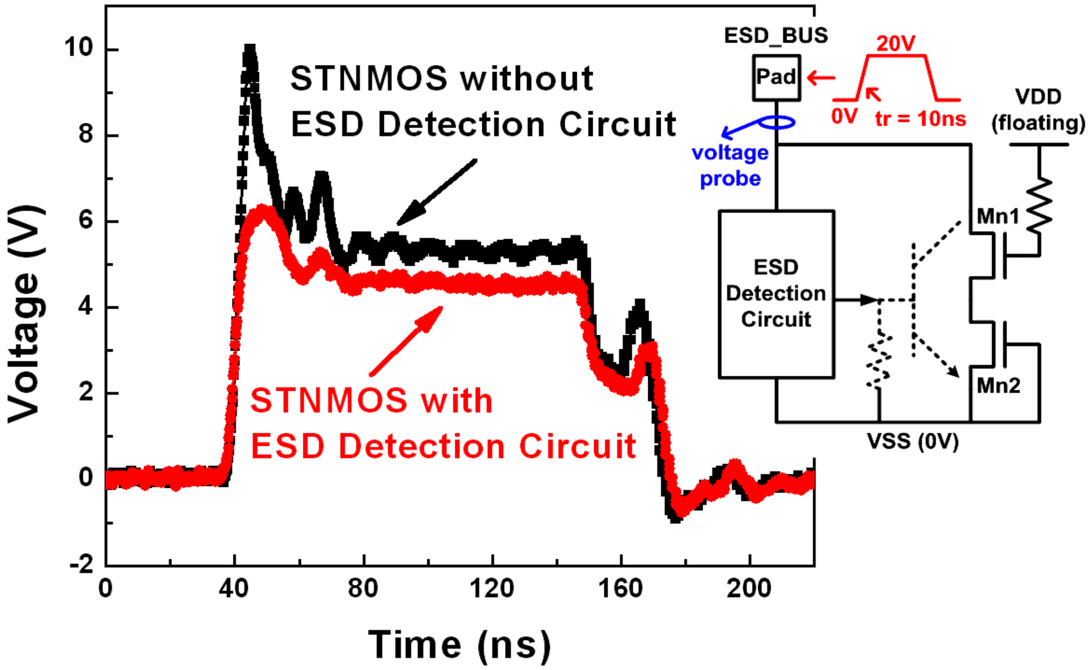


Fig. 4.13 The measured voltage waveform of STNMOS with or without the ESD detection circuit under 0 to 20V voltage pulse with a rise time of 10 ns on the ESD_BUS pad.

CHAPTER 5

ESD PROTECTION FOR AUTOMOTIVE VACUUM-FLUORESCENT-DISPLAY (VFD) DRIVER IC

In this chapter, a new electrostatic discharge (ESD) protection structure of high-voltage P-type silicon controlled rectifier (HVPSCR) embedded into the high-voltage PMOS device is proposed to greatly improve ESD robustness of the vacuum-fluorescent-display (VFD) driver IC for automotive electronics applications [73], [74]. By only adding the additional N+ diffusion into the drain region of high-voltage PMOS, the TLP-measured secondary breakdown current (It2) of output driver has been greatly improved greater than 6A in a 0.5-µm high-voltage CMOS process. Such ESD-enhanced VFD driver IC, which can sustain human-body-model (HBM) ESD stress of up to 8kV, has been in mass production for automotive applications in car without latchup problem. Moreover, with device widths of 500µm, 600µm, and 800µm, the machine-model (MM) ESD levels of the HVPSCR are as high as 1100V, 1300V, and 1900V, respectively [74].

5.1 Original Design for VFD I/O

The high-voltage output cell of the automotive VFD driver IC fabricated in a 0.5-µm high-voltage CMOS process is shown in Fig. 5.1. In this VFD driver IC, the output pull-up function is realized by the high-voltage PMOS (HVPMOS) which is connected between output pad and VDD of 5V, whereas the pull-down function is realized by the on-chip resistor of 300 kohm for vacuum fluorescent display. The resistor is connected from the output pad to VEE of -40V for VFD applications. Here, the internal core circuits are connected to the low voltage power supply with VDD of 5V and VSS of 0V.

5.1.1 Device Structure and I-V Characteristic of the HVPMOS

The device structure of the HVPMOS is drawn in Fig. 5.2. The high-voltage region is surrounded by the high-voltage (HV) P-well of lightly doped concentration with a specified clearance from the HV P-well edge to the drain (P+ diffusion) of the HVPMOS, where the clearance is indicated as C in Fig. 5.2. Such HV P-well with lightly doped concentration will provide the drain of HVPMOS with high enough breakdown voltage for VFD application. The breakdown voltage of the HVPMOS is specified to be higher than 45V for this VFD application.

While measuring the I-V characteristic of the HVPMOS in VFD driver I/O cell, the gate of the HVPMOS is connected to the core circuits. The DC I-V curve of HVPMOS in low-current region measured by curve tracer 370 is shown in the Fig. 5.3, where the breakdown voltage of this HVPMOS is ~ 65V. When the applied voltage is slightly larger than the breakdown voltage, the current will be increased sharply. While the HVPMOS is switching from off-state to the on-state, the DC I-V curve behavior is shown in the curve of the Fig. 5.3 marked with “on”. However, while the HVPMOS is switching from on-state to the off-state, the DC I-V curve behavior is shown in the curve of the Fig. 5.3 marked with “off”. There is no obvious snapback characteristic found in the DC I-V curve of HVPMOS. The TLP-measured I-V curve of the HVPMOS with a width of 600μm and a length of 2μm is shown in Fig. 5.4(a). The trigger voltage (Vt1) of TLP-measured I-V curve of HVPMOS is ~35V. Due to the inefficient parasitic p-n-p bipolar action in the HVPMOS, no obvious snapback characteristic is found. Therefore, the secondary breakdown current (It2) is only 0.07A which is quite low for ESD protection. Moreover, the TLP-measured I-V curve of the HVPMOS with a larger device size (with a width of 800μm and a length of 2μm) is shown in Fig. 5.4(b), the It2 is still only 0.08A. Here, the difference on trigger voltage of the HVPMOS measured by DC and TLP is caused by transient-coupling effect. The TLP is designed with a rise time of 10ns to simulate the HBM ESD event. The fast TLP dV/dt transient voltage at the drain could be coupled into the device through the parasitic capacitance in the drain/bulk junction to lower the trigger voltage.

5.1.2 ESD Robustness and Failure Analysis

The HBM ESD levels and TLP-measured It2 of the HVPMOS in VFD driver I/O cell with different device widths (but keeping the same length) are listed in Table I. With device widths of 500μm, 600μm, and 800μm, the It2 of the HVPMOS are 0.04A, 0.07A, and 0.08A, respectively. For such a lower It2, the HBM ESD levels of the HVPMOS are all about ~500V under the negative-to-VDD (ND-mode) ESD stress. Here, the failure criterion is defined at the leakage current greater than 1μA under a 45-V bias on the devices. The measured I-V curves of the HVPMOS (with a width of 600μm and a length of 2μm) in VFD driver I/O cell before and after 1-kV ND-mode HBM ESD stress is shown in Fig. 5.5, where the voltage applied at VDD with the output pad grounded is swept from 0 to 45V. Before ESD stress, the HVPMOS is turned off so that there is no leakage current between VDD and output pad. However, after ESD stress, the HVPMOS is burned out to cause a short circuit in the I-V curve. The failure analysis (FA) picture of this output cell on the HVPMOS (with a width of 600μm and a length of 2μm) after 1-kV ND-mode HBM ESD stress is shown in Fig. 5.6(a), where serious contact spiking from drain to source of the HVPMOS is found. Moreover, the enlarged pictures of contact spiking in the source and drain regions are shown in Fig. 5.6(b) and 5.6(c), respectively, where the lightened contacts are damaged by HBM ESD stress. Due to the too low TLP-measured It2 and ESD levels, the HVPMOS is not suitable as the ESD protection device for the output cell of VFD driver IC.

5.2 New ESD Design for VFD I/O

A new ESD protection structure with the high-voltage p-type SCR (HVPSCR) embedded into the output HVPMOS is proposed to greatly improve ESD robustness of the automotive VFD driver IC. The output cell with the embedded HVPSCR for automotive VFD drive IC is shown in Fig. 5.7. With the addition of power-rail ESD clamp circuit [8], the positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) ESD stresses on the output pin can be discharged through HVPSCR to VSS or VDD with the cooperation of power-rail ESD clamp circuit.

5.2.1 Device Structure and Turn-on Mechanism of the HVPSCR

The device structure of the HVPSCR embedded into output HVPMOS is drawn in Fig. 5.8, where an additional N+ diffusion is inserted into the drain region in the HV P-well of HVPMOS. The SCR path in the HVPSCR is from VDD to the output pad which is composed by P+ diffusion (source of HVPMOS), N-well, HV P-well (drain of HVPMOS), and N+

diffusion in HV P-well. Here, only an additional N+ diffusion is added into the HVPMOS to form the HVPSCR for ESD protection. So, only a little increase of silicon area is used to realize this HVPSCR. The final die size of the VFD driver IC with the proposed HVPSCR for ESD protection is almost kept the same.

The equivalent circuit of the HVPMOS with the embedded HVPSCR device is shown in Fig. 5.9, where the anode of HVPSCR is connected to VDD and the cathode of HVPSCR is connected to the output pad. The HVPSCR device is composed of a lateral PNP bipolar transistor and a vertical NPN bipolar transistor to form a 2-terminal/4-layer PNPN (P+/N-well/HV P-well/N+) structure. The trigger voltage of the HVPSCR device is the same as that of the HVPMOS, which is determined by the drain avalanche breakdown voltage of the N-well/HV P-well junction. Such that, while the overstress voltage reaches the breakdown voltage of N-well/HV P-well junction, the embedded HVPSCR will be triggered on to discharge ESD current. The turn-on mechanism of HVPSCR is somewhat similar to PMOS triggered SCR [75], [76], where PMOS is first turned on by the ESD transient pulse, then SCR can be triggered on when the current reaches the trigger current of SCR.

During the PD-mode ESD stress, the positive ESD voltage is applied to the output pad and VDD is relatively grounded. The parasitic diode (N-well/HV P-well junction) of the HVPMOS will be forward biased to clamp the ESD voltage. During the ND-mode ESD stress, the negative ESD voltage is applied to the output pad and VDD is relatively grounded. When the magnitude of the applied voltage is greater than the drain breakdown voltage of HVPMOS, the hole and electron current will be generated through the avalanche breakdown mechanism. The electron current will flow through the N-well to N+ diffusion connected to anode of HVPSCR, which will lower the voltage level of the N-well. As long as the voltage drop across the N-well resistor ($R_{\text{N-well}}$) is greater than the turn-on voltage of lateral PNP transistor, the lateral PNP transistor will be triggered on to keep HVPMOS into its breakdown region. While the lateral PNP transistor is turned on, the hole current will be injected through the HV P-well into P+ diffusion (connected to cathode of HVPSCR) to increase the voltage level of HV P-well. As the injected hole current is larger than some critical value, the voltage drop across the HV P-well resistor ($R_{\text{HV P-well}}$) will be greater than the turn-on voltage of the vertical NPN transistor. The vertical NPN transistor will be turned on to inject the electron current through the N-well into N+ diffusion to further bias the lateral PNP transistor. Such positive feedback regeneration physical mechanism [77], [78] will initiate the latching action in the HVPSCR. Finally, the HVPSCR will be successfully triggered into its latching state with the positive-feedback regenerative mechanism [77], [78] Once the HVPSCR is triggered on, the required holding current to keep the NPN and PNP transistors on can be generated through the positive-feedback regenerative mechanism of latchup without involving the avalanche breakdown mechanism again. So, the HVPSCR will have a lower holding voltage than that of HVPMOS. Therefore, the ND-mode ESD current can be effectively discharged by the HVPSCR to protect the VFD driver IC.

The latchup issue [79], [80] should be considered when the HVPSCR is used for ESD protection. When ICs are in normal circuit operating conditions, the HVPSCR device could be accidentally triggered on by noise pulse [81]. However, for VFD application, during normal circuit operating conditions, the current from VDD through HVPSCR to VEE will be limited to some smaller value of ~ 0.15mA by the large pull-down resistor R of 300kohm. Such a limited current is much lower than the holding current (~35mA, from the measured result in silicon) of the HVPSCR, which can avoid latchup issue between the power lines during normal circuit operating conditions. On the other hand, if the HVPMOS is triggered on by the transient noise pulse, the unwanted transient noise current will flow through the HVPMOS and absorbed by VDD power supply. Therefore, the latchup problem will not occur in such VFD driver IC with the HVPSCR embedded into the HVPMOS.

5.2.2 ESD Protection Design for VFD I/O with Both HVPSCR and Power-Rail ESD Clamp Circuit

To sustain a high ESD robustness for VFD I/O, the power-rail ESD clamp circuit between VDD and VSS is added to support ESD discharge path between output pad and VSS. The power-rail ESD clamp circuit composed by resistor, capacitor, inverter and NMOS is shown in Fig. 5.10. Here, the RC value is designed with a time constant of about ~ 1μs to distinguish the VDD power-on event (with a rise time in milliseconds) or ESD stress events (with a rise time in nanoseconds) [8]. During the normal VDD power-on transition (from low to high), the input of the inverter can follow up in time with the power-on VDD voltage to keep the output of the inverter at zero. Hence, the NMOS device is kept off and does not interfere with the functions of the internal circuits. When a positive ESD voltage is applied to VDD with VSS relatively grounded, the RC delay will keep the input of the inverter at a low-voltage level within a relative long time. Therefore, the output of the inverter will be pulled high by the ESD energy to trigger on the NMOS device. While the NMOS device is turned on, the ESD current is discharged from VDD to VSS through the NMOS device.

When a negative ESD voltage is applied to VDD with VSS relatively grounded, the negative ESD current can be discharged through the forward-biased drain-to-bulk parasitic diode in the NMOS.

The ESD current paths of the new proposed ESD protection for VFD I/O in four ESD-stress modes are shown in Figs. 5.11(a) ~ 5.11(d). Under PS-mode ESD-stress condition, the ESD current will flow from output pad through the parasitic diode of HVPMOS to VDD, and then through power-rail ESD clamp circuit to VSS. Under NS-mode ESD-stress condition, the ESD current will flow from VSS through power-rail ESD clamp circuit to VDD, and then through the HVPSCR to output pad. Under PD-mode ESD-stress condition, the ESD current will flow from output pad through the parasitic diode of HVPMOS to VDD. Under ND-mode ESD-stress condition, the ESD current will flow from VDD through the HVPSCR to the output pad. Therefore, the new proposed ESD protection design can provide a higher ESD level for such VFD driver ICs.

For VFD application, because of the large resistor R of 300kohm between output pad and VEE, the ESD current from output pad to VEE will be limited by the resistor R. Hence, both positive and negative ESD stresses on the output pad with VEE relatively grounded can sustain high ESD robustness.

5.3 Experimental Results

5.3.1 I-V Characteristic of the HVPSCR

The DC I-V curve of the HVPSCR measured by curve tracer 370 under room temperature of 25°C is shown in Fig. 5.12(a), where the DC trigger voltage of HVPSCR is ~ 65V, which is the same as that of HVPMOS. Before the SCR path is triggered on, the DC I-V curve behavior of HVPSCR is the same as that of HVPMOS. When the current is larger than ~ 5mA, the embedded HVPSCR is triggered on into its holding state with a DC holding voltage of ~ 5V. While the HVPSCR is switching from off-state to the on-state, the DC I-V curve behavior is shown in the curve of the Fig. 5.12(a) marked with “on”. However, while the HVPSCR is switching from on-state to the off-state, the DC I-V curve behavior is shown in the curve of the Fig. 5.12(a) marked with “off”, where the holding current is about ~ 35mA. Because the holding voltage of the HVPSCR is smaller than the operation voltage (45V), the HVPSCR could be triggered on to suffer latchup failure in VFD driver IC by the transient noise pulse. However, the maximum DC operation current across the pull-down resistor R between the output pad and the VEE power pad is 0.15mA. This DC current is obtained from the maximum voltage drop which is 45V (between VDD and VEE) divided by 300kohm when the pull-up HVPMOS is turned on. The current of 0.15mA is less than the DC holding current (~ 35mA) of the HVPSCR, which can avoid the latchup issue between the power lines during normal operating conditions. Moreover, the DC I-V curve of the HVPSCR measured by curve tracer 370 under the temperature of 125°C is shown in Fig. 5.12(b), where the holding voltage (current) is decreased from ~ 5V (~ 35mA) to ~ 3V (~ 20mA) as the temperature is increased from 25°C to 125°C. Though the latchup problem is very sensitive to the high temperature, the maximum current flowing across the resistor is still kept at 0.15mA for the high temperature due to the large resistor R. The HVPSCR can not stay in its turn-on state if the supplied current is smaller than its holding current. Hence, even for the high ambient temperatures as 125°C, the HVPSCR is still kept at the off-state to avoid the latchup problem. Hence, under normal circuit operating conditions, the HVPSCR can be free to latchup problem between the power lines in the VFD driver IC despite of a potentially low DC holding voltage below the operation voltage.

The TLP-measured I-V curve of the HVPSCR with a width of 600µm and a length of 2µm is shown in Fig. 5.13. The trigger voltage of the HVPSCR in the TLP-measured I-V curve is about ~53V and the trigger current is about 0.27A. Moreover, in the inset figure, a high trigger current of almost 0.27A can be obviously found, where the latchup immunity can be achieved over 200mA by preventing unwanted triggering during normal circuit operation. Here, before HVPSCR is triggered on, HVPMOS will handle the low TLP current. As the TLP current is higher than 270mA, the HVPSCR will be fully turned on. With the excellent clamping behavior of the HVPSCR, a very low holding voltage of the HVPSCR can be obtained around 5V. According to the power dissipation of P=I×V, where I indicates the ESD discharge current and V indicates the holding voltage of the device, the device with a lower holding voltage during ESD stress can sustain a higher ESD level. The TLP-measured It2 of HVPSCR is greater than 6A which is much higher than that (0.07A) of HVPMOS. So, the HVPSCR can indeed sustain a much higher ESD level for the output cell of this VFD driver IC.

From the previous work [82], a similar solution was proposed to improve the ESD robustness in a smart power IC. An ESD robust output switch, called SCR-LDMOS, was modified from the standard lateral LDMOS without any additional processing, where the device structure of SCR-LDMOS is re-drawn in Fig. 5.14 [82]. The characteristics of the SCR-LDMOS are kept the same as those of the LDMOS during normal circuit operating conditions and the SCR (P+/N-well/P-well/N+) will be turned on to a low holding voltage to discharge the ESD current during ESD stress. However, no n-type high-voltage device (such as HVNMOS) was provided in this work with the cost-efficient CMOS process for VFD driver IC. So, such a SCR-LDMOS can't be applied in our VFD driver IC to improve ESD robustness. Moreover, the use of SCR-LDMOS in smart-power technology has still to watch the latchup problem during normal circuit operating conditions. In our work, the use of the HVPSCR did not cause latchup problem between the power lines in such VFD driver IC due to the large resistor R between output pad and VEE.

5.3.2 ESD Robustness of the VFD Driver IC

TLP-measured It2, human-body-model (HBM) and machine-model (MM) ESD levels of the HVPSCR under different device widths (but keeping the same length) are shown in Table II. The It2 of the HVPSCR with device widths of 500μm, 600μm, and 800μm are all over 6A, whereas the HBM ESD levels can pass over 8kV under ND-mode ESD stress. Moreover, with device widths of 500μm, 600μm, and 800μm, the MM ESD levels of the HVPSCR are 1100V, 1300V, and 1900V, respectively. With both the new proposed HVPSCR embedded into the HVPMOS and the power-rail ESD clamp circuit, the HBM ESD robustness of the output cell in the automotive VFD driver IC has been successfully improved from 500V up to 8kV within almost the same die size.

The partial layout view of this VFD driver IC with HVPSCR in I/O cell is shown in Fig. 5.15, which can fully meet the ESD specification of automotive applications. Moreover, the automotive driver IC has also successfully passed the 200mA quasi-static latchup test of EIA/JEDEC standard [83]. Such an ESD-enhanced driver IC has been in mass production for the VFD applications in car.

5.4 Summary

The HVPMOS is not suitable for ESD protection in VFD driver IC for automotive electronics applications due to a poor ESD level. To greatly improve ESD robustness, a new ESD protection structure of HVPSCR embedded into the HVPMOS is proposed by only adding an additional N+ diffusion into the drain region of HVPMOS. With almost the same layout area, the It2 of the output cell has been improved over 6A, as well as, the HBM ESD level of such VFD driver IC with HVPSCR can sustain up to 8 kV. With device widths of 500µm, 600µm, and 800µm, the MM ESD levels of the HVPSCR are 1100V, 1300V, and 1900V, respectively. Moreover, the automotive driver IC can also pass the 200mA quasi-static latchup test.

Table 5.1

TLP_It2 and HBM ESD levels under negative-to-VDD ESD stresses of the HVPMOS.

HVPMOS Device Width (Length=2μm)	500μm	600μm	800μm
TLP_It2	0.04A	0.07A	0.08A
HBM ESD Level Under ND-mode ESD Stress	<500V	<500V	<500V

Table 5.2

TLP_It2, HBM and MM ESD levels under negative-to-VDD ESD stresses of the HVPSCR.

HVPSCR+HVPMOS Device Width (Length=2μm)	500μm	600μm	800μm
TLP_It2	>6A*	>6A*	>6A*
HBM ESD Level Under ND-mode ESD Stress	>8kV*	>8kV*	>8kV*
MM ESD Level Under ND-mode ESD Stress	1100V	1300V	1900V

*limitation due to the maximum level of test equipments

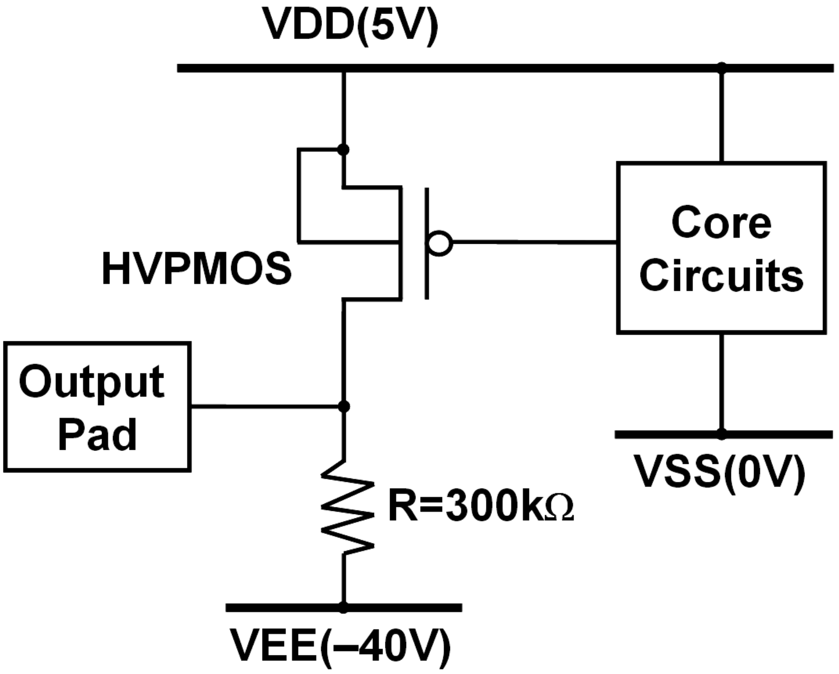


Fig. 5.1 The original output cell of the automotive VFD driver IC realized with the high-voltage PMOS (HVPMOS) and pull-down resistor.

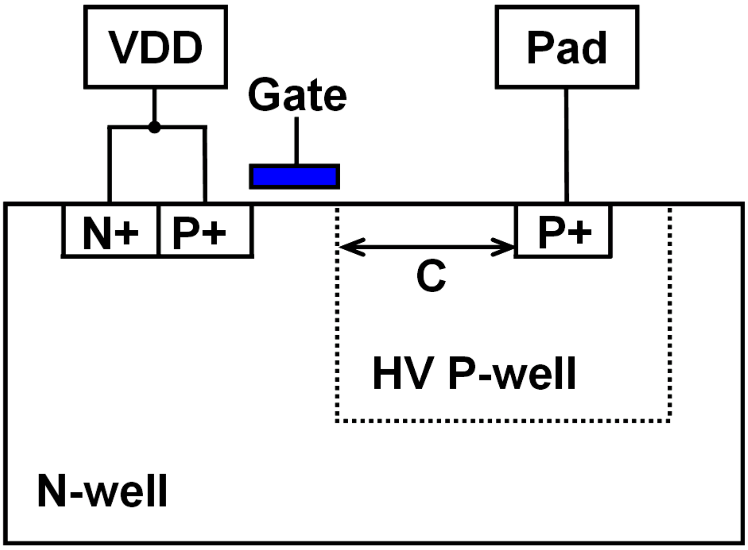


Fig. 5.2 The device structure of HVPMOS in the specific CMOS process. A HV P-well is used to surround the drain of HVPMOS to meet the HV application.

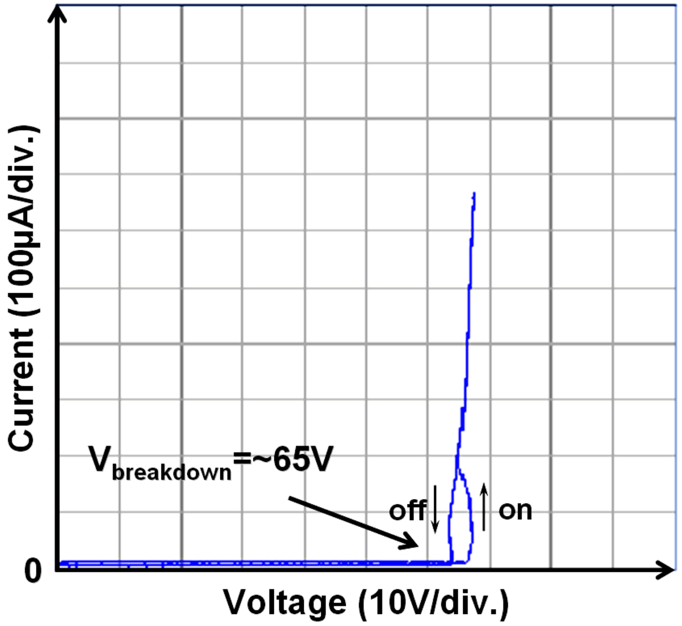
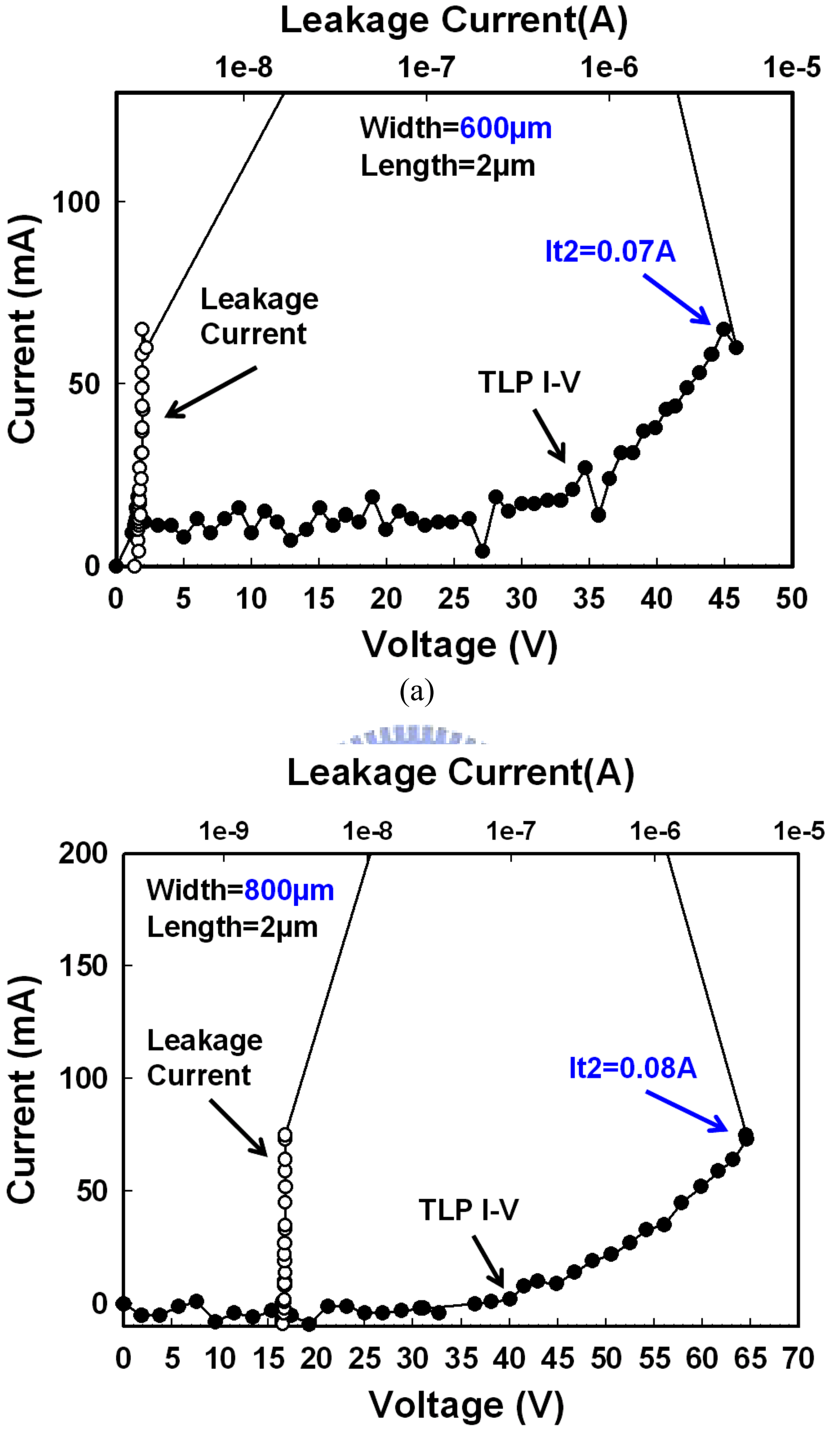


Fig. 5.3 The DC I-V curve of HVPMOS in low-current region, which has a breakdown voltage of 65V.



(a)

(b)

Fig. 5.4 The TLP-measured I-V curves of HVPMOS (a) with a width of 600µm and a length of 2µm, and (b) with a width of 800µm and a length of 2µm.

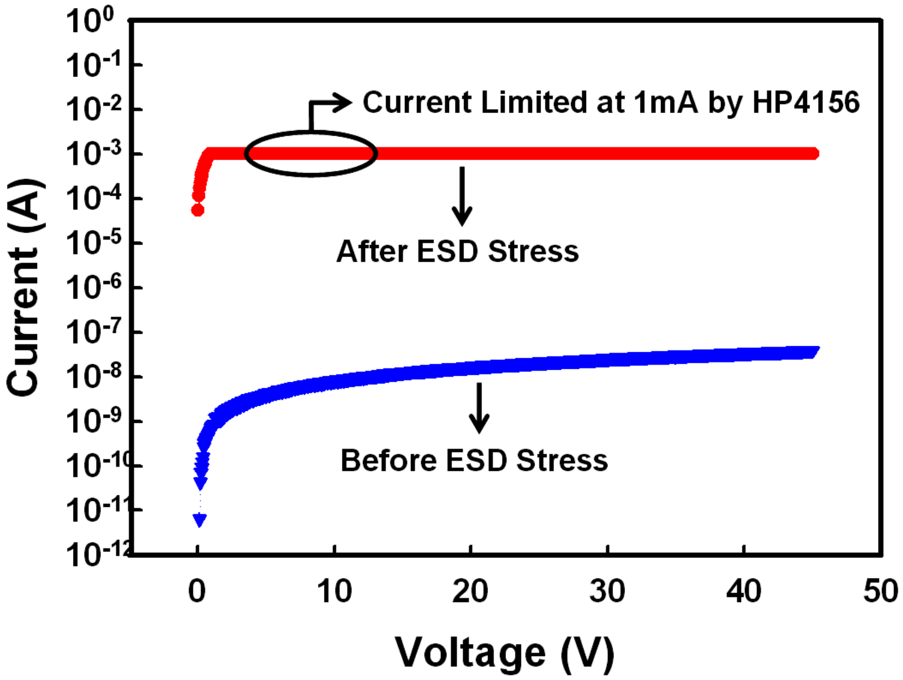
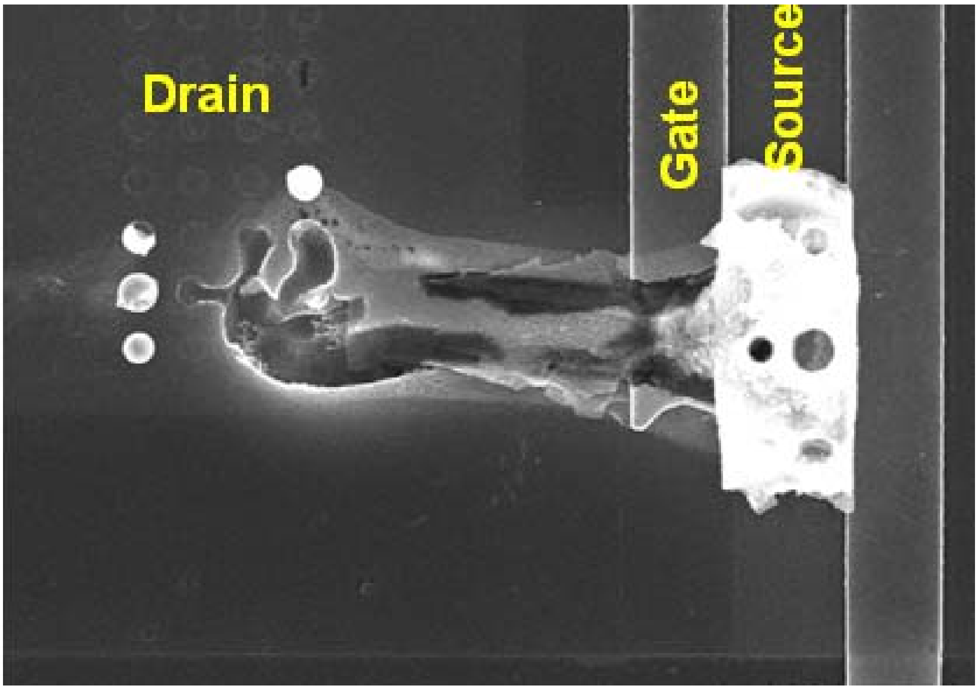
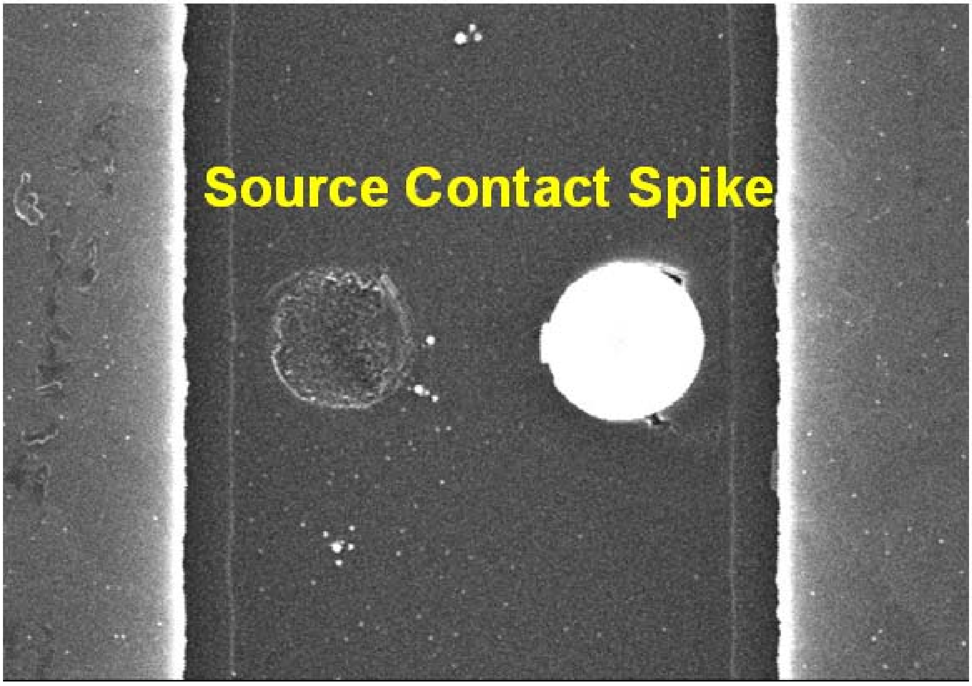


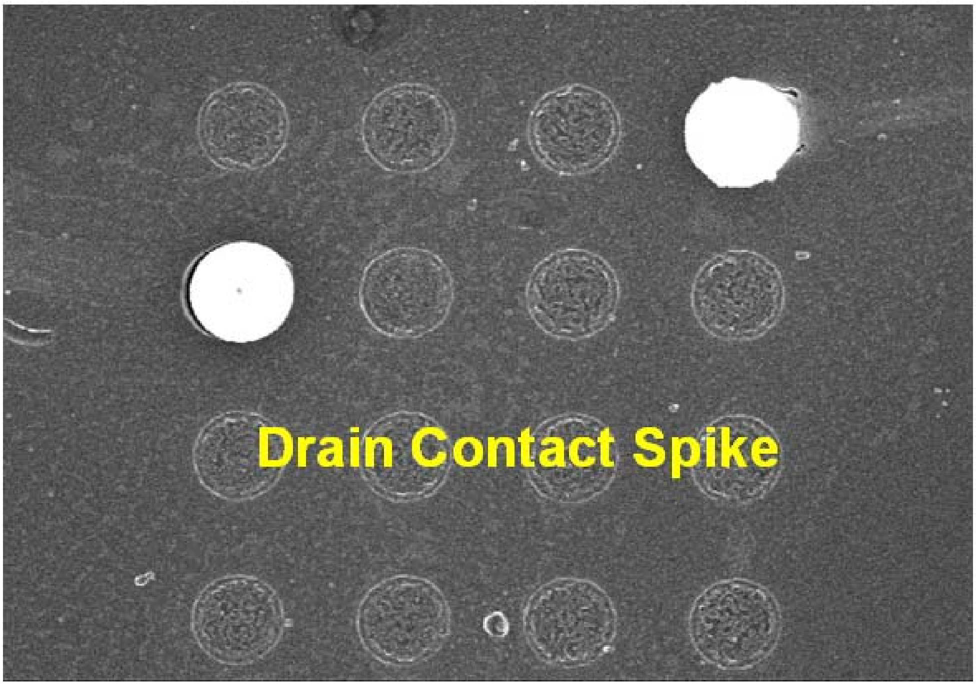
Fig. 5.5 The measured I-V curves of the HVPMOS (with a width of 600μm and a length of 2μm) in VFD driver I/O cell before and after 1-kV ND-mode HBM ESD stress.



(a)



(b)



(c)

Fig. 5.6 The SEM failure pictures of (a) the output HVPMOS with device width of 600μm and length of 2μm, (b) the contact spiking in the source region of HVPMOS, and (c) the contact spiking in the drain region of HVPMOS, in the VFD driver IC after 1-kV negative-to-VDD HBM ESD stress.

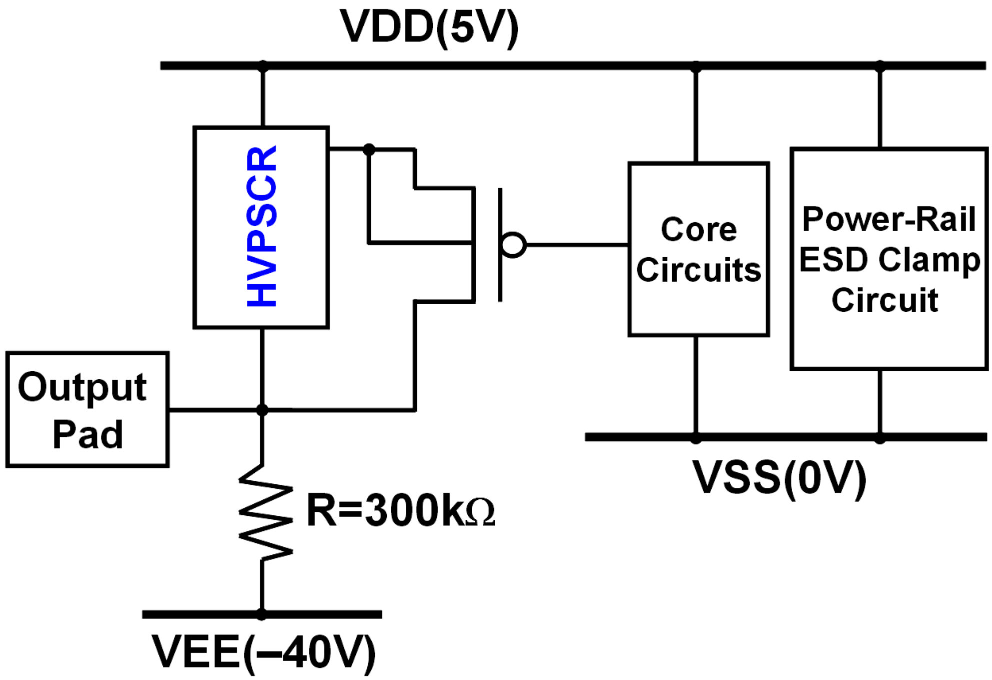


Fig. 5.7 The new proposed ESD protection design with the high-voltage p-type SCR (HVPSCR) embedded into the output HVPMOS to improve ESD robustness of output cell of the automotive VFD driver IC.

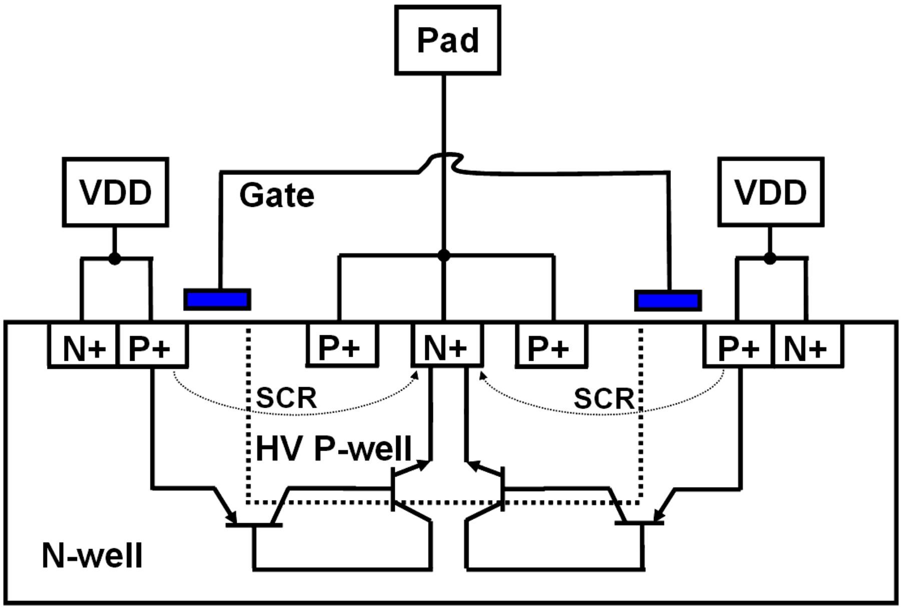


Fig. 5.8 The device structure of the HVPSCR embedded into the output HVPMOS.

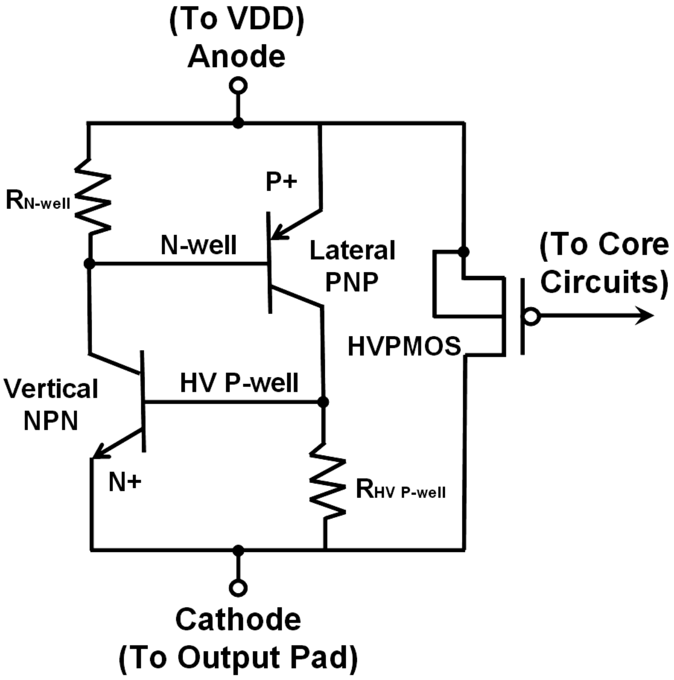


Fig. 5.9 The equivalent circuit of the HVPMOS with the embedded HVPSCR.

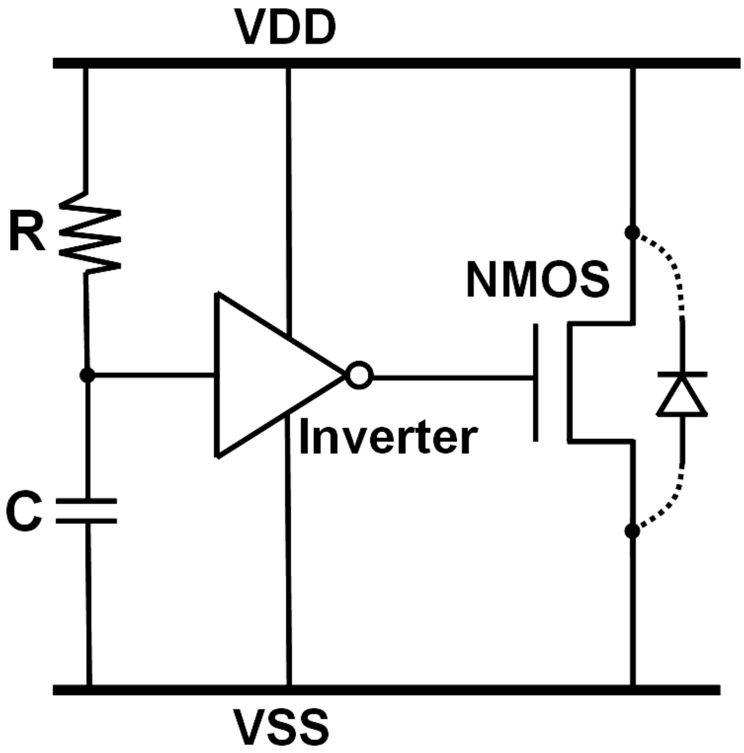
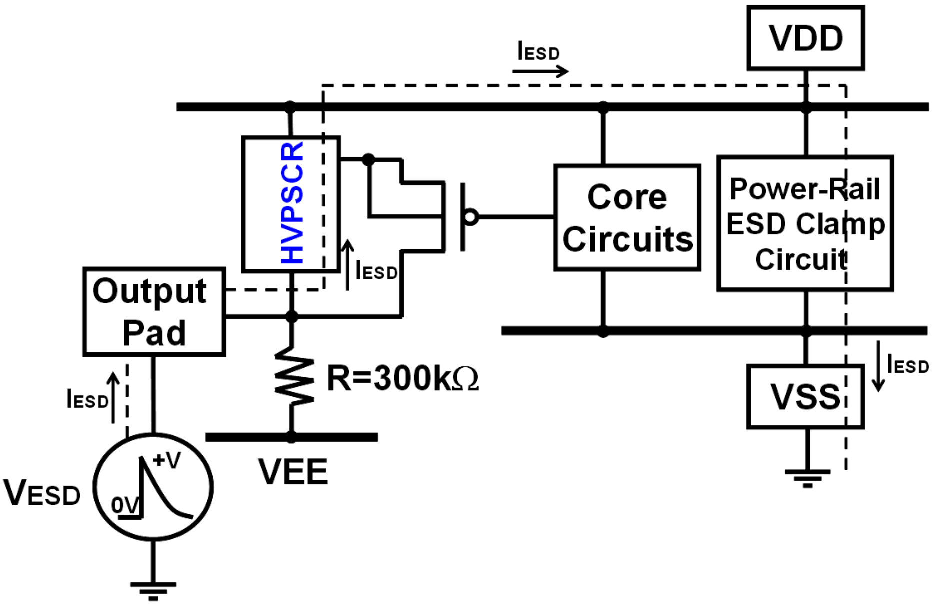
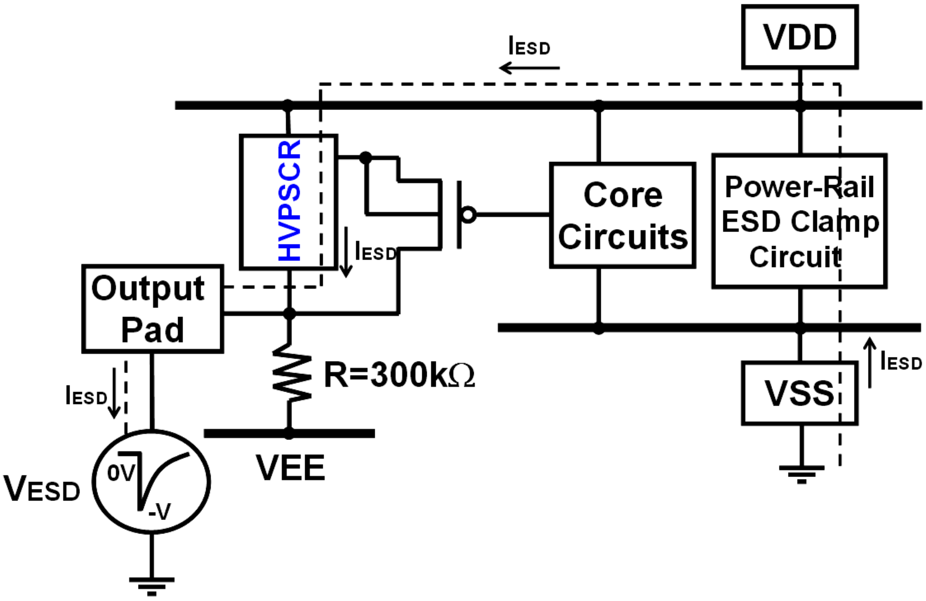


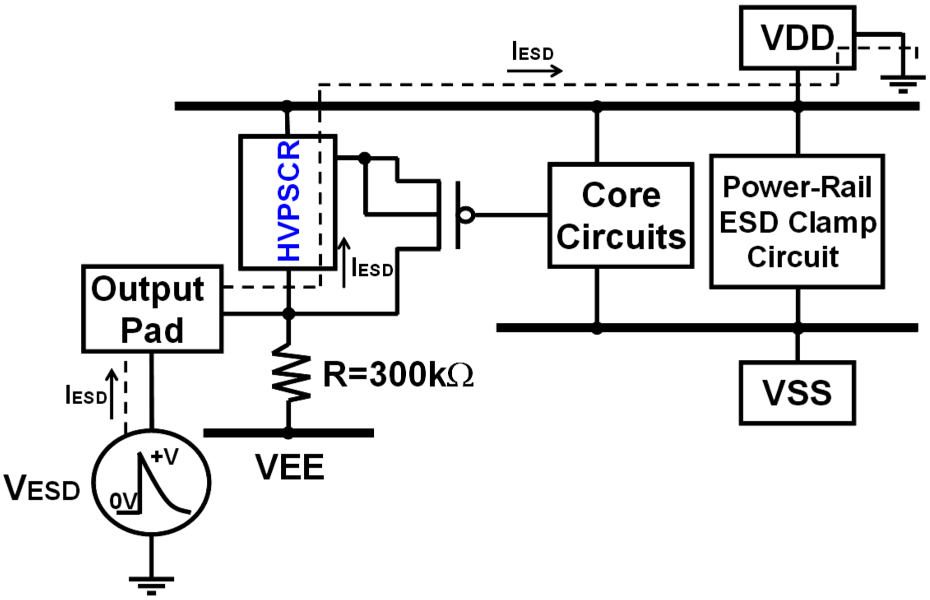
Fig. 5.10 The circuit schematic of the power-rail ESD clamp circuit which is composed by resistor, capacitor, inverter and NMOS.


VDD
IESD
HVPSCR
Core Circuits
Power-Rail ESD Clamp Circuit
IESD
Output Pad
R=300kΩ
IESD
IESD
VSS
VESD
+V
0V
VEE

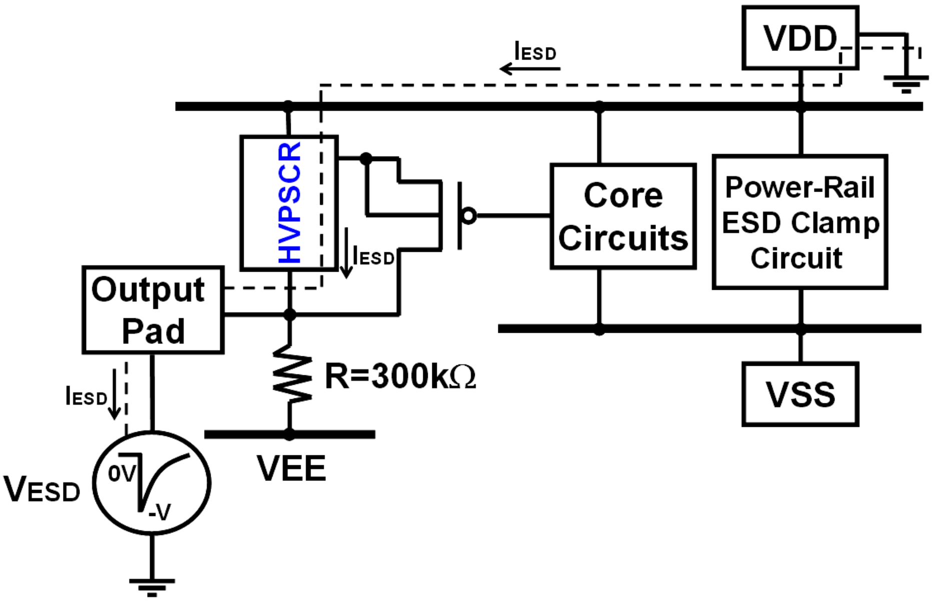
(a)


VDD
IESD
HVPSCR
Core Circuits
Power-Rail ESD Clamp Circuit
IESD
Output Pad
R=300kΩ
IESD
IESD
VSS
VESD
0V
-V
VEE

(b)

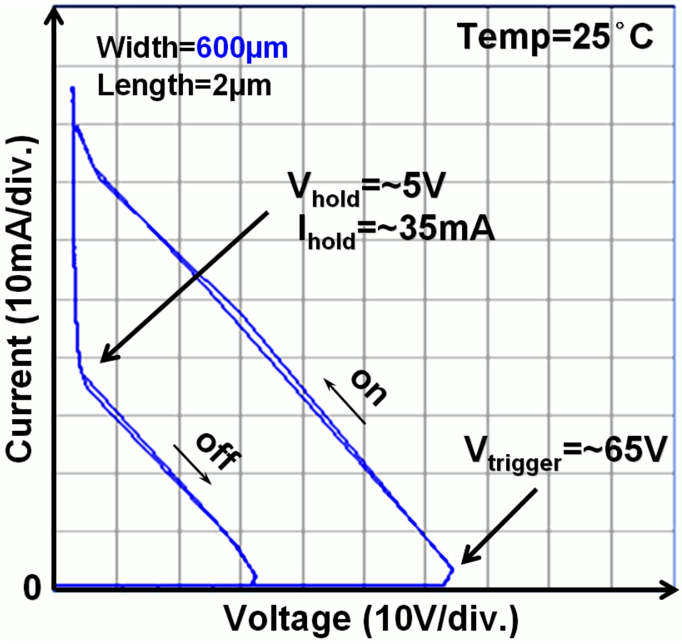


(c)

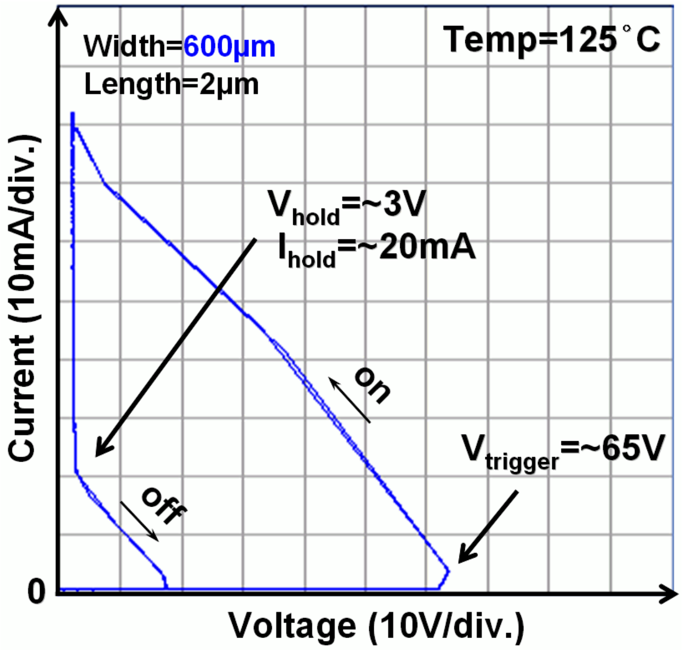


(d)

Fig. 5.11 The ESD current paths on the VFD driver IC with HVPSCR and power-rail ESD clamp circuit under (a) positive-to-VSS (PS-mode), (b) negative-to-VSS (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode) ESD-stress conditions.



(a)



(b)

Fig. 5.12 The DC I-V curves of the HVPSCR (a) with a DC trigger voltage of 65V and a holding voltage (current) of ~ 5V (~ 35mA) under the temperature of 25°C, and (b) with a DC trigger voltage of 65V and a holding voltage (current) of ~ 3V (~ 20mA) under the temperature of 125°C.

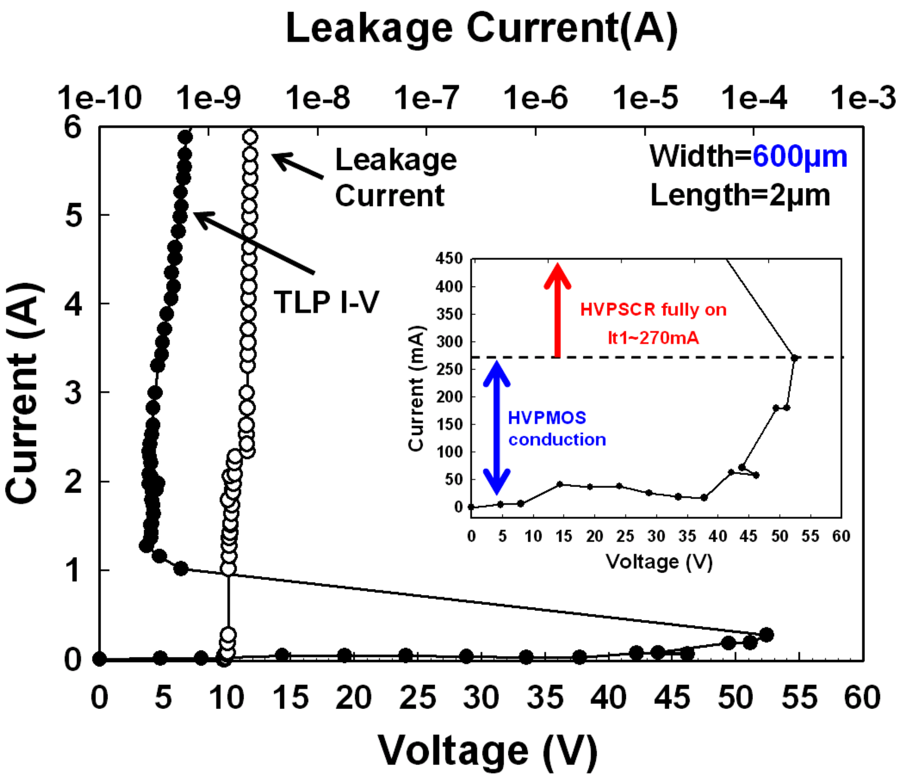


Fig. 5.13 The TLP-measured I-V curve of HVPSCR with a width of 600µm and a length of 2µm. A high trigger current of ~ 270mA can be seen in the inset figure drawn in the low-current region, so the HVPSCR can be fully triggered on when the current reaches above 270mA.

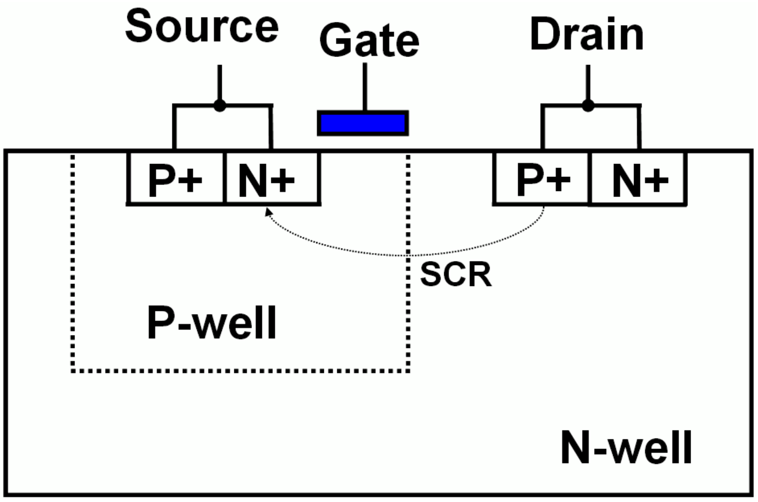


Fig. 5.14 The device structure of SCR-LDMOS [82].

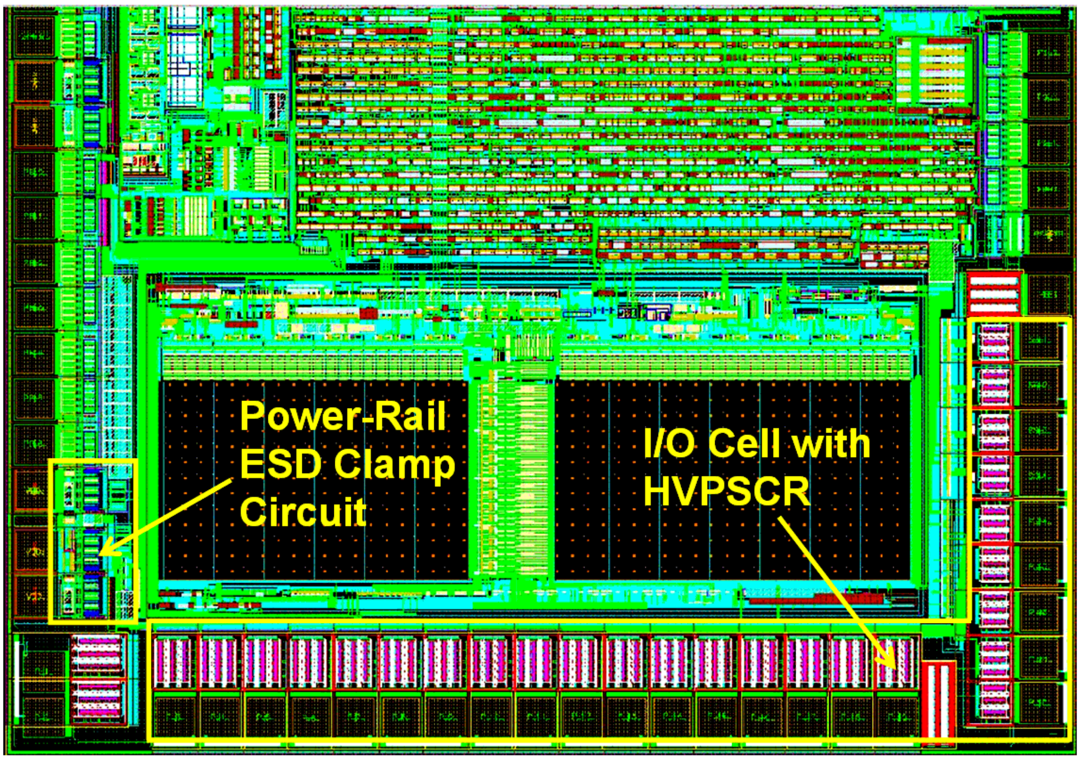


Fig. 5.15 The partial layout view of the VFD driver IC with the HVPSCR in I/O cell, which can sustain HBM ESD stress of up to 8kV.

CHAPTER 6

ESD ROBUSTNESS OF ON-CHIP ESD PROTECTION DEVICES IN 40-V CMOS TECHNOLOGY

In this chapter, the dependences of drift implant and layout parameters on ESD robustness in a 40-V CMOS process have been investigated in silicon chips [84], [85]. From the experimental results, the high-voltage (HV) MOSFETs without drift implant in the drain region have better TLP-measured It2 and ESD robustness than those with drift implant in the drain region. Furthermore, the It2 and ESD level of HV MOSFETs can be increased as the layout spacing from the drain diffusion to polygate is increased. It was also demonstrated that a specific test structure of HV n-type silicon controlled rectifier (HVNSCR) embedded into HV NMOS without N-drift implant in the drain region has the excellent TLP-measured It2 and ESD robustness. Moreover, due to the different current distributions in HV NMOS and HVNSCR, the dependences of the TLP-measured It2 and HBM ESD levels on the spacing from the drain diffusion to polygate are different [85].

6.1 Device Structures in 40-V CMOS Process

To integrate the high-voltage devices while maintaining the characteristics of the standard 0.35-μm low-voltage CMOS process without changing all of the design rules and device parameters, the device structures of high-voltage MOSFET can be achieved by adding several additional mask layers in the standard 0.35-μm CMOS technology. The additional mask layers are HV N-well, HV P-well, N-drift or P-drift, N-grade or P-grade, and N-field or P-field. The HV N-well and HV P-well in the HV region are complementary layers which are fabricated on the same P-substrate. The lightly doped N-drift (P-drift), N-grade (P-grade), and N-field (P-field) implants are required for high voltage MOSFETs to sustain the high voltage (40V) during normal operating conditions in 0.35-μm 40-V CMOS process.

In the given 0.35-μm 40-V CMOS process, the device structures in the test chip can be classified as: (1) HV NMOS with or without N-drift implant in the drain region, (2) HV PMOS with or without P-drift implant in the drain region, and (3) HV n-type SCR (HVNSCR) embedded into HV NMOS with or without N-drift implant in the drain region.

6.1.1 HV NMOS With or Without N-Drift Implant

The device cross-sectional views of HV NMOS with or without N-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 6.1(a) and 6.1(b), respectively. The HV NMOS is fabricated in the HV P-well, as shown in Fig. 6.1(a), where the P-field implant is used as isolation ring to isolate the device from the other. The N-grade implant is used to increase the breakdown voltage of the drain region in the HV NMOS. Moreover, the HV NMOS has lightly doped N-drift implant below the field oxide in the drain region, and utilizes the field oxide between the gate and the drain contact to minimize the peak electric field around the corner of the drain region, which can avoid the hot carrier effect in the N-channel. The device structure of HV NMOS without N-drift implant was also fabricated, as shown in Fig. 6.1(b), where the N-drift in the drain region was removed.

The trigger voltage of the HV NMOS device is determined by the drain avalanche breakdown voltage of the N-grade/HV P-well junction. While the overstress voltage reaches the breakdown voltage of N-grade/HV P-well junction, the parasitic lateral n-p-n BJT in HV NMOS will be triggered on to discharge ESD current.

6.1.2 HV PMOS With or Without P-Drift Implant

The device cross-sectional views of HV PMOS with or without P-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 6.2(a) and 6.2(b), respectively. The HV PMOS is fabricated in the HV N-well, as shown in Fig. 6.2(a), where the purpose of N-field implant is the same as the P-field implant used in HV NMOS to isolate device from the other. The P-grade implant in the drain region is also used to increase its breakdown voltage for high voltage application. The lightly doped P-drift implant below the field oxide is also used to avoid the hot carrier effect in the P-channel. The device structure of HV PMOS without P-drift implant was also fabricated, as shown in Fig. 6.2(b), where the P-drift in the drain region was removed.

The trigger voltage of the HV PMOS device is determined by the drain avalanche breakdown voltage of the P-grade/HV N-well junction. While the overstress voltage reaches the breakdown voltage of P-grade/HV N-well junction, the parasitic lateral p-n-p BJT in HV PMOS will be triggered on to discharge ESD current.

6.1.3 HVNSCR With or Without N-Drift Implant

It has been well known that SCR has a good ESD protection capability. Hence, to improve the ESD robustness of HV NMOS, the part of drain region in HV NMOS was replaced by P+ diffusion to form a SCR structure in the device, where the P+ diffusion is conjunction with N+ diffusion in the drain region. The device cross-sectional views of HVNSCR with or without N-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 6.3(a) and 6.3(b), respectively. The SCR path in the HV NMOS was composed by P+ diffusion in the drain region, N-grade, HV P-well, N+ diffusion in the source region. Here, no extra layout area is needed to realize this HVNSCR structure in HV NMOS.

The HVNSCR device is composed of a lateral n-p-n BJT and a vertical p-n-p BJT to form a 2-terminal/4-layer PNPN (P+/N-grade/HV P-well/N+) structure. The trigger voltage of the HVNSCR device is the same as that of the HV NMOS, which is determined by the drain avalanche breakdown voltage of the N-grade/HV P-well junction. While the overstress voltage reaches the breakdown voltage of N-grade/HV P-well junction, the HV NMOS will be first triggered on by the ESD transient pulse, and then the embedded HVNSCR will be triggered on to discharge ESD current.

The equivalent circuit of the HVNSCR device embedded into HV NMOS is shown in Fig. 6.4. When the magnitude of the applied voltage is greater than the drain breakdown voltage of HV NMOS, the hole and electron currents will be generated through the avalanche breakdown mechanism. The hole current will flow through the HV P-well to P+ diffusion connected to the P-field ring of HV NMOS, which will increase the voltage level of the HV P-well. As long as the voltage drop across the HV P-well resistor ($R_{HV\ P\text{-}well}$) is greater than the cut-in voltage of lateral n-p-n BJT, the lateral n-p-n BJT will be triggered on to keep HV NMOS into its breakdown region. While the lateral n-p-n BJT is turned on, the electron current will be injected through the N-grade into N+ diffusion in the drain of HV NMOS to lower the voltage level of N-grade. As the injected electron current is larger than some critical value, the voltage drop across the N-grade resistor ($R_{N\text{-}grade}$) will be greater than the cut-in voltage of the vertical p-n-p BJT. The vertical p-n-p BJT will be turned on to inject the hole current through the HV P-well into P+ diffusion to further bias the lateral n-p-n BJT. Such positive feedback regeneration physical mechanism [77], [78] will initiate the latching action in the HVNSCR. Finally, the HVNSCR will be successfully triggered into its latching state by the positive-feedback regenerative mechanism [77], [78]. Once the HVNSCR is triggered on, the required holding current to keep the n-p-n and p-n-p BJTs on can be generated through the positive-feedback regenerative mechanism of latchup without involving the avalanche breakdown mechanism again.

6.2 Experimental Results and Discussion

6.2.1 TLP-Measured I-V Characteristics

To simulate the human-body-model (HBM) [1] ESD event, the transmission line pulsing generator (TLPG) [86] is designed to generate the stable and consistent pulses of very high current in a very short period of time. To investigate the device behavior during HBM ESD stress, the TLP with a pulse width of 100ns and a rise time of 10ns has been widely used to measure the secondary breakdown current (It2) of ESD devices. In the test chip, the device dimension (W/L) of HV NMOS was 200μm/3μm and the device dimension (W/L) of HV PMOS was 200μm/4μm, where the minimum device lengths (L) of HV NMOS and HV PMOS are 3μm and 4μm, respectively, in the given 0.35-μm 40-V CMOS process. The device dimension (W/L) of HVNSCR is also kept the same as that of HV NMOS. Generally, the ESD robustness is highly dependent on the ESD current discharging path among HV MOSFETs. In HV MOSFETs, the location of ESD damage is usually occurred at the drain region. Therefore, in this test chip, the drift implant in the drain region and the layout spacing (D) from the drain diffusion to polygate were split to see its impact on ESD performance.

The TLP-measured I-V curves of HV gate-grounded NMOS (GGNMOS) with or without N-drift implant in the drain region are shown in Fig. 6.5, where the layout spacing from the drain diffusion to polygate (D, as shown in Fig. 6.1) is split to find the dependence on TLP-measured It2. The breakdown voltage of HV GGNMOS with or without N-drift implant is about 70V~75V, which is higher than the operation voltage of 40V. When the parasitic n-p-n BJT in HV GGNMOS is turned on, it will snap back with a low holding voltage. Comparing to other HV CMOS processes with deeper N-well and n+ buried layer

(NBL) [87], no double-snapback characteristic was found in the TLP-measured I-V curves of HV GGNMOS in the given 0.35-µm 40-V CMOS process with the shallower N-grade implant. The double-snapback characteristic occurs while the ESD current path changes from vertical direction (deeper region) to lateral direction (shallower region) [87], [36]. However, the ESD current flows only in the lateral direction due to the shallower N-grade implant.

In Fig. 6.5(a), with N-drift implant in the drain region, the TLP-measured It2 of HV GGNMOS are 1.1A, 1.5A, and 1.7A for the spacing D of 5.5µm, 7.5µm, and 9.5µm, respectively. The trigger voltage and holding voltage will be increased when the spacing D is increased. In Fig. 6.5(b), without N-drift implant in the drain region, the TLP-measured It2 of HV GGNMOS are 1.3A, 1.6A, and 1.9A for the spacing D of 5.5µm, 7.5µm, and 9.5µm, where the It2 and the holding voltage are obviously increased as the parameter D is increased. The trigger voltage is 75V which is independent to the spacing D.

Comparing Fig. 6.5(a) and Fig. 6.5(b), under the same spacing of D, the HV GGNMOS without N-drift implant in the drain region has a higher It2 than that with N-drift implant in the drain region. To further illustrate the impact of N-drift implant on the turn-on mechanism of HV GGNMOS, the simulated current distributions of HV GGNMOS before and after the parasitic n-p-n BJT is triggered on are shown in Fig. 6.6 and 6.7, respectively. Because the doping concentration of N-grade implant is higher than that of N-drift implant, the breakdown voltage of the N-grade/HV P-well junction is lower than that of the N-drift/HV P-well junction. Some part of current among HV GGNMOS with N-drift implant flows through the N-grade/HV P-well junction, as shown by the indicated region A in Fig. 6.6(a). This part of current flows from drain into HV P-well and finally to source, which results in a longer current path to trigger on the parasitic n-p-n BJT. So, the TLP-measured I-V curves appear a high resistance region before the parasitic n-p-n BJT in HV GGNMOS is turned on. Here, a higher trigger voltage is needed to turn on the parasitic n-p-n BJT in HV GGNMOS with N-drift implant, where the trigger voltage will be increased when the spacing D is increased due to a longer current path. The other part of current among HV GGNMOS with N-drift implant flows through the corner between the N-drift implant and the channel, as shown by the indicated region B in Fig. 6.6(a). This part of current could cause the current crowding at the channel surface to damage the device easily while the parasitic n-p-n BJT being triggered on. Moreover, the current path of HV GGNMOS without N-drift implant flows directly from drain through the N-grade/HV P-well junction to source, as shown in Fig. 6.6(b). Hence, the trigger voltage is kept the same as the breakdown voltage of N-grade/HV

P-well while the spacing D is increased. Most of the current flows from drain to source instead of into the HV P-well, which would not cause a longer current path to trigger on the parasitic n-p-n BJT. So, HV GGNMOS without N-drift implant in the drain region can switch to its snapback region quickly with a lower holding voltage, which in turn results in a higher TLP-measured It2. Here, due to a little part of current path through the corner between the N-drift implant and the channel of HV GGNMOS with N-drift implant, as shown at the indicated region of B in Fig. 6(a), the measured breakdown voltage (70V) of the HV GGNMOS with N-drift implant under the spacing D of 5.5um could be somewhat a little lower than the measured breakdown voltage (75V) of the HV GGNMOS without N-drift implant under the spacing D 5.5um in the TLP I-V curves.

For HV GGNMOS with N-drift implant in Fig. 6.7(a), while the voltage reaches to the trigger voltage (the breakdown voltage of the N-drift/HV P-well junction), the current starts to flow through the N-drift/HV P-well junction and the parasitic n-p-n BJT of HV GGNMOS is turned on into the snapback region. After the parasitic n-p-n is triggered on, the ESD current in HV GGNMOS with N-drift implant will concentrate around the N-drift implant region, as shown in Fig. 6.7(a), which causes the device damage easily. On the contrary, the ESD current in HV GGNMOS without N-drift implant will flow more uniformly and deeper into the HV P-well to avoid the current crowding, as shown in Fig. 6.7(b), which in turn can sustain higher ESD stress [88]. Hence, HV GGNMOS without N-drift implant in the drain region has a higher It2 than that with N-drift implant in the drain region due to the different current distributions among the devices. Moreover, the It2 and holding voltage of HV GGNMOS with or without N-drift implant are increased while the spacing D is increased. Though the power dissipation is higher due to the higher holding voltage, the device can still achieve a higher It2 since the ESD current is spread deeper into the device [36].

The TLP-measured I-V curves of HV gate-VDD PMOS (GDPMOS) with or without P-drift implant in the drain region are shown in Fig. 6.8, where the spacing D is also split to find its impact on It2. The trigger voltage of HV GDPMOS with or without P-drift is ~80V, which is higher than the operation voltage of 40V in the given 0.35-μm 40-V CMOS process. When the parasitic p-n-p BJT of HV GDPMOS is triggered on, the current will be increased as the voltage is increased. Because the mobility of electron is higher than that of hole, the current gain of the parasitic p-n-p BJT in HV GDPMOS is lower than that of the parasitic n-p-n BJT in HV GGNMOS. Moreover, the base distance of the parasitic p-n-p BJT in HV GDPMOS (4μm) is longer than that of the parasitic n-p-n BJT in HV GGNMOS (3μm), which results in the more inefficient parasitic p-n-p bipolar action in the HV GDPMOS. Hence, there is no snapback characteristic in TLP-measured I-V curves of HV GDPMOS as compared with HV GGNMOS.

In Fig. 6.8(a), with P-drift implant in the drain region, the It2 of HV GDPMOS are 0.01A, 0.01A, and 0.06A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, respectively. After the parasitic p-n-p is triggered on, the current of HV GDPMOS will be slightly increased as the voltage is increased. When the voltage reaches to over 110V, the current will suddenly increase to burn out the HV GDPMOS. Moreover, In Fig. 6.8(b), without P-drift implant in the drain region, the It2 of HV GDPMOS are 0.13A, 0.1A, and 0.14A for the spacing D of 5.5μm, 7.5μm and 9.5μm, respectively, where the It2 is slightly increased as the parameter D is increased.

Comparing Fig. 6.8(a) and Fig. 6.8(b), under the same spacing of D, the HV GDPMOS without P-drift implant in the drain region has a higher It2 than that with P-drift implant in the drain region. In Fig. 6.2(a), because the ESD current of HV GDPMOS with P-drift implant flows in the longer current path through the P-grade/HV N-well junction, the TLP-measured I-V curves appear a high turn-on resistance and a higher holding voltage. In Fig. 6.2(b), the current path of HV GDPMOS without P-drift implant flows directly through the P-grade/HV N-well junction. Hence, the turn-on resistance of GDPMOS without P-drift implant in the drain region is much lower than that with P-drift implant in the drain region, which will result in the lower holding voltage and higher It2.

Table I summarizes the dependence of TLP-measured It2 of HV GGNMOS and GDPMOS with or without drift implant under different spacings D. Because no snapback characteristic is found in the TLP-measured I-V curves of HV GDPMOS, the holding voltage of HV GDPMOS is much higher than that of HV GGNMOS, which results in a lower It2 of HV GDPMOS. For both HV GGNMOS and HV GDPMOS with the same spacing of D, the device without drift implant in the drain region has a higher It2 than that with drift implant in the drain region due to the different current distributions among the devices. Moreover, HV MOSFETs with drift implant in the drain region has the longer current path than that without drift implant in the drain region.

The TLP-measured I-V curves of HVNSCR with or without N-drift implant in the drain region under different layout spacings D are shown in Fig. 6.9. Though the measured trigger voltage of HVNSCR is lower than that of HV GGNMOS, it is still higher than the operation voltage of 40V in the given 0.35-μm 40-V CMOS process. After the HVNSCR is triggered on into its snapback region, it will keep at the lower holding voltage.

In Fig. 6.9(a), with N-drift implant, the TLP-measured It2 of HVNSCR are 4.9A, 4A, and 2.4A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, where the It2 is obviously increased as the spacing D is decreased. While the spacing D is increased, the distance from anode to cathode of SCR path is increased, which results in the increase of the holding voltage [29]. In Fig. 6.9(b), without N-drift implant, the TLP-measured It2 of HVNSCR are all over 6A for the spacing D of 5.5μm, 7.5μm, and 9.5μm. Comparing Fig. 6.9(a) and Fig. 6.9(b), under the same spacing of D, the HVNSCR without N-drift implant in the drain region also has a higher It2 than that with N-drift implant in the drain region. Moreover, HVNSCR without N-drift implant in the drain region has a lower trigger voltage, which can be triggered on into its snapback region earlier.

Table II summarizes the dependence of TLP-measured It2 of HV GGNMOS and HVNSCR with or without N-drift implant under different spacings D. With the same spacing of D, both HV GGNMOS and HVNSCR without N-drift implant in the drain region have higher TLP-measured It2 than those with N-drift implant in the drain region. From the TLP-measured I-V curves, the trigger voltage and holding voltage of HVNSCR is lower than that of HV GGNMOS. Therefore, the TLP-measured It2 of HVNSCR is higher than that of HV GGNMOS. In HV GGNMOS, only the drain avalanche breakdown current can be generated to the HV P-well to trigger on the parasitic lateral n-p-n BJT. In HVNSCR, the parasitic vertical p-n-p BJT can be turned on because part of the current can flow from P+ diffusion of the drain region to HV P-well. The parasitic vertical p-n-p BJT can also provide a current to trigger on the parasitic lateral n-p-n BJT. Furthermore, with the turned on vertical p-n-p BJT, the current in HVNSCR flows more deeply into the HV P-well as compared to HV GGNMOS, which can make the current more uniform distribution among the HVNSCR to sustain higher ESD stress. Due to the different current distributions in HV GGNMOS and HVNSCR, the dependences of TLP-measured It2 on the spacing of D are different. For HV GGNMOS, as the spacing of D is increased, the ESD discharge energy will not concentrate at the local drain region and the ESD current can be spread deeper into the device, which results in the higher TLP-It2. However, for HVNSCR, as the spacing of D is increased, the trigger and holding voltage of SCR path is increased, which results in a lower TLP-It2.

6.2.2 HBM ESD Robustness

HBM ESD events are produced by the discharge of a charged 100pF capacitor through a 1.5kOhm resistor. The HBM ESD levels of HV GGNMOS, HV GDPMOS, and HVNSCR under different spacings D are shown in Figs. 6.10 ~ 6.12, respectively. In ESD test, the HBM levels are measured under the failure criterion defined as the I-V characteristic curve shifting over 30% from its original curve after three continuous ESD zaps at every ESD test voltage level.

In Fig. 6.10, the HBM ESD levels of HV GGNMOS with N-drift implant in the drain region are about 400V which is not enough for on-chip ESD protection device in HV CMOS ICs due to the low ESD robustness. By removing the N-drift implant in the drain region, the HBM ESD levels of HV GGNMOS with the same device dimension can be improved up to over 2kV. Moreover, while the spacing D is increased from 5.5μm to 9.5μm, the HBM ESD levels of HV GGNMOS without N-drift implant can be improved from 2kV to 2.8kV.

In Fig. 6.11, the HBM ESD levels of HV GDPMOS are only improved from 200V to 300V by removing the P-drift implant in its drain region. Moreover, the HBM ESD levels of HV GDPMOS are not increased when the spacing of D is increased with the minimum step of 100V in the measurement. Such a low ESD robustness of HV GDPMOS is not suitable for on-chip ESD protection device in HV CMOS ICs. To achieve a good on-chip ESD protection, the power-rail ESD clamp circuit [8] should be added across the power lines of HV CMOS ICs to avoid the ESD current flowing through HV GDPMOS in the breakdown operation.

In Fig. 6.12, the HBM ESD levels of HV GGNMOS can be greatly improved by replacing partial N+ diffusion in the drain region with P+ diffusion to form HVNSCR. The HBM ESD levels of HVNSCR can be further improved by removing the N-drift implant in drain region. Here, the HBM ESD levels of HVNSCR are not obviously increased when the spacing of D is decreased. For HVNSCR without N-drift implant in the drain region, the variation on the measured data is increased as the spacing D is increased. From these experimental results, HVNSCR with high ESD level can be used as a good on-chip ESD protection device for HV CMOS ICs.

Because of the strong snapback phenomenon with a lower holding voltage in HV GGNMOS and HVNSCR, the non-uniform turn-on mechanism may occur among the devices, which could cause the HBM ESD test results not to correlate well with TLP measurements (It2). The TLP could serve effectively as a voltage and current limiter (similar to ballasting resistor) that could improve device's robustness in high current region, while the limiting mechanism doesn't exist in real HBM ESD event [89]. So, the devices with and without N-drift implant could be uniformly turned on during TLP measurement. Moreover, the ESD current among the devices without N-drift implant will flow more uniformly and deeper into the HV P-well to avoid the current crowding, so the devices without N-drift implant could serve as the devices with a ballasting resistor to force device uniform turn-on and to improve its ESD robustness. Hence, as comparing to the TLP-measured It2, the HBM ESD levels of the HV devices have a significant improvement by removing the N-drift implant.

6.2.3 Failure Analysis

The failure analysis (FA) pictures of HV GGNMOS, HV GDPMOS, and HVNSCR after 3-kV, 400-V, and 5-kV HBM ESD stresses are shown in Figs. 6.13, 6.14 and 6.15, respectively. In Fig. 6.13, the contact spiking was found in the drain region of the HV GGNMOS without N-drift implant under the spacing of 7.5μm after 3-kV HBM ESD stress. In Fig. 6.14, the contact spiking was also found in the drain region of the HV GDPMOS without P-drift implant under the spacing of 7.5μm after 400-V HBM ESD stress. Moreover, in Fig. 6.15, the contact spiking was found in the drain region of the HVNSCR without N-drift implant under the spacing D of 7.5μm after 5-kV HBM ESD stress.

6.3 Summary

The drift implant in the drain region and layout spacing (D) from the drain diffusion to polygate have been split to verify the ESD robustness of HV MOSFETs in a given 40-V CMOS process. It has been found that HV MOSFETs without drift implant in drain region have higher TLP-measured It2 and higher ESD robustness than those with drift implant in the drain region. Moreover, without N-drift implant, the It2 and ESD level of HV GGNMOS can be obviously improved as the spacing D is increased. The ESD robustness of HV GGNMOS can be improved up to 2-kV HBM by removing the N-drift implant in the drain region. The HVNSCR without N-drift implant in drain region has highest ESD performance in a given 40-V CMOS process. For HVNSCR, the TLP-measured It2 can be improved over 6A and the ESD robustness can be improved to 4-kV by removing N-drift implant in the drain region. Moreover, the ESD level and It2 of HV NMOS can be increased as the layout spacing D from the drain diffusion to polygate is increased. The ESD level and It2 of HVNSCR are increased as this spacing D is decreased.

Table 6.1

TLP-measured It2 of HV GGNMOS and HV GDPMOS with or without drift implant under different spacings D.

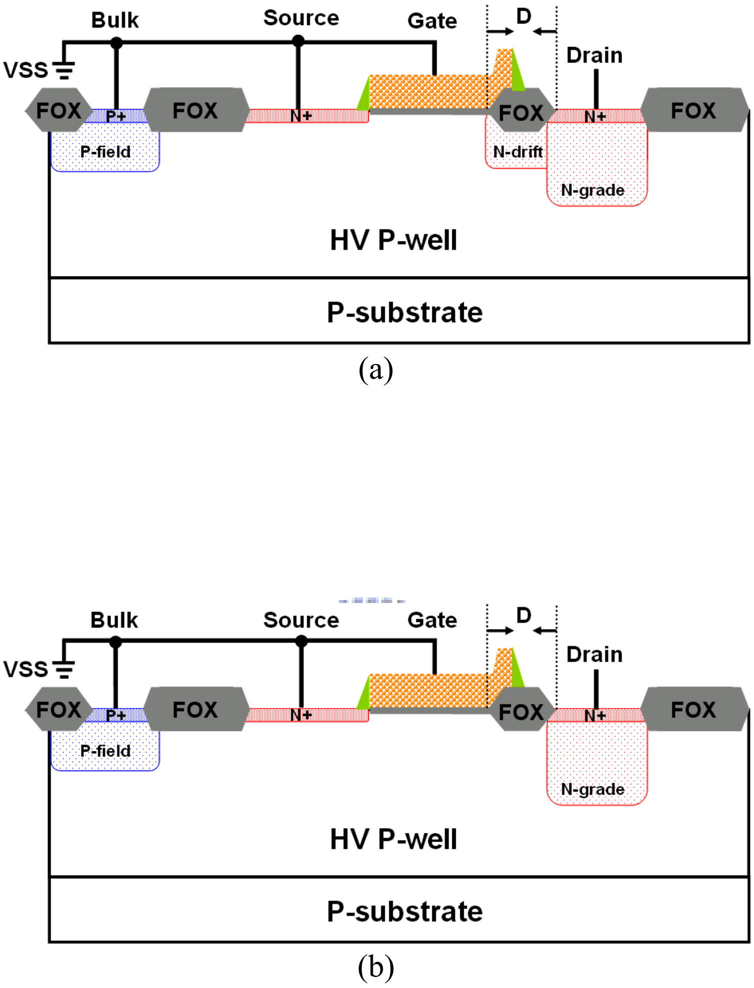
Spacing D in Layout	**5.5µm**	**7.5µm**	**9.5µm**
TLP-Measured It2 of HV GGNMOS (With N-Drift Implant)	**1.1A**	**1.5A**	**1.7A**
TLP-Measured It2 of HV GGNMOS (Without N-Drift Implant)	**1.3A**	**1.6A**	**1.9A**
TLP-Measured It2 of HV GDPMOS (With P-Drift Implant)	**0.01A**	**0.01A**	**0.06A**
TLP-Measured It2 of HV GDPMOS (Without P-Drift Implant)	**0.13A**	**0.1A**	**0.14A**

Table 6.2

TLP-measured It2 of HV GGNMOS and HVNSCR with or without drift implant under different spacings D.

Spacing D in Layout	**5.5µm**	**7.5µm**	**9.5µm**
TLP-Measured It2 of HV GGNMOS (With N-Drift Implant)	**1.1A**	**1.5A**	**1.7A**
TLP-Measured It2 of HV GGNMOS (Without N-Drift Implant)	**1.3A**	**1.6A**	**1.9A**
TLP-Measured It2 of HVNSCR (With N-Drift Implant)	**4.9A**	**4A**	**2.4A**
TLP-Measured It2 of HVNSCR (Without N-Drift Implant)	**>6A***	**>6A***	**>6A***

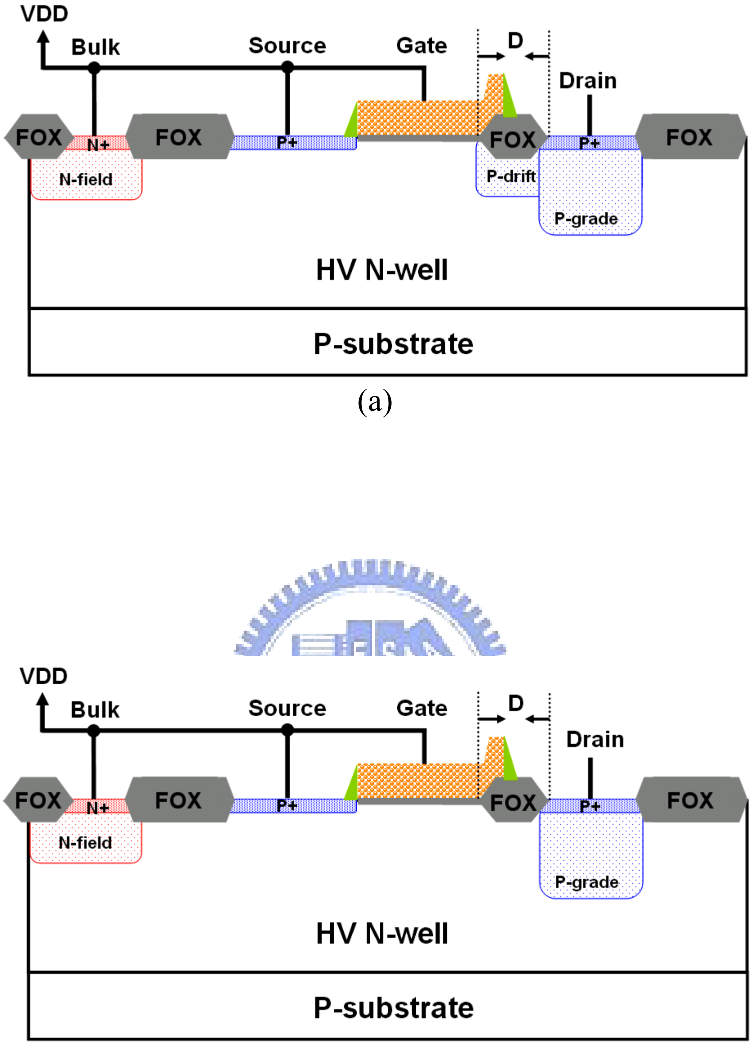
*limitation due to the maximum level of test equipments



(a)

(b)

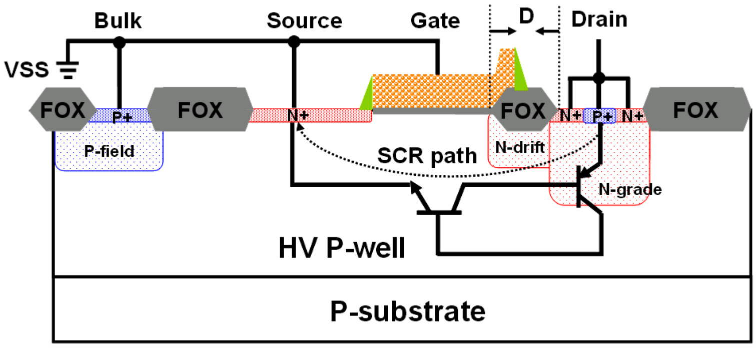
Fig. 6.1 The cross-sectional views of HV NMOS (a) with, and (b) without, N-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chip.



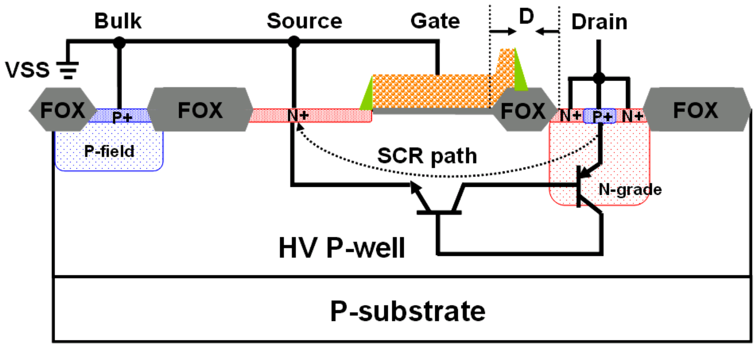
(a)

(b)

Fig. 6.2 The cross-sectional views of HV PMOS (a) with, and (b) without, P-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chip.



(a)



(b)

Fig. 6.3 The cross-sectional views of HVNSCR (a) with, and (b) without, N-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chip.

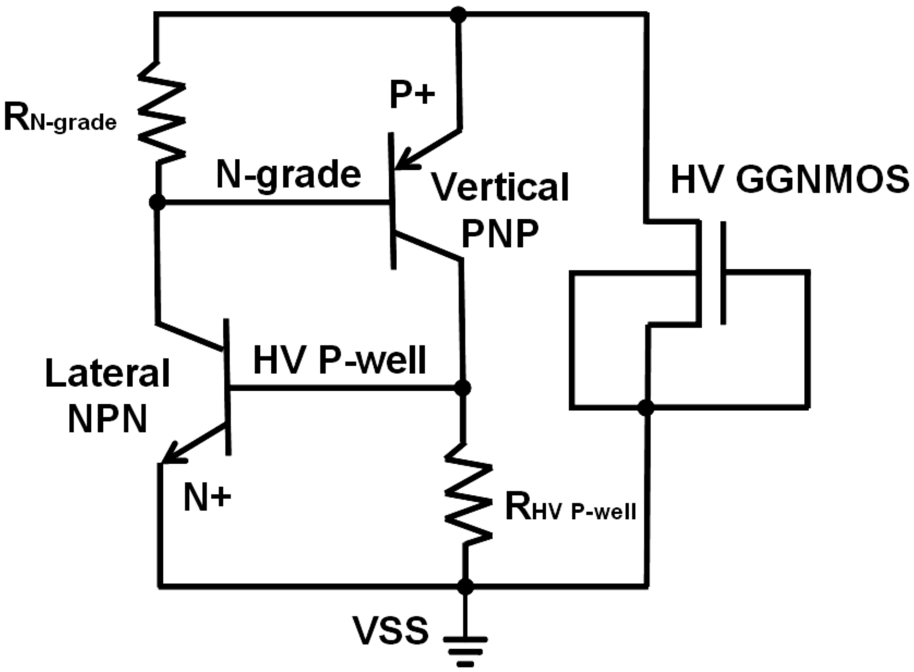
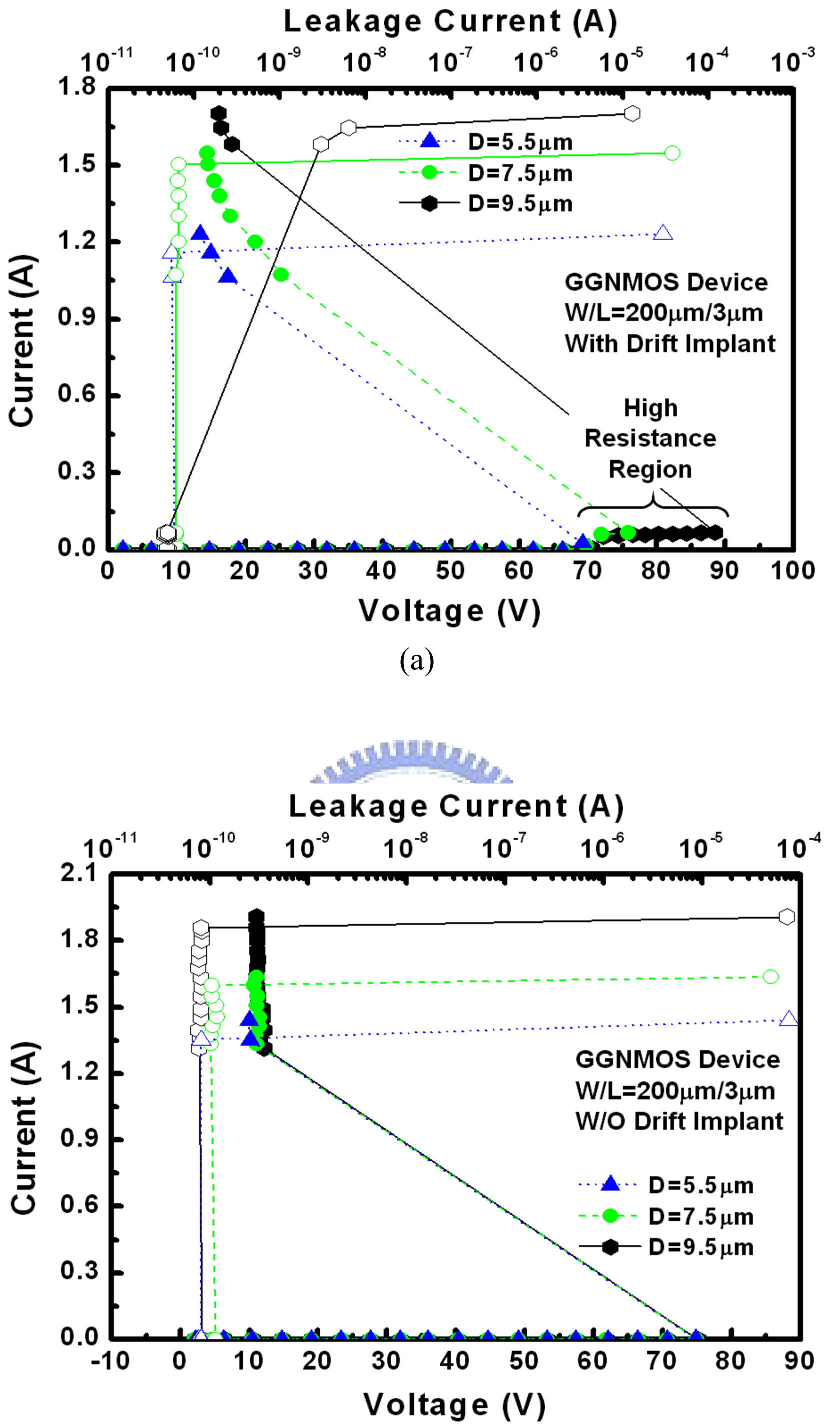


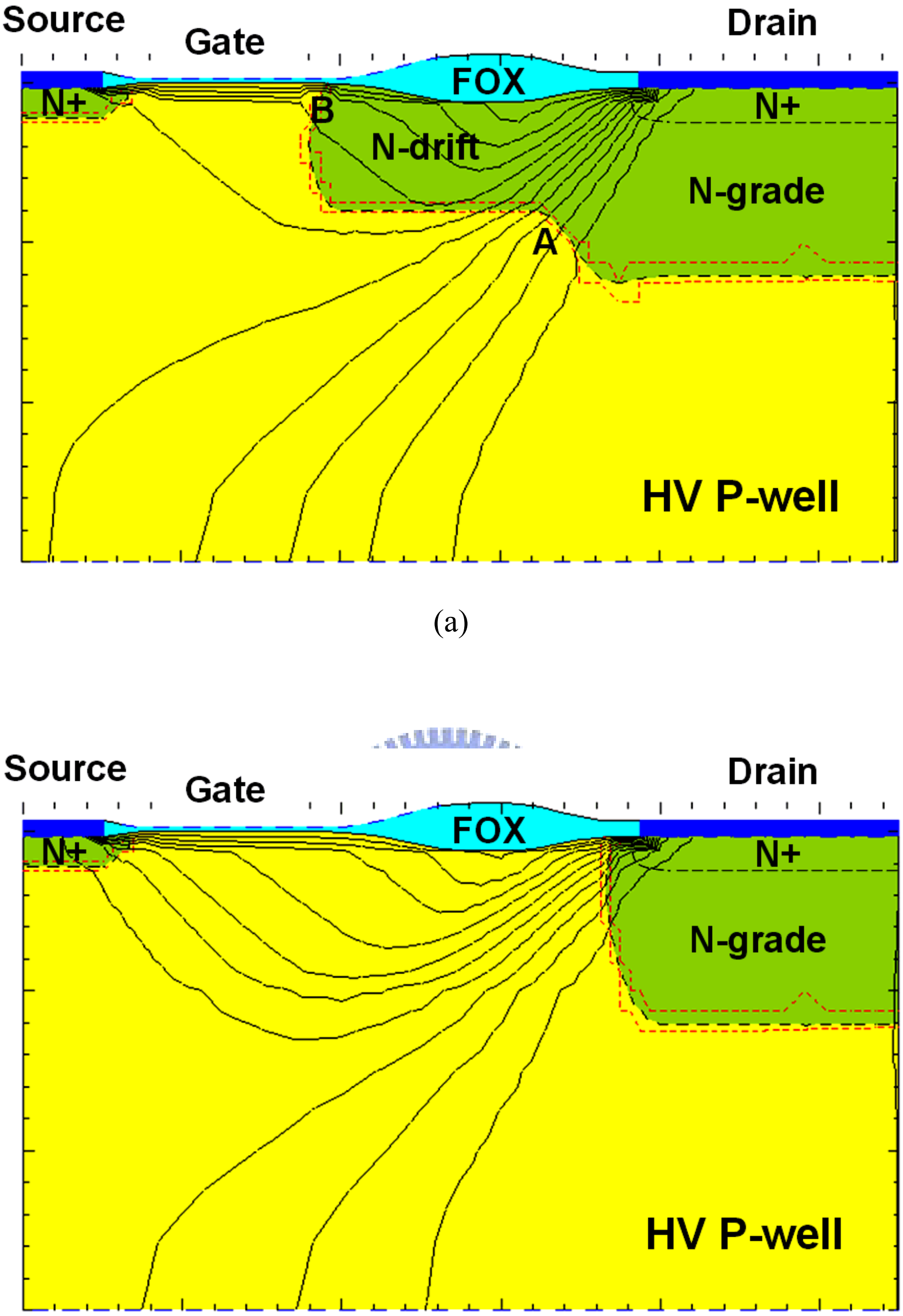
Fig. 6.4 The equivalent circuit of the HVNSCR embedded into HV GGNMOS.



(a)

(b)

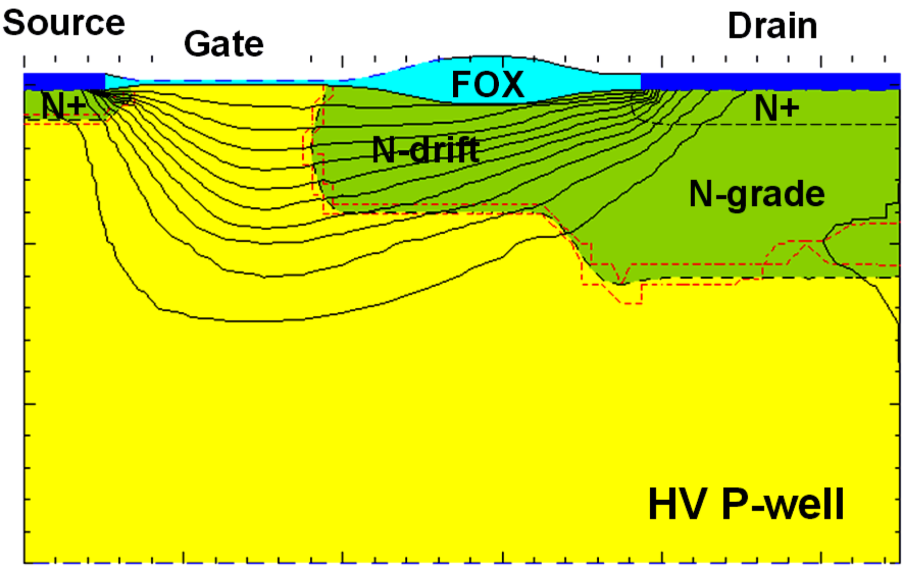
Fig. 6.5 The TLP-measured I-V curves of HV GGNMOS (a) with, and (b) without, N-drift implant in the drain region under different spacings D.



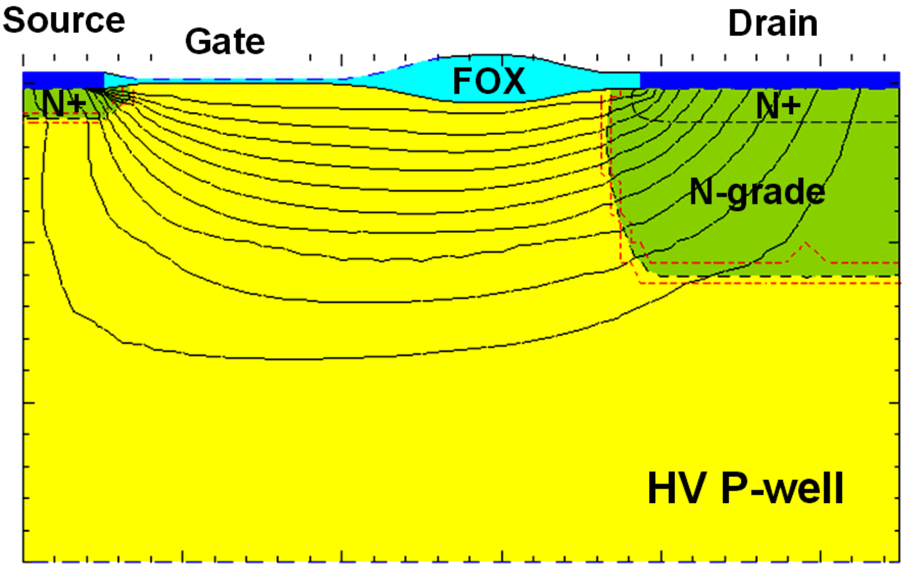
(a)

(b)

Fig. 6.6 The simulated current distributions of HV GGNMOS (a) with, and (b) without, N-drift implant in the drain region before the parasitic n-p-n BJT is triggered on.

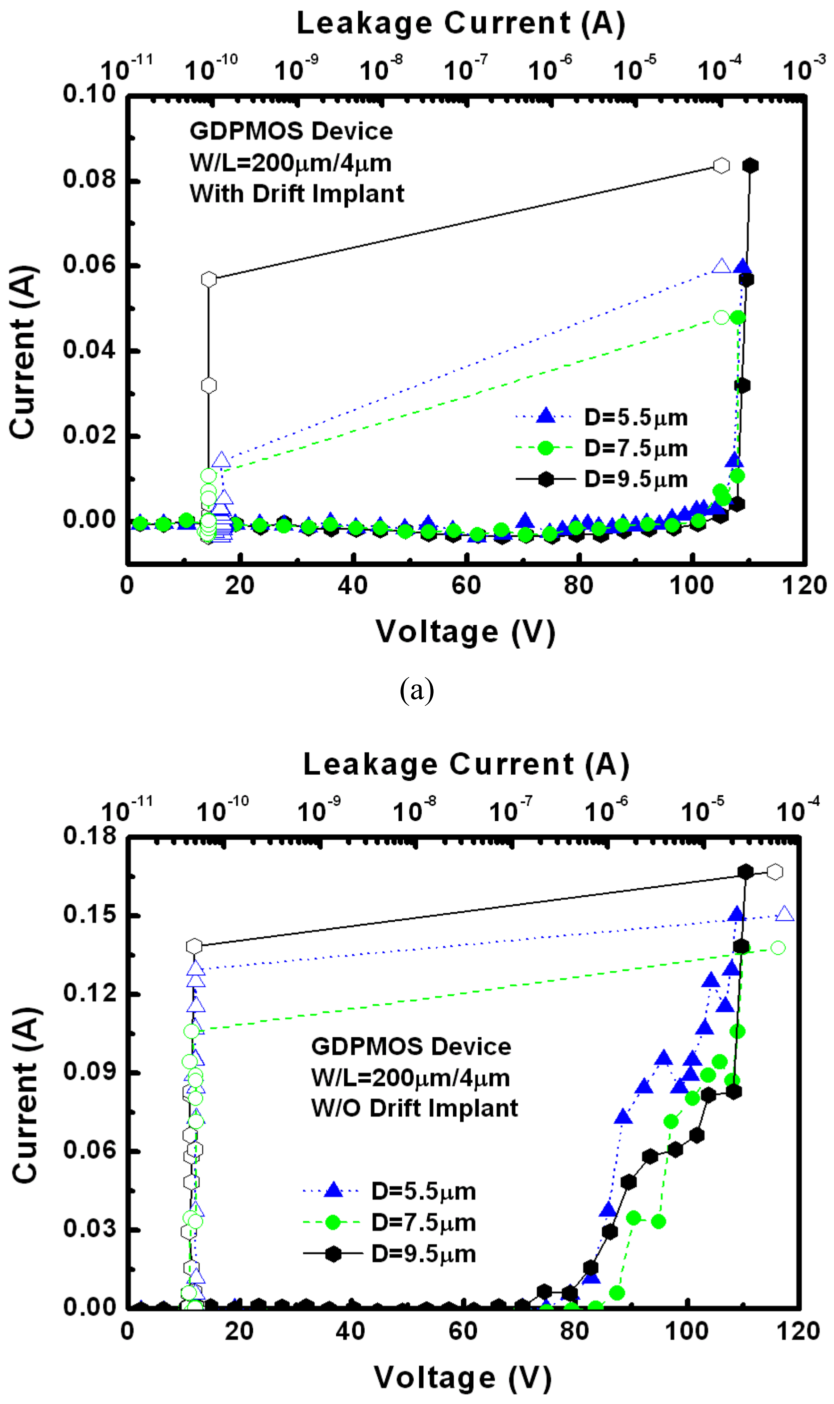


(a)



(b)

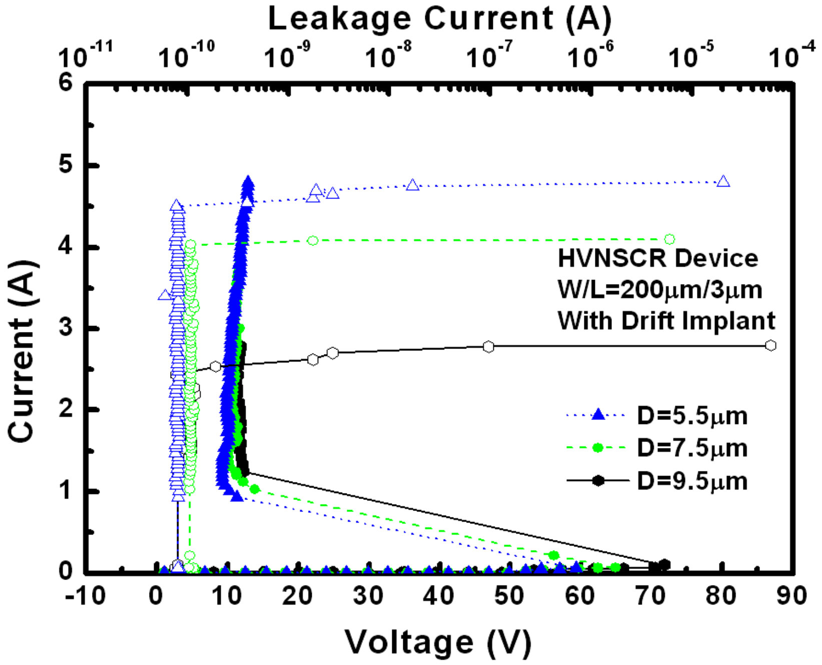
Fig. 6.7 The simulated current distributions of HV GGNMOS (a) with, and (b) without, N-drift implant in the drain region after the parasitic n-p-n BJT is triggered on.



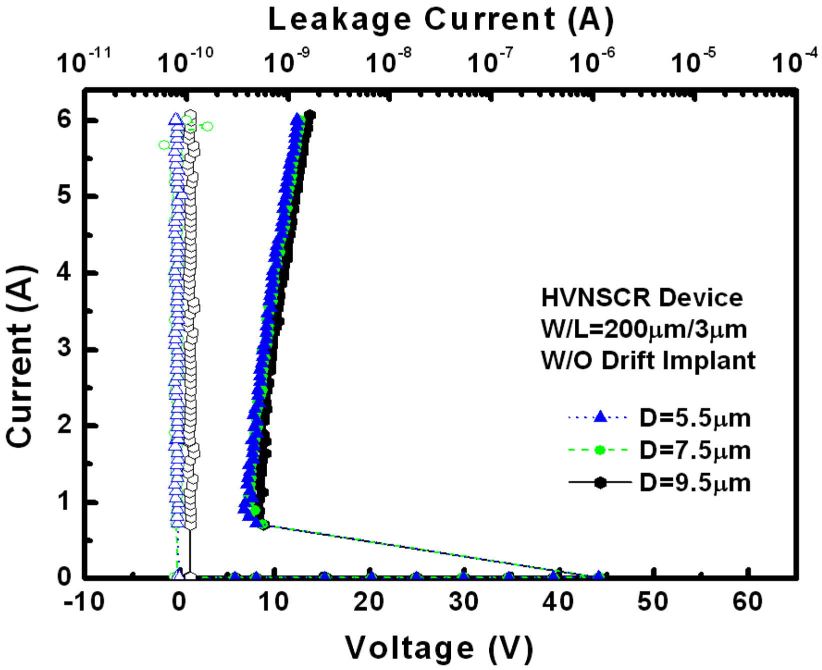
(a)

(b)

Fig. 6.8 The TLP-measured I-V curves of HV GDPMOS (a) with, and (b) without, P-drift implant in the drain region under different spacings D.



(a)



(b)

Fig. 6.9 The TLP-measured I-V curves of HVNSCR (a) with, and (b) without, N-drift implant in the drain region under different spacings D.

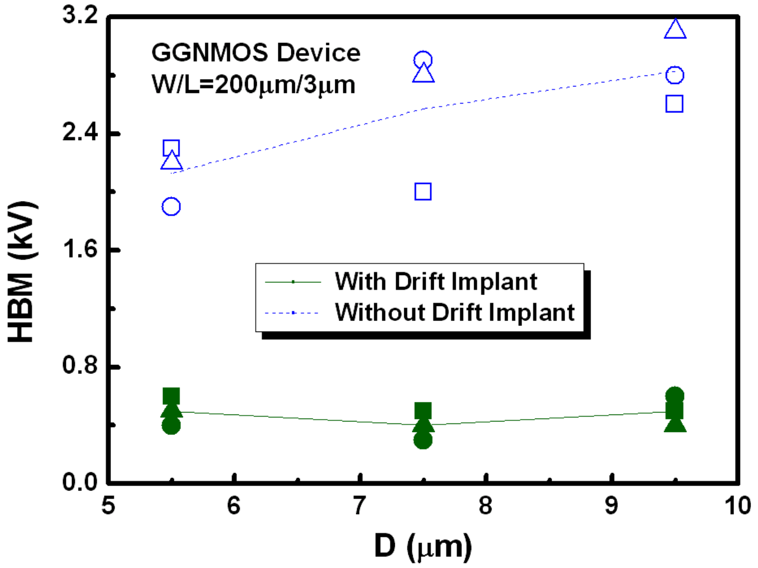


Fig. 6.10 The HBM ESD levels of HV GGNMOS with or without N-drift implant in the drain region under different spacings D.

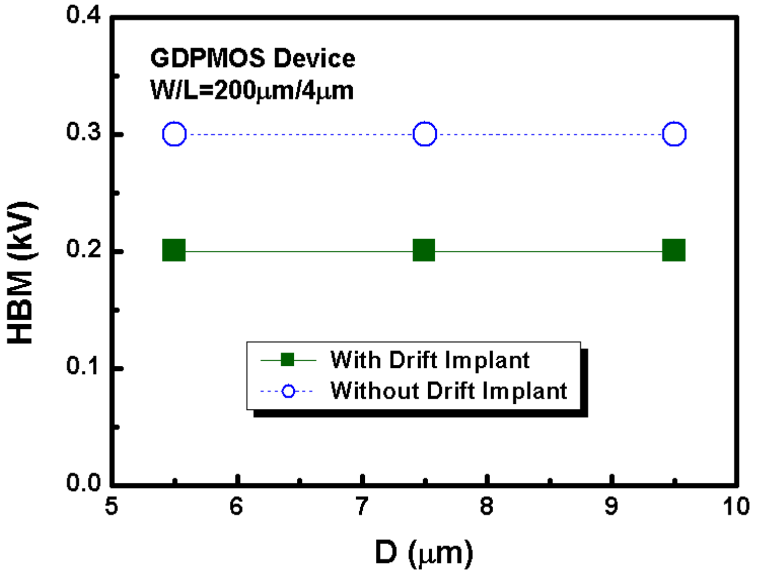


Fig. 6.11 The HBM ESD levels of HV GDPMOS with or without P-drift implant in the drain region under different spacings D.

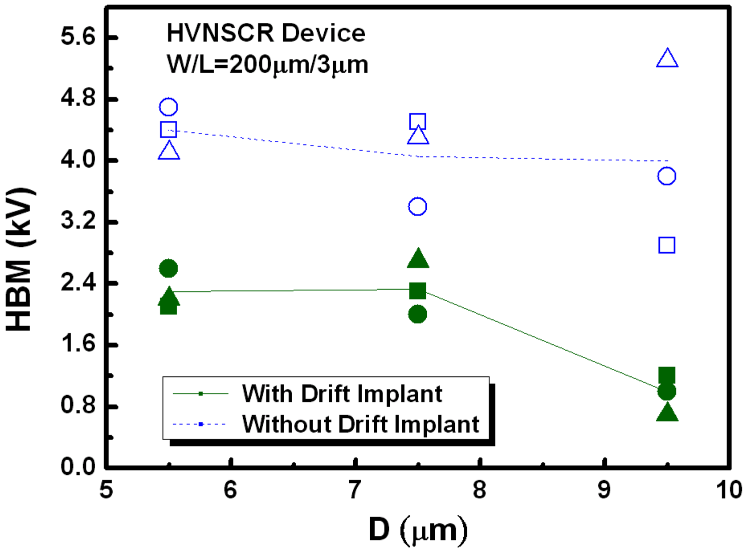


Fig. 6.12 The HBM ESD levels of HVNSCR with or without N-drift implant in the drain region under different spacings D.

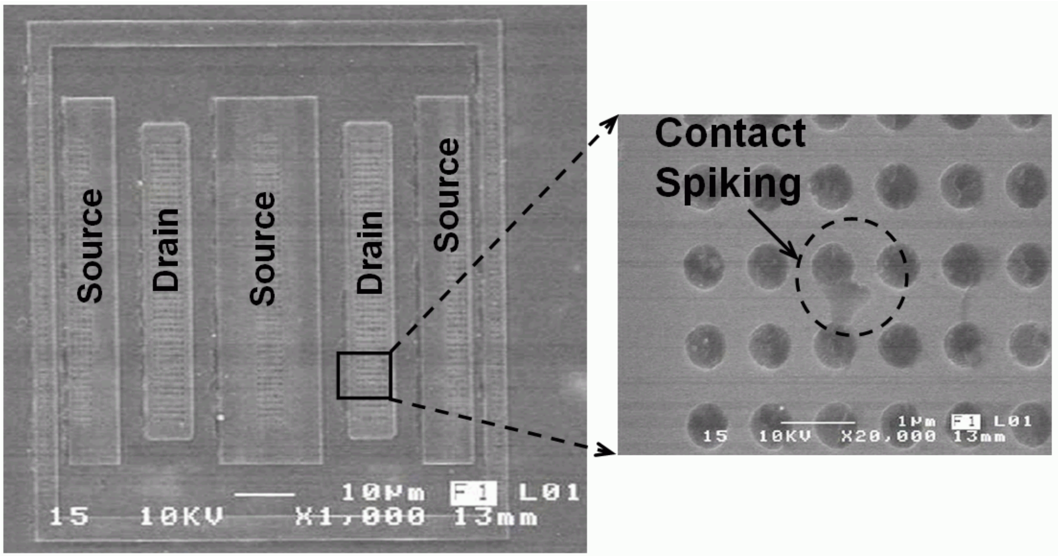


Fig. 6.13 The SEM failure picture of contact spiking in the drain region of HV GGNMOS under the spacing D of 7.5μm after 3-kV HBM ESD stress.

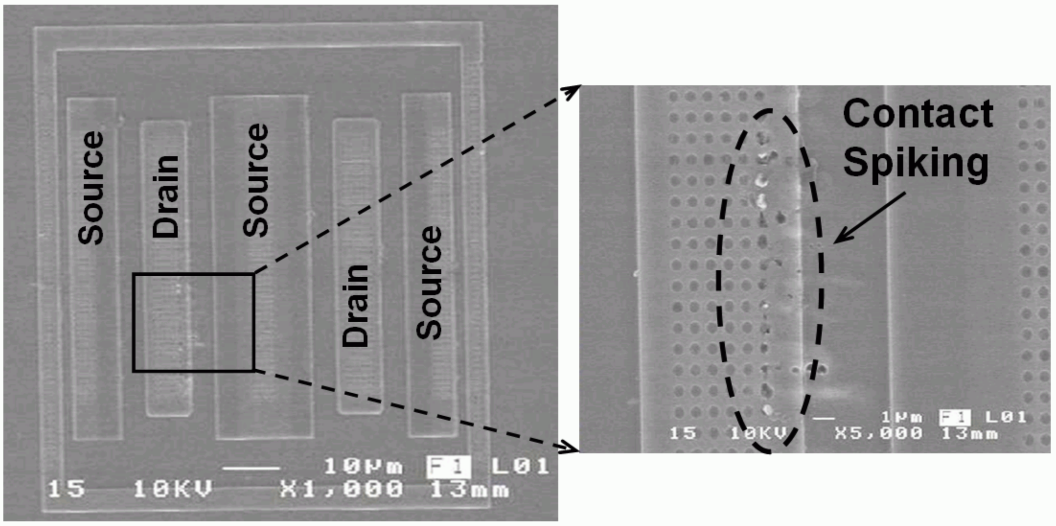


Fig. 6.14 The SEM failure picture of contact spiking in the drain region of HV GDPMOS under the spacing D of 7.5μm after 400-V HBM ESD stress.

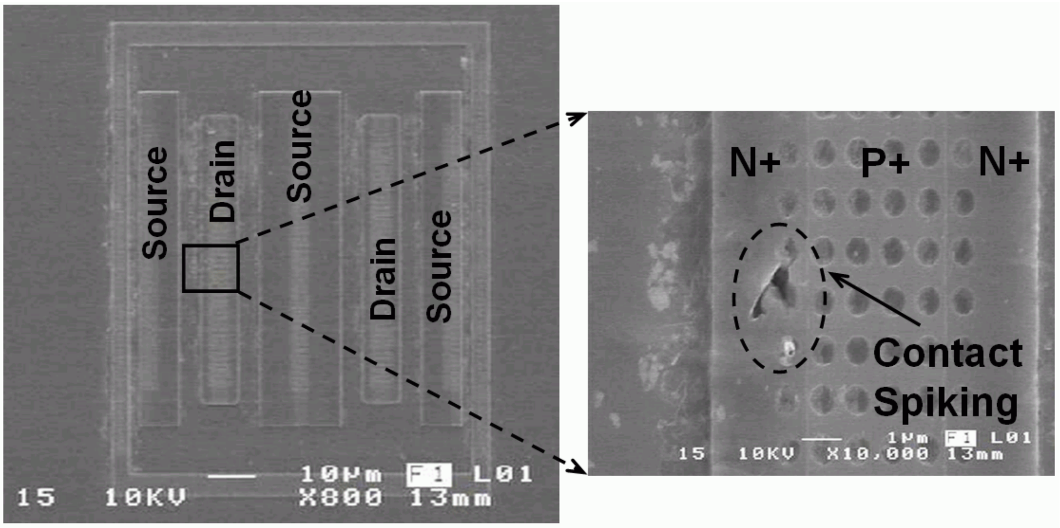


Fig. 6.15 The SEM failure picture of contact spiking in the drain region of HVNSCR under the spacing D of 7.5μm after 5-kV HBM ESD stress.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

7.1 Main Results of This Thesis

In this thesis, the novel ESD protection circuits have been developed for mixed-voltage I/O interfaces and high-voltage CMOS process with high ESD robustness. Each of the ESD protection circuits has been successfully verified in the testchips.

In chapter 2, a comprehensive overview on the ESD protection designs has been discussed for the mixed-voltage I/O circuits without suffering the gate-oxide reliability issue. To improve ESD level of the mixed-voltage I/O circuits, the ESD protection design without increasing the process complexity is strongly requested by the mixed-voltage I/O circuits in consumer IC products. Such ESD protection design in the mixed-voltage I/O circuits still meets the gate-oxide reliability constraints, and needs to prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current. To design the efficient ESD protection circuit for the mixed-voltage I/O circuits with low parasitic capacitance for high-speed I/O applications and low standby leakage current for low-power applications will continually be an important challenge to SOC implementation in the nanoscale CMOS technology.

In chapter 3, ESD protection design for the mixed-voltage I/O interfaces with new proposed LVTPNP devices has been successfully verified to achieve a good ESD protection in a 0.35-μm CMOS process. The proposed LVTPNP devices have the higher ESD level than that of the traditional PNP device. Moreover, the multi-finger layout style has been used to increase the effective device width among the LVTPNP device for improving ESD robustness in both 0.35-μm and 0.25-μm CMOS processes. Comparing among these LVTPNP devices, the type3 LVTPNP in the multi-finger layout style can sustain the highest ESD stress for application in the mixed-voltage I/O interfaces. ESD protection co-designed with the LVTPNP device and the power-rail ESD clamp circuit has been successfully implemented to protect the ADSL input stage in a 0.25-μm salicided CMOS process.

In chapter 4, to enhance chip-level ESD/EMC immunity, a new ESD protection scheme with an ESD_BUS and a high-voltage-tolerant ESD clamp circuit for system-on-chip with 1.2/2.5 V mixed-voltage I/O interfaces has been successfully designed and verified in a 0.13 μm CMOS process. The ESD stresses on the mixed-voltage I/O pad and the pin-to-pin ESD stresses can be effectively discharged by the proposed ESD protection scheme. With the substrate-triggered current generated from the ESD detection circuit, the turn-on speed and ESD robustness of the high-voltage-tolerant ESD clamp circuit can be significantly increased as compared with a stand-alone STNMOS. For STNMOS with a device dimension (W/L) of 480 μm/0.2 μm, the HBM (MM) ESD level of the 1.2/2.5 V mixed-voltage I/O interfaces can be improved from 5 kV (275 V) to 6.5 kV (400 V) by the ESD detection circuit in the proposed ESD protection scheme.

In chapter 5, the HVPMOS is not suitable for ESD protection in VFD driver IC for automotive electronics applications due to a poor ESD level. To greatly improve ESD robustness, a new ESD protection structure of HVPSCR embedded into the HVPMOS is proposed by only adding an additional N+ diffusion into the drain region of HVPMOS. With almost the same layout area, the It2 of the output cell has been improved over 6A, as well as, the HBM ESD level of such VFD driver IC with HVPSCR can sustain up to 8 kV. With device widths of 500μm, 600μm, and 800μm, the MM ESD levels of the HVPSCR are 1100V, 1300V, and 1900V, respectively. Moreover, the automotive driver IC can also pass the 200mA quasi-static latchup test.

In chapter 6, the drift implant in the drain region and layout spacing (D) from the drain diffusion to polygate have been split to verify the ESD robustness of HV MOSFETs in a given 40-V CMOS process. It has been found that HV MOSFETs without drift implant in drain region have higher TLP-measured It2 and higher ESD robustness than those with drift implant in the drain region. Moreover, without N-drift implant, the It2 and ESD level of HV GGNMOS can be obviously improved as the spacing D is increased. The ESD robustness of HV GGNMOS can be improved up to 2-kV HBM by removing the N-drift implant in the drain region. The HVNSCR without N-drift implant in drain region has highest ESD performance in a given 40-V CMOS process. For HVNSCR, the TLP-measured It2 can be improved over 6A and the ESD robustness can be improved to 4-kV by removing N-drift implant in the drain region. Moreover, the ESD level and It2 of HV NMOS can be increased as the layout spacing D from the drain diffusion to polygate is increased. The ESD level and

It2 of HVNSCR are increased as this spacing D is decreased.

7.2 Future Work

In mixed-voltage I/O interfaces, the effective ESD protection design has been proposed and verified in this thesis. But, the design of the high-voltage-tolerant ESD clamp circuit with low-voltage devices should be concerned about the standby leakage current in nanoscale CMOS technology, especially when the IC is operating at high-temperature environment. In high-voltage CMOS technology, the ESD robustness of the ESD protection devices has been greatly improved and verified in this thesis. However, the latchup or latchup-like failure from such ESD protection devices should be considered under normal circuit operating condition, especially while the devices are used in the power-rail ESD clamp circuit. To avoid the latchup or latchup-like issues in high-voltage CMOS ICs, the total holding voltage of the ESD protection devices can be designed with stacked-device structure to be higher than the supply voltage. But, the layout area of the stacked-device structure will increase as compared to that of the single device, especially for high ESD robustness requirement. The design of new device with the characteristics of both high holding voltage and high ESD robustness from the structure design or process modification will be a useful solution.

REFERENCES

[1] *ESD Association Standard Test Method ESD STM5.1-2001, for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level, 2001.*

[2] A. Wang, *On-Chip ESD Protection for Integrated Circuits*, Boston, Kluwer, 2001.

[3] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd Edition, John Wiley & Sons, Ltd., England, 2002.

[4] S. Voldman, *ESD Physics and Devices*, John Wiley & Sons, Ltd., England, 2004.

[5] C. Duvvury, R. Rountree, and O. Adams, "Internal chip ESD phenomena beyond the protection circuit," *IEEE Trans. on Electron Devices*, vol. 35, no. 12, pp. 2133–2139, Dec. 1988.

[6] C. Johnson, T. J. Maloney, and S. Qawami, "Two unusual HBM ESD failure mechanisms on a mature CMOS process," in *Proc. EOS/ESD Symp.*, 1993, pp. 225–231.

[7] V. Puvvada and C. Duvvury, "A simulation study of HBM failure in an internal clock buffer and the design issue for efficient power pin protection strategy," in *Proc. EOS/ESD Symp.*, 1998, pp. 104–110.

[8] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.

[9] T. Furukawa, D. Turner, S. Mittl, M. Maloney, R. Serafin, W. Clark, J. Bialas, L. Longenbach, and J. Howard, "Accelerated gate-oxide breakdown in mixed-voltage I/O circuits," in *Proc. IEEE Int. Reliability Physics Symp.*, 1997, pp. 169–173.

[10] E. Takeda and N. Suzuki, "An empirical model for device degradation due to hot-carrier injection," *IEEE Electron Device Lett.*, vol. 4, no. 4, pp. 111–113, Apr. 1983.

[11] S. Voldman, "ESD protection in a mixed voltage interface and multirail disconnected power grid environment in 0.5- and 0.25-μm channel length CMOS technologies," in *Proc. EOS/ESD Symp.*, 1994, pp. 125–134.

[12] S. Dabral and T. J. Maloney, *Basic ESD and I/O Design*, John Wiley & Sons, Inc., New York, 1998.

[13] M. Hargrove, S. Crowder, E. Nowak, R. Logan, L. Han, H. Ng, A. Ray, D. Sinitsky, P. Smeys, F. Guarin, J. Oberschmidt, E. Crabbe, D. Yee, and L. Su, "High-performance

sub-0.08-μm CMOS with dual gate oxide and 9.7-ps inverter delay,” in *IEDM Tech. Dig.*, 1998, pp. 627–630.

[14] S. Poon, C. Atwell, C. Hart, D. Kolar, C. Lage, and B. Yeargain, “A versatile 0.25-μm CMOS technology,” in *IEDM Tech. Dig.*, 1998, pp. 751–754.

[15] M. Takahash, T. Sakurai, K. Sawada, K. Nogami, M. Ichida, and K. Matsud, “3.3V-5V compatible I/O circuit without thick gate oxide,” in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 1992, pp. 23.3.1–23.3.4.

[16] M. J. M. Pelgrom and E. C. Dijkmans, “A 3/5 V compatible I/O buffer,” *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 823–825, Jul. 1995.

[17] J. Conner, D. Evans, G. Braceras, J. Sousa, W. Abadeer, S. Hall, and M. Robillard, “Dynamic dielectric protection for I/O circuits fabricated in a 2.5-V CMOS technology interfacing to a 3.3-V LVTTL bus,” in *Int. VLSI Circuits Symp. Tech. Dig.*, 1997, pp. 119–120.

[18] G. Singh and R. Salem, “High-voltage-tolerant I/O buffers with low-voltage CMOS process,” *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1512–1525, Nov. 1999.

[19] H. Sanchez, J. Siegel, C. Nicoletta, J. Nissen, and J. Alvarez, “A versatile 3.3/2.5/1.8-V CMOS I/O driver built in a 0.2-μm 3.5-nm Tox 1.8-V CMOS technology,” *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1501–1511, Nov. 1999.

[20] A. J. Annema, G. Geelen, and P. De Jong, “5.5-V I/O in a 2.5-V 0.25-μm CMOS technology,” *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 528–538, Mar. 2001.

[21] C.-H. Chuang and M.-D. Ker, “Design on mixed-voltage-tolerant I/O interface with novel tracking circuits in a 0.13-μm CMOS technology,” in *Proc. IEEE Int. Symp. Circuits and Systems*, 2004, pp. 577–580.

[22] W. Anderson and D. Krakauer, “ESD protection for mixed-voltage I/O using nMOS transistors stacked in a cascode configuration,” in *Proc. EOS/ESD Symp.*, 1998, pp. 54–71.

[23] J. Miller, M. Khazhinsky, and J. Weldon, “Engineering the cascoded nMOS output buffer for maximum Vt1,” in *Proc. EOS/ESD Symp.*, 2000, pp. 308–317.

[24] M.-D. Ker, H.-C. Hsu, and J.-J. Peng, “ESD Implantation for sub-quarter-micron CMOS technology to enhance ESD robustness,” *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2126–2134, Oct. 2003.

[25] V. A. Vashchenko, A. Concannon, M. Ter-Beek, and P. Hopper, “Physical limitation of the cascoded snapback nMOS ESD protection capability due to the non-uniform turn-off,” *IEEE Trans. Device Mater. Reliab.*, vol. 4, no. 2 pp. 281–291, June 2004.

[26] J.-H. Lee, J.-R. Shih, Y.-H. Wu, and T.-C. Ong, “The failure mechanism of high voltage tolerance IO buffer under ESD,” in *Proc. IEEE Int. Reliability Physics Symp.*, 2003, pp. 269–276.

[27] C.-Y. Huang, W.-F. Chen, S-Y Chuan, F.-C. Chiu, J.-C. Tseng, I-C. Lin, C.-J. Chao, L.-Y. Leu, and M.-D. Ker, “Design optimization of ESD protection and latchup prevention for a serial I/O IC,” *Microelectron. Reliab.*, vol. 44, no. 2, pp. 213–221, Feb. 2004.

[28] W. Morris, “Latchup in CMOS,” in *Proc. IEEE Int. Reliability Physics Symp.*, 2003, pp. 76–84.

[29] M.-D. Ker and W.-Y. Lo, “Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology,” *IEEE Trans. Semicond. Manufact.*, vol. 16, no. 2 pp. 319–334, May 2003.

[30] H. Ballan and M. Declercq, *High Voltage Devices and Circuits in Standard CMOS Technologies*, Kluwer Academic, 1998.

[31] M. P. J. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker, and W. Fichtner, “Analysis of lateral DMOS power devices under ESD stress conditions,” *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2128–2137, Nov. 2000.

[32] C. Duvvury, F. Carvajal, C. Jones, and D. Briggs, “Lateral DMOS design for ESD robustness,” in *IEDM Tech. Dig.*, 1997, pp. 375–378.

[33] C. Duvvury, D. Briggs, J. Rodrigues, F. Carvajal, A. Young, D. Redwine, and M. Smayling, “Efficient npn operation in high voltage NMOSFET for ESD robustness,” in *IEDM Tech. Dig.*, 1995, pp. 345–348.

[34] C. Duvvury, J. Rodriguez, C. Jones, and M. Smayling, “Device integration for ESD robustness of high voltage power MOSFETs,” in *IEDM Tech. Dig.*, 1994, pp. 407–410.

[35] J.-H. Lee, J.-R. Shih, C.-S, Tang, K.-C. Liu, Y.-H. Wu, R.-Y. Shiue, T.-C. Ong, Y.-K. Peng, and J.-T. Yue, “Novel ESD protection structure with embedded SCR LDMOS for smart power technology,” in *Proc. IEEE Int. Reliability Physics Symp.*, 2002, pp. 156–161.

[36] V. De Heyn, G. Groeseneken, B. Keppens, M. Natarajan, L. Vacaresse, and G. Gallopyn, “Design and analysis of new protection structures for smart power technology with controlled trigger and holding voltage,” in *Proc. IEEE Int. Reliability Physics Symp.*, 2001, pp. 253–258.

[37] G. Bertrand, C. Delage, M. Bafleur, N. Nolhier, J. Dorkel, Q. Nguyen, N. Mauran, D.

Tremouilles, and P. Perdu, “Analysis and compact modeling of a vertical grounded-base n-p-n bipolar transistor used as ESD protection in a smart power technology,” *IEEE J. Solid-State Circuits*, vol. 36, no. 9, pp. 1373–1381, Sep. 2001.

[38] M.-D. Ker and K.-H. Lin, “The impact of low-holding-voltage issue in high-voltage CMOS technology and the design of latchup-free power-rail ESD clamp circuit for LCD driver ICs,” *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1751–1759, Aug. 2005.

[39] J.-H. Lee, J.-R. Shih, Y.-H. Wu, B.-K. Liew, and H.-L. Hwang, “An analytical model of positive HBM ESD current distribution and the modified multi-finger protection structure”, in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 1999, pp. 162–167.

[40] N. Boswell, “Vacuum fluorescent display developments,” *IEE Colloquium on Graphic Display Devices*, 1989, pp. 3/1–3/2.

[41] A. Slack, “Prospective developments in automotive instrumentation,” in *Proc. IEEE Int. Electronics Manufacturing Technology Symp.*, 1998, pp. 10–15.

[42] M.-D. Ker and T.-Y. Chen, “Substrate-triggered technique for on-chip ESD protection design in a 0.18-μm salicided CMOS process,” *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1050–1057, Apr. 2003.

[43] M.-D. Ker, K.-H. Lin, and C.-H. Chuang, “On-chip ESD protection design with substrate-triggered technique for mixed-voltage I/O circuits in sub-quarter-micron CMOS process,” *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1628–1635, Oct. 2004.

[44] M.-D. Ker and H.-C. Hsu, “ESD protection design for mixed-voltage I/O buffer with substrate-triggered circuit,” *IEEE Trans. Circuits and Systems I*, vol. 52, no. 1, pp. 44–53, Jan. 2005.

[45] J. Smith, “A substrate triggered lateral bipolar circuit for high-voltage tolerant ESD protection applications,” in *Proc. EOS/ESD Symp.*, 1998, pp. 63–71.

[46] M.-D. Ker and C.-H. Chuang, “ESD protection design for mixed-voltage CMOS I/O buffers,” *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1046–1055, Aug. 2002.

[47] S. Voldman and G. Gerosa, “Mixed-voltage interface ESD protection circuits for advanced microprocessors in shallow trench and LOCOS isolation CMOS technologies,” in *IEDM Tech. Dig.*, 1994, pp. 277–280.

[48] S. Voldman, G. Gerosa, V. Gross, S. Dickson, N. Furkay, and J. Slinkman, “Analysis of snubber-clamped diode-string mixed voltage interface ESD protection network for

advanced microprocessors," in *Proc. EOS/ESD Symp.*, 1995, pp. 43–61.

[49] M. Tong, R. Gauthier, and V. Gross, "Study of gated PNP as an ESD protection device for mixed-voltage and hot-pluggable circuit applications," in *Proc. EOS/ESD Symp.*, 1996, pp. 280–284.

[50] T. Maloney and S. Dabral, "Novel clamp circuits for IC power supply protection," in *Proc. EOS/ESD Symp.*, 1995, pp. 1–12.

[51] M.-D. Ker and K.-H. Lin, "Design on ESD protection schemes for IC with power-down-mode operation," *IEEE J. of Solid-State Circuits*, vol. 39, no. 8, pp. 1378–1382, Aug. 2004.

[52] E. R. Worley, R. Gupta, B. Jones, R. Kjar, C. Nguyen, and M. Tennyson, "Sub-micron chip ESD protection schemes which avoid avalanching junctions," in *Proc. EOS/ESD Symp.*, 1995, pp. 13–20.

[53] M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD protection design on analog pin with very low input capacitance for high-frequency or current-mode applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1194–1199, Aug. 2000.

[54] C.-H. Chen, Y.-K. Fang, C.-C. Tsai, S. Tu, K.-L. Chen, and M.-C. Chang, "High voltage tolerant ESD design for analog applications in deep submicron CMOS technologies," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2002, pp. 89–92.

[55] H.-H. Chang, M.-D. Ker, K.-T. Lee, and W.-H. Huang, "Output ESD protection using dynamic-floating-gate arrangement," U.S. Patent # 6,034,552, Mar. 3, 2000.

[56] M.-D. Ker and C.-H. Chuang, "ESD implantations in 0.18-μm salicided CMOS technology for on-chip ESD protection with layout consideration," in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2001, pp. 85–90.

[57] M.-D. Ker and W.-J. Chang, "ESD protection design of low-voltage-triggered p-n-p devices and their failure modes in mixed-voltage I/O interfaces with signal levels higher than VDD and lower than VSS," *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 3, pp. 602–612, Sep. 2005.

[58] M.-D. Ker, W.-J. Chang, and W.-Y. Lo, "Low-voltage-triggered PNP devices for ESD protection design in mixed-voltage I/O interface with over-VDD and under-VSS signal levels" in *Proc. IEEE Int. Symp. Quality Electronic Design (ISQED)*, 2004, pp. 433–438.

[59] W.-J. Chang and M.-D. Ker, "Layout optimization on low-voltage-triggered PNP devices for ESD protection in mixed-voltage I/O interfaces," in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2004, pp. 213–216.

[60] D. Neamen, *Semiconductor Physics & Devices*, 2nd ed., New York: McGraw-Hill, 1997.

[61] G. Notermans, A. Heringa, M. Van Dort, S. Jansen, and F. Kuper, "The effect of silicide on ESD performance," in *Proc. IEEE Int. Reliability Physics Symp.*, 1999, pp. 154–158.

[62] M.-D. Ker and C.-H. Chuang, "ESD protection design for high-speed I/O interfaces of stub series terminated logic (SSTL) in a 0.25-µm salicided CMOS process," in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2004, pp. 217–220.

[63] K. Esmark, W. Stadler, M. Wendel, H. Goher, X. Guggenmos, and W. Fichtner, "Advanced 2D/3D ESD device simulation-a powerful tool already used in a pre-Si phase" in *Proc. EOS/ESD Symp.*, 2000, pp. 420–429.

[64] A. Salman, R. Gauthier, W. Stadler, K. Esmark, M. Muhammad, C. Putnam, and D. Ioannou, "Characterization and investigation of the interaction between hot electron and electrostatic discharge stresses using NMOS devices in 0.13 µm CMOS technology" in *Proc. IEEE Int. Reliability Physics Symp.*, 2001, pp. 219–225.

[65] K. Nikawa, "Optical beam induced resistance change (OBIRCH): overview and recent results," in *Proc. 16th Annual Meeting of IEEE Lasers and Electro-Optics Society (IEOS), 2003*, vol. 2, pp. 742–743.

[66] L. Soon, D. Ling, M. Kuan, K.-W. Yee, D. Cheong, and G. Zhang, "Application of IR-OBIRCH to the failure analysis of CMOS integrated circuits," in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2003, pp. 86–91.

[67] M.-D. Ker, W.-J. Chang, C.-T. Wang, and W.-Y. Chen, "ESD protection for mixed-voltage I/O in low-voltage thin-oxide CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Tech. Dig. Papers*, 2006, pp. 546–547.

[68] M.-D. Ker and K.-H. Lin, "Overview on electrostatic discharge protection designs for mixed-voltage I/O interfaces: design concept and circuit implementations," *IEEE Trans. Circuits and Systems I*, vol. 53, no. 2, pp. 235–246, Feb. 2006.

[69] M.-D. Ker, W.-Y. Chen, and K.-C. Hsu, "Design on power-rail ESD clamp circuit for 3.3-V I/O interface by using only 1-V/2.5-V low-voltage devices in a 130-nm CMOS process," *IEEE Trans. Circuits and Systems I*, vol. 53, no. 10, pp. 2187–2193, Feb. 2006.

[70] M.-D. Ker and W.-J. Chang, "Overview on ESD protection design for mixed-voltage I/O interfaces with high-voltage-tolerant power-rail ESD clamp circuits in low-voltage

thin-oxide CMOS technology," *Microelectron. Reliab.*, vol. 47, no. 1, pp. 27-35, Jan. 2007.

[71] T. Li, C.-H. Tsai, E. Rosenbaum, and S.-M. Kang, "Substrate resistance modeling and circuit-level simulation of parasitic device coupling effects for CMOS I/O circuits under ESD stress," in *Proc. EOS/ESD Symp.*, 1998, pp. 281–289.

[72] X. Y. Zhang, K. Banerjee, A. Amerasekera, V. Gupta, Z. Yu, and R. W. Dutton, "Process and layout dependent substrate resistance modeling for deep sub-micron ESD protection devices," in *Proc. IEEE Int. Reliability Physics Symp.*, 2000, pp. 295–303.

[73] M.-D. Ker, W.-J. Chang, M. Yang, C.-C. Chen, M.-C. Chan, W.-T. Shieh, and K.-L. Yen, "ESD protection structure with embedded high-voltage p-type SCR for automotive vacuum-fluorescent-display (VFD) applications," in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2005, pp. 67–70.

[74] M.-D. Ker and W.-J. Chang, "On-chip ESD protection design for automotive vacuum-fluorescent-display (VFD) driver IC to sustain high ESD stress," *IEEE Trans. Device Mater. Reliab.*, in press, 2007.

[75] B. Keppens, M. P. J. Mergens, C. S. Trinh, C. C. Russ, B. V. Camp, and K. G. Verhaege, "ESD protection solutions for high voltage technologies," in *Proc. EOS/ESD Symp.*, 2004, pp. 289–298.

[76] M.-D. Ker, C.-Y. Wu, and H.-H. Chang, "Complementary-LVTSCR ESD protection circuit for submicron CMOS VLSI/ULSI," *IEEE Trans. Electron Devices*, vol. 43, no. 4, pp. 588–598, Apr. 1996.

[77] M.-D. Ker and C.-Y. Wu, "Modeling the positive feedback regenerative process of CMOS latchup by a positive transient pole method-part I: theoretical derivation," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1141–1148, June 1995.

[78] M.-D. Ker and C.-Y. Wu, "Modeling the positive feedback regenerative process of CMOS latchup by a positive transient pole method-part II: quantitative evaluation," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1149–1155, June 1995.

[79] M. J. Hargrove, S. Voldman, R. Gauthier, J. Brown, K. Duncan, and W. Craig, "Latchup in CMOS technology," in *Proc. IEEE Int. Reliability Physics Symp.*, 1998. pp. 269–278.

[80] M.-D. Ker, "Lateral SCR devices with low-voltage high-current triggering characteristics for output ESD protection in submicron CMOS technology" *IEEE Trans. Electron Devices*, vol. 45, no. 4, pp. 849–860, Apr. 1998.

[81] M.-D. Ker and H.-H. Chang, “How to safely apply the LVTSCR for CMOS whole-chip ESD protection without being accidentally triggered on,” *J. Electrostatics*, vol. 47, no. 2 pp. 215–248, Oct. 1999.

[82] S. Pendharkar, R. Teggatz, J. Devore, J. Carpenter, T. Efland, and C.-Y. Tsai, “SCR-LDMOS: a novel LDMOS device with ESD robustness,” in *Proc. Power Semiconductor Devices and ICs Symp*., 2000, pp. 341–344.

[83] *IC Latch-up Test*, EIA/JEDEC Stand. No. 78, Electron. Industries Assoc., 1997.

[84] W.-J. Chang, M.-D. Ker, T.-H. Lai, T.-H. Tang, and K.-C. Su, “ESD robustness of 40-V CMOS devices with/without drift implant,” in *Final Report of IEEE Integrated Reliability Workshop*, 2006, pp. 167–170.

[85] W.-J. Chang and M.-D. Ker, “The impact of drift implant and layout parameters on ESD robustness for on-chip ESD protection devices in 40-V CMOS technology,” *IEEE Trans. Device Mater. Reliab.*, in press, 2007.

[86] T. J. Maloney and N. Khurana, “Transmission line pulsing techniques for circuit modeling of ESD phenomena,” in *Proc. EOS/ESD Symp*., 1985, pp. 49–54.

[87] M.-D. Ker and K.-H. Lin, “Double snapback characteristics in high voltage nMOFETs and the impact to on-chip ESD protection design,” *IEEE Electron Device Lett*., vol. 25, no. 9, pp. 640–642, Sep. 2004.

[88] V. Parthasarathy, V. Khemka, R. Zhu, J. Whitfield, A. Bose, and R. Ida, “A double RESURF LDMOS with drain profile engineering for improved ESD robustness,” *IEEE Electron Device Lett*., vol. 23, no. 4, pp. 212–214, Apr. 2002.

[89] S.-C. Huang, J.-H. Lee, S.-C. Lee, K.-M. Chen, M.-H. Song, C.-Y. Chiang, and M.-C. Chang, “Circuit and silicide impact on the correlation between TLP and ESD (HBM and MM),” in *Final Report of IEEE Integrated Reliability Workshop*, 2004, pp. 169–172.

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PUBLICATION LIST

(A) Referred Journal Papers:

[1] M.-D. Ker and **Wei-Jen Chang**, "ESD protection design of low-voltage-triggered p-n-p devices and their failure modes in mixed-voltage I/O interfaces with signal levels higher than VDD and lower than VSS," *IEEE Trans. Device Material Reliability*, vol. 5, no. 3, pp. 602–612, Sep. 2005.

[2] M.-D. Ker and **Wei-Jen Chang**, "Overview on ESD protection design for mixed-voltage I/O interfaces with high-voltage-tolerant power-rail ESD clamp circuits in low-voltage thin-oxide CMOS technology," *Microelectronics Reliability*, vol. 47, no. 1, pp. 27–35, Jan. 2007.

[3] **Wei-Jen Chang** and M.-D. Ker, "The impact of drift implant and layout parameters on ESD robustness for on-chip ESD protection devices in 40-V CMOS technology," *IEEE Trans. Device Material Reliability*, vol. 7, no. 2, pp. 324–332, June 2007.

[4] M.-D. Ker and **Wei-Jen Chang**, "On-chip ESD protection design for automotive vacuum-fluorescent-display (VFD) driver IC to sustain high ESD stress," *IEEE Trans. Device Material Reliability*, *in press*, 2007.

[5] M.-D. Ker and **Wei-Jen Chang**, "Chip-level ESD/EMC protection design for system-on-chip with mixed-voltage I/O interfaces," submitted to *IEEE Trans. Electromagnetic Compatibility.*

(B) International Conference Papers:

[1] M.-D. Ker, **Wei-Jen Chang**, and W.-Y. Lo, "Low-voltage-triggered PNP for ESD protection in mixed-voltage I/O interface" in *Proc. Int. Conf. Solid State Devices and Materials (SSDM)*, 2003, pp. 404–405.

[2] M.-D. Ker, **Wei-Jen Chang**, and W.-Y. Lo, "Low-voltage-triggered PNP devices for ESD protection design in the mixed-voltage I/O interface with over-VDD and under-VSS signal levels," in *Proc. IEEE Int. Symp. Quality Electronic Design (ISQED)*, 2004, pp. 433–438.

[3] **Wei-Jen Chang** and M.-D. Ker, “Layout optimization on low-voltage-triggered PNP devices for ESD protection in mixed-voltage I/O interfaces,” in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2004, pp. 213–216.

[4] M.-D. Ker, **Wei-Jen Chang**, M. Yang, C.-C. Chen, M.-C. Chan, W.-T. Shieh, and K.-L. Yen, “ESD protection structure with embedded high-voltage p-type SCR for automotive vacuum-fluorescent-display (VFD) applications” in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2005, pp. 67–70.

[5] M.-D. Ker, **Wei-Jen Chang**, C.-T. Wang, and W.-Y. Chen, “ESD protection for mixed-voltage I/O in low-voltage thin-oxide CMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Tech. Dig. Papers*, 2006, pp. 546–547.

[6] **Wei-Jen Chang** and M.-D. Ker, “ESD protection design for CMOS integrated circuits with mixed-voltage I/O interfaces” in *Proc. 2nd Conference on Ph.D. Research in MicroElectronics and Electronics (PRIME)*, 2006, pp. 305–308.

[7] **Wei-Jen Chang**, M.-D. Ker, T.-H. Lai, T.-H. Tang, and K.-C. Su, “ESD robustness of 40-V CMOS devices with/without drift implant,” in *Final Report of IEEE Integrated Reliability Workshop*, 2006, pp. 167–170.

[8] **Wei-Jen Chang**, M.-D. Ker, T.-X. Lai, T.-H. Tang, and K.-C. Su, “The impact of N-drift implant on ESD robustness of high-voltage NMOS with embedded SCR structure in 40-V CMOS process,” in *Proc. IEEE Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2007, pp. 249–252.

(C) Local Journal Papers:

[1] 張瑋仁、柯明道,“利用低壓之金氧半電晶體元件來設計可承受高工作電壓之晶電放電箝制電路,” 電子月刊, 第 142 期, pp. 209-220, May 2007.

(D) Local Conference Papers:

[1] M.-D. Ker, **Wei-Jen Chang**, and W.-Y. Lo, “ESD protection design for mixed-voltage I/O interfaces with input voltage levels higher than VDD and lower than VSS,” in *Proc. VLSI Design/CAD Symp.*, 2003.

[2] M.-D. Ker, **Wei-Jen Chang**, and W.-Y. Lo, “ESD protection design for mixed-voltage I/O interfaces with input voltage levels higher than VDD and lower than VSS," in *Proc. Taiwan Electrostatic Discharge Conf.*, 2003.

[3] **Wei-Jen Chang** and M.-D. Ker, “A new ESD protection structure with embedded high-voltage p-type SCR (HVPSCR) for vacuum-fluorescent-display (VFD) dirver IC of automotive electronics applications” in *Proc. Taiwan Electrostatic Discharge Conf.*, 2005.

[4] **Wei-Jen Chang** and M.-D. Ker, “High-voltage-tolerant ESD clamp circuits in low-voltage CMOS technology,” in *Proc. Taiwan Electrostatic Discharge Conf.*, 2006.

[5] **張瑋仁**、柯明道、賴泰翔、唐天浩、蘇冠丞, “在高壓 40 伏特之金氧半元件之中探討在汲極下端之飄移離子植入對元件之靜電放電防護能力之影響,” 2006 年台灣靜電放電研討會.

(E) Patents:

[1] **Wei-Jen Chang**, T.-X. Lai, M.-D. Ker, T.-H. Tang, and K.-C. Su, “The design of latchup-free power-rail ESD clamp circuit in high-voltage CMOS technology,” U.S. and R.O.C. Patent pending.

(F) Awards:

[1] 第四屆聯發科技獎學金得主（4th MediaTek Fellowship Award）, 2005–2007.

[2] 第二屆台積電傑出學生研究獎—碩博組佳作（2nd TSMC Outstanding Student Award, Commendation）, 2007.