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TABLE CAPTIONS

Table 3.1 Summary of our results, C_t/C_c is base on the assumption of the thickness of the tunnel oxide equal to 80\AA and control gate area equal to the floating gate area. Ten years operation voltage is obtained from TDDB plot. $V_{\text{interpoly}}$ means the voltage which across the interpoly dielectric. We also assume NOR type flash W/E voltage is 10V and NAND type flash W/E voltage is 20V.

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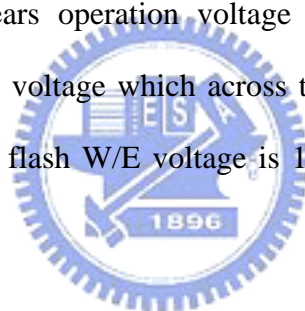


FIGURE CAPTIONS

Chapter 1

Fig.1.1 Basic flash memory cell structure

Fig.1.2 The relation between dielectric constant with band gap and breakdown electric field.

Fig.1.3 A diagram of the typical PECVD system

Fig.1.4 A diagram of the RTA system

Fig.1.5 Three tunneling mechanisms (a) Direct tunneling (b) F-N tunneling (c) F-P tunneling

Chapter 2

Fig.2.1 TiN/NiTiO/poly-Si capacitor fabrication process flow which include (a) after pure NH_3 surface nitridation (b) after Ni/Ti stack was deposited by PVD (c) Rapid thermal anneal (d) after define gate, passivation oxide was deposited by PECVD (e) after contact hole etched and metal pad defined and etched, the final structure was finished.

Fig.2.2 J-E curve with various post-oxidation anneal temperature, under positive gate bias.

Fig.2.3 J-E curve with various post-oxidation anneal temperature, under negative gate bias.

Fig.2.4 Weibull distribution of leakage current density at $V_g = +1\text{V}$ with various post-oxidation anneal.

Fig.2.5 Weibull distribution of leakage current density at $V_g = -1\text{V}$ with various post-oxidation anneal.

Fig.2.6 Weibull distribution of breakdown electric field with various pre-oxidation

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Fig.2.7 Weibull distribution of breakdown electric field with various post-oxidation anneal, under negative gate bias.

Fig.2.8 Weibull distribution of breakdown charge with various post-oxidation anneal, under positive gate bias.

Fig.2.9 TDDB characteristic with various post-oxidation anneal, under positive gate bias.

Fig.2.10 AFM surface roughness of the as-oxidation sample.

Fig.2.11 AFM surface roughness of the NiTiO with 800°C anneal.

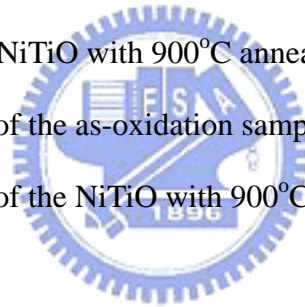
Fig.2.12 AFM surface roughness of the NiTiO with 900°C anneal.

Fig.2.13 TEM image of the as-oxidation sample.

Fig.2.14 TEM image of the NiTiO with 900°C anneal.

Fig.2.15 AES depth profile of the as-oxidation sample.

Fig.2.16 AES depth profile of the NiTiO with 900°C anneal.



Chapter 3

Fig.3.1 TiN/NiTiO/poly-Si capacitor fabrication process flow which include (a) pure NH₃ surface nitridation (b) Ni/Ti deposited by PVD (c) NH₃ plasma pre-oxidation treatment (d) rapid thermal anneal (e) passivation oxide deposited by PECVD (f) after contact hole etched and metal pad defined and etched, the final structure was finished.

Fig.3.2 Positive gate bias J-E characteristic of NiTiO under various anneal temperature with plasma treatment (PLOX) and without plasma treatment (OX).

Fig.3.3 Negative gate bias J-E characteristic of NiTiO under various anneal temperature with plasma treatment (PLOX) and without plasma treatment

(OX).

Fig.3.4 Weibull distribution of leakage current density at $V_g = +1V$, these samples aren't annealing in RTA.

Fig.3.5 Weibull distribution of leakage current density at $V_g = -1V$, these samples aren't annealing in RTA.

Fig.3.6 Delta leakage current under various anneal temperature at $V_g = +1V$. Delta leakage current = $I_{\text{anneal}} - I_{\text{as-oxidation}}$.

Fig.3.7 Delta leakage current under various anneal temperature at $V_g = -1V$. Delta leakage current = $I_{\text{anneal}} - I_{\text{as-oxidation}}$.

Fig.3.8 Weibull distribution of leakage current density at $V_g = +1V$, these samples under 900°C anneal in RTA.

Fig.3.9 Weibull distribution of leakage current density at $V_g = -1V$, these samples under 900°C anneal in RTA.

Fig.3.10 E_{BD} under various anneal temperature for positive gate bias.

Fig.3.11 E_{BD} under various anneal temperature for negative gate bias.

Fig.3.12 Charge to breakdown characteristic under positive gate bias.

Fig.3.13 TDDB characteristic under positive gate bias.

Fig.3.14 Surface roughness of Ni/Ti stack structure without NH_3 plasma treatment.

Fig.3.15 Surface roughness of Ni/Ti stack structure with 20Watts 5 minutes NH_3 plasma treatment.

Fig.3.16 Surface roughness of Ni/Ti stack structure with 20Watts 10 minutes NH_3 plasma treatment.

Fig.3.17 Surface roughness of Ni/Ti stack structure with 40W 5 minutes NH_3 plasma treatment.

Fig.3.18 Surface roughness of NiTiO with 20Watts 5 minutes NH_3 plasma pre-oxidation treatment.

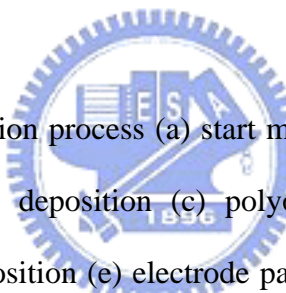
- Fig.3.19** Surface roughness of the NiTiO with 20Watts 10 minutes NH₃ plasma pre-oxidation treatment.
- Fig.3.20** Surface roughness of the NiTiO with 40Watts 5 minutes NH₃ plasma pre-oxidation treatment.
- Fig.3.21** Summary of the surface roughness from Fig.3.14 to Fig.3.17
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- Fig.3.23** A sketch map of metal oxidation without NH₃.plasma pre-oxidation treatment. The length of the arrow means the oxidation speed.
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- Fig.3.27** TEM image of the sample with NH₃ plasma + 900°C post-oxidation anneal.

Chapter 4

- Fig.4.1** TiN/CoTiO/poly-Si capacitor fabrication process flow which include (a) pure NH₃ surface nitridation (b) Co/Ti deposited by PVD (c) NH₃/N₂O plasma pre-oxidation treatment (d) NH₃/N₂O plasma post-oxidation treatment (e) passivation oxide deposited by PECVD (f) after contact hole etched and metal pad defined and etched, the final structure was finished.
- Fig.4.2** J-E characteristic of substrate injection with various plasma treatment methods.
- Fig.4.3** J-E characteristic of gate injection with various plasma treatment methods.
- Fig.4.4** Weibull plot of the leakage current density at V_g =+1V

- Fig.4.5** Weibull plot of the leakage current density at $V_g = -1V$
- Fig.4.6** Weibull plot of the breakdown electric field under substrate injection.
- Fig.4.7** Weibull plot of the breakdown electric field under gate injection.
- Fig.4.8** Effective oxide thickness with various plasma treatment methods.
- Fig.4.9** Charge to breakdown characteristic under substrate injection.
- Fig.4.10** TDDB characteristic under substrate injection.
- Fig.4.11** TEM image of the as-oxidation sample.
- Fig.4.12** TEM image of the sample with NH_3 pre-oxidation treatment.
- Fig.4.13** TEM image of the sample with N_2O pre-oxidation treatment.
- Fig.4.14** TEM image of the sample with N_2O post-oxidation treatment.

Chapter 5

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- Fig.5.1** P-MOSCAP fabrication process (a) start material (b) LOCOS, tunnel oxide growth and poly-Si deposition (c) polyoxide fabrication (d) polyoxide etch-out and Al deposition (e) electrode pattern definition and back-side Al deposition.
- Fig.5.2** J-E characteristics of tunneling oxides with additional polyoxide (TEOS or NiTiO) process following poly-silicon gate deposition.
- Fig.5.3** Leakage current density (at $E=2.85MV/cm$) and E_{BD} statistics of tunneling oxides, with additional polyoxide (TEOS or NiTiO) process.
- Fig.5.4** High-frequency and quasi CV plots for the tunneling oxides with additional polyoxide (TEOS or NiTiO) process.
- Fig.5.5** Interface state densities of tunneling oxides with additional TEOS or NiTiO polyoxide process.
- Fig.5.6** TDDB analysis of tunneling oxides with TEOS or NiTiO films fabricated on top of poly-silicon gate.