Chapter 1

Introduction

1.1 General background

With the consumer electronic products are widely used everywhere, such as mobile phone, digital camera, PDA and etc. Memory had already become the important component [1]. According to the different memorial mechanism, it can be divided into two kinds. One is the volatile memory, such as DRAM (Dynamic Random Access Memory) and SRAM (Static Random Access Memory).The other is Non-volatile memory, such as mask read only memory (Mask ROM), programmable read only memory (PROM), electrically programmable read only memory (EPROM), electrically erasable programmable read only memory(EEPROM) and the flash memory.

Mask ROM is an embedded type memory, so it is commonly used in the memory cassettes for video game. It is inconvenient to producer, because if we only want to change one cell's condition (1 or 0), all of the mask must be reproduced. So PROM gradually replaces it.

EPROM is the first one that can program the memory cell by electrical method. Generally, it programs the memory cell by using channel hot electron (CHE) that was injected into floating gate. However, EPROM can't erase by electrical method. Illuminate the UV light erases it. So a quartz window is necessary on the package of the EPROM. However illuminate the UV light will erase entire memory cell; we can't

select the cell which we want to erase it.

The appearances of EEPROM solve the problem of EPROM that we described above. It can both program and erase by electrical method. But in order to achieve this merit, a select transistor is needed. So the memory cell density of EEPROM is lower than the EPROM. This shortage let the EEPROM only apply in lower storage capacity equipment. Flash memory follows the basic structure of EPROM. It can both program and erase by electrical method, but the select transistor isn't needed. So the memory cell size of flash memory is smaller than EEPROM. For this reason, it have huge amount of competitiveness in memory market.

1.2 Motivation

The sketch map of flash memory cell was shown in Fig.1.1, the tunneling oxide thickness was defined as D_1, the thickness of inter-poly dielectric was defined as D_2 ; the capacitance between floating gate and silicon substrate was defined as C_1, the capacitance between the floating gate and the control gate was define as C_2.

Now, if we apply a voltage V_{CG} to the control gate, silicon substrate was set to ground, the floating gate voltage V_{FG} will be described as follow:

$$V_{FG} = \frac{C_2}{C_1 + C_2} \times V_{CG}$$

The value of $C_2/(C_1+C_2)$ was so called coupling ratio. For low power consumption electronic product application, the flash need lower V_{CG} to achieve program/erase purpose. See the equation given above, the increase of the coupling ratio is a method to achieve the low voltage operation purpose. [2]

In order to increase the coupling ratio, the capacitance of inter-poly dielectric must be increase. There are two methods to achieve this purpose, the first is to

decrease the thickness of inter-poly dielectric, and the next is using high-k material as inter-poly dielectric. In the past years, silicon dioxide and oxide-nitride-oxide (ONO) structure was used as the material for inter-poly dielectric. However, as we described above, the higher coupling ratio, the thinner inter-poly dielectric was needed. According to the International Technology Roadmap for Semiconductors (ITRS) [3], Because of the ten years data retention time was required for flash memory, when the poly-oxide thickness is down below 100Å, there have no solution below this generation. So, it is to be imperative to replace the poly-oxide with high-k material. It is because under the same effective-oxide-thickness (EOT), high-k materials have lower leakage current than the silicon dioxide. [4]

There are various kinds of high-k materials; such as HfO_2, ZrO_2, La_2O_3, Si_3N_4, Al_2O_3, Ta_2O_5 and etc are two-component high-k material. Besides, $ZrTiO_3$, $BaSrTiO_3$, $CoTiO_3$, $NiTiO_3$ and etc are multi-component high-k material. Fig.1.2 shows some of these high-k materials, which include their dielectric constant. From Fig.1.2 we can observe that the more components of the high-k materials to have, the higher dielectric constant which the high-k materials will reveal and it also show that the increase of K value will decrease the band gap and breakdown electric field [5]. Besides, not all of the high-k materials are compatible for device fabrication process. One of the critical problems is the thermal stability with itself and with silicon. [4]

Lately, incorporating nitrogen into high-k materials such as HfO_2 and ZrO_2 improves the thermal stability and immunity to impurity diffusion during the subsequent thermal process. Moreover, the crystallization temperature was increased up to ~1000^{o}C.[6]-[8]

Pan et al shows the characteristic of the $NiTiO_3$ and $CoTiO_3$ on the single crystal Si and it exhibits high dielectric constant which is suitable for our demand [9]-[11]. In this thesis we investigated the basic electrical properties of NiTiO and CoTiO on the

poly-Si and we use the NH_3 and N_2O plasma to improve their qualities.

1.3 The Fundamentals of This Research

1.3.1 System Configuration

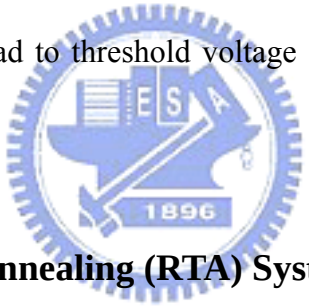
1.3.1.1 PECVD System

Fig.1.3 shows a diagram of a typical PECVD system. PECVD uses a radio frequency (rf) power to generate glow discharge to transfer the energy into the reactant gases, allowing the deposition of the substrate at a lower temperature than in the APCVD or the LPCVD process. Hence the low deposition temperature is a major advantage of PECVD. Desirable properties such as good adhesion, low pinhole density, good step coverage, adequate electrical properties, and compatibility with fine-line pattern transfer processes have made some PECVD films useful in ULSI circuits .Plasma-deposited nitride and oxide can be used as insulators between the metal layers , especially since the underlying metals have low melting points. PECVD also provides deposition of amorphous silicon films, although these films have not yet been used in the ULSI circuits. The PECVD amorphous silicon has been widely applied in TFT LCDs.

The plasma is generated by the application an r.f. field to a low pressure gas, thereby creating free electrons within the discharge region. T he electrons gain their energy form the electric field. When they collide with gas molecules, the reactants gases (e.g., silane and nitrogen or oxygen-containing species) dissociate and ionize. The energetic species are then adsorbed on the film surface. These radicals tend to have high sticking coefficients and also appear to migrate easily along the surface after adsorption. These two factors can lead to excellent film conformality. Upon

being adsorbed on the substrate, the radicals are subjected to ion and electron bombardment and rearrangements and react with other adsorbed species to form new bonds and the resulting film .Atom rearrangement includes diffusion of the absorbed atoms onto stable sites and concurrent desorption of reaction products. The desorption rates depend on the substrate temperatures; higher temperatures produce films with fewer entrapped by-products. Note that homogeneous gas-phase nucleation should be avoided to produce particulate contamination.

The fact that the radicals formed in the plasma discharge are highly reactive causes some stoichiometric problems, because the reactions are so varied and complicated. Moreover, the by-products and incidental species are incorporated into the reactant films, especially hydrogen, nitrogen, and oxygen. Excessive incorporation of these contaminants may lead to threshold voltage shifts in MOS circuits that use these PECVD films.



1.3.1.2 Rapid Thermal Annealing (RTA) System

Introducing dopant atoms into a semiconductor is only the first step in changing its electrical properties. As discussed in some papers. Implantation damages the target and displaces many atoms for each implanted ion. The electrical behavior after implantation is dominated by deep-level electron and hole traps, which capture carriers and make the resistivity high. Annealing is required to repair lattice damage and put dopant atoms on substitutional sites where they will be electrically active. The success of annealing is often measured in terms of the fraction of the dopant that is electrically active, as found experimentally using a Hall Effect technique. The Hall Effect measures an average effective doping, which is an integral over local doping densities and local mobilities evaluated per unit of surface area. For VLSI, the

challenge in annealing is not simply to repair damage and activate dopant, which any long, high-temperature anneal will achieve, but to do so while minimizing diffusion so that shallow implants remain shallow. In addition, the rapid thermal N_2O/N_2 annealing for densification is required to improve characteristics of CVD oxide. All of this has motivated much recent work in rapid thermal annealing (RTA), where annealing time are on the order of seconds.

Fig.1.4 shows a schematic diagram of an isothermal rapid annealing system. Isothermal annealing covers heating process longer than 1s, including furnace steps. Rapid isothermal annealing uses tungsten-halogen lamps or graphite resistive strips to heat the wafer form one or both sides. This offers significant advantages for VLSI processing because good activation can be obtained with less diffusion than with furnace annealing. The process is also cleaner because the walls of the chamber remain cold. RTA heating occurs because photons are absorbed by free carriers in the silicon, which then transfer their energy to the lattice. The heating rate depends on the number of carriers, which is a function of temperature and doping, and on surface emissivity. This makes temperature measurement difficult because the probe must have absorption characteristics similar to the wafers being processed. Therefore, small thermocouples and optical pyrometers are often used.

1.3.2 Oxide Integrity Measurement

1.3.2.1 Basic I-V Characteristics

The phenomenon of carrier injection into the oxide by tunneling is due to the quantum-mechanical nature of the electron. In the classical sense, the oxide represents an impenetrable barrier to injection of electrons into the conduction-band of the

silicon if they process kinetic energies smaller than 3.1Ev.Howere; the wave nature of the electron (or hole) allows a finite probability of crossing the barrier even if the electron does not possess sufficient kinetic energy. This probability increases with larger gate electric fields and/or thinner barriers. Electrons injected by tunneling are generally considered to be in equilibrium with the lattice, and thus are characterized as being"cold", i.e., not "hot"

Fig.1.5 shows a diagram of three tunneling mechanisms. The first type of tunneling is called direct tunneling. For gate oxides thinner than 6nm, the tunneling current is observed to exhibit a weaker dependence on oxide fields. This has been explained by attributing the gate current in such oxides to direct tunneling through the forbidden gap of the SiO2 to the gate electrode. Such direct tunneling is known to occur in thin oxides at low voltages. An expression for the tunneling probability can be derived, but no analytical expression is available as in the case of F-N tunneling.

The second type of tunneling is called Fowler-Nordheim tunneling. Here electrons are injected by tunneling into the conduction band of the oxide through the triangular energy barrier. Once injected into the oxide conduction band, electrons are accelerated by the oxide field toward the anode (gate), causing a gate current. To determine the probability of an electron exhibiting F-N tunneling through a barrier, Schroedinger's equation is solved for a triangular barrier. The WKB approximation is adopted, and the following expression for the tunneling current is derived:

$$J= AE^2 \exp(-B/E)$$

Where $A=q^3m_0/8\pi hem_e^*$,$B=8\pi(2m_e^*)^{1/2}(e\psi_b)^{3/2}/3eh$, J is current density in A/cm^2,and E is the oxide field in V/cm. According to this equation, the oxide current is exponentially dependent on the electrons field and experimental studies have found that the equation accurately describes the oxide current. It should also be noted that it may be possible for electrons to be hot but not possess sufficient energy to surmount

the barrier. In this case, carrier injection may occur by allowing these hot carriers to tunnel through a smaller triangular barrier distance.

The Frenkel-Poole emission, shown in the insert of Fig.1.5(c), is due to field-enhanced thermal excitation of trapped electrons into the conduction band. For traps states with coulomb potentials, the expression is virtually identical to that of the Schottky emission. The barrier height, however, is the depth of the trap potential well.

1.3.2.2 Measuring Time-Dependent Breakdown Behavior

If the electric field in the oxide E_{0X} is kept constant during the stress test (implying also that the applied voltage is held constant), the biasing time (instead of the oxide voltage) becomes the variable. The length of time t_{BD} elapsed until breakdown occurs is then measured. The time-to-breakdown behavior of a group of oxide samples under such test conditions is referred to as time-dependent dielectric breakdown(TDDB).Breakdown is said to occur when the voltage across the oxide suddenly drops. This test is frequently referred to as the constant-voltage time-to-breakdown test.

An alternative to the constant-voltage test is the constant-current time-to breakdown test. Here, a preset current is injected into the oxide (by Fowler-Nordheim injection), and this value I_{inj} is held constant as the test proceeds. Voltage and time are recorded until the voltage suddenly drops. Results from such tests indicate that the time-to-breakdown is dependent on the value of the current density $J_{inj}=I_{inj}/A$-the larger the current density, the shorter the time t_{BD} until breakdown occurs.

If the constant-current test is used to determine t_{BD}, the product of the current density and t_{BD} provides another measure of the oxide breakdown behavior. This quantity is referred to as the charge-to-breakdown Q_{bd}. When comparing oxide

breakdown behavior, those oxides exhibiting larger Q_{bd} are deeming superior. In a constant-current test the value of Q_{bd} is simply calculated form

$$Q_{BD} = J_{inj} \times t_{BD}$$

It has been found that for smaller values of J_{inj} the value of Q_{bd} for defect-free gate oxide films (i.e., intrinsic oxides) is constant as a function of the magnitude of J_{inj}.For larger values of J_{inj} the value of Q_{bd} must be used (i.e, Q_{bd} is the time integral of J_{inj} form the time the bias is applied, to the time of breakdown)

$$Q_{BD} = \int_0^{t_{BD}} J_{inj}\, dt$$

For larger values of J_{inj} the value of Q_{bd} tends to decrease.

1.3.2.3 Mathematics of Reliability Characteristics

The dielectric strength (E_{ox} at breakdown observed in the ramp-voltage test), the time-to-breakdown t_{BD}, or charge-to- breakdown Q_{bd} are all important parameters that describe the breakdown of a single oxide sample. However, in a group of oxide samples of the same area and thickness the above values will vary from sample to sample. The reliability of an oxide id defined as “the probability that it will not suffer breakdown under the stated operating conditions for the defined lifetime of the system”. Here we present the terms and the mathematical functions with which oxide reliability is quantitatively characterized.

Let there be N devices in a population, whose ”reliability” one wishes to determine, and let these devices be placed under test at a time “t”. It is observed $N_f(t)$ of the devices have failed and that $N_s(t)=N-N_f(t)$ devices have survived. The ratio of surviving devices to the number of original devices placed under test (N_s/N) is defined as the reliability. Similarly, the ratio of $N_f(t)/N$ is a measure of the unreliability of the

devices and is usually termed the cumulative distribution (or failure) function F(t). F(t) describes the probability that a device will fail at a time before time t. In general, F(t) has the following properties:

$$F(t)=0 \qquad t < 0$$

$$0 \leqq F(t) \leqq F(t`) \qquad 0 \leqq t \leqq t`$$

$$F(t)->1 \qquad t->1$$

The cumulative failure percentage (i.e. the fraction of parts from a group of samples that will fail prior to a specific time t) can be obtained from F (t). The time-to-failure data from the constant-voltage or constant-current tests are frequently plotted on a cumulative percentage failure graph, with the time axis scale plotted in terms of ln t.

If the failure rate of a group of parts varies as the power of the age of the device (as is observed to be the case of oxide breakdown failures), the time-to-failure versus cumulative percentage failure is likely to be well fitted with a Weibull cumulative distribution function. The early failure of gate oxides can be represented by a Weibull distribution, and Weibull plotting paper is often used in presenting oxide TDDB data. The failure rate of parts whose failure statistics can be represented with the Weibull function is expressed as

$$\lambda(t) = (\beta/\alpha) \times t^{\beta-1}$$

where α and β are constants. From Eq.2-5 we can calculate that

$$F(t) = 1-\exp\left[-(1/\alpha)\times t^{\beta}\right]$$

When experimental data is fitted to an assumed cumulative failure function to determine the function parameters as well as the goodness of fit, appropriate plotting paper must be used. That is, the scales of the paper must be such that the experimental data will lie on a straight line if the data is well represented by the assumed distribution. Such plotting paper is available for use with the Weibull distribution function. For the Weibull distribution function

$$1\text{-}F(t) = \exp\left[-(1/\alpha) \times t^{\beta}\right]$$

$$\ln\left\{\ln\left[1\text{-}F(t)\right]^{-1}\right\} = \beta \ln t - \ln\alpha$$

which is linear in the form y = mx + b.

1.4 Organization of the Thesis

In Chapter 1, the background of memory, the fundamentals of this research and motivation of this thesis are described.

In Chapter 2, the basic electrical characteristics of nickel titanium oxide on poly-Si are presented, and we also show the thermal stability of this film by post-oxidation anneal.

In Chapter 3, NH_3 plasma was applied to our NiTiO process as the metal pre-oxidation treatment; we compare the thermal stability and electrical reliability between the NiTiO with NH_3 plasma pre-oxidation treatment and without NH_3 plasma pre-oxidation treatment.

In Chapter 4, the basic electrical characteristic of coble titanium oxide on poly-Si are presented, and we also show the properties of coble titanium oxide with NH_3 or N_2O plasma pre-oxidation treatment and we compare the pre-oxidation treatment and post-oxidation treatment by the NH_3 or N_2O plasma.

In Chapter 5, we investigated the influence of our metal oxidation process to the tunneling oxide. When the nickel titanium oxide was used as inter-poly dielectric

At the end of this thesis, conclusions are given in Chapter 6.

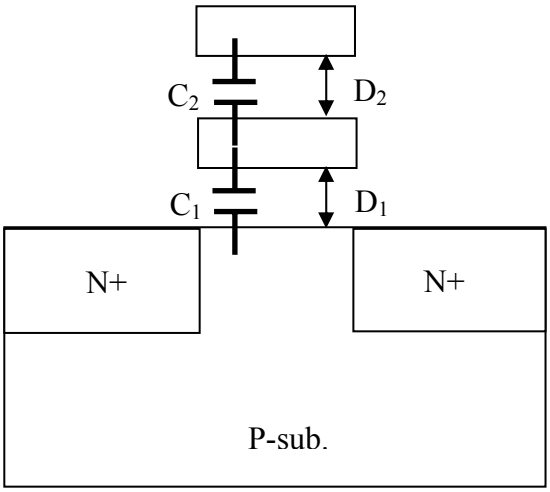


Fig.1.1 Basic flash memory cell structure

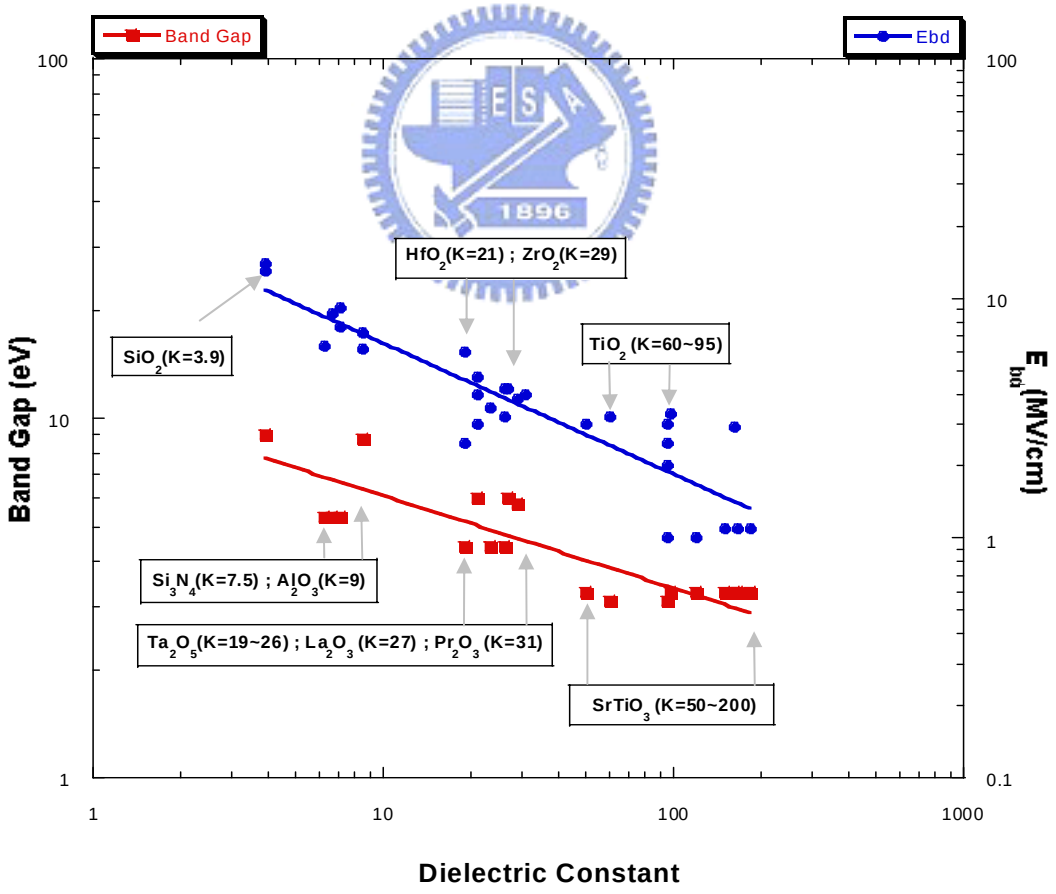


Fig.1.2 The relation between dielectric constant with band gap and breakdown electric field.

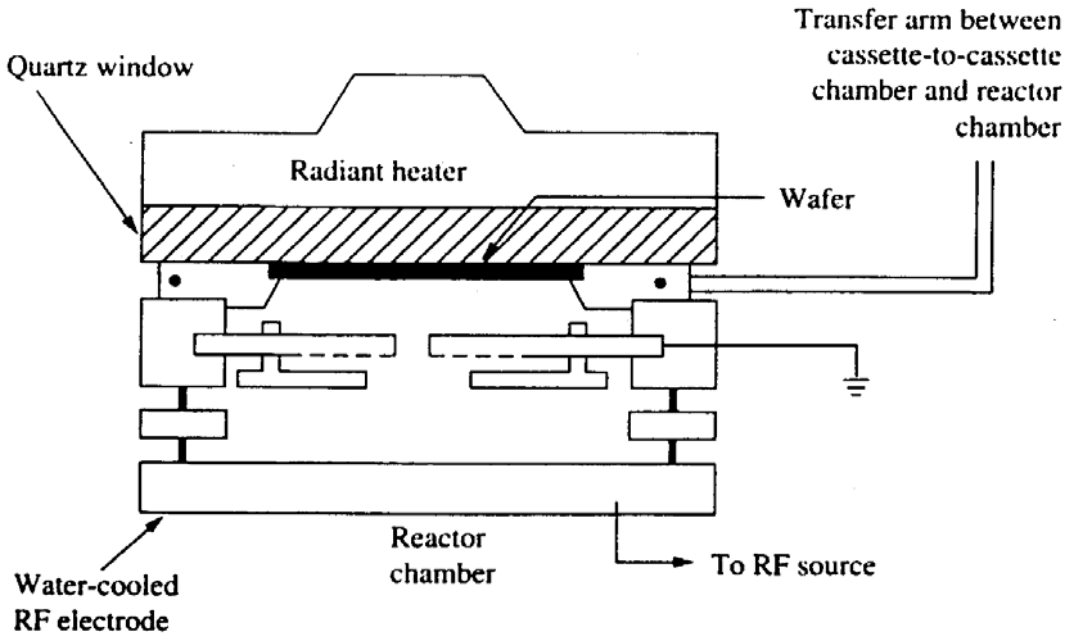


Fig.1.3 A diagram of the typical PECVD system

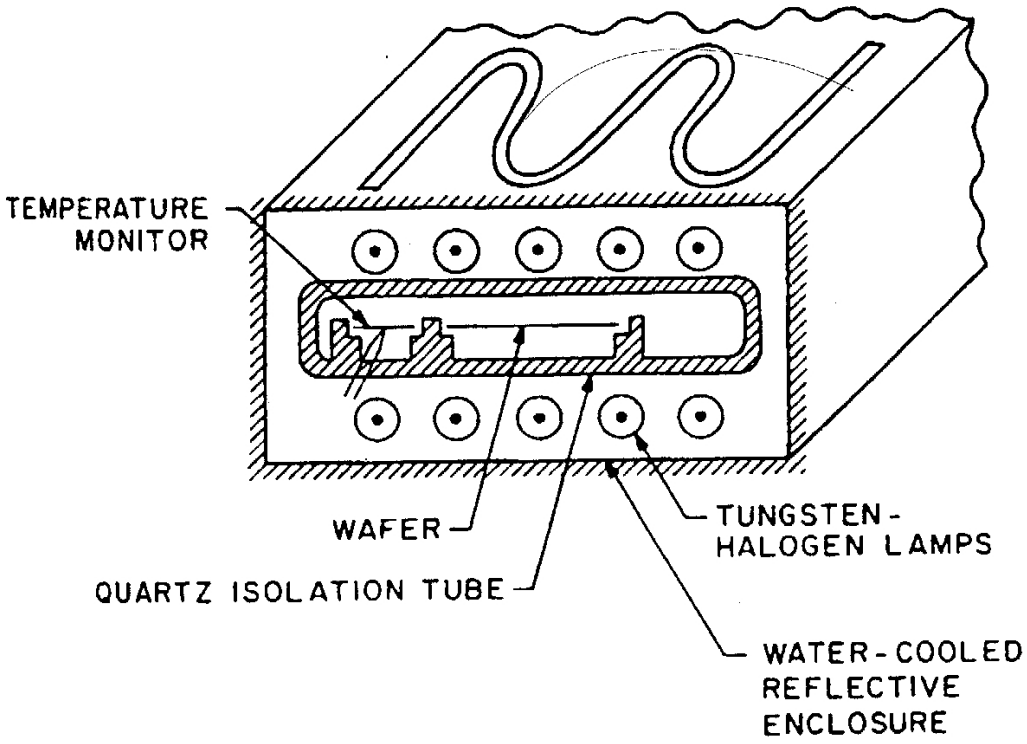
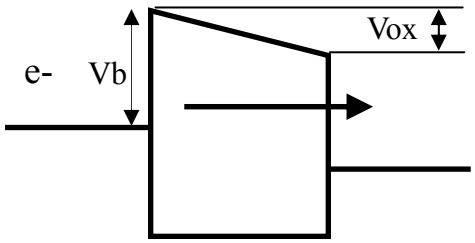
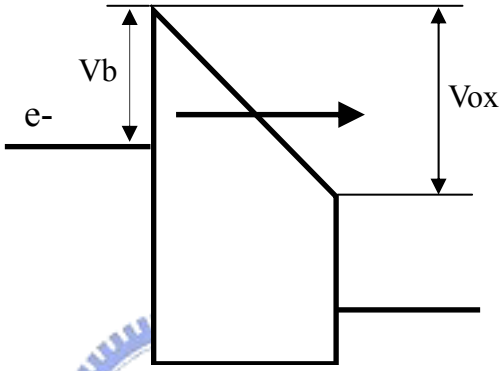


Fig.1.4 A diagram of the RTA system



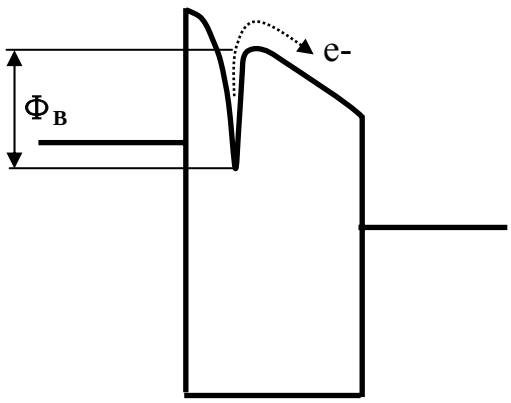
Vox < Vb

(a) Direct Tunneling



Vox > Vb

(b) F-N Tunneling



(c) Trap Assisted Tunneling

(F-P Tunneling)

Fig.1.5 Three tunneling mechanisms (a) Direct tunneling (b) F-N tunneling (c) F-P tunnelung

Chapter 2

Characteristics of NiTiO Interpoly Dielectric by Post Oxidation Anneal

2.1 Introduction

Recent years, many materials systems are currently under consideration as potential replacements for SiO_2 as the gate dielectric material, DRAM storage capacitance, and non-volatility memory interpoly dielectric. For a new high-k material application in device fabrication, the guidelines are (a) permittivity, band gap, and band alignment to silicon, (b) thermodynamic stability, (c) film morphology, (d) interface quality, (e) compatible with the current or expected materials to be used in processing for device, (f) process compatibility and (g) reliability. [4]

In this work, for the first time, we investigated the thermal stability of NiTiO high-k material. We use post-oxidation anneal to model the high temperature step which it will use in device fabrication process.

2.2 Experimental Procedure

N+-polysilicon/NiTiO/TiN capacitors were fabricated on 6-inches <100> p-type wafer with resistivity of 5-10 Ω-cm. Fig.2.1 shows the process flow chart and cross section view for each main step. First, a 3000Å field oxide was thermal grown by wet oxidation at 800°C to serve as isolation substrate. After 3000Å in-situ doped amorphous silicon deposited by LPCVD system, furnace annealing 800°C 2 hours

was used to turn it to poly silicon and activated the dopant.

Before metal deposition, NH_3 surface nitridation was used to grow a thin Si_3N_4 layer, as shown in Fig.2.1(a). Afterward, all samples were immediately deposited in sequence with Ti (50 Å) and then Ni (50 Å) film from independent targets by using PVD method, as shown in Fig.2.1(b). The direct thermal oxidation was carried out at 800°C in diluted O_2 (N_2/O_2=2/1) gas. Then 800°C 60sec. and 900°C 60sec. post oxidation annealing were used to investigate the thermal stability of the NiTiO film, as shown in Fig.2.1(c). 150nm thick TiN metal gate was formed by sputter in 50% N_2 ambient (Ar:N_2=1:1). The gate regions were patterned by lithography and etched by ILD4100 metal etcher. Moreover, as shown in Fig.2.1(d), a 3000Å SiO_2 film was deposited as passivation layer by PECVD system and contact hole was etched by dry etching. Finally, a 5000Å Al gate electrode was deposited by physical vapor deposition and defined the metal pad by ILD4100 metal etcher, as shown in Fig. 2.1(e).

2.3 Results and Discussion

In this section, electrical and physical characteristics of NiTiO on poly-Si with various post-deposited treatment were discussed.

2.3.1 J-E Characteristic

Fig.2.2 and Fig.2.3 plot the J-E characteristics of NiTiO with various post-oxidation anneal under positive gate bias and negative gate bias, respectively. Low field leakage current and high field leakage current are rising with the increase of annealing temperature. The weibull distribution of low field leakage current density under substrate injection and gate injection were shown in Fig.2.4 and Fig.2.5, respectively. After 900°C 60sec. anneal, the magnitude of leakage current density

shows an increase of more than one order. The weibull distribution of breakdown electric field under substrate injection and gate injection were shown in Fig.2.6 and Fig.2.7, respectively. After 900°C 60sec. anneal, the magnitude of breakdown electric field shows a decrease of 0.5MV/cm. This drop off occur after 800°C 60 sec. annealing for gate injection and take place after 900°C 60sec. annealing for substrate injection.

2.3.2 Charge to Breakdown Characteristic

Fig.2.8 shows the charge to breakdown characteristic with stress current density 0.2mA/cm^2. NiTiO on poly-Si reveals the Q_{BD} value equal to 0.006C/cm^2. With the post-oxidation anneal, Q_{BD} value will decrease to 0.003C/cm^2. These values are smaller than the thermal oxide which is thermal growing on poly-Si.[12]

2.3.3 TDDB Characteristics

Fig.2.9 presents the TDDB characteristics of NiTiO on poly-Si. Fitting three points of the positive breakdown voltage for each sample draws the projected 10-years lifetime. From this plot, NiTiO on poly-Si reveal 2.05 (volt) ten years operation voltages. Sample with 900°C 60sec. post-oxidation anneal will degrade the reliability of NiTiO on poly-Si. Ten years operation voltage decrease from 2.05(volt) to 0.8(volt).

2.3.4 AFM Surface Roughness Analysis

The electrical performance of interpoly dielectric is strong relation to the roughness between the electrode and dielectric interface [12]-[14]. Fig.2.10 to Fig.2.12 show the surface roughness of NiTiO with various post-oxidation anneal. Because we didn't find the NiTiO wet etch solution, so we can't present the interface roughness between NiTiO and poly-Si. From these plots, surface roughness didn't raise with the increase of the anneal temperature. So we think that electrical properties

degradation may not attribute to the change of the surface roughness.

2.3.5 TEM Image

Fig.2.13 and Fig.2.14 show the TEM image of NiTiO on poly-Si and NiTiO on poly-Si with 900^{o}C 60sec. annealing, respectively. All samples show nearly the same physical thickness 200Å. Even with 900^{o}C post-oxidation annealing, the thickness of the interfacial layer still equal to 50Å. In addition, after 900^{o}C annealing, the black portion become larger than the as-oxidation sample. Therefore, we think that some crystal phase formed after 900^{o}C annealing and these phases result in the electrical properties degradation.

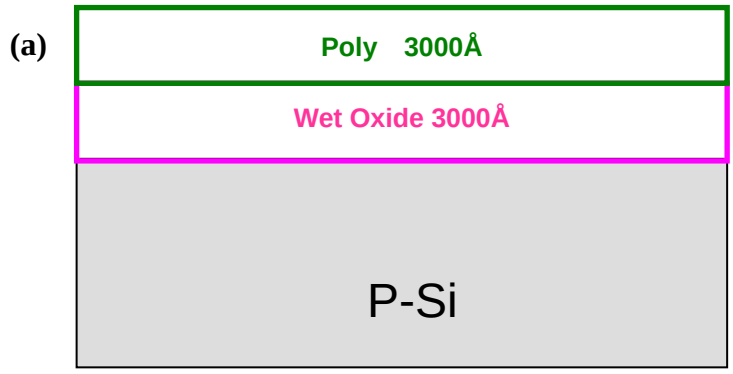
2.3.6 AES analysis

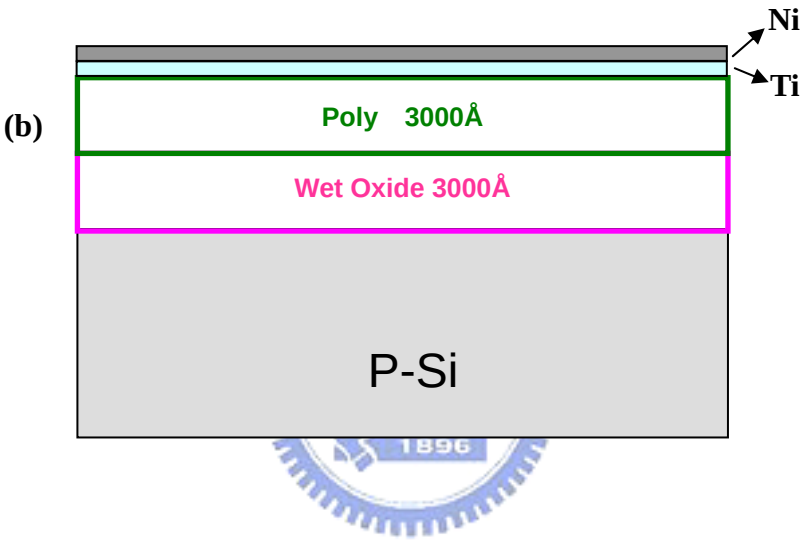
Fig.2.15 and Fig. 2.16 present the AES depth profile of NiTiO on poly-Si and NiTiO on poly-Si with 900^{o}C 60sec. annealing, respectively. The physical thickness of sample with 900^{o}C annealing seems thicker than the as-oxidation sample. This result isn't consistent with TEM image. We believe machine sputter rate is different from two samples. Because of the machine can't distinguish nitrogen signal and titanium signal, so nitrogen profile isn't presented in these plots. We think that the interfacial layer, from these plots, is a composite of Ni, Ti, O, Si and N. Nitrogen is introduced by the process step of surface nitridation on poli-Si.

2.4 Summary

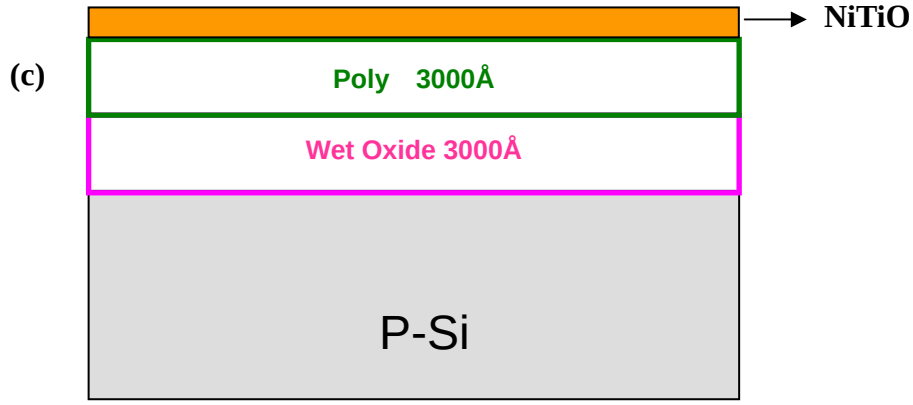
In this chapter, the basic characteristic of the NiTiO on the poly-Si with various temperatures of the post-oxidation annealing was presented. From our result, post-oxidation annealing will degrade electrical properties of NiTiO. By TEM images, these properties degradation may due to some crystal phases formed in NiTiO film after 900^{o}C 60 seconds annealing.

Pure NH_3 surface nitridation





Rapid Thermal Anneal



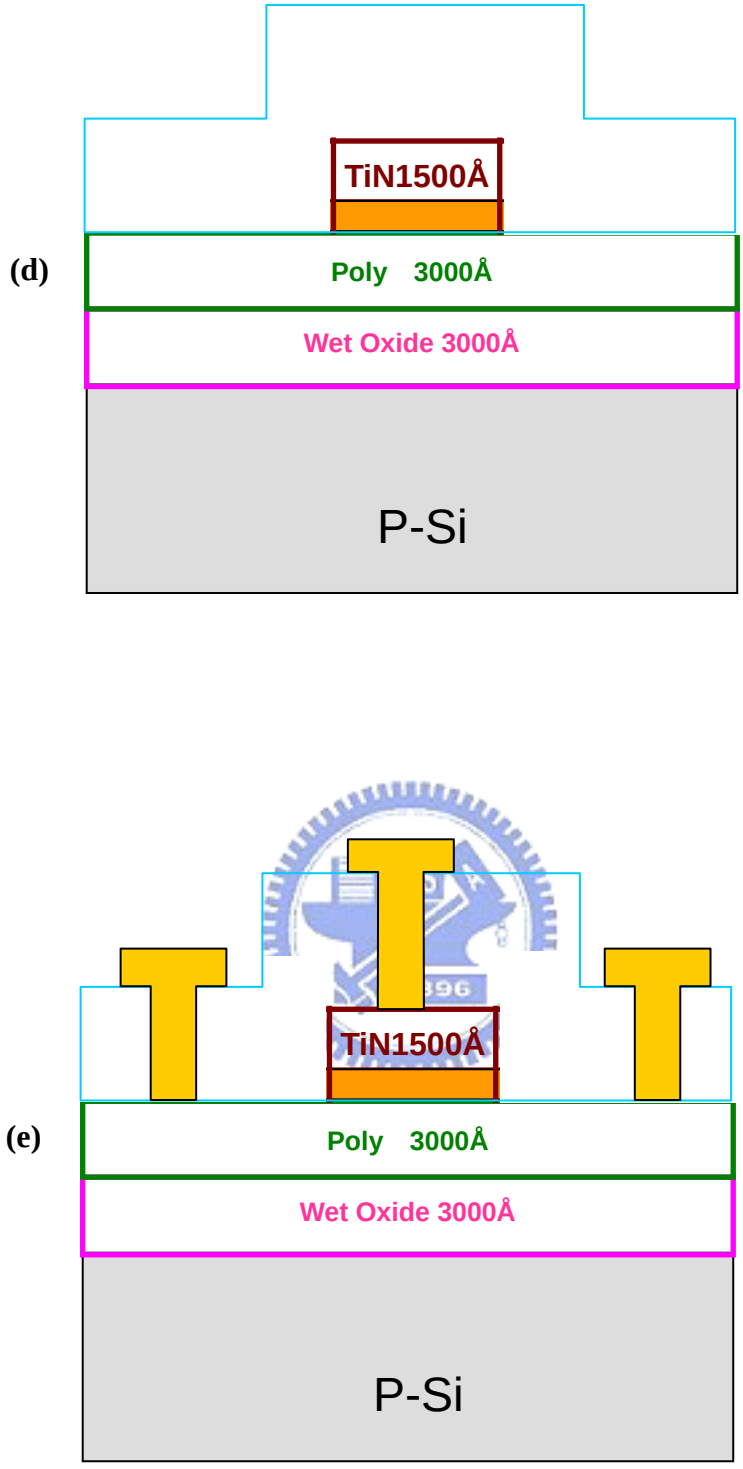


Fig.2.1 TiN/NiTiO/poly-Si capacitor fabrication process flow which include (a) after pure NH_3 surface nitridation (b) after Ni/Ti stack was deposited by PVD (c) rapid thermal anneal (d) after define gate, passivation oxide was deposited by PECVD (e) after contact hole etched and metal pad defined and etched, the final structure was finished.

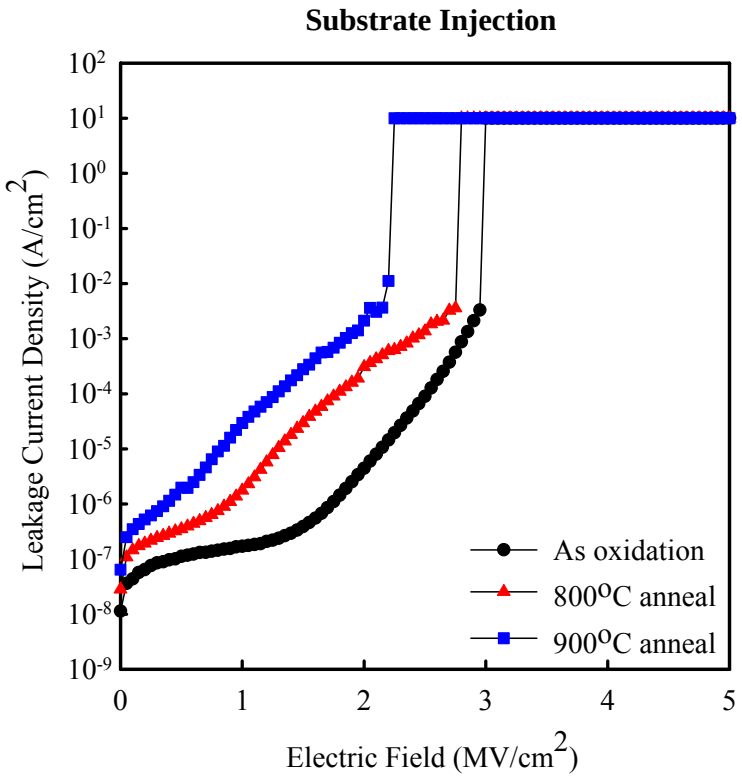


Fig.2.2 J-E curve with various post-oxidation anneal temperature, under positive gate bias.

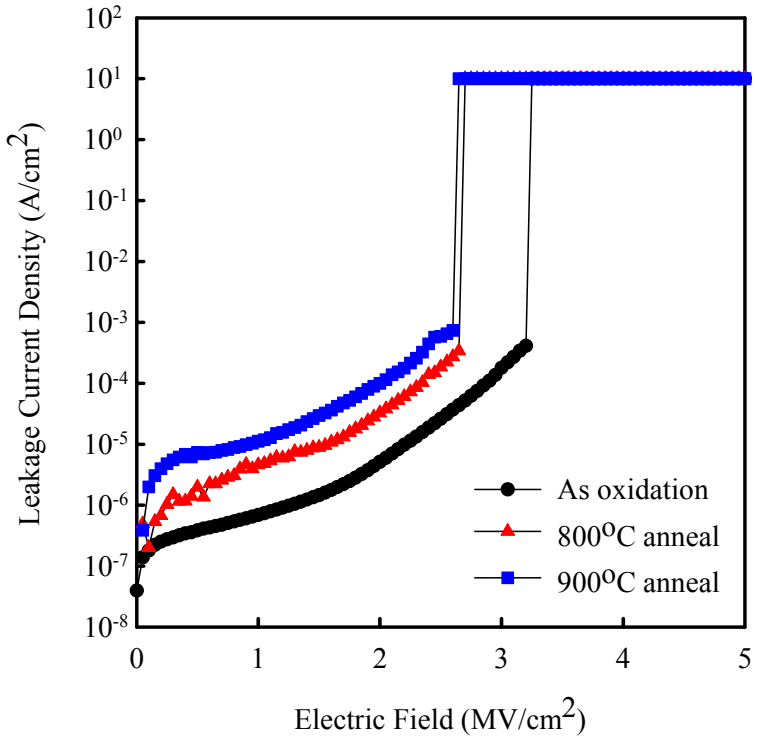


Fig.2.3 J-E curve with various post-oxidation anneal temperature, under negative gate bias.

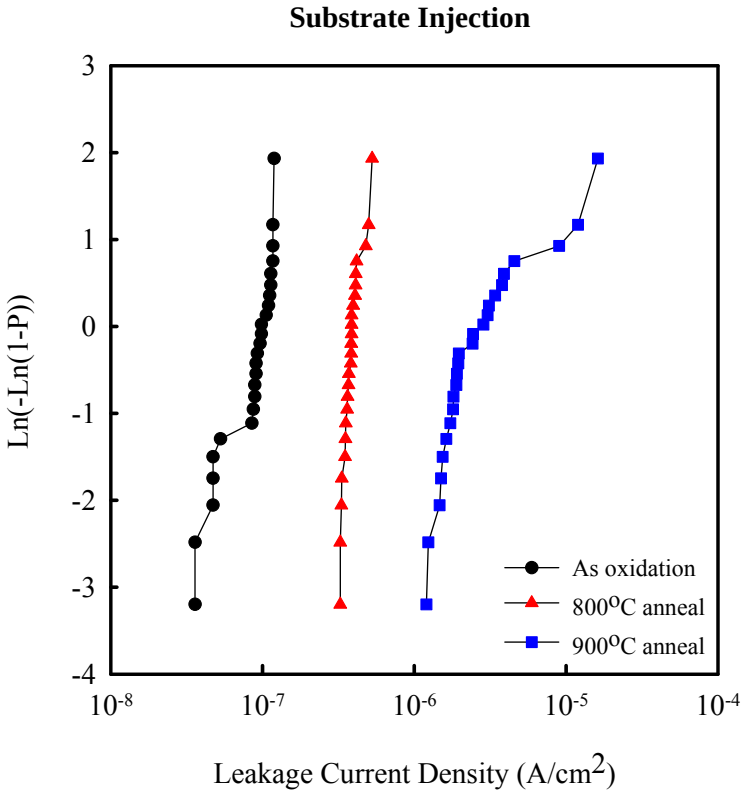


Fig.2.4 Weibull distribution of leakage current density at Vg= +1V with various post-oxidation anneal.

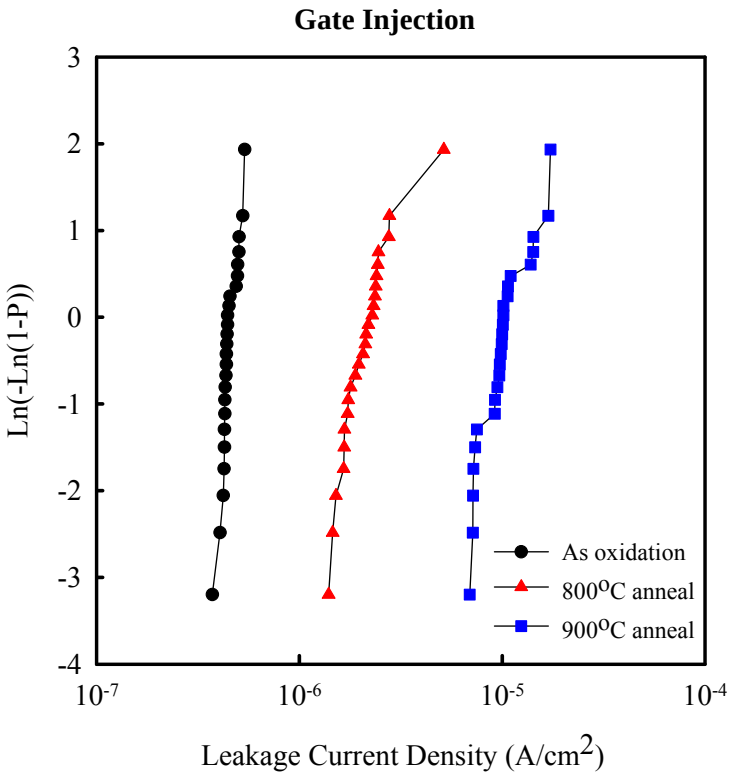


Fig.2.5 Weibull distribution of leakage current density at Vg= -1V with various post-oxidation anneal.

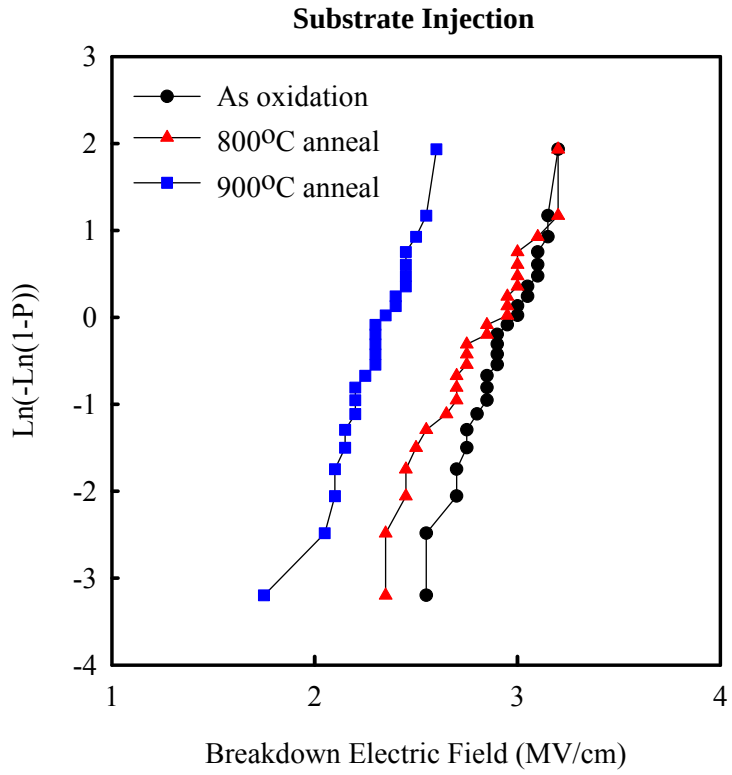


Fig.2.6 Weibull distribution of breakdown electric field with various pre-oxidation anneal, under positive gate bias.

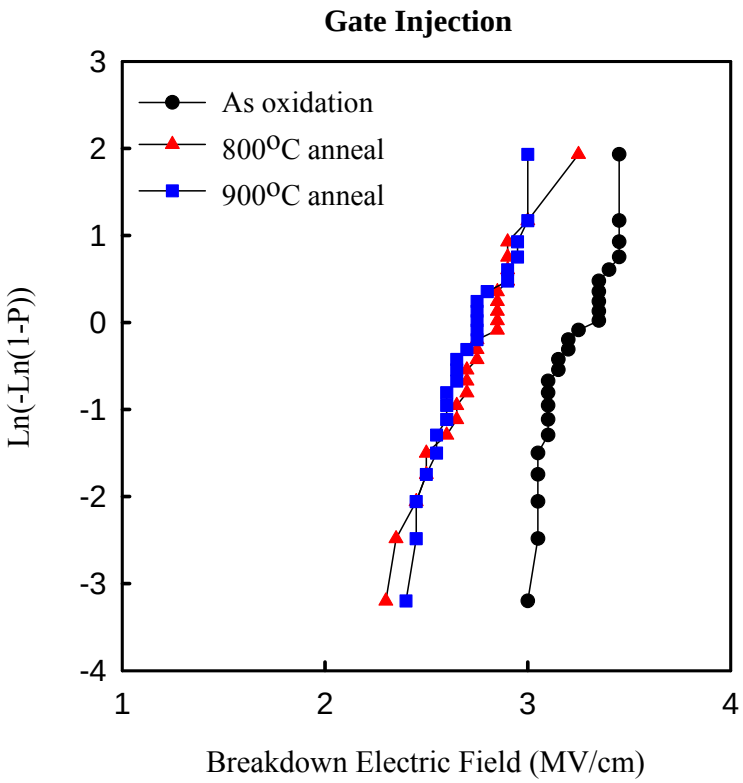


Fig.2.7 Weibull distribution of breakdown electric field with various post-oxidation anneal, under negative gate bias.

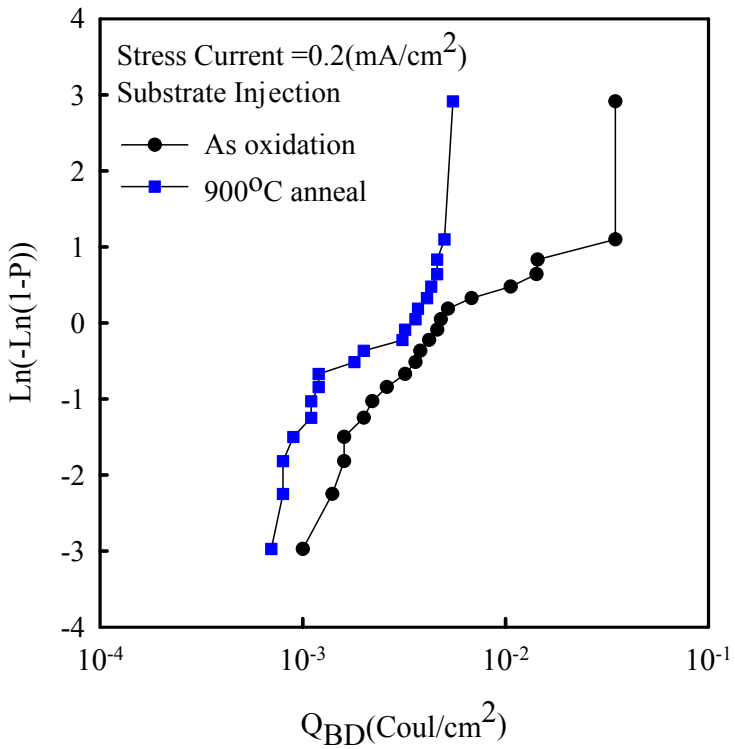


Fig.2.8 Weibull distribution of breakdown charge with various post-oxidation anneal, under positive gate bias.

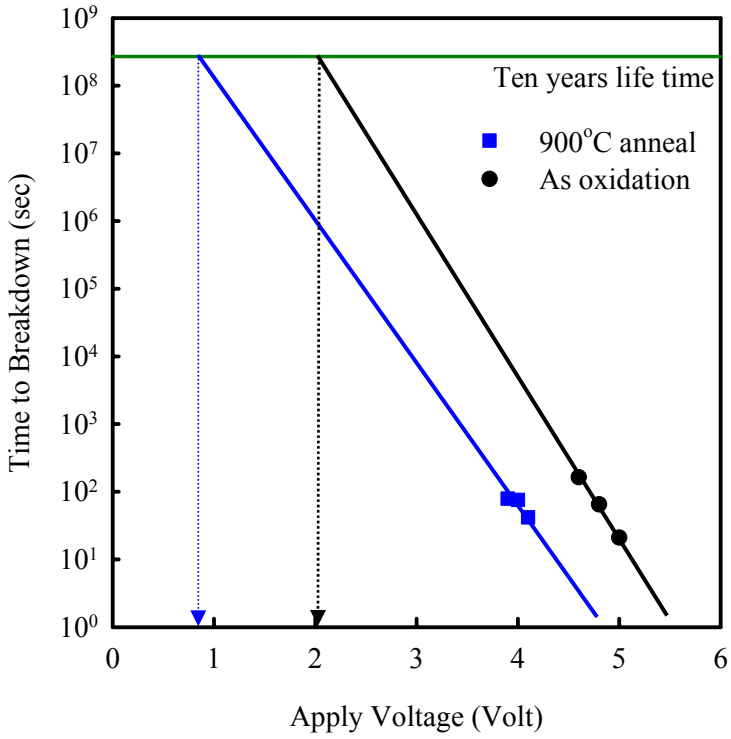


Fig.2.9 TDDB characteristic with various post-oxidation anneal, under positive gate bias.

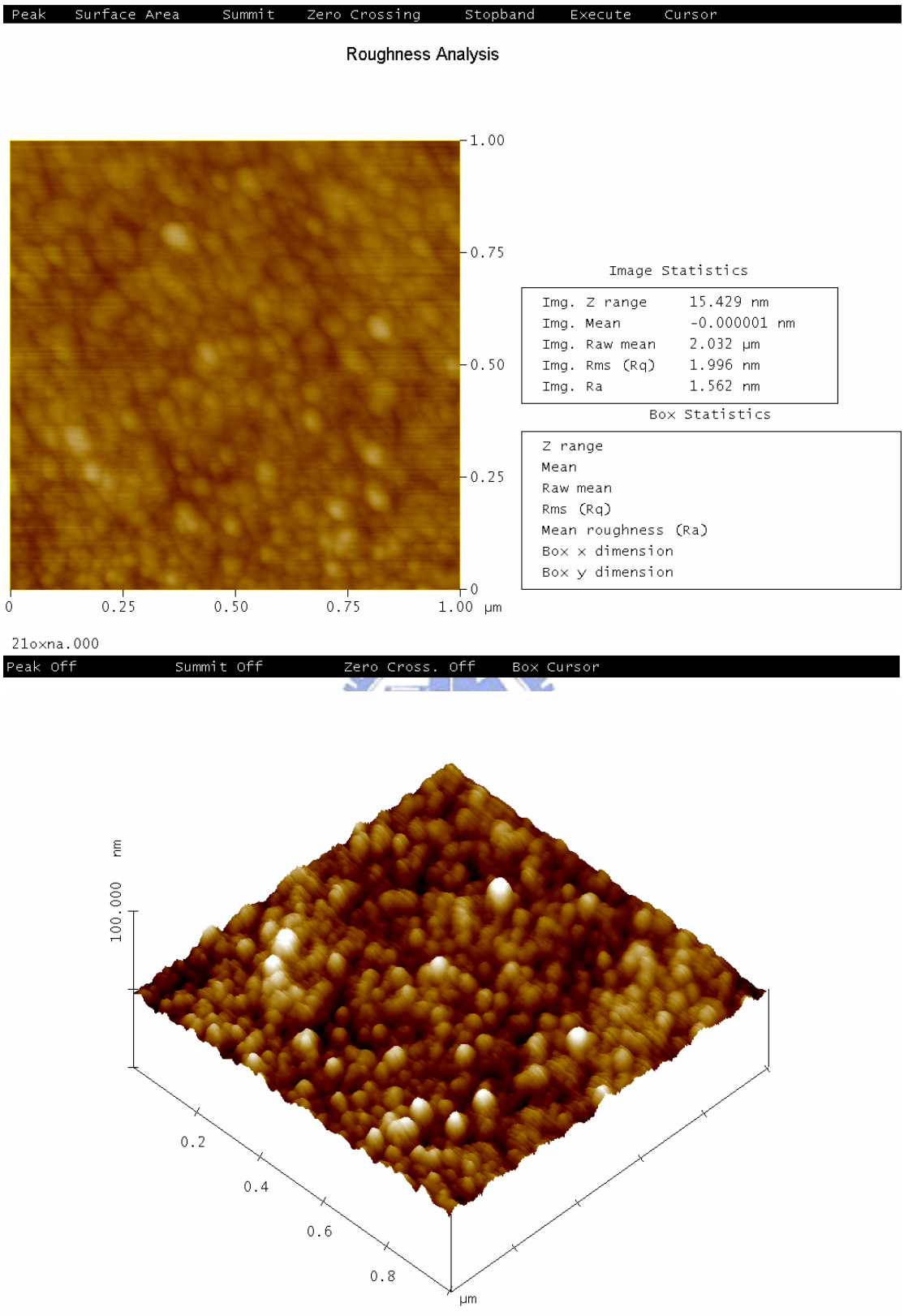


Fig.2.10 AFM surface roughness of the as-oxidation sample.

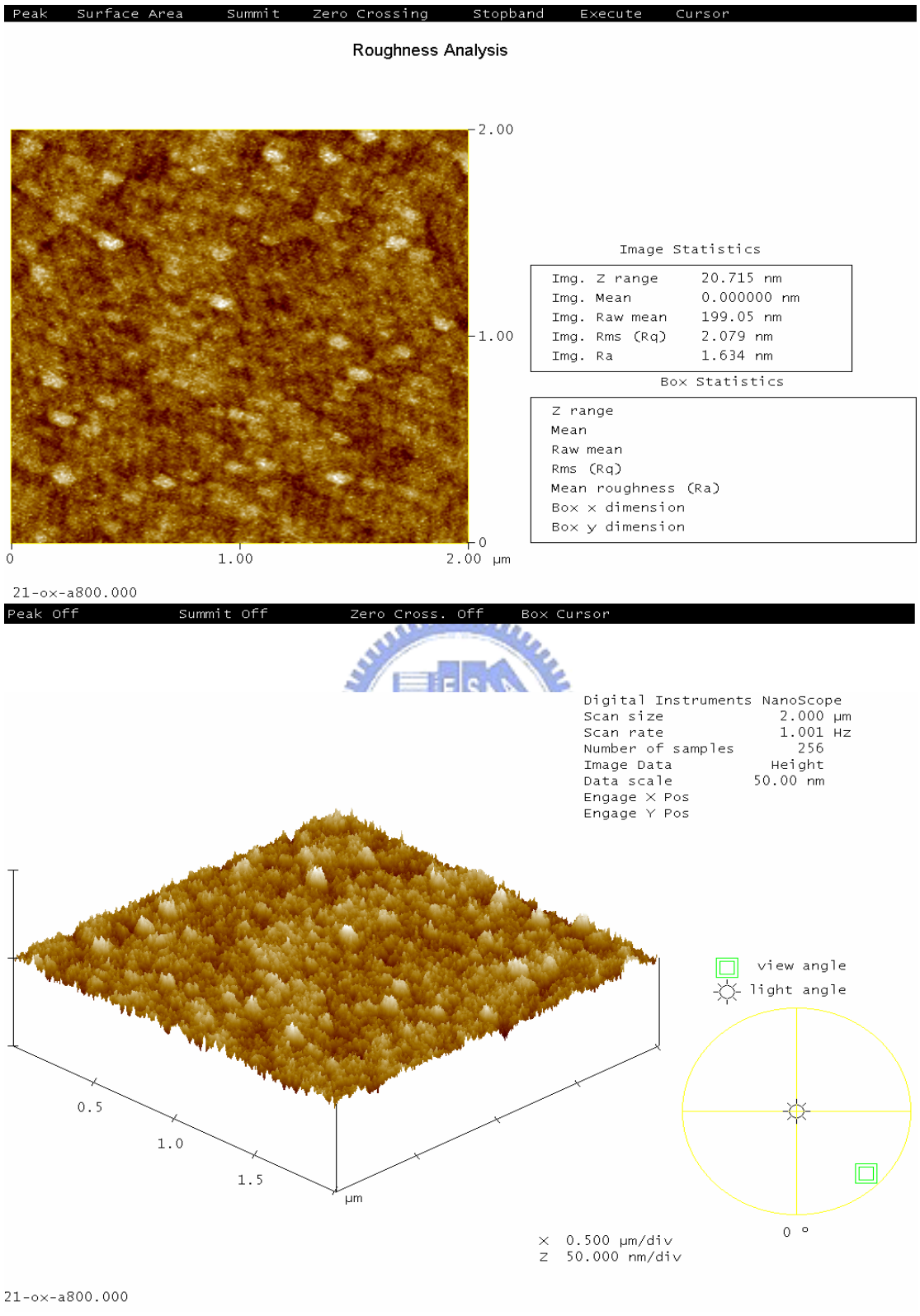


Fig.2.11 AFM surface roughness of the NiTiO with 800°C anneal.

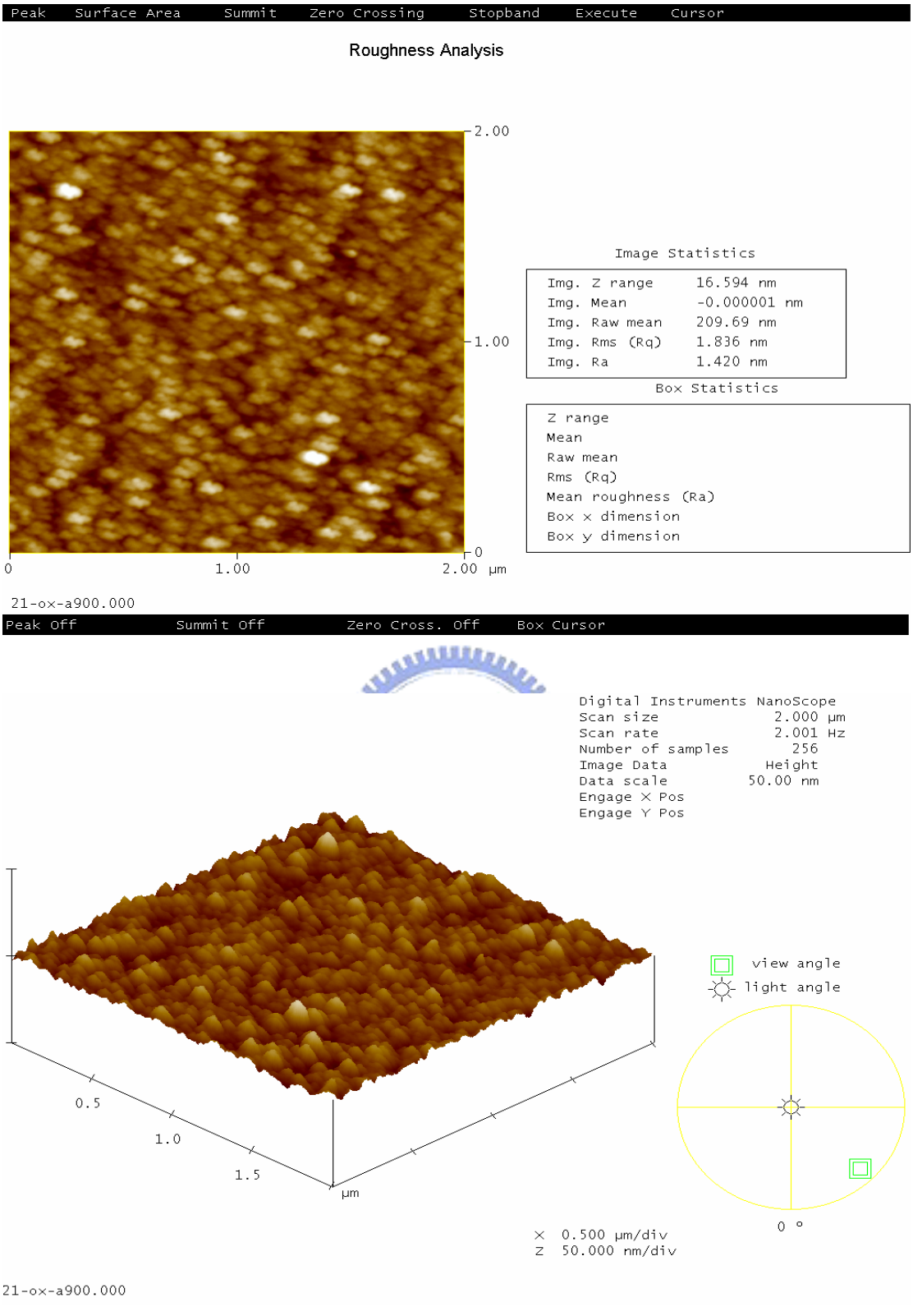


Fig.2.12 AFM surface roughness of the NiTiO with 900°C anneal.

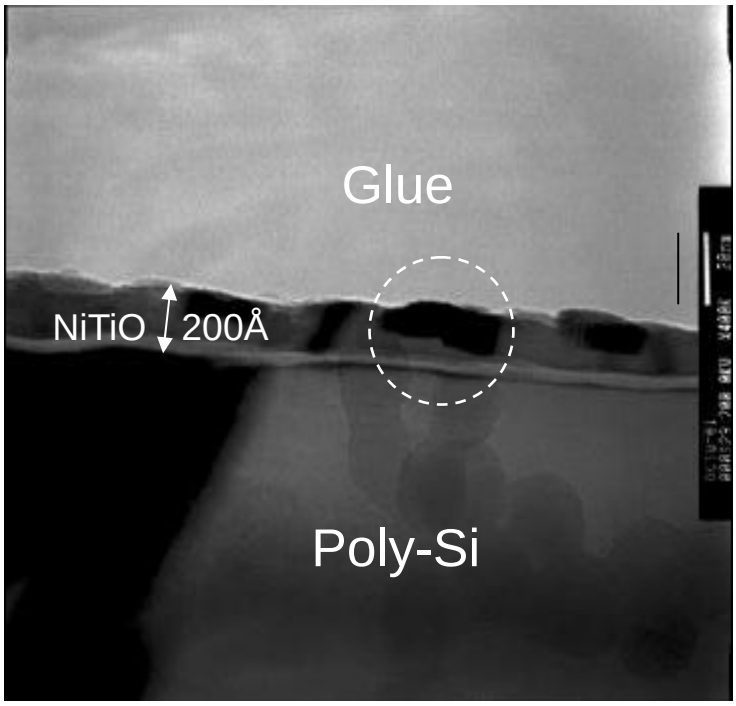


Fig.2.13 TEM image of the as-oxidation sample.

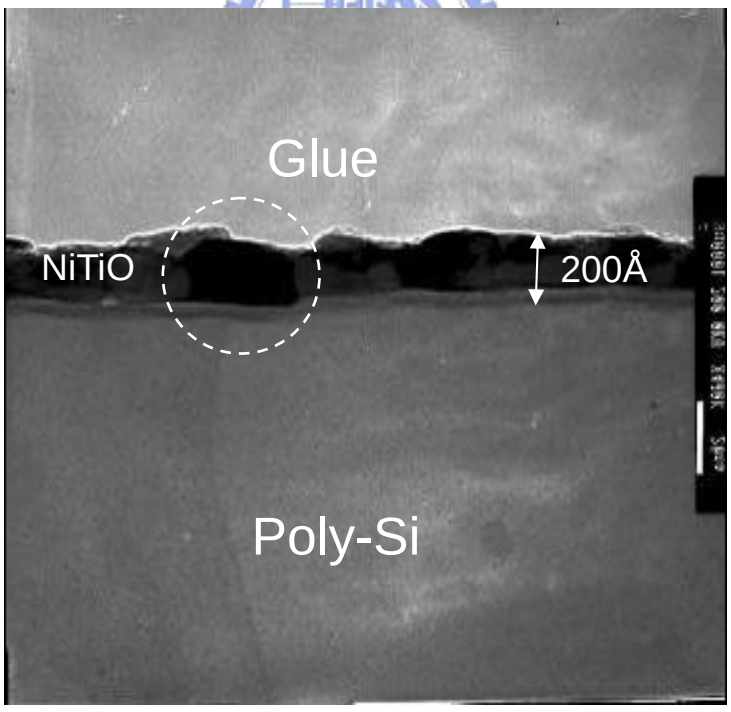


Fig.2.14 TEM image of the NiTiO with 900^{o}C anneal.

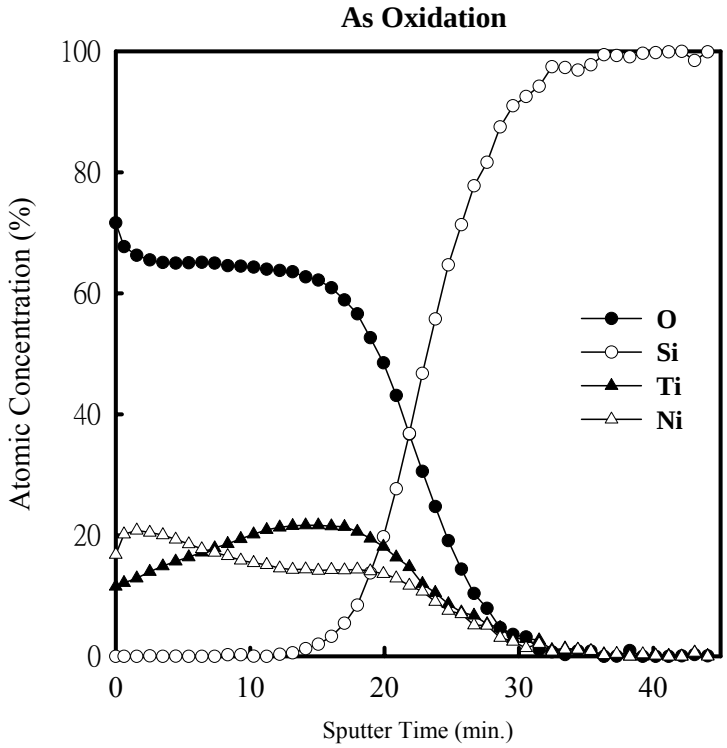


Fig.2.15 AES depth profile of the as-oxidation sample.

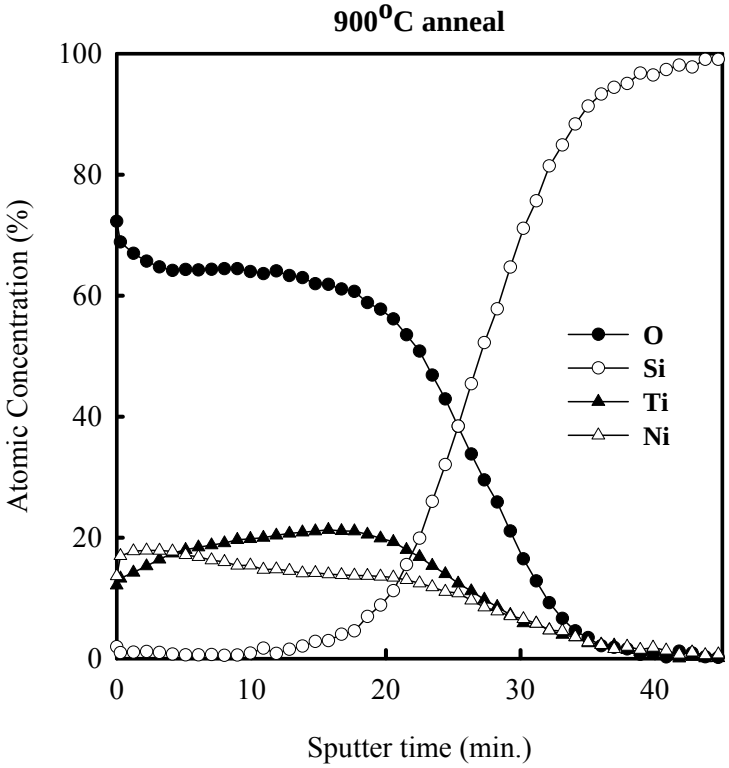


Fig.2.16 AES depth profile of the NiTiO with 900°C anneal.

Chapter 3

Characteristics of NiTiO Interpoly Dielectric by NH_3 Plasma Pre-oxidation treatment

3.1 Introduction

There are some reports show that oxidized the nitride metal such as ZrN or HfN to obtain ZrO_xN_y and HfO_xN_y. It reveals the improvement of thermal stability and retard crystallization [6]-[8]. From Chapter 2, Our NiTiO was formed by oxidized the Ni/Ti two metal stack structure. If we nitride the metal before oxidation, we believe it can obtain more reliable film after the oxidation process was carry out. In this work, the nitridation process using NH_3 plasma pre-oxidaiton treatment on Ni/Ti stack structure follow by thermal oxidation was used to fabricate the NiTiO film. We expect such process could improve electrical properties and the reliability of this film.

3.2 Experimental procedure

N+-polysilicon/NiTiO/TiN capacitors were fabricated on 6-inches <100> p-type wafer with resistivity of 5-10 Ω-cm. Fig.3.1 shows the process flow chart and cross section view for each main step. First, a 3000Å field oxide was thermal grown by wet oxidation at 800^{o}C to serve as isolation substrate. After 3000Å in-situ doped amorphous silicon deposited by LPCVD system, furnace annealing 800^{o}C 2 hours was used to turn it to poly silicon and activated the dopant.

Before metal deposition, NH_3 surface nitridation was used to grow a thin Si_3N_4 layer, as shown in Fig.3.1(a). Afterward, all samples were immediately deposited in

sequence with Ti (50 Å) and then Ni (50 Å) film from independent targets by using PVD method, as shown in Fig.3.1(b). Some of the sample use NH_3 plasma treatment to treat the two matal stack structure, as shown in Fig.3.1(c). The plasma condition are 20(W) 5(min.), 20(W) 10(min.), 40(W) 5(min.) and 40(W) 10(min.). Direct thermal oxidation was carried out at 800^{o}C in diluted O_2 (N_2/O_2=2/1) gas. Then 800^{o}C 60sec and 900^{o}C 60sec post oxidation annealing were used to investigate the thermal stability of NiTiO film with plasma treatment, as shown in Fig.3.1(d). 1500Å thick TiN metal gate was formed by sputter in 50% N_2 ambient (Ar:N_2=1:1). The gate regions were patterned by lithography and etched by ILD4100 metal etcher. Moreover, as shown in Fig.3.1(e), 3000Å SiO_2 film was deposited as passivation layer by PECVD system and contact hole was etched by dry etching. Finally, a 5000Å Al gate electrode was deposited by physical vapor deposition and defined the metal pad by ILD4100 metal etcher, as shown in Fig.3.1(f).

3.3 Results and Discussion

In this section, basic J-E characteristic, reliability analysis and material analysis were discussed here. HP4156 was used in all electrical measurement.

3.3.1 J-E Characteristic

Fig.3.2 and Fig.3.3 plot the positive and negative J-E characteristic of NiTiO under various annealing temperature with plasma treatment (PLOX) and without plasma treatment (OX), respectively. With plasma pre-oxidation treatment, as shown in Fig. 3.4 and 3.5, the low field leakage current will increase more than one half orders. According to someone's research, the band gap of NiTiO is 3.18(eV) [15]-[16]. We believe that schottky emission is one of the components in low field leakage current. Sample with NH_3 plasma pre-oxidation treatment will make the barrier height

lowing and this result in higher leakage current. Besides, sample with NH_3 plasma pre-oxidation treatment perform better thermal stability than those without NH_3 plasma pre-oxidation treatment. This phenomenon is more evident for negative gate bias. Fig.3.6 and Fig.3.7 show the delta leakage current at low electric field under various anneal temperature for positive and negative gate bias, respectively. we defines the delta leakage current as the following equation:

$$\text{Delta leakage current} = I_{\text{anneal}} - I_{\text{as-oxidation}}$$

With the increase of anneal temperature, the leakage current showed faster increase at that sample which is without NH_3 plasma pre-oxidation treatment. On the contrary, leakage current showed more stable at that sample which is with NH_3 plasma pre-oxidation treatment. Fig.3.8 and 3.9 show the weibull distribution of positive and negative gate bias leakage current density, respectively. These samples are under 900^{o}C anneal in RTA and these two plots is very easy to realize from above description. Fig.3.10 and 3.11 show the E_{BD} of positive and negative gate bias, under various post-oxidation anneal temperature. Each of the point was extracted from the 50% weibull plot. Sample with NH_3 plasma pre-oxidation treatment reveal higher E_{BD}. After post-oxidation anneal the E_{BD} will decrease for all samples.

3.3.2 Charge to Breakdown Characteristics

Fig.3.12 shows the charge to breakdown characteristic under stress current is 0.2mA/cm^2. Sample with NH_3 plasma pre-oxidation treatment can improve the Q_{BD} value from 0.006C/cm^2 to 0.06C/cm^2. After post anneal process, the Q_{BD} value will decrease to 0.01C/cm^2.

3.3.3 TDDB Characteristic

Fig.3.13 presents the TDDB characteristics. Fitting three points of the positive breakdown voltage for each sample draws the projected 10-year lifetime. Sample with NH_3 plasma pre-oxidation treatment can improve the ten years operation voltage from

2.05(V) to 3.4(V) for positive gate bias and from 3.2(V) to 4.6(V) for negative gate bias.

In Chapter 1, we describe the coupling ratio base on series capacitance model. Coupling ratio was defined as follow equation:

$$C.R. = \frac{Cc}{Cc + Ct}$$

Cc means the capacitance between control gate and floating gate and Ct means the capacitance between floating gate and substrate. If we divide C.R. by Cc, the C.R. will become as follow equation:

$$C.R. = \frac{1}{1 + \frac{Ct}{Cc}}$$

Table 3.1 gives a summary of our result. Coupling ratio was obtained from above equation. Ct/Cc is based on the assumption of the thickness of the tunnel oxide equal to 80Å and control gate area equal to the floating gate area. Ten years operation voltage is obtained from TDDB plot. $V_{dielectric}$ means the voltage which across the interpoly dielectric. It can be obtained from follow equation:

$$V_{dielectric} = V_{CG} \times (1 - C.R.)$$

V_{CG} means the voltage apply on control gate. We also assume NOR type flash W/E voltage is 10(V) and NAND type flash W/E voltage is 20(V). From this table, sample with NH_3 plasma pre-oxidation treatment can apply in NOR type flash memory.

3.3.4 AFM Surface Roughness Analysis

From Fig.3.14 to Fig.3.17 show the surface roughness of Ni/Ti stack structure with and without NH_3 plasma treatment. These results were summarized in Fig.3.21 and we observed that even increase the plasma power or the time of plasma treatment, the roughness of the metal surface has no significant change. However, after oxidation, as shown in Fig.3.18~3.20, samples with NH_3 plasma pre-oxidation treatment reveals

smaller surface roughness than those without NH_3 plasma pre-oxidation treatment. These results were summarized in Figure 3.22. We will give a possible reason in following article.

Metal is a composite of many grains in a microcosm, like poly-Si, it also have grain boundary between grain and grain. When we treat metal by NH_3 plasma, nitrogen will incorporated into metal film. When we raised the temperature, we believed that nitrogen will segregate to grain boundary. As shown in Figure 3.23 and 3.24, in the oxidation step, sample without plasma treatment exhibits different oxidation velocity between grain and grain boundary. Grain boundaries are oxidized more rapidly than the center of the grains. In contrast, if nitrogen segregates to the grain boundary, its oxidation speed will be retarded. So, sample with NH_3 plasma treatment have more uniform oxidation speed and this will result in smoother surface roughness. We believe that the smoother surface roughness and nitrogen incorporation play an important role in the improvement of those electrical properties.

3.3.5 Effective Oxide Thickness

Fig.3.25 (a) shows the effective oxide thickness with and without NH_3 plasma treatment under various post anneal temperature. With the increase of the post-oxidation anneal temperature, the EOT will decrease. From TEM image, the physical thickness in all samples is nearly the same. Therefore, we conclude that post anneal process will increase the dielectric permittivity (K value) of this thin film. Moreover, samples with NH_3 plasma pre-oxidation treatment show larger EOT than those without plasma treatment. We think that there are two possible reasons. One is that samples with plasma treatment have lower K value than those without plasma treatment [17].

Another is about the surface roughness. Fig.3.25 (b) shows the sketch map with and without NH_3 plasma pre-oxidation treatment. The increase of surface roughness

also means that it have larger effective area under the same square measure. The capacitance is proportional to the area, larger area result in larger capacitance which will be measured. EOT is inverse proportional to the value of capacitance. So, the rougher of the surface reveals the lower EOT.

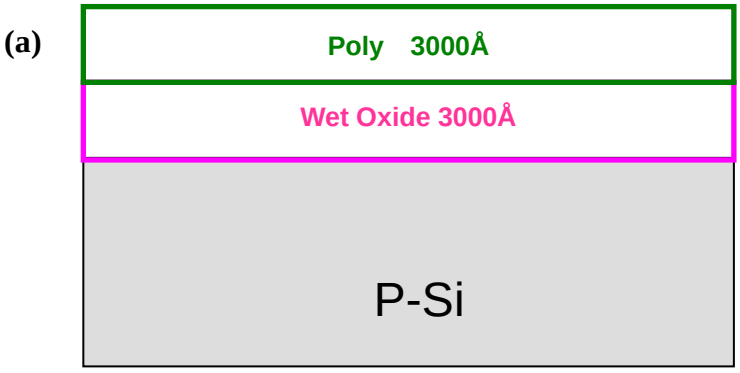
3.3.6 TEM Image

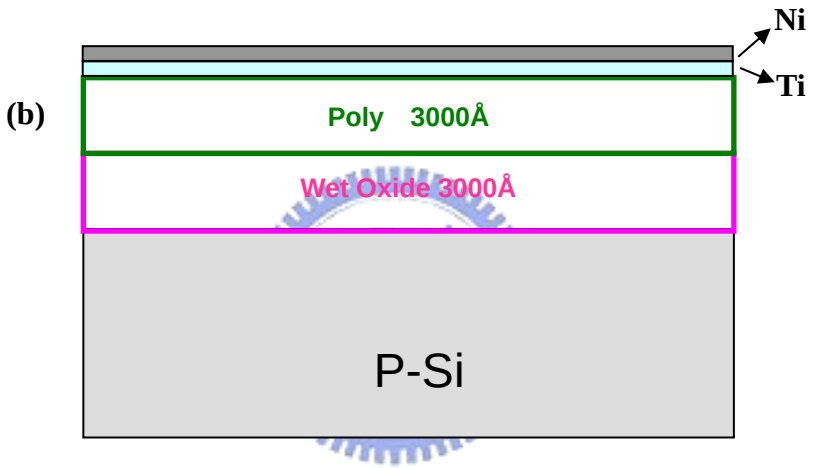
Fig.3.26 and Fig.3.27 show the TEM images. All of the samples have the same physical thickness 200Å. Even after 900^{o}C 60 sec anneal, physical thickness of the interfacial layer still unchanged. Compare with Chapter 2 (Fig.2.13 and Fig.2.14), after NH_3 plasma pre-oxidation treatment, there is less agglomeration in the NiTiO thin film.

3.4 Summary

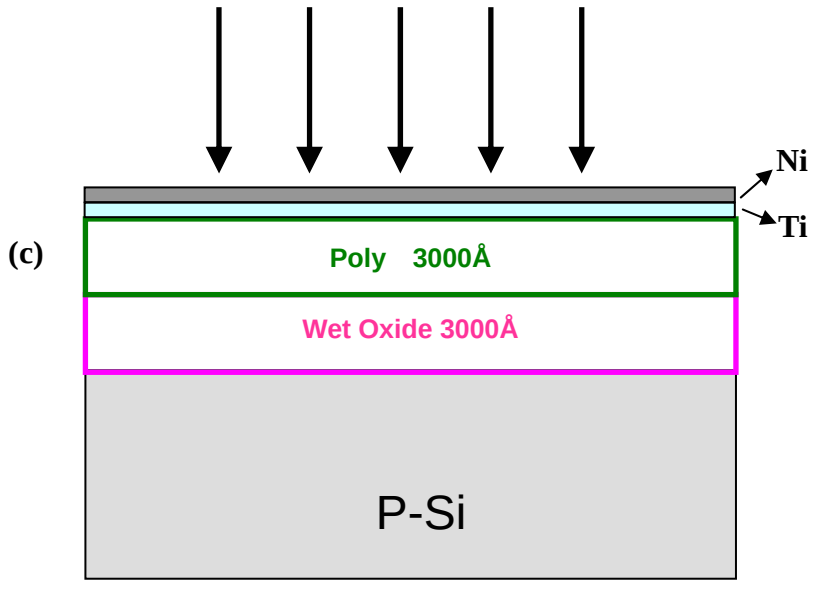
In this chapter, we first time use NH_3 plasma pre-oxidation treatment on NiTiO films. By using this process, electrical properties and the reliability of NiTiO can be improved. After NH_3 plasma pre-oxidation treatment, NiTiO reveals potential for NOR type flash application.

Pure NH_3 surface nitridation





NH_3 plasma treatment



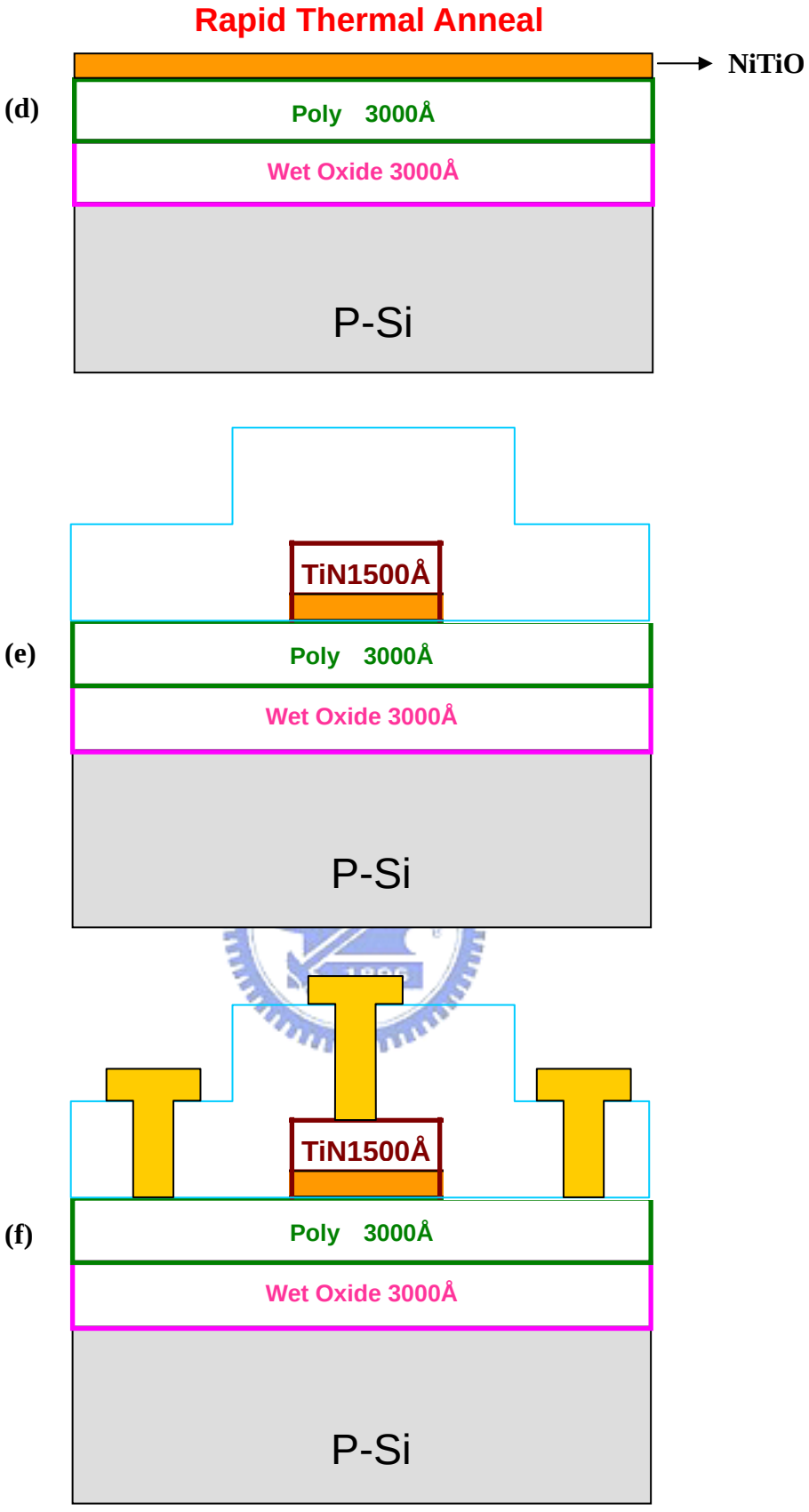


Fig.3.1 TiN/NiTiO/poly-Si capacitor fabrication process flow which include (a) pure NH_3 surface nitridation (b) Ni/Ti deposited by PVD (c) NH_3 plasma pre-oxidation treatment (d) rapid thermal anneal (e) passivation oxide deposited by PECVD (f) after contact hole etched and metal pad defined and etched,the final structure was finished.

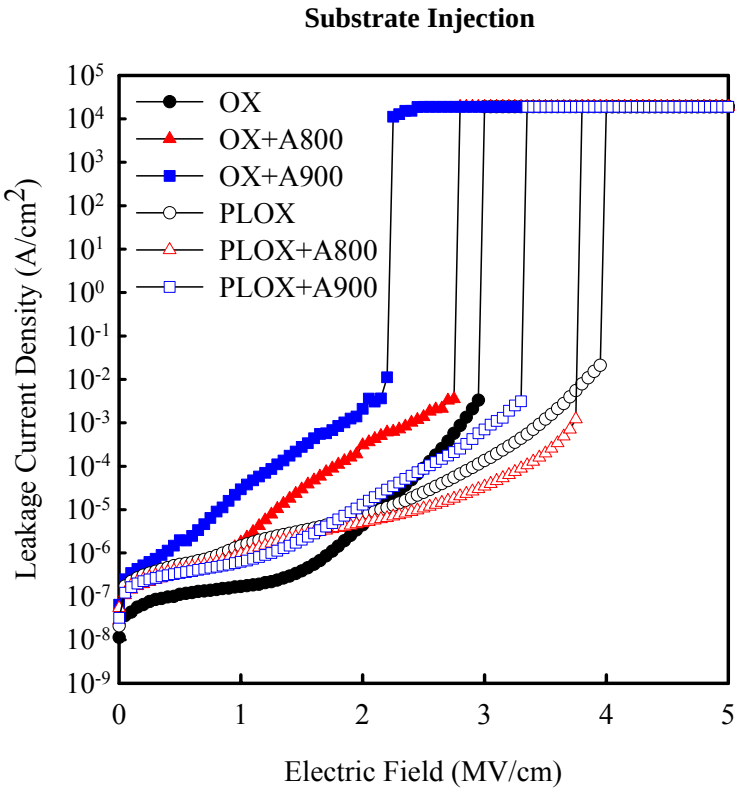


Fig.3.2 Positive gate bias J-E characteristic of NiTiO under various anneal temperature with plasma treatment (PLOX) and without plasma treatment (OX).

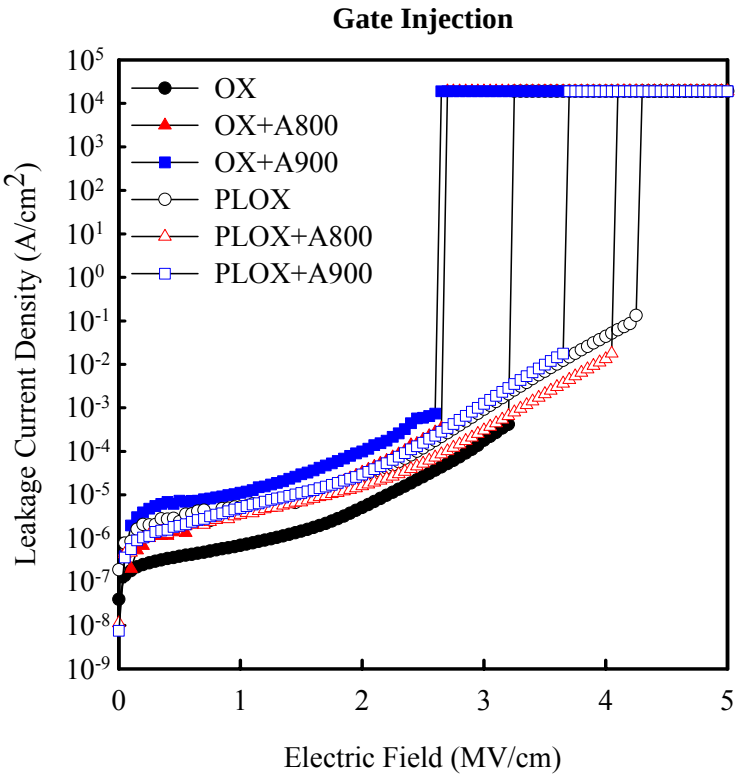


Fig.3.3 Negative gate bias J-E characteristic of NiTiO under various anneal temperature with plasma treatment (PLOX) and without plasma treatment (OX).

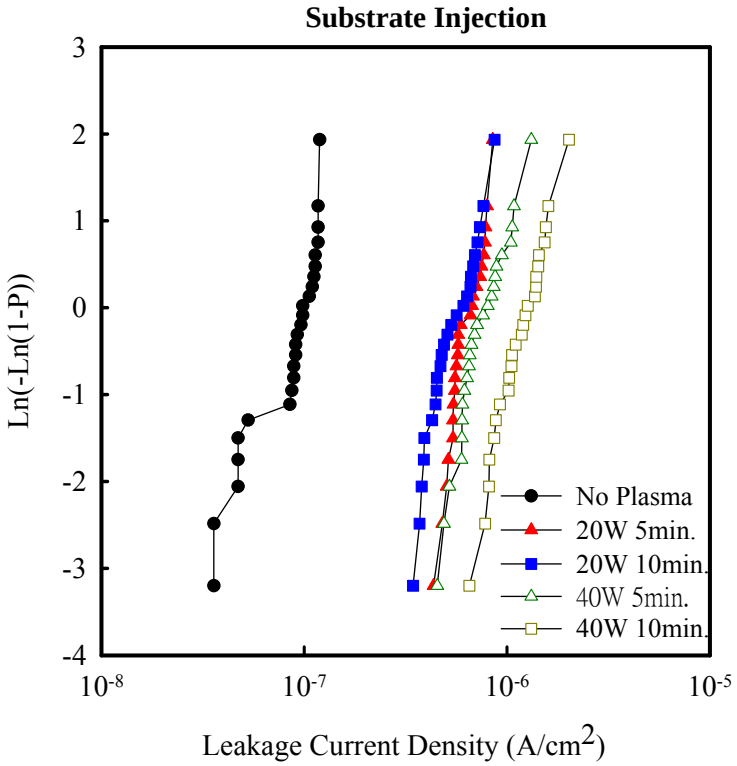


Fig.3.4 Weibull distribution of leakage current density at Vg =+1V, these samples aren't annealing in RTA.

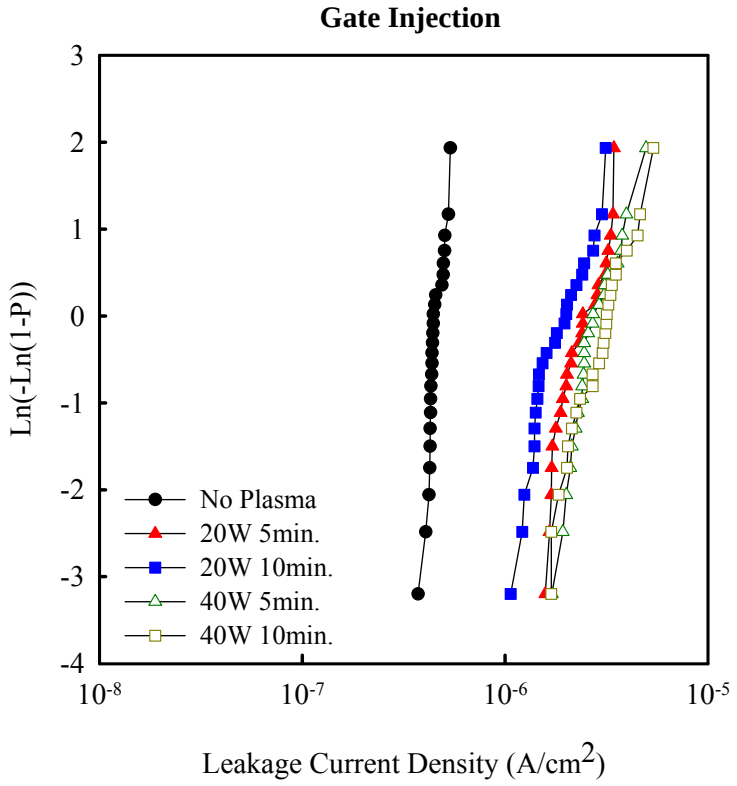


Fig.3.5 Weibull distribution of leakage current density at Vg = -1V, these samples aren't annealing in RTA.

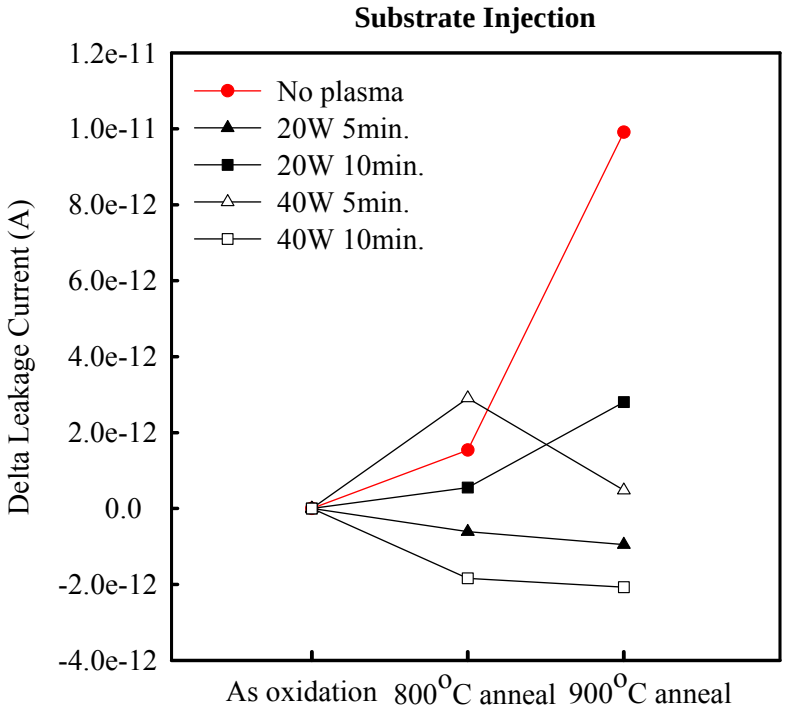


Fig.3.6 Delta leakage current under various anneal temperature at Vg = +1V. Delta leakage current = $I_{anneal} - I_{as\text{-}oxidation}$.

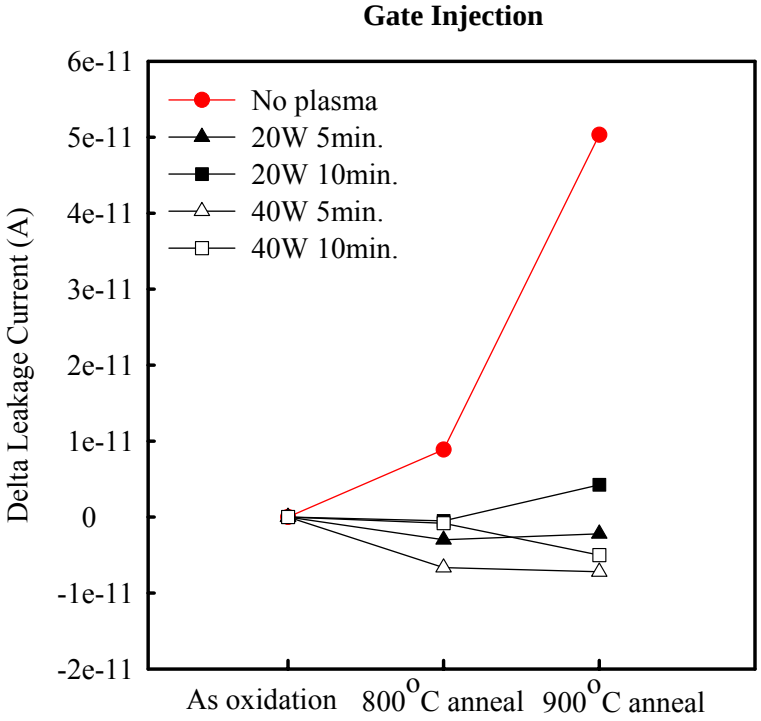


Fig.3.7 Delta leakage current under various anneal temperature at Vg = -1V. Delta leakage current = $I_{anneal} - I_{as\text{-}oxidation}$.

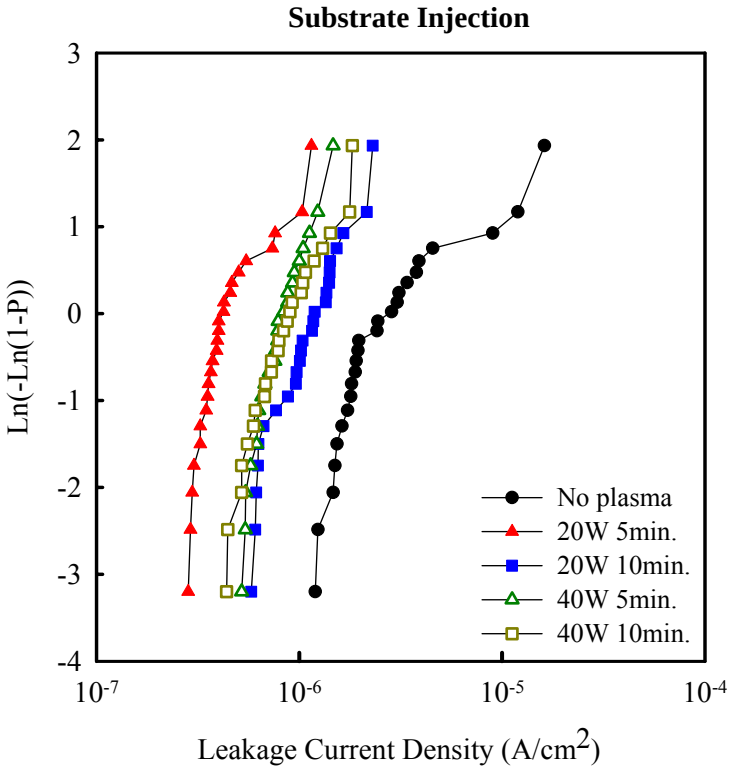


Fig.3.8 Weibull distribution of leakage current density at Vg =+1V, these samples under 900°C anneal in RTA.

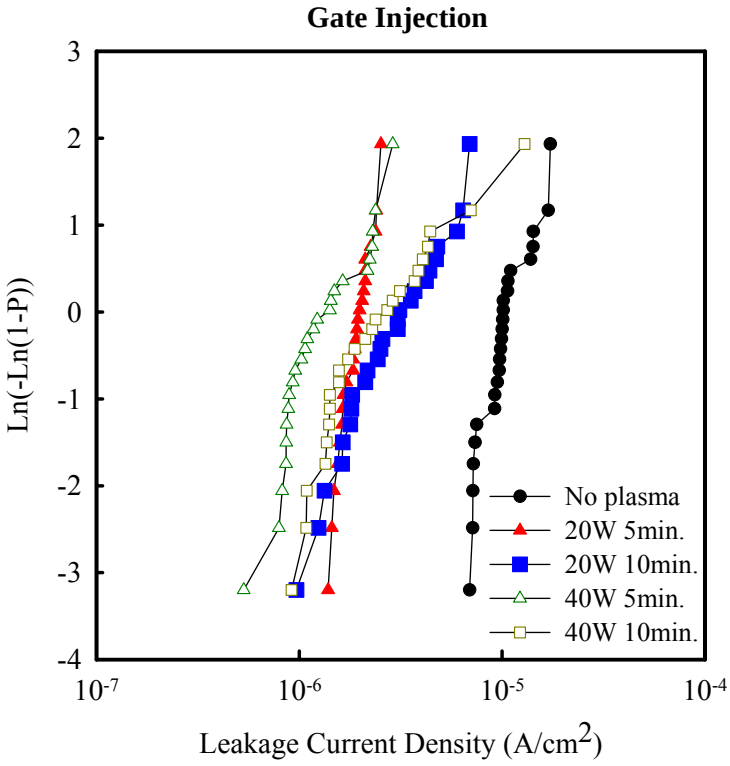


Fig.3.9 Weibull distribution of leakage current density at Vg = -1V, these samples under 900°C anneal in RTA.

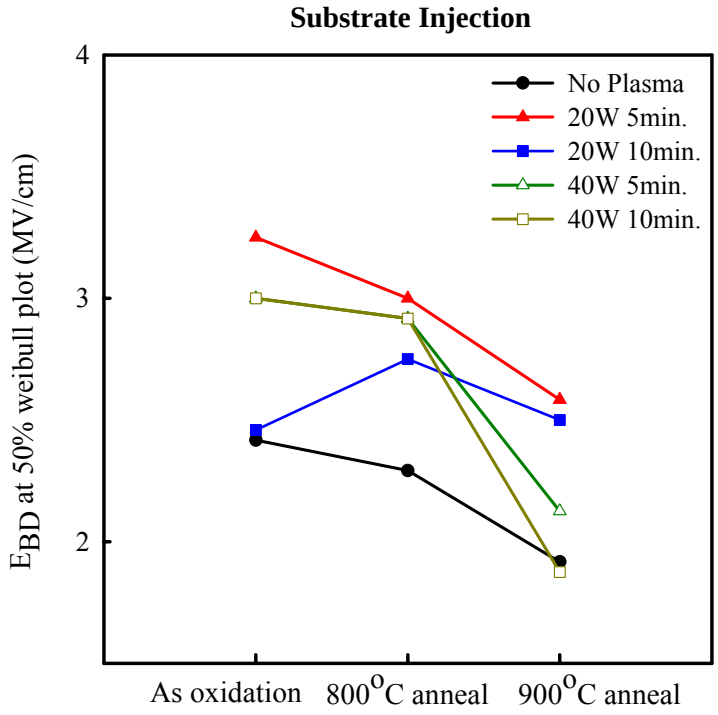


Fig.3.10 E_{BD} under various anneal temperature for positive gate bias.

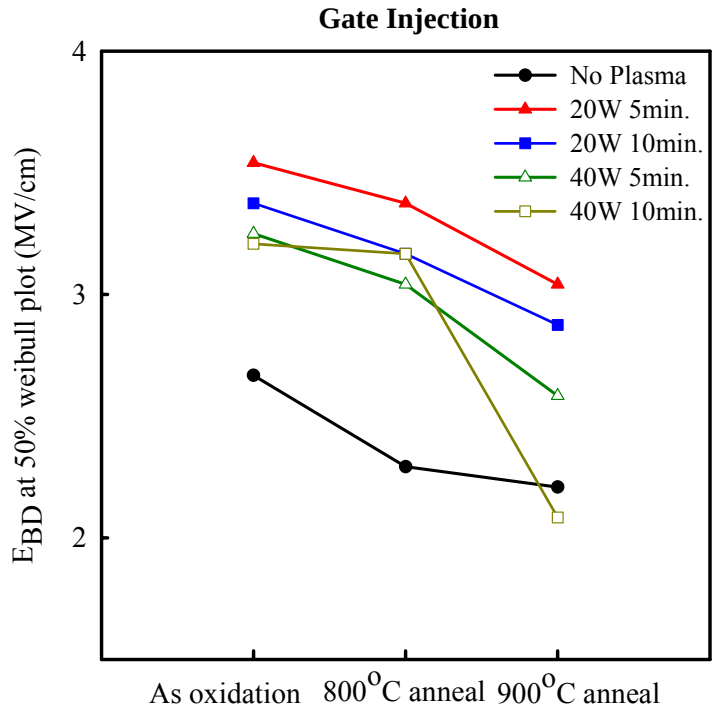


Fig.3.11 E_{BD} under various anneal temperature for negative gate bias.

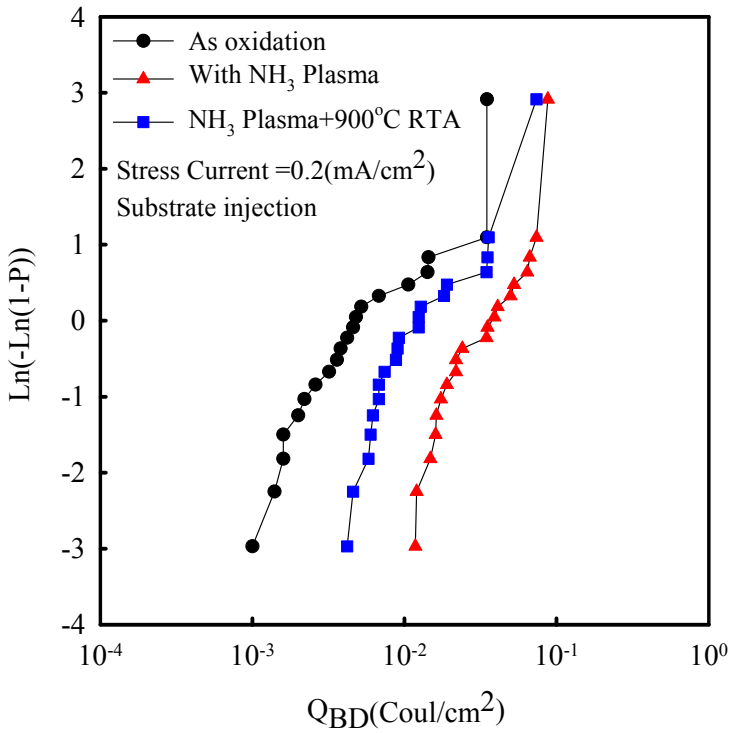


Fig.3.12 Charge to breakdown characteristic under positive gate bias.

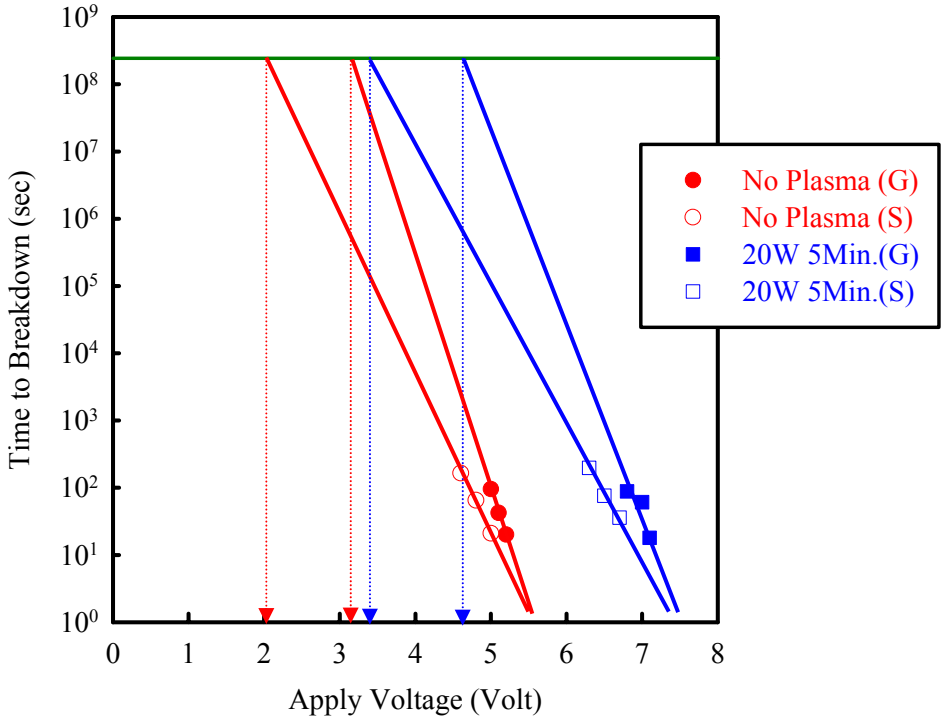


Fig.3.13 TDDB characteristic under positive gate bias.

Table 3.1 summary of our result, Ct/Cc is base on the assumption of the thickness of the tunnel oxide equal to 80Å and control gate area equal to the floating gate area. Ten years operation voltage is obtained from TDDB plot. $V_{interpoly}$ means the voltage which across the interpoly dielectric. We also assume NOR type flash W/E voltage is 10V and NAND type flash W/E

CONDITION / PARAMETER	OX	PLOX
EOT(Å)	35.1	37.5
Effective K value	22.2	20.8
Ct/Cc	0.438	0.468
Coupling Ratio	0.695	0.680
Ten years operation voltage(Volt)	2.05	3.4
$V_{Interpoly}$ (Volt) (NOR 10V)	3.05	3.19
Pass or Fail	Fail	Pass
$V_{Interpoly}$ (Volt) (NAND 20V)	6.1	6.3
Pass or Fail	Fail	Fail

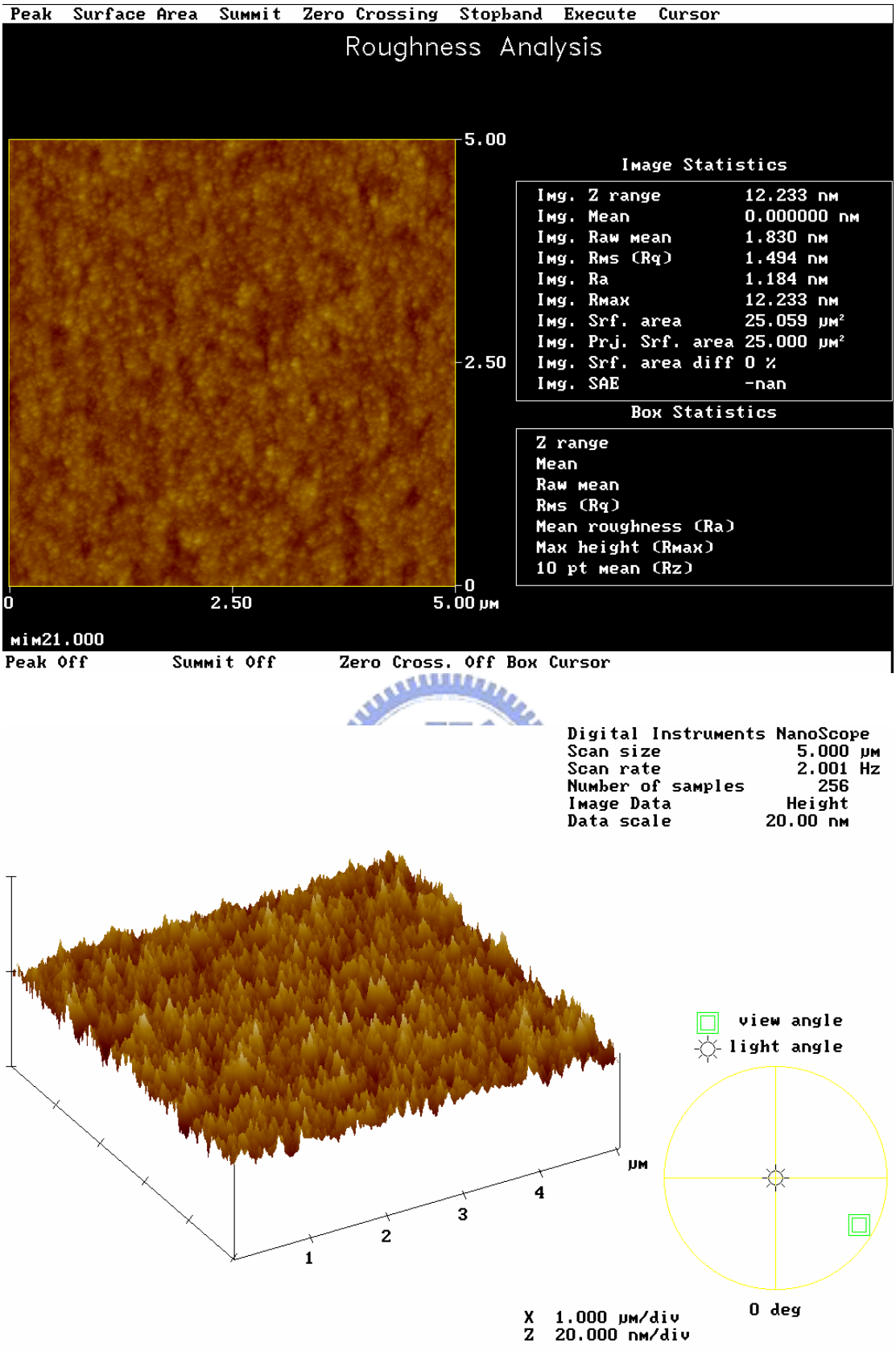


Fig.3.14 Surface roughness of Ni/Ti stack structure without NH_3 plasma treatment.

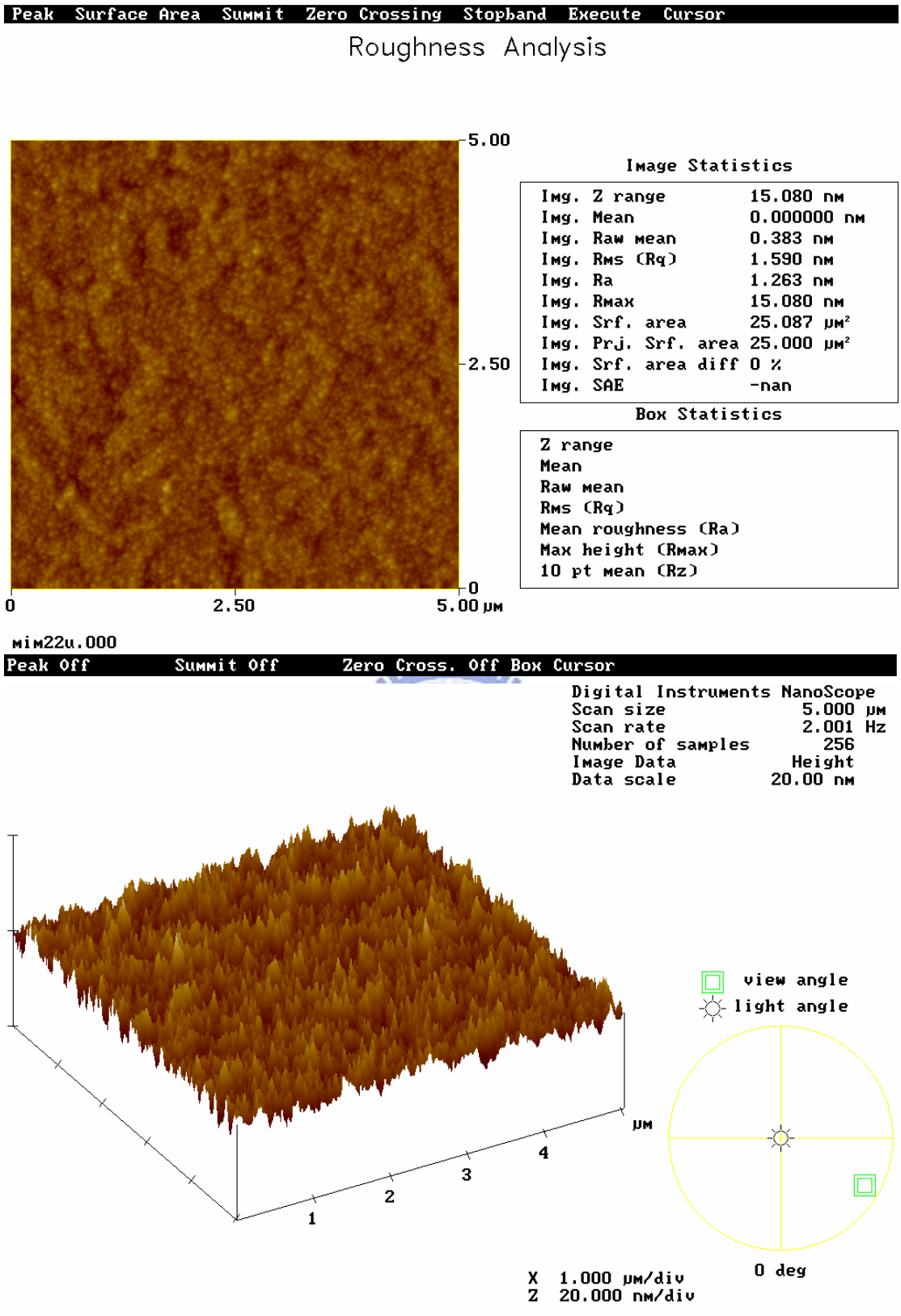


Fig.3.15 Surface roughness of Ni/Ti stack structure with 20Watts 5 minutes NH_3 plasma treatment.

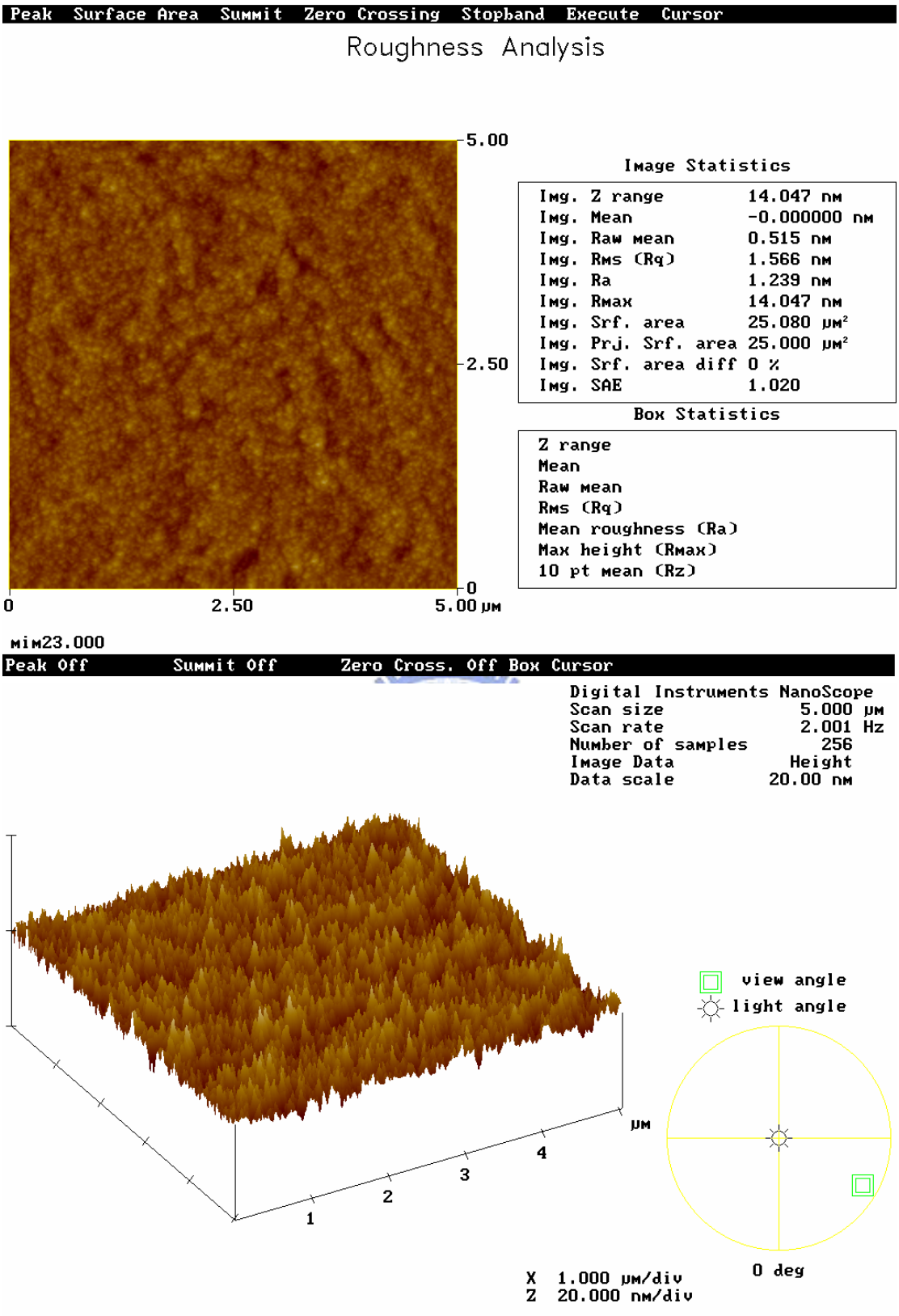


Fig.3.16 Surface roughness of Ni/Ti stack structure with 20Watts 10 minutes NH_3 plasma treatment.

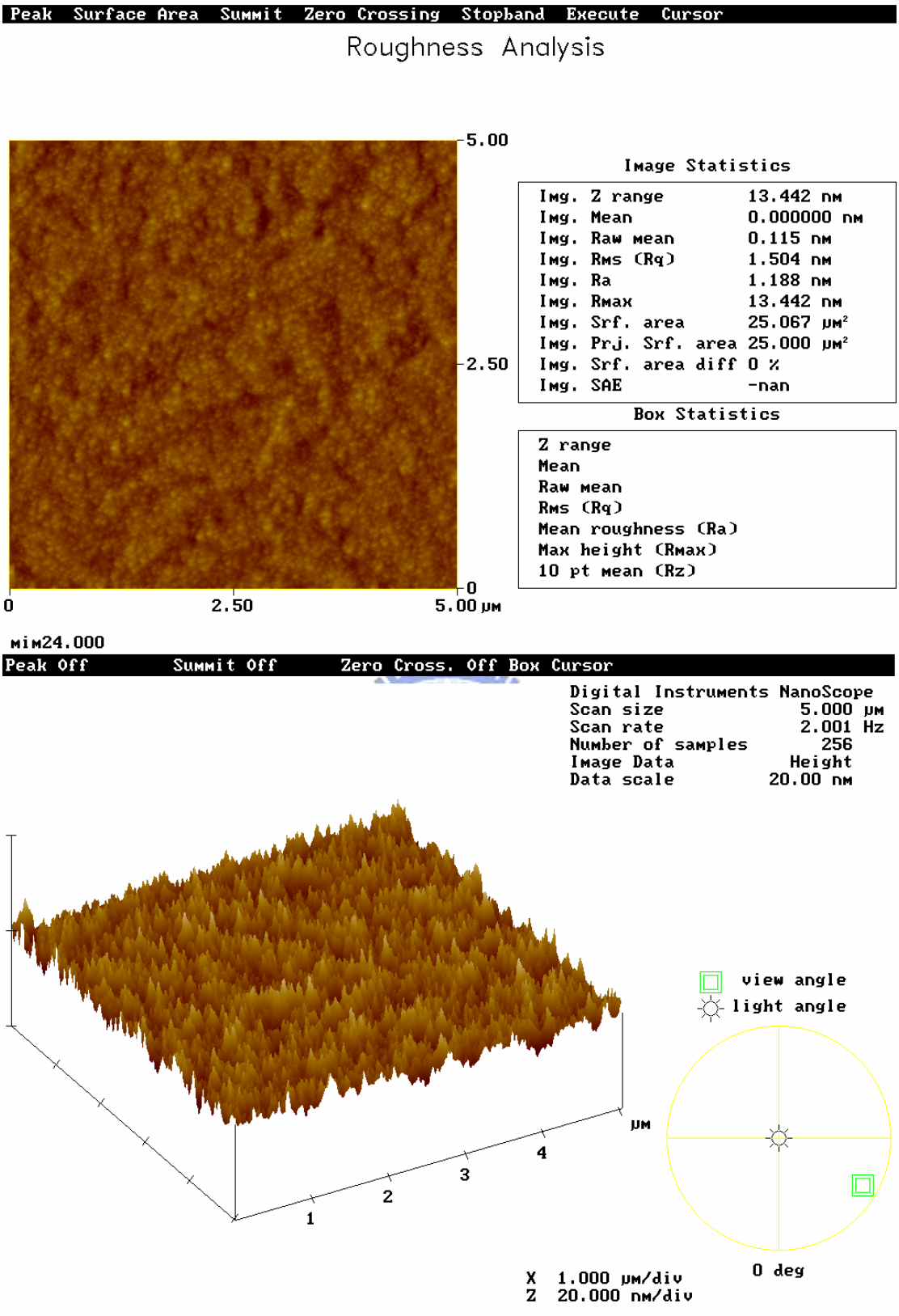
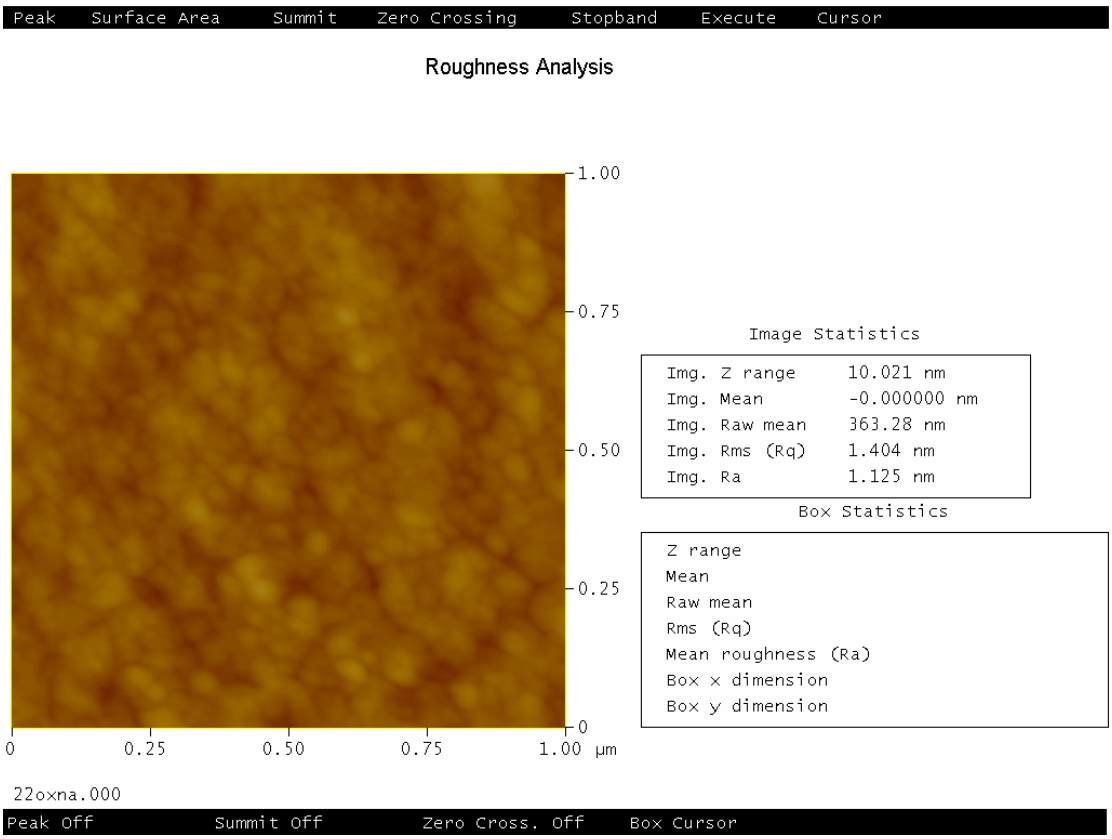


Fig.3.17 Surface roughness of Ni/Ti stack structure with 40W 5 minutes NH_3 plasma treatment.



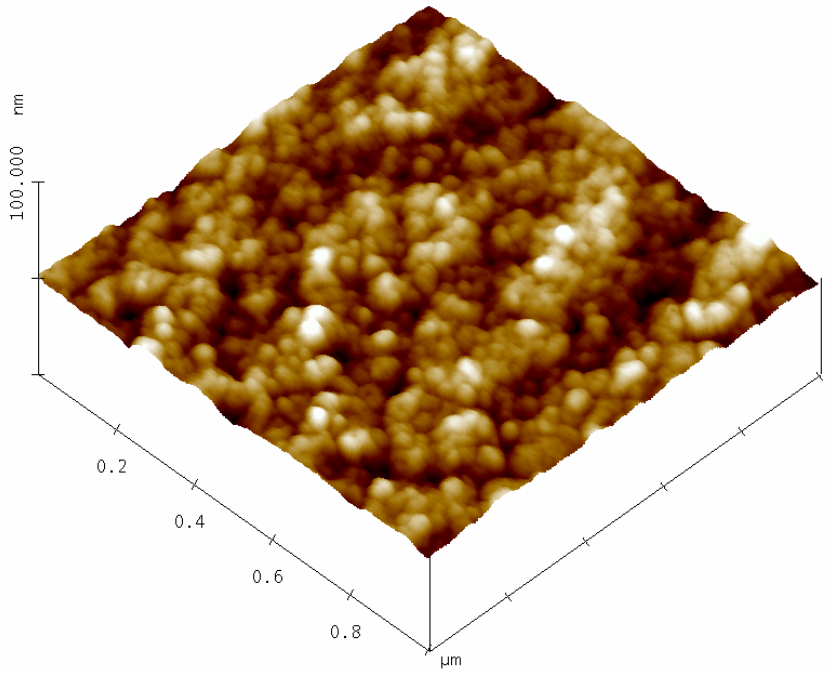


Fig.3.18 Surface roughness of NiTiO with 20Watts 5 minutes NH_3 plasma pre-oxidation treatment.

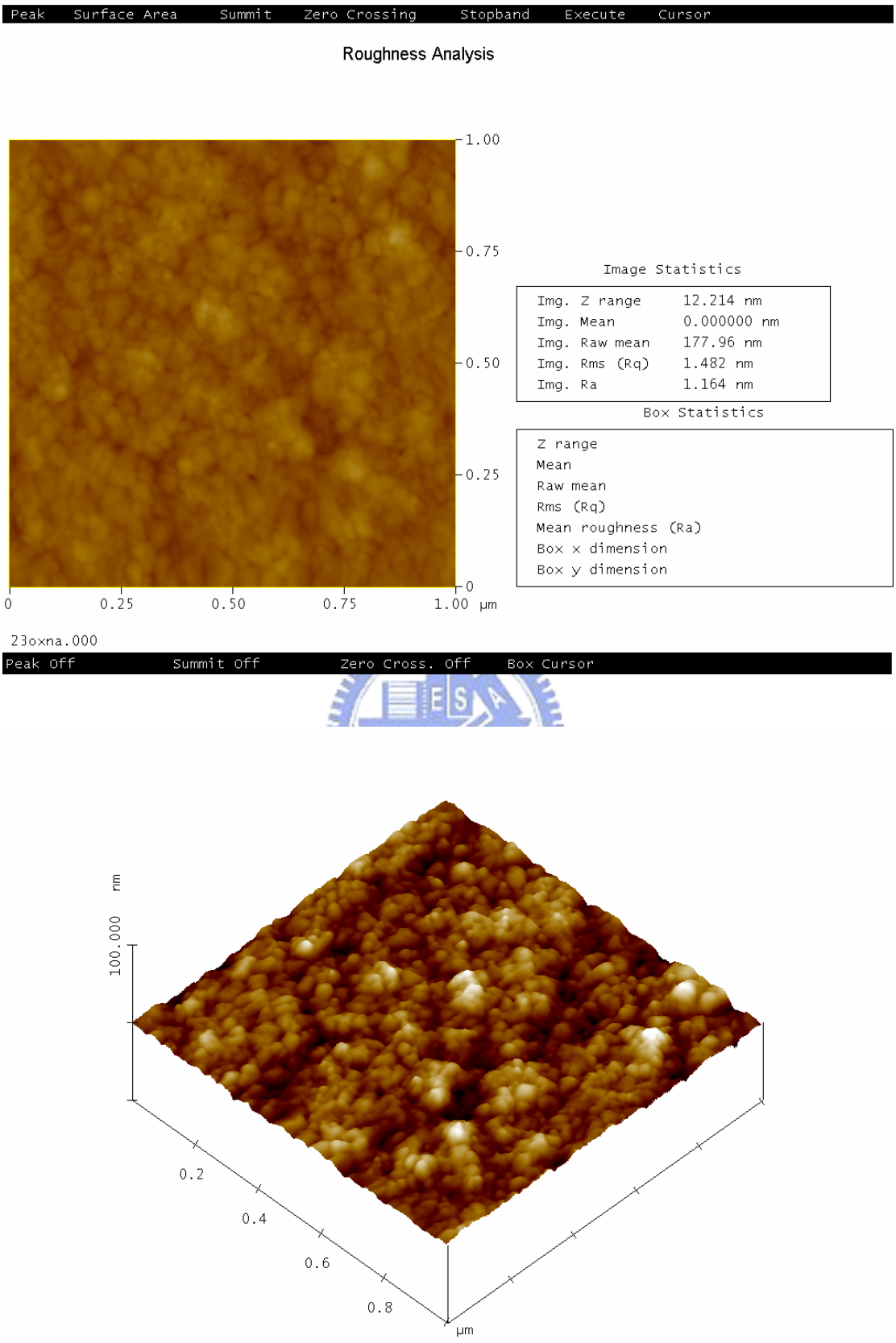


Fig.3.19 Surface roughness of the NiTiO with 20Watts 10 minutes NH_3 plasma pre-oxidation treatment.

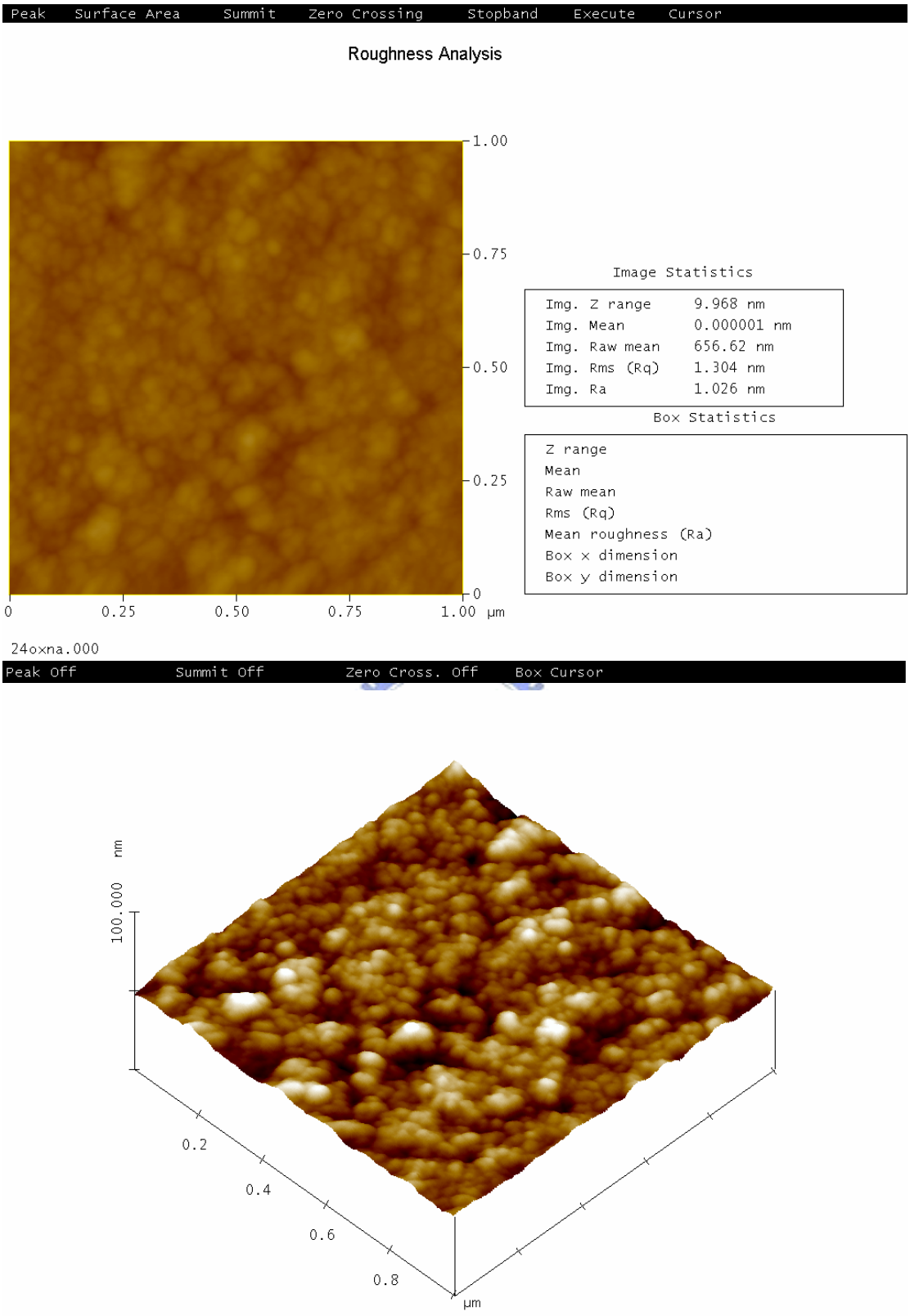


Fig.3.20 Surface roughness of the NiTiO with 40Watts 5 minutes NH_3 plasma pre-oxidation treatment.

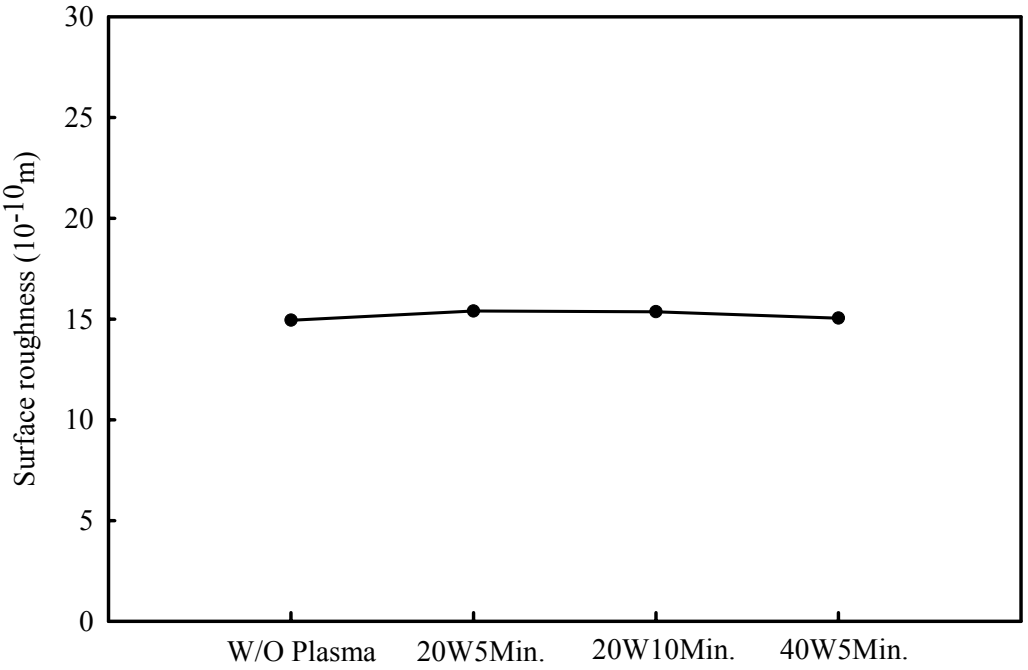


Fig.3.21 Summary of the surface roughness from Fig.3.14 to Fig.3.17 .

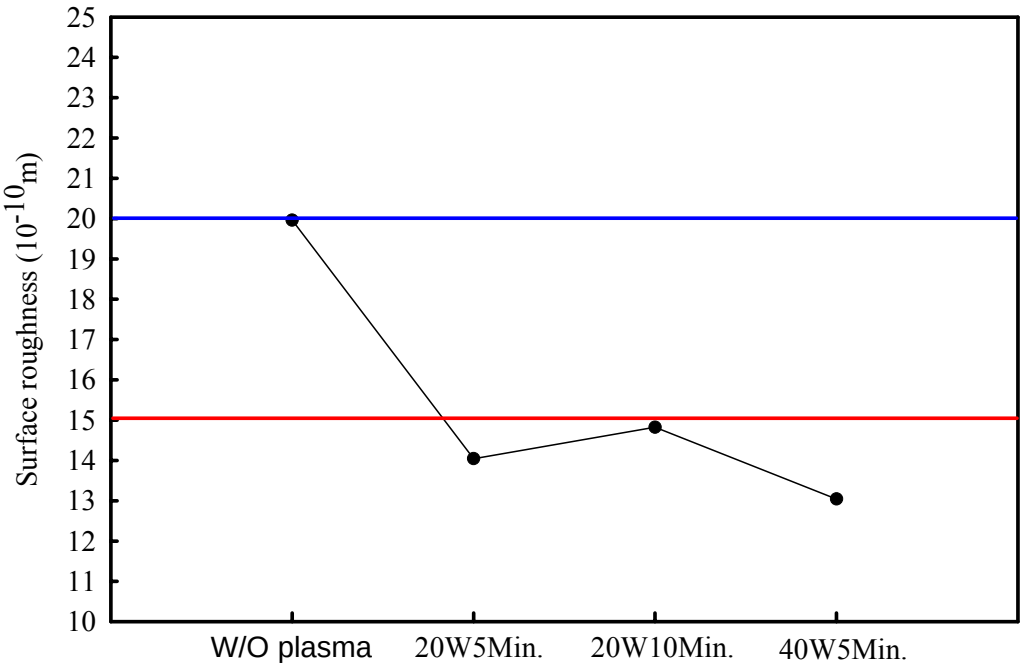


Fig.3.22 Surface roughness of the NiTiO with and without NH_3 plasma pre-oxidation treatment.

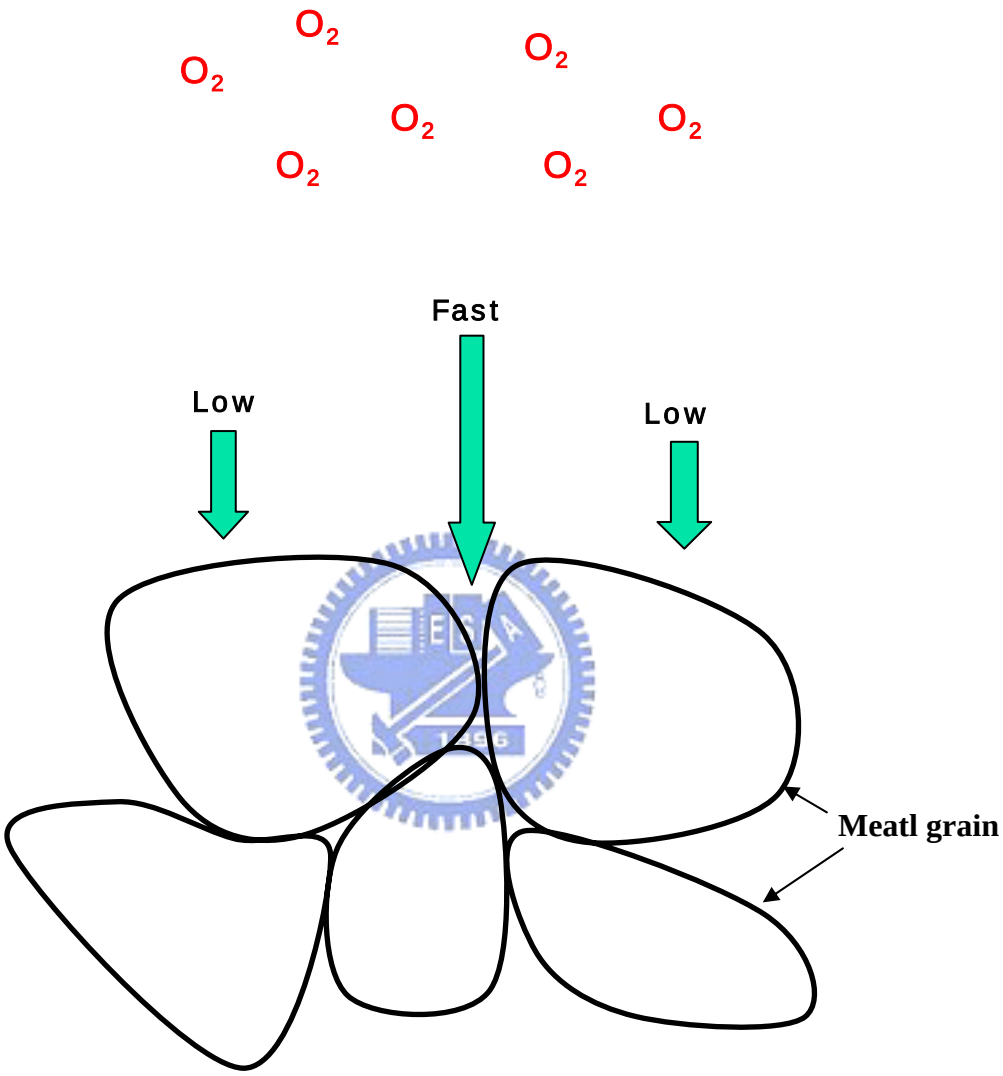


Fig.3.23 A sketch map of metal oxidation without NH_3.plasma pre-oxidation treatment. The length of the arrow means the oxidation speed.

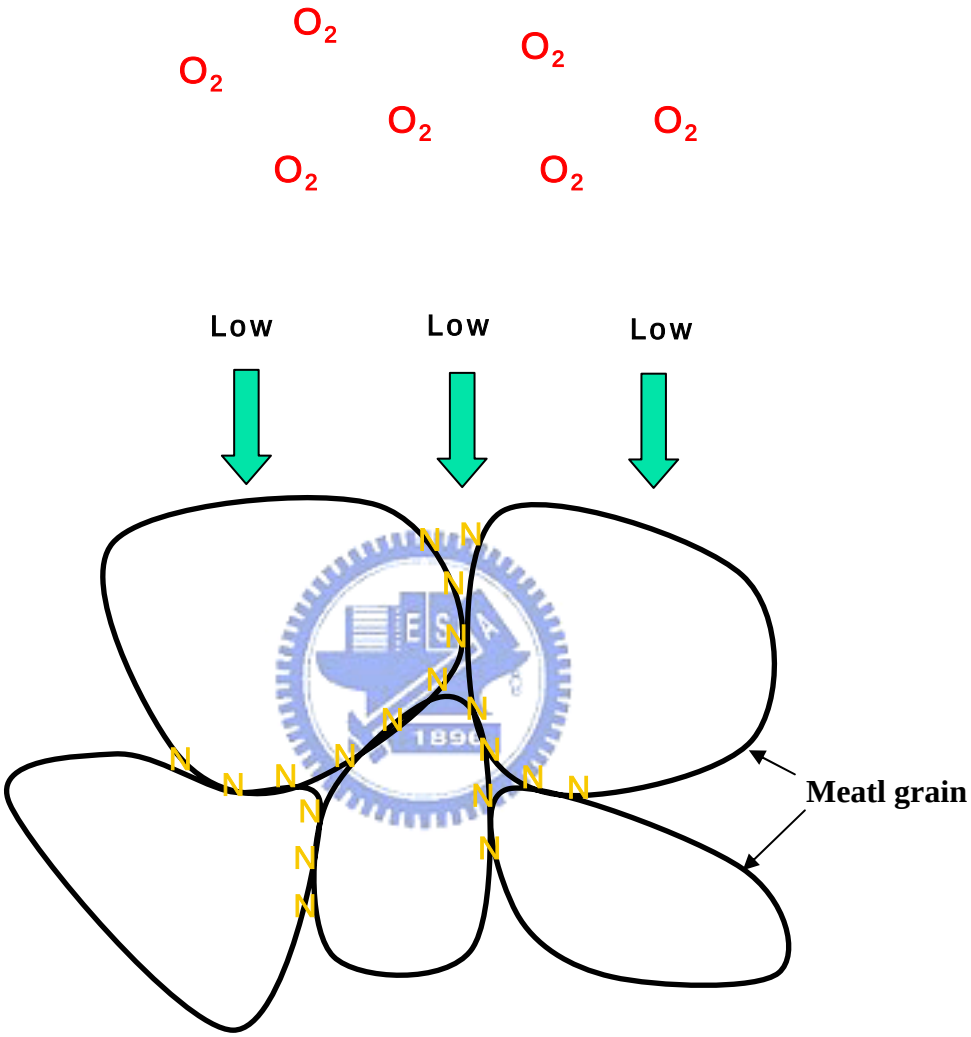


Fig.3.24 A sketch map of metal oxidation with NH_3.plasma pre-oxidation treatment. The length of the arrow means the oxidation speed.

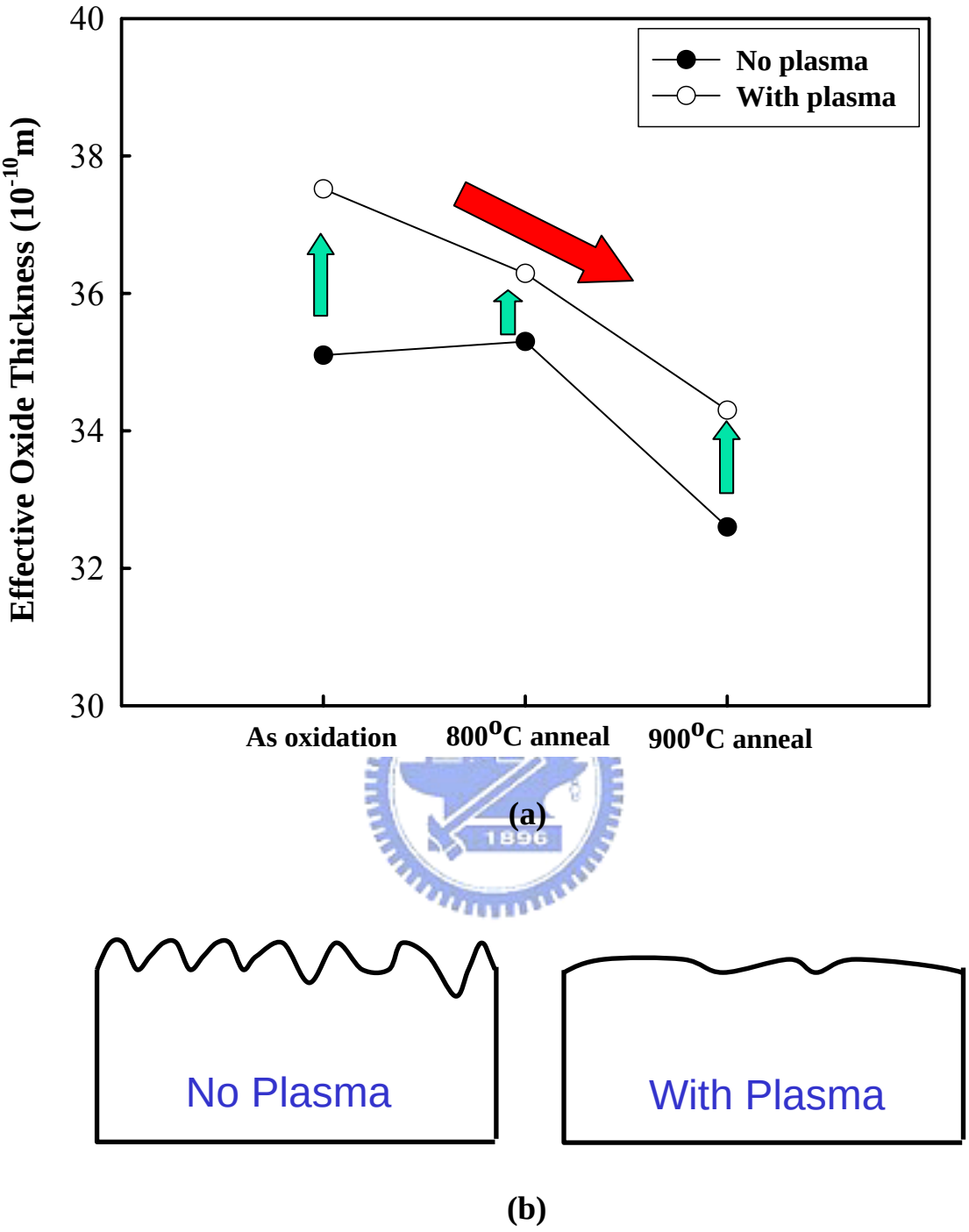


Fig.3.25 (a) The relation of EOT with the temperature of post-oxidation anneal (b) surface roughness sketch map with and without NH_3 plasma treatment.

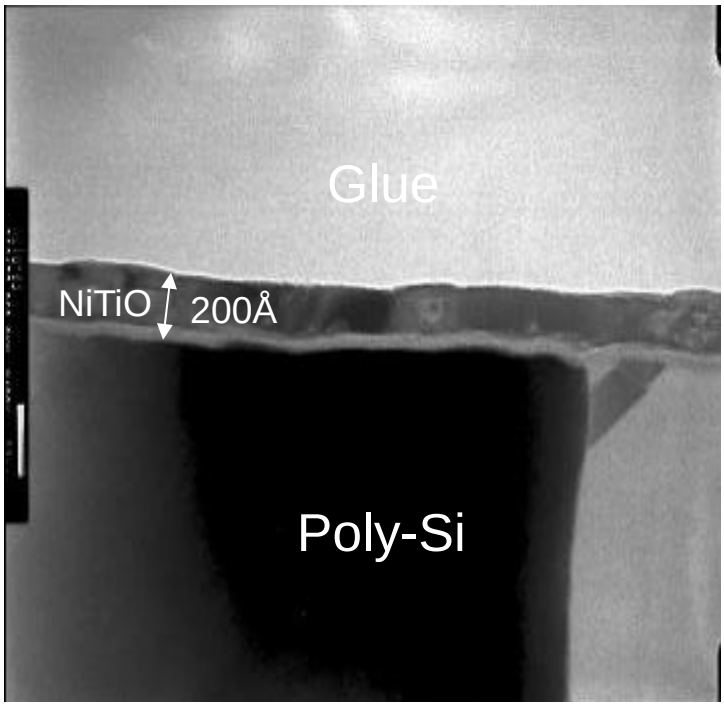


Fig.3.26 TEM image of the sample with NH_3 plasma treatment.

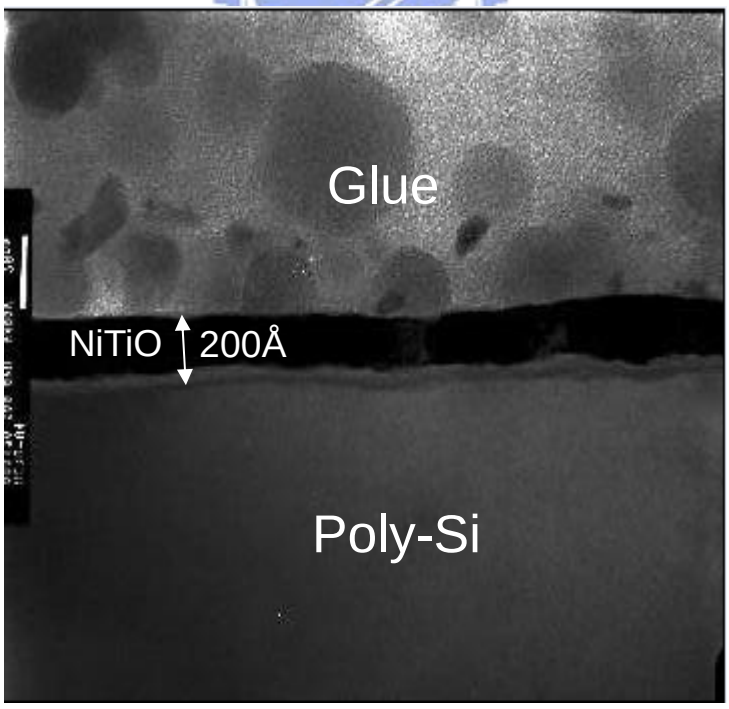


Fig.3.27 TEM image of the sample with NH_3 plasma + 900^{o}C post-oxidation anneal.

Chapter 4

Comparsion CoTiO Interpoly Dielectric between NH_3/N_2O Plasma Pre-Oxidation Treatment and NH_3/N_2O Plasma Post-Oxidation Treatment

4.1 Introduction

From Chapter 3, we show that NH_3 plasma pre-oxidation treatment is useful to improve the NiTiO electrical properties. From the reports of Pan et al. CoTiO has higher effective K value and better electrical properties than NiTiO [9]. Wang et al. say that NH_3 and N_2O plasma post deposition anneal also improve electrical properties of high-k film on the single crystal silicon [18]-[20]. So, in this chapter, we use NH_3 and N_2O plasma to treat CoTiO film on the poly-Si and compare the method of plasma treatment between pre-oxidation treatment and post-oxidation treatment.

4.2 Experimental procedure

N+-polysilicon/CoTiO/TiN capacitors were fabricated on 6-inches <100> p-type wafer with resistivity of 5-10 Ω-cm. Fig.4.1 shows the process flow chart and cross section view for each main step. First, a 300nm field oxide was thermal grown by wet oxidation at 800^{o}C to serve as quartz substrate. After 300nm in-situ doped amorphous silicon deposited by LPCVD system, furnace annealing 800^{o}C 2 hours was used to turn it to poly silicon and activate the dopant.

Before metal deposition, NH_3 surface nitridation was used to grow a thin Si_3N_4 layer, as shown in Fig.4.1 (a). Afterward, all samples were immediately deposited in

sequence with Ti (50 Å) and then Co (50 Å) film from independent targets by using PVD method, as shown in Fig.4.1 (b). Some of the sample use NH_3 or N_2O plasma treatment to treat the two matal stack structures, as shown in Fig.4.1(c). NH_3 or N_2O plasma recipe is 20W 5 minites which is the best recipe we obtain from chapter 3. Direct thermal oxidation was carried out at 800^oC in diluted O_2 (N_2/O_2=2/1) gas. Then NH_3 or N_2O plasma post-oxidation treatment was used to treat the CoTiO film, plasma recipe is 20W 5 minites, as shown in Fig.4.1 (d). 150nm thick TiN metal gate was formed by sputter in 50% N_2 ambient (Ar:N_2=1:1). The gate regions were patterned by lithography and etched by ILD4100 metal etcher. Moreover, as shown in Fig.4.1 (e), 300nm SiO_2 film was deposited as passivation layer by PECVD system and contact hole was etched by dry etching. Finally, a 500nm Al gate electrode was deposited by physical vapor deposition and defined the metal pad by ILD4100 metal etcher, as shown in Fig.4.1 (f).

4.3 Results and Discussion

In this section, basic J-E characteristic, reliability analysis and TEM image was discussed here. HP4156 was used in all electrical measurement.

4.3.1 J-E Characteristic

Fig.4.2 and Fig.4.3 present the J-E characteristic under positive gate bias and negative gate bias, respectively. Sample with N_2O and NH_3 plasma pre-oxidation treatment (N_2O+OX and NH_3+OX) have higher breakdown electric field. Low field leakage current density is nearly the same, as shown in Fig.4.4 and Fig.4.5. Only slight higher leakage current for sample with pre-oxidation treatment.This phenomenon is quiet different from NiTiO sample which was shown in Chapter 3. This may due to samples with pre-oxidation treatment have a little lower effective barrier height but the amount of the barrier lowering is samller than the sample of

NiTiO. Fig.4.6 and Fig.4.7 show the weibull plot of breakdown electric field under positive gate bias and negative gate bias, respectively. Samples with pre-oxidation treatment have E_{BD} more than 5.5MV/cm. E_{BD} reveals 2MV/cm improvement was gained. EOT versus various plasma treatment methods was shown in Fig.4.8. Samples under pre-oxidation treatment have larger EOT than those samples with post-oxidation treatment. This result is the same with the NiTiO which we discussed in chapter 3.

4.3.2 Charge to Breakdown Characteristics

Fig.4.9 plots the weibull distribution of charge to breakdown value under stress current density 1mA/cm^2. By using NH_3 or N_2O plasma pre-oxidation treatment, Q_{BD} was improved from 0.12C/cm^2 to 0.6C/cm^2. In addition, we also observe that post-oxidation treatment (OX+N_2O and OX+NH_3) will degrade the Q_{BD} value.

4.3.3 TDDB Characteristics

Fig.4.10 plots the TDDB characteristics with various plasma treatment methods. Samples with pre-oxidation treatment have larger ten years operation voltage than those post-oxidation treatments. Compare with the N_2O plasma and the NH_3 plasma pre-oxidation treatment, N_2O plasma is more reliable than NH_3 plasma. Using the method we bring up in Chapter 3, the summary of our result was described in Table 4.1.For NOR type flash, all of the sample are passing except for N_2O plasma post-oxidation treatment. For NAND type flashes, only for the samples with pre-oxidation treatment are usable. We think that there are two possible reasons result in the reliability degradation for samples with post-oxidation treatment. One is post-oxidation treatment generate some plasma damages and after plasma treatment, there is no high temperature process to repair these damages. Another is the post-oxidation treatment inject more hydrogen (by NH_3 plasma) or oxygen (by N_2O

plasma) result in the reliability degradation.

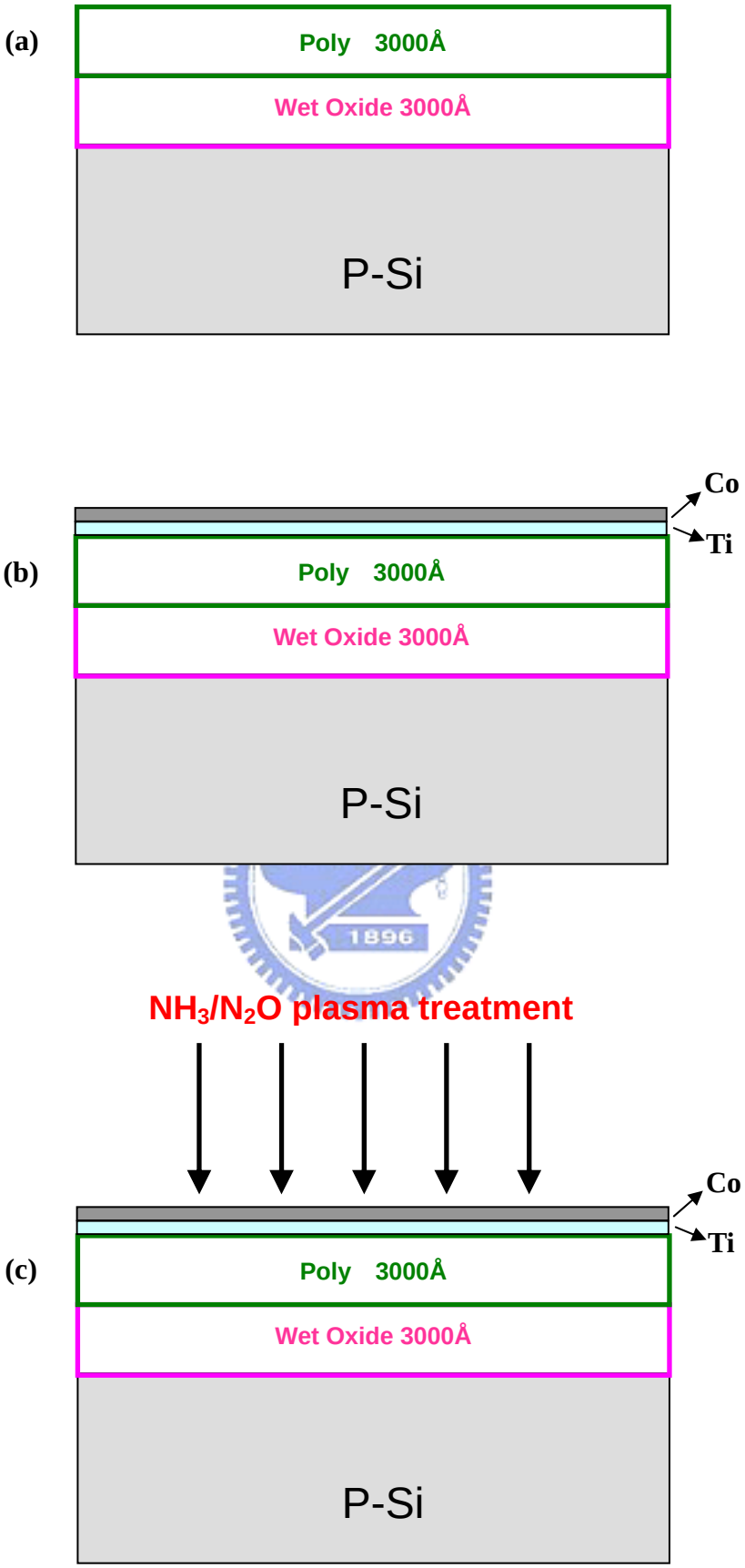
4.3.4 TEM Image

Figure 4.11-14 show the TEM images of the as-oxidation and sample with NH_3 plasma pre-oxidation treatment, N_2O plasma pre-oxidation treatment and N_2O plasma post oxidation treatment, respectively. Physical thickness of all these samples is roughly equal to 250Å. Sample with N_2O plasma pre-oxidation treatment have thicker interfacial layer than others, this is maybe one of the reasons for it reveal larger EOT.

4.5 Summary

In this chapter, basic characteristic of CoTiO on poly-Si was presented, and we also compare the pre-oxidation treatment with post oxidation treatment. E_{BD} of CoTiO on poly Si is 3.3MV/cm, Q_{BD} is 0.12C/cm^2 and ten years operation voltage is 3.6V. Under NH_3 or N_2O plasma pre-oxidation treatment, low field leakage current will slightly increase, but these plasma treatments make the CoTiO on poly-Si more reliable. In contrast; post-oxidation treatment will degrade the reliability of the CoTiO on the poly-Si.

Pure NH_3 surface nitridation



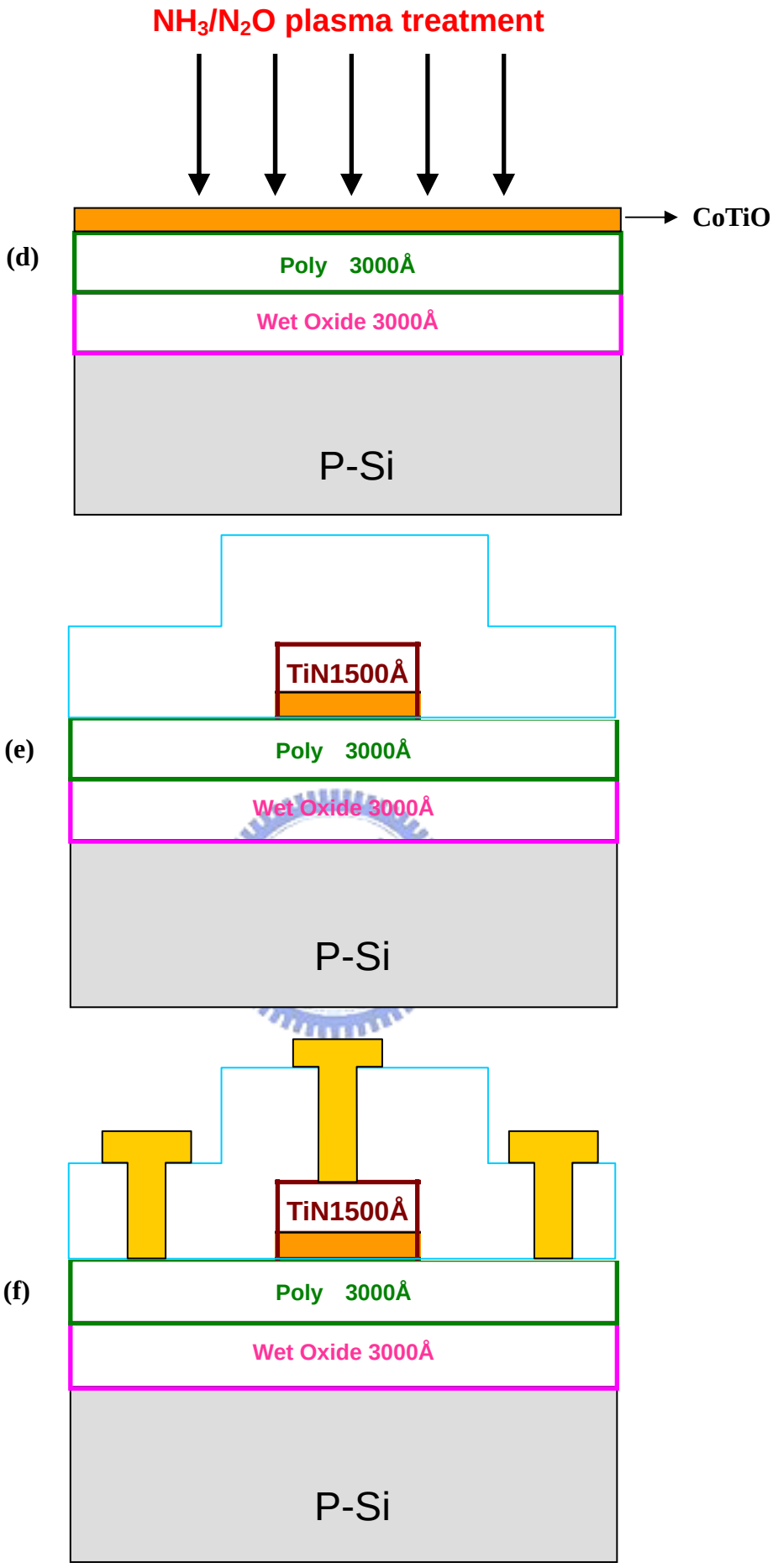


Fig.4.1 (a)(b)(c)(d)(e), the TiN/CoTiO/poly-Si capacitor fabrication process flow

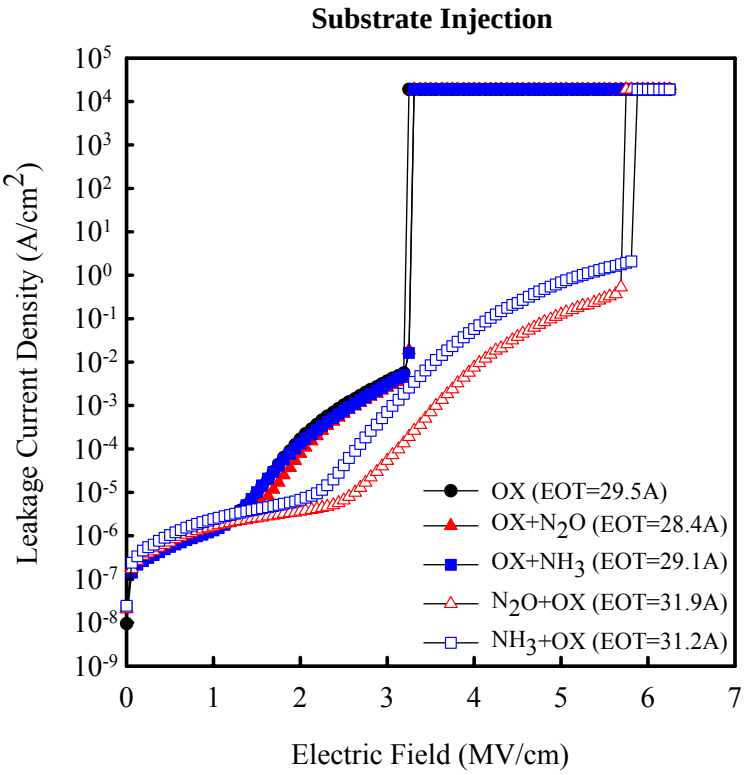


Fig.4.2 J-E characteristic of substrate injection with various plasma treatment methods.

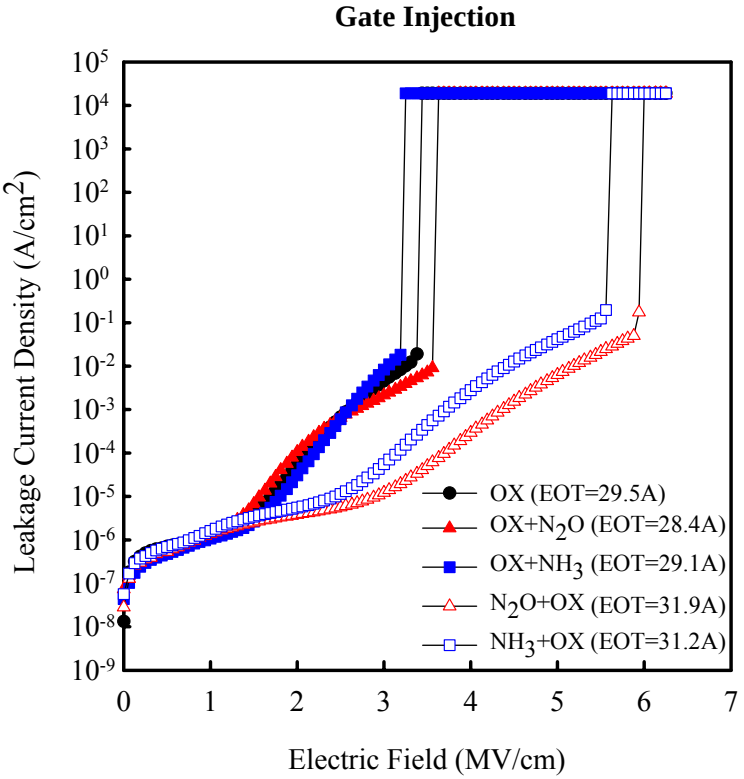


Fig.4.3 J-E characteristic of gate injection with various plasma treatment methods.

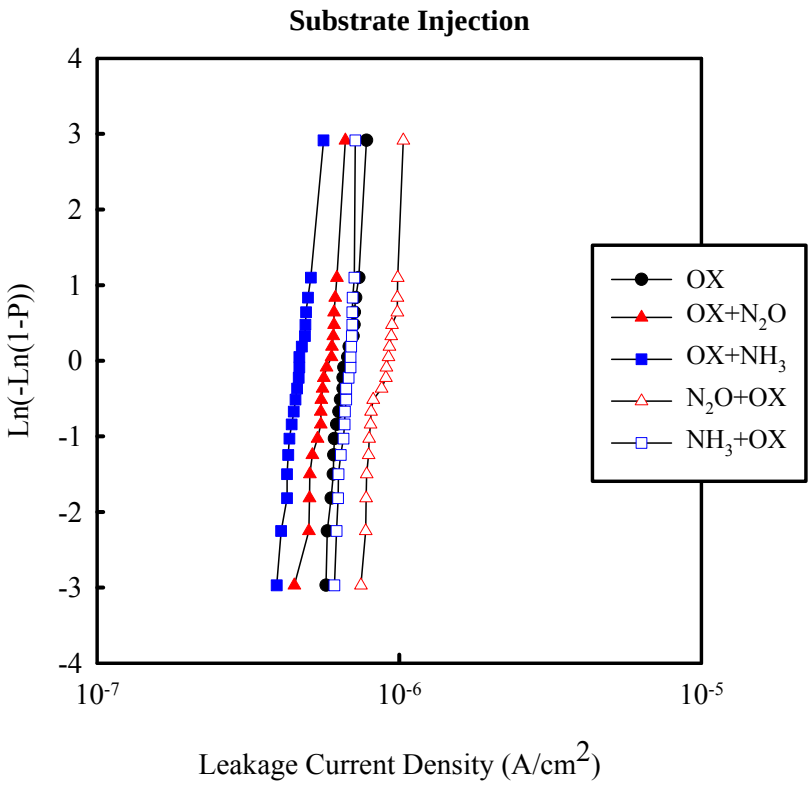


Fig.4.4 Weibull plot of the leakage current density at Vg =+1V

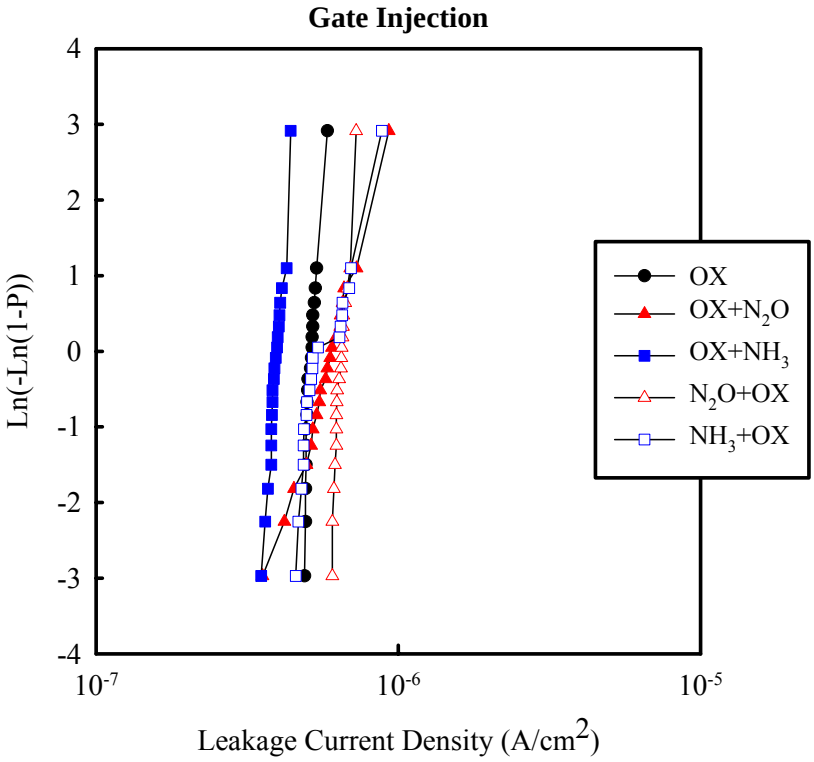


Fig.4.5 Weibull plot of the leakage current density at Vg = -1V

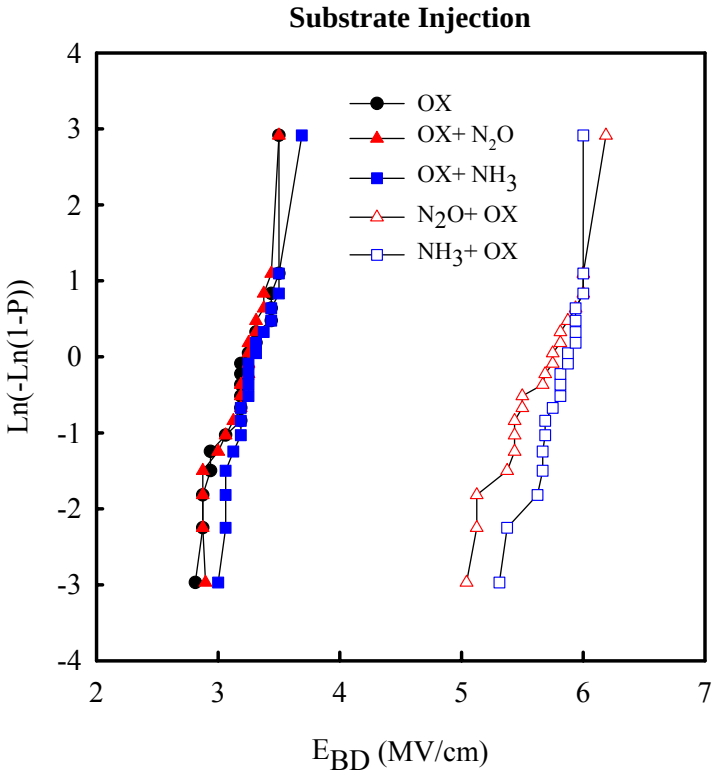


Fig.4.6 Weibull plot of the breakdown electric field under substrate injection.

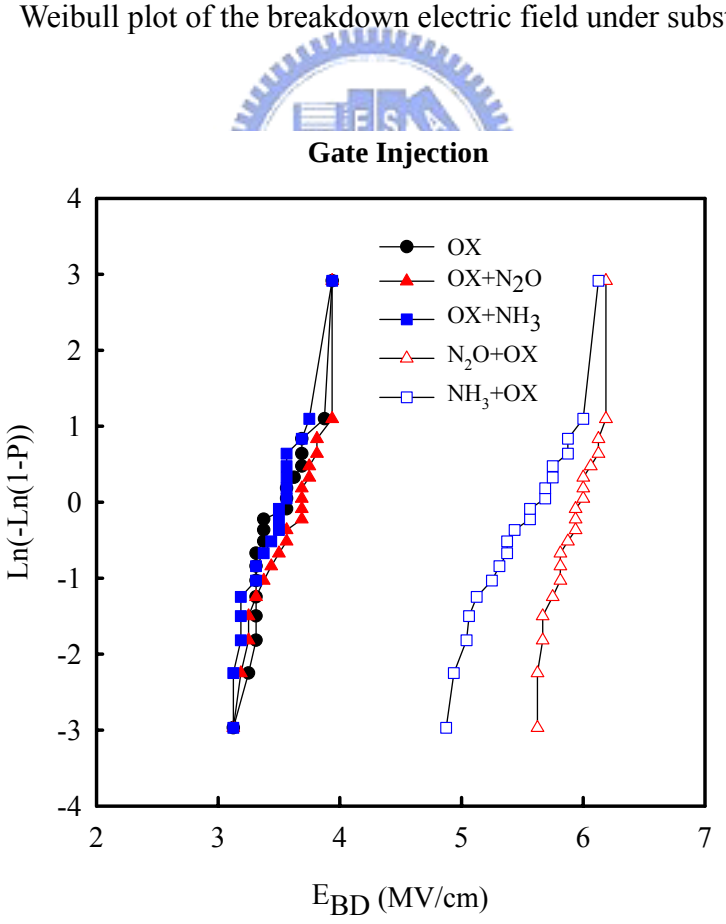


Fig.4.7 Weibull plot of the breakdown electric field under gate injection.

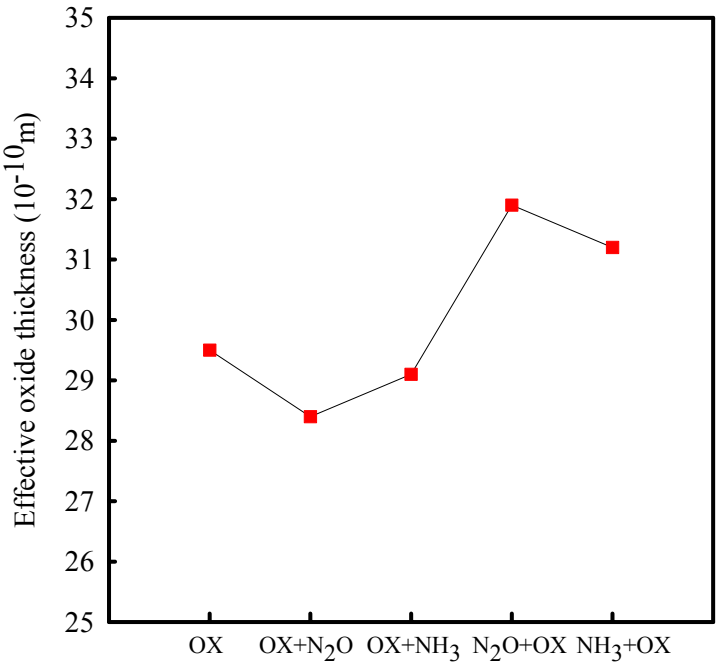


Fig.4.8 Effective oxide thickness with various plasma treatment methods.

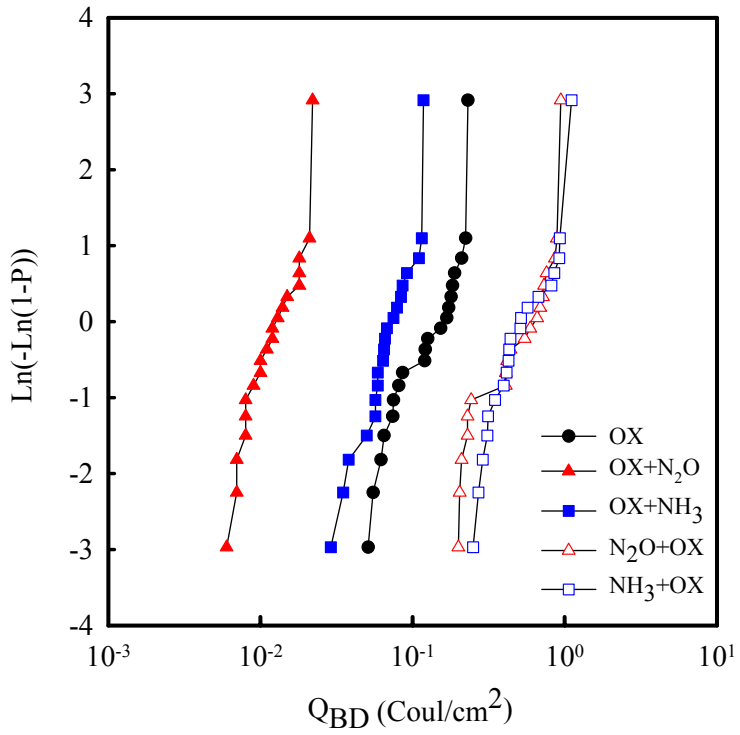


Fig.4.9 Charge to breakdown characteristic under substrate injection.

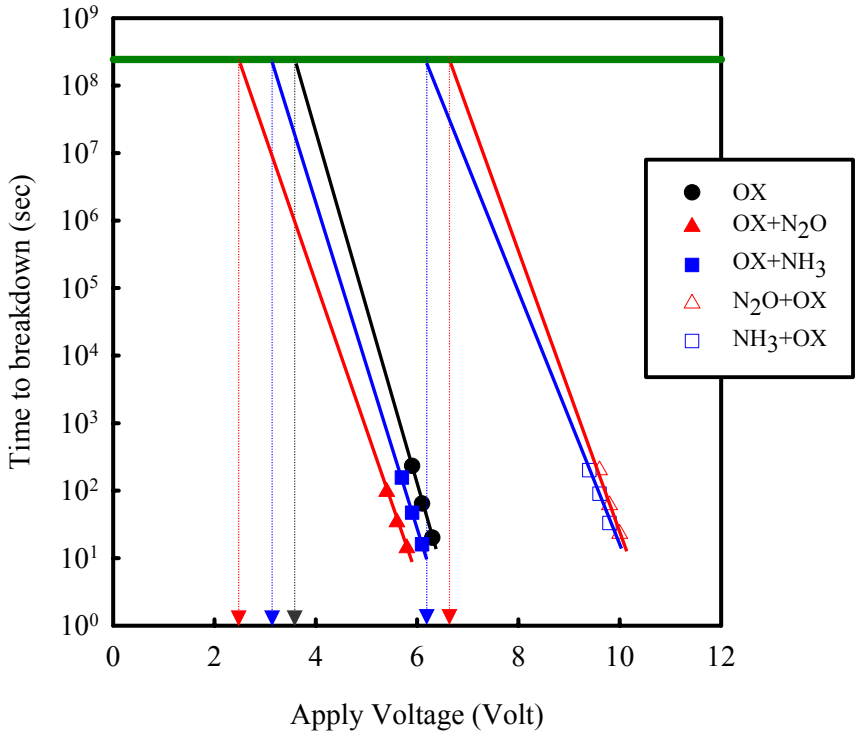


Fig.4.10 TDDB characteristic under substrate injection.

Table 4.1 Summary of our results, Ct/Cc is base on the assumption of the thickness of the tunnel oxide equal to 80Å and control gate area equal to the floating gate area. Ten years operation voltage is obtained from TDDB plot. $V_{interpoly}$ means the voltage which across the interpoly dielectric. We also assume NOR type flash W/E voltage is 10V and NAND type flash W/E voltage is 20V.

CONDITION / PARAMETER	OX	OX+N_2O	OX+NH_3	N_2O+OX	NH_3+OX
EOT(Å)	29.5	28.4	29.1	31.9	31.2
Effective K value	33.05	34.33	33.5	30.56	31.25
Ct/Cc	0.368	0.355	0.363	0.398	0.39
Coupling Ratio	0.73	0.738	0.733	0.715	0.719
Ten years operation voltage(Volt)	3.6	2.4	3.1	6.6	6.2
$V_{Interpoly}$ (Volt) (NOR 10V)	2.69	2.62	2.66	2.85	2.81
Pass or Fail	Pass	Fail	Pass	Pass	Pass
$V_{Interpoly}$ (Volt) (NAND 20V)	5.39	5.24	5.33	5.7	5.61
Pass or Fail	Fail	Fail	Fail	Pass	Pass

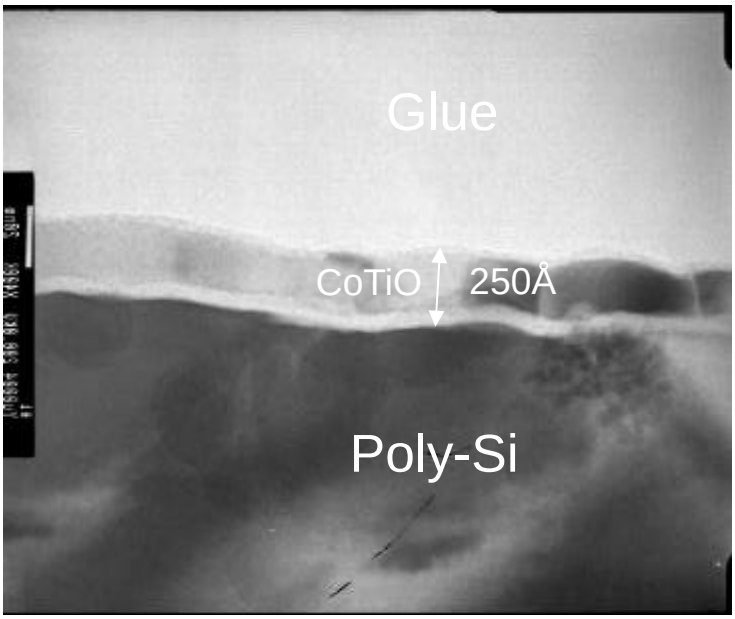


Fig.4.11 TEM image of the as-oxidation sample.

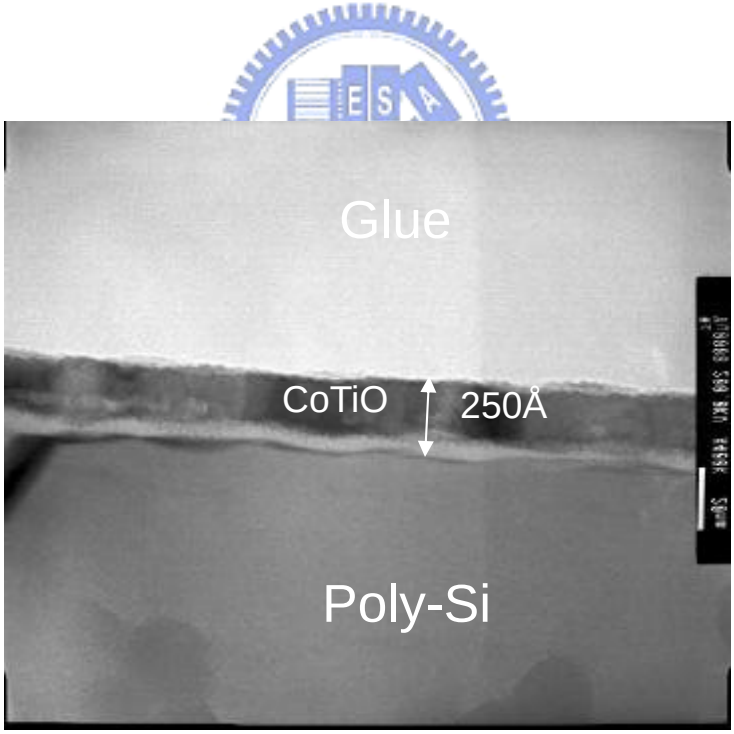


Fig.4.12 TEM image of the sample with NH_3 pre-oxidation treatment.

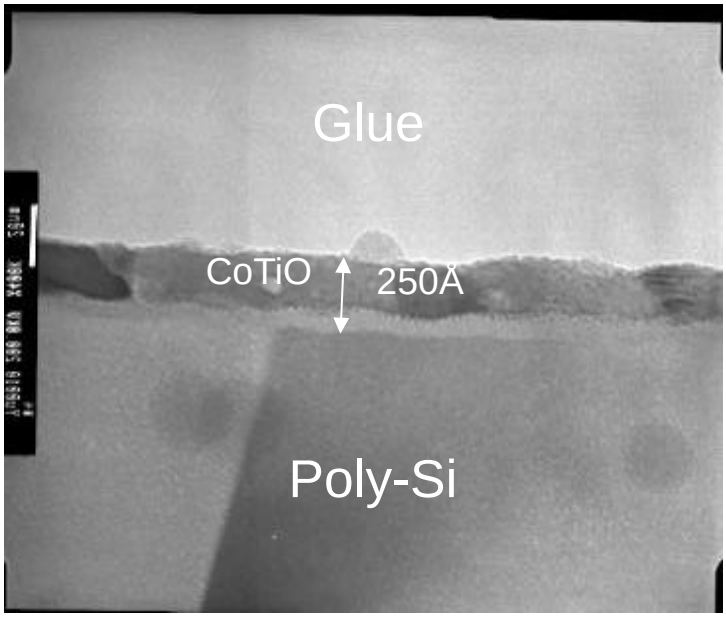


Fig.4.13 TEM image of the sample with N_2O pre-oxidation treatment.

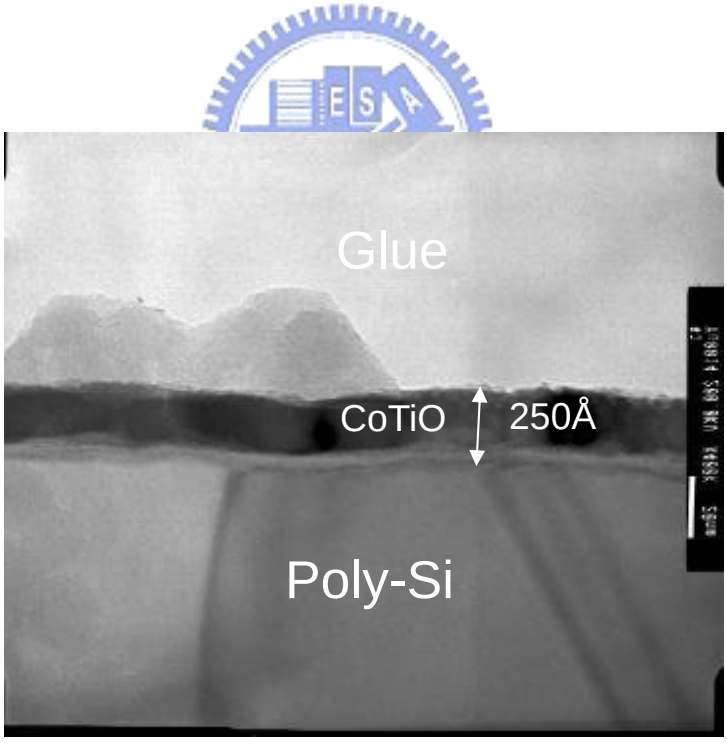


Fig.4.14 TEM image of the sample with N_2O post-oxidation treatment.

Chapter 5

NiTiO Compatibility for Flash memory Applications: the Influence on Tunneling-Oxide Integrity

5.1 Introduction

For a long time, metal contamination is a serious concern for the front-end device fabrication process, because it causes junction leakage and oxide degradation. Therefore, from starting-material preparation to device fabrication, there are many methods to avoid metal contamination, such as intrinsic gettering and extrinsic gettering on wafer backside, RCA clean, O_2+HCl mixing gas used in oxidation process, BPSG (Borophosphosilicate Glass) used as passivation dielectrics, etc[21]-[22]. However, some advanced technologies such as full-silicided gate and high-k gate dielectrics are metal-related processes. It is important to verify that metal-related processes won't degrade the device performance, which is the first concern in process integration. The NiTiO and CoTiO thin films presented in this thesis are formed by high temperature oxidation of sputtered metals. When they are applied to FLASH memory as alternative inter-poly dielectrics, would these metal-related processes affect the tunneling-oxide integrity? Recent reports demonstrated that full-silicided NiSi or $CoSi_2$ gate is feasible to MOSFET process, while the thermal-budget after metal deposition was well-controlled in a certain range [23]-[24]. For silicide formation, NiSi takes one-step annealing at rather low temperature (400^{o}C), and $CoSi_2$ takes two-step annealing (first 500^{o}C, and then 750^{o}C) [25]-[26]. These silicidation anneals are RTA (Rapid Thermal Anneal) processes,

which means lower thermal budget and little opportunities of metal diffusion into the gate-oxide. However, considering the furnace oxidation process utilized for NiTiO/CoTiO films, the metal diffusion is still an issue in further application. In this chapter, we applied NiTiO MIM to a flash memory gate stack, and investigated the tunneling oxide integrity for process evaluation. Compatible results are obtained. These metal oxide films showed promising properties as alternative high-k dielectrics for MIM applications.

5.2 Experimental procedure

P-MOS capacitors with LOCOS isolation and *in-situ* doped poly-Si gates were fabricated. Process flow chart was shown in Figure 5.1(a)-(e). As shown in Figure 5.1(a), process started with 6-inch p-type Si wafer. After standard clean, 350Å pad oxide and 1500Å nitride were deposited by LPCVD. The active regions were defined by photolithography (in reversed tone). Then Nitrides and pad oxides were selectively removed by dry etching. After dry-etch and clean process, wet oxides were thermally grown to 5500Å with H_2 and O_2. To remove remaining nitrides and pad oxides, H_3PO_4 and BOE were used respectively. Sacrificial oxides of 350Å thick were grown and soon removed by HF dip; this step was performed twice to eliminate Koei effects.

After LOCOS, 70Å tunneling oxides were thermally grown by a vertical furnace cluster, and 3000Å poly-silicon films were deposited with *in-situ* PH_3 doping. The structure was shown in Figure5.1 (b). In Figure 5.1 (c), samples were divided into two groups, and different inter-poly oxides were applied. For controls, 200Å TEOS oxides were deposited. For other samples, NiTiO films were fabricated using the process explained in Chapter 2. Prior to either inter-poly oxide deposition, a surface nitridation was performed at 800C in NH_3 for 2 hours, for all samples. In order to investigate the tunneling oxide integrity, the TEOS and NiTiO films were then etched

by dry etching. Aluminum films with target thickness 5000Å were deposited by thermal evaporation, as shown in Figure 5.1(d). The gate electrodes of capacitors were patterned and defined by ILD-4100 metal etcher with Cl_2 gas. Finally, as shown in figure 5.1(e), 5000Å thick Al films were deposited on the back of wafers to form the ohmic contact.

5.3 Results and Discussion

In this section, J-E characteristics, High-Low frequency C-V curves and TDDB reliability analysis of the tunneling oxides were evaluated. The J-E curves and reliability characteristics were measured by Agilent HP4156B semiconductor parameter analyzer. High frequency and quasi C-V curves were measured by Keithley model KI82 system.

5.3.1 J-E Characteristics

Figure 5.2 shows a plot of current density versus applied electric filed. Comparing the tunneling-oxide J-E curves, no significant differences were observed between samples that underwent conventional TEOS polyoxide process and those underwent NiTiO high-k polyoxide process. Figure 5.3 shows the Weibull plots of breakdown electric fields, and of leakage current densities under an electric field of 2.85MV/cm. There was no obvious degradation in tunneling-oxide E_{BD} or low field leakage distribution, while the TEOS polyoxides were replaced with NiTiO films, which involved high temperature oxidation of metal thin films.

5.3.2 Interface State Density

In the high-temperature metal oxidation process, if metal penetrated into poly-Si and arrived at tunnel oxide, it would cause defects in the oxide bulk or interface states at the oxide/Si interface. If metal contamination produced oxide traps or interface states, it would appear to be CV curve shifts or distortion [27]. Figure 5.4 shows the

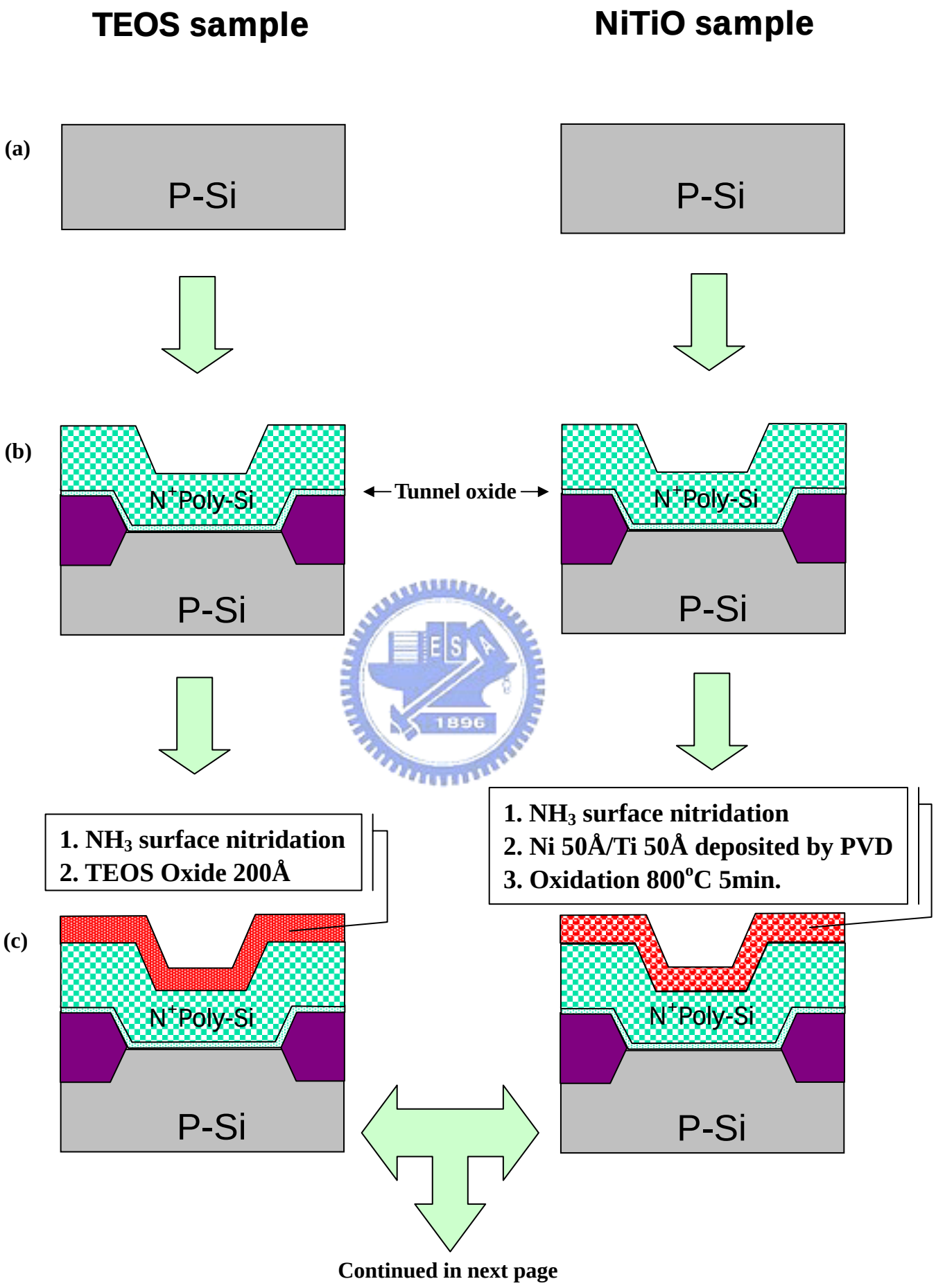
high-frequency CV and quasi CV curves. Comparing with the TEOS polyoxide processed sample, the sample with NiTiO process shows no distortion or shifts in CV curves of the tunneling oxide. Figure 5.5 shows the interface-state densities extracted from CV curves. TEOS processed and NiTiO processed samples exhibited very similar interface-state density profile, which is around 10^{11} ($cm^{-2}eV^{-1}$).

5.3.3 TDDB Characteristics

Figure 5.6 shows TDDB characteristics of the tunneling oxides. For each condition, five different voltage biases were tested on the tunneling oxides. The ten-year lifetime was obtained by extrapolation. Both TEOS processed and NiTiO processed samples have the same ten-year operation field of 8.7MV/cm for the tunneling oxides. This result suggests that the application of NiTiO films doesn't degrade the tunneling-oxide reliability.

5.4 Summary

In this chapter, we designed a simple experiment to demonstrate the practicability of high-temperature metal oxidation process. When we applied NiTiO dielectrics on the floating gate of FLASH memory structure, this process showed no negative influence on the tunneling oxides. Therefore, we can draw a preliminary conclusion that NiTiO/CoTiO MIM process is a feasible alternative for high coupling-ratio capacitor applications.



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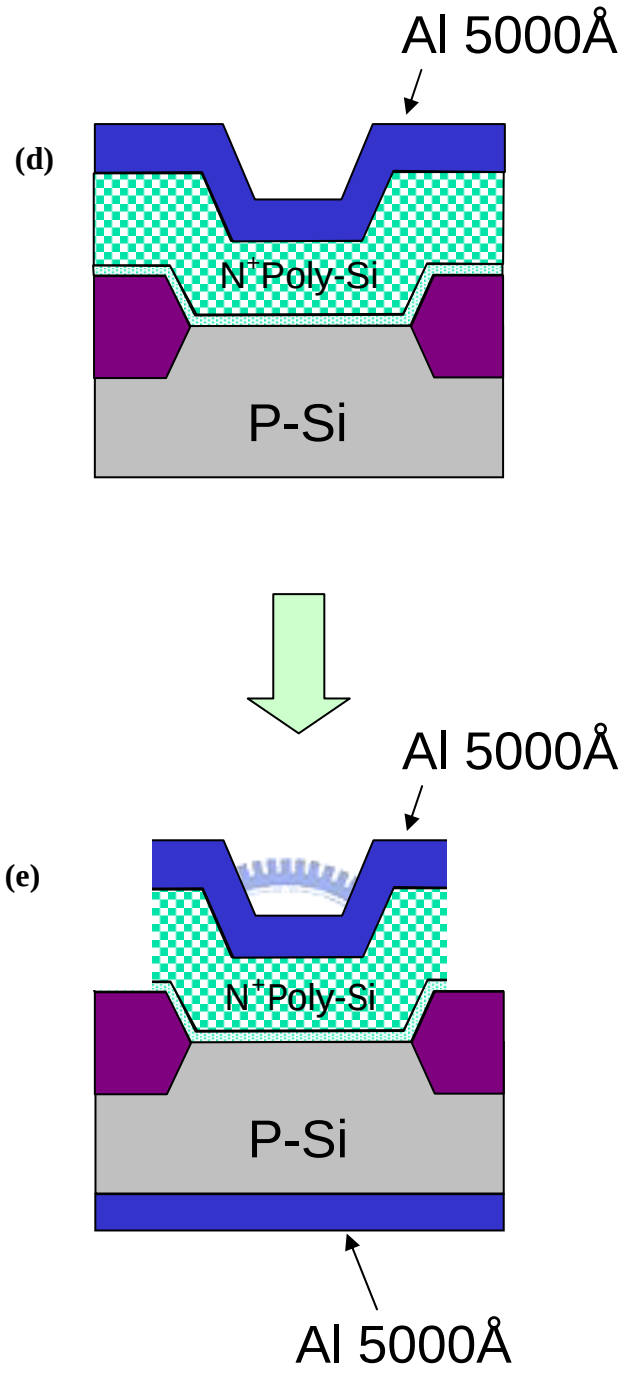

Fig.5.1 P-MOSCAP fabrication process (a) start material (b) LOCOS, tunnel oxide growth and poly-Si deposition (c) polyoxide fabrication (d) polyoxide etch-out and Al deposition (e) electrode pattern definition and back-side Al deposition.

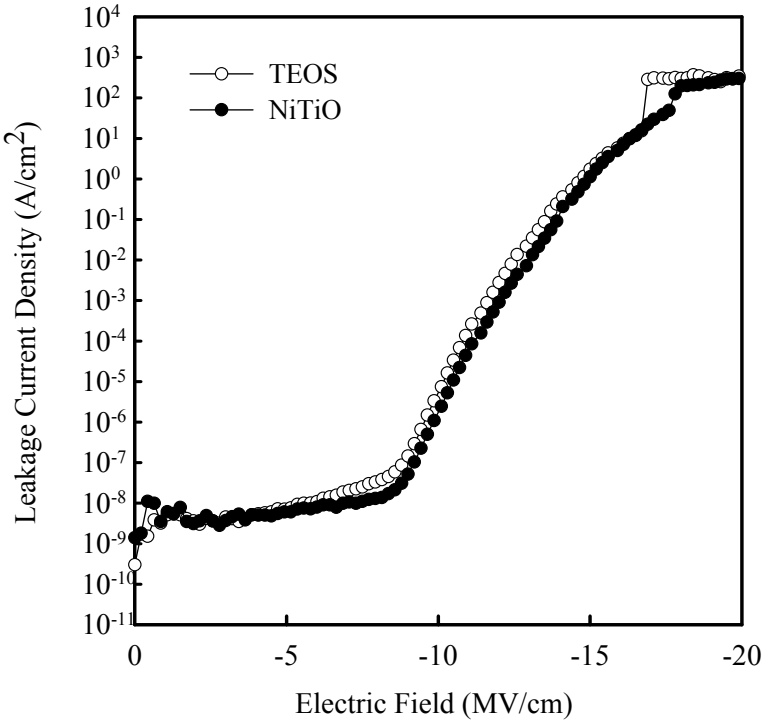

Fig.5.2 J-E characteristics of tunneling oxides with additional polyoxide (TEOS or NiTiO) process following poly-silicon gate deposition.

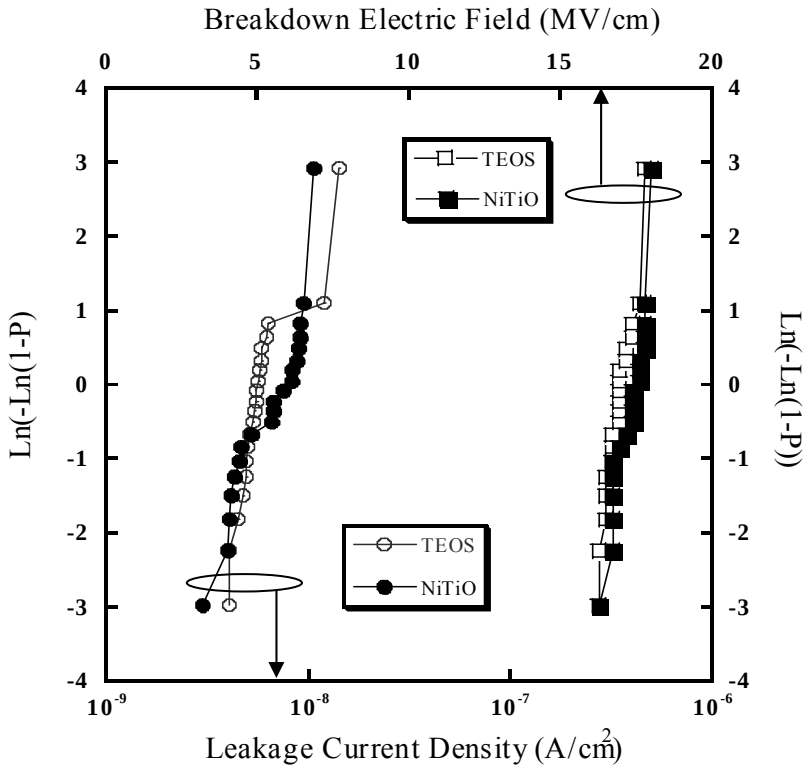

Fig.5.3 Leakage current density (at E=2.85MV/cm) and E_{BD} statistics of tunneling oxides, with additional polyoxide (TEOS or NiTiO) process.

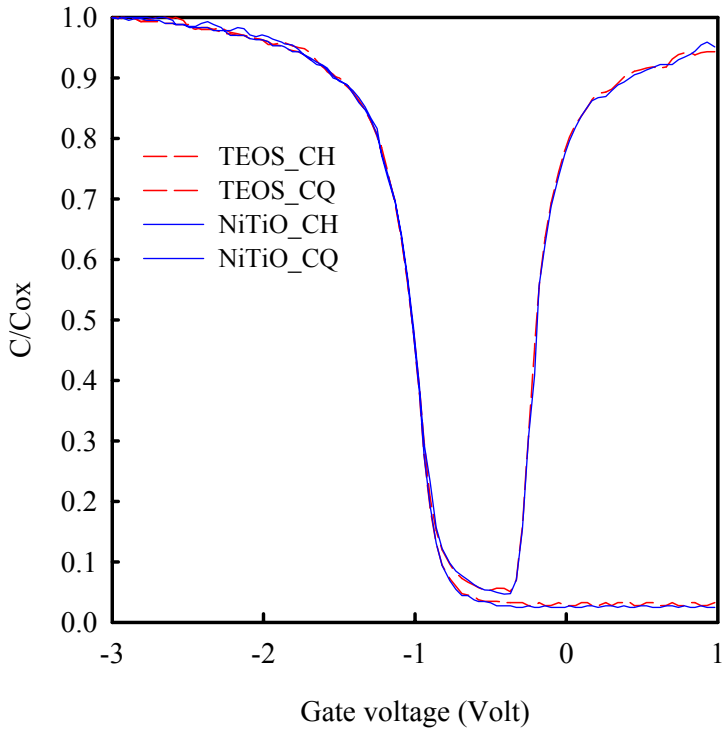

Fig.5.4 High-frequency and quasi CV plots for the tunneling oxides with additional polyoxide (TEOS or NiTiO) process.

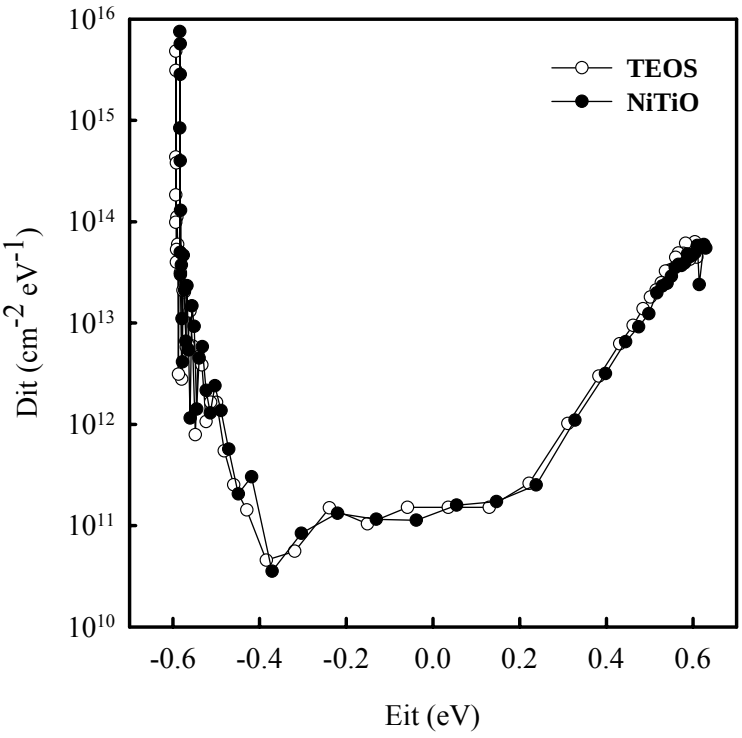

Fig.5.5 Interface state densities of tunneling oxides with additional TEOS or NiTiO polyoxide process.

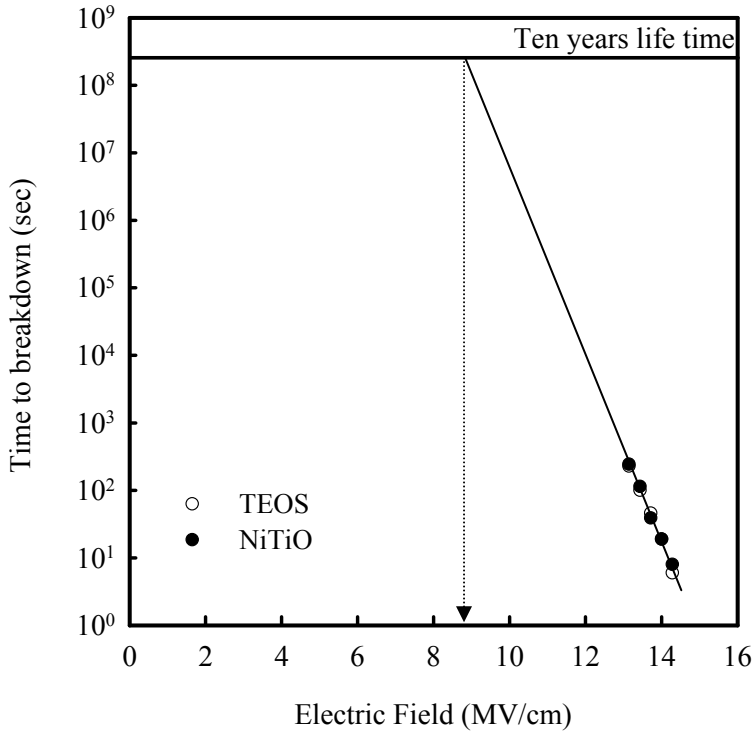

Fig.5.6 TDDB analysis of tunneling oxides with TEOS or NiTiO films fabricated on top of poly-silicon gate.

Chapter 6

Conclusions

In this thesis, characteristics and reliability of NiTiO and CoTiO as interpoly dielectrics with various plasma treatment method and rapid thermal annealing have been studied. All results of this study are summarized as below.

The thermal stability of NiTiO on poly-Si was investigated. After post-oxidation annealing, the leakage current, breakdown field and reliability are all degraded. From TEM image, we believe that some crystal phases formed in NiTiO film after post-oxidation anneal is responsible for these electrical properties degradation.

Then, NH_3 plasma pre-oxidation treatment was first used in NiTiO film. By adding this process, thermal stability of the low field leakage current, breakdown electric field, and reliability of this film can be improved. From material analysis, NiTiO with NH_3 plasma pre-oxidation treatment reveal less agglomeration and smoother surface roughness. We believe that NH_3 plasma could incorporate nitrogen into the film and strengthen it.

Moreover, plasma treatments are applied to CoTiO interpoly dielectric. In this experiment, both N_2O and NH_3 plasma were used. We demonstrate pre-oxidation treatment is superior to post-oxidation treatment. Comparing the reliability of CoTiO with NiTiO, (Table 3.1 and Table 4.1) CoTiO is more reliable than NiTiO. After our

pre-oxidation treatment, CoTiO reveal more potential for application in flash memory.

Finally, considering the fabrication process of these two materials, we demonstrate the feasibility of high temperature metal oxidation process for flash memory applications. MOS capacitors with additional polyoxide (TEOS or NiTiO) process were fabricated. Our experimental data reveal high temperature metal oxidation process doesn't degrade the tunneling oxide quality.

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Study of NiTiO/CoTiO Inter-poly Dielectrics with NH_3/N_2O Plasma Treatment

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