Chapter 2

Uniformity in the Interditigated Layout and Multi-channel Structure of Low-Temperature Polycrystalline Silicon Thin Film Transistors

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2.1 Introduction

Low-temperature poly-Si TFT plays an important role for the realization of system-on-panel by means of its higher driving current and better reliability. For the applications of high-speed circuits such as memories, processors, and drivers, excellent performances of reliability and uniformity of LTPS-TFTs are strongly required [2.1]-[2.4]. To achieve high performance poly-Si TFTs, high quality poly-Si thin film is firstly required. It is known that the existence of traps in poly-Si thin film has great impact on the electrical properties of poly-Si TFTs. The conductivity of poly-Si TFT is mainly influenced by the grain boundaries because the trap levels at the grain boundaries form the potential barrier. Recently, high performance and high reliability poly-Si thin film transistors with multi-channel structure were reported to reduce grain boundary defects and exhibit superior gate control ability [2.5]-[2.13]. It is referred to induce side-channels on both channel regions which increase effective channel width. As a result, the slicing layout of poly-Si TFTs with multi-channel

structure can obtain higher driving current and reduce grain boundary defects. Besides, the effect of the active region pattern becomes more significant as the channel width is scaled down.

On the other hand, the passivation by hydrogen plasma has been proved to reduce the grain boundary trap states in many researches. The sub-threshold swing and threshold voltage are strongly influenced by the density of dangling-bond midgap states, while the leakage current and field-effect mobility are related to the strain-bond which exists in tail states [2.14]-[2.17]. Among the various plasmas, hydrogenation plasma is the best candidate to passivate the midgap trap state arising from the dangling bonds in the grain boundaries effectively.

In many circuit design compensation techniques, such as AMOLED pixel design and analogue buffer circuits using matching TFTs with the same property assumption. Design skills are used that the threshold voltage and field-effect mobility difference can be cancelled in circuit operation. However, the uniformity of polycrystalline TFT's is expected to be worse than that of MOS transistors qualitatively. Mismatching behaviors that can still be observed between the electrical characteristics of equally designed devices. This is because the result of several random process which occur during every fabrication of the devices.

Many researches have been reported that the fewer the grain boundaries within the channel region, the better the electrical characteristic of LTPS-TFTs will be. However, an increase in the average grain size leads to an increase in variations in the number of grains. This tough problem will degrade the uniformity of electric quality of low temperature poly-Si TFTs seriously [2.18]. Therefore, it is very important to improve the uniformity and performance of LTPS-TFTs. Some reports also focused on uniformity issue by proving mathematical equations [2.19] but there is no research reported by experiment. In this work, the uniformity and performance of interdigitated

layout and multi-channel structure with slicing layout method are fabricated and investigated. Only layout method is modified without changing the original process steps. At last, the mechanism of improving uniformity and electrical performance is elaborated in detail.

2.2 Dimensional Effects and Layout Methods on the Matching Properties of P-channel Low-Temperature Polycrystalline Silicon Thin-Film Transistors

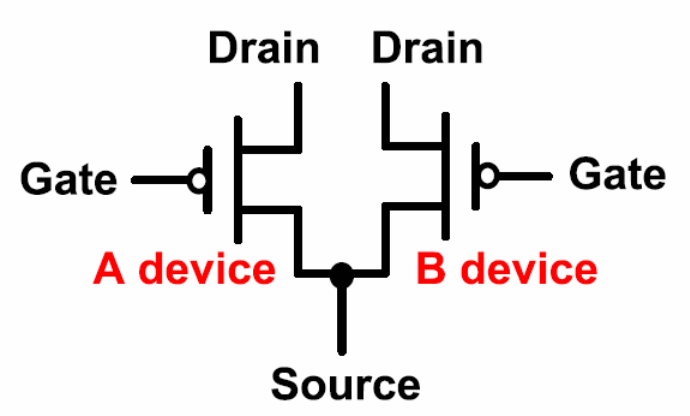
There are many integrated circuits employing matched transistors concept which assumes the characteristics of neighboring transistors to be identical. Design skills are used that the threshold voltage and field-effect mobility difference can be cancelled in circuit operation. However, the uniformity of polycrystalline TFT's is expected to be worse than that of MOS transistors qualitatively. Mismatching behaviors that can still be observed between the electrical characteristics of equally designed devices. This is because the result of several random process which occur during every fabrication of the devices.

2.2.1 Experimental Procedure and Results

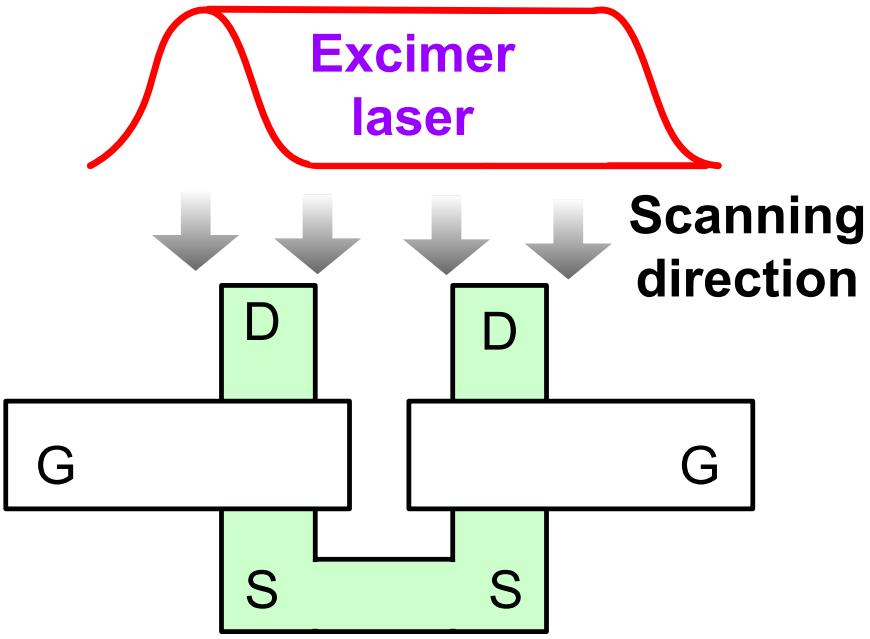
The p-channel LTPS TFTs were fabricated by the following sequence of processes. First, a 3000Å-thick buffer oxide and 500Å-thick a-Si thin film was deposited on glass substrate. Then, the amorphous Si thin film was crystallized by

KrF excimer laser annealing at room temperature. After defining the active layer, a 1000Å-thick gate oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 400°C. A 3000Å-thick MoW thin film was then deposited at 200°C by sputtering for gate electrode. Then, the MoW thin film and gate oxide were etched to form gate electrodes. Next, a 4000Å-thick oxide was deposited by PECVD as interlayer. Finally, p-channel LTPS TFTs were formed after contact-hole formation and metallization. All the devices are unhydrogenated.

In order to realize the matching properties of LTPS TFTs, the p-type differential pair devices were fabricated, shown in Fig. 2-1(a). Fig. 2-1(b) shows the layout method corresponding to excimer laser scanning direction. The I-V curves of the TFTs were measured using an HP 4156 semiconductor parameter analyzer. The maximum field-effect mobility was extracted from the transconductance in the linear region at Vds= -0.1V. The minimum subthreshold swing were measured at Vds = -0.1 V and the threshold voltage was defined as the gate voltage required to achieve a normalized drain current of Ids = $(W/L)*10^{-8}$ A at Vds = -0.1 V.



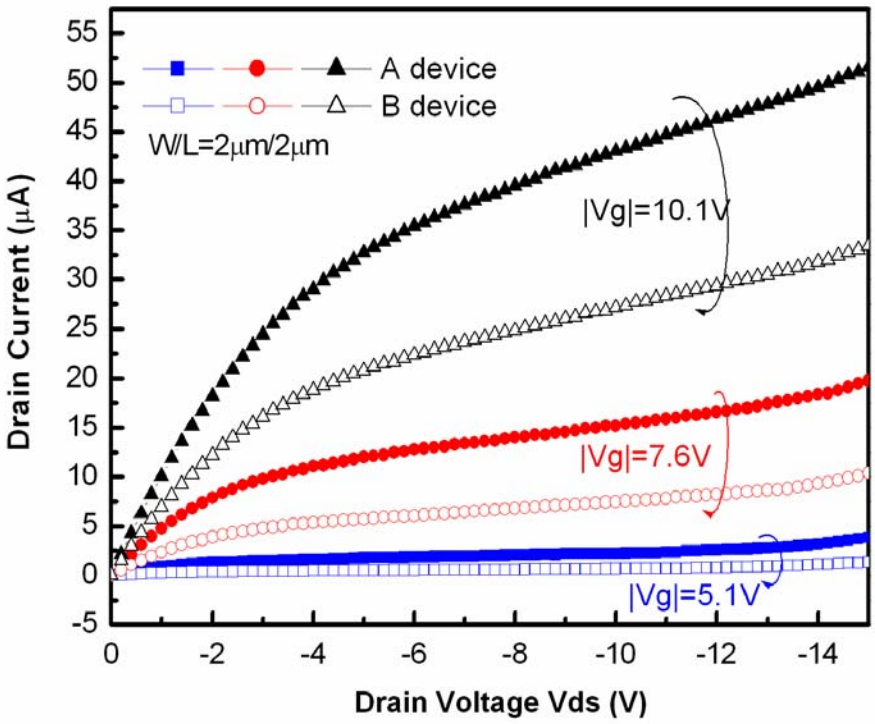
(a)



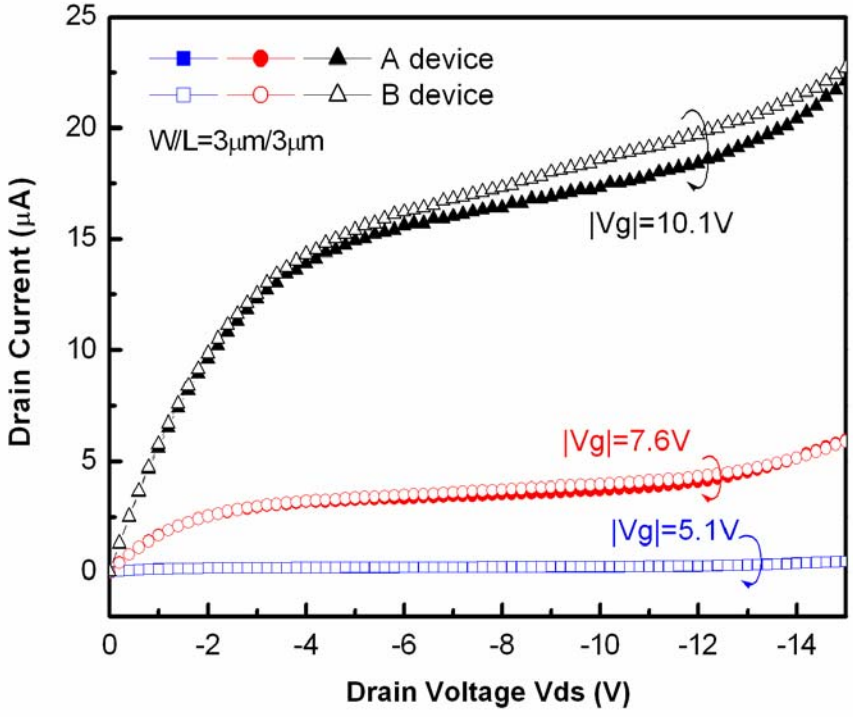
(b)

Fig. 2-1. (a) The differential pair circuit, (b) Parallel arrangement layout method corresponding to excimer laser scanning direction of matching TFTs

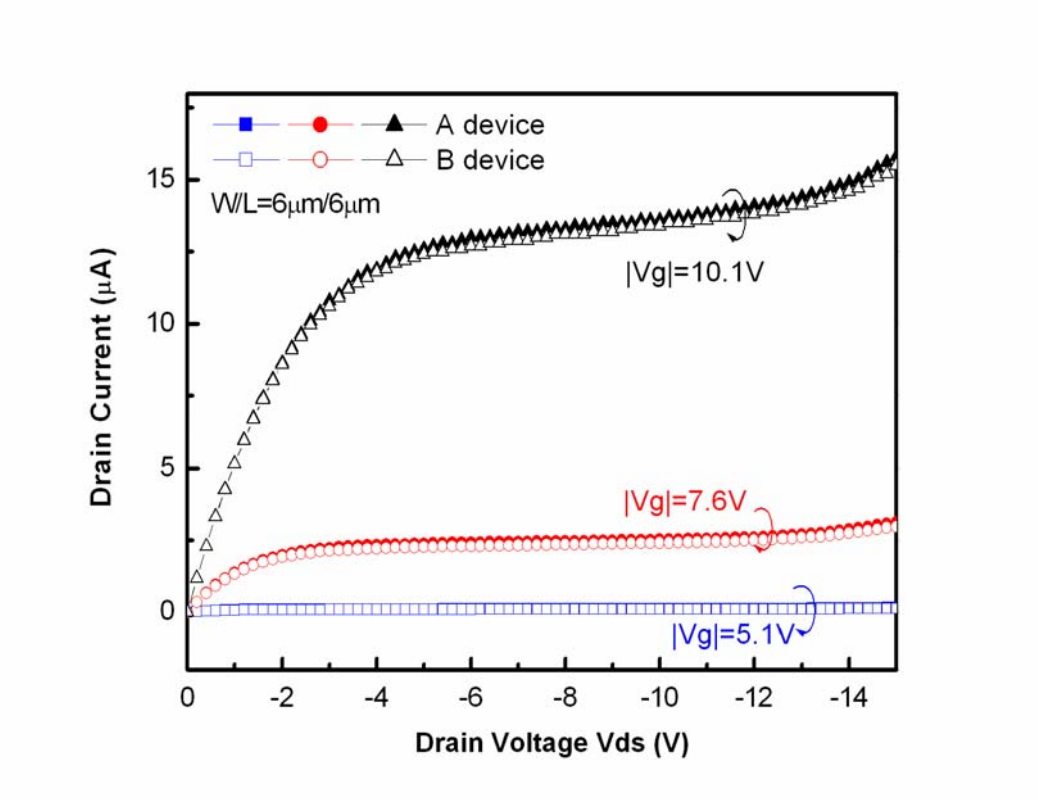
Fig. 2-2 (a)-(d) shows the typical normalized output characteristics (i.e. W/L ratio=1) of non-passivated p-channel matching TFTs with W/L = 2 μm/2 μm, 3 μm/3 μm, 6 μm/6 μm, and 12 μm/12 μm. The channel dimension dependence of drain current Ids is observed. In Fig. 2-2(a), the small dimension exhibits larger output current and more serious kink effect. It is reported that the improved grain structure of the TFT's with small channel dimensions may be related to the decrease in the number of grain boundaries in the active channel of the devices. Furthermore, these results reveal that the difference of output characteristics decrease with larger device size. Uncontrolled variations tend to become dominant for small device sizes. They require device or circuit designs to improve the overall uniformity.


A device
B device
W/L=2μm/2μm
|Vg|=10.1V
|Vg|=7.6V
|Vg|=5.1V
Drain Current (μA)
Drain Voltage Vds (V)
55
50
45
40
35
30
25
20
15
10
5
0
-5
0
-2
-4
-6
-8
-10
-12
-14

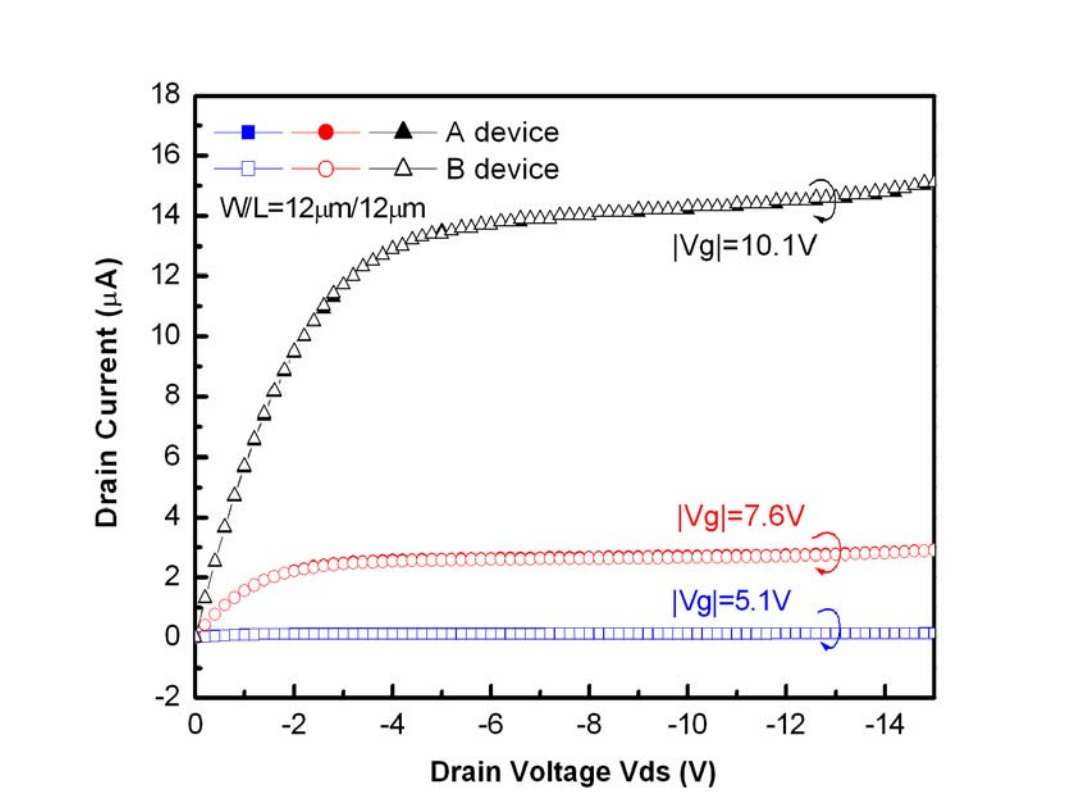
(a)


A device
B device
W/L=3μm/3μm
|Vg|=10.1V
|Vg|=7.6V
|Vg|=5.1V
Drain Current (μA)
Drain Voltage Vds (V)
25
20
15
10
5
0
0
-2
-4
-6
-8
-10
-12
-14

(b)


A device
B device
W/L=6μm/6μm
|Vg|=10.1V
|Vg|=7.6V
|Vg|=5.1V
Drain Current (μA)
Drain Voltage Vds (V)
15
10
5
0
0
-2
-4
-6
-8
-10
-12
-14

(c)


A device
B device
W/L=12μm/12μm
|Vg|=10.1V
|Vg|=7.6V
|Vg|=5.1V
Drain Current (μA)
Drain Voltage Vds (V)
18
16
14
12
10
8
6
4
2
0
-2
0
-2
-4
-6
-8
-10
-12
-14

(d)

Fig. 2-2. Normalized output characteristics (i.e. W/L ratio=1) for non-passivated p-channel matching TFTs with (a)W/L = 2 μm/2 μm, (b)3 μm/3 μm, (c)6 μm/6 μm, and (d)12 μm/12 μm. The small dimension exhibits larger output current and more serious kink effect.

2.2.2 Comparison of Different Layout Methods

Fig. 2-3 and 2-4 show the other two layout methods corresponding to excimer laser irradiating direction. For convenience, the parallel, perpendicular, and interdigitated arrangement refer to Fig. 2-1(b), Fig. 2-3, and Fig. 2-4, respectively. Each point is calculated from a mean value of five pairs of matching TFTs.

The threshold voltage differences for the three types of arrangement matching TFTs with different channel widths and channel lengths are plotted in Fig. 2-5. The threshold voltage difference order is around 0.03V-2V in parallel arrangement, 0.02V-0.23V in perpendicular arrangement and 0.02V-0.15V in interdigitated arrangement. For easy comparison, the Fig. 2-5(a) graph would be rescaled to Fig. 2-5(b), which has the same scale as perpendicular arrangement in Fig. 2-5(c) and interdigitated one in Fig. 2-5(d). The threshold voltage difference is mainly attributed to the grain boundaries. The grain boundaries cause dangling bonds and traps which lead to high energy barrier for the channel conducting. It is clear that threshold voltage difference of interdigitated arrangement smaller than parallel and perpendicular ones. Furthermore, the small TFTs suffer from larger threshold voltage difference than large ones. The large contribution of threshold voltage variations suggests that circuit and device design using small TFTs must be more variation-tolerant.

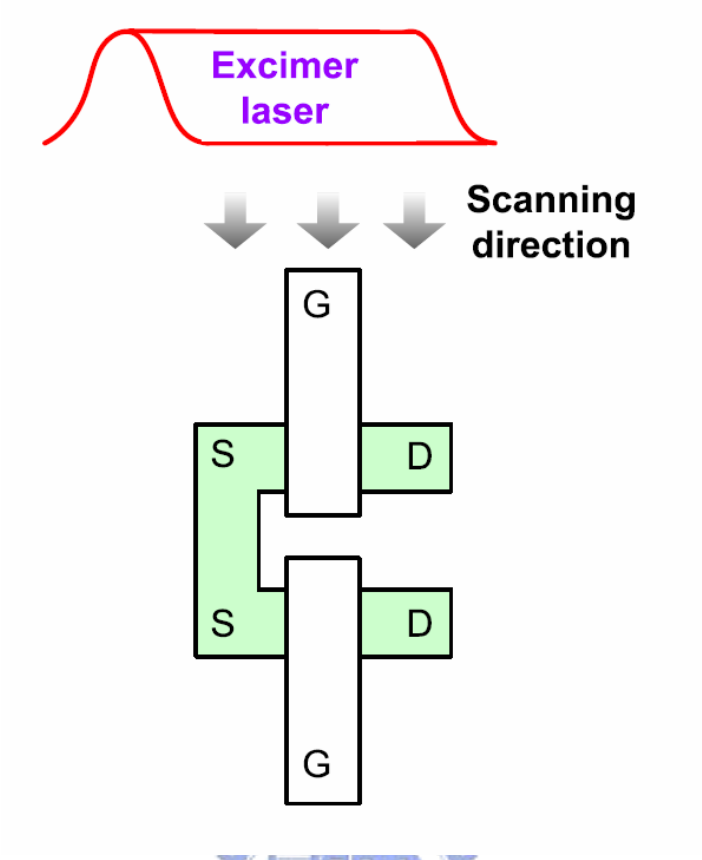


Fig. 2-3. Perpendicular arrangement layout method corresponding to excimer laser scanning direction of matching TFTs.

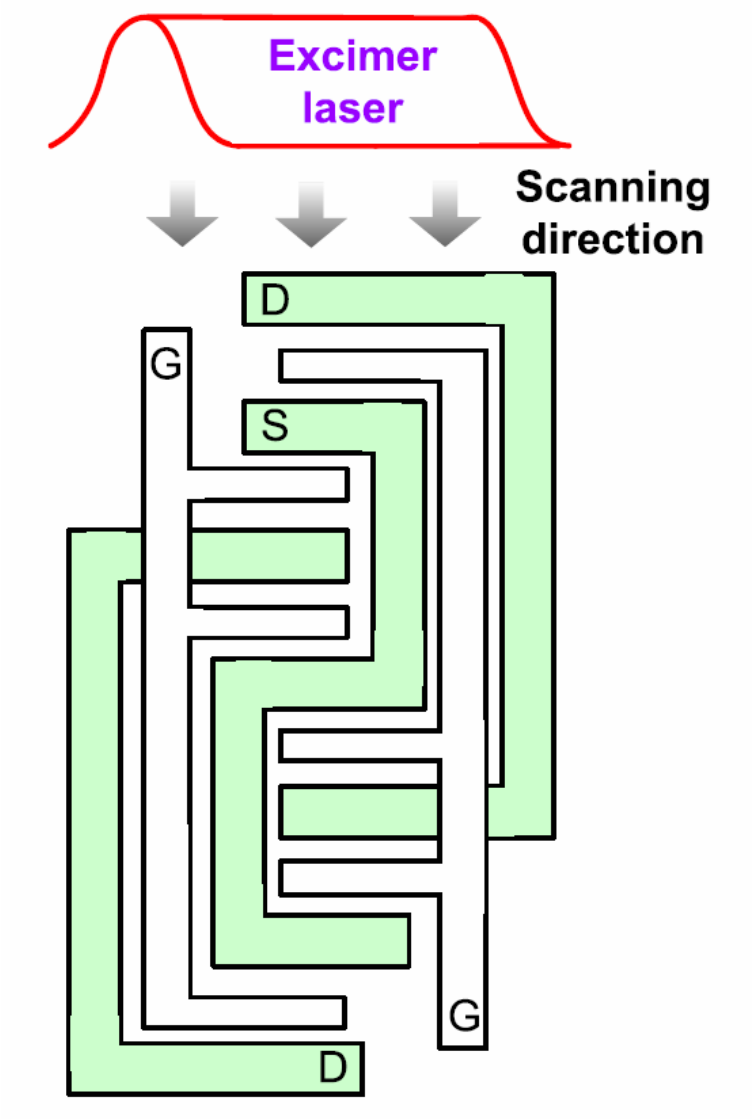


Fig. 2-4. Interdigitated arrangement layout method corresponding to excimer laser scanning direction of matching TFTs.

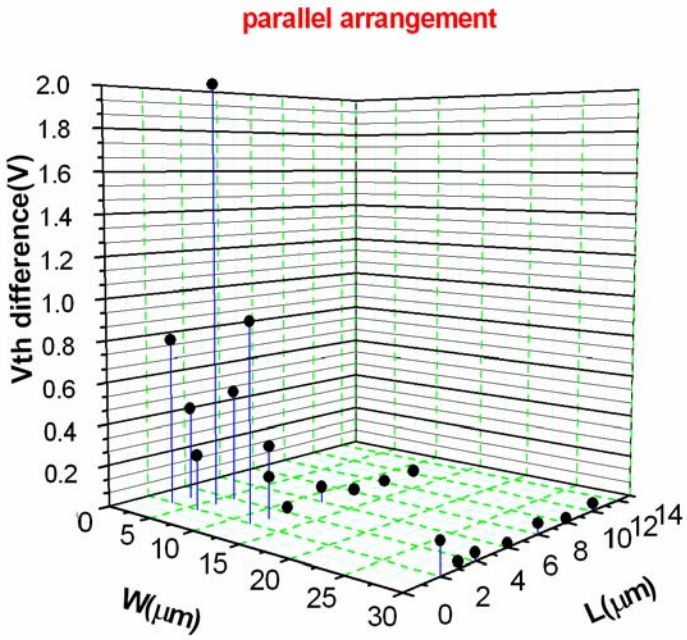


Fig. 2-5(a)

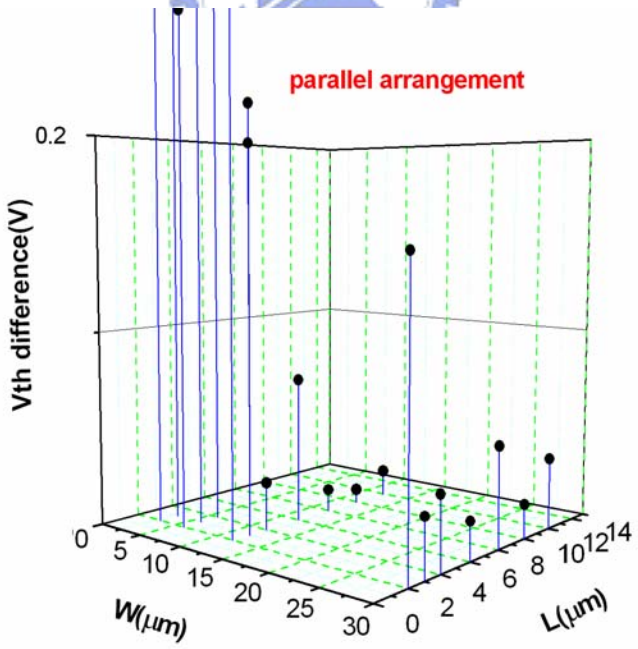


Fig. 2-5(b)

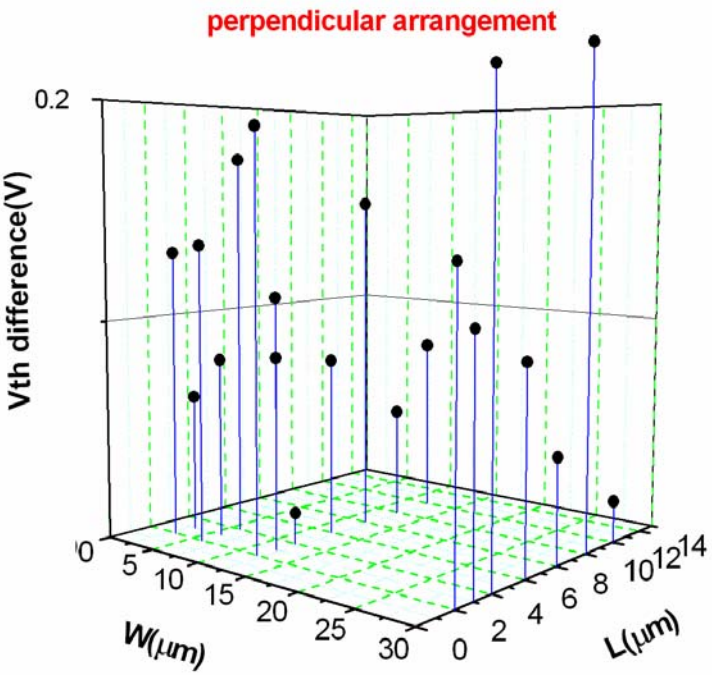


Fig 2-5(c)

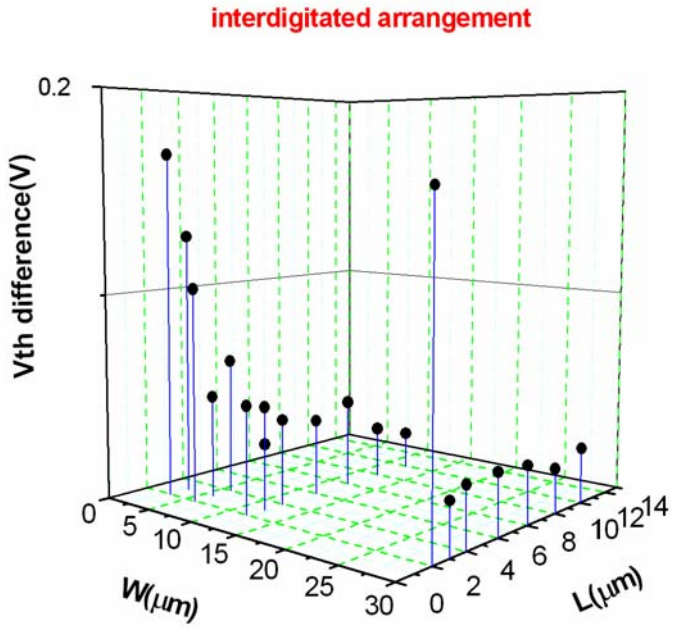


Fig. 2-5(d)

Fig. 2-5. Threshold voltage difference between different layout methods of matching TFTs with different channel widths and channel lengths (a) parallel arrangement, (b) parallel arrangement in magnified scale, (c) perpendicular arrangement, and (d) interdigitated arrangement.

Concerning field-effect mobility, manufacturers are primarily concerned with higher mobilities at the driver area in order to squeeze in all the required circuitry within the narrow pixel pitch as well as to integrate more circuitry. Field-effect mobility performance is closely tied to the grain size and grain crystallinity. Since the defect traps place a profound influence on electrical characteristics of LTPS TFTs, the mobility difference issue is essential. Fig. 2-6(a)-(c) shows the field-effect mobility difference between matching TFTs with different channel widths and channel lengths. In general, the field-effect mobility difference ranges from $0.04cm^2/V*s$ to $2.4cm^2/V*s$ of parallel arrangement, from $0.7cm^2/V*s$ to $4.4cm^2/V*s$ of perpendicular arrangement and from $0.07cm^2/V*s$ to $2.2cm^2/V*s$ of interdigitated arrangement.

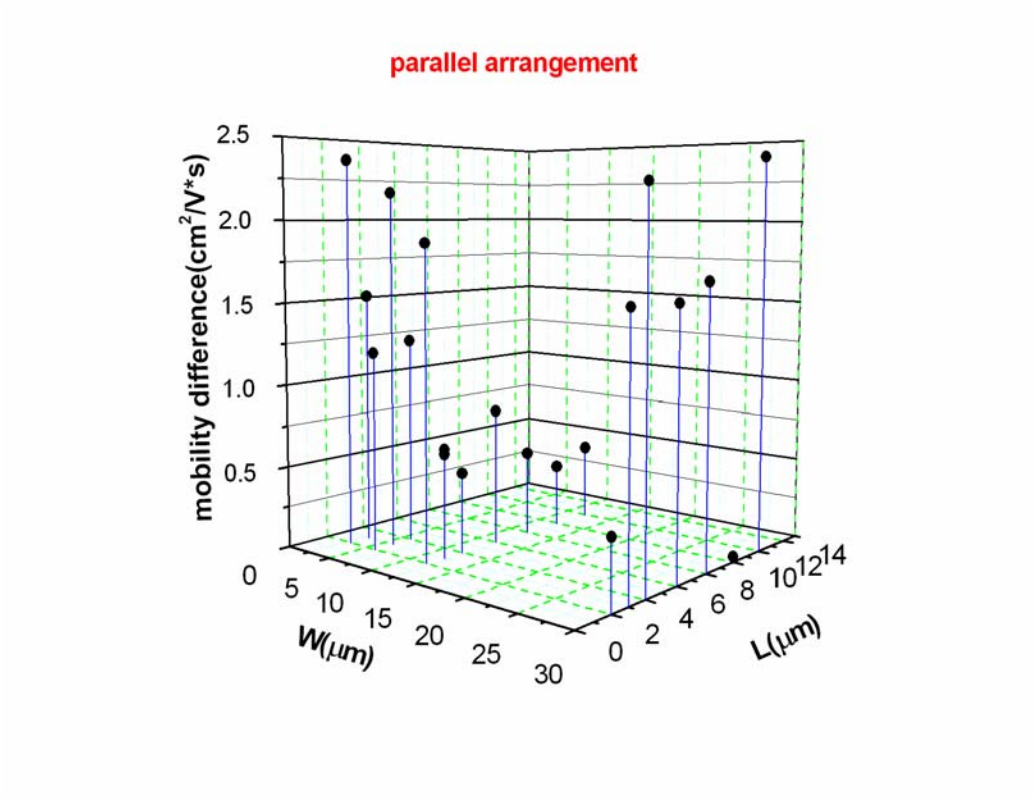


Fig. 2-6(a)

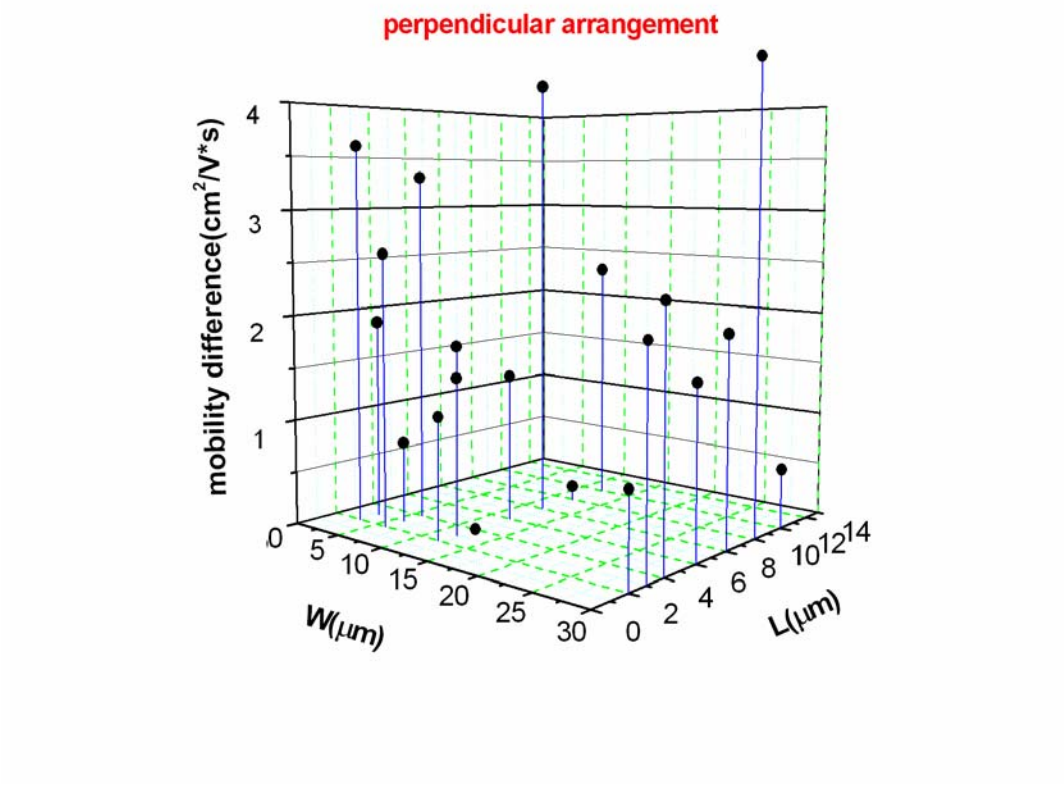


Fig. 2-6(b)

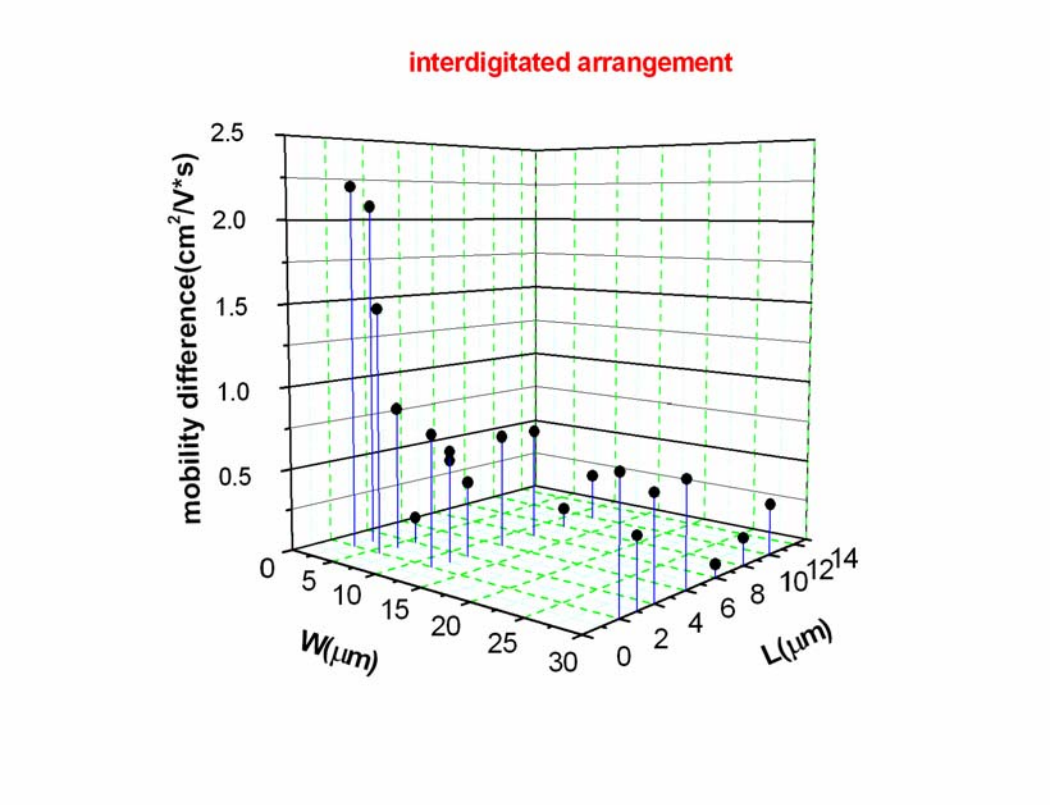


Fig. 2-6(c)

Fig. 2-6. Field-effect mobility difference between different layout methods of matching TFTs with different channel widths and channel lengths (a) parallel arrangement, (b) perpendicular arrangement, and (c) interdigitated arrangement.

Fig. 2-7(a)-(b) shows the mismatching factor related to active area. The mismatching factor is defined as the difference between maximum value (threshold voltage, field-effect mobility) and minimum value, divided by the average absolute value. From these plots, the worst situation always happened on small active area in different electrical characteristics and layout methods. The worse mismatching factor is around 0.2 (20% mismatch) in device characteristics, and the usual mismatching factor is around 0.05 (5% mismatch) in device characteristics. It is observed that interdigitated arrangement have better tolerance than parallel arrangement and perpendicular arrangement in electrical data statistically of matching TFTs.

Furthermore, there are no systematic trend is present in parallel arrangement and perpendicular arrangement in whole electrical properties. This is because the grain structure after excimer laser irrdiation is polygon-like but not stripe-like. The corresponding grain boundaries with the current flow are randomly located in the channel. Therefore, the current flow is not hindered by specific direction.

The occurrence of grain boundaries is random and the defect density is difficult to control in each device. In addition to well process control, optimized design of the device layout can further reduce the variation of matching LTPS TFTs.

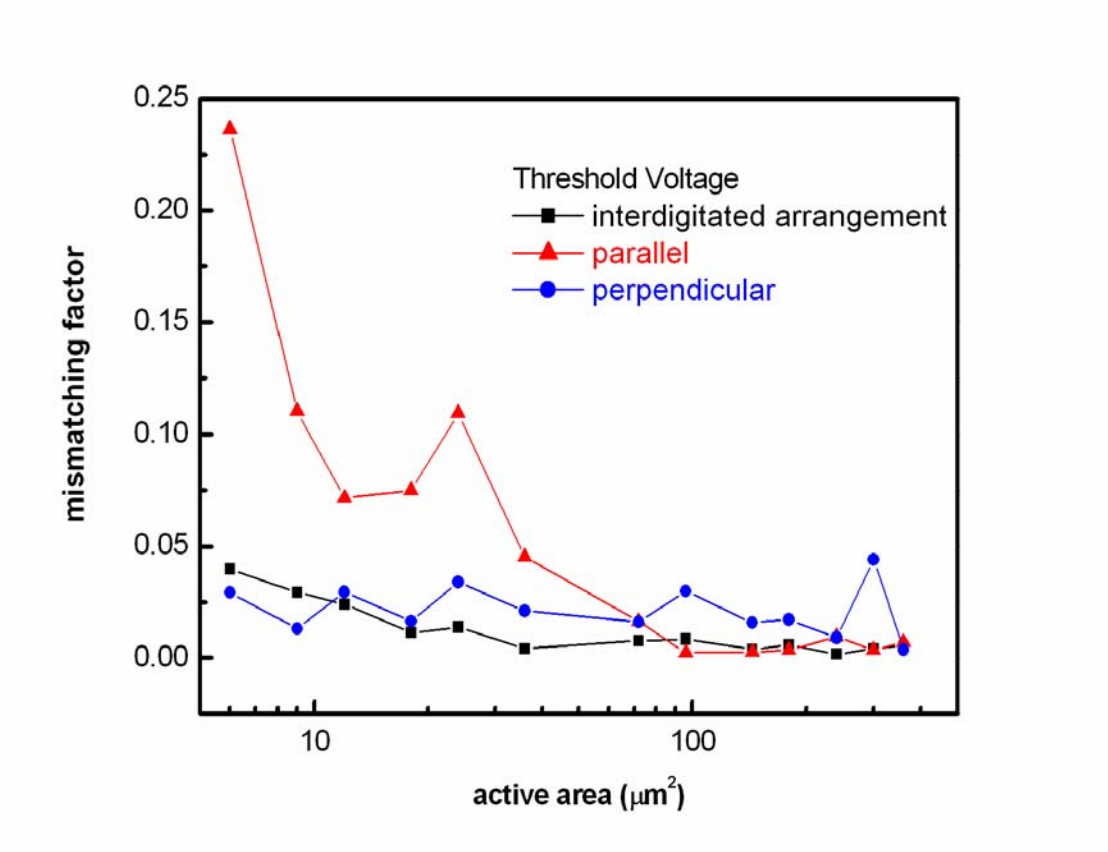


Fig. 2-7(a)

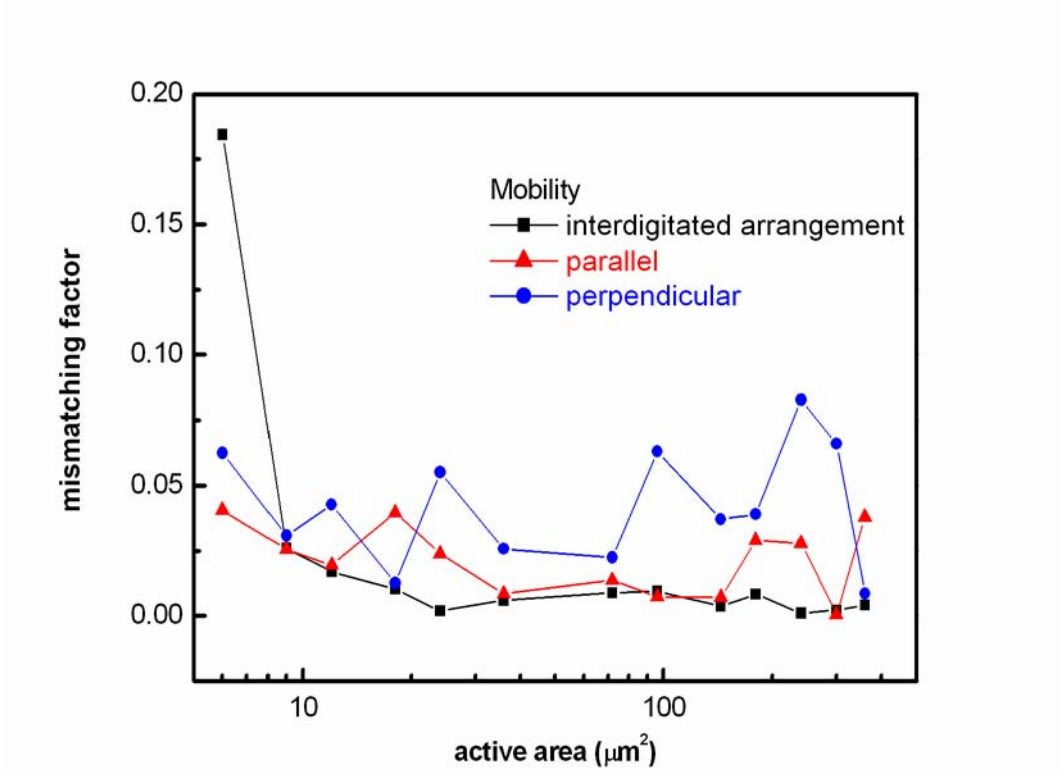


Fig. 2-7(b)

Fig. 2-7. (a)Threshold voltage and (b) Field-effect mobility measured from p-channel LTPS TFTs with different active areas. The worse mismatching factor is around 0.2 (20% mismatch) in device characteristics, and the usual mismatching factor is around 0.05 (5% mismatch) in device characteristics.

2.3 Devices Fabrication of the Low-Temperature Polycrystalline-Silicon Thin Film Transistors with Multi-Channel Structure

2.3.1 Experimental Procedure

At first, the comparison of layout and circuit configuration between conventional

single channel TFTs and multi-channel TFTs is introduced in Fig. 2-8. The signal channel of original device is divided into several poly stripes in multi-channel device which can be easily seen from top view of device.

A buffer oxide and a 500Å-thick a-Si thin film were deposited by furnace and by low pressure chemical vapor deposition (LPCVD) on Si wafer sequentially. Then, the amorphous Si thin film was crystallized by KrF excimer laser (248nm) annealing at room temperature in a vacuum ambient. After defining the active layer pattern, the tetraethyl orthosilicate (TEOS) gate oxide was deposited 500Å by LPCVD. Next, a 2000Å-thick a-Si thin film was then deposited for gate electrode. Self-aligned implantations of phosphorous with dosage of 5×10^{15} cm^{-2} were carried out to form the source and drain regions for n-channel TFTs. Passivation interlayer with a 3000Å-thick TEOS oxide was then deposited, following by dopant activation by annealing at 300°C in the furnace. The device was finished after contact opening and 5000 Å-thick Al metallization by thermal coater. Finally, a 20-mins sintering process was executed at 400°C for reducing the contact resistance of the source/drain electrodes. The detailed process flow chart of ELC LTPS TFTs fabrication is shown in Fig. 2-9.

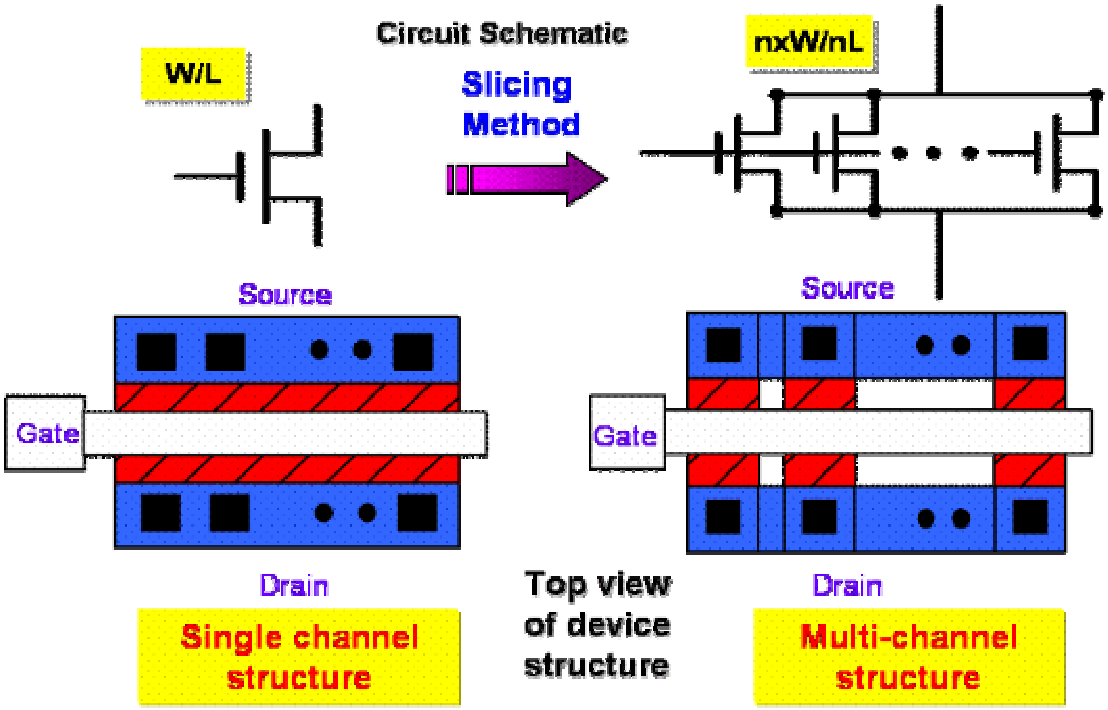


Fig. 2-8. The comparison of layout and circuit configuration between conventional single channel TFTs and multi-channel TFTs.

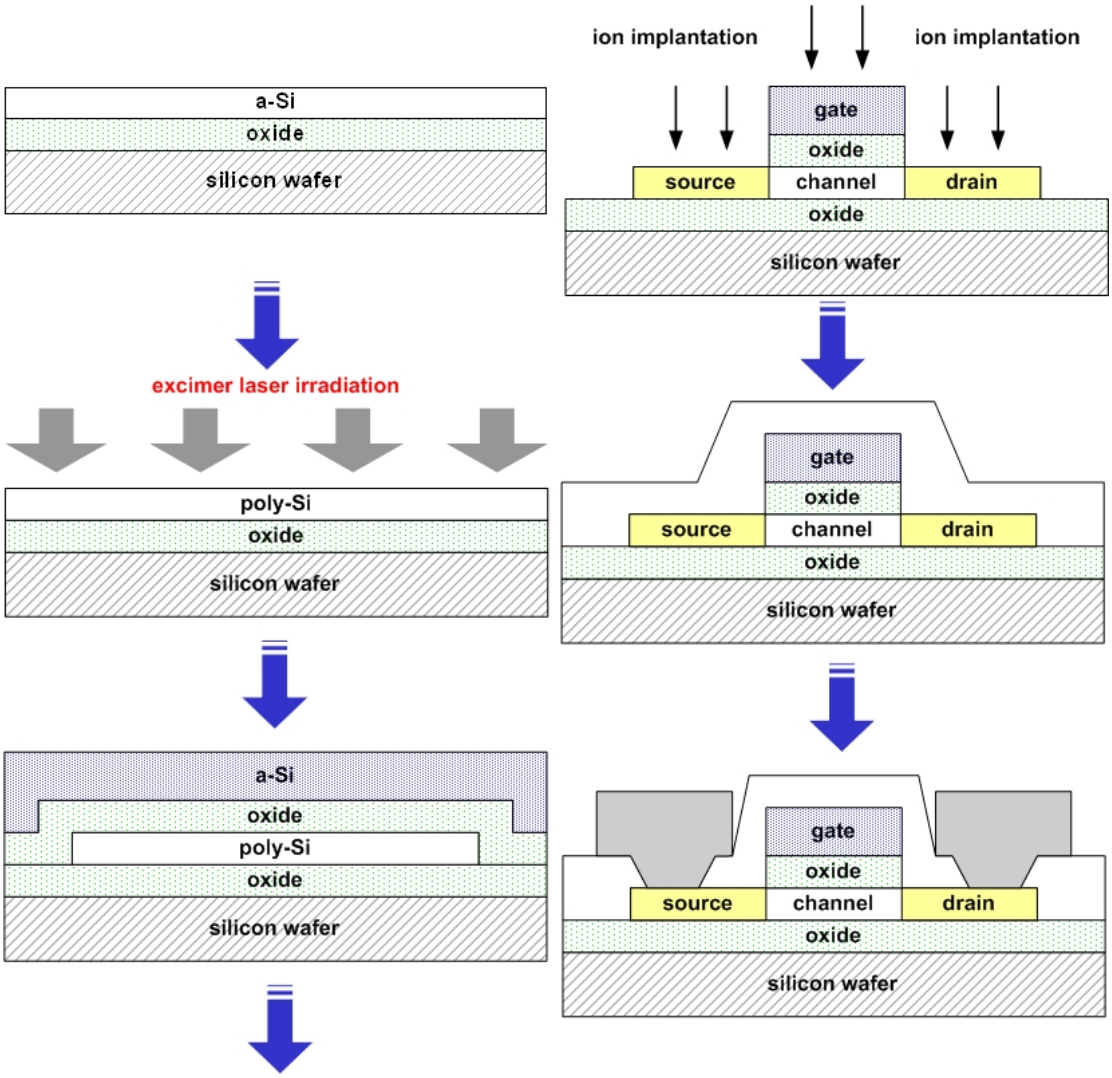


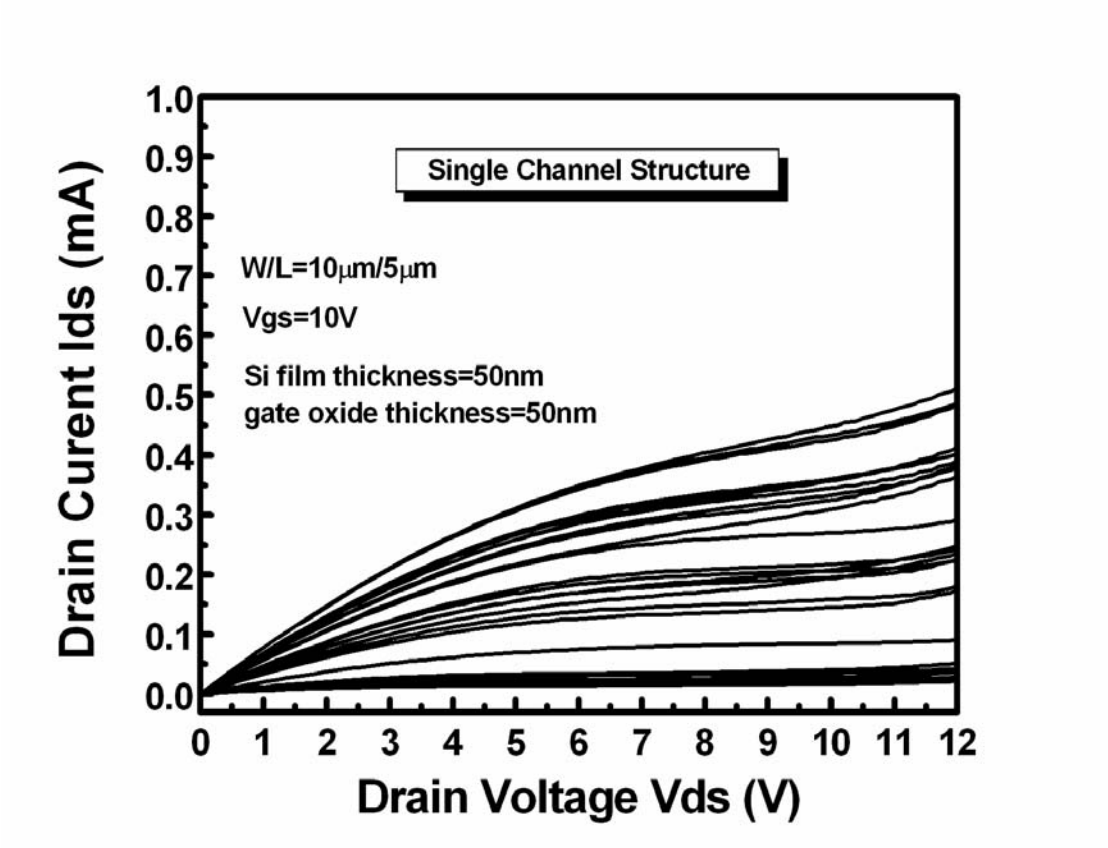
Fig. 2-9. The process procedure of fabricating ELC LTPS TFTs.

2.3.2 Measured Results and Discussion

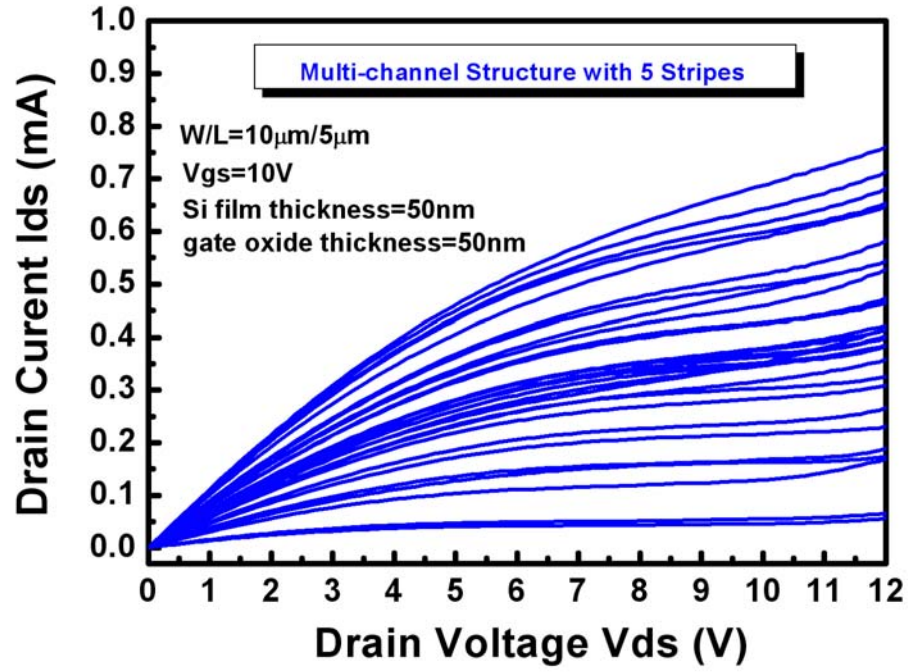
In this work, multi-channel TFTs include different number of stripes for a fixed device size, that is, five stripes and ten stripes. After the device fabrication is finished, the HP 4156C semiconductor parameter analyzer, probe station, and HP 41501A source-measure unit (SMU) and pulse generator expander are utilized to measure the device characteristics.

At first, the output characteristics of LTPS TFTs was measured and statistically

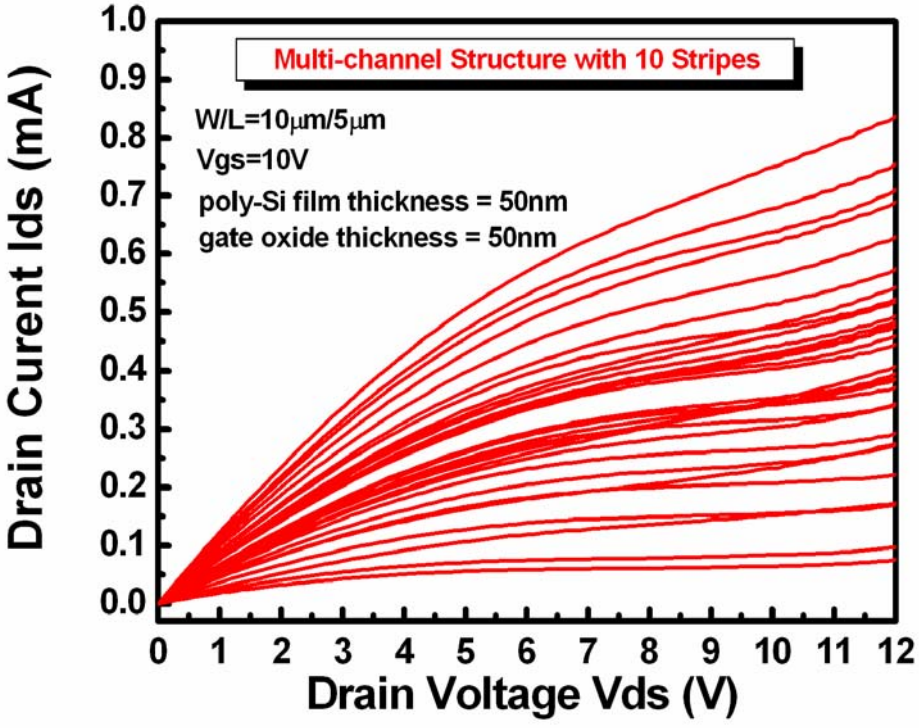
plotted. The distributed output characteristic of thirty low temperature poly-Si thin film transistors (W/L=10μm/5μm) with single channel structure, five poly strips, and ten poly strips are shown in Fig. 2-10(a)-2-10(c), respectively. From these figures, it is observed that the on current of the multi-channel devices are slightly larger than the single channel devices. However, the device-to-device non-uniformity in multi-channel TFTs seems not to be improved obviously compared with the single channel structure.



(a)


Multi-channel Structure with 5 Stripes
W/L=10μm/5μm
Vgs=10V
Si film thickness=50nm
gate oxide thickness=50nm
Drain Curent Ids (mA)
Drain Voltage Vds (V)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
0 1 2 3 4 5 6 7 8 9 10 11 12

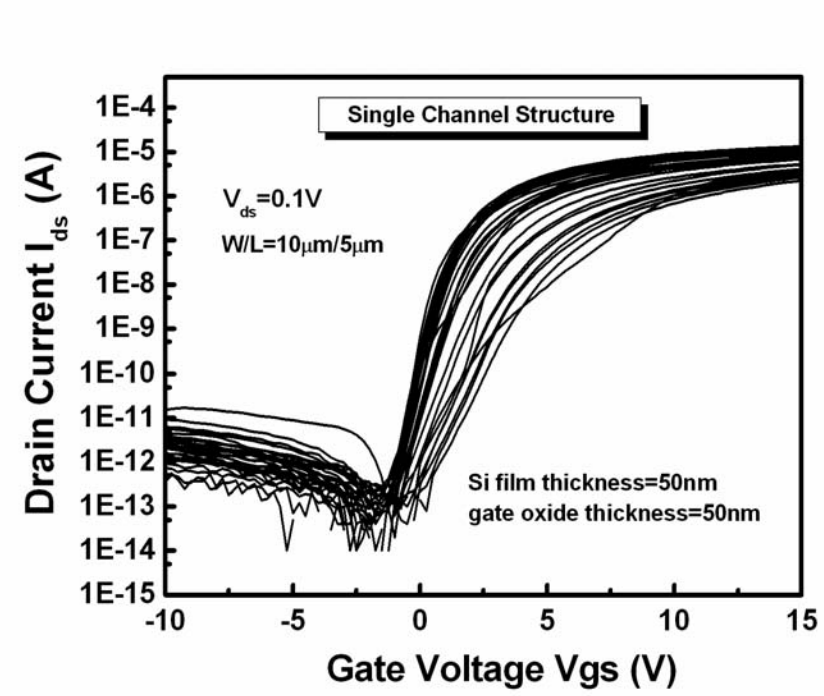
(b)


Multi-channel Structure with 10 Stripes
W/L=10μm/5μm
Vgs=10V
poly-Si film thickness = 50nm
gate oxide thickness = 50nm
Drain Curent Ids (mA)
Drain Voltage Vds (V)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
0 1 2 3 4 5 6 7 8 9 10 11 12

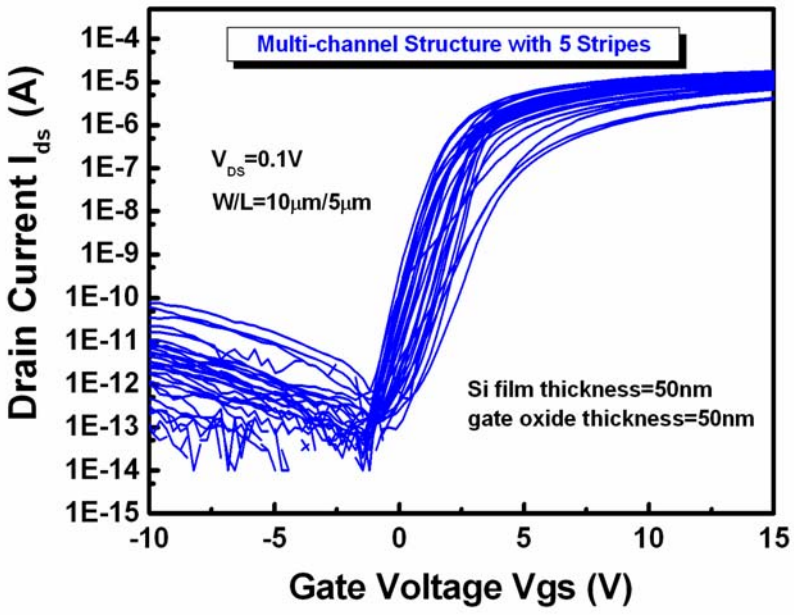
(c)

Fig. 2-10. Output characteristics of thirty LTPS TFTs at Vgs=10V in (a) single channel devices, (b) multi-channel devices with five stripes, and (c) multi-channel devices with ten stripes.

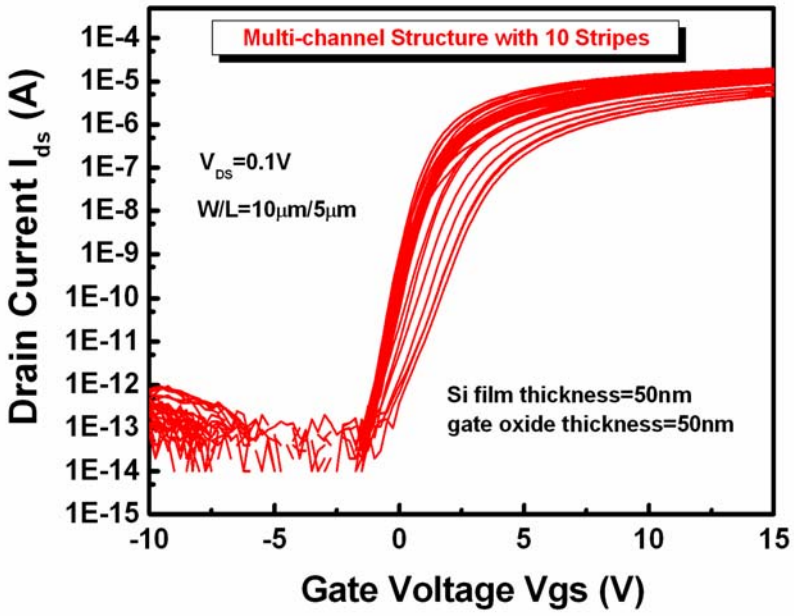
On the other hand, the transfer characteristics of thirty LTPS TFTs show much information about device electrical performances which are shown in Fig. 2-11(a)-2-11(c). It is clear that the distribution of sub-threshold swing is more uniform with the increasing channel stripes. Nevertheless, the distributed threshold voltages are more uniformed in multi-channel structures especially in ten stripes. Comparatively, the on current and leakage current are both almost on a par distributed in the single channel and multi-channel devices.



(a)



(b)



(c)

Fig. 2-11. Transfer characteristics of thirty LTPS TFTs at V_{ds} = 0.1 V in (a) single channel devices, (b) multi-channel devices with five stripes, and (c) multi-channel devices with ten stripes.

In order to further investigate the correlation between the electrical performance statistics and multi-channel effect, the cumulative probability distribution of three main electrical parameters, including the threshold voltage (Vth), sub-threshold swing (SS), and transconductance (gm) are shown in Fig. 2-12 to Fig. 2-17. Fig. 2-12 to Fig. 2-14 shows the threshold voltage, sub-threshold swing, and transconductance in W/L=10μm/5μm LTPS TFTs, respectively. It is obvious that the single channel devices suffer larger variations in threshold voltage and sub-threshold swing compared with multi-channel devices, however, the distribution of transconductance did not show the same information. This means that there are still large variations existing in transconductance even in multi-channel structure with slicing layout method employed. Fig. 2-15 to Fig. 2-17 also shows the same critical parameters distribution in 200μm/5μm devices. These figures reveal the same trend both in the 10μm/5μm and 200μm/5μm dimension. In this experiment, the slicing layout with ten stripes suffers from the minimum device-to-device variations especially in threshold voltage and sub-threshold swing. It proves the multi-channel structure can reduce the non-uniform electrical characteristics of LTPS-TFTs effectively. The data of cumulative distributions are summarized in Table 2-1. It is clear that threshold voltage and sub-threshold swing variations are reduced employing multi-channel structure either 10μm/5μm or 200μm/5μm dimension.

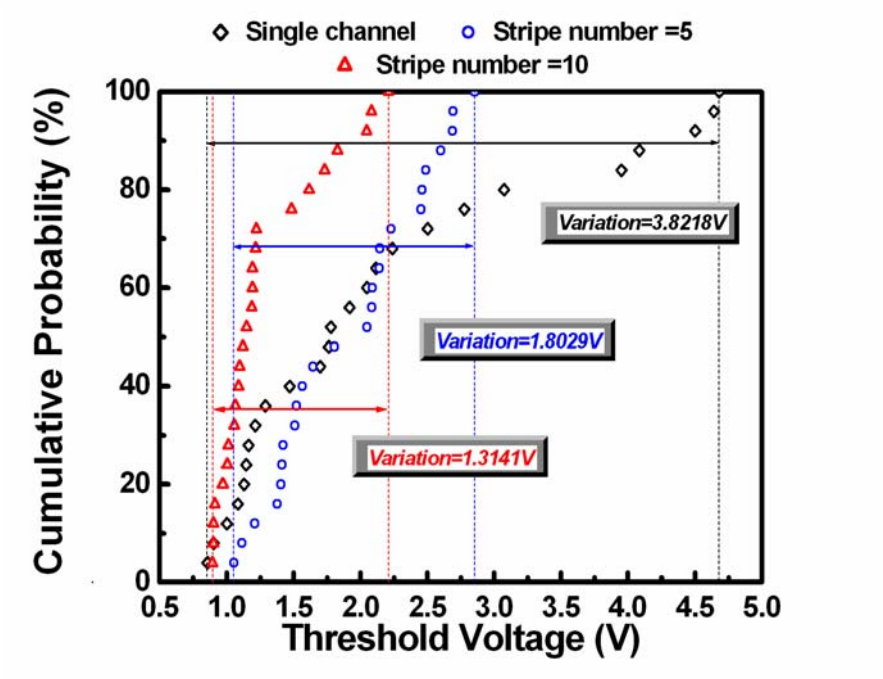


Fig. 2-12. The comparison of cumulative distributions for the threshold voltage from twenty-five n type LTPS-TFTS (W/L=10μm/5μm) in single channel structure and multi-channel structure.

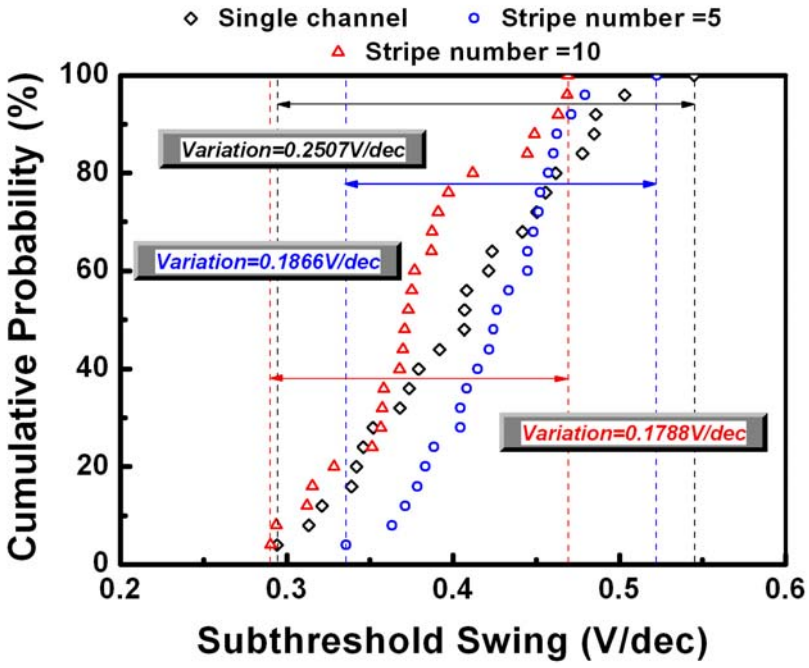


Fig. 2-13. The comparison of cumulative distributions for the sub-threshold swing from twenty-five n type LTPS-TFTS (W/L=10μm/5μm) in single channel structure and multi-channel structure.

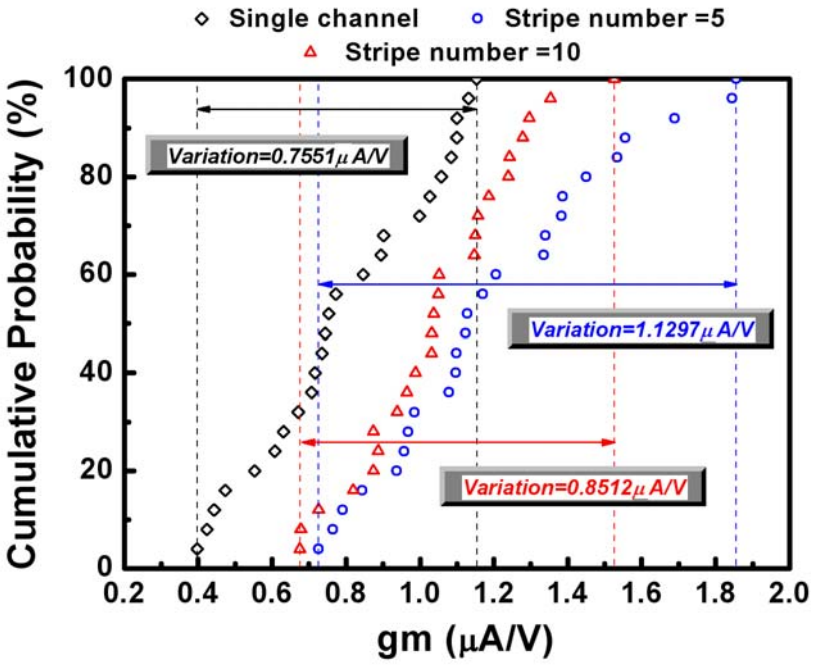


Fig. 2-14. The comparison of cumulative distributions for the transconductance from twenty-five n type LTPS-TFTS (W/L=10μm/5μm) in single channel structure and multi-channel structure.

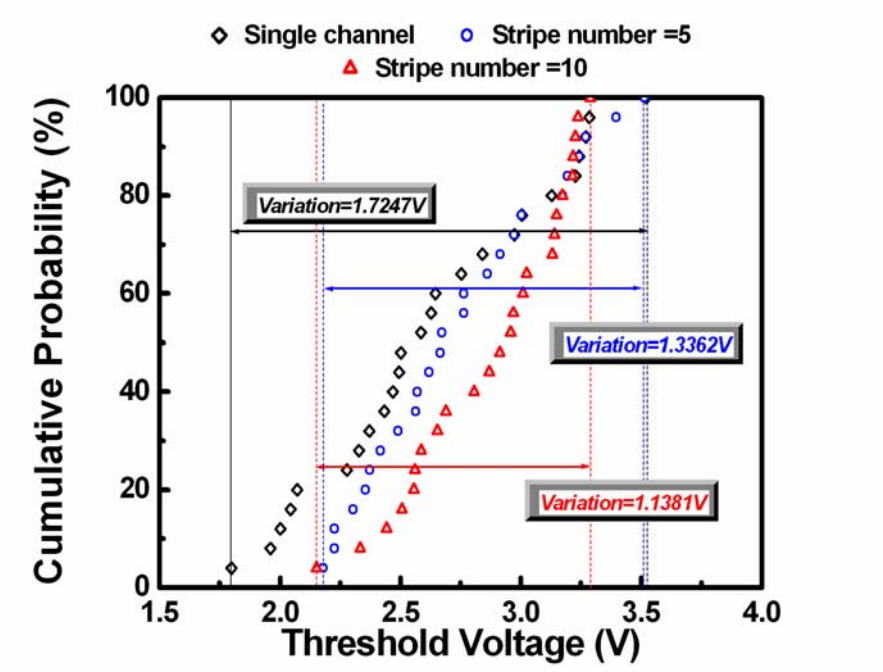


Fig. 2-15. The comparison of cumulative distributions for the threshold voltage from twenty-five n type LTPS-TFTS (W/L=200μm/5μm) in single channel structure and multi-channel structure.

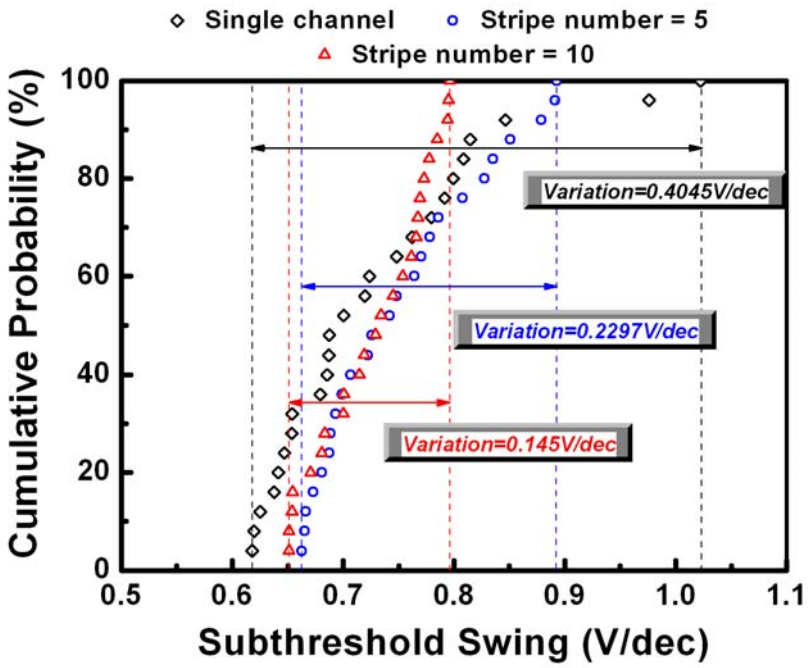


Fig. 2-16. The comparison of cumulative distributions for the sub-threshold swing from twenty-five n type LTPS-TFTS (W/L=200μm/5μm) in single channel structure and multi-channel structure.

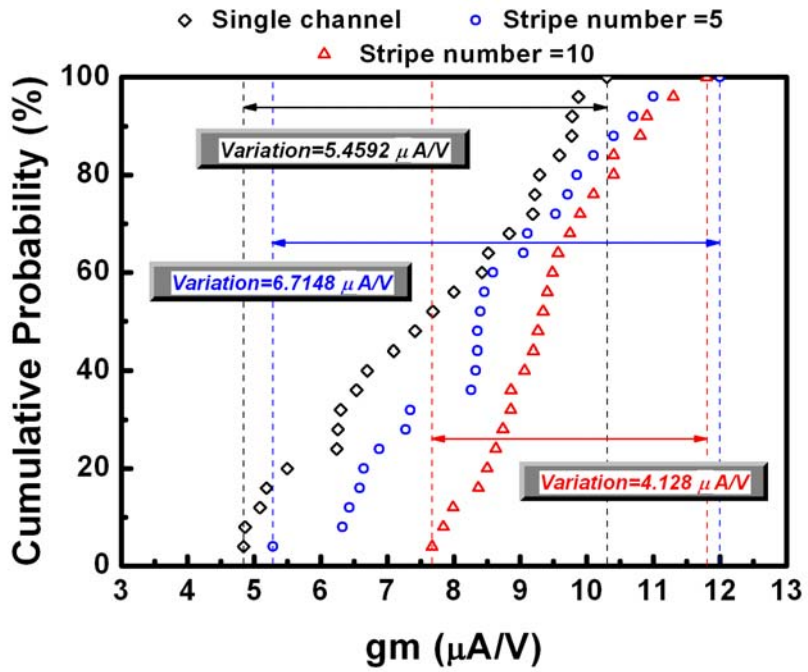


Fig. 2-17. The comparison of cumulative distributions for the transconductance from twenty-five n type LTPS-TFTS (W/L=200μm/5μm) in single channel structure and multi-channel structure.

Structure		Single channel	Multi-channel	
Stripe number		1	5	10
W=10 μm	Threshold voltage variation (V)	3.8217	1.8029	1.3141
	Sub-threshold swing variation (V/dec)	0.2507	0.1866	0.1788
	Ion variation ratio (at Vgs=10V, Vds=8V)	2.11	1.66	1.69
W=200 μm	Threshold voltage variation (V)	1.7247	1.3362	1.3181
	Sub-threshold swing variation (V/dec)	0.4045	0.2297	0.145
	Ion variation ratio (at Vgs=10V, Vds=8V)	2.54	1.70	1.45

Table 2-1. Comparisons of electrical characteristics between single channel structure and multi-channel in W=10μm and W=200μm.

2.4 Discussions of the Improved Uniformity Mechanisms between the Conventional and Multi-channel Structures

From the previous experimental results, it shows that the uniformity of the threshold voltage and sub-threshold swing can be improved in multi-channel structure of LTPS TFTs while that of transconductance is not. In the section, the mechanisms of multi-channel structure on device uniformity of LTPS TFTs will be discussed. In the following parts, three possible mechanisms influencing the device uniformity are listed and proposed to explain phenomena including effective tri-gate structure, passivation effect, and probability effect.

- **Effective tri-gate structure :**

Several researches have been reported that the multi-channel structure possess an effective tri-gate result in nano-scale which is shown in Fig. 2-18 [2.5], [2.8]. Besides, TFTs with multiple channels not only enhance gate control capability but also increase the sidewall channel width effectively. In our design, however, the smallest stripe is 1μm accompanying with 500Å gate oxide which only has limited effective tri-gate result. As a result, the effective tri-gate structure phenomenon is considered not the dominant factor in our experiment.

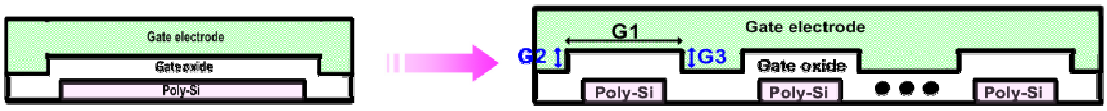


Fig. 2-18. Cross-section view of the multi-channel structure.

- **Passivation effect :**

The passivation is an important process step during the fabrication of LTPS TFTs, since it can passivate the traps or defects in grain boundaries and poly-Si/oxide interface. It has also been verified that the hydrogenation passivation treatment can improve the uniformity of TFT characteristics significantly for the reduction of the defect density in the poly-Si thin film in 2003 [2.20]. Defect traps have great impacts on the device performance. Threshold voltage and sub-threshold swing are affected by deep state which is also called inter-grain defects, while the field-effect mobility and leakage current are influenced by tail states also called intra-grain defects [2.14]. Because the thin film transistors with multi-channel structure can enhance the passivation efficiency, it can greatly reduce the device variation. However, there is no plasma treatment during fabrication process. As a result, the passivation effect is excluded from the reason of improving uniformity in our devices.

- **Grain distribution effect :**

So far, there are no reports mentioning about this reason. Nevertheless, this mechanism is the dominant factor in our experiment. For excimer laser crystallized LTPS TFTs, the non-uniform pulse-to-pulse energy density causes the non-uniform grain size distribution due to its nature grain growth mechanism. The random grain size distribution is the major issue of huge variations in electrical characteristics.

According to the possible grain related to device location, the possible figure is shown in Fig. 2-19. In Fig. 2-19(a), single channel device maybe locates in different position A and B. Taking position A for example, the device locates in many tiny grains, the threshold voltage and sub-threshold swing must be degraded and its value will be higher. While in device B situation, the device locates in larger grains, the electrical performance must be raised which means the threshold voltage and sub-threshold swing are lowered. Compared with these two devices, the electrical performance suffers huge variations due to the varied grain distribution.

As for the multi-channel devices in the same location, the situation becomes Fig. 2-19(b). Active region of device A shifts to larger grains, while that of device B is added more smaller grains. Consequently, the difference of grain and grain boundary numbers between two devices will be minimized. In the grain boundary, the dangling bonds existing in deep states strongly affect the threshold voltage and sub-threshold swing of poly-Si TFTs. Due to the minimized variation of grain boundary numbers causing from larger area in multi-channel structures, the threshold voltage and sub-threshold swing difference between multi-channel structures will be reduced which is consistent with experimental results. On the other hand, the strain bonds existing in the tail states dominate the leakage current and field-effect mobility. In previously description, the grain and grain boundary numbers will be closed in multi-channel structure. The numbers of tail states in per unit device area of multi-channel structure are almost the same as the single channel structure. Therefore,

there are still large variations existing in multi-channel devices compared with single channel devices. In conclusion, the multi-channel structure with slicing layout method can reduce the variations of deep states effectively but can not eliminate the tail states. The major advantage is that the differences of threshold voltage and sub-threshold swing between multi-channel structures will be reduced.

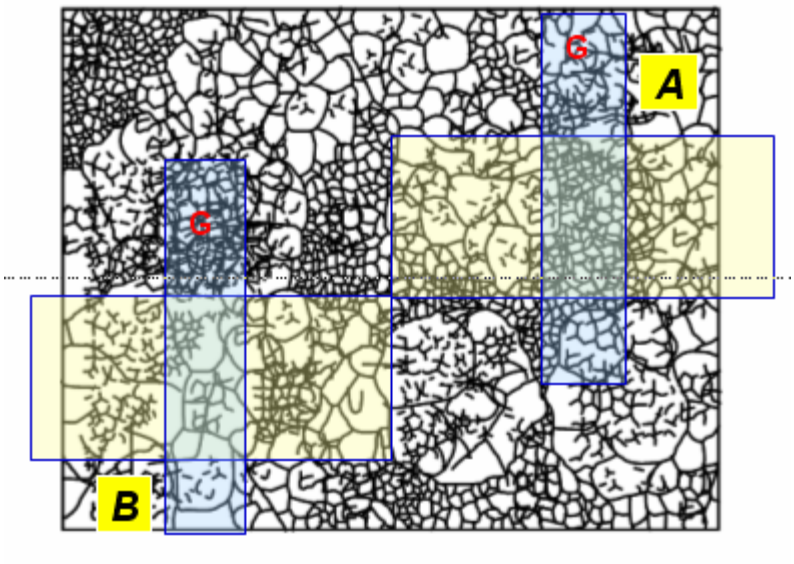


Fig. 2-19.(a) Probable distribution of relative location between devices and grains in single channel structure.

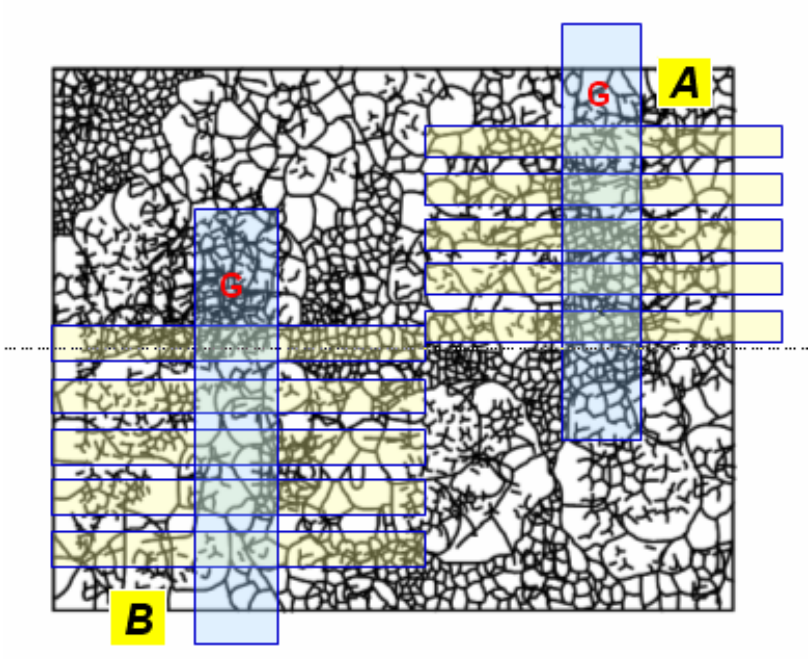


Fig. 2-19.(b) Probable distribution of relative location between devices and grains in

multi-channel structure.

2.5 Summary

In this chapter, a variety of closely spaced arrays of nominally identical devices were manufactured with various geometries. The matching properties of LTPS TFTs have been measured and analyzed. It is observed that interdigitated arrangement have better tolerance than parallel arrangement and perpendicular arrangement in electrical data statistically of matching TFTs. The uniformity in the multi-channel structure of low-temperature polycrystalline silicon thin film transistors has been proved to be superior to the single channel, especially in the threshold voltage and sub-threshold swing. Only layout method must be modified without changing the original process. The cumulative probability distributions are also summarized to verify its uniformity.

The uniformity of the threshold voltage and sub-threshold swing in the multi-channel structure of low-temperature polycrystalline silicon thin film transistors has been proved to be superior to the single channel. Besides, the properties variations of mobility (μ) and leakage current (Ioff) still remain since the numbers of tail states in per unit device area of multi-channel structure are almost the same as the single channel structure.

Three possible mechanisms influencing uniformity of devices have been discussed to explain the phenomena, which are effective tri-gate structure, passivation effect, and grain distribution effect. Among these possible mechanisms, grain distribution effect is considered to be the dominate factor in our experiment. The major advantages are that the threshold voltage and sub-threshold swing difference between multi-channel devices will be reduced, which is beneficial in whole panel uniformity.