Chapter 3

Evaluated Results of Conventional Pixel Circuit, Other Compensation Circuits and Proposed Pixel Circuits for Active Matrix Organic Light Emitting Diodes (AMOLEDs)

3.1 Introduction

Organic light emitting diode displays can be classified into passive matrix (PMOLED) or active matrix (AMOLED) based on its driving method. Passive matrix has some drawbacks such as higher power consumption and shorter lifetime [3.1]-[3.2], particularly in the large panel size. On the contrary, active matrix backplane is suitable for the high quality and high definition displays, especially for the television applications. Besides, using low-temperature polycrystalline silicon thin film transistors (LTPS TFTs) is better than amorphous silicon thin film transistors (a-Si TFTs) for the high resolution displays due to the superiorities of integrating the peripheral electronics, low power consumption and low fabrication cost (in smaller panel applications). In the active matrix driving scheme, two thin film transistors and one storage capacitor in each pixel are employed to achieve the continuous

illumination throughout the entire frame time and the current flow through driving transistors is used to control different gray scales of the display brightness [3.3]. However, the device-to-device variations in LTPS TFT's due to the diverse process fabrication bring about the diversity of the gray scale and the uneven colors. As for this reason, a lot of compensated circuits are proposed to solve this problem.

All the pixel circuits for active matrix organic light emitting diodes are categorized into digital driving, analog driving, and novel driving methods [3.4]-[3.14]. Digital driving method can provide precise color reproduction because each OLED device is controlled by an independent switch, but its applications are only suitable for the small size and low resolution panels. As implied by the name, the analog driving applies analog voltage or current signals to pixels as the data. The advantages of analog driving are effective for high resolution panels and higher yield rate than digital driving.

In this chapter, dimensional effects of transistors and storage capacitor in the conventional pixel circuit were simulated, the transistor slicing method with multi-channel structure are used to enhance uniformity. Digital driving circuits include area ratio gray scale method (ARG) [3.15] and time ratio gray scale method (TRG) [3.16] for obtaining different gray scales while analog driving circuits are divided into voltage programmed circuits [3.17] and current programmed circuits [3.18] based on the applied input signals. The advantages and disadvantages of these driving methods will be investigated in detail in the following sections.

Dimensional effects of typical pixel circuit for AMOLED including one switching TFT, one driving TFT, and one storage capacitor which shown in Fig. 3-1 will be discussed in detail. When the scan line is selected, the switching TFT1 is turned on and transfer the data voltage to the gate node of the driving TFT2, and the storage capacitor Cs is also charged at the same time. After the switching TFT1 is

turned off, the charged storage capacitor Cs is kept the original signal and supply the driving TFT2 the constant current to light OLED.

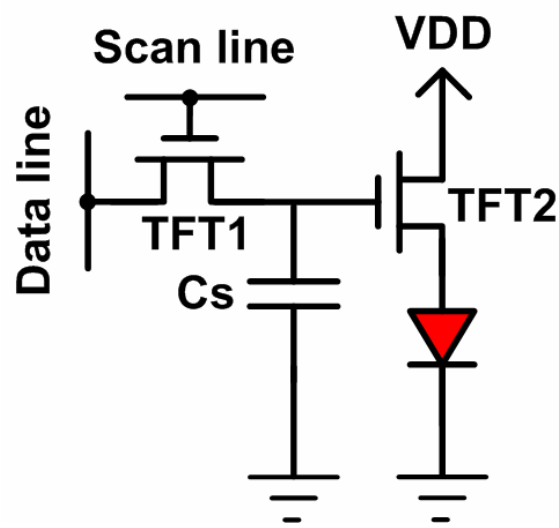


Fig. 3-1. Typical N-type LTPS TFT pixel circuit for AMOLED.

Voltage compensation pixel circuits are more attractive since poly-Si TFT data drivers, which are compatible with LCD data drivers, can be integrated on the display panel to decrease the module cost and increase the panel reliability. Many voltage programming were reported in this chapter with complex configurations and driving signals. However, simpler pixel circuit is favored for high resolution and system on panel realization.

In this chapter, to overcome the problems caused by spatially non-uniform characteristics between thin film transistors across the panel, two new pixel circuit designs for active matrix organic light emitting diodes based on the low-temperature polycrystalline silicon thin-film transistors were proposed and verified by SPICE simulation. Diode connection concept was adopted in these compensation circuits with threshold voltage compensation. The pixel circuits consisting of five TFTs, one additional control signal, and one storage capacitor were used to enhance the image uniformity of the display.

3.2 Simulation Results of Dimensional Effects on Transistors and Storage Capacitor in Conventional Pixel Circuit

First of all, the typical current versus voltage curve of OLED's and the electrical characteristics of LTPS TFT's such as transfer characteristic must be fabricated and obtained to start the whole pixel design. BSIMpro v2 was used to extract the OLED and TFT parameters providing for pixel circuit simulation. The LTPS TFT simulation model is represented by RPI parameters (LEVEL 62), and the used simulator is HSPICE. The OLED emission area is assumed 60μm x 220μm which is roughly corresponding to four inch QVGA specification.

Fig. 3-2 and Fig. 3-3 shows the measured and simulated from extraction results of OLED's I-V curve ranged from 0-10V and the transfer characteristics of n channel LTPS TFT (8μm/8μm), respectively. Each of them both has good fitting results from these two figures.

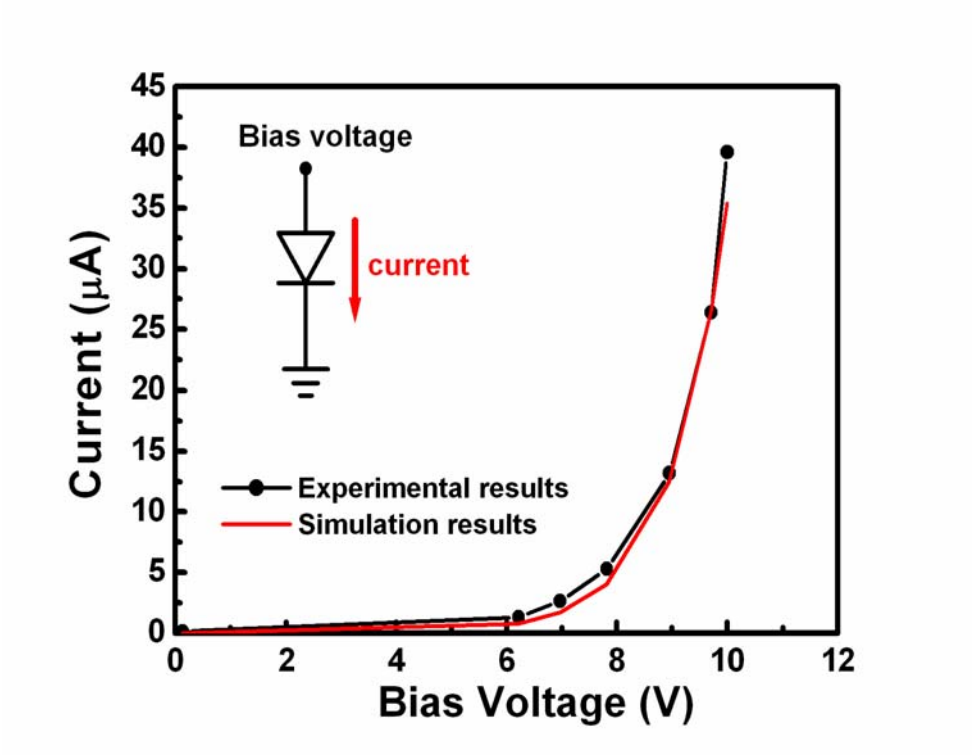


Fig. 3-2. The measured and simulation result of OLED's current versus bias voltage characteristics.

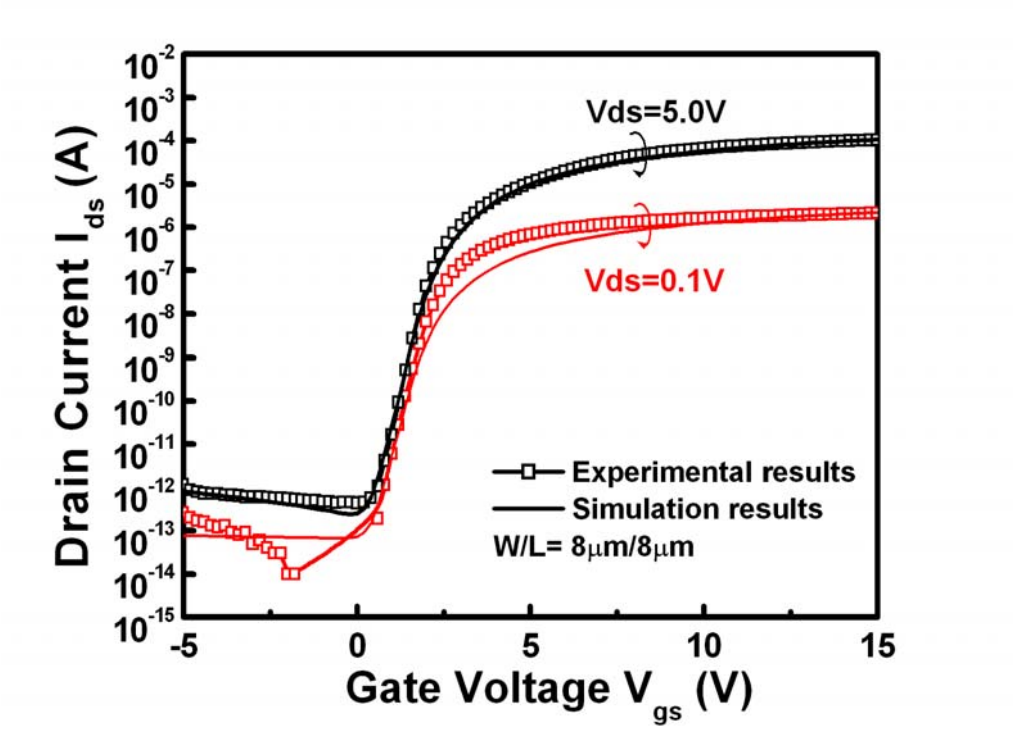


Fig. 3-3. The measured and simulation results of n type LTPS TFT's transfer characteristics.

3.2.1 The Effect of Switching TFT

Three different dimensions of switching TFT including W/L = 10μm/10μm, 20μm/10μm, and 10μm/20μm are compared where the driving TFT is fixed at 100μm/10μm and the storage capacitor is 0.5pF in the conventional pixel circuit. In this case, the power supply (V_{DD}) is assumed 10V, and the scan line (V_{scan}) is a voltage pulse signal with peak value 10V and base value 0V. Fig. 3-4 shows the simulation results of different situations with varied switching TFT dimensions. Even though the largest W/L ratio reaches four times than smallest one in switching TFT dimension, there is no obvious difference between the anode voltages of OLED in the simulation results.

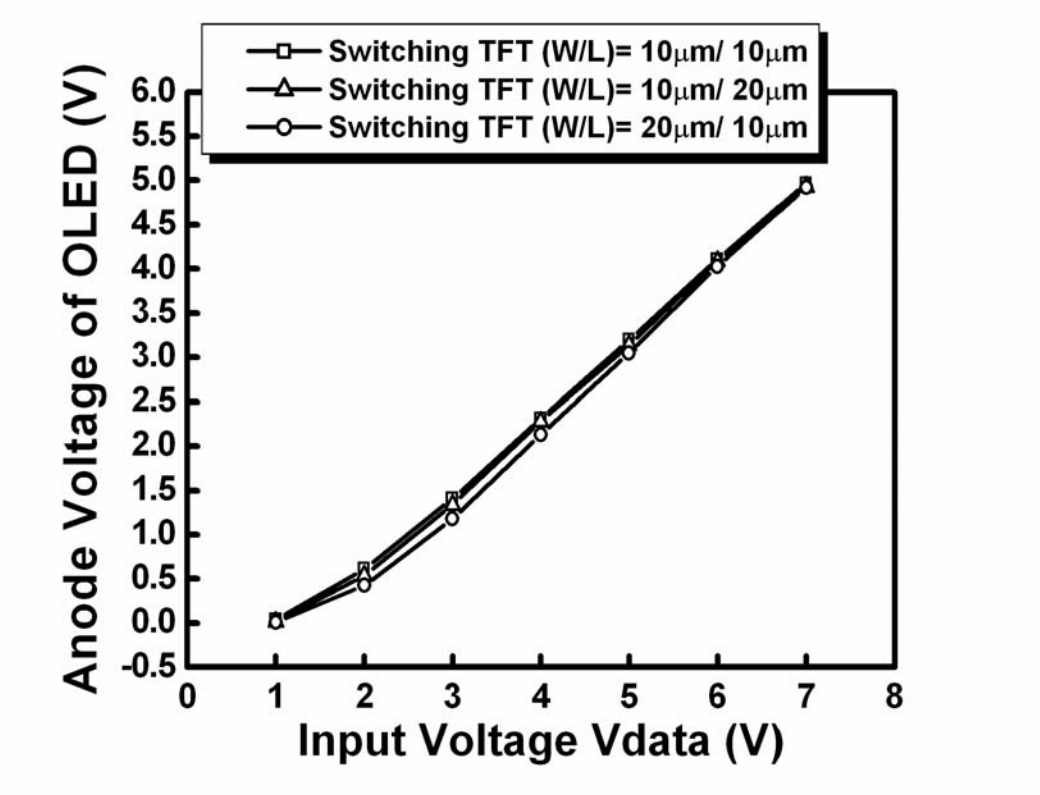


Fig. 3-4. The simulation results are compared with the varied switching TFT dimensions.

3.2.2 The Effect of Driving TFT

Three different dimensions of driving TFT including W/L = 10μm/10μm, 50μm/10μm, and 100μm/10μm are compared after fabrication where the switching TFT is fixed at 10μm/10μm and the capacitance of the storage capacitor is 0.5pF in the conventional pixel circuit. In this case, the power supply (V_{DD}) is assumed 10V, and the scan line (V_{scan}) is a voltage pulse signal with peak value 10V and base value 0V. Fig. 3-5 shows the comparison of simulation results with the varied driving TFT dimensions. From the simulation results, the anode voltage of OLED is a function of input voltages; it is also increased slightly with the size of driving TFT, which is more obvious in the experimental results. Nevertheless, it doesn't mean that the larger dimension the better it is, it must be depended on the panel specification to design the proper size.

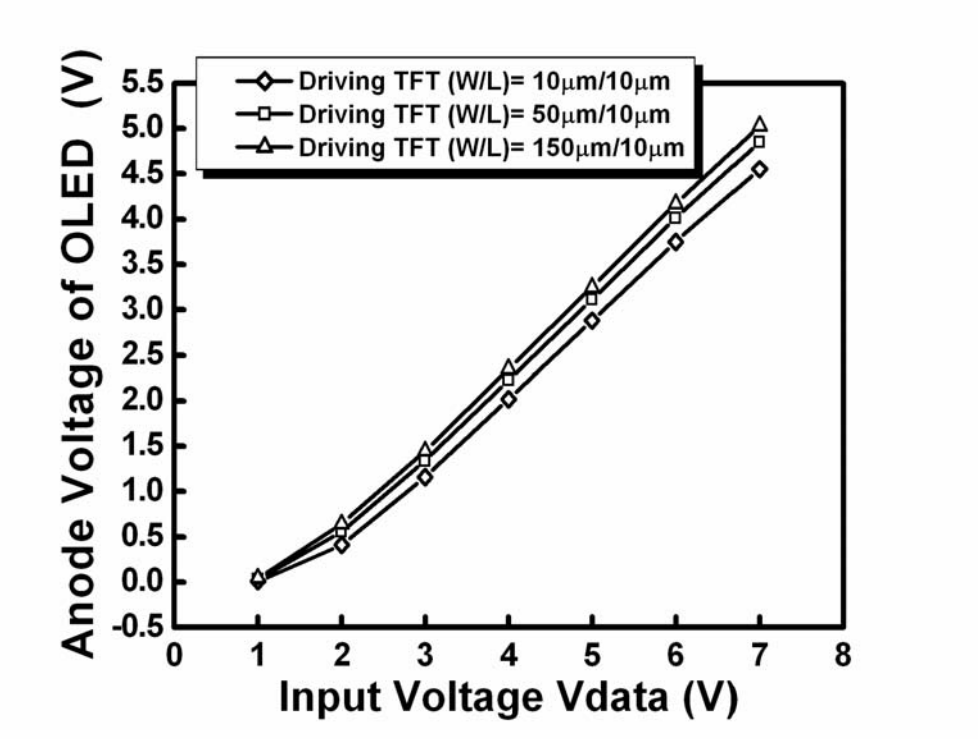


Fig. 3-5. The simulation results are compared with the varied driving TFT dimensions.

3.2.3 The Effect of Storage Capacitor

To study the effect of storage capacitor, two different storage capacitors including 0.1pF, and 2pF are compared after fabrication where the switching TFT is fixed at 10μm/10μm and the driving TFT is fixed at 100μm/10μm in the conventional pixel circuit. In this case, the power supply (V_{DD}) is assumed 10V, and the scan line (V_{scan}) is a voltage pulse signal with peak value 10V and base value 0V. Fig. 3-6 shows the simulated voltages stored in the capacitors with varied capacitances when the input data voltage= 5V. It is clear that small storage capacitor only needs short charging time from the inset; however, the large storage capacitor retains the data voltage well which means good holding capability. The proper storage capacitor is also decided by the panel specifications such as resolution, gray scale, and so on.

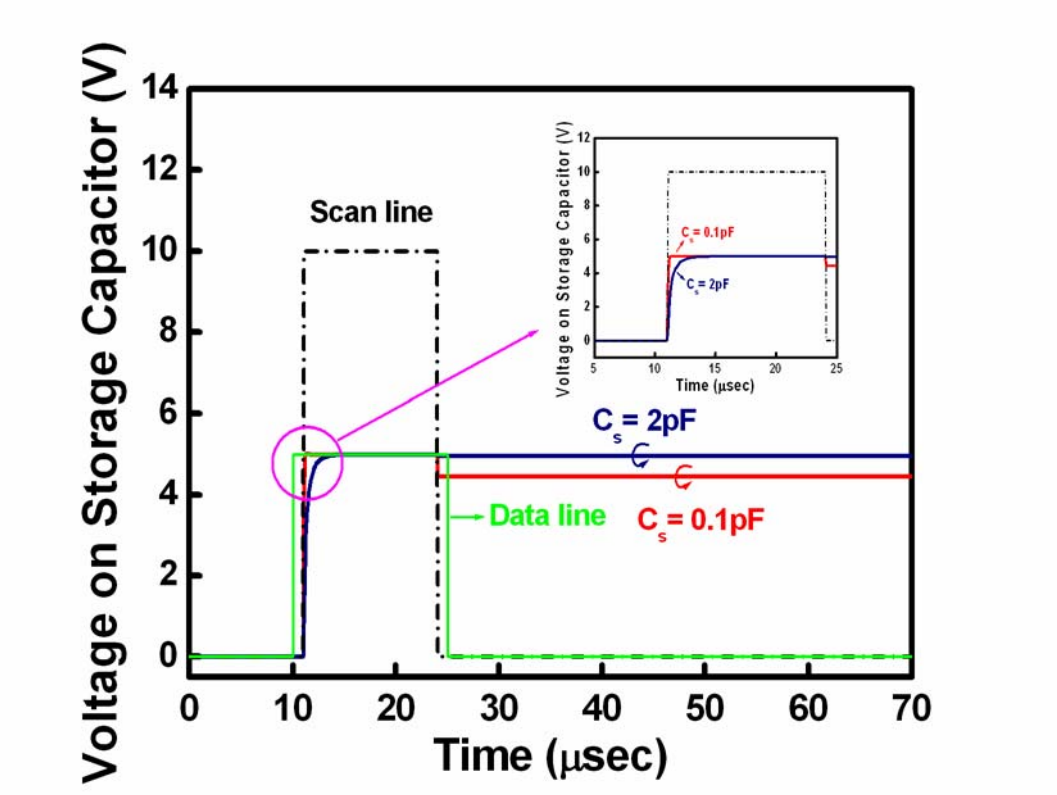


Fig. 3-6. The simulated voltages stored in the capacitors with varied capacitances when the input data voltage= 5V.

3.2.4 The Effect of Transistor Slicing Layout

Due to the previous investigation in chapter 2, multi-channel structure is used to improve uniformity of transistors which can enhance high display quality. In this section, the slicing layout referred to multi-channel structure is applied to the driving TFT. Fig. 3-7 shows the comparison of the slicing method effect in simulation and measured results of OLED anode voltages versus input data voltage ranges 1V to 6V. It shows the OLED anode voltage enhanced which represents higher current driving capability of driving TFT with transistor slicing layout is. As for simulation results, Monte Carlo simulation with an assumption of normal distribution was executed to examine the effects of device variations. The model typical parameter and the deviation value of the threshold voltage and mobility belonged to driving TFT are 1.55V, ± 1V, 52.02 cm^2/V-s, and ± 20 cm^2/V-s, respectively. In this experiment, ten smaller LTPS TFTs with each one 10μm/10μm stripe are used to replace a larger 100μm/10μm driving TFT. On the other hand, the results were calculated from ten testing pixel circuits. Definition of the non-uniformity here is the difference between the minimum output voltage and the maximum output voltage divided by the average output voltage. It can be seen that the non-uniformity can be reduced effectively from the conventional layout to slicing layout in Fig. 3-8. Since slicing layout can promote the output current and improve the uniformity for the LTPS TFTs, non-uniformity problem in the circuit can be slightly released.

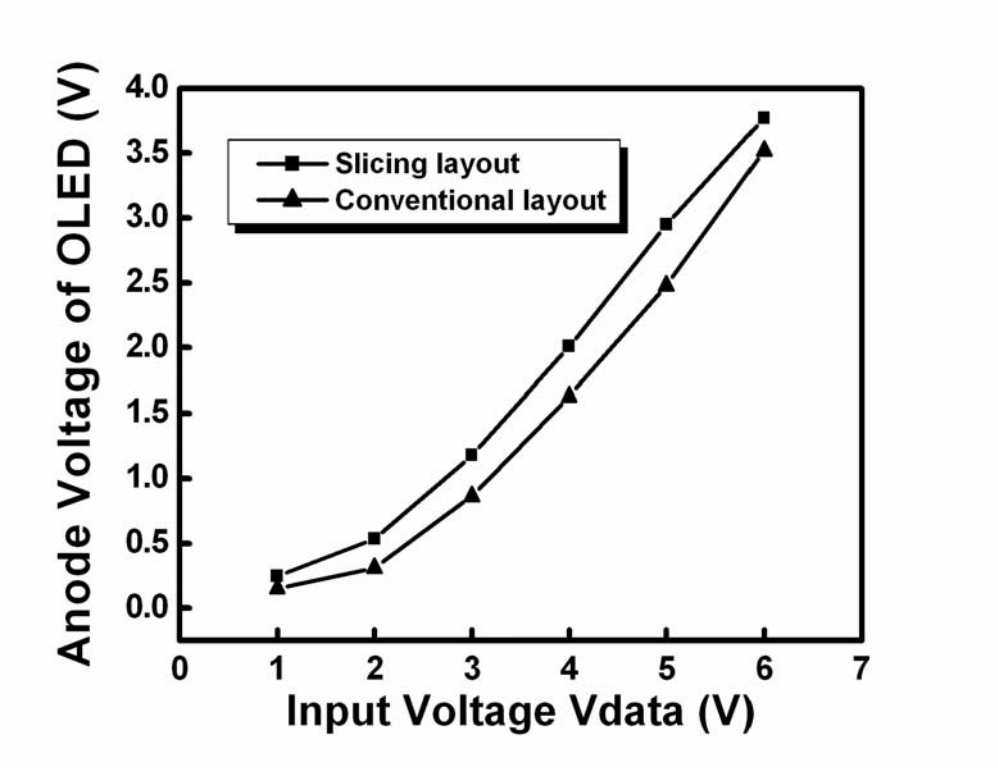


Fig. 3-7. Comparison of the slicing method effect in simulation and measured results of OLED anode voltages versus input data voltage ranges 1V to 6V.

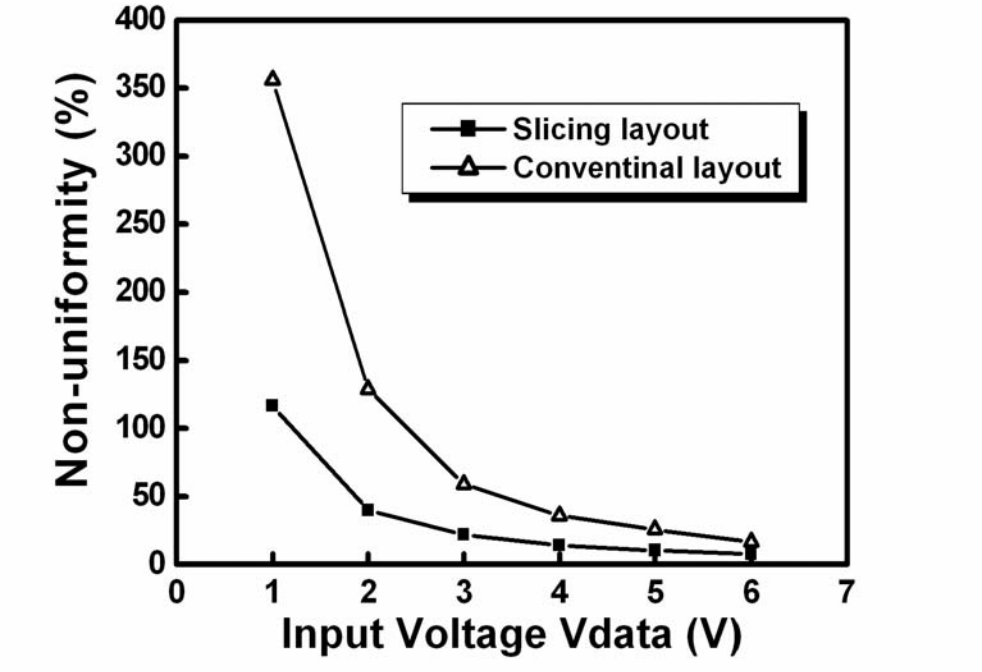


Fig. 3-8. Comparison of the slicing method effect in simulation and measured results of non-uniformity versus input data voltage ranges 1V to 6V.

3.3 Digital Driving Circuits

Although the slicing method of TFTs can reduce the non-uniformity effectively, it still hardly achieves the requirement of the high end applications such as high image quality. Instead of device structures, materials, processes, more and more methods were developed towards driving manners which can be categorized into digital driving, analog driving, and novel driving methods.

As implied in the name, digital driving means that the driving transistor is operated in the digital mode, either in the on state or off state. More uniform brightness image with the full digital operation can be achieved since the image uniformity is almost not affected by the varied electrical characteristics of transistors. It includes area ratio gray scale method and time ratio gray scale method.

3.3.1 Area Ratio Gray Scale Method (ARG)

Fig. 3-9 shows a single pixel circuitry of area ratio gray scale method, which area is divided into plural sub-pixels [3.4], [3.19]. Each sub-pixel is controlled either in the completely on state or complete off state, deviation of the transistors can be compensated at the same time. In this manner, binary area ratio was used, the area ratio of the sub-pixels is $2^0 : 2^1 : 2^2 : \cdot\ \cdot : 2^{n-1}$ and the brightness is proportional to the area of the sub-pixel when they are in the on state. For instance, there are two sub-pixels, 2^2=4 gray scales are obtained. In addition to compensate the deviation of TFTs, it also eliminates the digital to analog converter in the peripheral circuits. So the circuit in full digital operation will be simpler and less power will be consumed.

However, this method is not suitable for high resolution displays which the pixel area is limited. It needs high-end process design rule to match up which is difficult for further improvement.

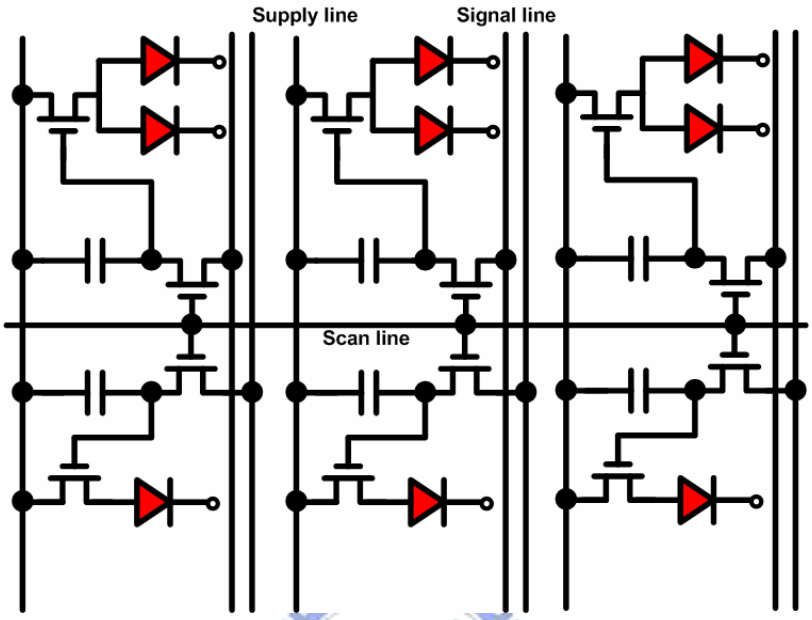


Fig. 3-9. Pixel circuitry of area ratio gray scale method.

3.3.2 Time Ratio Gray Scale Method (TRG)

As for time ratio gray scale method, each frame is separated into several sub frames and the brightness is controlled by adjusting the duration of lighting period. One frame of the 5-bit gray scales, for example, is divided into five sub frames as shown in Fig. 3-10. Each sub frame consists of an addressing period and lighting period [3.5], [3.16], [3.19]-[3.21]. In time ratio method, the gray scale is expressed whether the OLED is lighting or not. Each pixel takes either the bright state or dark state. The lighting period of each sub frame is established in a manner proportional to the exponential of factor 2 generally, which is 1 : 2 : 4 : 8 : 16. Consequently, 5-bit gray scale which refers to 32 gray scales can be acquired. The pixel circuit is the same as traditional two transistors and one capacitor structure, but a different point is the

driving TFT operation condition. Driving TFT works in saturation region in analog driving generally, but works in linear region in digital time ratio gray scale method. Therefore, the voltage between drain and source electrodes of driving TFT is very small so that the voltage applied to the OLED anode is quite equal [3.20].

Time ratio method also has trouble in high resolution display since it takes long time to charge the large OLED capacitance when the low gray scale is displayed [3.19]. In addition, it is needed to increase the number of sub-frames with higher power consumption inevitably.

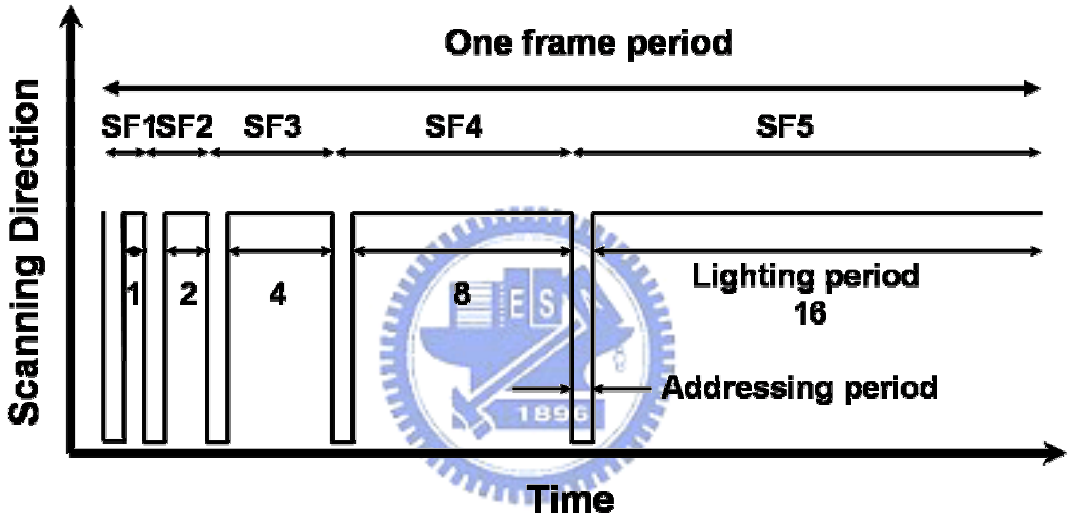


Fig. 3-10. Timing diagram of time ratio gray scale method.

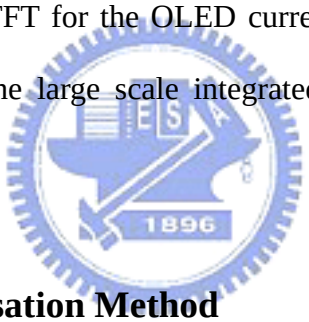
3.4 Simulation Results of Analog Driving Circuits

Due to analog driving method does not encounter the problems digital driving meets likes needing high addressing speed or high-end process design rule causing higher power consumption or complex processes for high resolution and high gray scale display. Hence, the voltage programming and current programming methods belonging to analog driving method are considered the future display applications. In the following sections, the voltage programming and current programming methods

are categorized and represented by several examples. The information of operation principle with each pixel circuit schematic and timing diagram is compared and discussed in detail.

3.4.1 Voltage Programming Circuits

Though voltage programming pixel circuits can only compensate the threshold voltage variations of the poly-Si TFTs, voltage programming pixel circuits are still more attractive for integration of driver on the same glass substrate. Driving configuration of voltage programming pixel circuits refers to data signal applying to the gate terminal of driving TFT for the OLED current. The principal advantage of this driving method is that the large scale integrated circuits (LSIs) of traditional driver for LCD are available.



3.4.1.1 Self-Compensation Method

Self-compensation method refers to compensate the threshold voltage variation of the driving TFT in the pixel circuit [3.22]-[3.24]. Driving steps are usually divided into three stages: First, reset the previous data voltage in the initialization period. Second, store the threshold voltage of driving transistors in the compensation period. Third, receive the data voltage in the data-input period. Fig.3-11 shows an example of self-compensation pixel circuit and the timing diagram [3.22]. In first stage, T2, T3, and T4 are turned on and the data signal is set to ground. Therefore, the gate voltage of T1 is initialized to ground at this stage. In the compensation period, Select 2 signal turns off the T4 and a compensation voltage is applied to the data line which stores

ΔV corresponding to threshold voltage of T1. Finally, Select 1 turns off T2 and T3 and only T4 is turned on, the data line is applied to the exact input data voltage. The gate voltage of T1 becomes the input data voltage plus threshold voltage solving the varied threshold voltage of driving transistors across the panel.

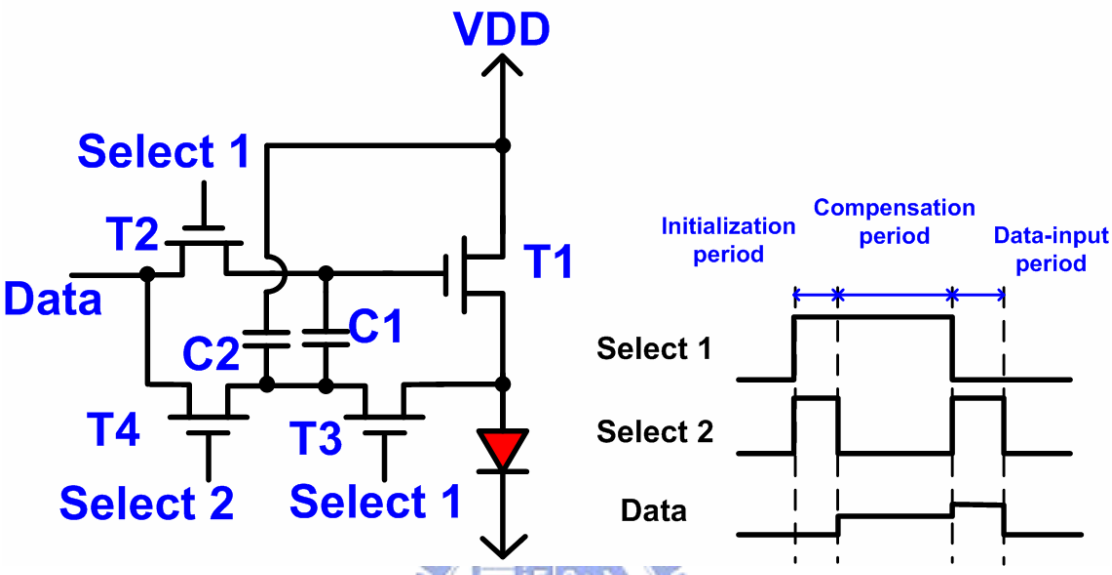


Fig. 3-11. An example of self-compensation pixel circuit and its timing diagram.

3.4.1.2 Matching TFTs Method

The initial assumption used in the matching TFTs method is that the electrical characteristics of neighboring TFTs are considered to be identical [3.25]-[3.26]. Fig. 3-12 shows a schematic diagram of matching transistors pixel circuit and its timing diagram. After the reset in the first period, the voltage of node A is higher than that of node B when inputs data voltage; and T3 turns on while T4 turns off. The data voltage from the node A is transferred to node B through T3 until node B becomes V_{data} - $|V_{th\_T3}|$, and the modulated data voltage is stored in C. This voltage would decide the current flow through OLED given by the following equation while driving transistor T2 is operated in the saturation region:

$$I_D = \frac{1}{2}k_2(V_{gs\_T2} + |V_{th\_T2}|)^2 = \frac{1}{2}k_2(V_{data} - |V_{th\_T3}| - V_{DD} + |V_{th\_T2}|)^2 = \frac{1}{2}k_2(V_{data} - V_{DD})^2,$$

$$(\text{if } |V_{th\_T3}| = |V_{th\_T2}|), \quad \text{where } k_2 = \mu C_{ox}\frac{W_2}{L_2} \text{ .....(3.1)}$$

From this equation, the drain current of T2 is independent of the threshold voltage of T2 with the threshold voltages of T2 and T3 are assumed to be identical. However, one major problem of this method is the low data voltage occurs when showing a low brightness picture. Since the low data voltage hardly turns on the diode-connected TFTs, which would be a limit for production.

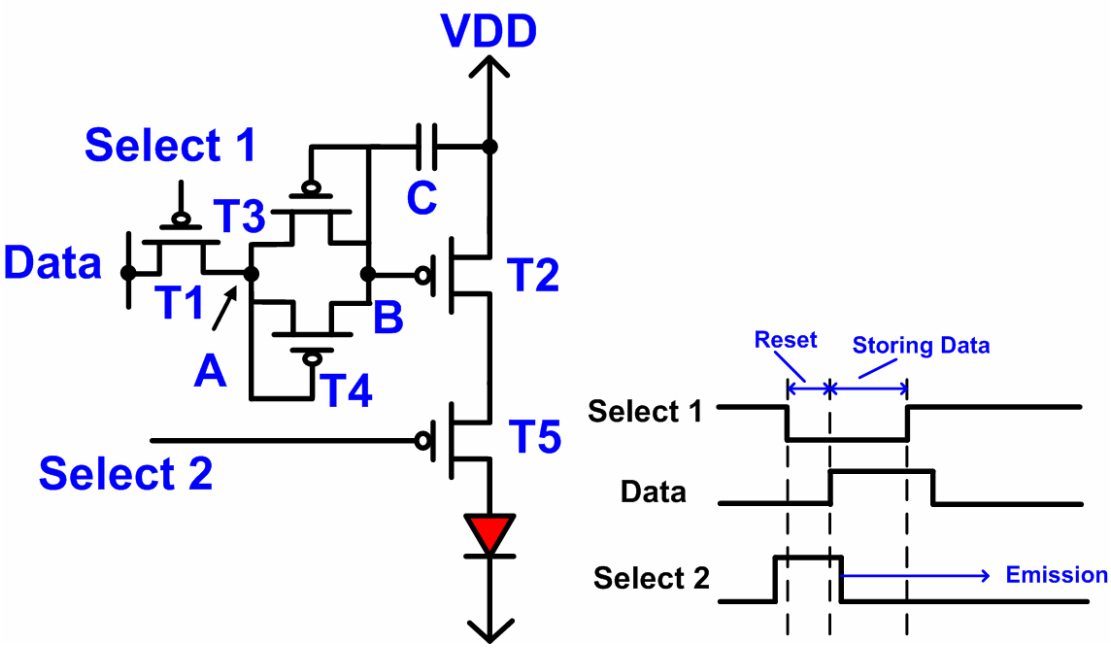


Fig. 3-12. An example of matching transistors pixel circuit and its timing diagram.

3.4.1.3 Resistance or Active Load Method

This method means compensation is executed by adding resistor [3.27] or active load [3.28] in the conventional pixel circuit. Fig. 3-13 shows an example of active load method pixel circuit. Besides switching transistor T1 and driving transistor T3, an active resistor T2 is added to this circuit. The driving scheme is the same as conventional pixel circuit. With the active load, the reduction in output current will be

responded by the voltage drop across it and a voltage increase at node A. As node A voltage increases, the drain to source voltage of T3 increases enhancing the output current of T3. This feedback phenomenon represents compensation for the initial output current decrease. Therefore, the output current level drifts induced by process variations or device aging can be reduced by adjusting operating point of the resistance or active load.

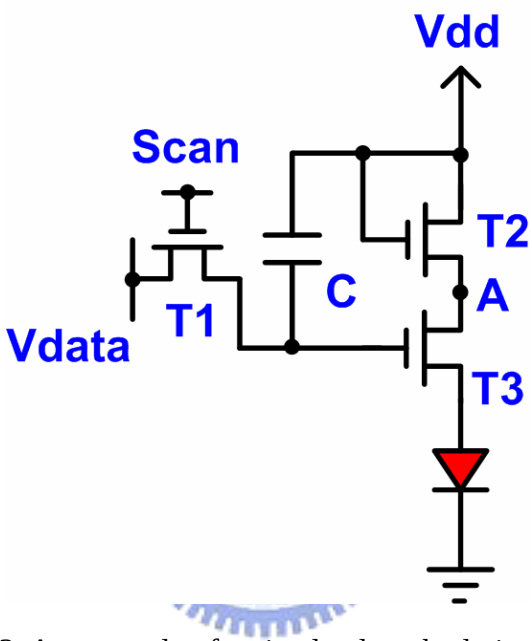


Fig. 3-13. An example of active load method pixel circuit.

3.4.1.4 Diode Connection Method

As for the diode connection method, the driving transistor is diode-connected while compensation period operates [3.29]-[3.33]. Fig. 3-14 (a) shows the gate terminal is connected to the resulting anode in an n-channel transistor, and the gate terminal is connected to the resulting cathode in a p-channel transistor. The Vt represents the nominal threshold voltage of transistors, and ΔVt stands for voltage difference of serial connection of voltage source. ΔVt is insensitive to the output current of OLED proved in the following diode-connected pixel circuit shown in Fig.

3-14 (b). The driving schemes are described as follows. In the first setup period, Select 1 signal goes high and Select 2 signal goes low, driving transistor T5 is diode-connected with a voltage Vt-ΔVt stored at node A. In the second pre-charge period, Select 1 signal and Select 2 signal go high, the voltage of node G is 0V. The voltage across the capacitor is charged to Vdd. In the third programming period, Select 1 signal goes high and Select 2 signal goes low, the capacitor C discharges until the G node voltage reaches Vdata-(Vt-ΔVt). Therefore, the G' node voltage equals Vdata-Vt regardless of the value of ΔVt. In the fourth display period, T5 acts as a constant current source independent of ΔVt and Vt values, and capacitor C retains the gate voltage of T5 during the frame time.

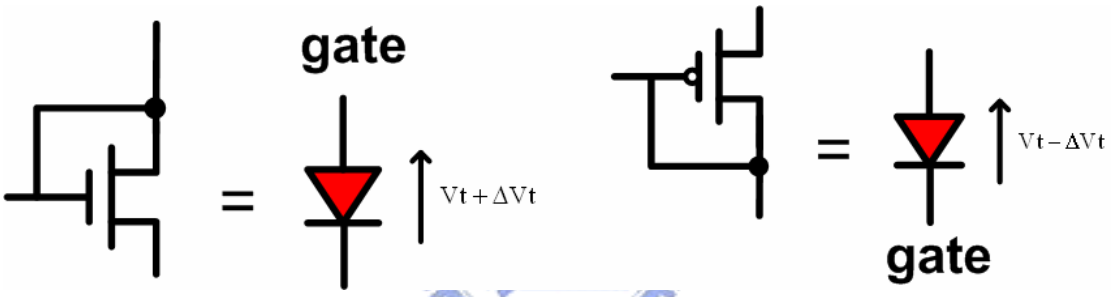


Fig. 3-14. (a) Diode connected transistors for n channel and p channel transistors.

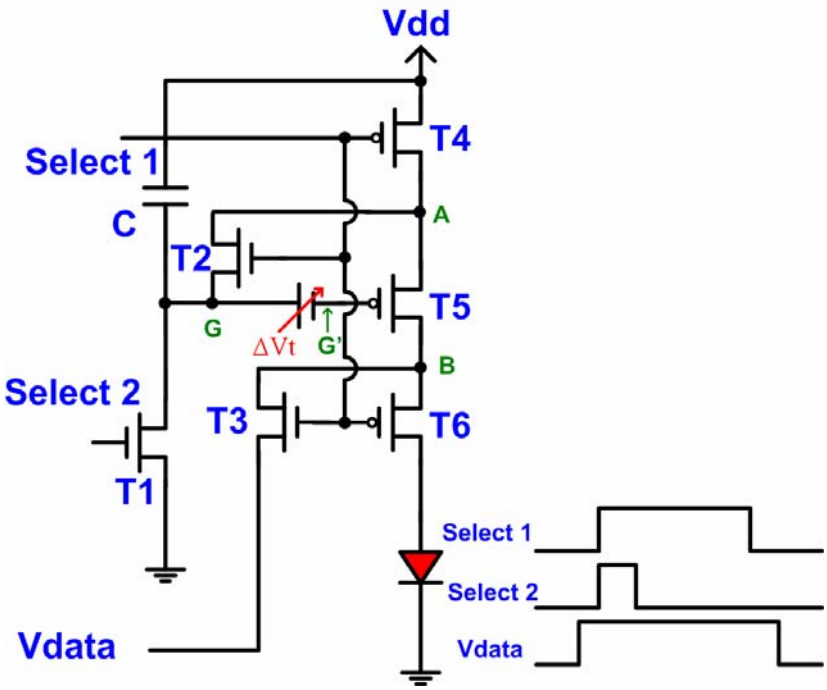


Fig. 3-14. (b) Example of diode-connected method pixel circuit.

3.4.1.5 AC Driving Method

The characteristic of OLED may be changed such as threshold voltage shift after long time operation and this would cause the non-uniform image. When OLED operates at constant driving current, the luminance and the efficiency will decay gradually. Some researches reported that reversed-bias can induce recovery phenomenon of degradation in OLEDs and improved the lifetime issue [3.34]-[3.37] which is shown in Fig. 3-15. The treatment of reverse bias improves the J-V characteristics and increases the energy efficiency. By means of an alternating cathode voltage of OLED, the voltage drop at the Vdd electrode caused by the parasitic resistance of the electrode can be compensated [3.37]. However, AC driving method does not take the variations between each transistor into consideration which is the biggest

problem.

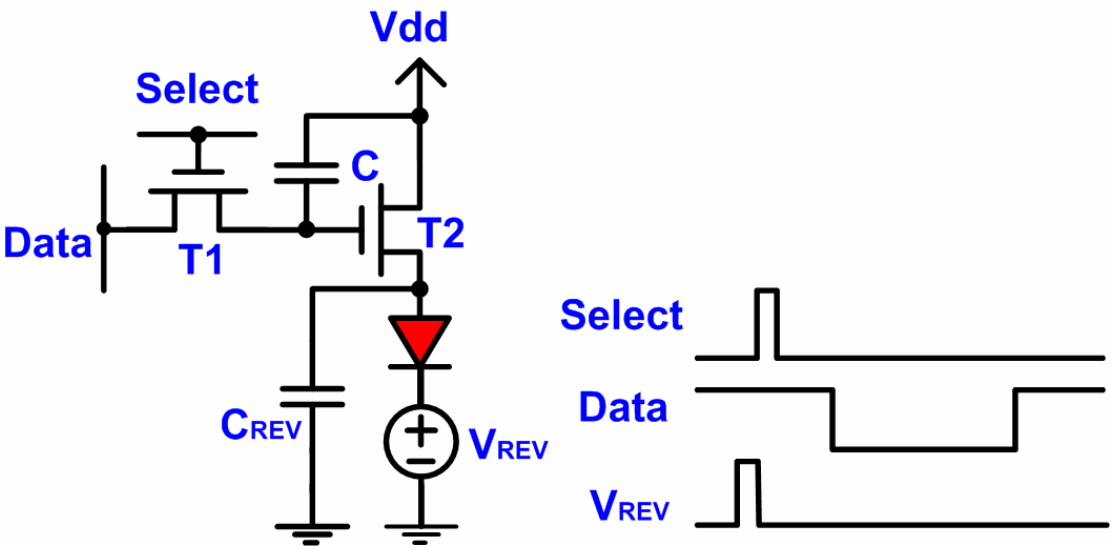


Fig. 3-15. An example of AC driving pixel circuit.

3.4.2 Current Programming Circuits

The current programming method generally applies current to the OLED as current data. If the current source delivers the uniform current in the frame time, the display performs uniform image. Compensating the threshold voltage and mobility variation of transistors at the same time is the major advantage of this method. The current programming method can be classified into current copy method and current mirror method which will be introduced as follows.

3.4.2.1 Current Copy Method

The current copy scheme and its timing diagram are shown in Fig. 3-16 [3.38]. In this schematic, programming the pixel is accomplished by turning off T4 by VGP line and turning on T1 and T2 by Scan line in the addressing time. The input programming current Idata flows through the diode-connection driving transistor T2 to set the pixel current. At this time, capacitor C stores the gate to source voltage of T3. The effects of variation in electrical performance of the driving TFT can be stored and will be cancelled during the following period. In the reproduction period, T1 and T2 are turned off and the pixel is connected to the power supply line V_{DD} through T4 for illumination. It is supposed to reproduce the value of data current because the capacitor C maintains the same gate to source voltage during the rest of the frame period. Hence, the programming current and the reproduction current has a linear relation. However, the charging time of the data line capacitive load is a big issue since the data current is only less than few μA and only one row time is available for programming. The slow charging time may cause this pixel circuit to fail in high

resolution displays.

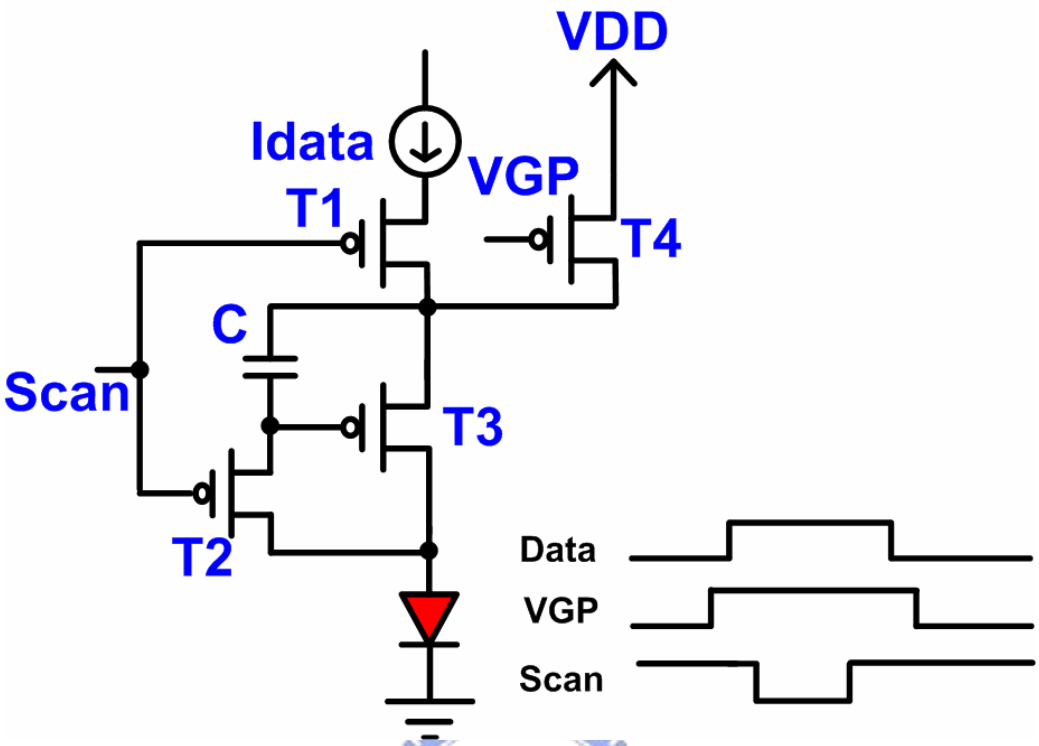


Fig. 3-16. Current copy pixel circuit and its timing diagram.

3.4.2.2 Current Mirror Method

An equivalent current mirror pixel circuit is proposed by Sony Corp. shown in Fig. 3-17 [3.39]. In the programming stage, both the Write scan and Erase scan are selected. The data current Idata is applied to the data line with T1 and T2 forming a current mirror structure. T3 acts as a switch; T4 operates for matching drain to source current of T1 to Idata and C stores the corresponding voltage. T2 isolates OLED during the data writing process, and drives the OLED based on the stored capacitor voltage during illumination. By designing larger W/L ratio of T1 compared to T2, Idata is larger than the current flow through OLED, which is beneficial for fast addressing time even for low luminance level. However, this driving method also has a weak point that requires the matching electrical properties of T1 and T2 which is

difficult for LTPS TFT process.

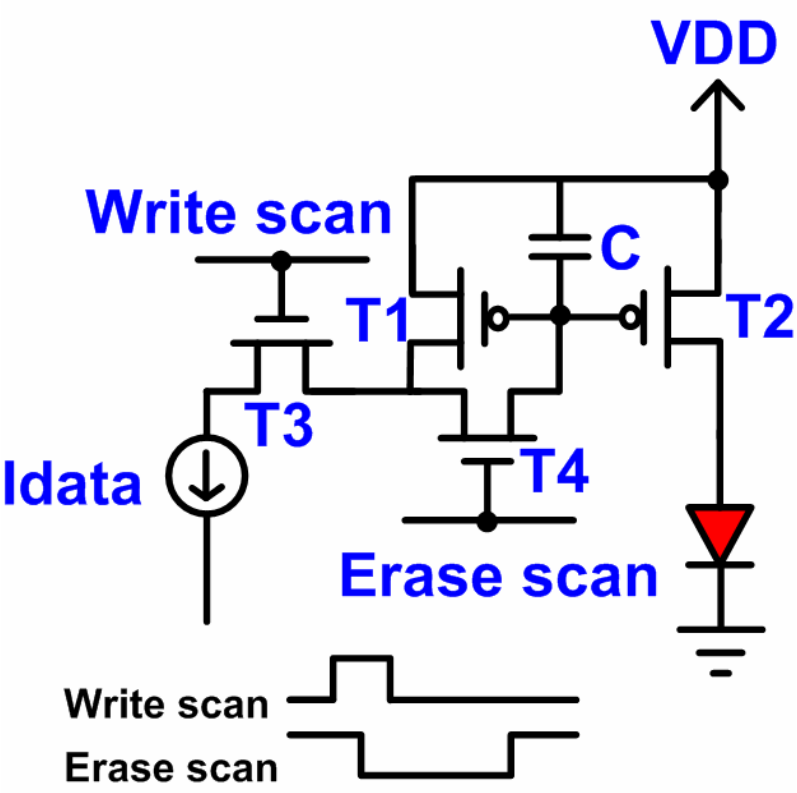


Fig. 3-17. Current mirror pixel circuit and its timing diagram.

3.4.3 Novel Driving Circuits

There are still other pixel circuits which are not completely belonged to voltage programming or current programming circuits, and these circuits will be discussed in this part.

First, *Polarity-Balanced Driving* for reducing the threshold voltage shift especially for a-Si TFTs will be introduced [3.40]. It consists of dual scan line and double conventional pixel structure with positive and negative driving shown in Fig. 3-18. The scan m ($2n\text{-}1^{th}$) is high in the odd frame and turns SW1 and SW2 on, while the capacitor (Cst1) is charged by positive data (+Vdata) to maintain data voltage during this frame. The DTR1 drives the OLED and DTR2 is annealed by negative

bias through Vdata2 line. SW3 and SW4 operate in the same way during the even frame. Each driving TFT positively shifted in threshold voltage when displaying data and annealed by negative bias when neighboring TFT operates. However, this driving method includes dual scan lines, six transistors and two capacitors in a pixel pitch occupying large active area which is hardly realized in high resolution displays.

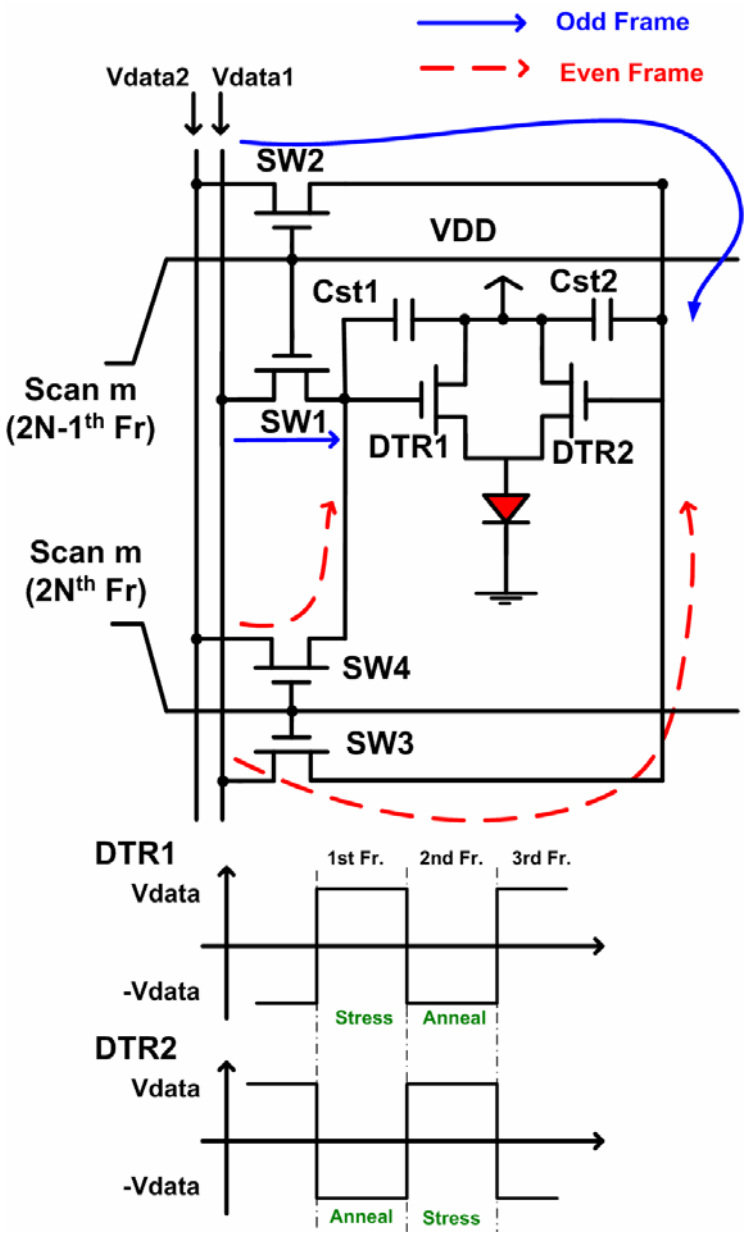


Fig. 3-18. Polarity balanced driving method and driving sequence.

Second, *Clamped Inverter Driving* to perform high inter-pixel uniformity and

gamma correction will be introduced [3.41]-[3.45]. Fig. 3-19 shows the configuration of the clamped inverter driving pixel circuit. During the writing period, T1 and T2 are turned on, and the analog signal voltage and the inverter's reset voltage are applied to each node in a storage capacitor C, respectively. The reset voltage is evidently a mean value of the inverter's ON and OFF state voltages. In the illumination period, T3 is set to the ON state and then the emission is controlled by a comparison with the sweep signal from the sweep line and the voltage stored in C. The inverter's deviation can be also suppressed by designing the inverter's TFTs with higher transconductance and lower channel conductance [3.41]-[3.45].

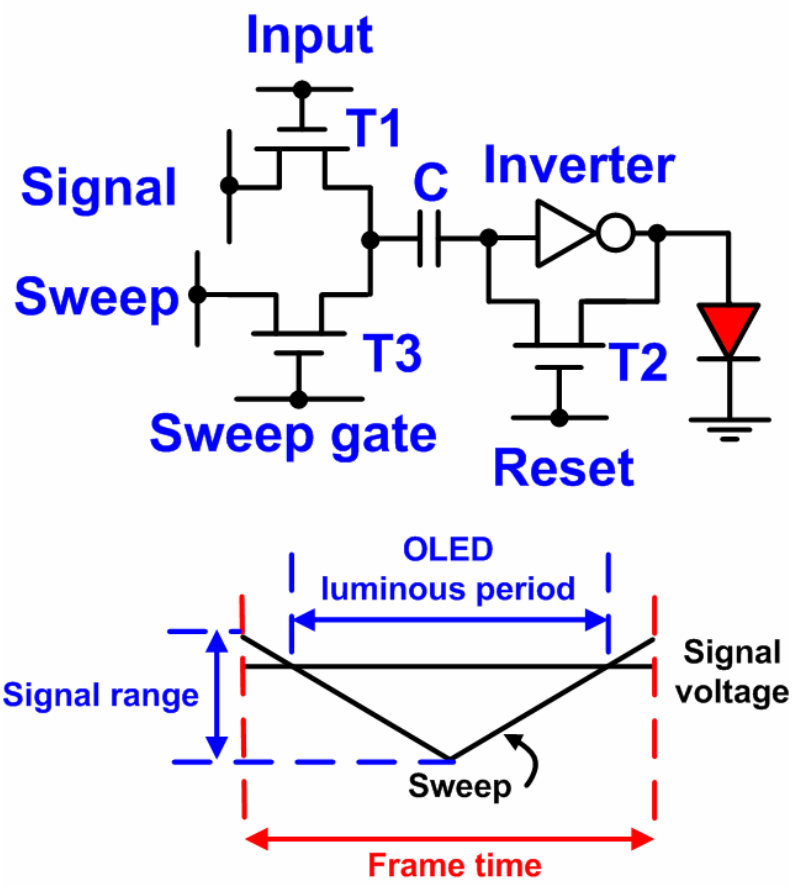


Fig. 3-19. Clamped inverter driving method and timing chart.

Third, *Time Division Control (TDC)* driving method which make it possible to realize high density AMOLED will be introduced in this section [3.46]. The

configurations of pixel circuit are shown in Fig. 3-20. One OLED emission area corresponds to one pixel circuit in conventional driving method, but the sequential control of emission can realize more than two pixel circuits in the TDC driving by using just one pixel circuit. One frame period of this driving method is divided into three subfields. Except high resolution display can be realized, the data driver in n-field TDC is only 1/n that of required in conventional driving method along with low manufacturing costs. This driving method can be also collocated with pixel compensation circuit. However, it must be increase the driving frequency in time division control driving method which leads to higher power consumption.

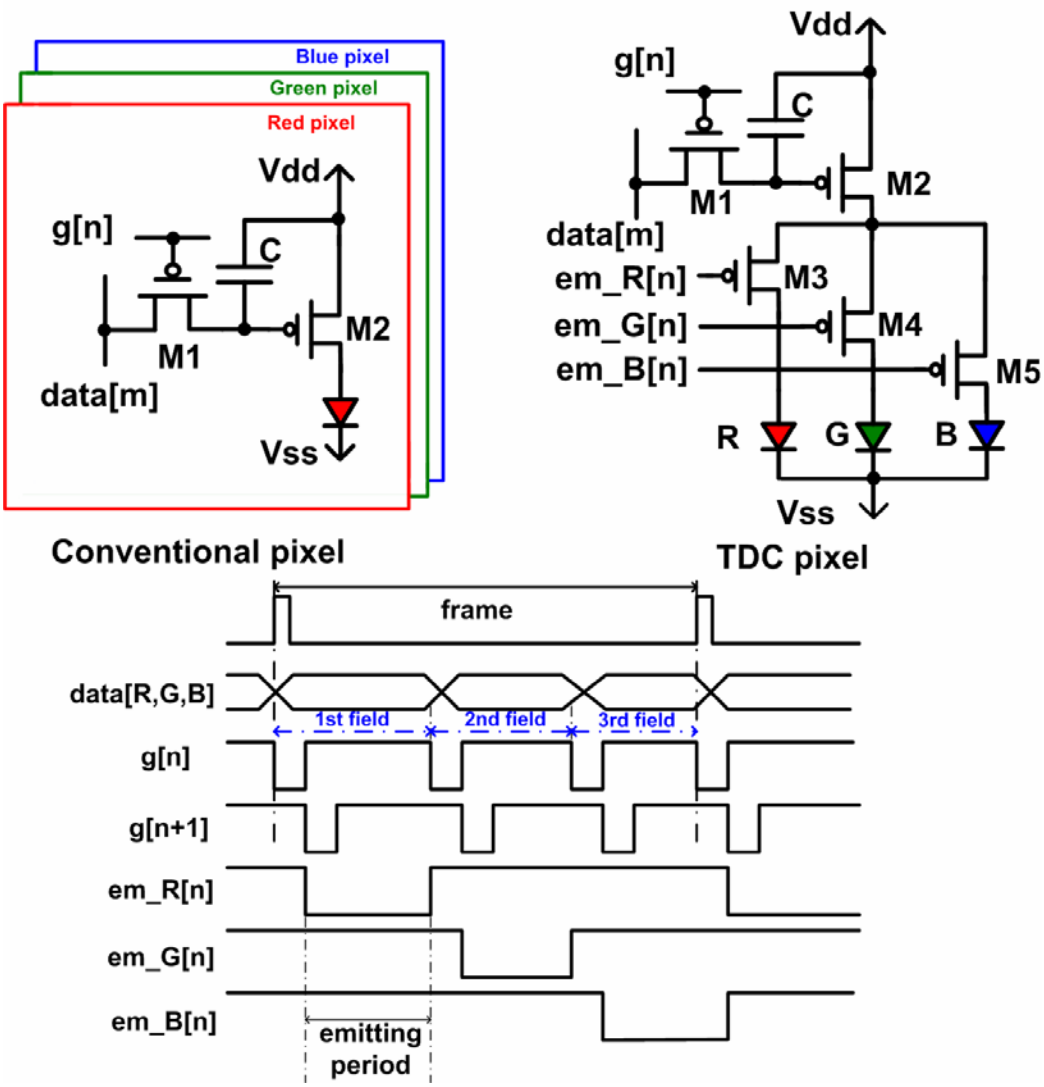


Fig. 3-20. Time division control driving method and timing diagram.