# Chapter 5

# Evaluated Results and Comparisons of Source Follower Type, Operational Amplifier Type, and Proposed Analog Buffer Circuits

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## 5.1 Introduction

Fig. 5-1 shows the block diagram of AMLCD panel composed of the data driver, scan driver, Vcom reference voltage, DC/DC converter, timing controller, etc [5.1]-[5.6]. Each function has been introduced in chapter 1.

Among these functional blocks, data driver shown in Fig. 5-2 has been considered the core part in the periphery circuits. It consists of shift register, data register, level shifter, digital to analog converter, and analog buffer mentioned in chapter 1. Pursuing the system-on-panel target, solve non-uniformity problem of LTPS-TFTs will be the main goal. It can be discussed from three topics: First, obtain highly uniform poly-Si thin film, less defect density variations, etc. in material and process technology. Second, get novel or modified device structures for better tolerance of device variation. For example, in chapter 2, LTPS-TFTs employed multi-channel structure with slicing layout method has been studied to improve the uniformity. Third, compensated circuit design is needed to correct the device-to-device variations of LTPS-TFTs.

In this work, the typical analog buffer with slicing layout method is adopted and studied the variation effect. Furthermore, all the compensation methods are classified and compared in this chapter.

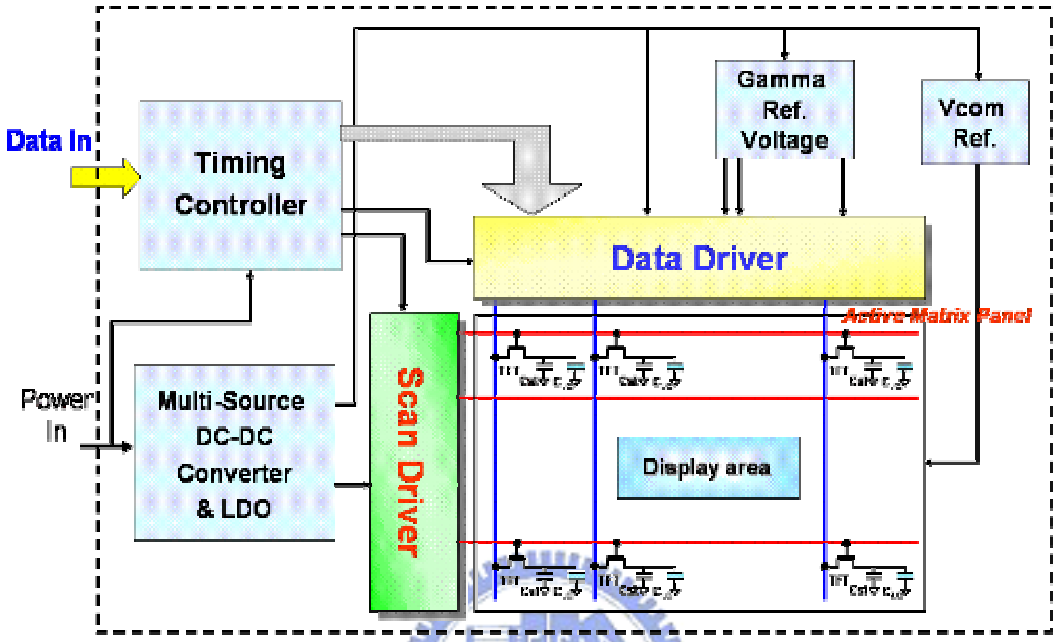


Fig. 5-1. Block diagram of AMLCD panel.

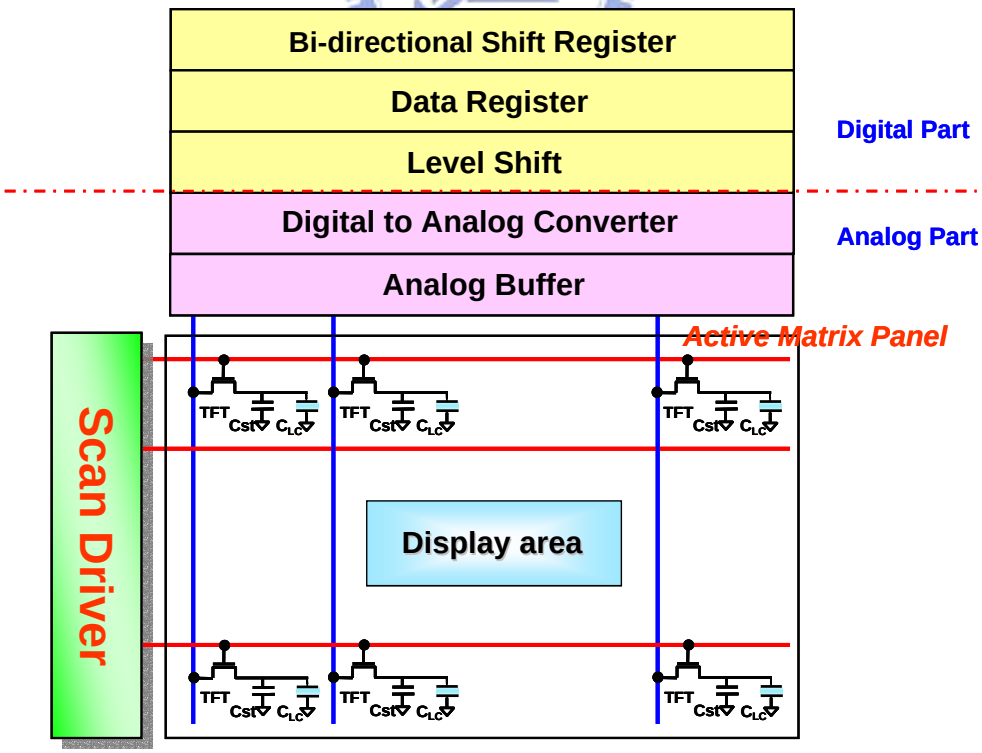


Fig. 5-2. Functional blocks of data driver circuits in AMLCD panel.

## 5.2 Considerations for Designing of LTPS-TFTs Analog Buffer Circuits

To design the analog buffer of the data driver, there are several important considerations for designing listed including the output voltage accuracy, layout area, driving capability, power consumption.

1. **Output voltage accuracy**

The major goal of analog buffer is transmitting the correct data and driving the large load capacitance in the panel. If the output signal from the DAC changed after passing analog buffer, the active area will show the wrong image and lead abnormal picture. Therefore, output voltage accuracy is the primary requirement in the analog buffer.

2. **Layout area**

In the driving architecture, hundreds of analog buffers are needed in the active matrix display. Each analog buffer matches a pixel pitch. As the resolution getting higher and higher, pixel pitch is reduced to get high quality display. Nevertheless, the simple configuration is more favorable for high resolution display.

3. **Driving capability**

In the large area and high resolution display, the loading is huge and the available charging time is short. During the limited output settling time, the output voltage must be charged to target value quickly. Thus, analog buffer with high driving capability is another requirement for future displays.

4. **Power consumption**

Power consumption is the important issue for portable applications. In the aspect, poly-Si TFTs consumes much power than single crystal Si for its lower carrier

mobility, higher threshold voltage, etc. Since hundreds of analog buffer are needed in the display, low power consumption is worthy of pursuing.

## 5.3 Simulation Results of Operational Amplifier Type (Op-amp-type) Analog Buffer

Through the measured results from conventional source follower of multi-channel structure has been improved, it still cannot achieve the standards of system-on-panel product. Therefore, circuit compensation techniques must be applied to the analog buffer for better performance. A lot of reports have been proposed to compensate the LTPS TFTs variations applied to the analog buffer. These analog buffer compensation circuits can be classified into operational amplifier type and source follower type. Operational amplifier type (Op-amp-type) analog buffer is introduced in this section 5.3, while source follower type will be discussed in section 5.4.

### 5.3.1 Typical Op-amp-type Analog Buffer

Fig. 5-3 shows the circuit configuration of the typical operational amplifier. It belongs to two-stage operational amplifier composed of a differential pair and an output stage. Monte Carlo simulation also was executed to investigate the performance under devices variations, where the mean value and deviation value of the threshold voltage and field-effect mobility are 1.45V, 0.5V and 65.69 $cm^2$/V-sec, 15 $cm^2$/V-sec, respectively. Each device is assumed to vary independently. The Monte

Carlo simulation results of the typical op-amp-type analog buffer with varied input voltage from 1V to 6V are shown in Fig. 5-4. It can be observed that offset voltage suffers huge variations exceeding 1400mV with the device variations. Therefore, an effective compensation method is required to promote the output voltage performace.

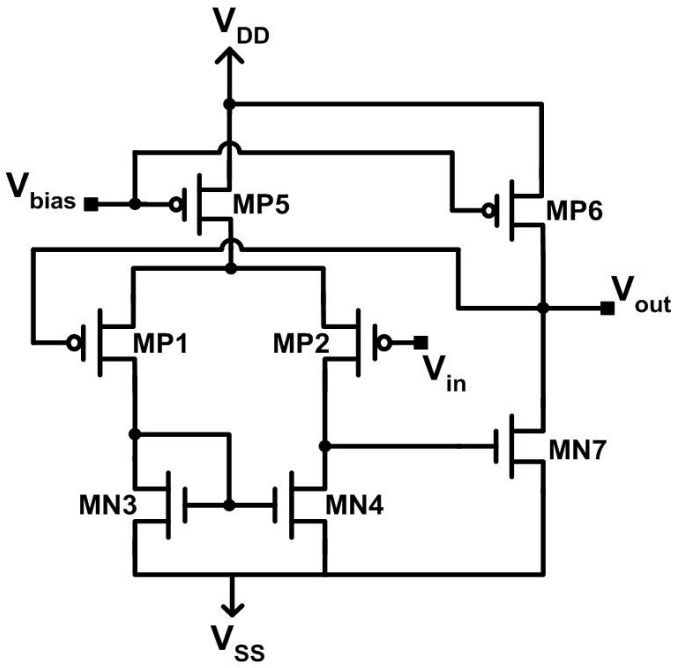


Fig. 5-3. Circuit configuration of the typical operational amplifier.

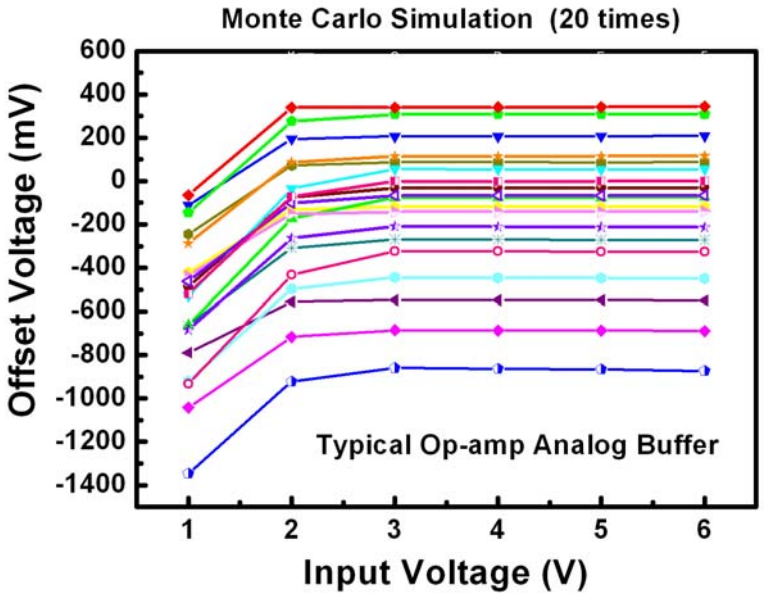


Fig. 5-4. Monte Carlo simulation results of the typical op-amp-type analog buffer with varied input voltage from 1V to 6V.

### 5.3.2 Bias Circuit Op-amp-type Analog Buffer

In the typical operational amplifier of Fig. 5-3, bias current would be varied if threshold voltage of MP5 is non-uniform. To avoid the problem, bias circuit compensation method has been proposed [5.7] and shown in Fig. 5-5. A threshold voltage insensitive to the gate bias voltage generating circuit is added to calibrate the threshold voltage variation on the bias current. The operation principle is described as follows. Without bias compensation in the beginning, the bias current would be

$$I_d = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{MN5}\left(V_{gs\_MN5} - V_{th\_MN5}\right)^2 \quad \text{..... (5.1)}$$

The current is depended on the mobility and threshold voltage variation, which leads the non-uniformity across the display. By adding the gate bias circuit, in the first stage, M1 turns on and the capacitor will be charged up to Vref. During the second period, M1 turns off while M2 turns on. The node Vg will be charged up to Vbias+Vth_MN3 with collocating higher Vref. After that, the current becomes

$$I_d = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{MN5}\left(V_{bias} + V_{th\_MN3} - V_{th\_MN5}\right)^2 \quad \text{..... (5.2)}$$

and $$I_d = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{MN6}\left(V_{bias} + V_{th\_MN3} - V_{th\_MN6}\right)^2 \quad \text{..... (5.3)}$$

With the assumption of MN3, MN5, and MN6 are matched, the bias current would be independent of threshold voltage variations.

However, the electrical characteristics would not be well-matched in LTPS-TFTs. Fig. 5-6 shows the Monte Carlo simulation results with the assumption of devices vary independently. It is clear that variations are still huge and this compensation circuit is impractical when devices not well-matched.

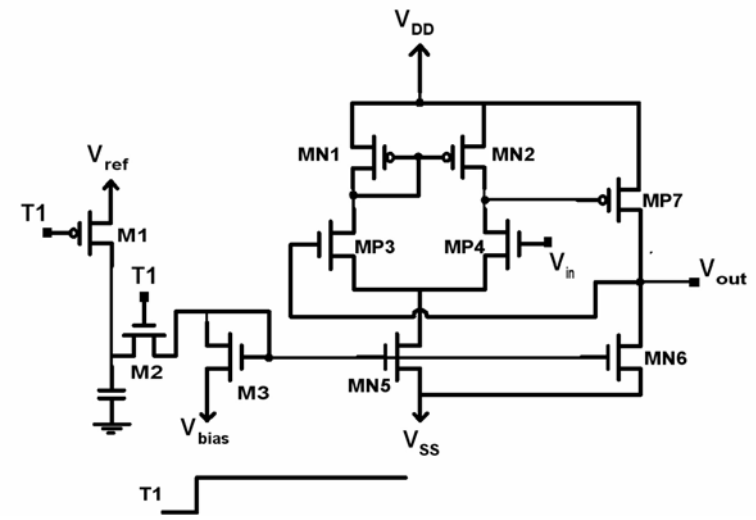


Fig. 5-5. Yiu's bias circuit compensated operational amplifier type analog buffer.

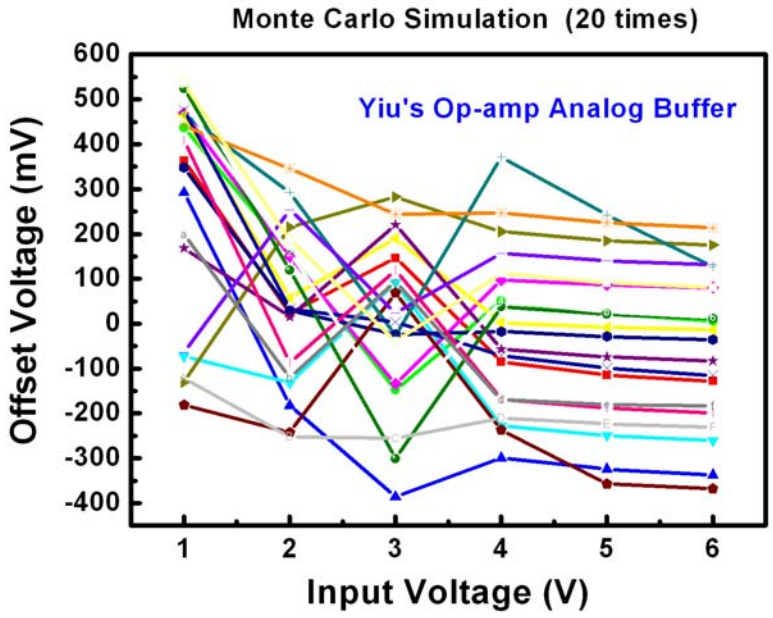


Fig. 5-6. Monte Carlo simulation results of the Yiu's operational amplifier type analog buffer with varied input voltages.

## 5.3.3 Differential Pair Op-amp-type Analog Buffer

Fig. 5-7 shows the circuit schematic and timing diagram of the Itou's differential amplifier [5.8]. Three switches and one capacitor are added to compensate the device mismatch of the differential pair stage. At the first calibration stage, S1 and S2 turn on

while S3 turns off. The gate to source voltage difference between the M3 and M4 is stored in the C1. While S1 and S2 turn off in the second operation stage, S3 turns on and the input data is transmitted to the output node. As a result, the final output voltage will be closed to the input voltage.

Monte Carlo simulation is also examined in Fig. 5-8. It is obvious that the output voltage difference is much smaller than the two previously described circuits. This is because this circuit added the capacitor to store the voltage difference which is lack in the two previous circuits. A slight bias voltage difference results in the different operation region of each transistor with varied electrical performance. The reason causes the previous circuits suffer huge output voltage variations. In the figure, output voltage remains large when input voltage ranges from 1 to 3 Volt. The reason maybe due to the differential pair (M1, M2) operates in the linear region while the transconductance are not kept constant. The load pair mismatch can't be stored accurately so that the output voltage is sensitive to the device variations.

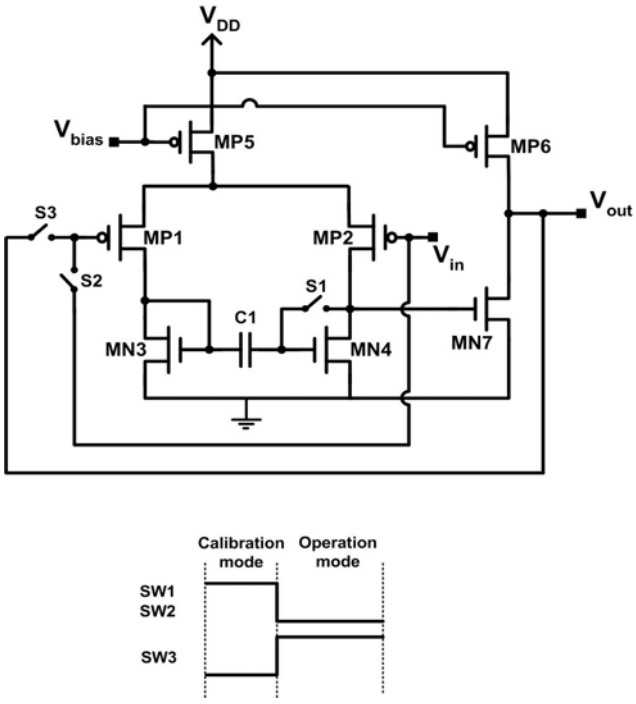


Fig. 5-7. Itou's differential amplifier compensated operational amplifier type analog buffer.

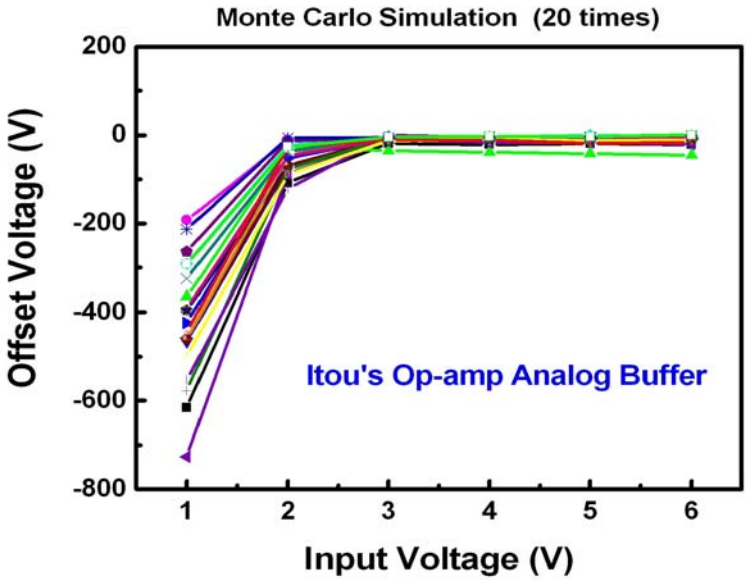


Fig. 5-8. Monte Carlo simulation results of the Itou's operational amplifier type analog buffer with varied input voltages.

## 5.4 Simulation Results of Source Follower Type Analog Buffer

In this section, various compensation methods employed source follower type analog buffer are introduced and simulated to compare with each other. It can be divided into conventional, self-compensation method, matching TFTs method, and current type compensation method.

### 5.4.1 Conventional Source Follower Type Analog Buffer

The conventional source follower type analog buffer is shown in Fig. 5-9, which only consists of single driving TFT. The loading capacitance is assumed 20pF. When

input voltage varies, the output voltage will keep at gate-to-source voltage minus threshold voltage (Vgs-Vth) theoretically. Therefore, the offset voltage is about the threshold voltage of LTPS TFTs. Monte Carlo simulation is also examined to realize the effect of electrical variations on offset voltage. Fig. 5-10 shows the variations about 700mV which lower than typical operational amplifier, but still can not be accepted. An effective compensation circuit is required to diminish the variation effects in LTPS-TFT analog buffer circuits.

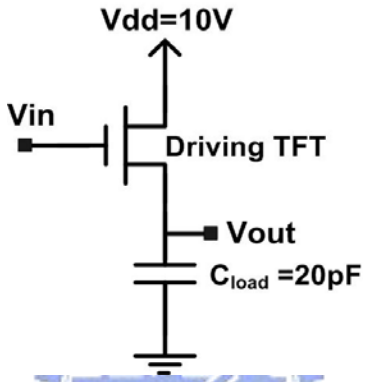


Fig .5-9. Schematic of conventional source follower type analog buffer.

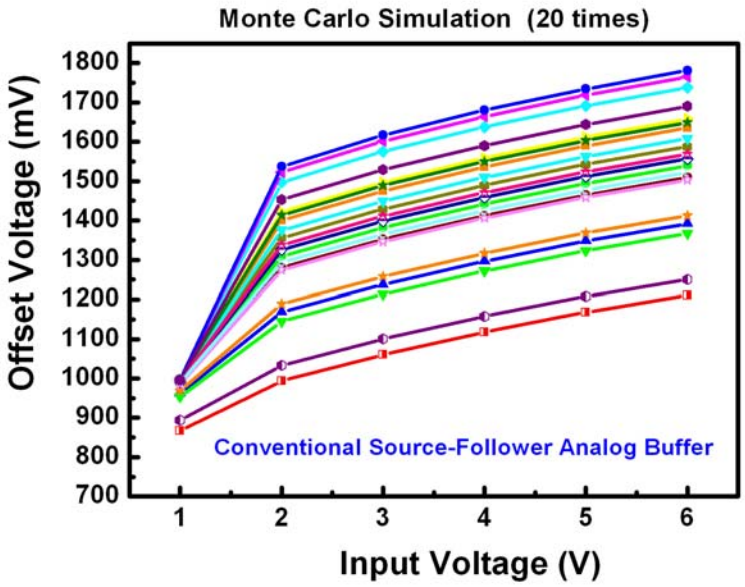


Fig. 5-10. Monte Carlo simulation results of the output offset voltage variations in conventional source follower type analog buffer.

## 5.4.2 Self-Compensation Method

Self-compensation means to calibrate the threshold voltage variations of driving transistor in the analog buffer circuit. At least one additional capacitor must be added to store the differences between transistors in the calibration stage. For example, the push-pull analog buffer was proposed by Chung et al. [5.9] shown in Fig. 5-11. In the first compensation period, input voltage is applied to the gate node of driving transistor. At this time, SW1 and SW2 turn on while the threshold voltage stored in Cvt. In the data input period, input voltage transmits and the gate node voltage of the driving TFT becomes input voltage plus the voltage stored in the capacitor during previous period. In the similar way, the p type driving transistor passes the negative data. Therefore, the threshold voltage variations of driving TFT would be cancelled by the method.

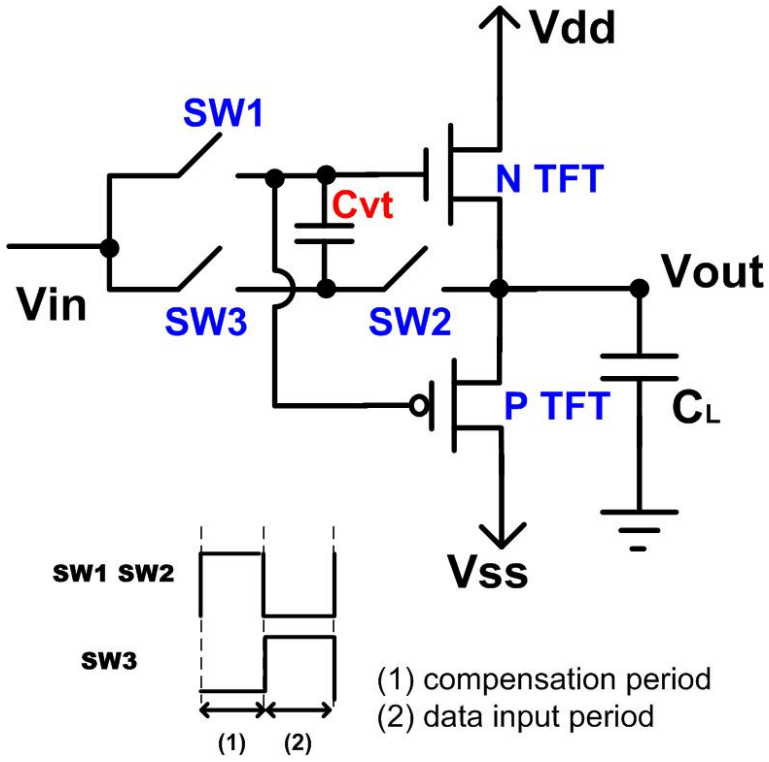


Fig. 5-11. Schematic and timing diagrams of Chung's push-pull type analog buffer.

Fig. 5-12 shows the output offset voltage varied simulation results of push-pull

type analog buffer. It is obvious that the variations are compensated well except when the voltage equal 1 to 2 V. The major reason is due to the threshold voltage is about 1.4V causing the poor sub-threshold characteristics. Besides, the driving TFT may not be biased in the same gate-to-source voltage between two operation stages.

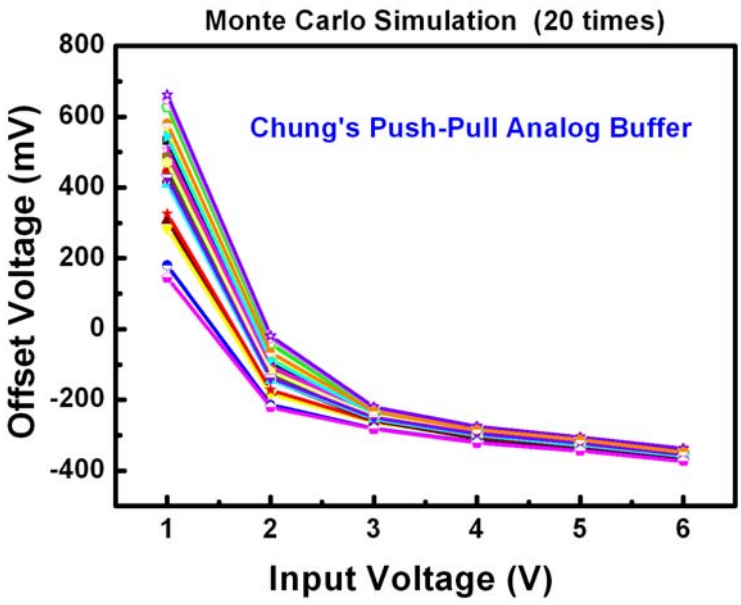


Fig. 5-12. Monte Carlo simulation results of the offset voltage variations of Chung's push-pull type analog buffer.

To solve the mentioned problem, double offset canceling method was proposed by Sony corp. [5.10]. This circuit consists of seven switches, two capacitors, one driving TFT, and one constant current source which are shown in Fig. 5-13. The concept is the same as push-pull type analog buffer, but the calibrating operation is operated two times. The one more calibration is executed to make sure the driving TFT biasing in the same condition. The operation sequence is described as follows: The SW6 turns on first to charge the $C_L$ voltage level to the output node. Then the both switches SW1 and SW4 turn on to supply the analog voltage from the input node. Next, SW1 turns off, and SW2 turns on to store the first offset voltage in the capacitor

ccn1. Then both SW2 and SW4 turn off, and SW3 turns on to store the second offset voltage in the ccn2. The stored voltage in the ccn2 comes very close to the actual offset voltage. Consequently, highly precise output voltage is achieved which leads to high quality image without fixed pattern noise.

Fig. 5-14 shows the simulation results of the output offset voltage variations in this double-offset-canceling circuit. It can be identified that final output voltage is almost independent of the threshold voltage variations. Though highly précised output voltage can be obtained, too many switches and control signal lines are needed in this circuit. It will occupy huge layout area and require complicated timing sequences which are not willing to designers.

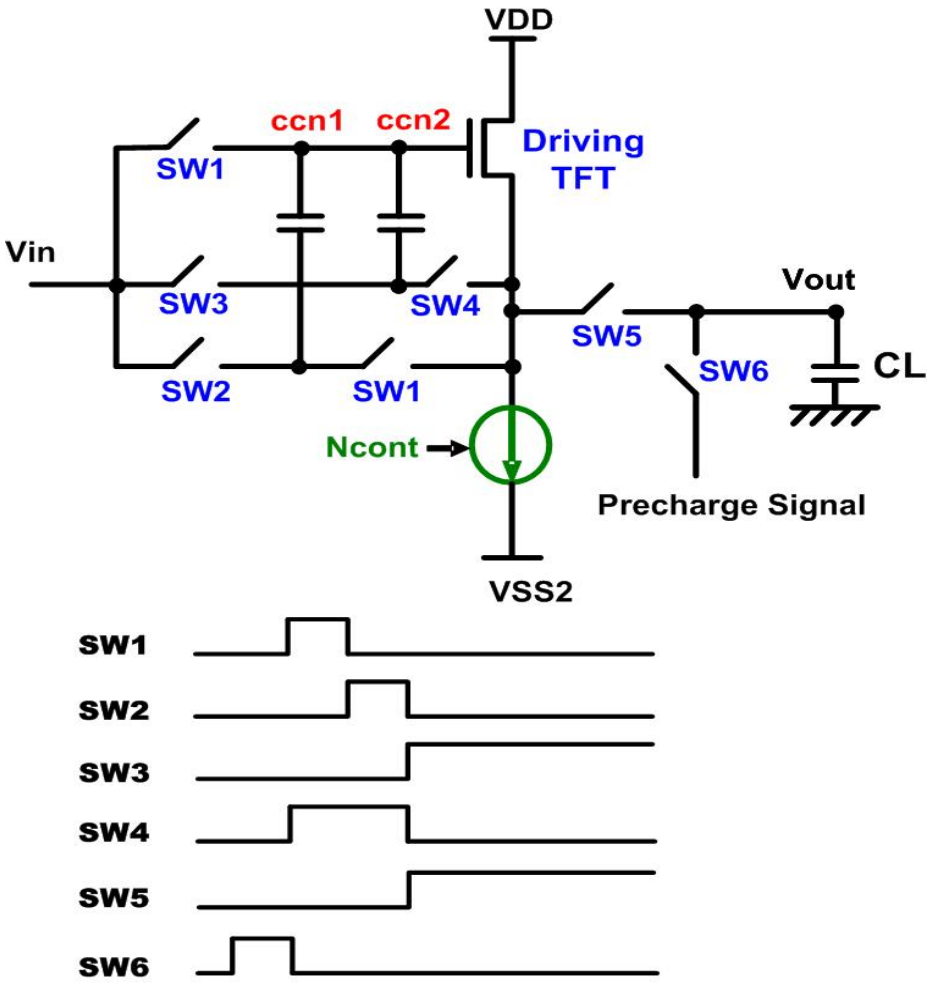


Fig. 5-13. Circuit configuration and timing diagrams of double-offset-canceling analog buffer.

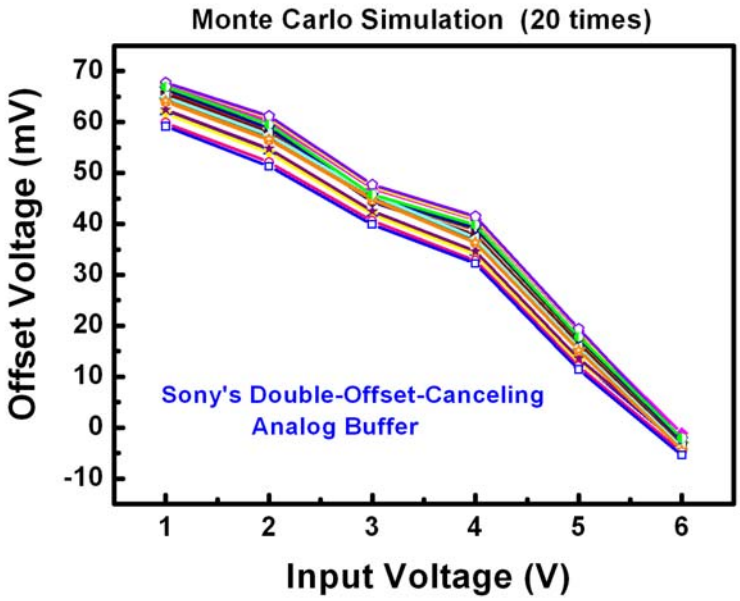


Fig. 5-14. Monte Carlo simulation results of the offset voltage variations of double-offset-canceling analog buffer.

Another self-compensation type analog buffer is shown in Fig. 5-15. It is composed of two transistors, four switches, and one additional capacitor. During the first compensation period, switch S1 and S3 turn on to lead the current flow through M2 and M1 is equal to each other. At this time, the variations of driving transistors have been stored in the capacitor. After that, S2 and S4 turn on in the data input period while the driving current is the same as first period. The operation means the M1 biased in the same condition in each period, and the threshold voltage and the field-effect mobility variations are compensated.

Fig. 5-16 reveals the Monte Carlo simulation results are normal except the low input data voltage. The main source of output voltage error is the small output resistance of the poly-Si TFTs. For this reason, the current in the two periods may be different causing the incorrect output voltage.

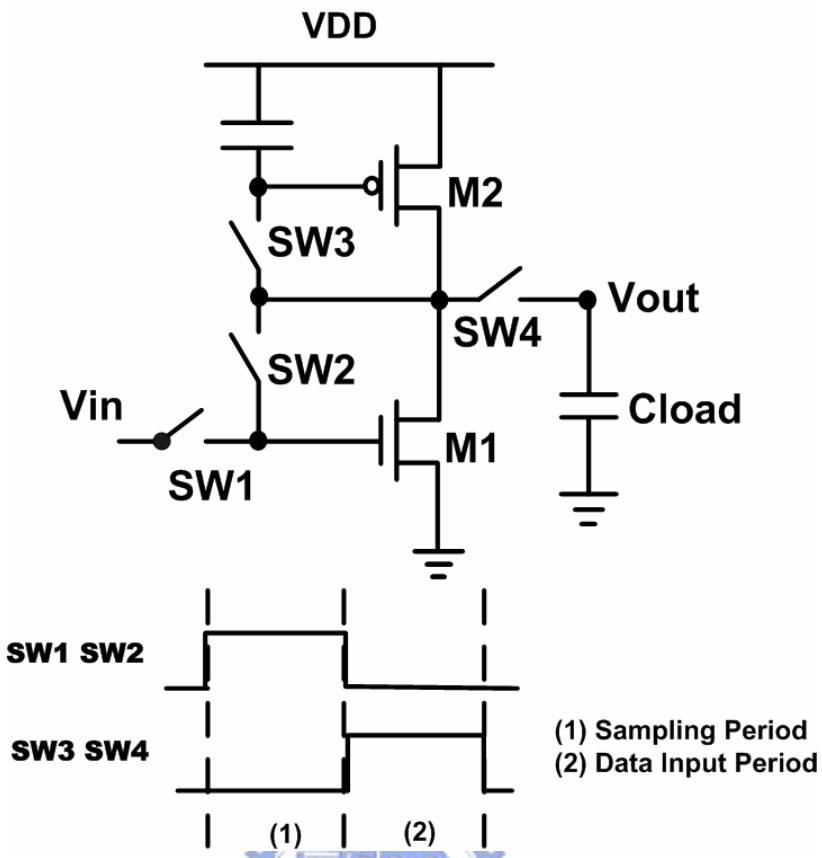


Fig. 5-15. Schematic and timing diagrams of Yoo's analog buffer.

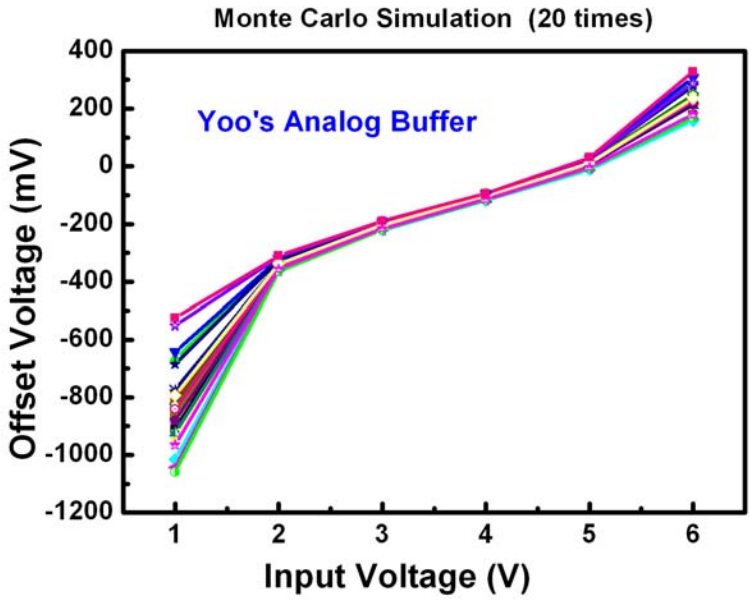


Fig. 5-16. Monte Carlo simulation results of the offset voltage variations of Yoo's analog buffer.

### 5.4.3 Matching TFTs Method

The concept used in matching TFTs type here is the same as AMOLED pixel circuits mentioned in chapter 3. The structure and timing diagram is shown in Fig. 5-17. It is composed of five transistors and two additional control lines. The reset signal is high to clear the previous data voltage in the loading capacitor, and the following input data signal is applied. When the voltage of node A is higher than node B, TFT N1 turns on and TFT N2 turns off. At this time, the gate voltage of driving TFT N3 becomes about Vin-$Vth_{\_N1}$ since TFT N1 is diode-connected configuration. Then the active signal is high. Since the node B is floating, the voltage will be charged up due to the bootstrapping effect. The voltage of node B reaches Vin+$Vth_{\_N2}$ and the TFT N2 turns on while TFT N1 turns off. The output voltage becomes Vin+$Vth_{\_N2}$-$Vth_{\_N3}$ after this operation. If the TFT N2 and TFT N3 are well-matched, the final output voltage reaches input voltage.

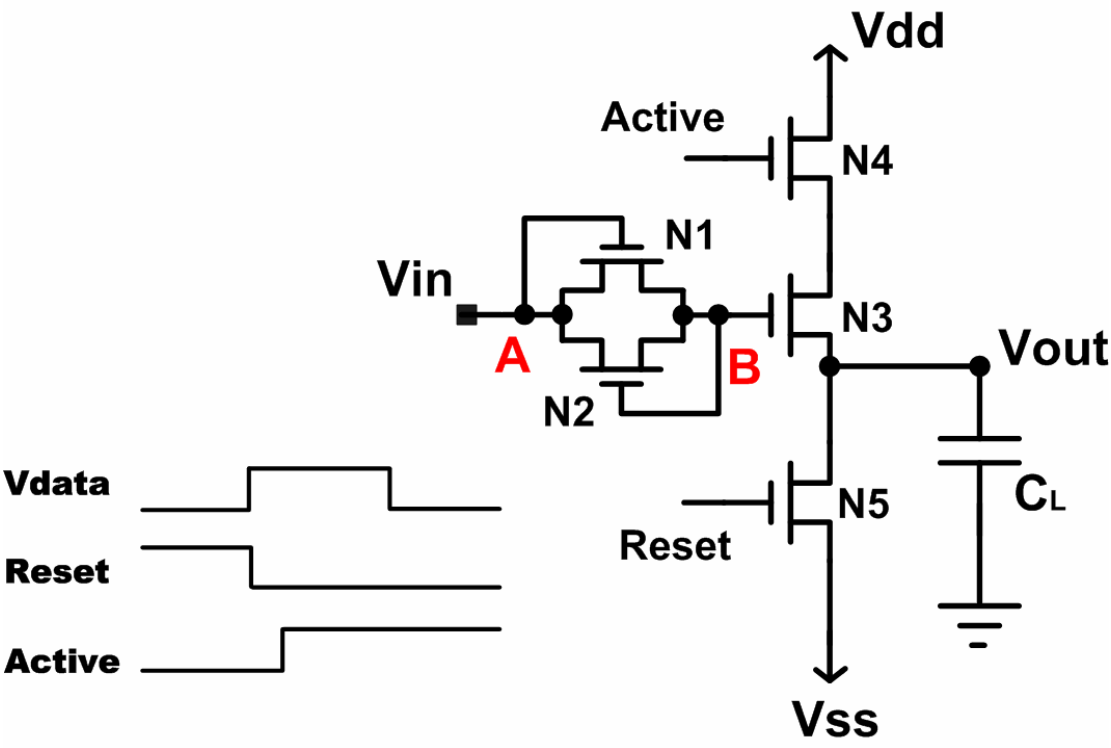


Fig. 5-17. Schematic and timing diagrams of matching TFTs type analog buffer.

However, it is impossible for fabricating the two identical devices, which means the offset voltage will not be cancelled perfectly. Fig. 5-18 shows the simulation results of all TFTs have random electrical performances. The variations are still huge even reaching 1000mV, it represents this method can not compensate the non-uniformity effectively.

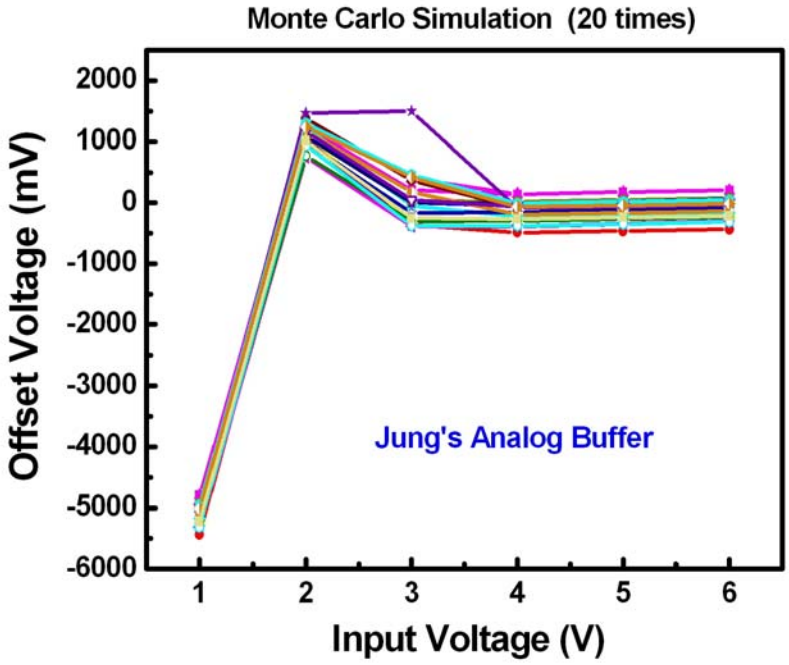


Fig. 5-18. Monte Carlo simulation results of the offset voltage variations of matching TFTs type analog buffer.

## 5.5 Issues of Conventional Source Follower Type Analog Buffer

The typical model of the LTPS TFTs used in this work is represented by the RPI parameters. In this work, the data line loading capacitance is assumed 20pF corresponding to a 2-inch QVGA LCD.

### 5.5.1 Unsaturated Output Voltage Phenomenon of the Analog Buffer

A conventional source follower and its output waveform are shown in Fig. 5-19. It is observed that the final output voltage is not kept constant, but exceeds the value of VGS-Vt expected in principle. It is ascribed to the sub-threshold current. As model used in this work, the sub-threshold swing of LTPS TFTs is about 0.3V/dec that is much larger than MOSFETs' (0.06V/dec). Consequently, the output voltage will be sensitive to the charging time for various product specifications. An active load is added to eliminate this phenomenon and the output waveform simulation result is also shown in Fig. 5-20. It is distinct that unsaturated phenomenon of the output voltage is suppressed and the final output voltage nearly kept constant. Fig. 5-21 plots the offset voltage (Vin-Vout) versus input voltage (Vin) of conventional source follower and source follower with active load with different charging time. It is observed that the offset voltage of conventional source follower and source follower with active load varies with different input voltage. Most importantly, the offset voltage difference of conventional source follower is larger than source follower with active load with different charging time which leading higher difficulty designing. Although offset voltage of source follower with active load larger than conventional source follower, it can be eliminated by gamma correction [3.43], [5.11]. According the results, the charging time variation-tolerant characteristic of source follower with active load is superior to the conventional source follower.

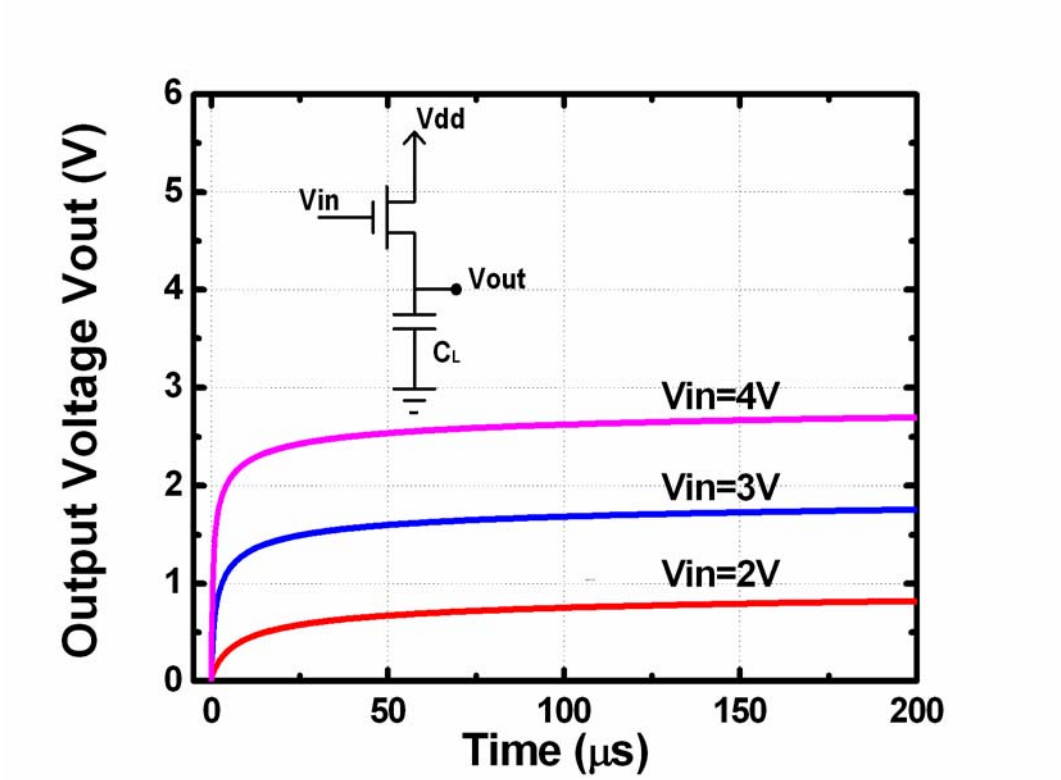


Fig. 5-19. Conventional source follower and its output waveform simulation results.

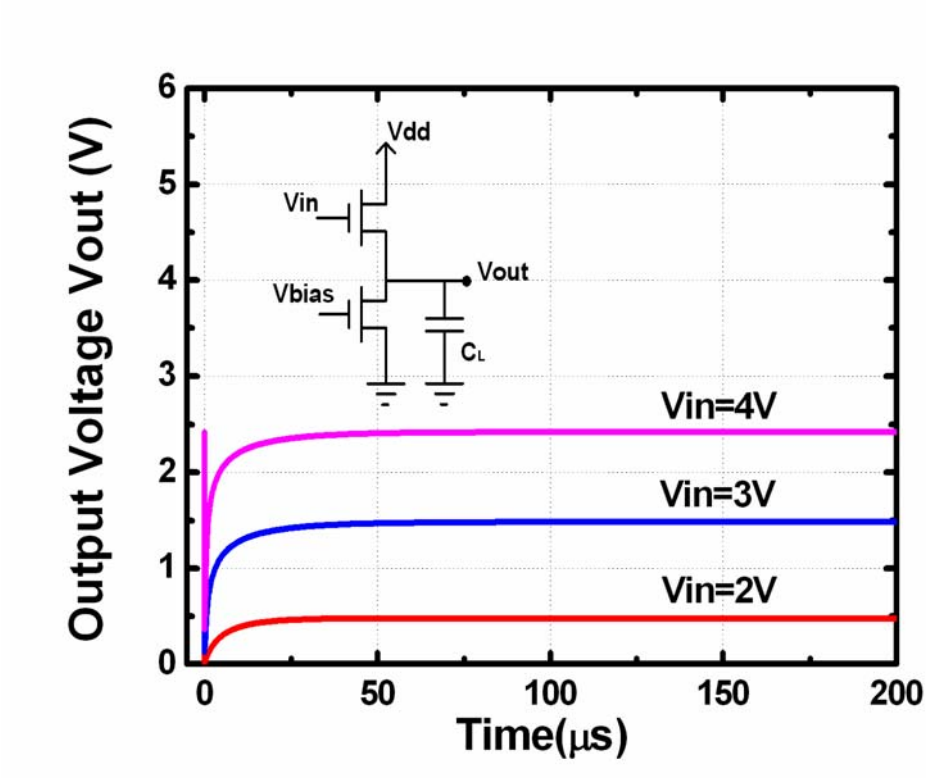


Fig. 5-20. Schematic of conventional source follower with an active load and its output waveform simulation results.

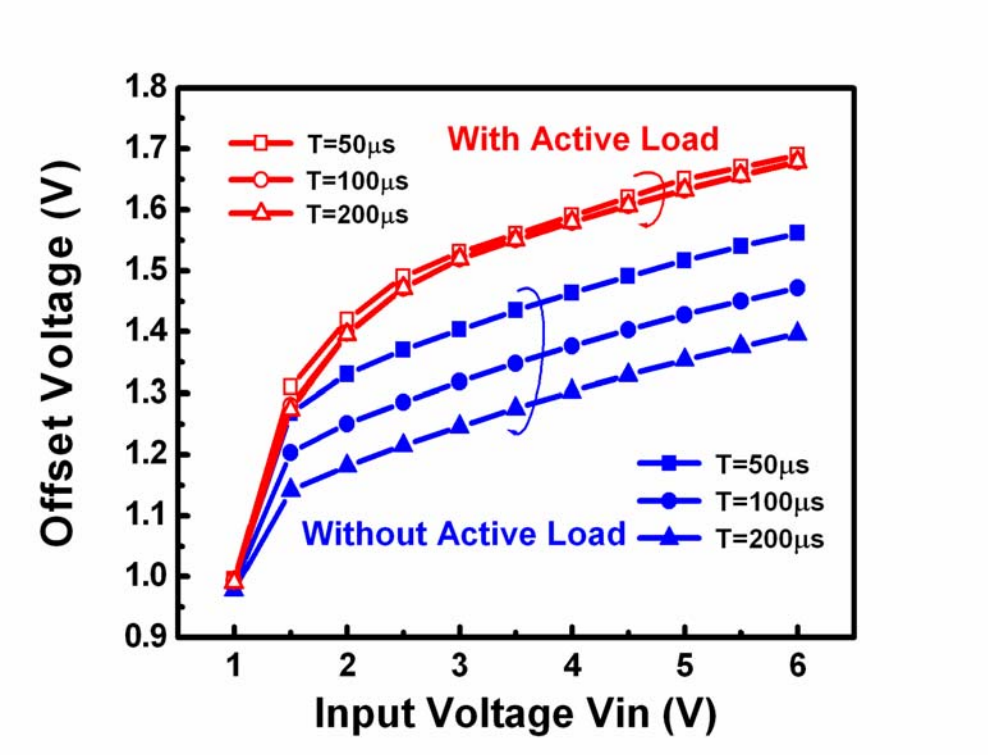


Fig. 5-21. Offset voltage comparison of conventional source follower and source follower with an active load in various charging time.

### 5.5.2 Output Voltage Distributed Phenomenon of the Analog Buffer

After solving the unsaturated output voltage problem, device-to-device variation problem still exists in our circuits. To study the effect of the device variation on the circuit performance, Monte Carlo simulation with an assumption of normal distribution is executed where the mean value and the deviation of the threshold voltage and mobility are 1.55V, ± 1V, 52.02 $cm^2$/V-s, and ± 20 $cm^2$/V-s, respectively. We assume that each of the TFTs in the buffer circuit varies independently.

Fig. 5-22 shows the twenty times Monte Carlo simulation results of the conventional source follower with active load when input voltage are 2V to 4V. It is

clear that the circuit suffers from huge variations and final output voltage varies due to the LTPS TFTs device variation. Therefore, an effective compensation circuit is required to eliminate device variation passing through the right data.

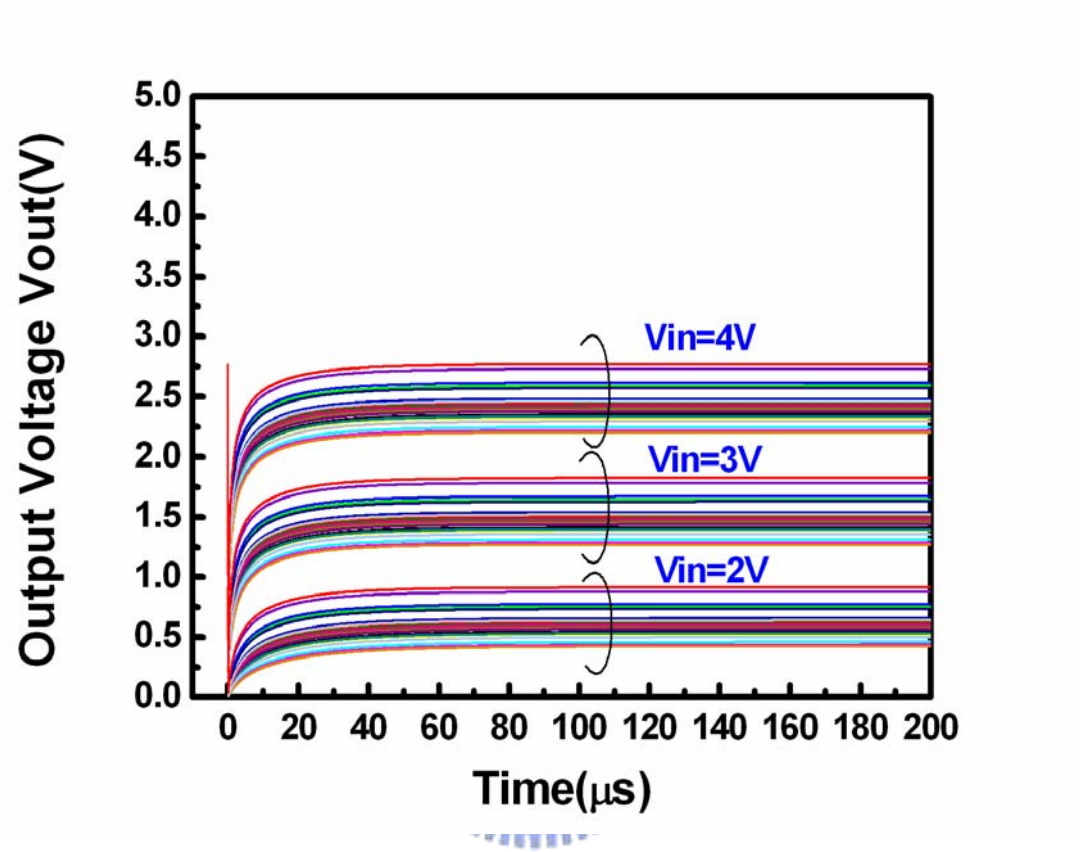


Fig. 5-22. Twenty times of Monte Carlo simulation results of the conventional source follower with an active load when input voltage 2V to 4V.

## 5.6 Proposed Source Follower Type Analog Buffer

It is obvious that the conventional source follower circuit suffers from huge variations and final output voltage varies due to the LTPS TFTs device variation from previous reports. Therefore, a new analog buffer is proposed in this article for the compensation of the device variations.

Fig. 5-23 shows a schematic of the proposed analog buffer consisting of two

n-type thin film transistors, one capacitor, and four switches and its timing diagram. The gate voltage of the active load TFT is biased at Vbias. The driving schemes are as follows: During first operating period, SW1 and SW2 are turned on, and SW3 and SW4 are turned off. There by, a voltage corresponding to the threshold voltage of the driving TFT, the threshold voltage of the active load, the bias voltage, and so on is stored in Cvt. After sampling period, SW3 and SW4 are turned on and SW1 and SW2 are turned off, then the voltage at the gate of the driving TFT is hold. Thus, the output voltage is compensated by the voltage stored in Cvt previously. Fig. 5-24 shows that the output voltage variation of the new type source follower. The output voltage variation decreases drastically. In the limited pixel pitch circuit design, the driving TFT is designed larger W/L ratio possessing higher driving capability and the active load is designed smaller W/L ratio to serve as constant current without kink effect. Table 5-1 shows the dynamic performance of settling time of the proposed analog buffer as input voltage ranges from 1V to 5V. Although the settling time is longer as input voltage is 5V, the input level of 5V is seldom used for the LCD data driver with common toggle driving method. Therefore, the dynamic performance of the proposed analog buffer is acceptable for the application of LCD data driver. The devices and timing simulation parameters used in the proposed circuit design are summarized in Table 5-2.

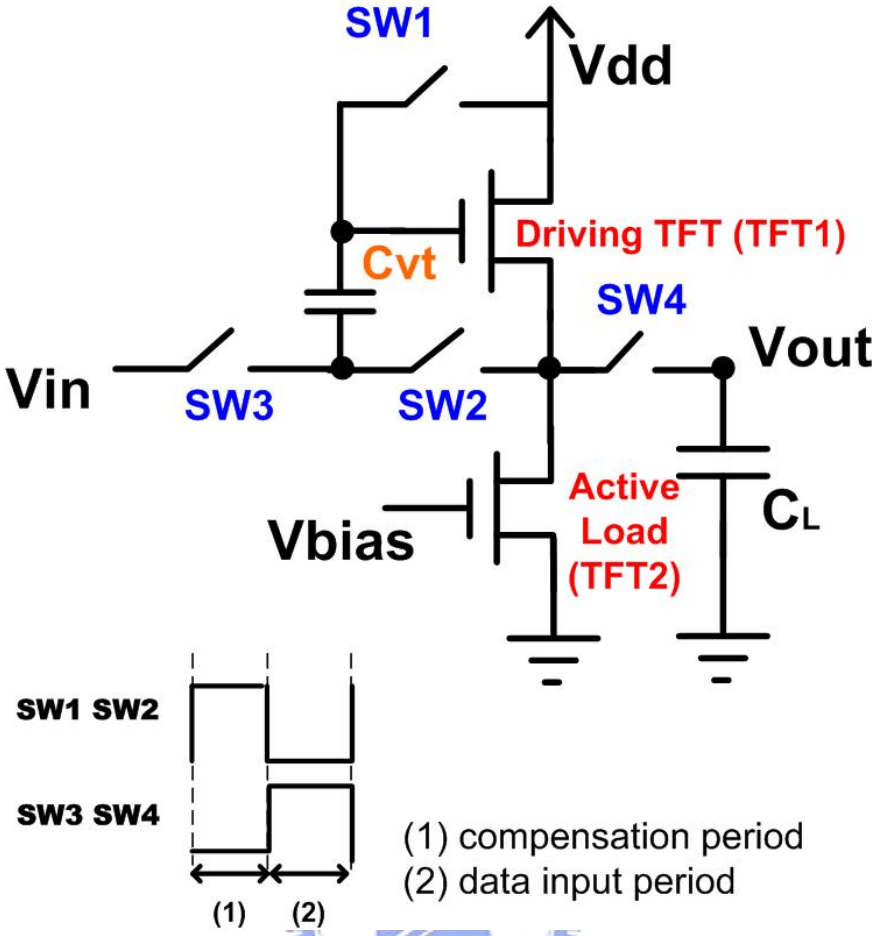


Fig. 5-23. The proposed analog buffer and its timing diagram of signal lines.

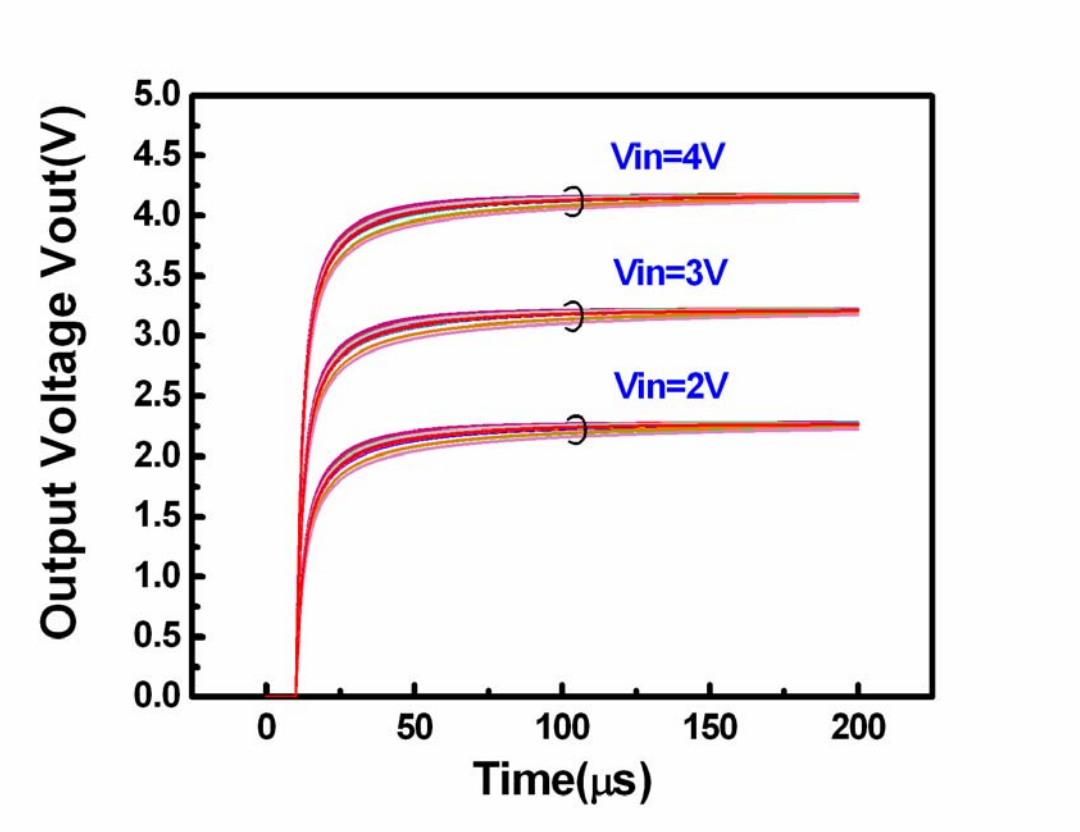


Fig. 5-24. Twenty times of Monte Carlo simulation results of the proposed analog buffer when input voltage 2V to 4V.

| Input Voltage Vin (V) | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| Settling Time ($\mu$sec) | 13.08 | 20.42 | 27.43 | 36.34 | 47.1 |

Table 5-1. The output settling time of the proposed analog buffer with input voltage ranges from 1V to 5V.

| Devices | Driving TFT | Active Load | Cs and $C_L$ |
|---|---|---|---|
| | 100 $\mu$m/8 $\mu$m | 8 $\mu$m/50 $\mu$m | 1pF and 20pF |
| Signals | Vdd | SW1~SW4 | |
| | 10V | 0V~10V | |
| Timing Period | Compensation Period T1 | Data Input Period T2 | |
| | 10 $\mu$sec | 10 $\mu$sec | |

Table 5-2. Timing period and device parameters of proposed analog buffer circuit simulation.

## 5.7 Comparisons between the Proposed Analog Buffer Circuit and Other Analog Buffer Circuits Design

The various operational amplifier and source follower type analog buffer circuits have been introduced in previous sections. In the following parts, each of them will be compared from several aspects such as output voltage accuracy, layout area, and power consumption. These data are also summarized and compared in Table 5-3.

**Output voltage accuracy**

About this point, it is hardly to be defined the standards of output voltage accuracy. First of all, the value of output-offset voltage is relative but not absolute. If the output offset voltage equal to the same large value when input voltage varies, it can be corrected by the gamma compensation well. The toughest problem is the output offset voltage "variation". Besides, there are no criteria about accuracy with the varied input signal. Offset voltage deviation and the offset variation at Vin=4V are listed and compared in Table 5-3. It can be observed that op-amp type and source

follower type with compensated capacitor obtain smaller variations at input voltage equal to 4V.

**Layout area**

From the previous circuit architectures, it is obvious that operational amplifier requires more transistors occupying large layout area. Beside, each analog buffer must be matched and fitted with a pixel pitch, which leads the large pixel size in operational amplifier type analog buffer. Table 5-3 reveals that fewer transistors are needed in the source follower type analog buffer that is beneficial for high-resolution display.

**Power consumption**

The power dissipation of the source follower type analog buffer is much lower than that of the operational amplifier type from the Table 5-3. Since hundreds of analog buffer circuits are required in the line at a time (LAAT) driving scheme. The source follower type analog buffer is the excellent candidate for the system on panel application.

**Overall Comparison**

The comparisons of the proposed analog buffer and others analog buffer including operational amplifier type and source follower type analog buffers are summarized and compared in the output voltage, circuit configuration, and power dissipations in this section. Among all the listed analog buffer circuits, the output offset voltage variations of proposed analog buffer circuits are smaller than that of others buffer circuits expect the Sony's double offset canceling buffer. Though the output performance of the Sony's double offset canceling analog buffer is amazing better, the requirements of many transistors and extra applied signals which occupies large area and cause much higher power consumption in comparison with our proposed analog buffer. The configuration and power dissipation of the proposed

analog buffer are also superior to others buffer circuits.

| Classifications \ Features | | Offset Voltage Deviation (mV) | Offset Variation at Vin=4V (mV) | Number of Transistors | Number of Capacitors | Additional Control Signals | Power Dissipation at Vin=4V ($\mu$W) |
|---|---|---|---|---|---|---|---|
| Operational Amplifier Type | Typical Two-Stage | 199 | 1434 | 7 | 0 | 0 | 78.4 |
| | Itou's Differential Pair Com. | 427 | 35 | 7 (with 13 switches) | 1 | 2 | 69.2 |
| | Yiu's Bias Circuit Com. | 452 | 546 | 10 | 0 | 1 | 184.5 |
| Source Follower Type | Conventional | 570 | 562 | 1 | 0 | 0 | 4.4 |
| | Chung's Push-Pull | 816 | 46 | 2 (with 8 switches) | 1 | 2 | 6.7 |
| | Sony's Double Offset Canceling | 40 | 9 | 1 (with 15 switches) | 2 | 6 with additional current source | 12.4 |
| | Jung's Matching TFT | 1272 | 634 | 5 | 0 | 2 | 6.6 |
| | Proposed Analog Buffer | 165 | 20 | 2 (with 10 Switches) | 1 | 2 | 5.8 |

Table 5-3. Comparisons of the proposed analog buffer and others buffer circuits.

# 5.8 Summary

In this chapter, several important considerations for designing are listed and discussed including the output voltage accuracy, layout area, driving capability, power consumption.

A lot of reports have been proposed to compensate the LTPS TFTs variations applied to the analog buffer that can be classified into operational amplifier type and source follower type. Each analog buffer circuit is discussed from all aspects in detail. Besides, each one is compared from several aspects such as output voltage accuracy, layout area, and power consumption. The source follower type analog buffer is considered as the excellent candidate for the system on panel target.

In addition to the threshold voltage difference of driving TFTs, the unsaturated of output voltage arisen from the significant sub-threshold current will also result in the difficulty of the buffer circuit design. An active load is added to eliminate this phenomenon and keep the constant voltage with varied charging time. A new simple source follower circuit using low-temperature polycrystalline silicon thin film transistors as analog buffer for the integrated data driver circuit of active matrix liquid crystal displays and active matrix light emitting diodes is proposed and simulated.

Among all the listed analog buffer circuits, the output offset voltage variations of proposed analog buffer circuits are smaller than that of others buffer circuits expect the Sony's double offset canceling buffer. Though the output performance of the Sony's double offset canceling analog buffer is amazing better, the requirements of many transistors and extra applied signals which occupies large area and cause much higher power consumption in comparison with our proposed analog buffer. The configuration and power dissipation of the proposed analog buffer are also superior to others buffer circuits.