Chapter 6

Experimental Results of the Conventional and Proposed Source Follower Type Analog Buffer Circuits

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6.1 Introduction

Low temperature poly-Si (LTPS) TFTs have attracted much attention in the application on the integrated peripheral circuits of active matrix liquid crystal displays (AMLCDs) and active matrix light emitting diodes (AMOLEDs) [6.1]-[6.9]. In a poly-Si TFT-LCD, poly-Si TFT is not only used to implement pixel circuit but also the driving circuit on a single glass substrate to reduce system cost and possess compact module.

Among the many data driving circuits employing LTPS TFTs, the output buffer is indispensable to drive the large load capacitance of the data bus. There are several requirements for the output buffer for a flat panel display data driver [6.10]. For example, as resolution getting higher and higher, more analogue buffers are needed. Therefore, its layout area must be reduced as possible to fit the pitch size. In addition, displays toward portable applications so that power dissipation must be minimized to extend the battery lifetime. However, comparing to the MOSFETs, the LTPS TFTs suffer from poor electrical characteristics and huge device-to-device variation mainly

due to the non-uniform grain structure across the whole glass substrate. Since thousands of output buffers are necessary for a poly-Si TFT-LCD, it is very essential to develop special analog buffers dealing with the device non-uniformity. Variations of LTPS-TFTs will cause the real output voltage not the target value and lead to the wrong gray scale. Thus, the output deviation depends on product specification must be decreased as possible conforming to high degree of matching among the data lines. Among many types of output buffer circuits for displays, source follower is considered an excellent candidate for the output buffer circuit for the “System on Panel” application because of its simplicity and low power dissipation [6.11] – [6.13].

The multi-channel structure mentioned in chapter 2 is applied to the driving TFT in the conventional source follower to improve the uniformity of output voltage performance in this section. Furthermore, a new simple source follower type circuit mentioned in previous chapter using low-temperature polycrystalline silicon thin film transistors as analog buffer for the integrated data driver circuit of active matrix liquid crystal displays and active matrix light emitting diodes is fabricated and measured in this chapter. In addition to the threshold voltage difference of driving TFTs, the unsaturated of output voltage arisen from the significant sub-threshold current will also result in the difficulty of the buffer circuit design. An active load is added and a calibration operation is applied to study the influences on the source follower circuit. The proposed circuit is capable of minimizing the variation from both the signal timing and the device characteristics through the measured results.

6.2 Measured Results of the Effect of Transistor Slicing Layout Method on Conventional Analog Buffer Circuit

As mentioned previously, LTPS TFTs adopted multi-channel structure with slicing layout has been proved to enhance uniformity. For further investigations, the multi-channel structure is applied to the driving TFT in the conventional source follower shown in Fig. 6-1. The device dimension was set to 100μm/8μm and divided into five or ten strips compared with signal channel. Besides, the data loading capacitance is assumed 15pF, and the fabrication process is the same as chapter 2. The measurement system is the same as probing AMOLED pixel signal except the oscilloscope changed to Aglient MSO 6034A.

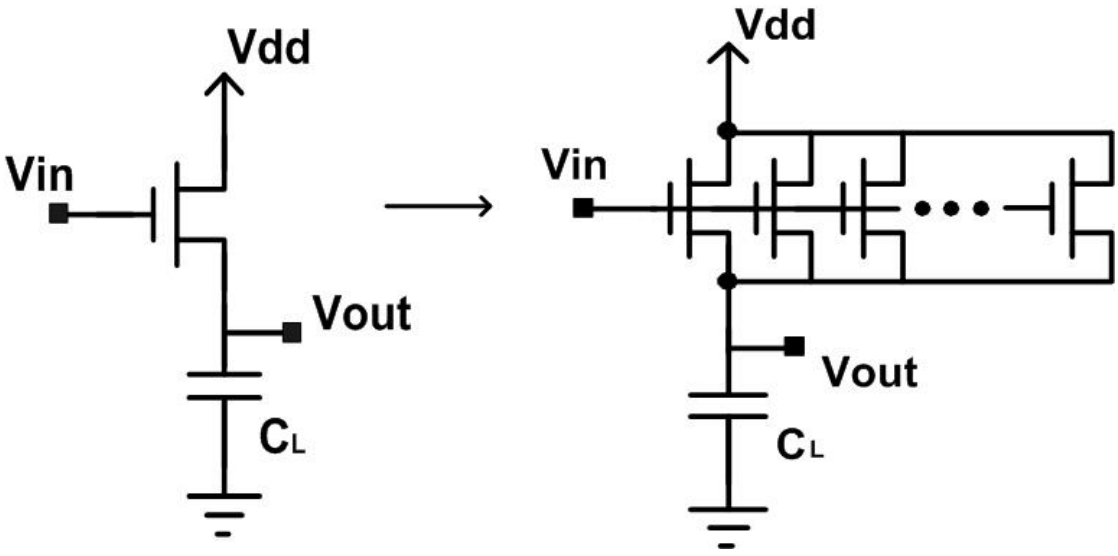

Fig. 6-1. Schematic configuration of the conventional analog buffer with the signal channel (left) and multi-channel (right) driving TFT.

Fig. 6-2 shows the ten sets measured results of the offset voltage (Vin-Vout) variations versus varied input voltages employed single channel structures. Large output offset voltage variations are shown in this figure even above 1600mV clearly. On the other hand, multi-channel structures with ten stripes are adopted in Fig. 6-3, while the offset voltage variation is greatly reduced and controlled below 900mV. In order to have obvious comparison, two figures are combined in Fig. 6-4. It is more

obvious that multi-channel structure improves the uniformity applied to the conventional source follower circuits. In conclusion, multi-channel structure of LTPS-TFTs can improve uniformity not only in device level but also in circuit level. The similar multi-channel structure results of improving uniformity have been proved in the AMOLED pixel circuit shown in chapter 4.

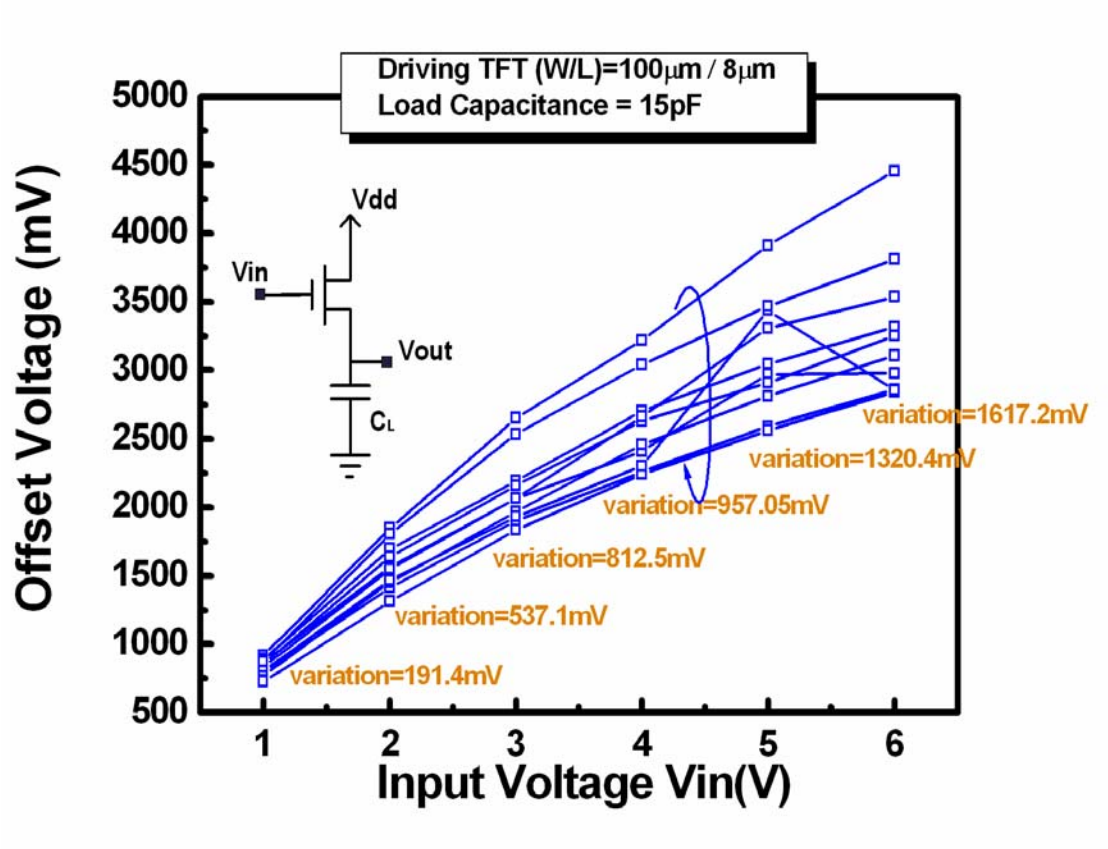

Fig. 6-2. Ten sets measured results of the offset voltage (Vin-Vout) variations versus varied input voltages employed single channel structures.

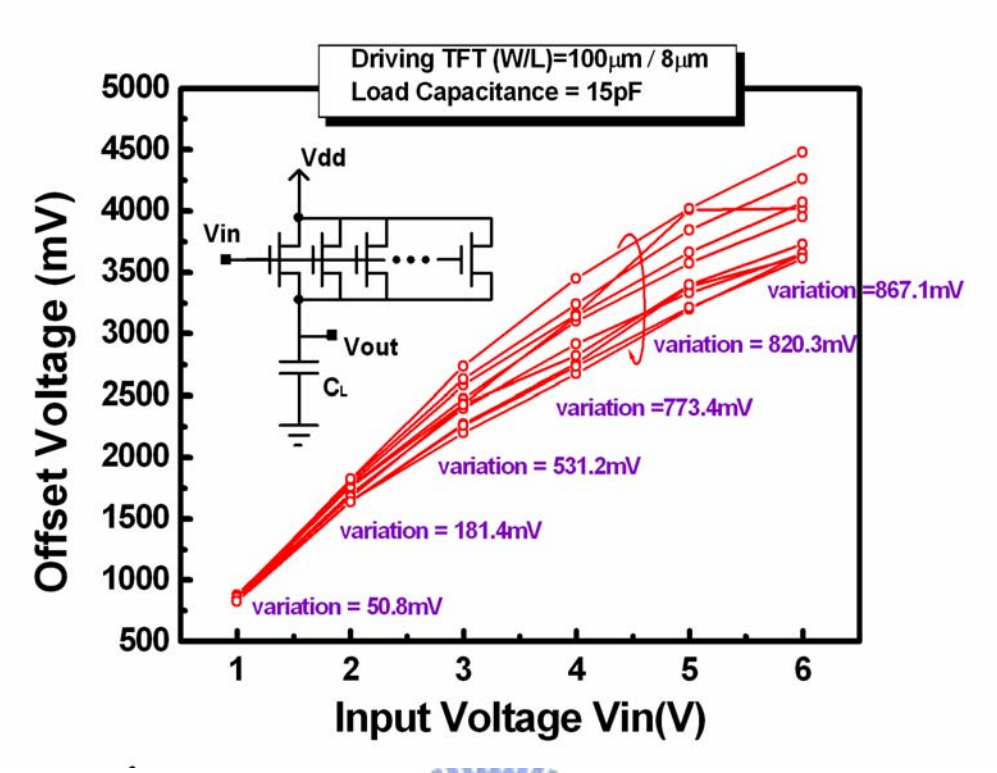

Fig. 6-3. Ten sets measured results of the offset voltage (Vin-Vout) variations versus varied input voltages employed multi-channel structures.

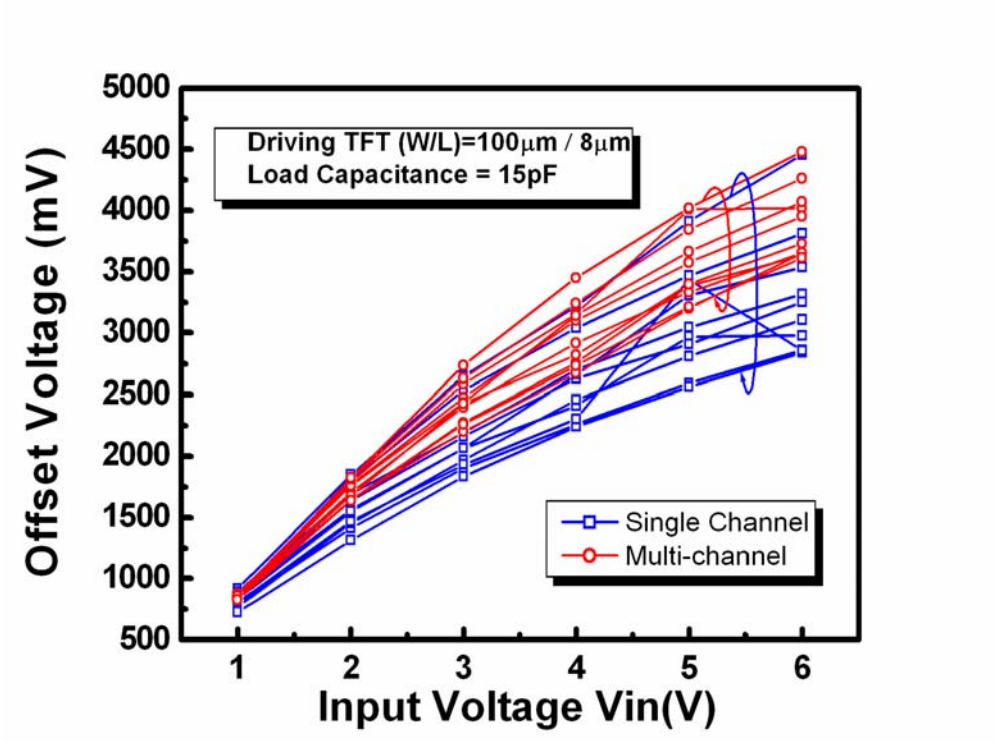

Fig. 6-4. Comparison of the measured output offset voltage variations between the single channel and multi-channel structure.

6.3 Proposed Source Follower Type Analog Buffer Fabrication and Measured Results

After the output buffer circuit design finished, several buffer circuits were fabricated and measured. The proposed analog buffer is fabricated using a LTPS CMOS process and measured to study the performance of the analog buffer. The fabrication process is described as follow. A buffer oxide and 500Å-thick a-Si was first deposited on the glass substrate sequentially. Then the amorphous silicon thin film was crystallized to poly-crystalline silicon film by KrF excimer laser. After the active region was defined, the channel doping procedure was carried out for adjusting the threshold voltage of n-type TFT. Then, high dose ion implantation was executed to source/drain regions of n-type TFT. Next, 1000 Å-thick gate oxide was deposited by plasma enhanced chemical vapor deposition (PECVD). A 3000Å-thick Cr film was deposited afterwards. Then, the gate oxide and the Cr film were etched to form the gate electrode. After that, a high dose self-aligned ion implantation was executed to form source/drain regions of p-type TFT, and a 4000Å-thick SiNx was deposited by PECVD as interlayer. Finally, the test circuits for the proposed analog buffer were accomplished after the contact holes formation and the 4000Å-thick Cr metallization. Fig. 6-5 shows the optical micrograph of proposed circuit after fabrication.

The measurement system includes four units mentioned in chapter 4: probe station and parameter analyzer, pulse generator for providing control signal pulse, programmable electrometer for supplying DC signal voltage, and oscilloscope to display the output signal. After probing system ready for measuring, several proposed analog buffer and conventional analog buffer circuits were measured and gathered

statistics. Fig. 6-6 shows comparison the offset voltage with different data voltages of the conventional and proposed analog buffers. It is observed that the output voltage of proposed analog buffer is closely equal to actual input voltage. On the other hand, the offset voltage of conventional analog is mostly above 1V which is large compared with proposed analog buffers. The proposed analog buffer output deviation is controlled under 50 mV regardless of threshold voltage variation showing extremely good results. We also measured eight sets data in each source follower circuits shown in Fig. 6-7. The figure shows that offset voltage of conventional analog buffer suffers huge variations and the proposed analog buffer has small output variability and better uniformity after threshold voltage calibration.

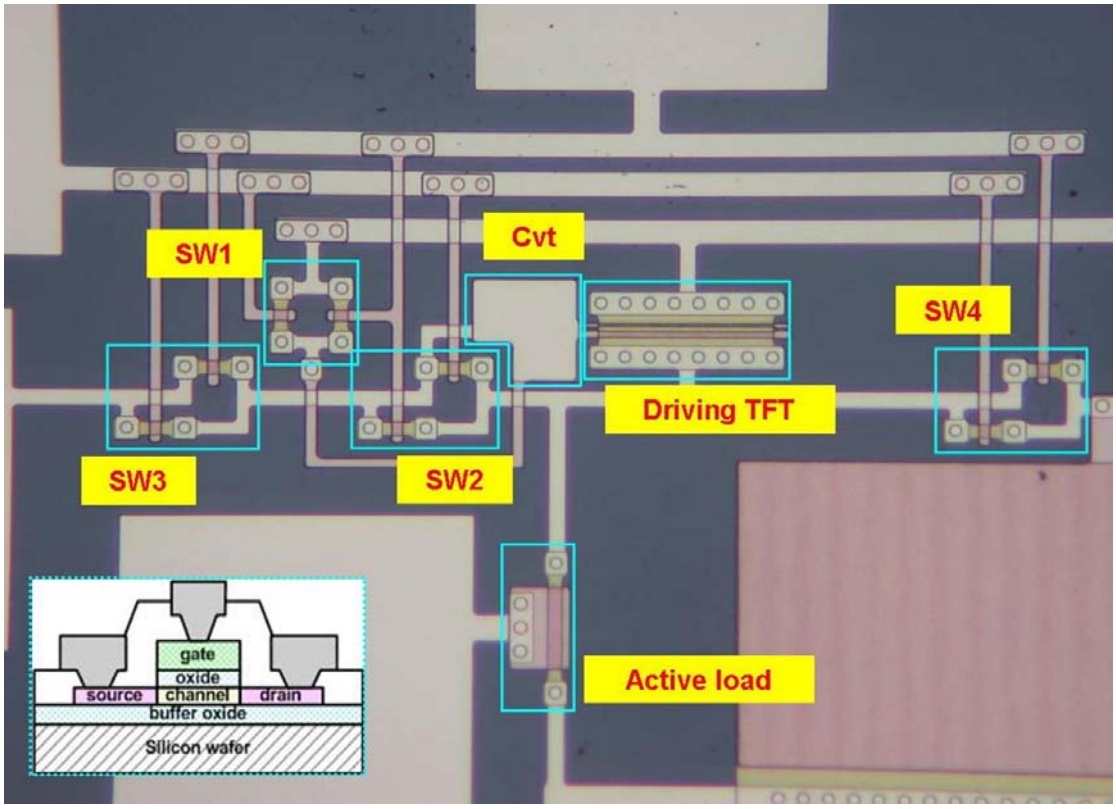

Fig. 6-5. The optical micrograph of the proposed of fabricated circuit.

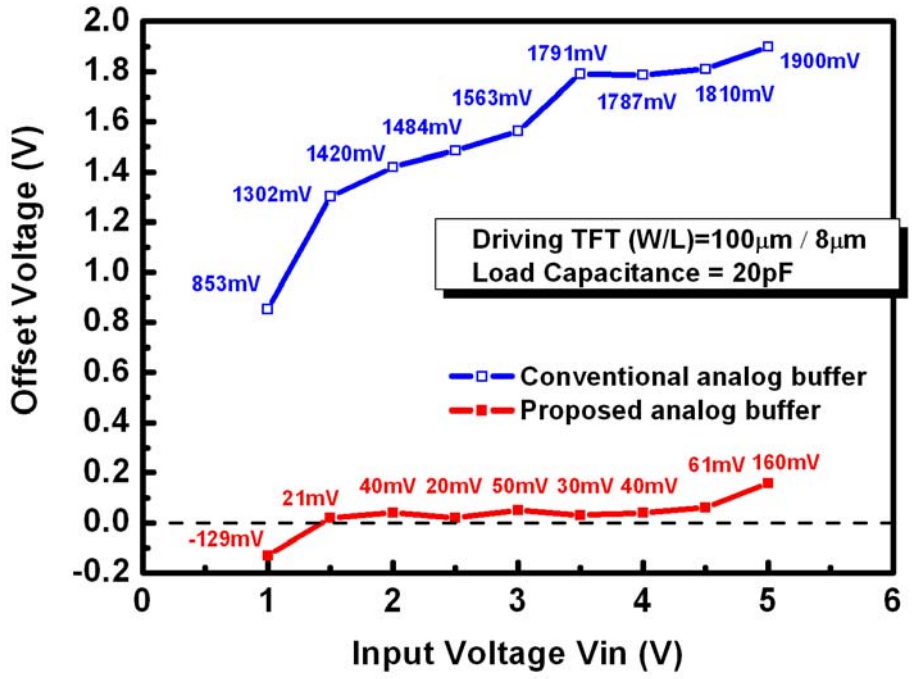

Fig. 6-6. Comparison of the measured offset voltage versus input voltage curve of the conventional and proposed analog buffers.

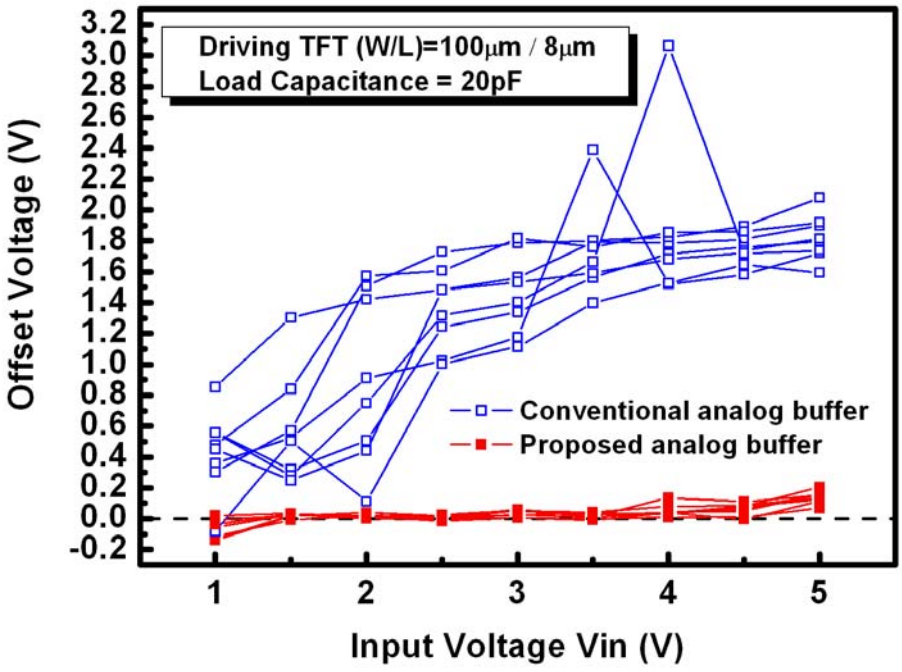

Fig. 6-7. Variations of eight buffer circuits between the offset voltage versus input voltage of the conventional and proposed analog buffers.

6.4 Bias Voltage Effects on Offset Voltage

The main source of the error in the output voltage is due to the small output resistance of the LTPS-TFTs [6.13]. In this section, the operation mode of the driving TFT and the active load will be discussed in detail. During the compensation period, the driving TFT and the active load are both working in the saturation region since the Vdd power line compensation where Vbias just turns on the active load. Nevertheless, during the data input period, the active load operates in linear or saturation region depending on input data voltage while the driving TFT still works in the saturation region. We divide it into two conditions for below discussing.

A. Driving TFT in saturation region, active load in saturation region while data input period

These results can be expressed by the mathematical formula as follows:

(We assumed that the driving TFT as TFT1 and the active load as TFT2 here for convenience)

(1)Compensation period:

$$I_D = K_1(V_{GS1} - V_{TH1})^2 = K_2(V_{GS2} - V_{TH2})^2$$

$$\rightarrow K_1(V_{DD} - V_{out} - V_{TH1})^2 = K_2(V_{bias} - V_{TH2})^2$$

$$\rightarrow a = \sqrt{K_1 / K_2} = \frac{V_{bias} - V_{TH2}}{V_{DD} - V_{out} - V_{TH1}}$$

$$aV_{DD} - aV_{out} - aV_{TH1} = V_{bias} - V_{TH2}$$

$$V_{out} = V_{DD} - V_{TH1} + \frac{1}{a}V_{TH2} - \frac{1}{a}V_{bias}$$

$$\therefore Cvt\_storage\_\Delta V = V_{DD} - V_{out} = V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias} \quad \text{..... (6.1)}$$

(2)Data input period:

$$I_D = K_1(V_{in} + \Delta V - V_{out} - V_{TH1})^2 = K_2(V_{bias} - V_{TH2})^2$$

$$\rightarrow a = \sqrt{K_1 / K_2} = \frac{V_{bias} - V_{TH2}}{V_{in} + (V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias}) - V_{out} - V_{TH1}}$$

$$\rightarrow aV_{in} - V_{TH2} + V_{bias} - aV_{out} = V_{bias} - V_{TH2}$$

$$\Rightarrow V_{out} = V_{in} \quad \text{..... (6.2)}$$

The equation (6.1) indicates that the variation of driving TFT and the active load both can be stored for the compensation during the operation period. Therefore, the equation (6.2) shows the output voltage equal to the input voltage theoretically.

B. Driving TFT in saturation region, active load in linear region while data input period

(1)Compensation period:

During the first operation period, the situation is the same as described previously which the voltage stored in the capacitor depending on the threshold voltage, bias voltage and the K_1/K_2 ratio.

(2)Data input period:

$$I_D = K_1(V_{in} + \Delta V - V_{out} - V_{TH1})^2 = K_2[(V_{bias} - V_{TH2})V_{out} - \frac{1}{2}V_{out}{}^2]$$

$$\rightarrow a^2[V_{in} + \Delta V - V_{out} - V_{TH1})^2 = (V_{bias} - V_{TH2})V_{out} - \frac{1}{2}V_{out}{}^2$$

from equation (1) : $\Delta V = V_{DD} - V_{out} = V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias}$

$$\rightarrow a^2[V_{in} + (V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias}) - V_{out} - V_{TH1}]^2 = (V_{bias} - V_{TH2})V_{out} - \frac{1}{2}V_{out}{}^2$$

$$\Rightarrow V_{out} = \underbrace{\frac{2(V_{bias}-V_{TH2})+4a(V_{bias}-V_{TH2})+4a^2V_{in}}{2(1+2a^2)}}_{\textbf{(A)}} +$$

$$\underbrace{\frac{\sqrt{[(4a+2)(V_{bias}-V_{TH2})+4aV_{in}]^2-4(2a^2+1)[2(V_b^2+V_t^2)]+4aV_{in}(V_{bias}-V_{TH2})+2a^2V_{in}{}^2-4V_{bias}V_{TH2}}}{2(2a^2+1)}}_{\textbf{(B)}}$$

We assume that $2a^2>>1$ and $4a>>2$

(A) term can be simplified to $V_{in}+\frac{(V_{bias}-V_{TH2})}{a}+\frac{(V_{bias}-V_{TH2})}{2a^2}$

(B) term :

$$\frac{\sqrt{[(4a+2)(V_{bias}-V_{TH2})+4aV_{in}]^2-4(2a^2+1)[2(V_b^2+V_t^2)]+4aV_{in}(V_{bias}-V_{TH2})+2a^2V_{in}{}^2-4V_{bias}V_{TH2}}}{2(2a^2+1)}$$

$$\approx \frac{\sqrt{[(4a)(V_{bias}-V_{TH2})+4aV_{in}]^2-4(2a^2)[2(V_b^2+V_t^2)]+4aV_{in}(V_{bias}-V_{TH2})+2a^2V_{in}{}^2-4V_{bias}V_{TH2}}}{4a^2}$$

$$\rightarrow \frac{\sqrt{0}}{4a^2}$$

Therefore, the output voltage can be simplified as

$$V_{out} = V_{in} + \frac{(V_{bias}-V_{TH2})}{a} + \frac{(V_{bias}-V_{TH2})}{2a^2} \qquad \text{……..…. (6.3)}$$

According to the equation (6.3) proved, the output voltage almost equal to the input voltage when the Vbias nearly just above V_{TH2} and the large factor a in design theoretically. The mobility of the driving TFT and the active load are almost equal. Therefore, the driving TFT is designed larger W/L ratio and the active load is designed smaller W/L ratio to possess large factor a coinciding with previously design in section III. The larger factor a, the output voltage is more accurate. However, the optimum design parameters must be confined to the display specifications.

The Fig. 6-8 shows the simulation results of offset voltage and power dissipation

related to bias voltage. It is shown that the offset voltage has optimum value around 2V which the active load just nearly turns on and leads to the active load biasing in the saturation region. The power dissipation also increases with the bias voltage in the same input data voltage. The Fig. 6-9 shows the comparison of the offset voltage versus bias voltage curve of the simulation and measured results when input voltage 3V. It is observed that the measured result trend is close to the simulation results. It shows that the offset voltage defined by Vin minis Vout turns from positive to negative value as bias voltage increasing, and a minimum offset voltage exists as the bias voltage is in the range between 2V to 2.5V. The tendency can be understood by the detailed discussion on the operation of driving TFT and the active load. During the compensation period, driving TFT is in the saturation region while the active load is also operated in the saturation region. However, during the data input period, the active load may operate in the saturation or the linear region depending on the bias voltage while the driving TFT is still in the saturation region. As the bias voltage is lower than the input voltage, the active load will operate in the saturation region and the output voltage is very closely to the input data voltage. The simulation and measured results of input voltage 2V also shown in Fig. 6-10 exhibiting the same trend. The larger bias voltage is the larger offset voltage is. Proper design of the bias voltage is required to achieve total performance.

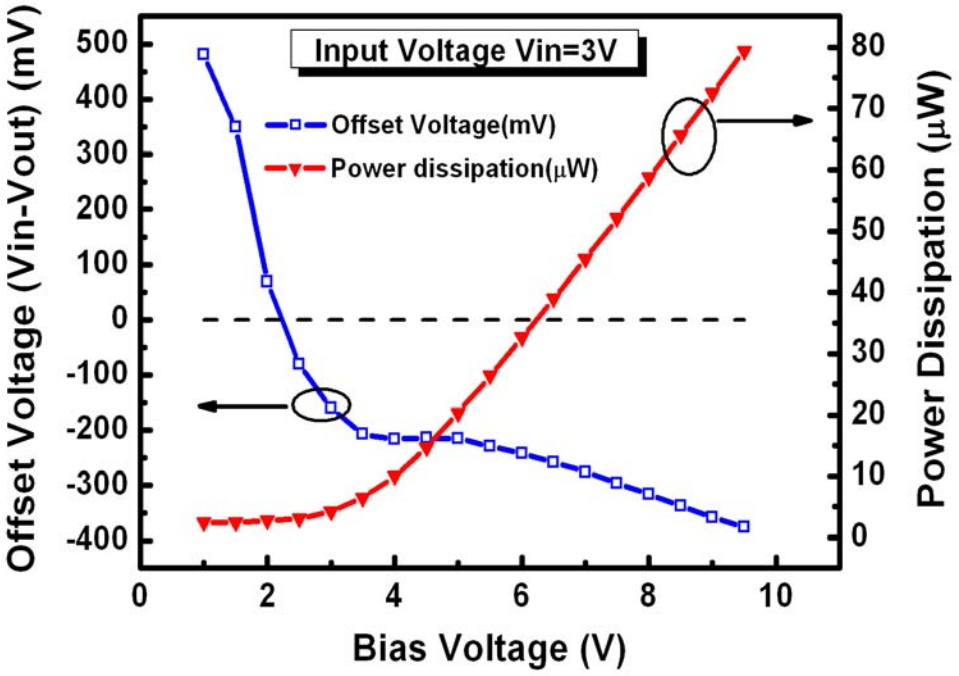

Fig. 6-8. Simulation results of the output offset voltage and the power dissipation for the proposed analog buffer with different bias voltage.

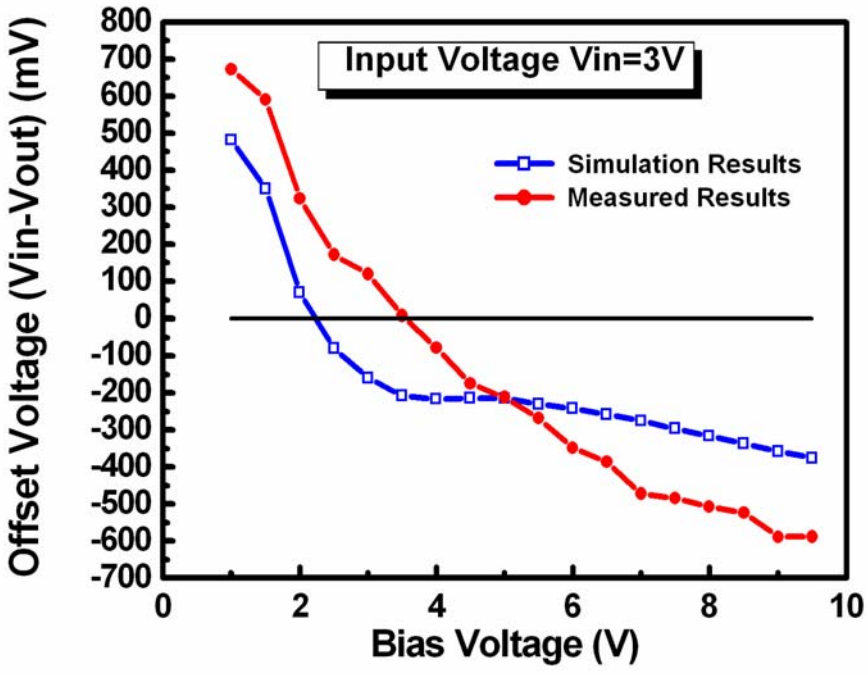

Fig. 6-9. Comparison of the offset voltage versus bias voltage curve of the simulation and measured results when input voltage 3V.

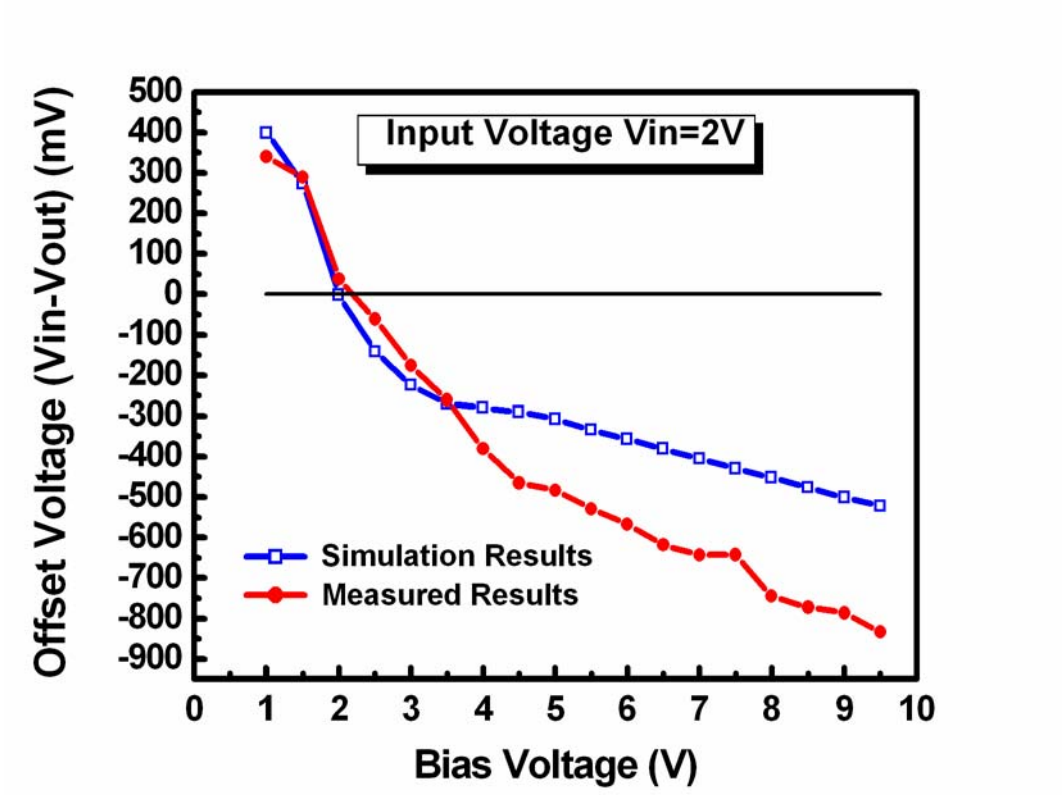

Fig. 6-10. Comparison of the offset voltage versus bias voltage curve of the simulation and measured results when input voltage 2V.

6.5 Summary

From the study of chapter 2, LTPS TFTs adopted multi-channel structure with slicing layout has been proved to enhance uniformity. Therefore, multi-channel structure is applied to the driving TFT in the conventional source follower. Large offset voltage variations above 1600mV in the conventional structure. On the other hand, multi-channel structure with ten strips is adopted, while the offset voltage variation is greatly reduced and controlled below 900mV. It is clear that multi-channel structure improves the uniformity applied to the conventional source follower circuits.

In this chapter, a novel source follower type analog buffer have been presented

and measured, where the driving circuit is formed by only two n-type thin film transistors, one capacitor, and four switches. The large mismatch of LTPS-TFTs in threshold voltage is compensated and output voltage comes very close to the actual input voltage. Much improved output voltage stability and simple configuration are achieved by adding the bias circuit and the compensation operation. Through the simulation, measured and formula proved results, the proposed source follower type analog buffer is capable of minimizing both of the variations from signal timing and the device varied characteristics remarkably. Regarding bias voltage, proper design of the bias voltage is required to achieve excellent performance.