國立交通大學

電子工程學系　電子研究所碩士班

碩士論文

應變矽金氧半導體場效電晶體的量子模擬

Quantum Simulation of Strained Si MOSFET

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中華民國九十三年六月

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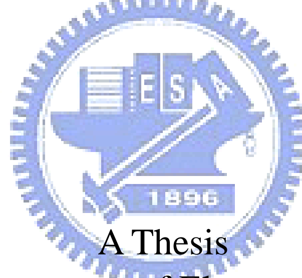

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應變矽的金屬氧化物半導體場效電晶體

之量子模擬

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摘　要

在本論文中，我們建構了可以模擬應變矽的金氧半場效電晶體元件的程式，該程式可以自我相容地解一維的Schrödinger和Poisson方程式，利用這個程式，我們研究了一些應變矽元件的量子化特性，特別是元件在彈道傳輸下的效能極限，以及直接穿隧的閘極漏電流。最後，我們提出並檢驗一種利用應變矽的雙閘極元件的架構，以量產的觀點來說，這種元件比傳統的雙閘極元件更具實用價值且有更好的元件特性。

Quantum Simulation of Strained Si MOSFET

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Abstract

A 1-D self-consistent Schrödinger-Poisson solver for dealing with strained Si MOSFETs has been successfully constructed in this thesis. Several quantum mechanical properties of strained Si devices have also been studied, especially the ballistic performance limit and the gate direct tunneling current. Finally, a strained double gate device has been proposed and examined. This new device might provide a more practical way from the manufacturability point of view while being able to create device performance superior over traditional double gate devices.

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由衷地感謝所有幫助我完成論文的人

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Chapter 1

Introduction

Recently, strained MOSFET has played an important role on the way toward the nano-scale device. Because strain changes the material's band structure, the carrier transport in the channel of the strained MOSFET has different manners than those in the unstrained one. The appropriate use of the strain can improve the device performance strikingly. Several strain technologies had been reported, which essentially can be categorized into two methods: one is substrate-induced strain and another is process strained Si (PSS). The substrate induced strain technology uses the substrate composed of the two lattice-mismatch layers. Due to this lattice mismatch, a biaxial stress is induced in the substrate. The Si stacking on $Si_{1-X}Ge_X$ is commonly utilized. The process strained Si employs special process technique to generate strain in the channel, including STI PSS, Cap-layer PSS, and Silicide PSS [1].

To understand the influence of strain on the electrical properties of the strained MOSFET is very important to the device modeling, and 1-D quantum simulation is necessary to conduct this issue. Because of the simple distribution of the strain, substrate induced strain in terms of the stacking Si on $Si_{1-X}Ge_X$ has been studied widely. In this thesis, we develop a program to quantum mechanically simulate the strained Si device on a MOS system and also examine the transport properties of interest.

In Chapter 2, SCHRED, a 1-D un-strain silicon quantum simulator from the Purdue University, which constitutes a basis for our strain version development, is introduced. The changes made in this source code to account for strain properties are detailed in Chapter 3, along with simulation results on the strained Si MOSFETs (Si

on $Si_{1-x}Ge_x$). In Chapter 4, we use the simulation results to study the effect of the strain on the direct tunneling gate current. In Chapter 5, a new strained silicon double gate device is proposed and examined via the developed quantum simulator. Finally, a brief conclusion is drawn in Chapter 6.

Chapter 2

1-D Quantum Mechanical Simulator

2.1 Description of the Program

As the MOSFET dimension scales down, the quantum effect is more and more important. Beside the concerned phenomena induced by the quantum effect, like poly-gate depletion and threshold voltage shift, the so-called subband engineering is also an attractive subject. To study these quantum phenomena, the self-consistent Schrödinger-Poisson simulation is needed. In this chapter, we introduce a 1-D quantum mechanical simulator developed by the group at the Purdue University [2], and another quantum mechanical simulator developed by our group. In addition, the performance limit of the device also serves as important guide during device development. In this chapter, the ballistic transport or transport without scattering is examined and linked to this limit.

SCHRED, a program developed by the group at the Purdue University [2], can quantum mechanically simulates a MOS system associated with traditional MOSFETs and double gate devices. This program solves the following equations simultaneously:

$$\frac{\partial^2 V}{\partial z^2} = \frac{\rho}{\varepsilon} \qquad \text{(Poisson equation)} \qquad (1)$$

$$\frac{-\hbar^2}{2m_Z}\frac{\partial^2}{\partial z^2}\Psi + V\Psi = E\Psi \qquad \text{(Schrödinger equation)} \qquad (2)$$

For the two-fold valleys, $m_Z = m_l$, and for the fourfold valleys, $m_Z = m_t$. The methods of solving Poisson equation consist of the finite difference method and the

incomplete LU method. In the underlying silicon region, Poisson equation can be written in the form

$$\frac{\partial^2 V}{\partial z^2} = \frac{-\left[\rho_{depl}(z) - e\sum_{i,j} N_{i,j}\left|\Psi_{i,j}(z)\right|^2\right]}{\varepsilon_{Si}} \tag{3}$$

Here ρ_{depl} is the depletion charge density and $N_{i,j}$, the 2-D carrier density in the subband *i* of the valley *j*, is expressed as [3]

$$N_{i,j} = \frac{m_{Di}kT}{\pi\hbar^2}\left\{\ln\left(1+e^{(E_F-E_{i,j})/kT}\right)+\ln\left(1+e^{(E_F-E_{i,j}-qV_D)/kT}\right)\right\} \tag{4}$$

The first term on the right-hand side of this equation is the contributions by the carriers injected from the source, and the second term from the drain. m_{Di} is the density of states effective mass for subband *i*; for the twofold valleys, $m_{Di} = 2m_t$, and for the fourfold valleys, $m_{Di} = 4\sqrt{m_t m_l}$. There are two extreme cases of $N_{i,j}$. One is for $V_D = 0$, the equilibrium case:

$$N_{i,j} = \frac{2m_{Di}kT}{\pi\hbar^2}\left\{\ln\left(1+e^{(E_F-E_{i,j})/kT}\right)\right\} \tag{5}$$

Another is the non-equilibrium case at $V_D >> 0$ where the carriers from the drain are suppressed, namely

$$N_{i,j} = \frac{m_{Di}kT}{\pi\hbar^2}\left\{\ln\left(1+e^{(E_F-E_{i,j})/kT}\right)\right\} \tag{6}$$

The shooting method are used to solve 1-D Schrödinger equation with the boundary conditions $\Psi = 0$ at the oxide-silicon interfaces. To describe the shooting method, let us rewrite the time-independent Schrödinger equation in the form:

$$\frac{d^2\psi}{dz^2} + k^2(z)\psi(z) = 0, \quad k(z) = \sqrt{\frac{2m^*}{\hbar^2}[E - V(z)]} \tag{7}$$

When discretized on a uniform mesh, one gets that:

$$\psi_{i+1} - \left(2 - k_i^2\Delta^2\right)\psi_i + \psi_{i-1} = 0 \tag{8}$$

Then,

1. Integrate the Schrödinger equation towards larger z from z_{min} with

$$\psi_{i+1} = (2 - k_i^2\Delta^2)\psi_i - \psi_{i-1}\ ; \tag{9}$$

2. Integrate the Schrödinger equation towards smaller z starting from z_{max} with

$$\psi_{i-1} = (2 - k_i^2\Delta^2)\psi_i - \psi_{i+1}; \tag{10}$$

3. At the matching point $z_{m,}$ one matches the solutions resulting from 1 and 2, and then renormalized the Ψ ; and
4. The eigenvalue is then signaled by equality of the derivatives at z_m:

$$\left.\frac{d\psi^{<}}{dz}\right|_{z_m} = \left.\frac{d\psi^{>}}{dz}\right|_{z_m} \quad \Rightarrow \quad f = \frac{1}{\psi}\left[\psi^{<}(z_m - \Delta) - \psi^{>}(z_m - \Delta)\right] \tag{11}$$

When the channel length is much smaller than the mean free path of the carrier, the carrier can propagate through the channel from the source to the drain without any scatterings. This is called ballistic transport. For the ballistic limit, the injection velocity is [3]:

$$v_{inj}^{i} = \sqrt{\frac{2k_B T m_{ci}}{\pi m_{Di}^2}}\left(\frac{\Im_{1/2}\left[(E_F - \varepsilon_i)/k_B T\right]}{\ln(1+e^{(E_F-\varepsilon_i)/k_B T})}\right) \tag{12}$$

where $\Im_{1/2}[x]$ is the Fermi-Dirac integral of order one half as defined by Blakemore [4]. $m_{c,i}$ is the conductivity effective mass; for the twofold valleys, $m_{c,i} = 4m_t$ and for the fourfold valleys, $m_{c,i} = 4\left(\sqrt{m_t} + \sqrt{m_l}\right)^2$. The ballistic current can then be calculated:

$$I_{BALLISTIC} = \sum_{i,j} qN_{i,j} v_{inj}^{i,j} \tag{13}$$

2.2 Simulation Results

Fig.2.1 shows the wave functions simulated by the SCHRED. In this figure, we see that the wave functions of the twofold valleys are larger than those of the fourfold valleys. Because of the heavier effective mass perpendicular to the Si-oxide interface, the twofold valleys are preferential on the electron occupancy. Fig.2.2 shows that the

electrons mainly occupy the twofold valleys at the high gate voltage.

On the other hand, our developed quantum mechanical Simulator, the modified version of the SCHRED, can have more features. Fig.2.3 displays comparison of the simulated Q_{inv} between Si (110) and Si (100). For Si (110), the fourfold valleys have $m_Z = 0.315m_0$, and the twofold valleys have $m_Z = 0.19m_0$ [5]. Because the effective mass m_z of the Si (110) are lighter than those of Si (100), Si (110) has poorer ability to induce Q_{INV}.

Another new function is the simulation of the body effect. Because the quasi-Fermi level of the minority carrier is lowered down due to applied substrate bias, this gives rise to more severe band bending, as shown in Fig.2.4. The corresponding V_{th} shift is shown in Fig. 2.5.

Chapter 3

Quantum Simulation of the Strained Si Device

3.1 Simulation of the Strained Si Device

In this chapter, we show the results of quantum mechanical simulation for the strained Si MOSFET using our developed QM Simulator, and compare with those from Takagi, et al. [6,7].

MOSFET fabricated on strained Si layer pseudomorpically grown on $Si_{1-x}Ge_x$ has better device performance than that on bulk Si. Because of the lattice mismatch between Si and $Si_{1-x}Ge_x$, the induced biaxial tensile stress on Si layer lowers the conduction band minima of the twofold degenerate valleys relative to that of the fourfold degenerate valleys by 0.67x, and the valance band maxima of the light hole are lower than that of the heavy hole by $0.44x + 0.219x^2 - 0.142x^3$ [8], as shown in Fig. 3.1. For NMOS, the energy lowering of the twofold valleys makes them more dominant on electron occupancy. As a result, the lighter conductivity mass of the twofold valleys and the suppression of the intervalley scattering between the twofold and fourfold valleys enhance the device performance [7].

The following expressions concerning the dependences of material parameters on the Ge content x have been incorporated in the our simulator:

$$\chi_{Si} = 4.05 + 0.67x \quad [9] \tag{14}$$

$$E_{g,Si} = 1.12 - 0.754x + 0.161x^2 - 0.2072x^3 + 0.058282x^4 \quad [10] \tag{15}$$

$$\Delta Ec = Ec(4\ fold) - Ec(2\ fold) = 0.67x \tag{16}$$

$$\Delta Ev = Ev(heavy) - Ev(light) = 0.44x + 0.219x^2 - 0.142x^3 \qquad (17)$$

where χ_{Si} is the electron affinity of the strained Si, $E_{g,Si}$ is the bandgap of the strained Si, ΔE_C is the conduction band splitting between the fourfold and twofold valleys, and ΔE_v is the valence band splitting between heavy hole and light hole.

The following are the 3-D electron and hole density for the strained Si:

$$n = \frac{1}{3}\left(12\left(\frac{2\pi m^* kT}{h^2}\right)\right)^{\frac{2}{3}} \frac{2}{\sqrt{\pi}} \Im_{\frac{1}{2}}\left(\frac{E_F - E_C}{kT}\right) + \frac{2}{3}\left(12\left(\frac{2\pi m^* kT}{h^2}\right)\right)^{\frac{2}{3}} \frac{2}{\sqrt{\pi}} \Im_{\frac{1}{2}}\left(\frac{E_F - E_C - \Delta E_C}{kT}\right) \qquad (18)$$

$$p = 2{m_{hh}}^{1.5}\left(\frac{2\pi m_0 kT}{h^2}\right)^{1.5} \frac{2}{\sqrt{\pi}} \Im_{\frac{1}{2}}\left(\frac{E_V - E_F}{kT}\right) + 2{m_{hl}}^{1.5}\left(\frac{2\pi m_0 kT}{h^2}\right)^{1.5} \frac{2}{\sqrt{\pi}} \Im_{\frac{1}{2}}\left(\frac{E_V - \Delta E_V - E_F}{kT}\right) \qquad (19)$$

Here, $\Im_{1/2}[x]$ is the Fermi-Dirac integral of order one half, $m^*=(m_l m_t^2)^{1/3}$, and m_{hh} and m_{hl} are the effective mass of the heavy and light hole, respectively. The first term on the right-hand side of (18) is the electron density from the twofold valleys and the second term from fourfold valley. The first term on the right-hand side of (19) is attributed to the heavy hole and the second is attributed to the light hole.

Furthermore, in the QM Simulator, we assume that the thickness of the strained layer is thick enough (typically, 60nm) to eliminate the effect of the discontinuity between Si and $Si_{1-X}Ge_X$. As a result, we only concern on the strained Si layer during our simulation. If the thickness of the strained Si layer is thin, the $Si_{1-x}Ge_x$ layer must be taken into account because the Si-$Si_{1-x}Ge_x$ discontinuity will influence the simulation results, as indicated in [9].

In addition, we neglect the variation of the curvature of the energy band. It means that we assume the effective mass of the carrier is constant with the strain.

Indeed, the effective mass of the carrier is a weak function of the strain [10].

3.2 Simulation Results

In this section, the strained Si device was examined using the developed QM simulator. Fig.3.2, Fig.3.3 and Fig.3.4 show the comparisons between our results and those from Takagi's research team. Obviously, comparable agreements are achieved. In addition, we also see that the electron occupancy of the twofold valleys increase strikingly as a result of the strain.

In Fig.3.5, the improvement of the v_{inj} due to the strain is apparent. More results such as in Fig.3.6 confirm that the strained Si device is a good choice to achieve low voltage application.

Chapter 4

Effect of Strain on Direct Tunneling Gate Current

4.1 Model for Direct Tunneling Current

In this chapter, we use the previous results to study the gate direct tunneling current for the strained Si device. The gate current contributed by the carrier direct tunneling through the gate oxide is very important for the modern device. So how the Ge content of the strained device affects the direct tunneling current is of interest to us. Although the direct tunneling current can be modeled accurately by the fully quantum mechanical simulation, but it is not efficient. An analytic model for direct tunneling current has been proposed [11],[12]. This method is simple and feasible for moderate to low gate voltage regime.

According to the model [11],[12], the gate current is

$$J = \sum_{i,j} J_{i,j} = \sum_{i,j} Q_{i,j} T / \tau \tag{20}$$

where $J_{i,j}$ is the tunneling current contributed by the carrier $Q_{i,j}$ in the ith subband of the jth valley, and T and τ are the tunneling probability and lifetime of that subband, respectively.

As shown in Fig.4.1, electrons in each subband have different probabilities to tunnel through the gate oxide. The transmission probability can be approximated by

$$T = T_{WKB} T_R \tag{21}$$

where T_{WKB} is the usual WKB tunneling probability valid for smoothly varying

potentials, and T_R is the correction factor for the reflections from the potential discontinuities.

The T_{WKB} is expressed as

$$T_{WKB} = \exp\left[\frac{E_g \sqrt{2m_{OX}}}{4\hbar q F_{OX}} \left(2\gamma' \sqrt{\gamma} + \sqrt{E_g} \sin^{-1} \gamma' \right) \Bigg|_{E_{OX}=q\phi_{an}}^{E_{OX}=q\phi_{cat}} \right] \tag{22}$$

where

$$q\phi_{cat} = q\chi_c - (E_{Si,\perp} + E_{Si,||}) \tag{23}$$

$$q\phi_{an} = q\chi_c - (E_{Si,\perp} + E_{Si,||}) - qF_{OX} t_{OX} \tag{24}$$

$$\gamma = E_{OX} \left(1 - \frac{E_{OX}}{E_G}\right) \tag{25}$$

$$\gamma' = \left(1 - \frac{2E_{OX}}{E_g}\right) \tag{26}$$

In above equations, $q\phi_{cat}$ and $q\phi_{ab}$ are the barrier heights at the cathode and anode interfaces, respectively. m_{OX} (=0.61m_0) and E_g (=9eV) are the effective mass and bandgap of oxide, respectively. $qF_{OX}t_{OX}$ is the potential drop across the oxide. $E_{Si,\perp}$ and $E_{Si,//}$ are the electron energy perpendicular and parallel to the interface of Si and oxide, respectively. χ_c is the discontinuity between the Si and SiO_2 conduction bands with a value of 3.15 eV.

The correction factor T_R is expressed as

$$T_R = \frac{4v_{Si,\perp}(E_{Si,\perp})v_{OX}(q\Phi_{cat})}{v^2{}_{Si,\perp}(E_{Si,\perp})+v^2{}_{OX}(q\Phi_{cat})} \times \frac{4v_{Si,\perp}(E_{Si,\perp}+qF_{OX}t_{OX})v_{OX}(q\Phi_{an})}{v^2{}_{Si,\perp}(E_{Si,\perp}+qF_{OX}t_{OX})+v^2{}_{OX}(q\Phi_{an})} \tag{27}$$

where

$$v_{OX} = \frac{1}{\gamma'}\sqrt{\frac{2\gamma}{m_{OX}}} \tag{28}$$

$$v_{Si,\perp} = \sqrt{\frac{2E_{Si,\perp}}{m_{Si,\perp}}} \tag{29}$$

where $v_{Si,\perp}(E_{Si,\perp})$ and $v_{Si,\perp}(E_{Si,\perp}+qF_{OX}t_{OX})$ are the group velocities of the electrons incident and leaving the oxide, respectively, and $v_{OX}(q\Phi_{cat})$ and $v_{OX}(q\Phi_{an})$ are the magnitudes of the purely imaginary group velocity of electrons at the cathode side and anode side within the oxide, respectively.

$\tau_{i,j}$, the tunneling lifetime of the electrons from the *i*th energy subband of the *j*th valley, can be written as:

$$\tau_{i,j} = \frac{j\pi\hbar}{E_{i,j}} \tag{30}$$

Finally, the direct tunneling current contributed by the *i*th subband of the *j*th valley can be evaluated analytically:

$$J_{G,i,j} = \left.\frac{Q_{i,j}T}{\tau_{i,j}}\right|_{E_{Si,\Pi}=\frac{1}{2}(E_F-E_{Si,\perp})} \tag{31}$$

4.2 Results of Simulation

With the method described above and our simulation results of the strained Si, we now discuss the effect of strained Si on direct tunneling current. Fig.4.2 and Fig.4.3 reveal the relationship between gate current and V_G in linear and log scale, respectively. These figures show a certain critical gate voltage above which the gate current decreases with increasing Ge content and below which the gate current increases with increasing Ge content. Furthermore, in Fig.4.4, the gate currents contributed by twofold valleys are dominant at low gate voltage, and they increase with increasing Ge content. On the other hand, the gate currents contributed by fourfold valleys are on the order of those contributed by twofold at high gate voltage or low Ge content. Obviously, the gate currents due to fourfold valleys decrease with increasing Ge content dramatically.

Fig.4.5 shows the difference of direct tunnel current between equilibrium and non-equilibrium conditions. In this figure, we see that the non-equilibrium state of MOSFET increases the gate leakage current at high gate voltage, and this degradation is relaxed as the Ge content increases. But at low gate voltage, the non-equilibrium state exhibits a reduction in the gate leakage current, and it is less pronounced as the Ge content increases.

4.3 Discussion

We explain the above results as follows. Although the potential barrier for the electron in the twofold valleys increase with increasing Ge content, the increasing rate of Q_{INV} at low gate voltage is much higher than that at high gate voltage, as shown in Fig.4.6. As a result, the increasing Ge content increases the gate leakage current at low gate voltage but suppresses the gate leakage current at high gate voltage. Fig.4.7

are the experiment data from AMD [13]. Although the process conditions of this device may be different from our simulation conditions, the figure shows the same trend as the simulation.

Chapter 5

Effect of Strain on Double Gate Device

5.1 Simulation of DG Device

In this chapter, double gate device simulation, another function of Purdue's program, is studied. A modified version of this program to study another kind of double gate strained Si device is developed.

DG device is one of the future device candidates because of its superior device performance over the single gate device. As mentioned in Chapter 2, the wave function of the fourfold valleys is larger than that of the twofold valleys. This means that the subband energy of the fourfold valleys tend to increase as the thickness of Si layer in the DG device shrinks to the comparable size of the wave function of the fourfold valleys. As a result, the energy difference in the lowest subband between the two valley groups is widening. Such quantum confinement effect makes the twofold valleys more preferential on electron occupancy, and results in the improvement of the mobility due to the suppression of the intervally scattering between the two- and fourfold valleys [12].

Fig.5.1 shows the wave function simulated by Purdue's program for the DG device with 5nm Si layer. Because of the space confinement of the wave function, their shapes are quite different from those in Fig.2.1. Fig.5.2 shows that the energy difference between the lowest subband of the two valley groups is widening as the result of space confinement.

5.2 Simulation of the Strained DG Device

Now, we propose another kind of double gate strained Si device. The device structure is shown in Fig.5.3. Fig.5.3(a) depicts that Si(100) is pseudomorpically grown on $Si_{1-x}Ge_x$. A narrow line with (100) sidewall surface is formed after etching the strained Si. Then, after growing the thermally oxide on the sidewall, metal gate is formed. Finally, this device is fin-FET like device. The top view of this device is schematically shown in Fig.3.3(b). Fig.5.4 schematically displays the constant energy surface of conduction band as viewed from the top of this device, where valley A denotes the twofold degenerate valleys with the energy lowering of 0.67x by the bottom strained Si, and valley B and C denote the twofold degenerate valleys perpendicular and parallel to the interface between the oxide and Si, respectively. For valley A, $m_{Di} = 2\sqrt{m_t m_l}$, $m_{c,i} = 4m_l$, for valley B, $m_{Di} = 2m_t$, $m_{c,i} = 4m_t$, and for valley C, $m_{Di} = 2\sqrt{m_t m_l}$ $m_{c,i} = 4m_t$.

Unlike the traditional DG device, the fourfold degenerate valleys are further spit into two twofold degenerate valleys. Because of the energy lowering, valley A is preferential on the electron occupancy. As a result, the intervalley scattering between any two valleys is suppressed and thereby only the intravalley scattering of the valley A needs to be concerned. Theoretically, this device should have better device performance. Unlike the subband engineering of the traditional DG device by the space confinement, this new DG device use both strain and space confinement to change the subband. Thus, this device can undergo subband engineering even for thick Si layer.

5.3 Results of Simulation

With this idea in mind, our QM simulator is suitable to simulate this device by

modifying Purdue's program. Fig. 5.5 and Fig. 5.6 show simulated $I_{BALLISTIC}$-V_G curves for t_{Si}=2nm and t_{Si}=50nm, respectively. For the thicker t_{Si}, the inclusion of Ge in substrate can improve the ballistic current. However, the inclusion of Ge degrades the performance for the thinner t_{Si}. To exploit it more, the effects of Ge content on the ballistic current and v_{inj} for various t_{Si} under fixed Q_{INV} are shown in Fig. 5.7 and Fig. 5.8, respectively. Obviously, there is a lower limit of t_{Si} to improve device performance by the inclusion of Ge in substrate. Fig. 5.9 and Fig.5.10 reveal the variation of electron occupancy of valley A and valley B for various t_{Si} under different Ge contents.

5.4 Discussion

We explain the above results as follows. At thicker t_{Si}, the main mechanism of subband engineering is energy splitting of conduction band induced by strain. This energy splitting makes the valley A preferential on electron occupancy so that the inclusion of Ge improves the device performance. However, as t_{Si} shrinks further, another mechanism of subband engineering, space confinement, which makes valley B preferential on electron occupancy and competitive with the previous mechanism. As a result, the inclusion of Ge degrades the device performance at thin t_{Si}.

Unlike the traditional DG device, which favors thin t_{Si}, this strained silicon device enhances the device performance at thick t_{Si}, but degradations occur at thin t_{Si}. Thus, a critical thickness of Si exist, which is found to be the thickness the space confinement starts to influence the wave function of the inversion charge. This critical thickness is about a few nanometer (~5nm in this case), and it continues to shrink as the dopping concentration of Si increases. Such thickness is not practical in view of

manufacture. This means that the strained Si provide a more practical way to improve device performance better than traditional DG device.

Chapter 6

Conclusion

Quantum simulation of strained Si device is successful developed. The simulated gate current via direct tunneling mechanism exhibits distinct dependencies on Ge content and gate voltage. Finally, a new strained DG device with better performance than traditional DG device is proposed and examined.

References

[1] C.Ge, et al., " Process Strained Si CMOS Featuring 3D Strain Engineering, " IEDM, p.73, 2003.

[2] http://www.nanohub.purdue.edu.

[3] F. Assad, Z.Ren, D.Vasileska, S.Datta, and M.Lundstrom, " On the performance Limits for Si MOSFET's:A Theoretical Study, " IEEE Transactions on Electron Device, 47, p.232, 2000.

[4] J.Blakemore, " Approximation of the Fermi-Dirac integrals, especially the function $\Im_{1/2}[x]$, used to describe electron density in a semiconductor, " Solid State Electronics, 25, p1067, 1982.

[5] F.Stern, " Self-Consistent Results for n-Type Si Inversion Layers, " Physical Review B, 5, 4891, 1972.

[6] S. Takagi, L. Hoyt, J. Welser, and F. Gibbons, " Comparative Study of Phonon Limited Mobility of Two Dimensional Electrons in Strained and Unstrained Si Metal Oxide Semiconductor Field Effect Transitor, " Journal of Applied Physics, 80, p.1567, 1996.

[7] S. Takagi, " Re-examination of Subband Structure Engineering in Ultra Short Channel MOSFETs under Ballistic Carrier Transport, " Symposium on VLSI Technology Digest of Technical Paper, p.115, 2003.

[8] S.Galdin, P.Dollfus, Val´erie Aubry-Fortuna, P. Hesto, and H.Osten, " Band Offset Predictions for Strained Group IV Alloys: $Si_{1-X-Y}Ge_XC_Y$ on Si(100) and $Si_{1-X}Ge_X$ on $Si_{1-Z}Ge_Z$(001), " Semicond. Sci. Technol., 15, p.565, 2000.

[9] J.Goo, Q.Xiang, Y.Takamura, F.Arasnia, E.Paton, P.Besser, J.Pan, and M.Lin, " Band Offset Induced Threshold Variation in Strained Si nMOSFETs, " IEEE Electron Device Letters, 24, p.568, 2003.

[10] M.Reiger and P.Vogl, " Electronic-band Parameters in Strained $Si_{1-X}Ge_X$ Alloys on $Si_{1-Z}Ge_Z$ Substrates, " Physical Review B, 48, p.14 276, 1993

[11] L.Register, E.Rosenbaum, and K.Yang, " Analytical Model for Direct Tunneling Current in Polycrystalline Si Gate Metal Oxide Semiconductor Devices, " Applied Physics Letters, 74, p.457, 1999.

[12] N.Yang, W.Henson, J.Hauser, and J.Wortman, " Modeling Study of Ultrathin Oxides Using Direct Tunneling Current and Capacitance-Voltage Measurements in MOS Devices, " IEEE Transactions on Electron Device, 46, p.1464, 1999.

[13] Q.Xiang, J.Goo, J.Pan, B.Yu, S.Ahmed, J.Zhang, and M.Lin, " Strained Si NMOS with Nickel-Silicide Metal Gate, " Symposium on VLSI Technology Digest of Technical Paper, p.101, 2003.

[14] S.Takagi, J.Koga, A.Toriumi, " Subband Structure Engineering for Performance Enhancement of Si MOSFETs, " IEDM, p.219, 1997.

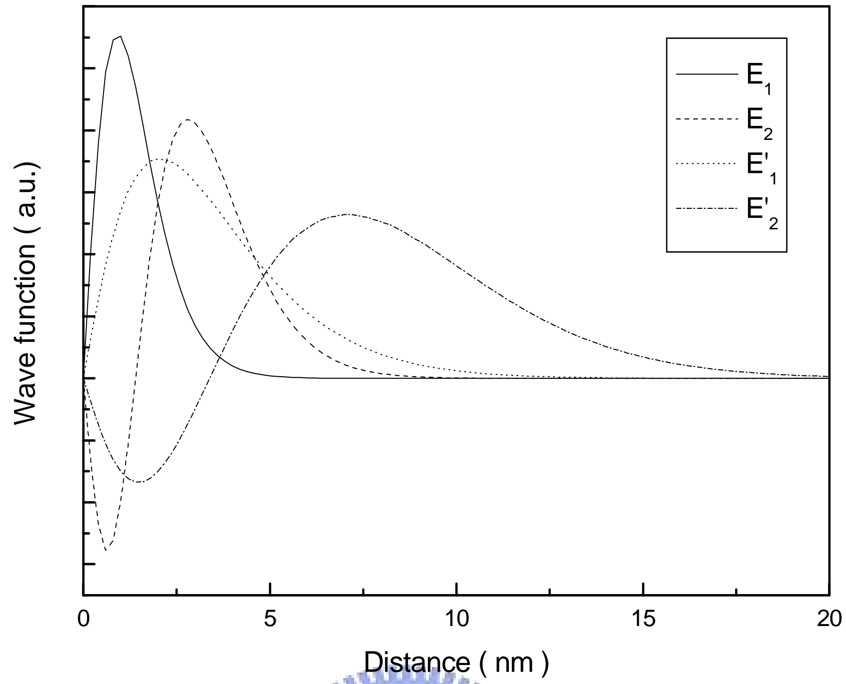


Fig.2.1 Wave function distribution

Simulation condition:

Metal gate with Φ=4.05 eV; N_{SUB} =1*10^{16} cm^{-3}

t_{OX} = 1.65*10^{-9} m; Temp=300K; and V_G=1.2 V.

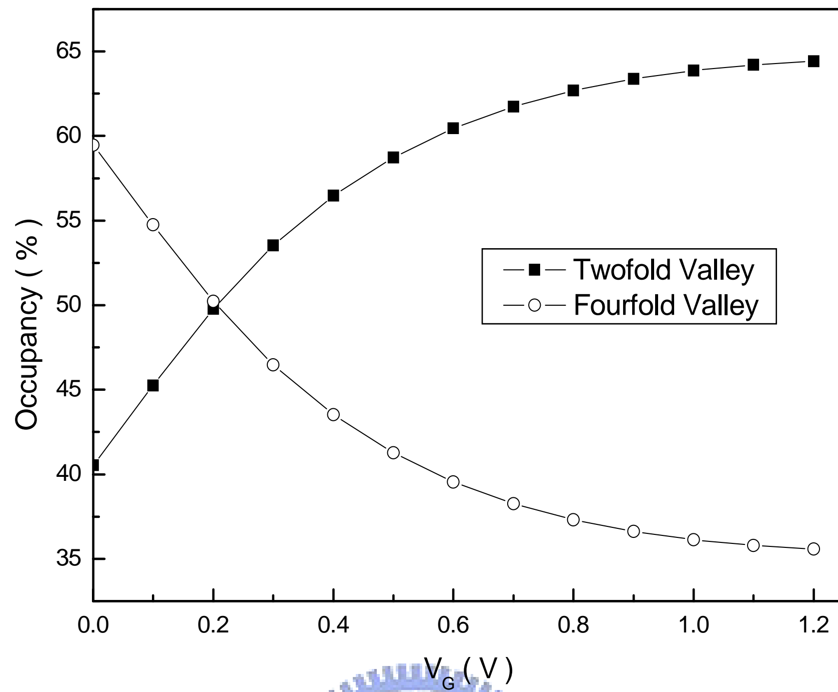


Fig.2.2 Variation of valley's occupancy verse V_G

Simulation condition:

Metal gate with Φ=4.05 eV; N_{SUB} =1*10^{16} cm^{-3};

t_{OX} = 1.65*10^{-9} m; and Temp=300K.

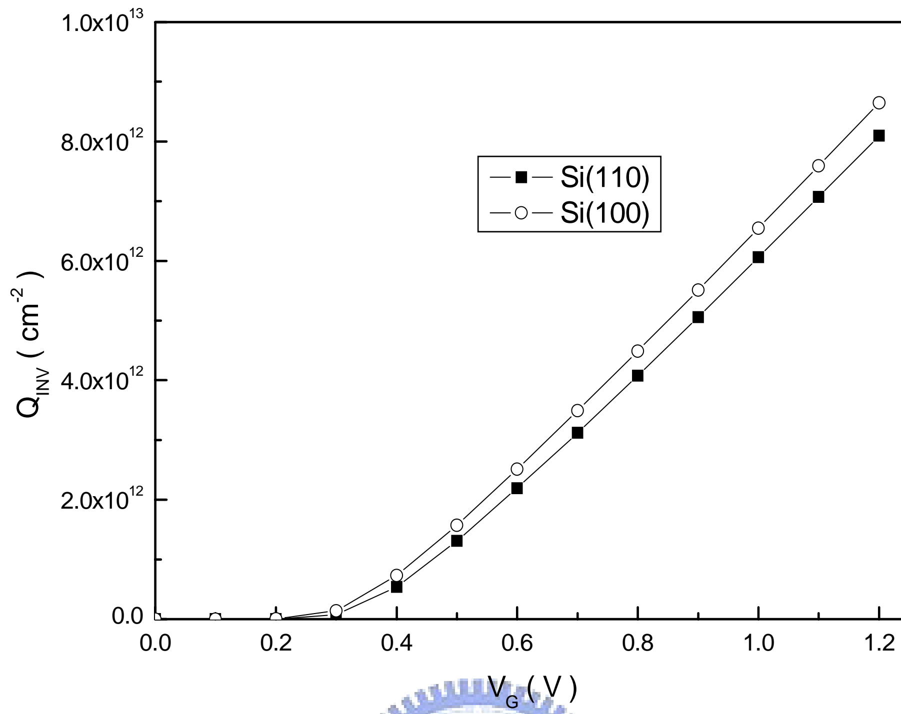


Fig.2.3 Comparison of induced Q_{INV} between Si(100) and Si(110).

Simulation condition:

Metal gate with Φ=4.05 eV; N_{SUB} =8*10^{17} cm^{-3}

t_{OX} = 1.65*10^{-9} m; and Temp=298K.

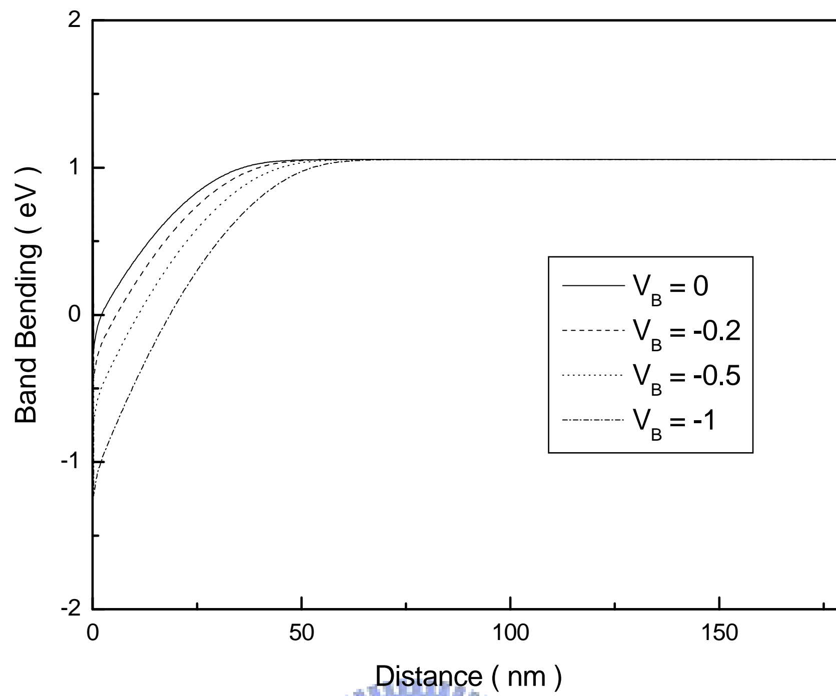


Fig.2.4 Band bending as a result of body effect.

Simulation condition:

Metal gate with Φ=4.05 eV; N_{SUB} =8*10^{17} cm^{-3};

V_G=1.2V; t_{OX} = 1.65*10^{-9} m; and Temp=298K.

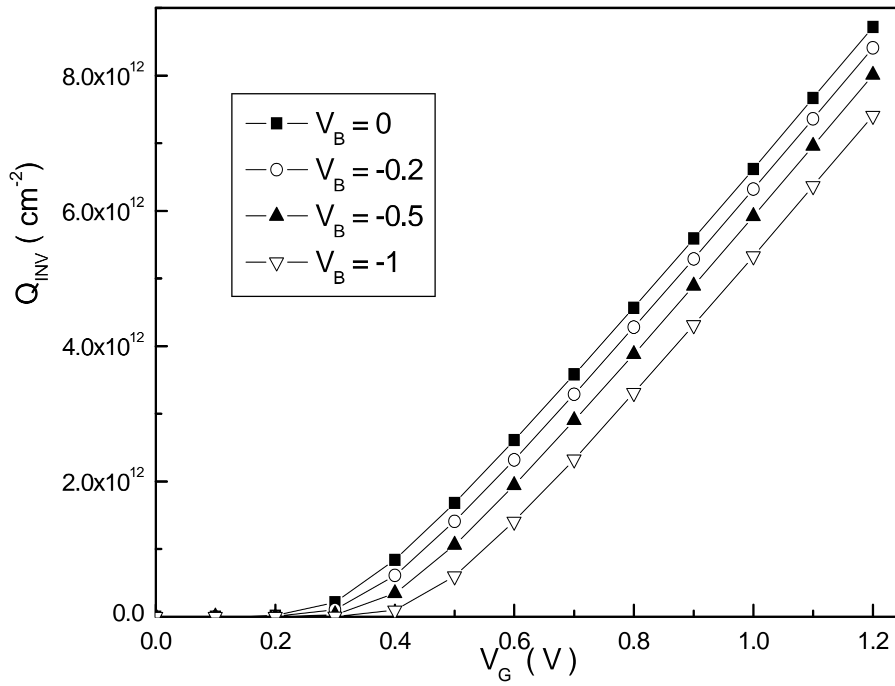


Fig.2.5 Induced Q_{INV} under body effect.

Simulation condition:

Metal gate with Φ=4.05 eV; N_{SUB} =8*10^{17} cm^{-3};

t_{OX} = 1.65*10^{-9} m; and Temp=298K.

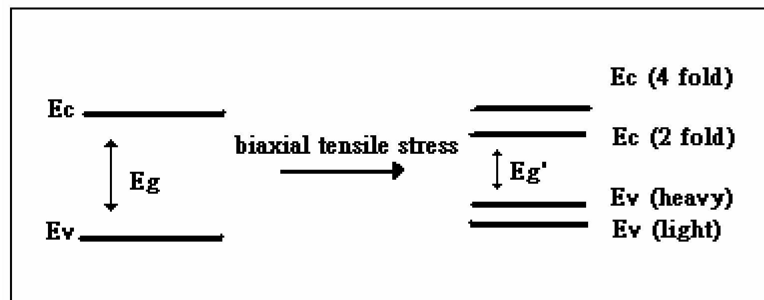


Fig.3.1 The effect of biaxial tensile strss on Si band structure.

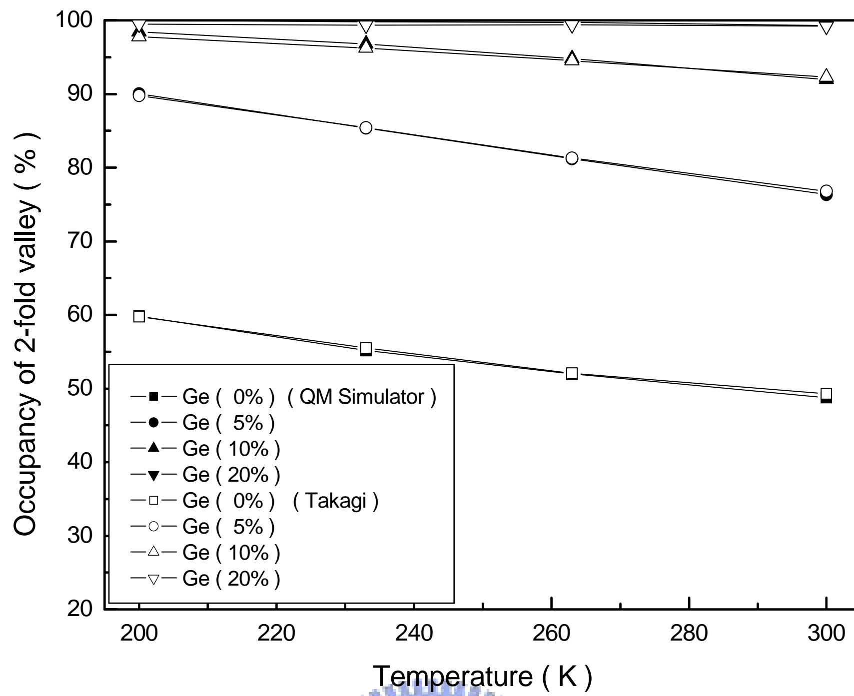


Fig.3.2 Comparison between the results from QM Simulator and Takagi [6].

Simulation condition:

Metal gate with Φ=4.05 eV; N_{SUB} =2*10^{16} cm^{-3};

t_{OX} = 1.65*10^{-9} m; Temp=300K; and Q_{INV}=1*10^{12} cm^{-2} .

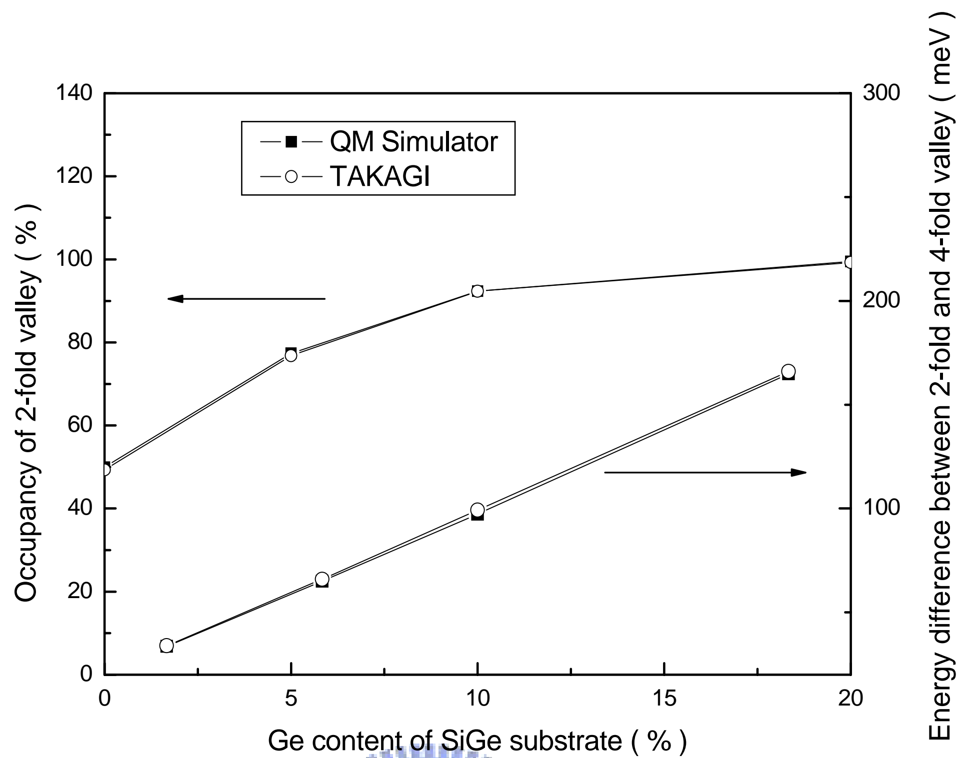


Fig.3.3 Comparison between the results from QM Simulator and Takagi [6]

Simulation condition:

Metal gate with Φ=4.05eV; N_{SUB} =2*10^{16} cm^{-3}

t_{OX} = 1.65*10^{-9} m; Temp=300K; and Q_{INV}=1*10^{12} cm^{-2}

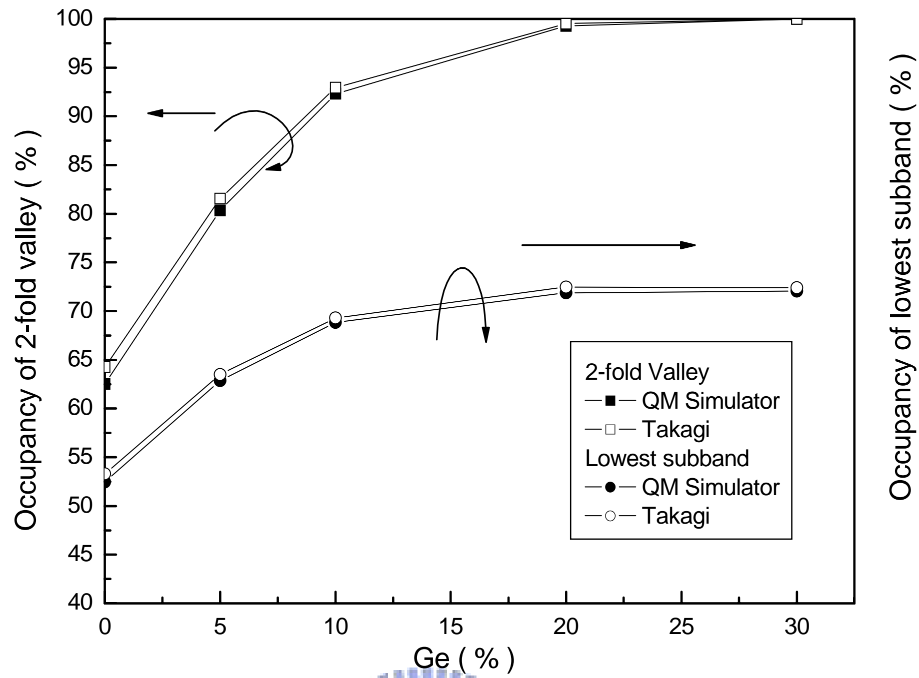


Fig.3.4 Comparison between the results from QM Simulator and Takagi[7]

Simulation condition:

Metal gate with Φ=4.05eV; N_{SUB}=1*10^{16} cm^{-3}

t_{OX} = 1.65*10^{-9} m; Temp=300K; and Q_{INV}=7*$10^{12}$$cm^{-2}$

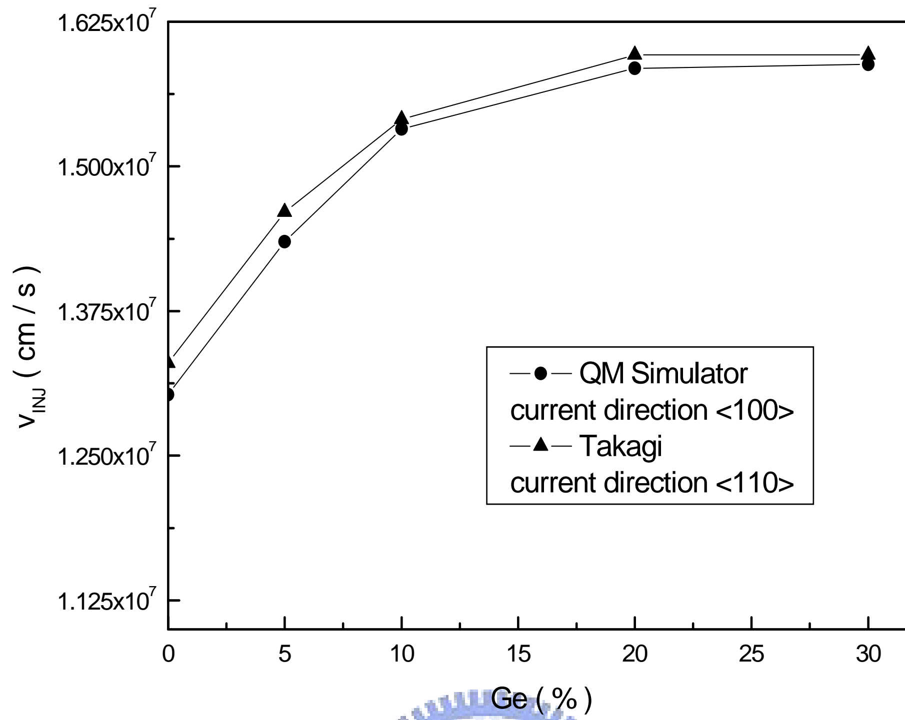


Fig.3.5 Comparison between the results from QM Simulator and Takagi[7]

Simulation condition:

Metal gate with Φ=4.05eV; $N_{SUB}=1*10^{16}$ cm^{-3}

$t_{OX} = 1.65*10^{-9}$ m; Temp=300K; and $Q_{INV}=7*10^{12}$ cm^{-2}

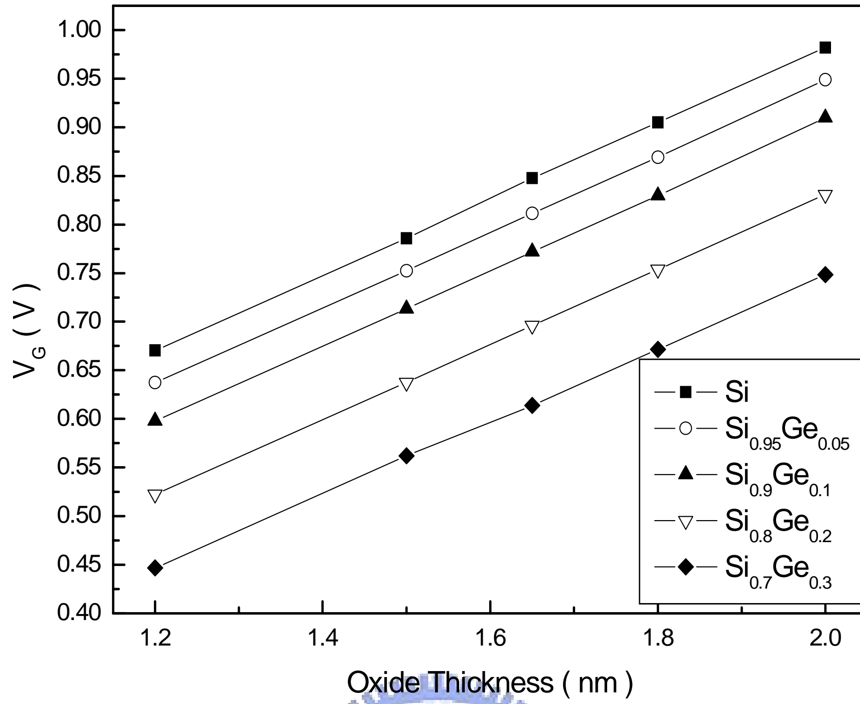


Fig.3.6 V_G for $Q_{INV}=5*10^{12}cm^{-2}$ verses oxide thickness

Simulation condition:

Metal gate with Φ=4.05eV; $N_{SUB}=8*10^{17}\ cm^{-3}$

$t_{OX} = 1.65*10^{-9}$ m; Temp=298K;

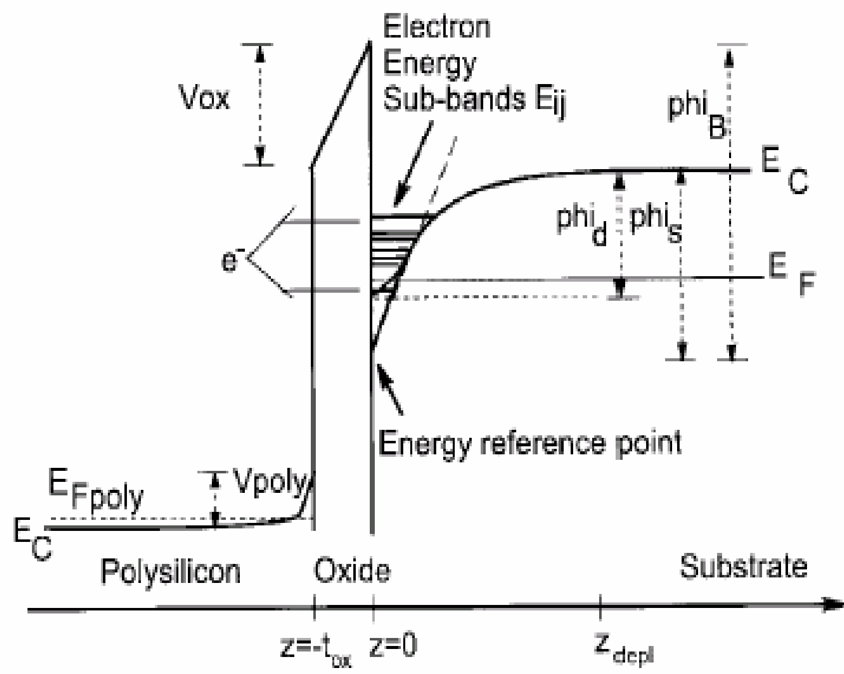
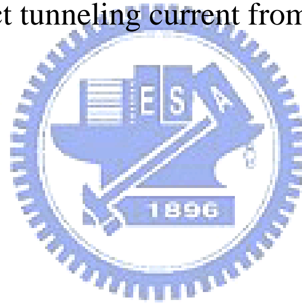


Fig.4.1 Direct tunneling current from the channel



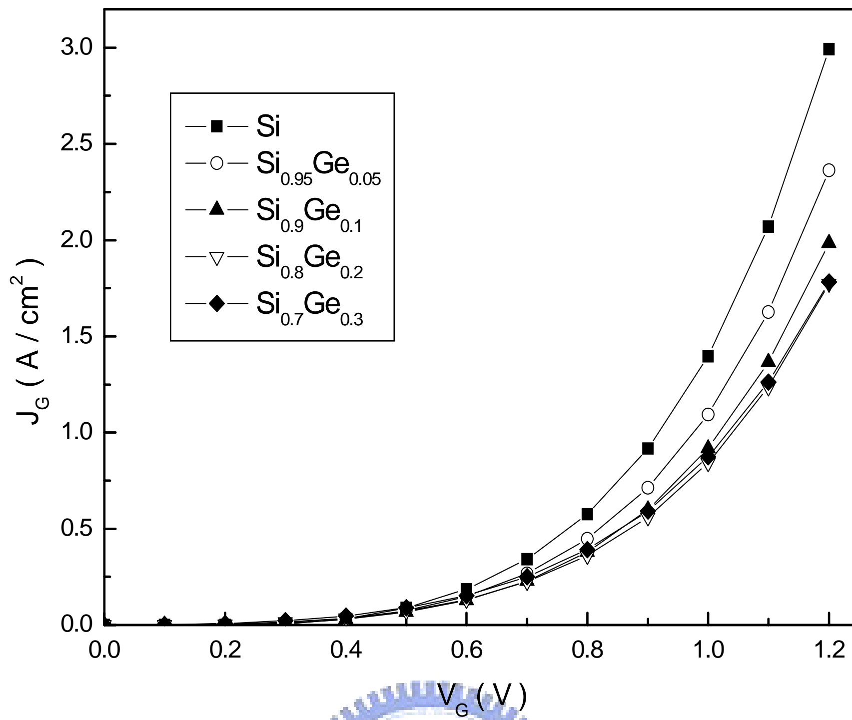


Fig.4.2 J_G for verses V_G for different Ge concentration (linear scale)

Simulation condition:

Metal gate with Φ=4.05eV;N_{SUB}=8*10^{17} cm^{-3}

t_{OX} = 1.65*10^{-9} m; and Temp=298K

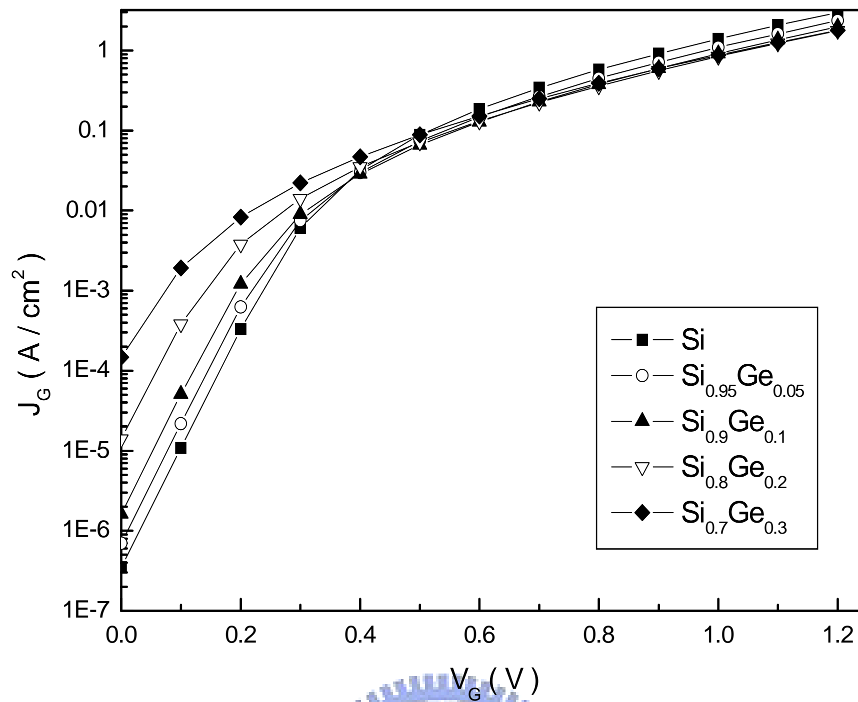


Fig.4.3 J_G for verses V_G for different Ge concentration (log scale)

Simulation condition:

Metal gate with Φ=4.05eV; N_{SUB} =8*10^{17} cm^{-3}

t_{OX} = 1.65*10^{-9} m; and Temp=298K

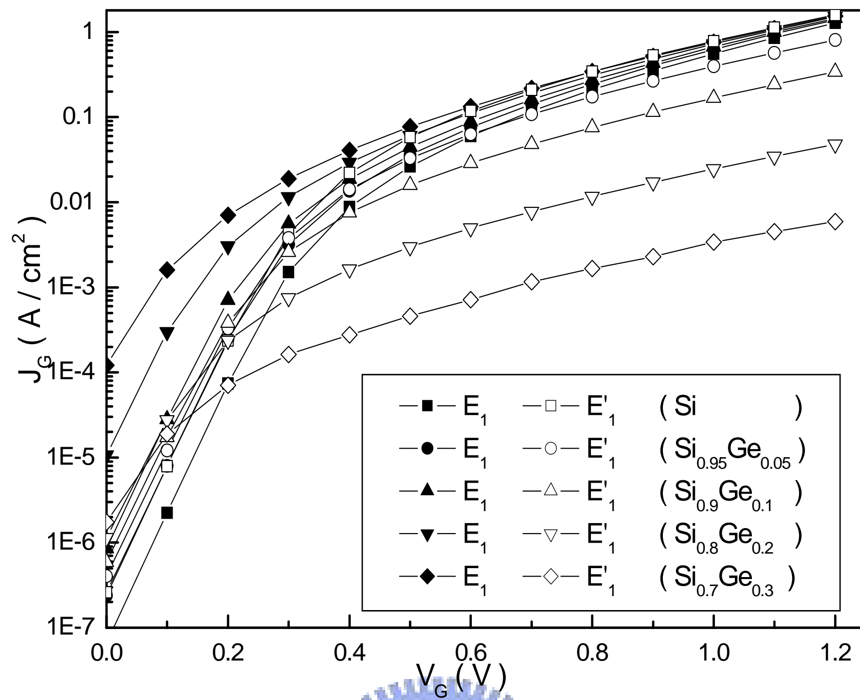


Fig.4.4 $J_{G,i}$ of each subband verses V_G for different Ge concentration

Simulation condition:

Metal gate with Φ=4.05eV; N_{SUB} =8*10^{17} cm^{-3}

t_{OX} = 1.65*10^{-9} m; and Temp=298K

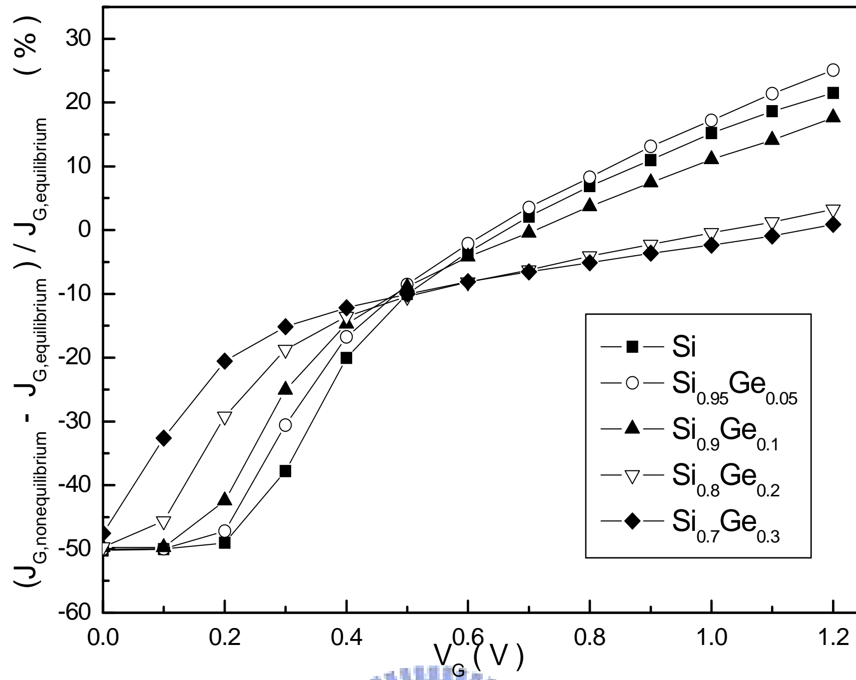


Fig.4.5 Comparison of J_G between equilibrium and non-equilibrium

Simulation condition:

Metal gate with Φ=4.05eV; N_{SUB} =8*10^{17} cm^{-3}

t_{OX} = 1.65*10^{-9} m; and Temp=298K

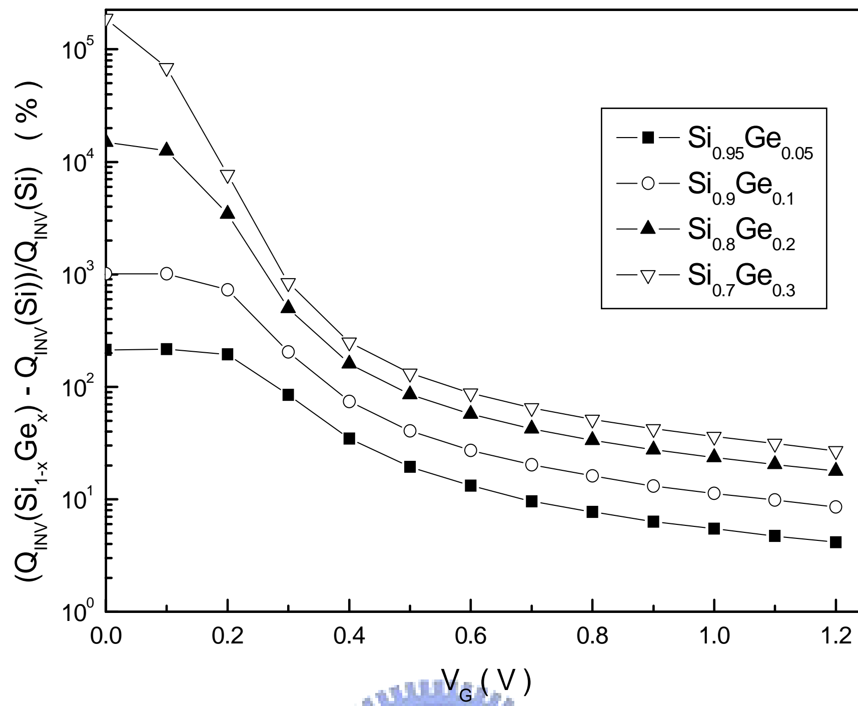
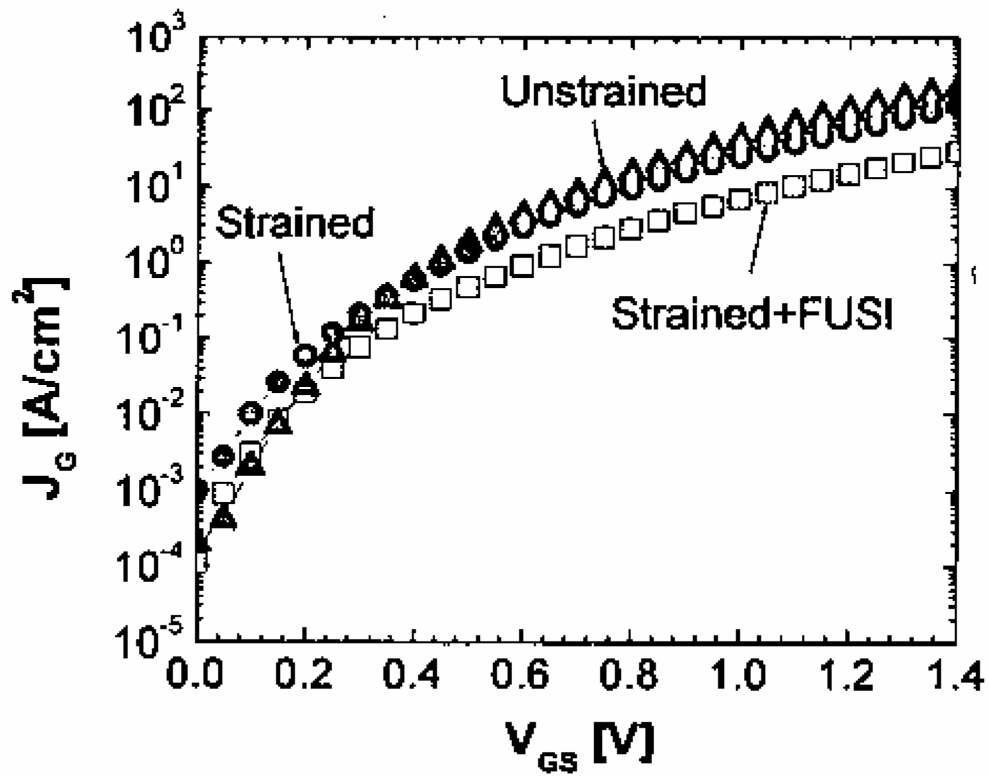


Fig.4.6 Variation of Q_{INV} vs. Ge concentration
Simulation condition:
Metal gate with Φ=4.05eV; N_{SUB} =8*10^{17} cm^{-3}
t_{OX} = 1.65*10^{-9} m; and Temp=298K



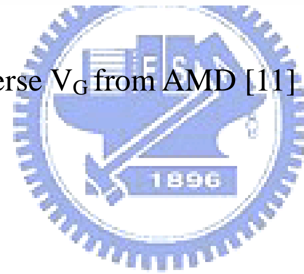


Fig.4.7 Data of J_G verse V_G from AMD [11]

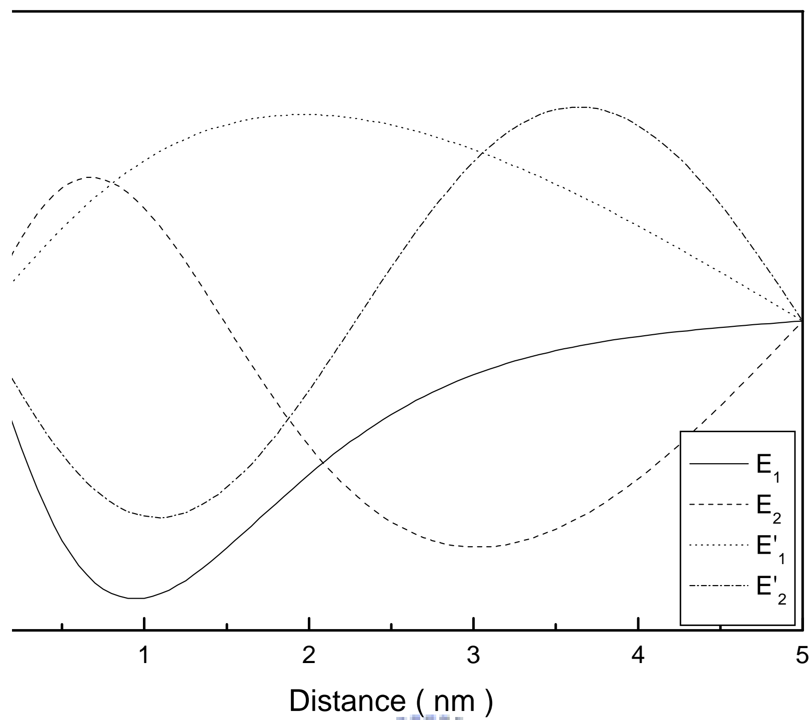


Fig.5.1 Wave function distribution

Simulation condition:

Metal gate $\Phi_1 = \Phi_1 = 4.05eV$; $N_{SUB} = 1*10^{16}$ cm^{-3}

$t_{OX,1} = t_{OX,2} = 1.65*10^{-9}$ m; Temp=300K; and t_{Si}=5nm

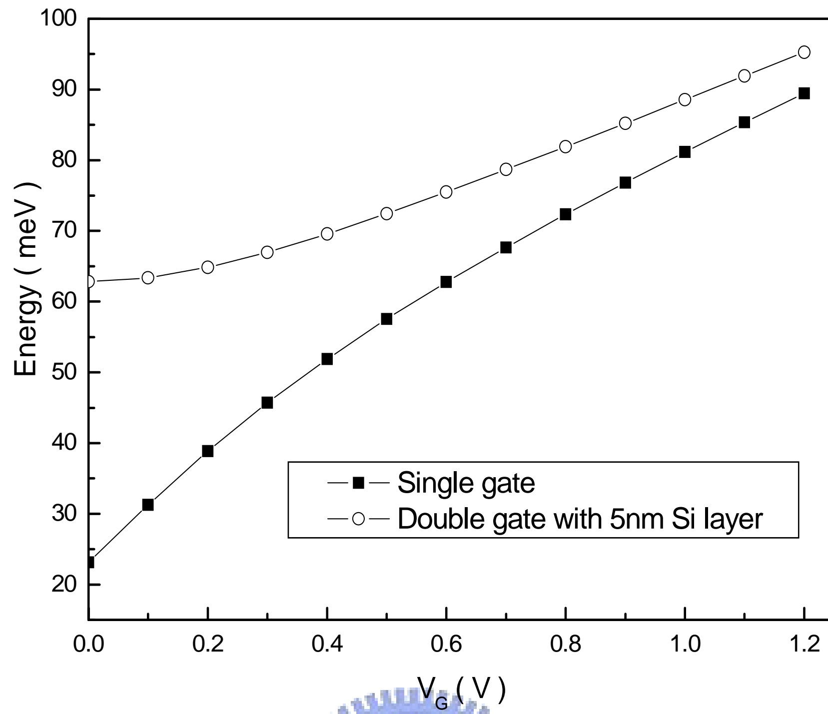


Fig.5.2 Energy difference between the lowest subband of the two valley group

Simulation condition(Single gate)

Metal gate with Φ=4.05eV; N_{SUB} =1*10^{16} cm^{-3}

t_{OX} = 1.65*10^{-9} m; and Temp=300K

Simulation condition(Double gate)

Metal gate Φ_1=Φ_1=4.05eV; N_{SUB} =1*10^{16} cm^{-3}

$t_{OX,1}$ = $t_{OX,2}$ = 1.65*10^{-9} m; Temp=300K; and T_{Si}=5nm

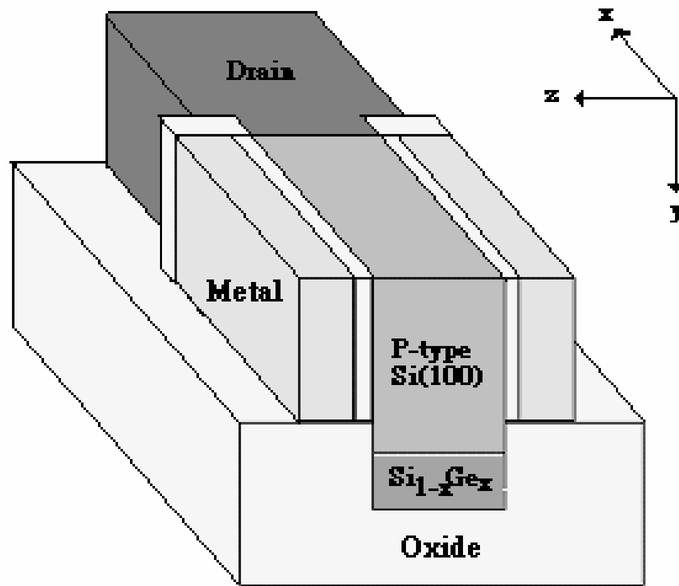


Fig 5.3. (a) Cross section view of strained Si DG device

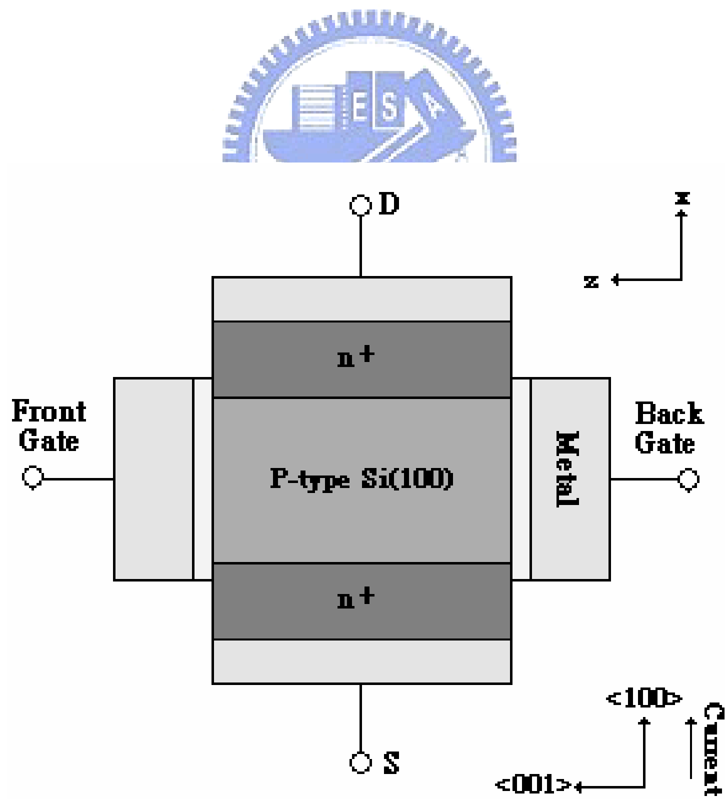


Fig 5.3. (b) Top view of strained Si DG device

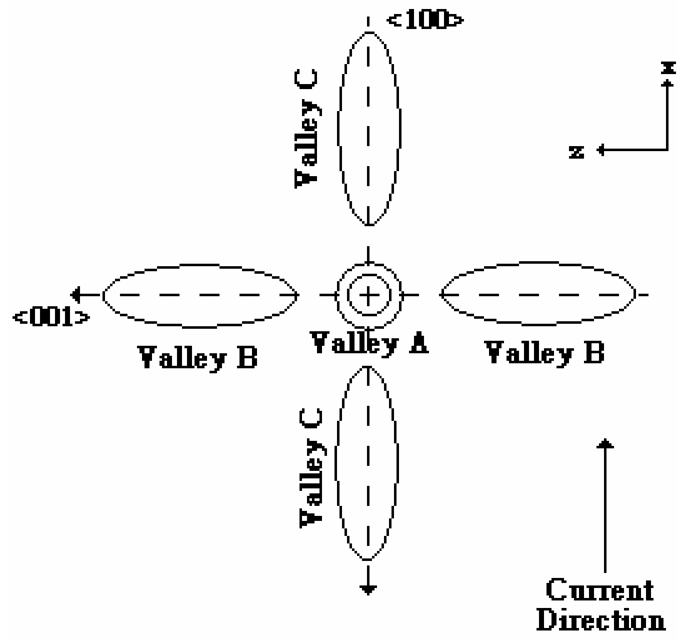


Fig 5.4 valleys of conduction band seen from the top of device

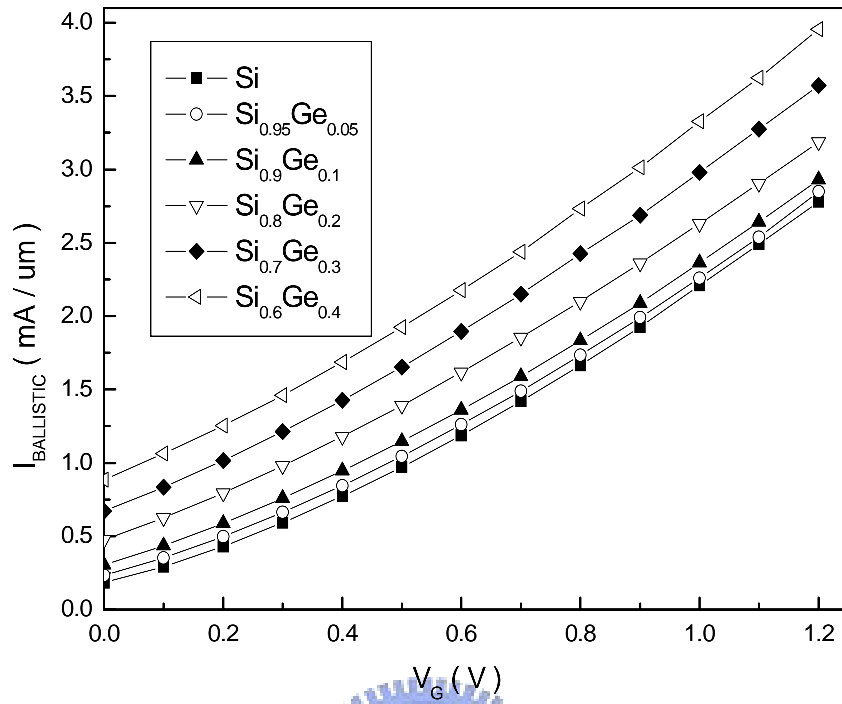


Fig.5.5 $I_{BALLISTIC}$ verse V_G for various Ge concentrations

Simulation condition:

Metal gate $\Phi_1=\Phi_1$=4.05eV; $N_{SUB}=1*10^{16}$ cm^{-3}

$t_{OX,1} = t_{OX,2} = 1.65*10^{-9}$ m; Temp=300K; and t_{Si}=50nm

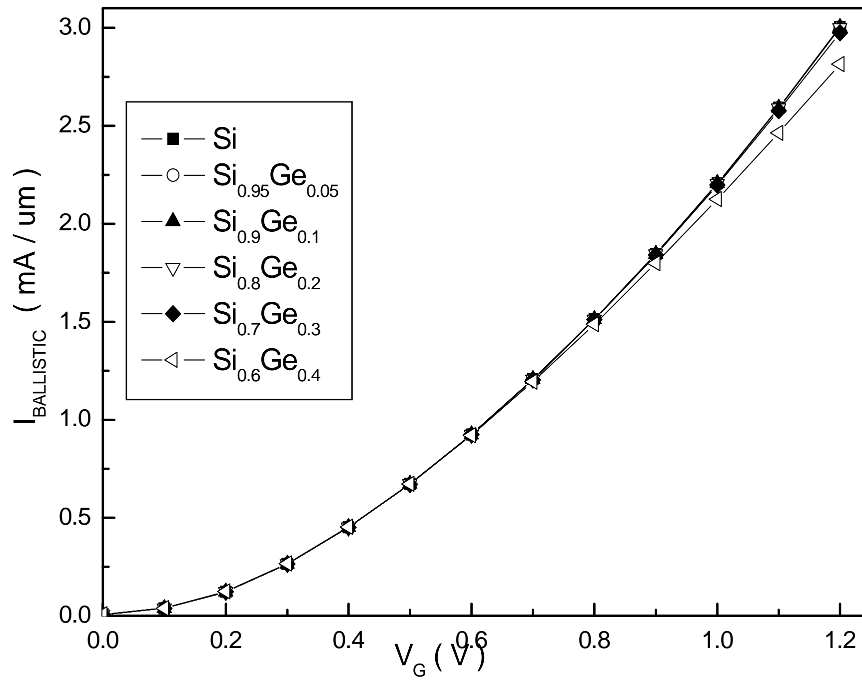


Fig.5.6 $I_{BALLISTIC}$ verse V_G for various Ge concentration

Simulation condition:

Metal gate $\Phi_1=\Phi_1=4.05eV$; $N_{SUB}=1*10^{16}\ cm^{-3}$

$t_{OX,1} = t_{OX,2} = 1.65*10^{-9}m$; Temp=300K; and t_{Si}=2nm

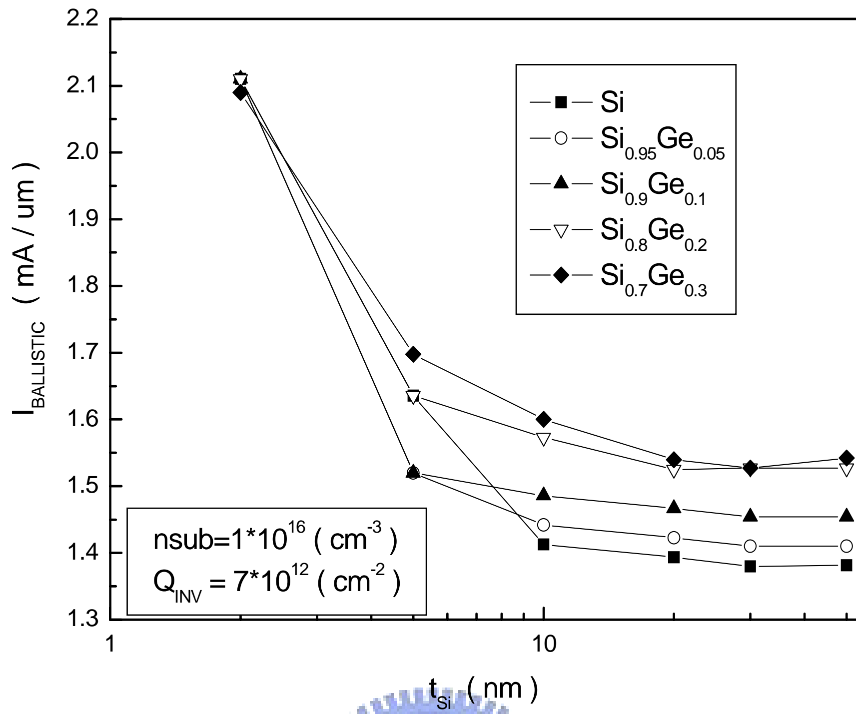


Fig.5.7 $I_{BALLISTIC}$ as $Q_{INV}=7*10^{12}$ cm^{-2} verse t_{Si} for various Ge concentration

Simulation condition:

Metal gate $\Phi_1=\Phi_1=4.05eV$; $N_{SUB}=1*10^{16}$ cm^{-3}

$t_{OX,1} = t_{OX,2} = 1.65*10^{-9}$ m; and Temp=300K

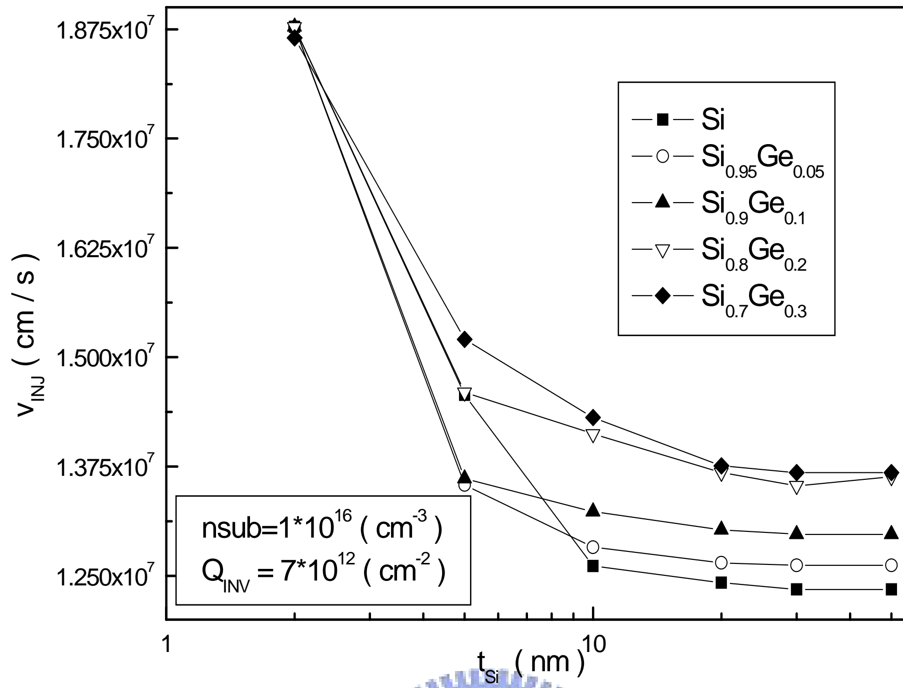


Fig.5.8 v_{INJ} as $Q_{INV} = 7*10^{12}$ cm^{-2} verse t_{Si} for various Ge concentration

Simulation condition:

Metal gate $\Phi_1 = \Phi_1 = 4.05$eV; $N_{SUB} = 1*10^{16}$ cm^{-3}

$t_{OX,1} = t_{OX,2} = 1.65*10^{-9}$ m; and Temp=300K

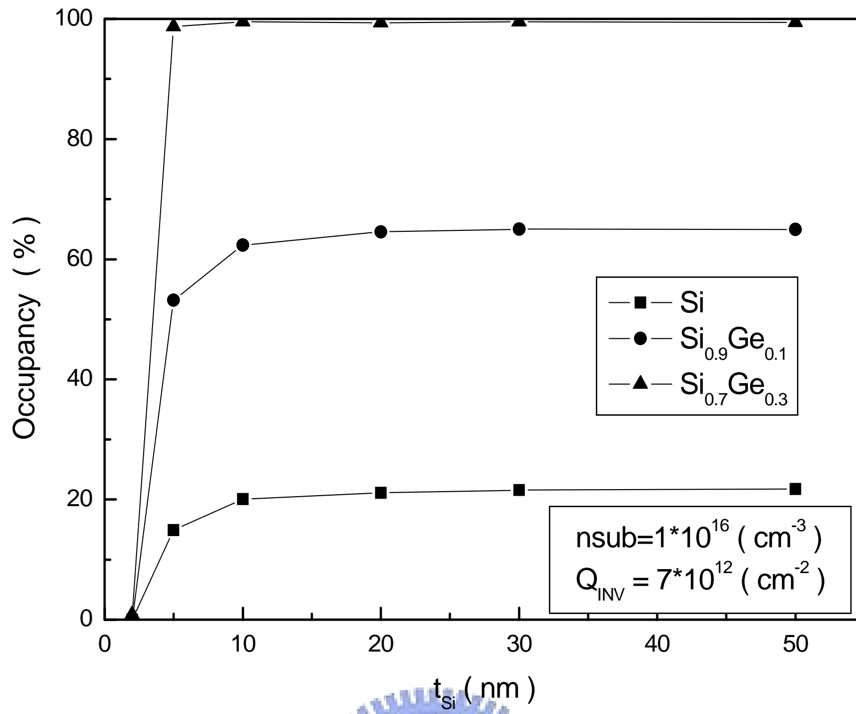


Fig.5.9 Electron occupancy of valley A as Q_{INV} =7*10^{12} cm^{-2} verse t_{Si} for various Ge concentration

Simulation condition:

Metal gate Φ_1=Φ_1=4.05eV; N_{SUB} =1*10^{16} cm^{-3}

$t_{OX,1}$ = $t_{OX,2}$ = 1.65*10^{-9} m; and Temp=300K

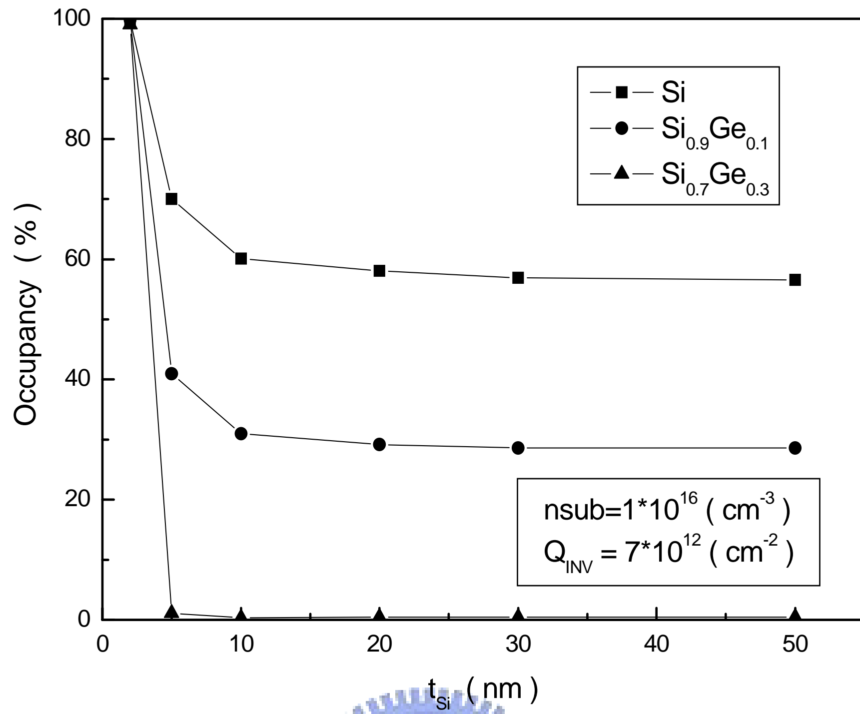


Fig.5.10 Electron occupancy of valley B as $Q_{INV}=7*10^{12}cm^{-2}$ verse t_{Si} for various Ge concentration

Simulation condition:

Metal gate $\Phi_1=\Phi_1=4.05eV$; $N_{SUB}=1*10^{16}\ cm^{-3}$

$t_{OX,1}=t_{OX,2}=1.65*10^{-9}\ m$; and Temp=300K

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論 文 題 目 ： 應變矽的金屬氧化物半導體場效電晶體之量子模擬

Quantum Simulation of Strained Si MOSFET