鈰金屬,鉿金屬閘極絕緣層 及複晶矽氮氧化層之研究

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摘　要

隨著系統晶片(SOC)的發展,持續降低非揮發記憶體中的複晶矽絕緣層及 CMOS 元件中的閘極絕緣層厚度以提高元件密度及降低操作電壓變得十分重要。為了滿足以上的需求並獲得一個較好的漏電流及可靠度,利用高介電常數材料(high-k)來取代二氧化矽及後續的處理變得不可或缺。

在論文中，用快速退火處理二氧化鉈絕緣層可以有效改善絕緣層特性。根據實驗的結果,快速退火可以有效消除絕緣層中的缺陷和Si基材中的介面層,進而改善二氧化鉈的品質和可靠度。除此我們也研究了二氧化鈰閘極漏電對溫度的相關性,及 F-N 和 F-P特性,進而從這些數據中我們提出Al/CeO_2/n-Si 的能階圖和電子傳遞的機制。我們發現沒有經過處理的試片是由F-P主導,而隨著高溫退火處理,會逐漸轉為F-N主導.因為絕緣層中的缺陷已被退火處理消除。

接著,第一次我們發現照光處理的二氧化鈦光觸媒可以有效改善經過氨氣電漿處理的二氧化鉿絕緣層,包括較低的閘極漏電,較大的崩潰電場,較佳的可靠度,及較長的十年工作電場。這是因為照光處理的二氧化鈦光觸媒可以使氧-氫及氮-氫等弱鍵斷裂,進而產生電子缺

陷來改善二氧化鉿絕緣層的特性。經由氨氣處理產生的相關弱氫鍵以前被研究過, 在絕緣層中會導致嚴重的固定氧化層電荷, 氧化層阻陷電荷, 及介面態階, 這些都會造成可靠度嚴重的下降。

最後, 我們利用低壓化學氣相沈積系統於複晶矽上沈積氮化矽層, 並利用二氧化氮快速退火和電漿處理來改善絕緣層特性。二氧化氮電漿處理可以使接近閘極的氮化矽再氧化形成氮氧化矽層。雖然經過電漿處理後, 電性厚度有些許增加, 但是處理過後的試片都有較高的崩潰電場, 較低的漏電流, 較長的十年工作電場, 及較高能階的阻障高度。尤其是加負電壓(閘極注入)時改善較明顯。不幸地, 電漿處理容易造成電漿傷害形成缺陷, 導致在定電流下有較高的電壓飄移。不過整體而言, 用二氧化氮快速退火及電漿處理的氮矽氧化層還是蠻應用在下一代的非揮發記憶體上。

The Study of Cerium-based Gate Dielectrics, Hafnium-based Gate Dielectrics, and Interpoly oxynitride

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ABSTRACT

For the system on a chip (SOC) application, a continuously scaling of interpoly dielectrics for electrically-erasable programmable read only memory (EEPROM) and gate dielectrics for complementary metal oxide semiconductor (CMOS) is needed to have high density and low operation voltage. To meet the above requirements and exhibit a low leakage current and a good reliability, the replacement of high dielectric constant (high-k) materials for silicon dioxide and additional treatment have become indispensable.

In this thesis, the improved characteristics of ultra–thin cerium dielectrics with rapid thermal annealing are investigated. Based on the experimental results, the rapid thermal annealing can effectively improve the reliability and quality of the cerium dioxide owing to the elimination of traps in the dielectrics and interfacial layer between CeO_2/Si.Besides, we also report the temperature dependence of gate leakage current, Frenkel-Poole (F-P) conduction and Fowler-Nordheim (F-N) tunneling characteristics, from which we deduce the energy band diagram for Al/CeO_2/n-Si

structure as well as its current transport mechanisms for the first time. Besides, the experimental results shows that F-P conduction dominants the as-deposited sample, and as the RTA temperature increases, the F-N tunneling become more important owing to the elimination of traps in the dielectrics.

Furthermore, for the first time, we present that irradiated TiO_2 Photocatalyst can obviously improve the HfO_2 with post NH_3 plasma treatment, including of lower gate leakage current, higher breakdown electric field, better reliability, and longer 10-year lifetime. It is because that irradiated TiO_2 Photocatalyst can induce a lot of electron traps owing to the O-H and N-H bonds breakage, which results in more obvious improvement of the HfO_2 film prepared with NH_3 plasma treatment. It is reported that the hydrogen-related traps (-H,-OH and –NH) provided by NH_3 in the dielectrics can cause fairly high fixed charge (Q_f), trapped charge (Q_{ot}),and interface state density (D_{it}) , which can result in serious reliability issue.

Finally, the interpoy-dielectrics deposited by LPCVD nitride and then prepared with N_2O RTA and followed by N_2O plasma treatment were studied. N_2O plasma treatment can cause the reoxidation of the nitride film to form a SiO_xN_y, which exist at the top of nitride (near the poly Ⅱ).Although the effective oxide thickness of the oxynitride film slightly increases after N_2O plasma treatment, it is found that the samples after the process of N_2O plasma treatment exhibit obviously higher breakdown field, lower leakage current, longer time-to-breakdown, and larger effective barrier height than the control samples. Moreover, the improvement is more apparent under negative bias(gate injection). Unfortunately, N_2O plasma treatment can bring about plasma damage, which leads to higher gate voltage shift due to higher electron traps and defects. In sum, the oxynitride treated by N_2O RTA and N_2O plasma treatment is still suitable for use in the next generation on EEPROM.