Chapter 1

Introduction

1.1 General background

MOS technology will face many of its tough challenges in the sub-90-nm device generation. Among them is the replacement of conventional SiO_2 or oxynitride gate dielectrics, which are facing their physical scaling limits. An SiO_2 or oxynitride dielectric only a few monolayers thick (15 Å) runs into problems with excessive gate leakage current caused by direct tunneling. In addition, reliability issues become a huge concern for such a thin SiO_2 dielectric. High dielectric constant or high-dielectrics offer the advantage of a thin equivalent oxide thickness (EOT), while maintaining a thicker physical dielectric thickness. Unfortunately, many high-k materials such as Ta_2O_5, TiO_2, $SrTiO_3$, and BST are thermally unstable when directly contacted with silicon [1] and need an additional barrier layer which may add process complexity and impose thickness scaling limit. Moreover, materials with too low or too high dielectric constant may not be adequate choice for alternative gate dielectric application. Ultra high-k materials such as STO or BST may cause fringing field induced barrier lowering effect [2]. Materials having relatively low dielectric constant such as Al_2O_3 and Y_2O_3 do not provide sufficient advantages over SiO_2 or Si_3N_4 [3].

Furthermore, developing nonvolatile memories such as EPROM, EEPROM, and Flash EEPROM has received increasing interest [4]–[6]. For double-poly floating gate structure (EPROM or EEPROM), the polyoxides require a low leakage current and high breakdown electric field to obtain adequate data retention characteristics

[4]–[6]. However, a nonuniform polyoxide film thickness and rough surface morphology of the polysilicon/polyoxide interface cause polyoxides to have a higher leakage current and lower dielectric breakdown field than those of silicon dioxide grown from a single crystalline silicon substrate [7]-[9]. This occurrence is attributed to local electric-field enhancement in rough polysilicon/polyoxide interface. Moreover, the surface roughness of polyoxide/polysilicon interface would be enhanced after thermal oxidation [9]–[11]. Therefore, how to reduce the roughness of polysilicon/polyoxide interface is a critical issue. To overcome this difficulty, the CVD oxide deposited on the polysilicon films (deposited polyoxide) is a highly attractive inter-polysilicon dielectric [11], [12]. Recently, chemical mechanical polishing (CMP) process has been used for planarization of multilevel interconnect [13], [14], polysilicon-filled trench isolation [15], and oxide-filled trench isolation [16]. CMP process, owing to its planarization properties, has also been used to improve the surface roughness of polysilicon film [17]. However, the insulating properties of polyoxide films thermally grown or deposited on polished polysilicon films have been paid scarce attention [18].

1.2 Motivation

Gate dilelectric materials having high dielectric constant, large band gap with a favorable band alignment, low interface state density and good thermal stability are needed for future gate dielectric application. Some of the more promising high-k candidates are ZrO_2 [19], [20], HfO_2 [21], [22], Zr–silicate [19], [23], and Hf–silicate [23], [24] since they have demonstrated EOT scalability(12 Å) with low leakage current. However, single oxide high-k dielectrics such as HfO_2 and ZrO_2 have been reported to be vulnerable to the diffusion of oxygen which causes formation of a

low-k interfacial layer at the Si interface [25]. EOT of HfO_2 with an initial EOT of increase more than during the post-metal-deposition anneal (PMA) at 950℃ [26]. The EOT increase would limit the use of high-k dielectrics for the self-aligned gate process requiring high temperature thermal process after the transistor fabrication. Several studies have focused on the improvement of the thermal stability of high-k gate dielectric to overcome the dielectrics' insufficient immunity to oxygen or impurity diffusion during the subsequent thermal process. Those studies include an NH_3 nitridation of Si surface [26], an incorporation of nitrogen into HfO_2 (i.e., hafnium oxynitride: HfON) [23],capping a HfO_2 layer with a nitrogen-incorporated layer (top nitridation) [27], hafnium silicate (HfSiO) and nitrogen incorporated hafnium silicate (HfSiON) [28].Moreover, the crystallization temperature of HfO_2 is quite low, which restricts the thermal budget after its deposition to avoid the higher leakage current and lateral nonuniformity associated with grain boundaries. Hf-silicate has been reported as a promising material with high crystallization temperature. However, the dielectric constants of silicates are usually less than 15 and therefore they may face the same scaling challenge as Al_2O_3.

On the other hand, the scaling down of interpoly dielectrics is critical for next generation nonvolatile memories with a small cell size and low programming voltage. For EEPROM and flash memory devices, the inter-polysilicon oxide demands a high breakdown field and low leakage current to obtain good data retention characteristics. Recently, N_2O grown polyoxide film show excellent electrical properties due to its incorporation of nitrogen at the polyoxide/poly-I interface [29]. However, the nonuniform polyoxide film and rough surface morphology of polysilicon/polyoxide interface in inter-polysilicon oxide cause a lower dielectric breakdown field and higher leakage current. It is previously reported using a CVD TEOS oxide deposited on the phosphorus *in-situ* doped polysilicon and N_2O RTA improves the electrical

quality of polyoxide due to smoother interface morphology and incorporation of nitrogen into the polyoxide [30]. In addition, the CMP process achieves a planar surface polysilicon film for polyoxide with a higher electron barrier height and lower electron trapping rate [31]. Therefore, how to reduce the roughness of polysilicon/polyoxide interface and the density of interface defects in the polyoxide become very important topic. However, the Si_3N_4/polysilicon interface is not yet as good as the SiO_2/polysilicon interface and the density of interface defects is also relatively high. An additional N_2O treatment can reduce this interface state and bulk trap densities [32], [33].

Therefore, as mentioned above, the main purpose of this research is to develop high quality high-k gate dielectrics and interpoly oxynitride dielectrics for SOC applications. We used post-deposition NH_3 or N_2O plasma treatment to improve the high-k gate dielectrics and interpoly oxynitride dielectrics. Moreover, for the first time, We also report irradiated TiO_2 Photocatalyst brings about some chemical reactions with the HfO_2 film treated by NH_3 plasma, which can apparently improve hafnium gate dielectrics.

1.3 Organization of the Thesis

In this thesis, we study the characteristics of CeO_2, HfO_2, and interpoly oxynitride.

In Chapter 2, the basic characteristics of CeO_2 gate dielectrics are presented, including the electrical characteristics such as J-E curves, EOT, C-V curves, dielectric breakdown, gate leakage current density and Frenkel-Poole (F-P) conduction and Fowler-Nordheim (F-N) tunneling characteristics.

In Chapter 3, for the first time, we proposed that irradiated TiO_2 Photocatalyst can obviously improve the HfO_2 with post NH_3 plasma treatment, including of lower

gate leakage current, higher breakdown electric field, better reliability, and longer 10-year lifetime.

In Chapter 4, the characteristics of interpoly oxynitride are investigated including the electrical characteristics such as J-E curves, dielectric strength, effective barrier height, gate voltage shift and time dependent dielectric breakdown.

At the end of this thesis, conclusions are given in Chapter 5.

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Chapter 2

Characteristics Improvement and Carrier Transportation of Cerium-based Gate Dielectrics with Rapid Thermal Annealing

2.1 Introduction

Recently, many high dielectric constant (high-k) materials like Al_2O_3, ZrO_2, and HfO_2 [1]-[3] have been widely studied to replace the silicon dioxide owing to the inevitability of its high leakage as the thickness scales down. Gate dielectric materials with a high dielectric constant, a low interface state density and a good thermal stability appear to be promising for next generation gate dielectric applications. Moreover, materials with too lower or too higher dielectric constant may not be adequate choice for alternative gate dielectric application. Ultra high-k materials such as STO or BST may cause fringing field induced barrier lowing effect [4]. And materials having relatively low dielectric constant such as Al_2O_3 and Y_2O_3 do not provide sufficient advantages over SiO_2 or Si_3N_4[5]. Cerium dioxide (CeO_2), which has been extensively researched for its use as a buffer layer for $YBa_2Cu_3O_{(7-x)}$ (YBCO) on sapphire [6], a buried insulator for silicon-on-insulator (SOI) [7] and $PbZrTiCeO_3$ (PZT) ceramics [8], has lately been used as gate dielectric material [9]. Many superior properties of cerium dioxide, such as a lattice nearly matched to that of silicon (a=0.5411nm) and a sufficiently high dielectric constant (~26) ensure its high thermal stability on silicon and high scaling capacity. Nevertheless, characteristics of cerium

dioxide are not yet fully understood. In this study, the improved characteristics of ultra–thin cerium dielectrics with rapid thermal annealing are investigated. We also report the temperature dependence of gate leakage current, Frenkel-Poole (F-P) conduction and Fowler-Nordheim (F-N) tunneling characteristics, from which we deduce the energy band diagram for Al/CeO_2/n-Si structure as well as its current transport mechanisms for the first time.

2.2 Experimental

Al/CeO_2/n-Si capacitors of an area of 6.36×10^{-5} cm^2 were fabricated on 4 inch n-type (100)-oriented Si wafers. Figure 1 shows the key process flows of cerium dielectrics with post-deposition anneal (PDA). All samples were first cleaned by a standard Radio Corporation of America (RCA) clean. The CeO_2 film was then deposited by a electron beam evaporation. After the gate dielectric had been formed, the samples were treated by rapid thermal anneal (RTA) at 600 ~ 950^oC for 60s in N_2 ambient. Then, a 5000 Å Al film was deposited on the CeO_2 film by a thermal coater. After that, the gate of the capacitor was defined lithographically and etched. Finally, a 5000 Å Al film was also deposited on the backside of the wafer to form the ohmic contact. Besides, there may be an interfacial layer between CeO_2 and silicon substrate. Therefore, the barrier parameters to be discussed in this paper are "effective" values that include the effects of these interfacial layers. The effective oxide thickness (EOT) was estimated by the high frequency (0.1 MHz) capacitance versus voltage (C-V) curves in the strong accumulation region without considering the quantum mechanical effects. The electrical properties were measured by using an HP 4156B semiconductor parameter analyzer and an HP4284A precision LCR meter.

2.3 Results and Discussion

In this section, some electrical and physical characteristics of metal CeO_2 semiconductor capacitors with various rapid thermal annealing were discussed.

2.3.1 Improved Characteristics of CeO_2 Gate Dielectrics

2.3.1.1 C-V Characteristics

The EOTs were extracted from the equation shown as following:

$$C = \varepsilon A/d. \qquad (2\text{-}1)$$

Where C is he capacitance value in the accumulation region (-2 V)

ε is the dielectric constant of Si (~3.9)

A is the area of the capacitor

d is the effective oxide thickness

Figure 2-2 shows the high frequency (0.1MHz) capacitance versus gate voltage (C-V) characteristics of cerium dielectrics with rapid thermal annealing at different annealing temperature. We can see that as the annealing temperature increases, the EOT decreases simultaneously from 20.9A to 13.7A. High temperature annealing can densify the CeO_2 film and make the dielectrics more stoichiometric. Besides, there are some distortions for the as-deposited sample and the sample with RTA at 600^{o}C. We believe that it is owing to the serious interface state (fast traps) at the CeO_2/Si substrate interface [10]. Ultra high temperature annealing may help to improve this distortion.

2.3.1.2 J-V Characteristics

The current density (J) in the J-V curve was obtained by using J=I/A, where A is the area of capacitor. The t_{ox} is the effective oxide thickness (EOT) determined by the

C-V measurement. Figure 2-3 shows the J-V characteristics of these samples. The breakdown electric field becomes larger and the leakage current density decreases as the annealing temperature increases. It should be noted that CeO_2 still has excellent electrical performance, even through the high temperature annealing up to 950^{o}C. It is seemed that the CeO_2 film does not crystallized after high temperature RTA treatment.

2.3.1.3 Characteristics of Gate-leakage Current Density

Figure 2-4 show the Weibull plots of the leakage current density at V_g=1V for the cerium dioxide treated by RTA at different temperature. We can observe the RTA treatment improves not only the leakage current density but also the distribution uniformity (Weibull slope).

2.3.1.4 Characteristics of voltage Breakdown

Figure 2-4 shows the Weibull plots of the dielectric breakdown voltage for the samples treated by RTA. As the RTA temperature increases, the breakdown voltage is raised form 1.4V to 2.3V.

2.3.1.5 Time Dependent Dielectric Breakdown

The Weibull plots of time to breakdown for the samples treated by RTA is presented in Figure 2-5.The samples are stressed at V_g=1V. Obviously, the time-dependent dielectric breakdown (TDDB) is improved after high temperature RTA treatment. Furthermore, the RTA treatment can effectively improve the reliability of the cerium dielectric film owing to the elimination of traps in the dielectrics and interfacial layer between CeO_2/Si.

2.3.1.6 HRTEM (High Resolution Transmission Electron Microscope)

Figure 2-6~2-9 show the high resolution transmission electron microscopy (HRTEM) images of the cerium dioxide without treatment and with rapid thermal annealing at 600~950^{o}C, respectively. For the TEM image of the as-deposited sample in Fig. 2-6, the physical thickness of the CeO_2 film is about 54 Å and obviously there is an interfacial layer about 18 Å existing between CeO_2 and the Si substrate. From Fig.2-7 to Fig.2-9, we can find that as the annealing temperature increases, the thickness of the CeO_2 film becomes thinner and densified. Besides, it is apparent that the interfacial layer thickness gradually decrease and finally almost disappear. Therefore, we can rationally suppose that the high temperature annealing can reduce the interfacial layer and improve the cerium dielectrics. The HRTEM results can explain the C-V characteristics of cerium dielectrics, as shown in Fig.2-2.

2.3.1.7 Auger electron spectrometer (AES) analysis

Figure 2-10~11 shows the Auger electron spectrometer (AES) analysis of the as-deposited and RTA 950℃ samples respectively. Form Fig.2-10, we can find the apparently interfacial layer between CeO_2 and Si substrate (marked in this figure). After the RTA 950℃ treatment in Fig.2-11, the composition of CeO_2 film is still stable and the interfacial layer becomes smaller.

2.3.1.8 Electron Spectroscopy for the Chemical Analysis(ESCA) Spectra

Figure. 2-13~14 shows the Ce3*f* electron spectroscopy for the chemical analysis (ESCA) spectra of the as-deposited and RTA 950℃ samples. A take-off angle (TOA) of 90°was used to measure the ESCA spectra. The peaks of Ce-O bonding are

respectively at 884 eV ($Ce3d_{3/2}$) and 902 eV ($Ce3d_{5/2}$). We can find the peaks and profiles of the as-deposited and RTA 950℃ samples are almost the same. It means that any other bonding, especially Ce-Si bonding, dose not formed in the cerium dielectrics after high temperature RTA treatment. Therefore, the cerium dielectric has excellent thermal stability on Si substrate.

2.3.2 Current Transportation of CeO_2 Gate Dielectrics

2.3.2.1 Temperature dependence of leakage current

The temperature dependence of leakage current was studied to understand the current transport mechanisms, which was measured from 30 to 110^{o}C. For the sample with RTA at 600^{o}C, the leakage current is obviously temperature dependent, as shown in fig. 2-14. However, the leakage current is temperature independent for the sample with RTA at 950^{o}C, as shown in fig. 2-15. Therefore, we can rationally suppose that Frenkel-Poole (F-P) conduction dominants the sample with RTA at lower temperature (600^{o}C), and Fowler-Nordheim (F-N) tunneling dominants the sample with RTA at higher temperature (950^{o}C).

2.3.2.2 Frenkel-Poole (F-P) conduction fitting

Figure 2-16 shows the F-P conduction fitting at V_g=1V for the samples with RTA at different temperature. We can find that less temperature dependence is obtained for the samples with higher annealing temperature. That is, the trapped charges are annealed at high RTA temperature. The experimental results show that F-P conduction dominants the samples with RTA at lower annealing temperature, and as the RTA temperature increases, the F-N tunneling becomes more and more important owing to the elimination of traps in the dielectrics.

2.3.2.3 Fowler-Nordheim (F-N) fitting in the high field region

Figure 2-17 shows the F-N fitting in the high field region of the sample with RTA at 950^{o}C and the measured CeO_2/Si barrier height is about 0.75eV, which we assume that $m^{*}=0.2m_0$ for Si to calculate the effective barrier height. It should be noted that this barrier height includes the effect of the interfacial layer between CeO_2 and Si.

2.3.2.4 Carrier transportation

Figure 2-18 shows carrier transportation of the sample with RTA at 600^{o}C and the charge trap energy level is about 0.605eV from the conduction band of CeO_2, which is extracted from the slope of F-P fitting shown in fig.2-16. It may be worth noting that, for the sample with RTA at 600^{o}C, Frenkel-Poole (F-P) conduction dominates because the trap energy level is much smaller than the Si/CeO_2 barrier height (0.75eV) shown in fig. 2-17.

2.3.2.5 The Band Diagram of Al/CeO_2/Si

Figure 2-19 shows the band diagram of Al/CeO_2/Si capacitor at flat-band. All parameters needed are calculated and indicated in this figure. Besides, we find the Si/CeO_2 barrier height is very low in comparison with Si/HfO_2 or other high k material. Therefore, if the higher temperature(>110^{o}C) dependence of leakage current was measured, the Schottky emission mechanism may dominate over the Frenkel-Poole (F-P) conduction and Fowler-Nordheim (F-N) conduction[11].

2.4 Summary

In conclusion, we propose an ultra-thin cerium dioxide with post-deposition rapid thermal annealing, which exhibits the thin EOT (~1.4nm for the RTA950^{o}C

sample) and superior properties. Based on the experimental results, the rapid thermal annealing can effectively improve the reliability and quality of the cerium dioxide owing to the elimination of traps in the dielectrics and interfacial layer between CeO_2/Si. Besides, the cerium dioxide has excellent thermal stability on Si substrate and high temperature to crystallize. Therefore, it can be the candidate for the future ultra-large scale integrated circuit (ULSI) applications.

Furthermore, based on the experimental results of the temperature dependence of gate leakage current, Frenkel-Poole (F-P) conduction and Fowler-Nordheim (F-N) tunneling characteristics, we have extracted the energy band diagrams and current transport mechanisms for Al/CeO_2/n-Si structure. The band diagram of cerium dioxide with Al gate was also established for the first time. In particular, we have obtained the CeO_2/Si barrier height of 0.75eV ($m^*=0.2m_0$ for Si) that will be useful for modeling and simulation in the cerium dielectrics. Besides, the experimental results shows that F-P conduction dominants the as-deposited sample, and as the RTA temperature increases, the F-N tunneling become more important owing to the elimination of traps in the dielectrics.

Capacitor process

1. RCA clean, HF dip to remove native oxide

2. Deposition of CeO_2 with E-gun

3. RTA (N_2 ambient)

400°C , 600 °C, 800 °C, 950 °C

4. TaN/Al gate (To avoid the drawbacks of poly gate) & Mask #1

5. Contact Al (backside)

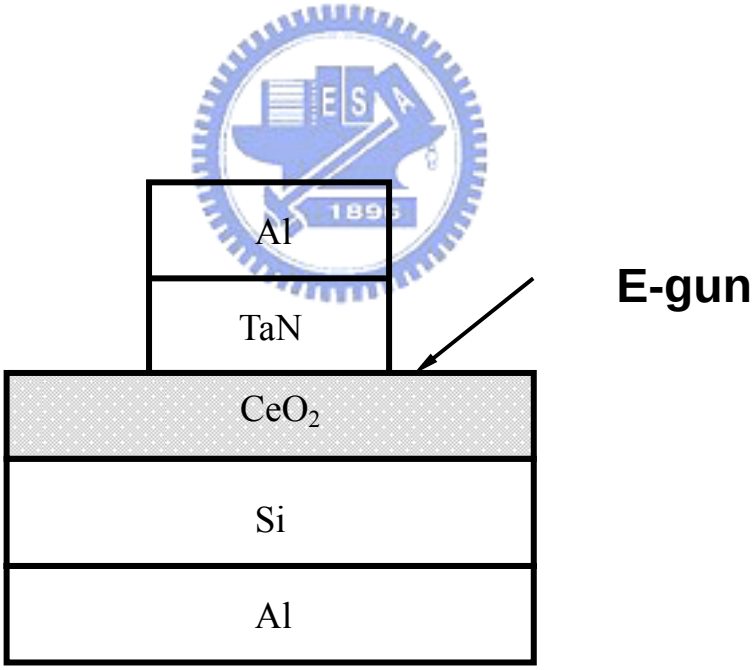

Fig.2-1 Key process flows of the fabrication for cerium dielectrics with post-deposition anneal (PDA).

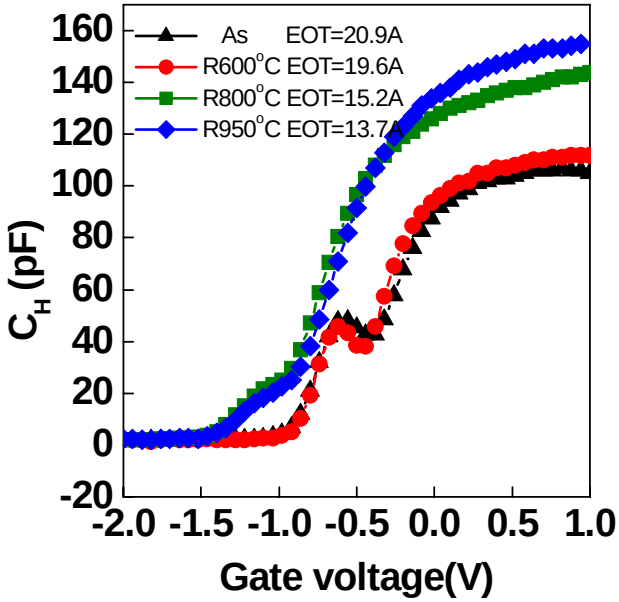

Fig.2-2 The high frequency (100kHz) C-V characteristics of cerium dielectrics with RTA at different temperature.

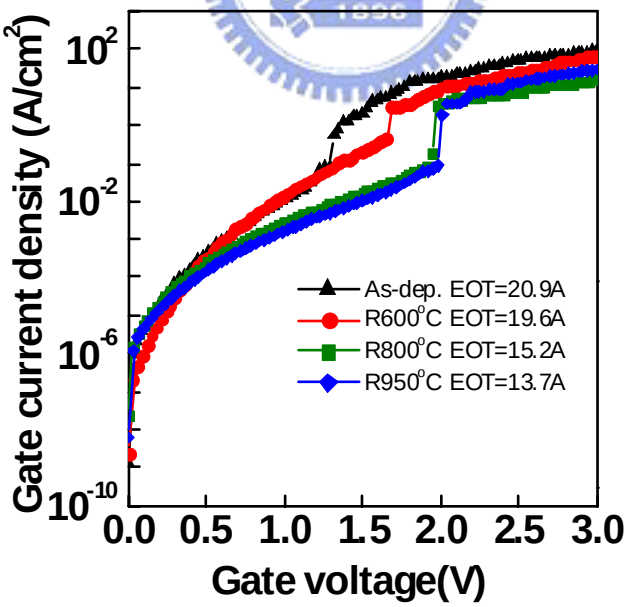

Fig.2-3 The J-V characteristics of cerium dielectrics with RTA at different temperature.

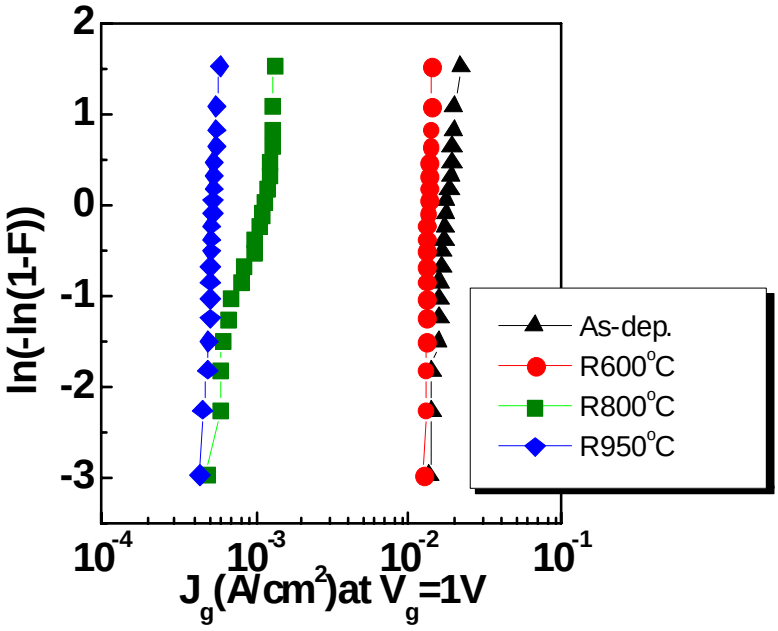

Fig.2-4 Weibull plots of the leakage current density at V_g=1V for the samples treated by RTA.

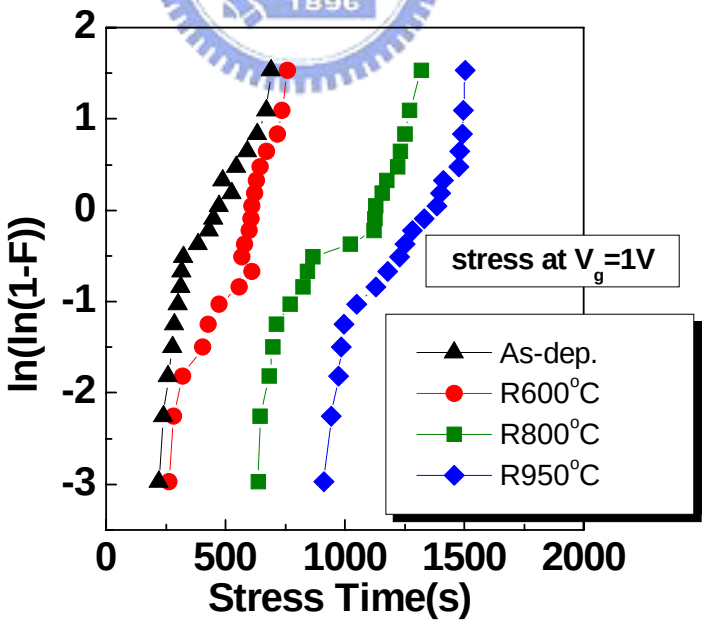

Fig.2-5 Weibull plots of time to breakdown for the samples treated by RTA.

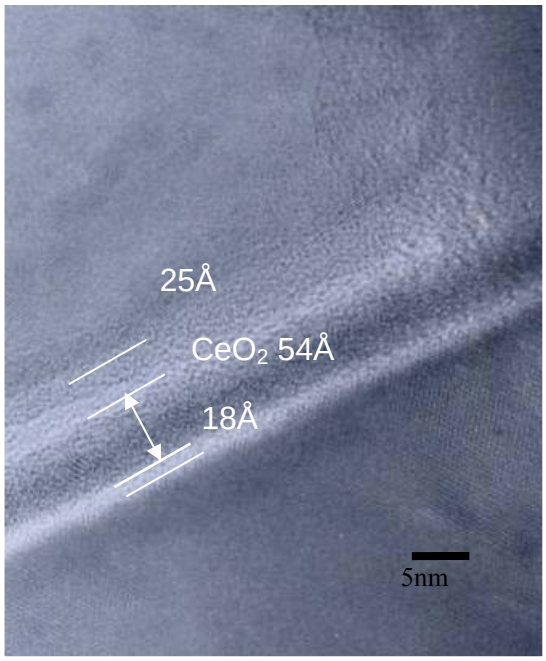

Fig.2-6 The TEM image of the cerium dioxide without RTA treatment

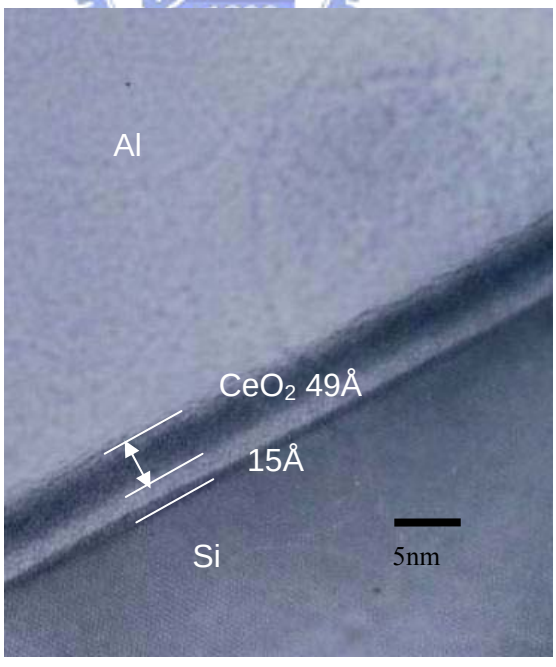

Fig.2-7 The TEM image of the cerium dioxide with RTA 600°C

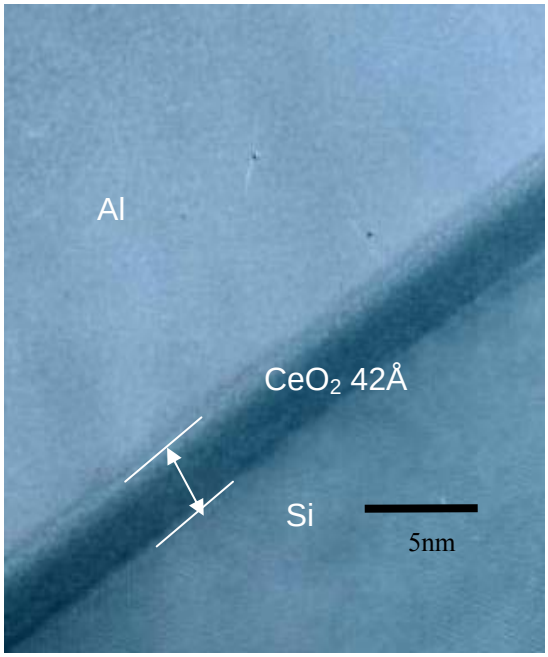

Fig.2-8 The TEM image of the cerium dioxide with RTA 800°C

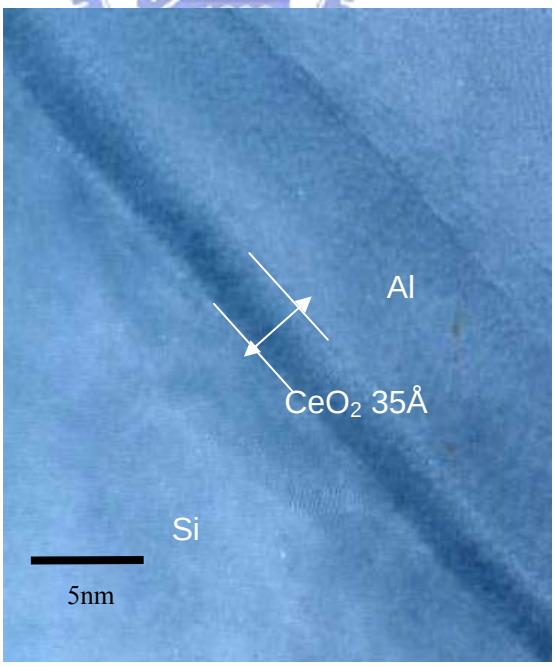

Fig.2-9 The TEM image of the cerium dioxide with RTA 950°C

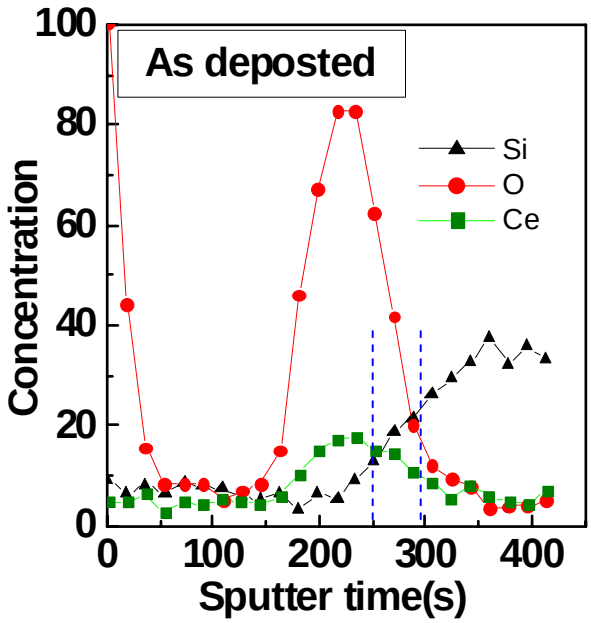

Fig.2-10 AES analysis of the as-deposited sample

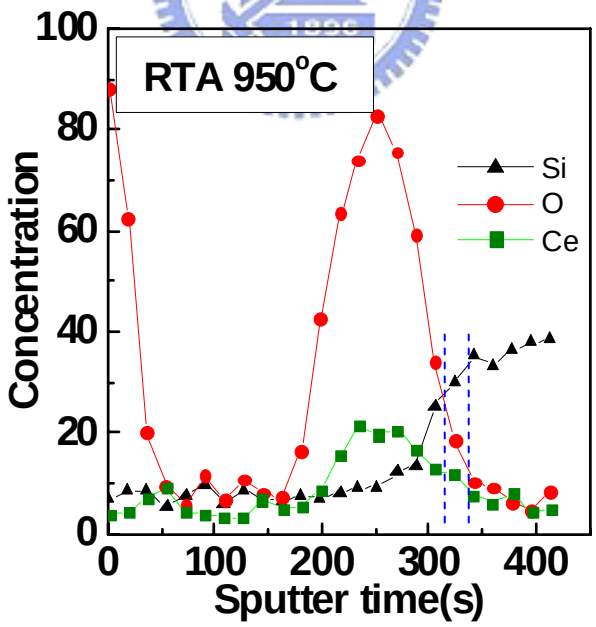

Fig.2-11 AES analysis of the sample treated by RTA 950℃

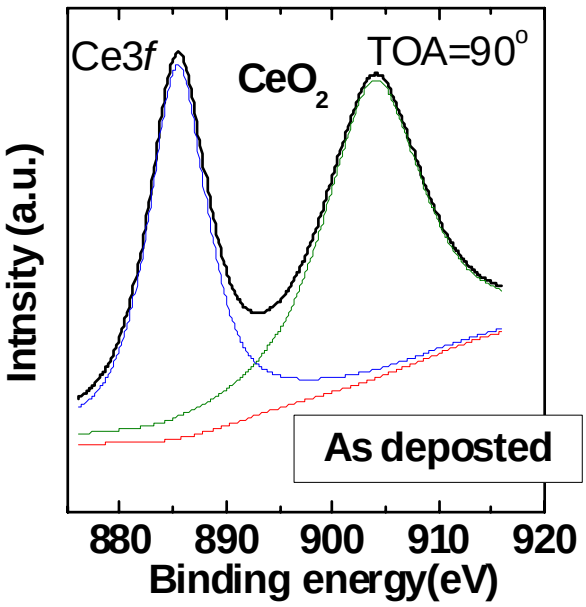

Fig.2-12 Ce3*f* ESCA spectra of the as-deposited sample.

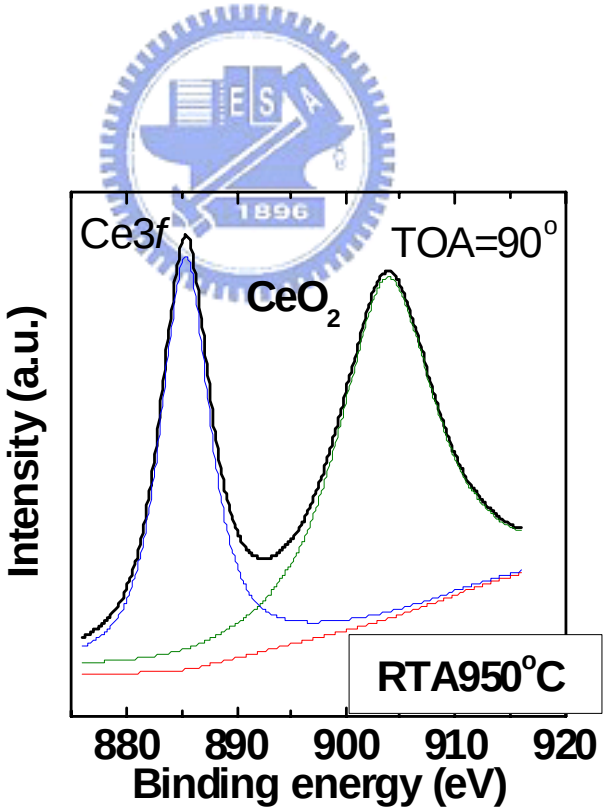

Fig.2-13 Ce3*f* ESCA spectra of the sample treated by RTA 950℃

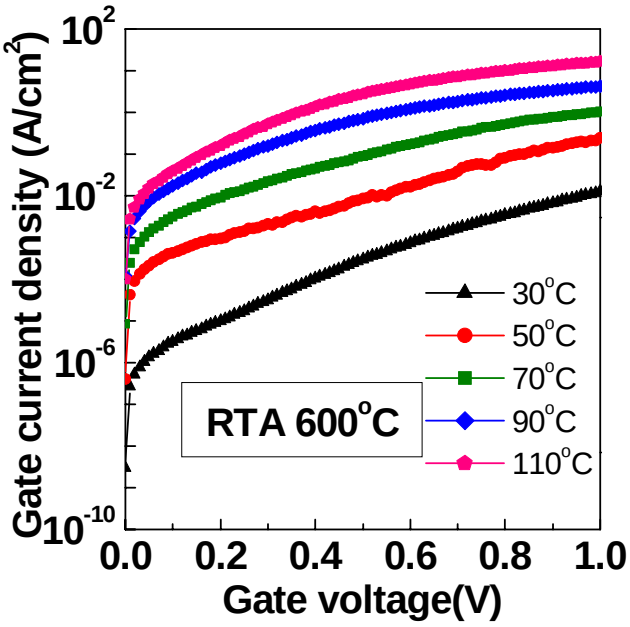

Fig.2-14 Temperature dependence of leakage current under substrate injection for the sample with RTA at 600℃.

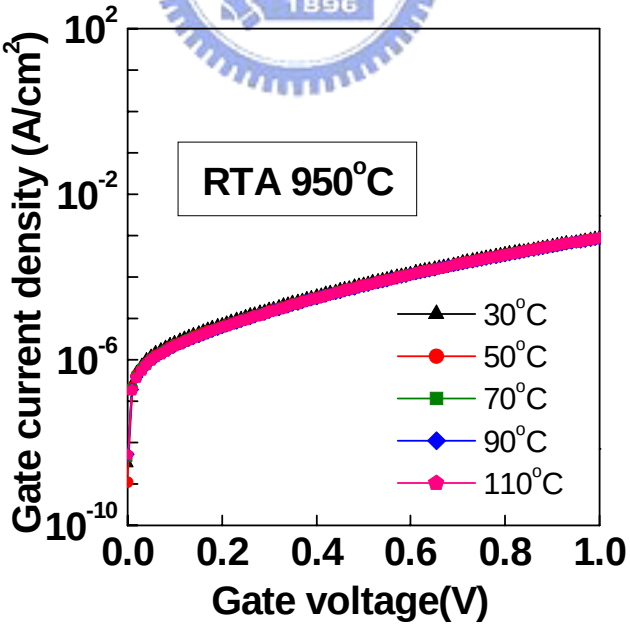

Fig.2-15 Temperature dependence of leakage current under substrate injection for the sample with RTA at 950℃.

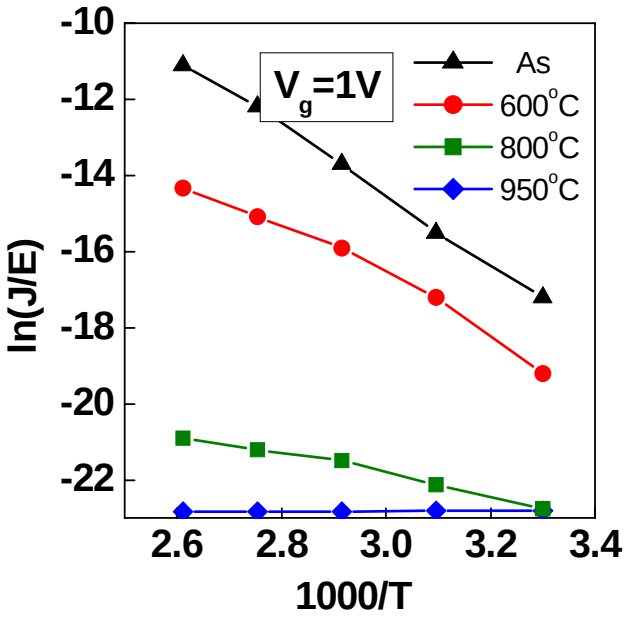

Fig.2-16 Frenkel-Poole (F-P) conduction fitting at V_g=1V for the cerium dielectrics with RTA.

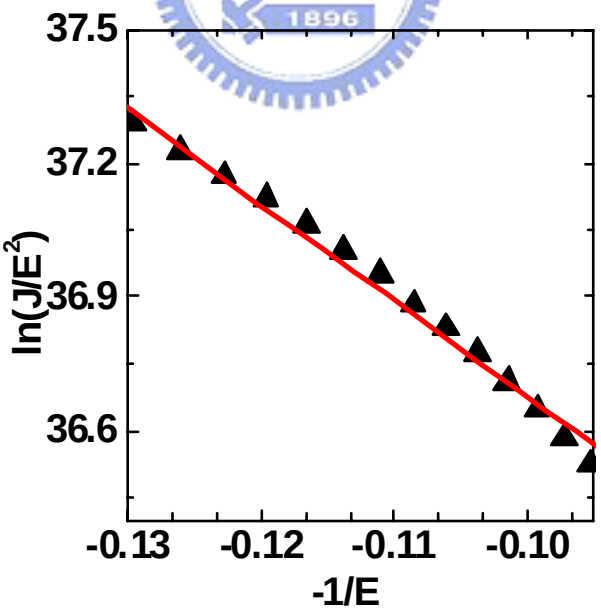

Fig.2-17 F-N fitting in the high field region of the sample with RTA at 950℃ and the CeO_2/Si barrier height is 0.75eV (m^*=0.2m_0 for Si).

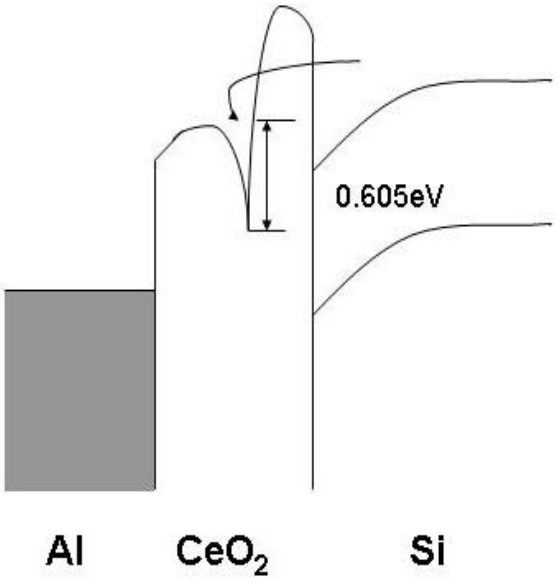

Fig.2-18 Carrier transportation of the sample with RTA at 600℃ and the trap energy level is about 0.605eV from the conduction band of CeO_2.

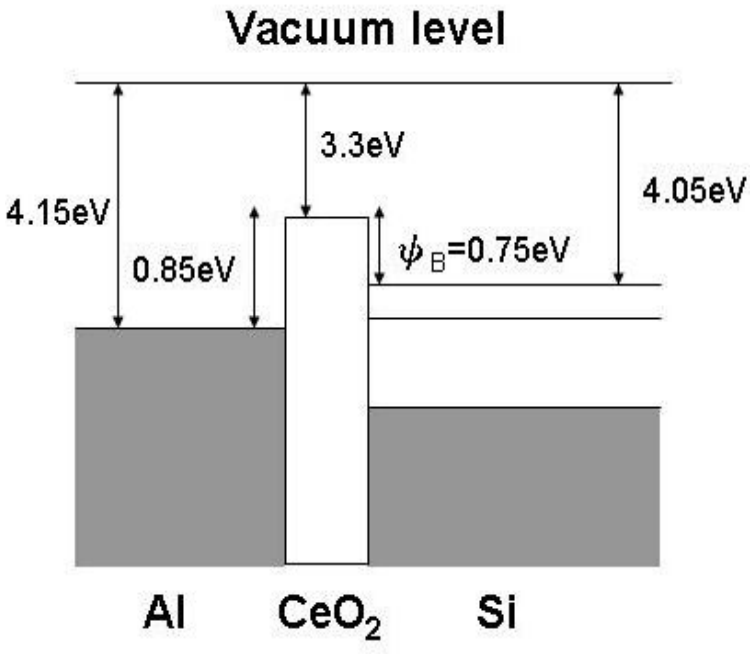

Fig.2-19 Band diagram of cerium dielectrics with Al gate.

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Chapter 3

Improved Hafnium-based Gate Dielectrics with NH_3 Plasma Treatment and Irradiated TiO_2 Photocatalyst

3.1 Introduction

3.1.1 Overview of the high-k dielectrics

According to the International Technology Roadmap for Semiconductor (ITRS), the gate dielectric needs to be scaled down below 1.2nm for 100-nm node CMOS technology and beyond [1] and the viability of SiO_2 will face severe challenges [2].Therefore, high-k dielectrics are being pursued as possible replacements for SiO_2. Among these dielectrics, HfO_2 appears promising due to its relatively high dielectric constant (~25) as compared to Si_3N_4 and Al_2O_3 [3], its relatively high free energy of reaction with Si (47.6 kcal/mole at 727℃) as compared to TiO_2 and Ta_2O_5 [4] and its relatively high band gap(~5.8eV) among its high-K contenders [5]. However, there are still many issues due to its low immunity to oxygen and boron diffusion. Oxygen easily diffuses through HfO_2 at high temperature, while results in low-k interfacial layer growth [6]. Boron diffusion from poly-Si gate into the Si substrate can cause threshold voltage shift and dielectric degradation [7].

Recently Si nitridation method by NH_3 annealing (BN: Bottom Nitridation) was suggested to overcome these problems of HfO_2 [8,9]. However, this technique results in higher interface charges [10], which leads to higher hysteresis and reduced channel mobility. Though surface nitridation forms a very thin Si_3N_4 layer at the HfO_2/Si interface, boron can still penetrate into the HfO_2 region and potentially

degrade MOSFET performance. An additional demerit of BN is the presence of hydrogen known to increase the electron trapping rates [11].

Therefore, one possible solution is to place the nitride barrier near the HfO_2 and gate electrode interface [12]. On the other hand, top nitridation (TN) on the HfO_2 is demonstrated by the deposition of Hf_xN_y on an HfO_2 layer to improve diffusion immunity without degrading interface quality. For the TN process, two techniques to make HfO_2 with TN involved: one is the post-deposition annealing by nitrogen-related gas after forming HfO_2 layer, and the other is a post-Hf_xN_y deposition annealing by sputtering. Despite the complicated process, the TN process provides an improved nitrogen profile and improved mobility due to favorable interface characteristics.

3.1.2 Overview of the TiO_2 Photocatalyst

TiO_2 is a semiconductor with a band gap energy Eg=3.2eV. If this material is irradiated with photons of the energy>3.2eV (wavelength λ<388nm, corresponding to the ultra-violet spectrum), the band gap is exceeded and an electron is promoted from the valence band to the conduction band (3-1). Consequently, electrons and positively charged holes are formed on the surface. The hole h^+ is the strong oxidant. They can react in an one-electron oxidation step with water (3-2) to produce reactive hydroxy-radical(• OH) which are very strong oxidizers, even stronger than the chlorine sterilizer, hydrochloric acid and ozone. Both the holes and the hydroxyl radicals are very powerful oxidants, which can be used to oxidize most harmful inorganic and organic contaminants. Moreover, the electron e^- is the strong reductant. And air oxygen can act as electron (3-3) by forming the super-oxide ion (O_2 • $^-$). Super oxide ions are also highly reactive particles, which are able to oxidize organic materials. Figure 3-1 (a)(b) [19,20] show the simplified reaction scheme of

photocatalysis.

Mechanism of the TiO_2 Photocatalyst:

$$TiO_2 + h\nu \rightarrow h^+ + e^- \quad (3\text{-}1)$$

$$H_2O + h^+ \rightarrow \cdot OH + H^+ \quad (3\text{-}2)$$

$$O_2 + e^- \rightarrow O_2 \cdot^- \quad (3\text{-}3)$$

In this study, for the first time, the improved characteristics of ultra–thin hafnium dielectrics prepared with both NH_3 plasma and irradiation treatment are investigated. We also report irradiated TiO_2 Photocatalyst brings about some chemical reactions with the HfO_2 film treated by NH_3 plasma, which can apparently improve hafnium gate dielectrics.

3.2 Experimental

In this chapter, Al/TaN/HfO_2/p-Si capacitors were fabricated. All 4-in p-type (100)-oriented wafers were first cleaned by standard RCA clean. Then, the HfO_2 film was deposited by a dual e-gun system immediately. After forming the gate dielectrics, some of the samples were treated by NH_3 plasma at 20W for 5 min. The gas flow rate is 60sccm and the reaction temperature is 350^{o}C.After that, the samples were irradiated by mask aligner (Light source 350~450nm) for 10 min. Then, a TaN metal gate of 25 nm is then deposited by a sputter. Thereafter, A Al film with a thickness of 500 nm was deposited on the TaN film by a thermal coater. The gate of the capacitor was patterned and defined by RIE with Cl_2/BCl_2 mixture. Finally, a 500 nm thick Al film was also deposited on the backside of the wafer to form the ohmic contact. The gate area is $6.362 \times 10^{-5} cm^2$. The cross-sectional view and total experimental procedures of the structure were shown in Fig. 3-2.

The electrical properties and reliability characteristics were measured by using the Hewlett-Packard 4156B (HP-4156B) semiconductor parameter analyzer. The

equivalent oxide thickness of the HfO_2 gate dielectric films were obtained by the high frequency (100KHz) C-V measurement using the Hewlett-Packard 4284.

3.3 Results and Discussion

3.3.1 SIMS analysis

Figure 3-3 shows the SIMS analysis of the as-deposited sample. The purity of HfO_2 target we use is 99.999% and other composition consists of TiO_2 and ZrO_2, which are both the same group with HfO_2 in a periodic table. From this figure, we can observe the HfO_2 film deposited by E-gun indeed consists of the TiO_2 Photocatalyst.

3.3.2 C-V Characteristics

The effective oxide thickness (EOT) was extracted from the equation shown as following:

$$C = \varepsilon A/d. \qquad (3\text{-}4)$$

Where C is he capacitance value in the accumulation region (-2 V)

ε is the dielectric constant of Si (~3.9)

A is the area of the capacitor

d is the effective oxide thickness

Figure 3-4 shows the high frequency (0.1MHz) capacitance versus gate voltage (C-V) characteristics of these samples. The EOT of these samples is about 1.8nm. We can see C-V curves don't change with the as-deposited sample and the sample treated by irradiation. Nevertheless, some C-V shifts are observed from the sample prepared with NH_3 plasma treatment owing to the nitrogen incorporation, making the flat-band shift toward less negative value[13-15]. Besides, it should be noted that the more shit in the sample treated by NH_3 plasma followed by irradiation is possibly due to a lot of

electron traps introduced during exposure by mask aligner. We suppose the wavelength of light source is 350~450nm, which exceeds the band gap of the TiO_2 Photocatalyst. So, an electron can be promoted from the valence to the conduction band. Consequently, the process is the charge-carrier generation (3-1). The hole h^+ is the strong oxidant and the electron e^- is the powerful reductant. We believe they can react with the HfO_2 film prepared with NH_3 plasma treatment. Possible chemical reactions of these are shown in following:

$$\equiv \mathbf{Hf\text{-}O\text{-}H + H + e^- (TiO_2 + h\nu) \rightarrow \equiv Hf\text{-}O^- + H_2} \quad \textbf{(3-5)}$$

$$\equiv \mathbf{Hf\text{-}N\text{-}H + H + e^- (TiO_2 + h\nu) \rightarrow \equiv Hf\text{-}N^- + H_2} \quad \textbf{(3-6)}$$

The observation indicates that a lot of oxide electron traps, $\equiv$Hf-O^- and $\equiv$Hf-N^-, in the dielectrics owing to the O-H and N-H bonds breakage, which the hydrogen is provided by the NH_3 plasma. Therefore, these reactions can explain the more shift for the C-V curve in the sample treated by NH_3 plasma and irradiation.

3.3.3 J-V Characteristics

The current density (J) in the J-V curve was obtained by using J=I/A, where A is the area of capacitor. The t_{ox} is the effective oxide thickness (EOT) determined by the C-V measurement. Figure 3-5 shows the J-V characteristics of these samples. We can find J-V curves are also the same with the as-deposited sample and the sample treated by exposure. Oppositely, NH_3 plasma treated samples perform well both in the breakdown voltage and the leakage current density, especially the sample under exposure. It is because that NH_3 plasma can induce the nitrogen incorporation and defect elimination to improve the dielectrics. Moreover, as the above-mentioned, irradiated TiO_2 Photocatalyst can induce a lot of electron traps owing to the O-H and N-H bonds breakage, which results in more obvious improvement of the HfO_2 film prepared with NH_3 plasma treatment. Nitridation was reported to introduce a large

number of hydrogen-containing species such as H, OH, and NH bonds into the films by dissociation of NH_3, resulting in a fatal disadvantage of large electron trapping. [11] Therefore, the sample treated by both NH_3 plasma and irradiation has the best performance of electrical properties.

3.3.4 Characteristics of Gate-leakage Current Density

Figure 3-6 shows the Weibull plot of the leakage current density at V_g=-1.5V for these samples. From this figure, we can observe that significant reduction of leakage currents is obtained after NH_3 plasma treatment. In addition, the improvement is more apparent during irradiation by mask aligner. Surprisingly, the improvement of the leakage current density is almost about one scale. We suppose it is possibly owing to a lot of electron traps generated during exposure, according to the C-V analysis.

3.3.5 Characteristics of voltage Breakdown

Figure 3-7 shows the Weibull plot of the dielectric breakdown voltage for the samples treated by NH_3 plasma and irradiation. From this figure, we can see that the dielectric breakdown field of the samples with the treatment of NH_3 plasma, especially during irradiation is obviously larger than the control sample with or without exposure. It is also found that irradiated TiO_2 Photocatalyst can apparently improve the breakdown field of the sample prepared with NH_3 plasma treatment.

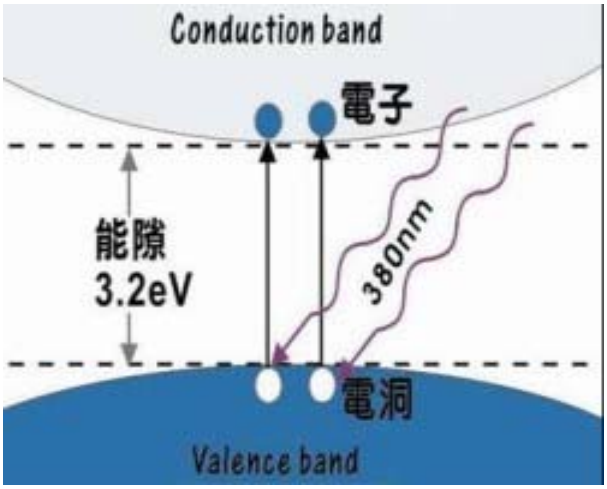
3.3.6 Time Dependent Dielectric Breakdown

The long-term reliability properties of the dielectrics are evaluated by measuring the time-dependent dielectric breakdown (TDDB) characteristics under constant oxide field stressing. The representative plots of current *vs* time during the

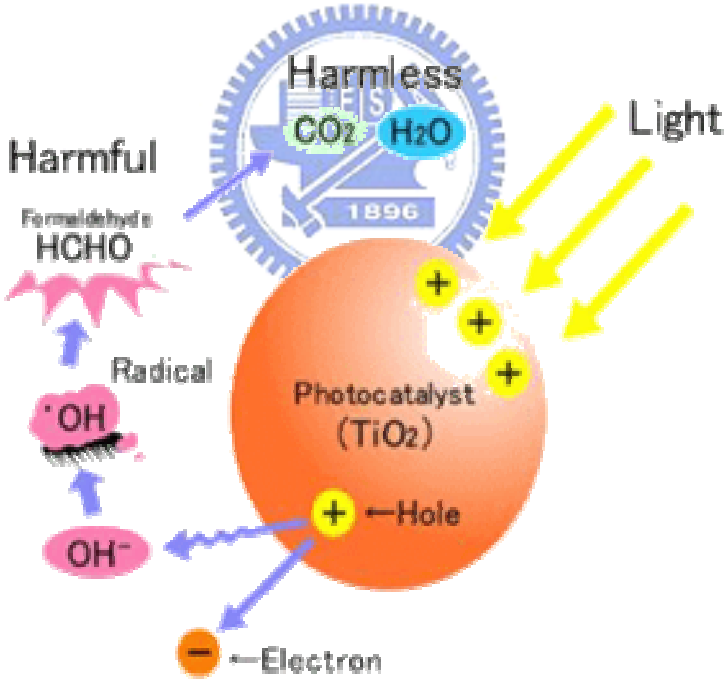
constant voltage stressing are shown in Fig. 3-8(-3V) and the Weibull plot of TDDB characteristics is presented in Fig. 3-9(-3V) and Fig.3-10 shows the negative breakdown field of the projected 10-year lifetime for these samples. From these figures, we can observe the treatment of NH_3 plasma is able to improve the reliability of HfO_2 film due to the nitrogen incorporation and if additionally during irradiation, it can improve more. We suppose irradiated TiO_2 Photocatalyst can result in the O-H and N-H bonds breakage, mentioned above, which leads to the obvious improvement of reliability. The hydrogen-related traps (-H,-OH and –NH) provided by NH_3 in the dielectrics cause fairly high fixed charge (Q_f), trapped charge (Q_{ot}),and interface state density (D_{it}) , which can result in serious reliability issue [11, 16-18].

3.4 Summary

In this chapter, for the first time, we present that irradiated TiO_2 Photocatalyst can obviously improve the HfO_2 with post NH_3 plasma treatment, including of lower gate leakage current, higher breakdown electric field, better reliability, and longer 10-year lifetime. Although NH_3 nitridation treatment can strengthen the dielectrics owing to the nitrogen incorporation [8~9,12], extra-hydrogen weak bonds such as O-H and N-H may degrade the reliability of dielectrics [16~18].To solve this problem, in general, additional thermal treatment higher than 600℃ can effectively cause these weak bonds breakage. At this section, we propose irradiated TiO_2 Photocatalyst can induce some chemical reactions (3-5,3-6)and generate a lot of electron traps owing to the O-H and N-H bonds breakage, which results in more obvious improvement of the HfO_2 film prepared with NH_3 plasma treatment.



(a)



(b)

Figure 3-1 (a)(b) [19,20] The simplified reaction scheme of photocatalysis.

Capacitor process

1. RCA clean, HF dip to remove native oxide

2. Deposition of HfO_2 with E-gun

3. Post-treatment

NH_3 plasma (350°C 20W 60sccm 600 mtorr) 5min

4. Irradiation by mask aligner for 10min

5. TaN/Al gate (To avoid the drawbacks of poly gate) & Mask #1

6. Contact Al (backside)

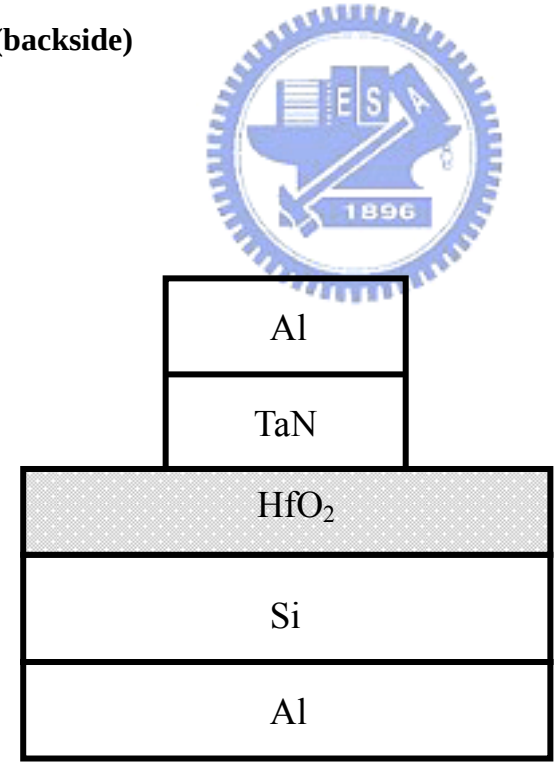


Fig.3-2 The cross-sectional view and total experimental procedures of the structure.

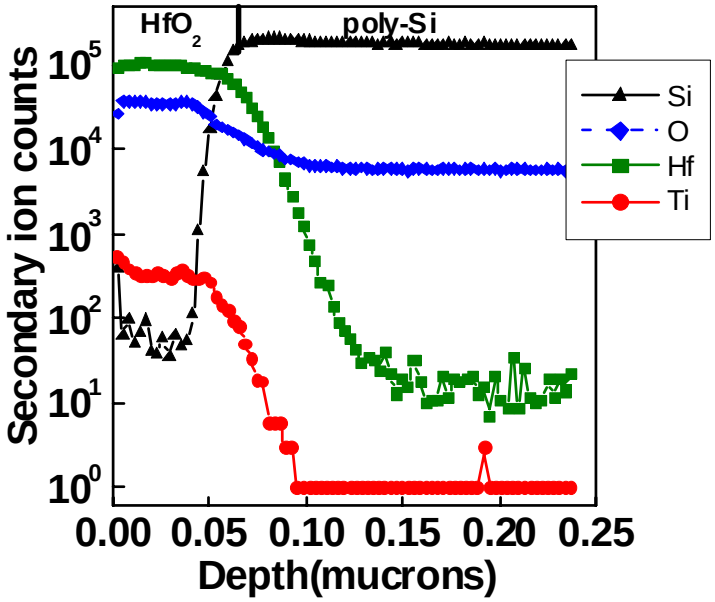


Fig.3-3. The SIMS analysis of the as-deposited sample

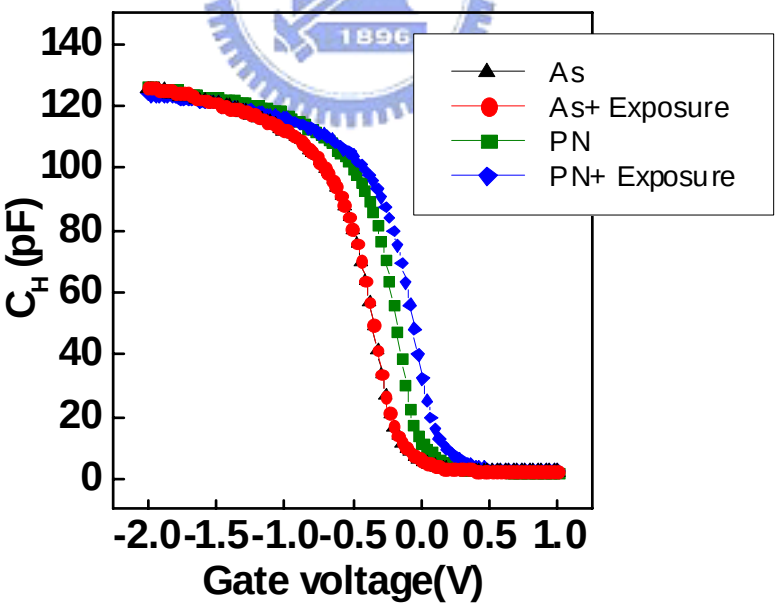


Fig.3-4 The high frequency (0.1MHz) capacitance versus gate voltage (C-V) characteristics of these samples.

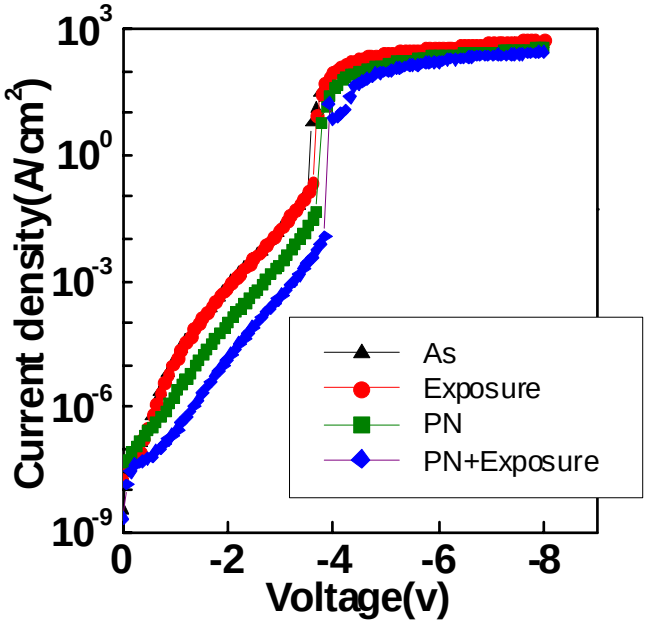


Fig.3-5 The J-V characteristics of these samples.

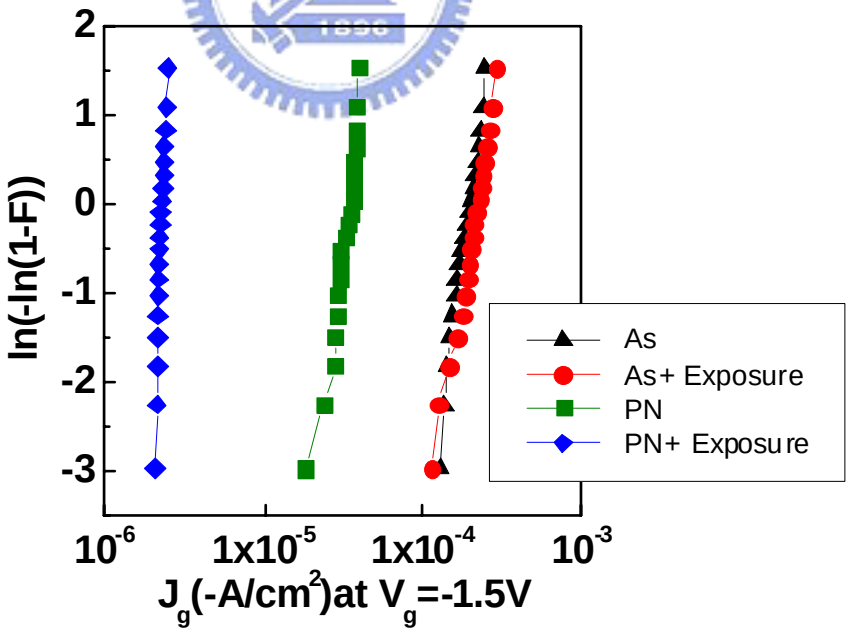


Fig.3-6 The Weibull plot of the leakage current density at V_g=-1.5V for these samples.

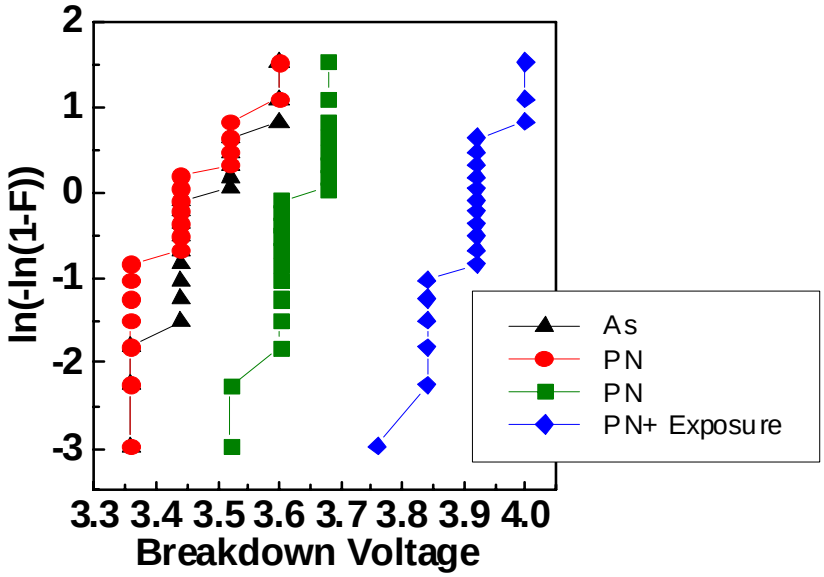


Fig.3-7 The Weibull plot of the dielectric breakdown voltage for these samples.

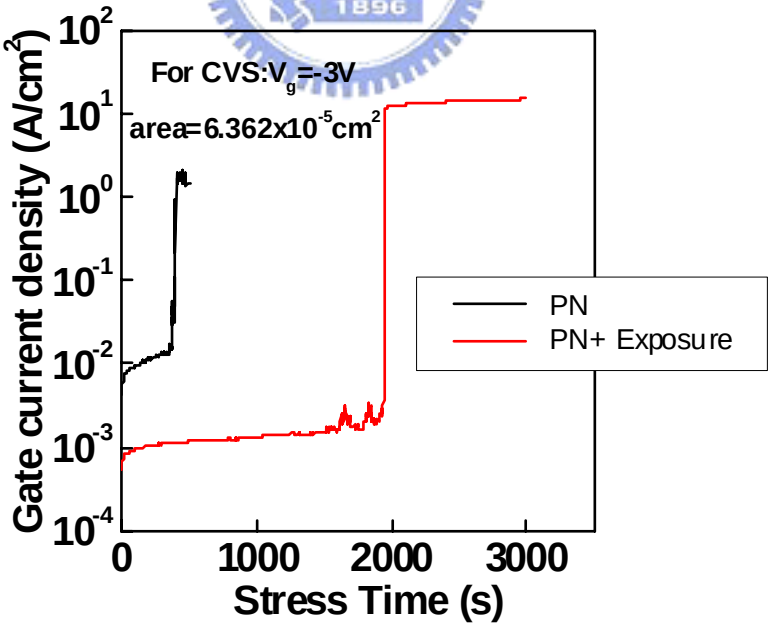


Fig.3-8 The representative plots of current *vs* time during the constant voltage stressing at -3V.

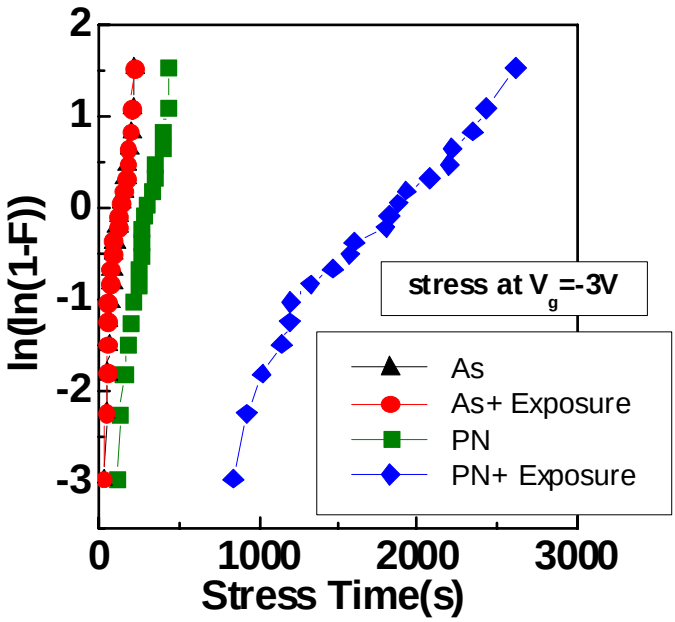


Fig.3-9 The Weibull plot of TDDB characteristics.

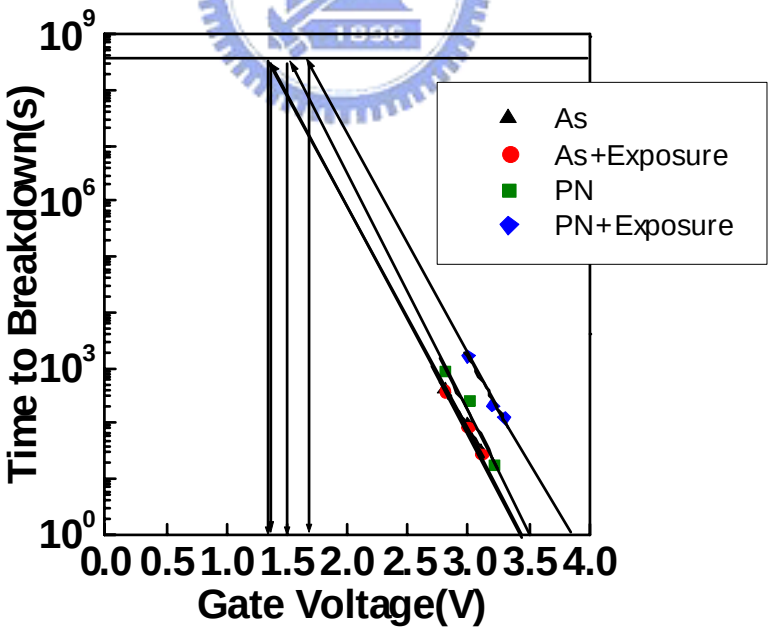


Fig.3-10 The negative breakdown field of the projected 10-year lifetime for these samples.

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Chapter 4

The preparation of interpoly-oxynitride dielectrics prepared with N_2O RTA and N_2O plasma treatment

4.1 Introduction

Thermally grown or deposited oxides on n^+ polysilicon have been used as the inter-dielectrics for nonvolatile memories such as erasable-programmable read-only memory(EPROM), electrical-erasable programmable read-only memory(EEPROM), and Flash memories. In order to obtain good data retention and endurance characteristics, inter-dielectrics with low conductivity (low leakage current) and high electric breakdown fields (E_{bd}) have been topics of research for a long time [1~3]. Because thermal oxidation of polysilicon leads to a rough polysilicon surface, it exhibits a lower dielectric strength and a higher leakage current than those of oxide grown on single crystal silicon [4~6]. Recently, in contrast to thermal oxide, deposited dielectric layers have been investigated as a very promising alternative, since these dielectric layers are deposited on the polysilicon layer without silicon consumption. Consequently, the surface of polysilicon is found to be smoother than oxidizing counterpart and dielectrics formed by low-pressure chemical vapor deposition(LPCVD) system have been used [7~9]. Furthermore, post deposition treatment in a rapid thermal annealing system is needed to improve electrical properties, which can achieve the effects of densification, re-oxidation, and nitridation [10]. It is also reported that N_2O-grown and N_2O-annealing polyoxides have better electrical performances than O_2-grown polyoxides, which attributes to the nitrogen

incorporation at the polyoxide/polysilicon interface [11~12].

In the recent memory technologies, short program/erase times and operating voltage reductions are most important issues to realize high speed/low power operation [13~15]. In order to accomplish these without a trade-off between low power and high speed operations, high coupling ratio should be achieved by increasing the floating gate capacitance [14~15]. However, decreasing the thickness of IPD to increase the floating gate capacitance may cause serious leakage and reliability problems which are fatal in the retention time of flash memories. Therefore, we focused on the application of high k IPD materials to increase and complexity of fabrication [16]. Moreover, the fact that oxynitride has a higher dielectric constant than the silicon dioxide presents many opportunities to decrease the EOT (equivalent oxide thickness).In this paper, for the first time, the interpoy-dielectrics deposited by LPCVD nitride and then prepared with N_2O RTA and N_2O plasma treatment were studied.

4.2 Experimental

In this chapter, n^+-polysilicon/interpoly-oxynitride/ n^+-polysilicon capacitors were fabricated. First, a 1000Å gate oxide was thermally grown on the 4-inch p-type (100) silicon substrate at 1050℃. Then the polysilicon film (poly Ⅰ) of 2000Å thickness was deposited in low pressure chemical vapor deposition (LPCVD) system and doped with $POCl_3$ at 900℃ for 30 min and drive in 15 min. The sheet resistance of poly1 was about 30-40 Ω/□. After a standard RCA cleaning, the silicon nitride films with thickness of 40Å were deposited in LPCVD system at 650℃. Soon after the nitrides deposited, they were annealed by RTAN_2O at 950^{o}C for 30sec.After that, they were treated by N_2O plasma at 20W, 50W for 10min . A second polysilicon film (poly Ⅱ) of 2000Å thickness was again deposited in LPCVD system and doped with

$POCl_3$ at 900℃ for 30 min and drive in 15 min. The sheet resistance of poly Ⅱ was about 30-40 Ω/□. After defining the poly Ⅱ's, the samples were deposited a 5000Å oxide by PECVD as passvation layers. Contact holes were defined and opened; then, a 5000 Å Al film was deposited and patterned as the electrodes. Finally, the samples were sintered at 350℃ for 30 min in N_2 ambient. Besides, the control sample was with N_2O RTA but without N_2O plasma treatment. The cross-sectional view and total experimental procedures of the structure were shown in Fig. 4-1.

The equivalent oxide thickness of the interpoly-oxynitride films were obtained by the high frequency (100KHz) C-V measurement. The electrical properties and reliability characteristics were measured by using the Hewlett-Packard 4156B (HP-4156B) semiconductor parameter analyzer.

4.3 Results and Discussion

4.3.1 J-E Characteristics

The electric field (E) in the J-E curve was obtained by using $E=V/t_{ox}$, where V was the applied voltage and t_{ox} was the effective oxide thickness (EOT) determined by the C-V measurement. Figure 4-2,and Figure 4-3 show the positive and negative J-E characteristics of these samples. The control sample was with RTAN_2O but without N_2O plasma treatment. We can find the interpoly-oxynitride dielectrics prepared with N_2O plasma treatment have improved breakdown electric field and leakage current density. In addition, it should be noted that under negative bias (gate injection), the improvement is more apparent. We believe N_2O plasma treatment can cause the reoxidation of the nitride film to form a SiO_xN_y, which exist at the top of nitride (near the poly Ⅱ). So, the effective oxide thickness of the oxynitride film slightly increases after N_2O plasma treatment. Therefore, the barrier height of SiO_xN_y and poly Ⅱ is

higher than Si_3N_4 and poly Ⅰ,which can explain the improvement of electrical properties is better under negative bias(gate injection). All phenomenon described above can be explained by the band diagrams in Fig.4-4 for the samples with N_2O plasma (a) under negative bias (gate injection) (b) under positive bias (substrate injection). Moreover, because poly Ⅰ undergoes extra thermal cycling than the poly Ⅱ, the grain growth will be more pronounced at the poly Ⅰ layer. The larger grain size of the poly Ⅰ layer may deteriorate its surface smoothness. Therefore the Si_3N_4/poly Ⅱ interface is smother than the Si_3N_4/poly Ⅰ interface, so at the same condition ,negative J-E curves have better performance than positive J-E curves.

4.3.2 Characteristics of Gate-leakage Current Density

Figure 4-5,and figure 4-6 show the Weibull plots of the leakage current density at V_g=±3V for the interpoly-oxynitride dielectrics prepared with N_2O RTA and N_2O plasma treatment. From these figures, we can observe that significant reduction of leakage currents is obtained after N_2O plasma treatment. The improvement is more apparent under negative bias(gate injection). Furthermore, it is also seen that the negative leakage current density is better than the positive leakage current density.

4.3.3 Characteristics of voltage Breakdown

Figure 4-7,and Figure 4-8 show the Weibull plots of the dielectric breakdown voltage for the samples treated by N_2O RTA and N_2O plasma treatment. From these figures, we can see that the dielectric breakdown field of the samples with the treatment of N_2O plasma is larger than the control sample without the treatment of N_2O plasma. This may be attributed to the reoxidation of the nitride film and form the SiO_xN_y oxynitride film to enlarge the dielectric breakdown field. Besides, it is also

found that the negative dielectric breakdown field is better than the positive dielectric breakdown field mentioned above.

4.3.4 Time Dependent Dielectric Breakdown

The long-term reliability properties of the dielectrics are evaluated by measuring the time-dependent dielectric breakdown (TDDB) characteristics under constant oxide field stressing. The representative plots of current *vs* time during the constant voltage stressing are shown in Fig. 4-9(4.2V),and Fig. 4-10(-4.7V), and the Weibull plots of TDDB characteristics are presented in Fig. 4-11(4.2V),and Fig. 4-12(-4.7V), and Fig. 4-13,and Fig. 4-14 show the positive and negative breakdown field of the projected 10-year lifetime for these samples. From these figures, we can find that the TDDB characteristics of the samples with the treatment of N_2O plasma are obviously improved. Recently, gate oxide failure is reported to be a limiting factor for scaling of oxide thickness, since time-to-breakdown decreases with increasing gate current [17]. The longer time-to-breakdown for the samples with N_2O plasma annealing is primarily ascribed to their lower leakage current, which causes less damage to the dielectric and thus contributes to a larger electric field of 10-year lifetime.

4.3.5 Gate Voltage Shift

The graphs of gate voltage shift versus stress time for the samples with RTAN_2O and N_2O plasma treatment is presented in Fig. 4-15.The figure indicates that electron trapping cause the increase in the gate voltage .Moreover, we can observe after the treatment of N_2O plasma, the gate voltage shift is more serious for both positive and negative gate injection. We believe the degradation should be due to plasma damage, which leads to higher electron traps and defects.

4.3.6 Measurement of Effective Barrier Height

The effective barrier height could be deduced from the Fowler-Nordheim tunneling equation or the Frenkel-Poole emission equation. First, we must measure the J-E curves in the accumulation region. Then we can calculate E from V, where V is V_{apply}. Based on the F-N tunneling model :

$$J \sim E^2 * \exp[-4(2m_e)^{1/2}(q\Phi_B)^{3/2}/3qhE] \quad (4\text{-}1)$$

$$\ln(J/E^2) \sim \{-4(2m_e)^{1/2}(q\Phi_B)^{3/2}/3qh\} * (1/E) \quad (4\text{-}2)$$

$$\ln(J/E^2) = \ln A - B/E \quad (4\text{-}3)$$

$$B = 46.8(\Phi_B)^{3/2} \quad (4\text{-}4)$$

Where E = electric field

m_e = effective electron mass

Φ_B = effective barrier height

B = the slope of $\ln(J/E^2)$ versus 1/E

From the plot of $\ln(J/E^2)$ versus 1/E, we can derive the value of Φ_B for F-N tunneling equation. In addition, based on the F-P tunneling model:

$$J = C_1 E * \exp\{-q[\Phi_B - (qE/\pi\varepsilon_i)^{1/2}]/kT\} \quad (4\text{-}5)$$

$$\ln(J/E) = \ln(C_1) - q[\Phi_B - (qE/\pi\varepsilon_i)^{1/2}]/kT \quad (4\text{-}6)$$

$$\ln(J/E) = C + D * E^{1/2} \quad (4\text{-}7)$$

$$C = \ln(C_1) - q\Phi_B/kT \quad (4\text{-}8)$$

Where C = the X- axis intersection

From the plot of ln(J/E) versus $E^{1/2}$, the X- axis intersection gives the value of $\ln(C_1) - q\Phi_B/kT$. Hence, if we desire to derive the value of Φ_B, we should have at least two different temperature T_1 and T_2 to cancel the constant of $\ln(C_1)$. In a word, the effective barrier height Φ_B is equal to $k(X_1-X_2)/q(T_2^{-1}-T_1^{-1})$ where X_1 and X_2 is the X- axis intersection at T_1 and T_2. We find that these samples show the relatively weak temperature dependence, so we believe the F-N tunneling is the dominant tunneling

mechanism. Fig.4-18 shows the F-N fitting in the high field region of the sample with RTA at 950^{o}C and the measured poly Ⅱ/SiO_xN_y barrier height is about 1.96eV.

Figure 4-16, and Figure 4-17 the plots both polarities of extrapolated electric field over the 10-year lifetime (E_{10y}) and the effective barrier height (Φ_B) determined by using the Fowler-Nordheim (F-N) model of the interpoly-oxynitride dielectrics prepared with N_2O plasma treatment. Indeed, the effective barrier height and the extrapolated electric field over the 10-year lifetime obviously increased after N_2O plasma treatment, especially under negative bias (gate injection).

4.4 Summary:

This work examined the interpoly-oxynitride films with N_2O RTA followed by N_2O plasma treatment. The control sample was with N_2O RTA but without N_2O plasma treatment. N_2O plasma treatment can cause the reoxidation of the nitride film to form a SiO_xN_y, which exist at the top of nitride (near the poly Ⅱ).Although the effective oxide thickness of the oxynitride film slightly increases after N_2O plasma treatment, it is found that the samples after the process of N_2O plasma treatment exhibit obviously higher breakdown field, lower leakage current, longer time-to-breakdown, and larger effective barrier height than the control samples. Moreover, the improvement is more apparent under negative bias(gate injection). Unfortunately, N_2O plasma treatment can bring about plasma damage, which leads to higher gate voltage shift due to higher electron traps and defects. In sum, the oxynitride treated by N_2O RTA and N_2O plasma treatment is still suitable for use in the next generation on EEPROM.

1. Isolation oxide 1000Å

2. Siliane(SiH_4) poly-Si 2000Å(poly1)

3. $POCl_3$ doped at 900℃

4. LPCVD nitride 40 Å

5. N_2O RTA 950℃ 30s

6. N_2O Plasma treatment 20W/50W 10 min 1000mmtorr

7. Siliane(SiH_4) poly-Si 2000Å(poly2)

6. POCl3 doped at 900℃

7. Define active region

8. PECVD oxide 5000Å

9. Open contact hole

10. Aluminum 5000Å

11. Define Aluminum pattern

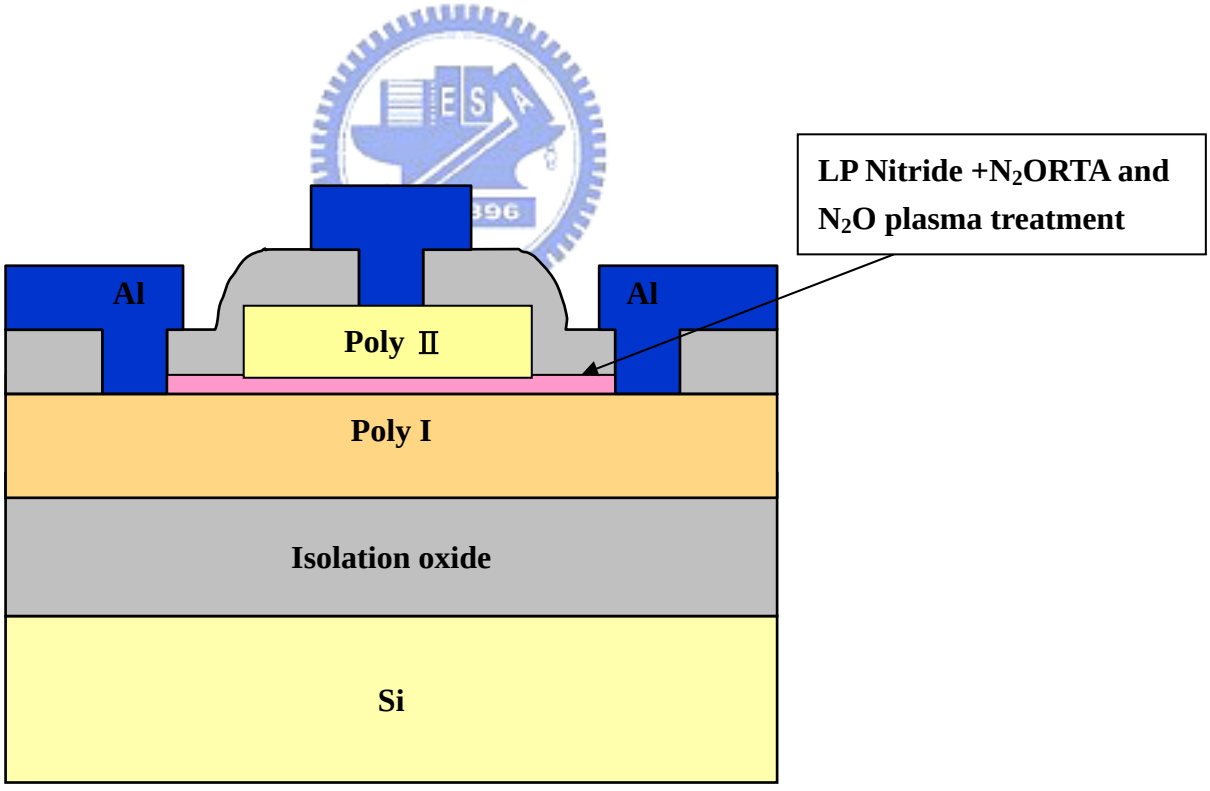

Fig.4-1 Key process flows of the fabrication for MIM capacitor with interpoly-oxynitride dielectrics.

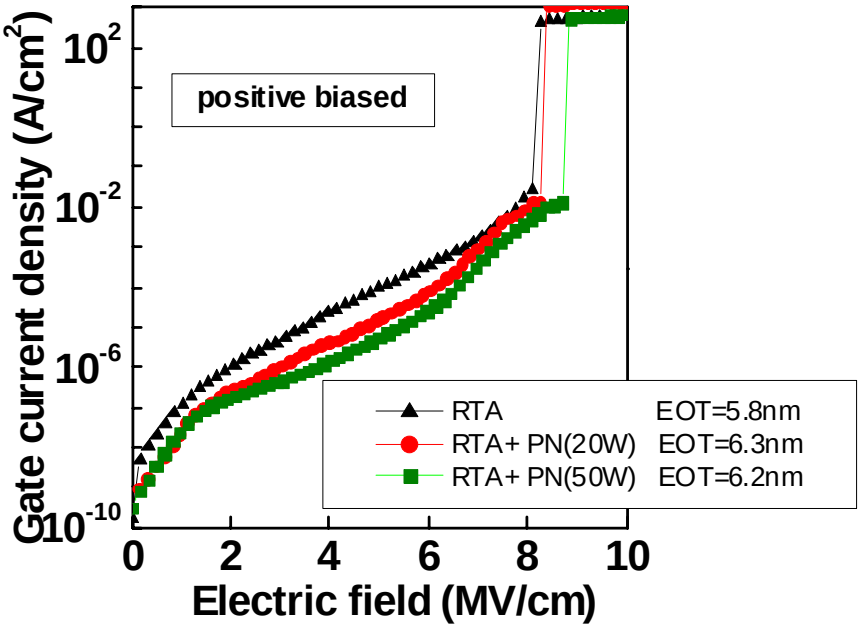

Fig.4-2 J-E characteristics of interpoly-oxynitride films of the control sample and the samples with N_2O RTA and N_2O plasma treatment, under poly Ⅱ positive bias.

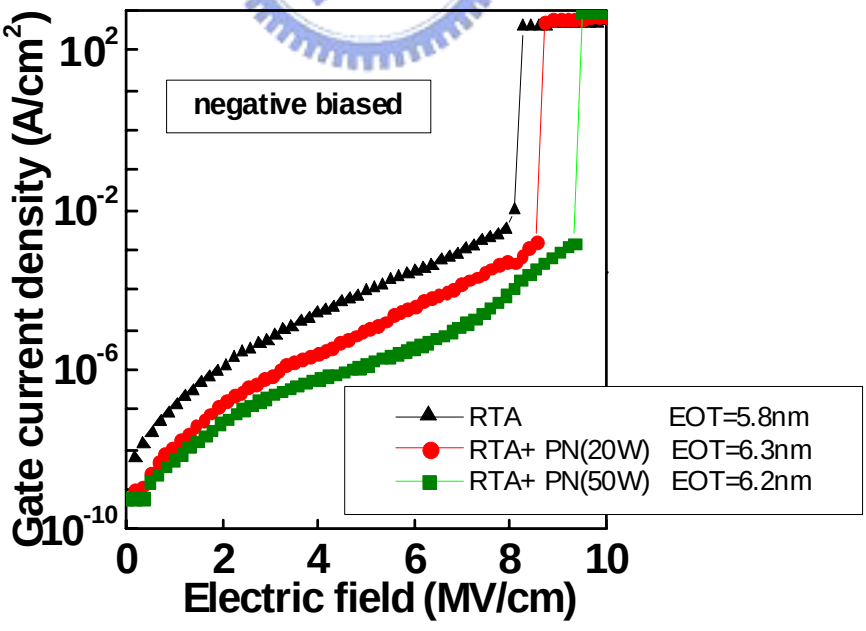

Fig.4-3 J-E characteristics of interpoly-oxynitride films of the control sample and the samples with N_2O RTA and N_2O plasma treatment, under poly Ⅱ negative bias.

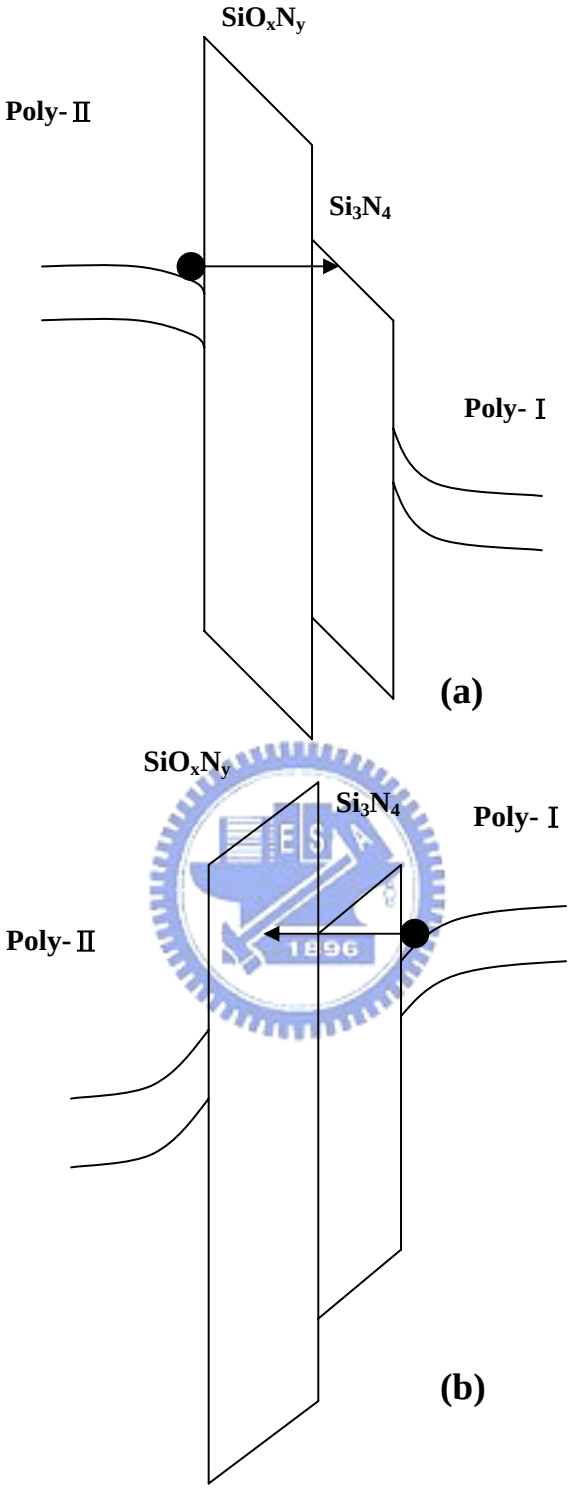

Fig.4-4 Band diagrams of the interpoly-oxynitride dielectrics for the samples with N_2O RTA and N_2O plasma treatment, under (a) poly Ⅱ negative bias and (b) poly Ⅱ positive bias.

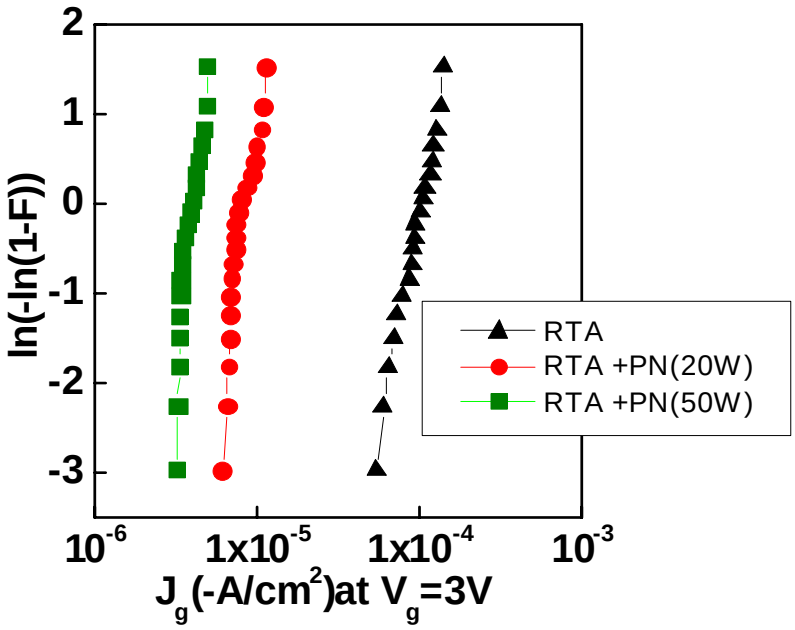

Fig.4-5 the Weibull plots of the leakage current density at V_g=+3V for the interpoly-oxynitride dielectrics prepared with N_2O RTA and N_2O plasma treatment.

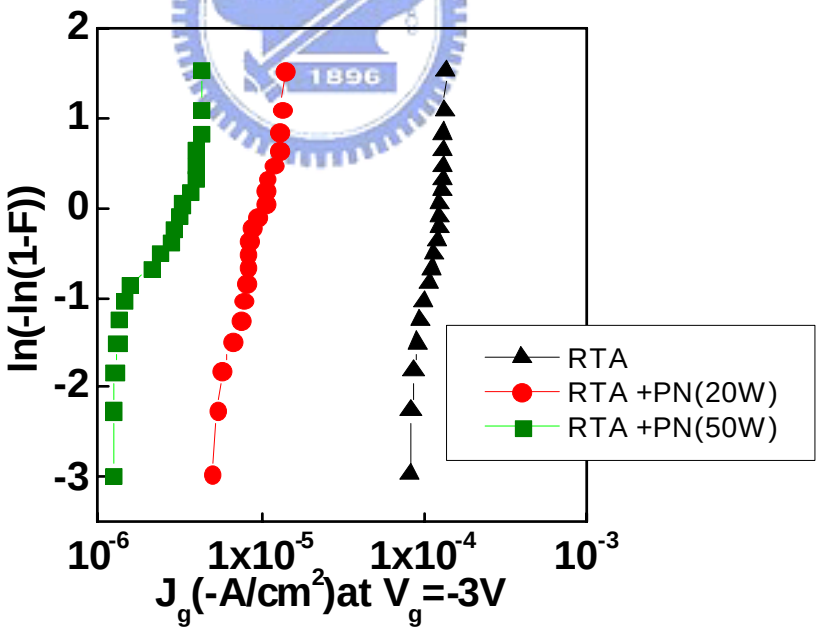

Fig.4-6 the Weibull plots of the leakage current density at V_g=-3V for the interpoly-oxynitride dielectrics prepared with N_2O RTA and N_2O plasma treatment.

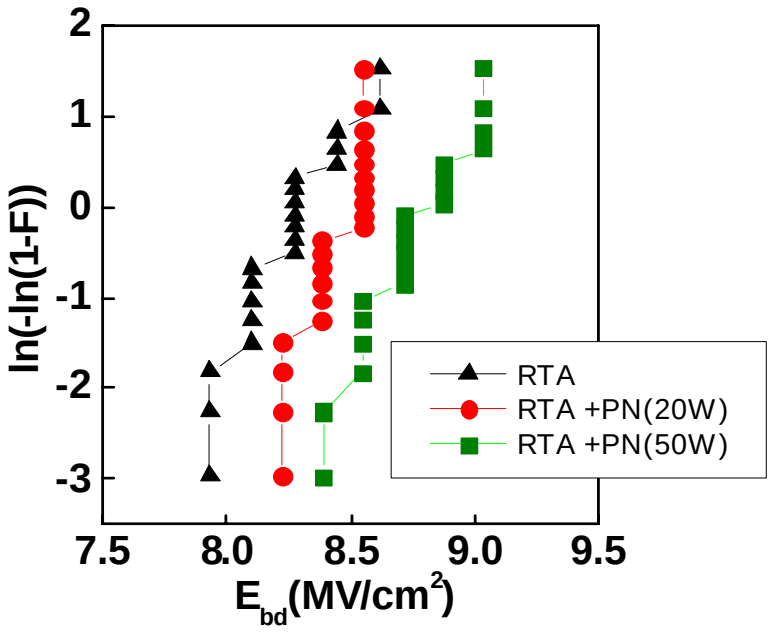

Fig.4-7 the Weibull plots of the dielectric breakdown voltage for the samples treated by N_2O RTA and N_2O plasma treatment under poly Ⅱ positive bias .

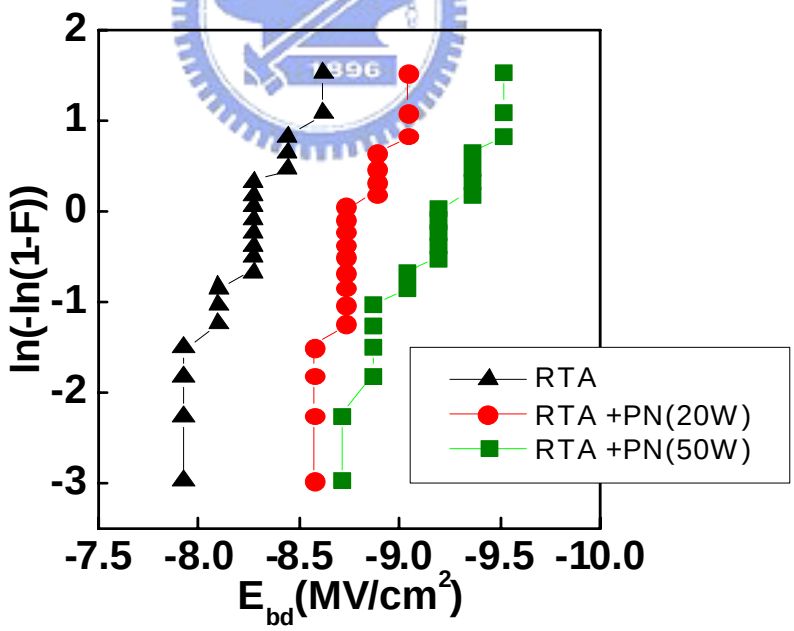

Fig.4-8. the Weibull plots of the dielectric breakdown voltage for the samples treated by N_2O RTA and N_2O plasma treatment under poly Ⅱ negative bias

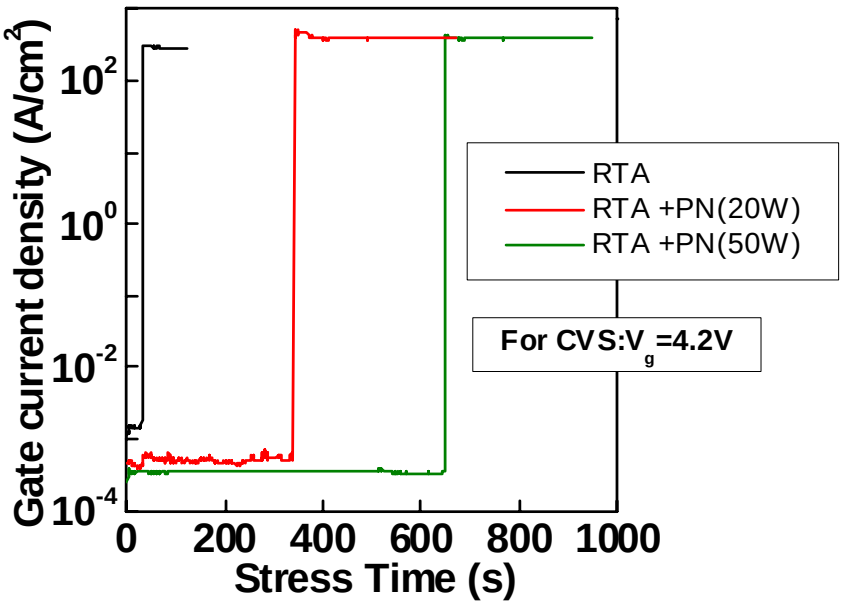

Fig.4-9 The representative plots of current *vs* time during the constant voltage stressing at V_g=4.2V.

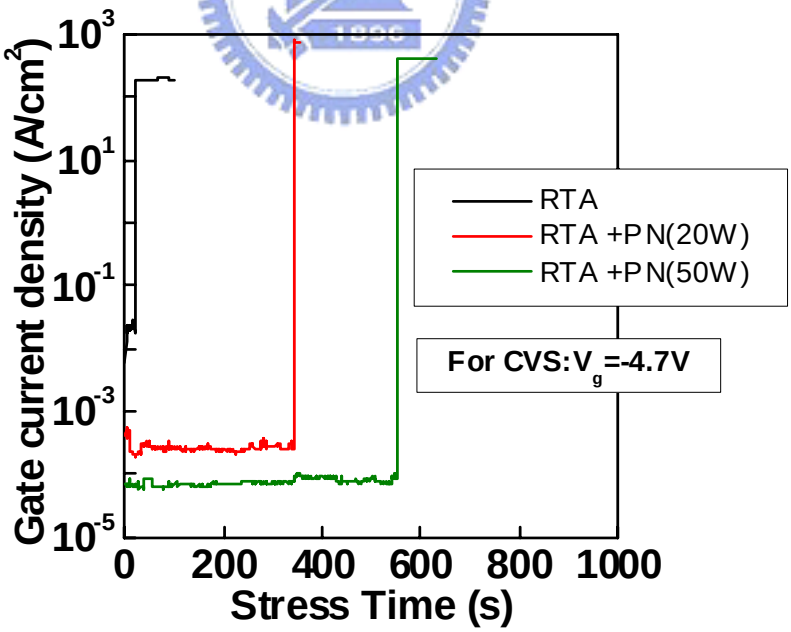

Fig.4-10 The representative plots of current *vs* time during the constant voltage stressing at V_g=-4.7V.

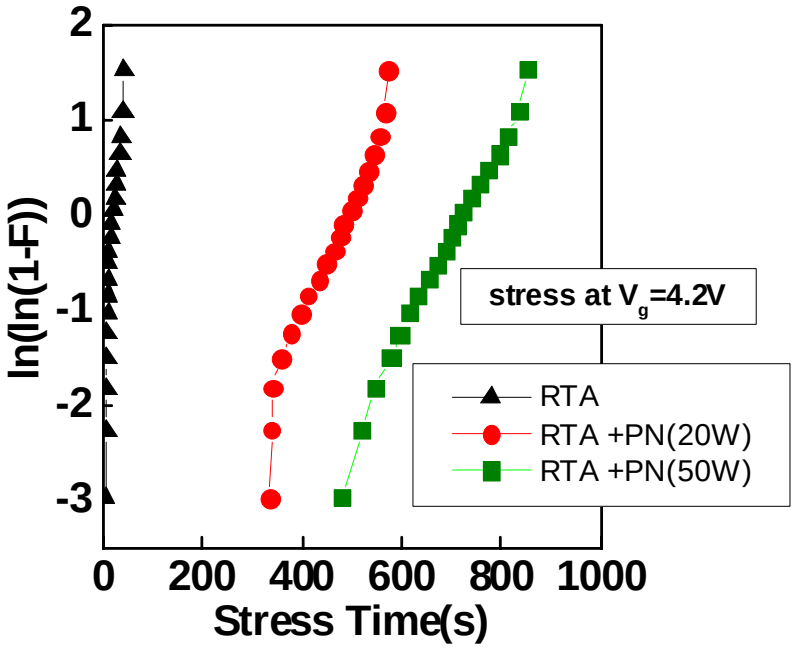

Fig.4-11 the Weibull plots of TDDB characteristics of the samples with N_2O RTA and N_2O plasma treatment, under poly Ⅱ positive bias.

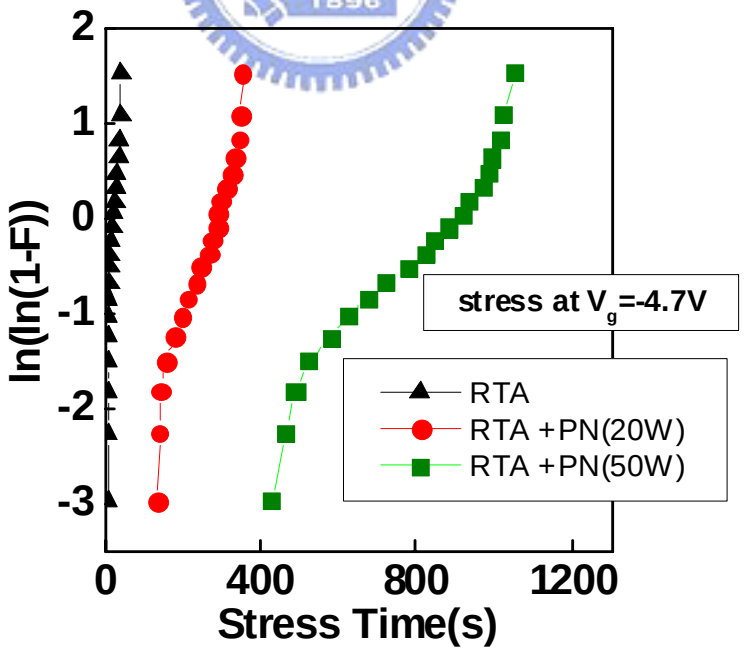

Fig.4-12 the Weibull plots of TDDB characteristics of the samples with N_2O RTA and N_2O plasma treatment, under poly Ⅱ negative bias.

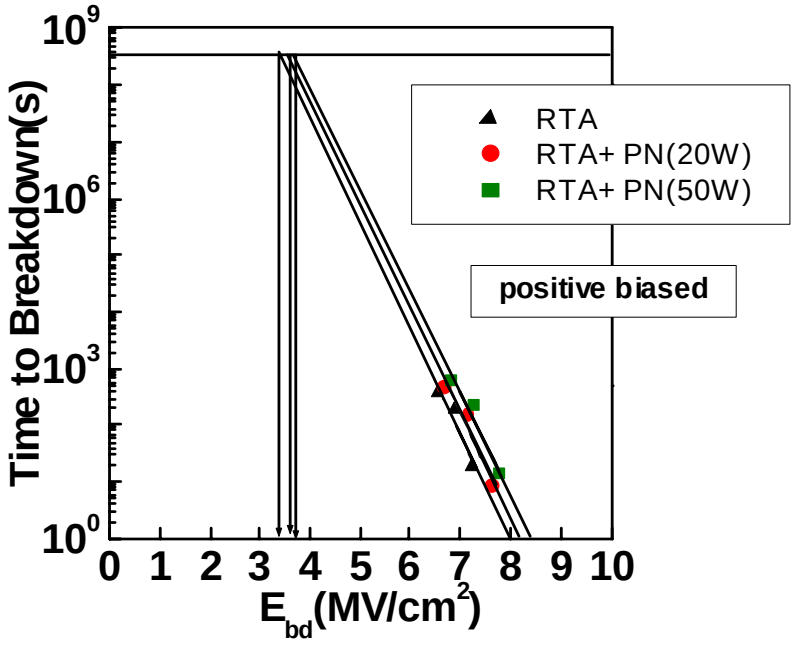

Fig.4-13 the positive breakdown field of the projected 10-year lifetime for these samples .

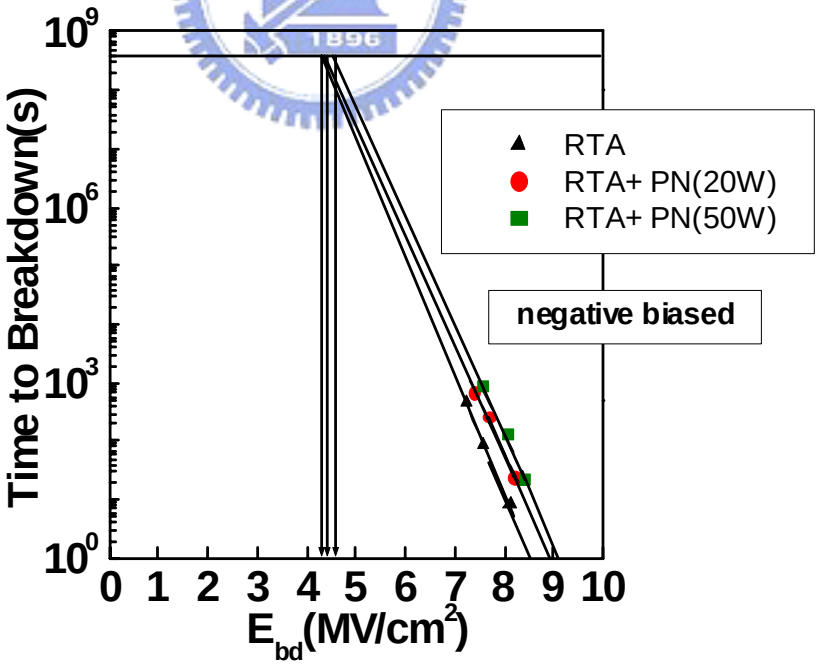

Fig.4-14 the negative breakdown field of the projected 10-year lifetime for these samples .

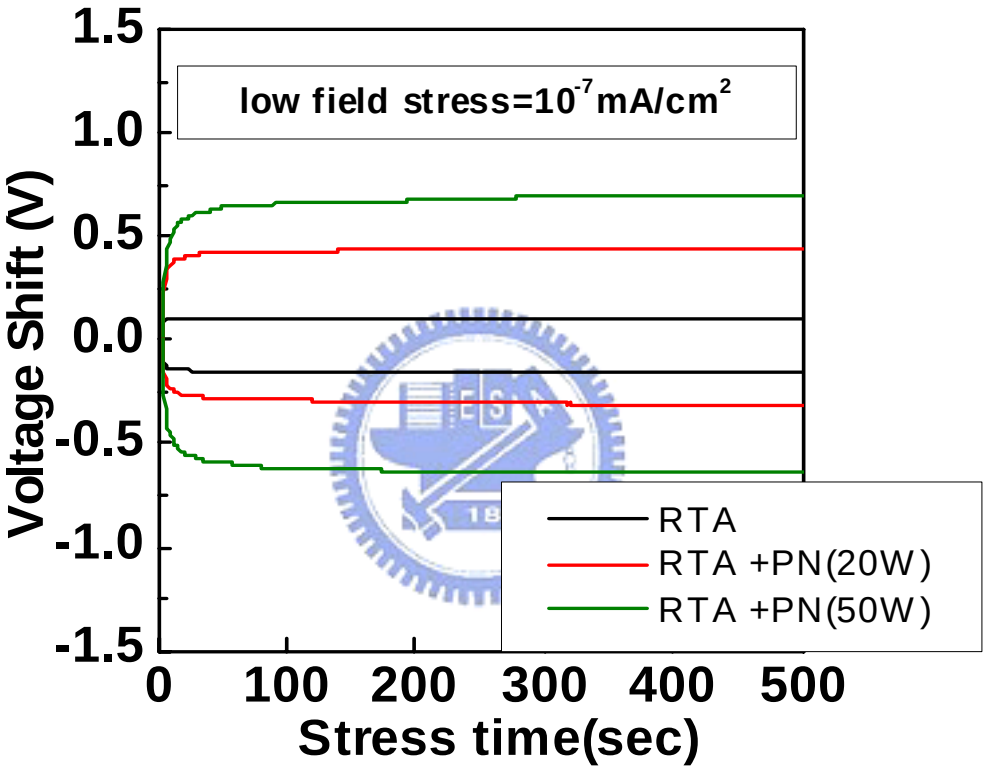

Fig.4-15 The graphs of gate voltage shift versus stress time for the samples with RTAN_2O and N_2O plasma treatment.

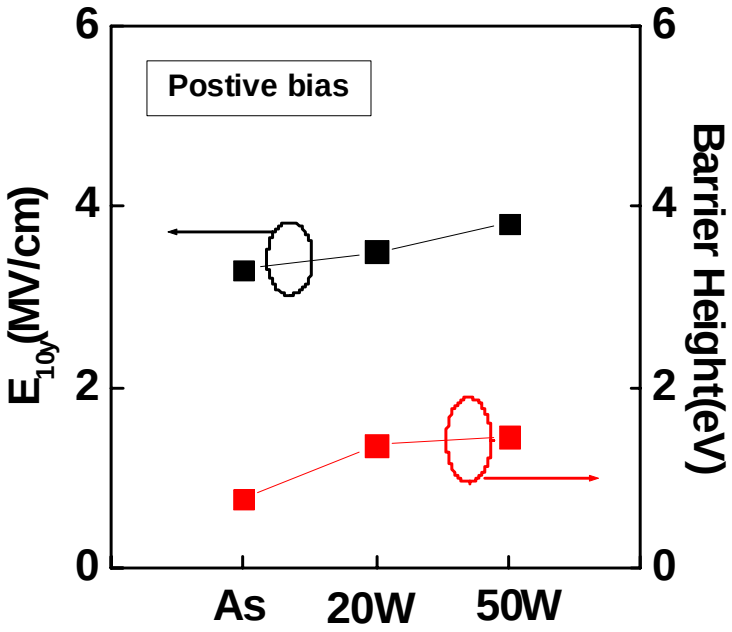

Fig.4-16 the plots both polarities of extrapolated electric field over the 10-year lifetime (E_{10y}) and the effective barrier height (Φ_B) under poly Ⅱ positive bias.

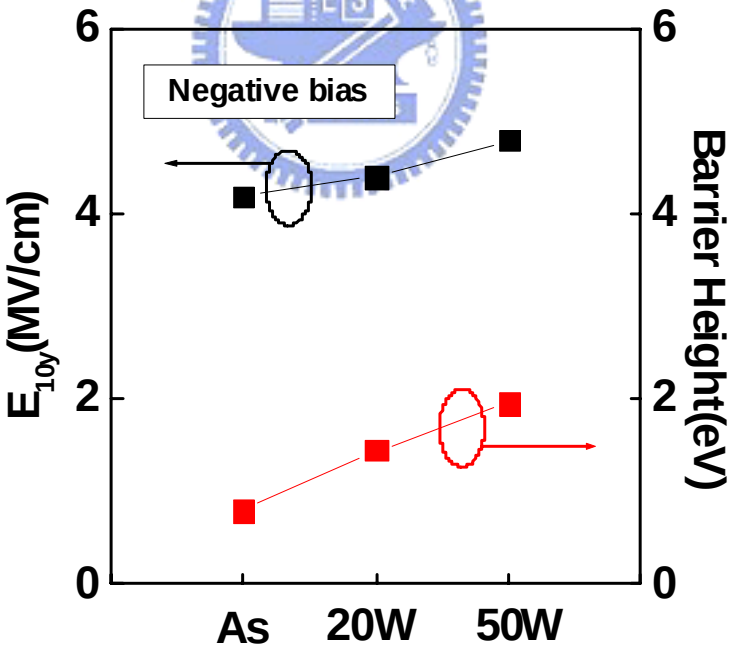

Fig.4-17 the plots both polarities of extrapolated electric field over the 10-year lifetime (E_{10y}) and the effective barrier height (Φ_B) under poly Ⅱ negative bias.

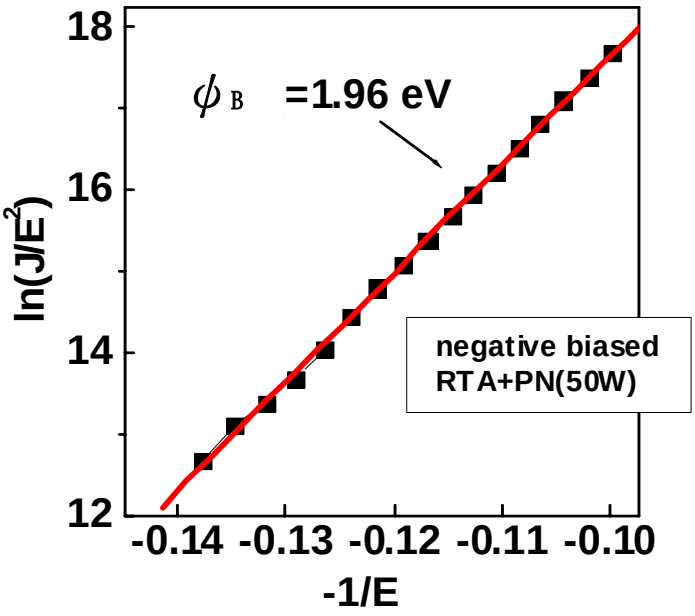

Fig.4-18 the F-N fitting in the high field region of the sample with RTA at 950°C and the measured poly Ⅱ/SiO_xN_y barrier height is about 1.96eV.

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Chapter 5

Conclusions

The study of Cerium-based gate dielectrics, Hafnium-based gate dielectrics, and inter-poly oxynitride were proposed. Major contributions of each subject in this work are summarized as follows.

First, we have investigated an ultra-thin cerium dioxide with post-deposition rapid thermal annealing, which exhibits the thin EOT (~1.4nm for the RTA950^{o}C sample) and superior properties. The rapid thermal annealing can effectively improve the reliability and quality of the cerium dioxide owing to the elimination of traps in the dielectrics and interfacial layer between CeO_2/Si. Besides, the cerium dioxide has excellent thermal stability on Si substrate and high temperature to crystallize. Therefore, it can be the candidate for the future ultra-large scale integrated circuit (ULSI) applications. In addition, the band diagram of cerium dioxide with Al gate was also established for the first time. In particular, we have obtained the CeO_2/Si barrier height of 0.75eV ($m^*=0.2m_0$ for Si) that will be useful for modeling and simulation in the cerium dielectrics. Besides, the experimental results shows that F-P conduction dominants the as-deposited sample, and as the RTA temperature increases, the F-N tunneling become more important owing to the elimination of traps in the dielectrics.

Next, for the first time, we present that irradiated TiO_2 Photocatalyst can obviously improve the HfO_2 with post NH_3 plasma treatment, including of lower gate leakage current, higher breakdown electric field, better reliability, and longer 10-year

lifetime. It is because that irradiated TiO_2 Photocatalyst can induce some chemical reactions and generate a lot of electron traps owing to the O-H and N-H bonds breakage, which results in more obvious improvement of the HfO_2 film prepared with NH_3 plasma treatment.

Finally, we have reported the interpoly-oxynitride films with N_2O RTA followed by N_2O plasma treatment. N_2O plasma treatment can cause the reoxidation of the nitride film to form a SiO_xN_y, which exist at the top of nitride (near the poly Ⅱ).Although the effective oxide thickness of the oxynitride film slightly increases after N_2O plasma treatment, it is found that the samples after the process of N_2O plasma treatment exhibit obviously higher breakdown field, lower leakage current, longer time-to-breakdown, and larger effective barrier height than the control samples. Moreover, the improvement is more apparent under negative bias(gate injection). Unfortunately, N_2O plasma treatment can bring about plasma damage, which leads to higher gate voltage shift due to higher electron traps and defects. In sum, the oxynitride treated by N_2O RTA and N_2O plasma treatment is still suitable for use in the next generation on EEPROM.

簡歷

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