Chapter 1

Introduction

1.1 Background

The rapid advancement of complementary metal-oxide-semiconductor (CMOS) integrated circuit(IC) technologies in the past few decades has enabled the Si-based microelectronics industry to meet several technological requirements and fuel market expansion. These requirements include high performance (speed), low static (off-state) power, and a wide range of power supply and output voltages. The key for the targets is the ability to perform a calculated reduction of the dimensions of the fundamental active device in the circuit, i.e. the metal-oxide-semiconductor field effect transistor (MOSFET)—a practice termed "scaling". Scaling of devices has resulted in a dramatic expansion in technology and communications markets including the market associated with high-performance microprocessors as well as low static-power applications, such as wireless system [10]. And thanks to the miniaturization, the number of components in a DRAM has increased more than 100,000 times and clock frequency of a CPU has increased to more than 2GHz.

The key element enabling the scaling of the Si-based MOSFETs is the dielectric,

and the resultant electrical properties associated with it, which is employed to isolate the transistor gate from the Si channel in a CMOS device. The requirement to scale SiO_2 arises from achieving a high current drive by keeping the amount of charge induced in the channel large as the power supply voltage decreases [11]. It is evident that shrinking the conventional MOSFET requires innovations to circumvent some fundamental physical barriers.

According to the International Technology Roadmap for Semiconductors (ITRS), a gate oxide thinner than 1.0 nm is needed within a decade, which is a formidable challenge. When the oxide thickness is less than 1.5 nm, there are only two to three atomic layers in the film. With such a thin gate oxide, carriers can transport through dielectric via direct tunneling and lead to an exponential increase of gate leakage current [1]–[4]. The resulting gate leakage current will increase the power dissipation and deteriorate the device performance and circuit stability for VLSI circuits. Therefore, alternative gate dielectrics with higher dielectric constants are being pursued due to their thicker physical thickness at the same equivalent oxide thickness (EOT). High-gate dielectrics such as Al_2O_3 (K~10), HfO_2 (K~25), ZrO_2 (K~25), La_2O_3 (K~27) and TiO_2 (K~50) have received much attention recently because of the effectiveness in preventing the direct gate tunneling [5]–[7].

In the last few years, many works have been done to understand the properties of abovementioned high-K gate dielectrics including the technological issues with their fabrication. Some of the problems currently being looked at by various research groups include interfacial layer formation during the thermal process, micro-crystal formation during the process and the mobility degradation. Also, higher physical gate dielectric thickness (by a factor of K_{gate}/K_{SiO2}) in MOS transistors results in higher fringing fields from gate to source/drain regions, which would weaken the gate control [8]. This leads to poor subthreshold performance and more severe short channel effects. Furthermore, materials having relatively low dielectric constant such as Al_2O_3 do not provide sufficient advantages over SiO_2 or Si_3N_4 [9]. Too low and too high dielectric constant materials may not be a good choice for alternative gate dielectric applications. Then, to find an appropriate dielectric constant material with suitable k value is very important. Recently, HfO_2 (K~25) and rare earth oxides such as La_2O_3 and Pr_2O_3 are considered to be the promising candidates for the next generation.

1.2 The Choice of High-K Materials

Applications of SiO_2 material in gate fabrication process were well defined for many decades because thermal oxide has several non-replaceable advantages, such as

being amorphous phase throughout the integration process, high-quality interface, and excellent thermal stability. Staying in amorphous phase is beneficial for the low leakage current, while less interface state density is critical to the resultant high carrier mobility at the Si/SiO_2 interface. This near perfect interface quality makes the carriers transporting in device channel suffer less scattering and/or trapping/detrapping. Moreover, the thermal stability of SiO_2 makes it extremely resistant to the high temperature processing in CMOS fabrication [12]. Even though thermal oxide possesses above-mentioned advantages, nevertheless, the intolerable large leakage current via direct tunneling imposes the physical limit on further oxide scaling. Hence, we are forced to consider replacing thermal oxide with those having higher dielectric constant to increase the physical thickness for lowering leakage current, while maintain the gate capacitance in aiming at continuing the pace of device shrinking.

Compared to the thermal grown SiO_2, the high-k materials have some challenging issues that need to be overcome. Critical issues and criteria for high-k materials are summarized in Table 1-1 [13]:

(1).Suitable k-value：

The dielectric constant has to be in the reasonable range according to the criteria. Those materials with slightly higher κ-value than thermal oxide do not meet the requirement of lowering the leakage current with increasing physical thickness. Large κ-value material, in general, has poor thermal stability and will suffer from larger fringing field and degraded short channel characteristics [14]. For example, when NMOS devices are working, the gate and drain are biased with the positive voltage, the source and the substrate are usually grounded. The fringing effect will make extra

field lines terminate in the S/D region and share the charge controllability with the gate. This will lower the potential in the channel for electron, and aggravate the gate control ability. The phenomenon makes the threshold voltage unstable, as it becomes harder for the gate to control the carriers in the channel. The off-state leakage current will also be increased by the FIBL (fringing field induced barrier lowing) effect.

(2). Wide bandgap

For gate dielectric, the leakage current is one of the most important issues for choosing high-k materials. However, it is found that most of the high-k materials do not have appropriate wide bandgap. The bandgaps of some well-known high-k materials are present in Fig 1-1 [13]. If high-k materials do not have appropriate barrier height with respect to the silicon substrate, electrons will transport (either by thermal emission or direct tunneling) through the gate dielectric easily and lead to unacceptably large leakage currents. These kinds of high-k materials are not suitable as the gate dielectrics to replace SiO_2.

(3). Thermal stability

Most high-k materials reported previously would react with the Si under equilibrium conditions. It will induce two kinds of reactions. First, after the relatively high temperature process, the metal in high-k materials would separate out, and the oxygen would react with Si to form an unwanted interfacial layer in the interface. The reaction relationship is represented as [eq-1] .

$$MO_x + Si = M + SiO_2 \quad \text{[eq-1]}$$

Second, the high-k materials MO_x will react with Si to form the silicide MSi_y , The reaction relationship is represented as [eq-2] .

$$MO_x + Si = MSi_y + Si \qquad \text{[eq-2]}$$

The formation of the silicide would provide the transport path to carriers, and induce large leakage current. Irrespective of SiO_2 or silicide MSi_y, these interfacial layers have lower k-value, and they would reduce the effective dielectric constant of the overall gate capacitor. This makes the effective oxide thickness (EOT) difficult to scale down.

(4). Interface quality

A high-quality interface between high-k films and Si substrates is essential. The interface would affect the carrier mobility in the channel, and is directly related to the device performance. Many high-k materials are plagued with the same mobility degradation problem. This degradation will lower the device driving current. The poor interface between high-k material and Si substrate and the origin of the interface traps are not fully understood. Therefore, good quality of interfacial layer between high-k material and Si substrate must be obtained.

(5). Film morphology

Most of the advanced gate dielectrics studied to date are either polycrystalline or single crystal films, however, it is desirable to choose a material that remains in a glassy phase (amorphous) throughout the necessary processing treatments. The thermal budget will have an important influence on the film morphology. Moreover,

high temperature process would make high-k dielectrics change phase [9]-[10], and would induce large gate leakage current.

1.3 Motivation

Reducing the gate leakage current in ultra thin gate dielectrics is the key issue for the research in high-k materials. Many high-k materials have emerged as promising gate dielectric candidates for sub 100nm technology due to their superior thermal stability, smaller leakage current than SiO_2, large band gap with favorable band alignments. Another consideration is that the integration of metal gate with high-k material in order to avoid the drawbacks of poly depletion.

Many groups worldwide have done numerous studies on HfO_2, and ZrO_2 gate dielectrics, and abundant papers have been published. These results have revealed that HfO_2 gate dielectrics have the potential to replace SiO_2 gate dielectric for future ULSI production.

Recently, rare earth metal oxides such as amorphous La_2O_3 gate dielectrics and Pr_2O_3 films deposited on Si substrates were reported as potential candidates for future high-k gate insulator, and they show excellent electrical properties such as high dielectric constant and small EOT with low leakage current density. The reason that various rare earth metal oxides have been reported is that the rare earth oxides are

expected to be stable in contact with Si even at high temperature from the thermodynamic point of view.

In line with this, we studied the characteristics of La_2O_3, Pr_2O_3 and HfO_2 gate dielectrics in this thesis. For La_2O_3 and Pr_2O_3, we studied their basic physical and electrical properties since only a very few literatures have ever reported on these two metal oxides. For HfO_2 gate dielectric, we introduced a new low temperature NH_3 treatment to improve its characteristics. We expect such processes could lower the leakage current, enhance the crystal temperature and further improve hysteresis, and reliability of the HfO_2 gate dielectric.

1.4 Thesis Organization

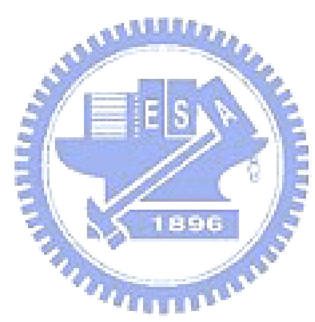
In this thesis, we studied the characteristics of La_2O_3, $Pr_2O_3$and HfO_2 gate dielectrics.

In Chapter 2, the basic characteristics of La_2O_3 and Pr_2O_3gate dielectrics are presented including the electrical characteristics such as J-V, EOT, C-V curves, gate leakage current density and material analyses. We employ the RTO pre-treatment to achieve better La_2O_3 gate dielectrics

In Chapter 3, the electrical characteristics of HfO_2 gate dielectrics with low temperature NH_3 treatment are presented. We discuss the effect of low temperature NH_3 treatment on J-V, C-V characteristics, breakdown field, gate leakage current,

SILC, hysteresis and reliability. We employ the low temperature NH_3 treatment in different process sequences such as bottom (surface) treatment, and top treatment (after deposition of HfO_2 gate dielectrics). We try to find out the optimized treatment method.

In Chapter 4, important conclusions from our experimental results are summarized, and recommendations for future work are given.



Chapter 2

Characterizations of E-Beam-Deposited La_2O_3, Pr_2O_3 High-k Thin Films on Si Substrates

2.1 Introduction

High-dielectric constant (high-k) materials for alternative gate insulator, such as ZrO_2, HfO_2, Al_2O_3 etc., have received much attention as a promising cure to the leakage current issue of ultra-thin SiO_2, the de facto gate dielectric for more than 30 years. However, there are still technical hurdles before these materials can replace SiO_2, such as interfacial layer and/or micro crystal formations during the post deposition annealing process that led to the increase of EOT (Equivalent Oxide Thickness) and gate leakage current, respectively [15-19].

Recently, rare earth metal oxides such as amorphous La_2O_3 [20] and epitaxial Pr_2O_3 [21] films deposited on Si substrates were reported as potential contenders for the next generation high-k gate insulator, and they showed excellent electrical properties such as high dielectric constant and small EOT with low leakage current density. Other rare earth metal oxides such as Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3 [22, 23]have also been reported for potential gate insulator applications. The incentive behind them is that the rare earth oxides are expected to be stable in contact with Si

even at high temperature from the thermodynamics point of view [24]. However, their properties, such as bandgap and lattice energy, are quite different from each other [25-28]. La_2O_3 and epitaxial Pr_2O_3 show excellent electrical properties. However, it is well known that they are unstable in contact with the air probably because their lattice energies are relatively low, and may have some problems during device fabrication processes. Even so, La_2O_3 film was reported to show pretty good characteristics. According to the literature [20], no interfacial silicate layer or mobility degradation was observed. The dielectric constant was 20-30. Another merit of the La_2O_3 insulator is that no micro-crystal formation was found even after high temperature processing.

In this chapter, the preliminary characteristics of La_2O_3 and Pr_2O_3 thin films were investigated for the high-k gate insulator applications. The films used in this study were deposited by e-beam deposition method. Basic electrical properties of La_2O_3 and Pr_2O_3 gate dielectrics wre presented.

2.2 Experiment（Ⅰ）

In this chapter, Al/ La_2O_3/p-Si capacitors were fabricated. 4-in p-type (100)-oriented wafers were first cleaned by standard RCA clean. Then, samples were divided into two groups. One group was processed without any surface treatment before the deposition of La_2O_3 films, while the other group received a surface

treatment before the La_2O_3 films deposition. The surface treatment was performed in a rapid thermal oxidation (RTO) system at 800°C for 3 sec in pure O_2 ambient to grow an ultra thin SiO_2 layer (~10Å , measured by optical measurement system - ellisometer) on Si surface

The La_2O_3 film was then deposited by a dual e-gun system immediately. The pressure in the chamber during depositions was about $3*10^{-6}$ Torr. Film deposition rates were 0.1-1A/S. Next, the deposited films were annealed in N_2 ambient for 60 seconds by RTA (Rapid Thermal Annealing) system at temperatures ranging between 600—800°C. Then, aluminum electrodes with a thickness of 500 nm were deposited on the gate dielectrics by a thermal coater. The gate of the capacitors were patterned and defined by RIE with Cl_2/BCl_2 mixture. Finally, aluminum electrodes with a thickness of 500 nm were deposited on the backside of the wafer to form ohmic contacts. The gate area is $6.4x10^{-5}$ cm^2. The cross-sectional view and key experiment procedures of the structure were shown in Fig. 2-1.

2.3 Results and Discussion（Ⅰ）

2.3.1Electrical properties of La_2O_3 gate dielectrics

High frequency capacitance-voltage (C-V) characteristics of La_2O_3 films fabricated with different post deposition annealing (PDA) are shown in Fig. 2-2 and 2-3 for the control and RTO-treated samples, respectively. These C-V curves were swept from inversion to accumulation. It can be seen that RTA PDA results in drastic

improvement in the C-V curves. It is worth noting that there is no shoulder in these curves corresponding to the depletion region, which indicates that the slow interface states presented at the interface are minimal [35].

The EOT value changes with different RTA temperatures. Fig. 2-4 shows that the EOT decreases at higher RTA temperatures, suggesting that the films become denser after the high RTA temperature annealing. Fig. 2-5 represents the leakage current density for various RTA temperatures. From the results of Fig. 2-4, 2-5, we can see that the control samples have higher leakage current than the RTO-treated samples. This may be due to the higher defect numbers in the control samples. While the samples with RTO treatment have lower defect density and better interface quality. Both are helpful in eliminating the leakage current level. It is also worthy to note that EOT values are almost the same for the control and RTO samples. RTO pre-treatment therefore provides an effective method to improve e-beam-deposited La_2O_3 films without sacrificing EOT.

2.3.2 Frequency dispersion

Theoretically, capacitance-voltage measurements on MOS capacitors should not show any frequency dependence in the measuring frequency range (typically between 100Hz and 1MHz)[36, 37]. The dispersion in the accumulation region is thought to be due to parasitic series resistance. Because the doping level of the Si substrate is not

high enough, poor conductivity in the substrate can lead to the so-called series resistance effects [37,38]. Another primary source of frequency dependence is the presence of interface traps [38], which will lead to the dispersion in the depletion region. One of the requirements for gate dielectric materials, according to the semiconductor industry association roadmap (ITRS), is the absence of frequency dispersion [39], and it is therefore important to perform C-V measurements at multiple frequencies to ensure that the dispersion issue is in check.

Figures 2-6(a)-(d) show the C-V curves measured at multiple frequencies for the control samples that received various RTA PDA. There is significant frequency dispersion in the depletion and accumulation regions. With higher temperature RTA, the frequency dispersion becomes even more severe. Figs. 2-7 (a)-(d) display C-V curves measured at multiple frequencies for the RTO samples with various RTA PDA. Compared to the control samples at 600-800° RTA PDA treatment, the dispersion in the accumulation region of RTO samples is improved. We believe this is due to a smaller leakage current (which will be discussed later in this chapter), so the series-resistance effect is less significant in the RTO samples.

2.3.3 Current density as a function of temperature

The J-V characteristics as a function of temperature are shown in Fig. 2-8. It is clearly seen that in the highly negative voltage regime (i.e., between -1.4V and -2.5V),

the leakage current is only weakly dependent on the measurement temperature, suggesting that the conduction is a field emission tunneling mechanism. At lower biases, however, the current is obviously dependent on the temperature, indicating there is a transition in the conduction mechanism. By fitting with the Poole-Frenkel mechanism, the energy of the trap level Φ_B was determined to be around 0.21 eV.

2.3.4 TEM

Fig. 2-9(a) shows the TEM image of the as-deposited control sample. There is an interfacial layer about 13Å existing between La_2O_3 film and Si substrate. The TEM image of the control sample with 600 °C RTA PDA is shown in Fig. 2-9(b). For the control sample, the interfacial layer does not become thicker after the high temperature RTA treatment. This indicates that La_2O_3 gate dielectric does not react with Si substrate even under thermal treatment, which is consistent with literature report [20]. For the RTO-treated sample, shown in Fig.2-9(c), it depicts an interfacial layer with thickness about 11 Å and the thickness of the gate dielectric is 56 Å. It is worth noting that the observed interfacial layer thickness almost equals to the targeted RTO thickness. From the thickness information of TEM, the dielectric constant is calculated to be 20. This value, albeit different from the published data, is still reasonable. From all TEM samples, we can see that the interface between the high-k

film and Si-substrate is not rough, and it seems that the samples were not crystallized after 600°C RTA. From these results, La_2O_3 films indeed possess better thermal stability than HfO_2 films to be presented in Chapter 3.

2.4 Experiment (Ⅱ)

In this section, Al/TaN/ Pr_2O_3 /p-Si capacitors were fabricated. 4-in p-type (100)-oriented wafers were first cleaned by standard RCA clean. The Pr_2O_3 film was then deposited by a dual e-gun system immediately. The pressure in the chamber during depositions was about $3*10^{-6}$ Torr. The deposition rates of the films were 0.1-1A/S. The deposited films were annealed in N_2 ambient for 60 seconds by RTA (Rapid Thermal Annealing) system at the temperatures of 600—800℃. Then, TaN electrodes with a thickness of 250nm were deposited on the gate dielectrics by sputtering. Aluminum electrodes with a thickness of 500 nm were then deposited on the TaN electrode by a thermal coater. The gate of the capacitors were patterned and defined by RIE with Cl_2/BCl_2 mixture. After gate patterning, the backside of the wafer was deposited with aluminum to reduce series resistance. Samples were then split into two groups. One group was put into the furnace to receive the sintering process, while the other group deliberately skipped the skipped to study its effect. The gate area of the test capacitors was $6.4x10^{-5}$ cm^2.

2.5 Results and Discussion (Ⅱ)

2.5.1 Electrical properties of Pr_2O_3 gate dielectrics

In this section, basic electrical properties of Pr_2O_3 gate dielectrics were presented.

The high frequency capacitance-voltage (C-V) characteristics of Pr_2O_3 films with various RTA PDA and no sintering are shown in Fig. 2-10(a). These C-V curves were obtained by sweeping from inversion to accumulation. It can be seen that RTA treatment leads to significant variation of the C-V characteristics.

EOT values are certainly different for different RTA temperatures. Fig. 2-11 shows EOT as a function of RTO PDA. It can be seen that EOT decreases with increasing RTA temperature. This can be due to a denser film, or serious thermal stress on the high-k films after high temperature RTA. Both would induce larger leakage current density. This is consistent with the leakage current shown in Fig. 2-12. From our results, the high RTA treatment could reduce the EOT but it would increase the leakage current density, so a trade-off exists.

Fig.2-13 shows the hysteresis as a function of RTA temperature for samples with (square) and without (circle) sintering. It can be seen that samples with sintering show better hysteresis characteristics than those without sintering. We speculate that the traps in the high-k films are reduced after sintering.

Figs. 2-14(a) and (b) show TEM images of the samples without and with RTA treatment at 600°C. Both show interfacial layer of about 10Å. The thickness of the samples with RTA 600 °C treatment became denser but the interfacial layers do not change significantly after higher temperature RTA. From these results, Pr_2O_3 films are

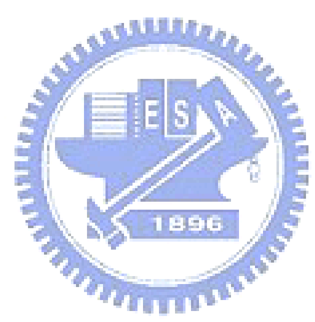
stable with Si substrate after 600°C RTA treatment. The interface between the high-k film and Si substrate is atomically sharp and the gate dielectric does not depict any apparent crystallization. This material seems to have good thermal stability as well. In addition, there is no interfacial layer between the high-k film and the TaN electrode. This is consistent with literature report that the TaN electrode is stable with high-k films [31]. Our results therefore lend support to TaN as a good electrode material for thin gate dielectrics.

2.6 Summary

In this chapter, we have explored the use of RTO pre-treatment to improve the electrical properties of La_2O_3 films. Our experimental results show that RTO pre-treatment can indeed reduce leakage current, frequency dispersion. From the TEM pictures, we confirm that La_2O_3 films have good thermal stability because the interfacial layer does not increase with higher RTA temperature. And there is no crystallization observed. RTO pre-treatment therefore appears to be conducive to better electrical characteristics of La_2O_3 films.

Pr_2O_3 gate dielectrics were also studied in this chapter. Initially, sintering process was not applied because of instrument problems. After we resolved the instrument problems, we compared the difference between samples with and without sintering process. Although the sintering process is found to reduce the hysteresis in C-V

curves, it also increases the EOT and degrades the leakage current, compared to the samples without sintering. From the TEM image, we found that the interfacial layer still does not increase easily with higher RTA temperature. This result is similar to the La_2O_3 gate dielectrics. We also found that TaN gate is stable with high-k films.



Chapter 3

Effects of Low-Temperature NH_3 Treatment on HfO_2/SiO_2 Stack Gate Dielectrics by MOCVD

3.1 Introduction

Recently, MOSFETs with high-k gate dielectrics such as La_2O_3, ZrO_2 and HfO_2 have been studied intensively [29,30,31]. However, these materials suffer from oxygen and/or dopant penetration through dielectrics due to their low crystallization temperature. Oxygen and boron atoms can readily diffuse along the grain boundaries once the dielectric is crystallized, and lead to the formation of unwanted interfacial layer and the dielectric reliability degradation, respectively. In light of this, how to increase the crystallization temperature of high-k dielectrics is one of the important issues in the material development. Among many candidates, HfO_2 seems to be the most promising because of its compatibility with the poly-silicon gate process and relatively superior scalability [31,32]. Nevertheless, the boron penetration problem still needs to be resolved. Moreover, the decrease in the accumulation capacitance as a result of charge depletion in the poly gate electrodes becomes intolerable as the gate dielectric is scaled below 10Å equivalent oxide thickness (EOT). To circumvent the poly depletion issue, it seems unavoidable to replace it with metal gate electrode.

In this chapter, TiN, which has a midgap work function, is used as the gate electrode. The main advantage of employing a midgap metal is that it results in a symmetrical V_t value for both nMOS and pMOS, because by definition the same potential barrier exists between the metal Fermi level and the conduction and valence bands of Si. This leads to a simpler CMOS processing scheme, since only one mask and one metal are required for the gate electrode (and no ion implantation step is necessary for adjusting the threshold voltage).

Recently, nitridation of the Si surface using NH_3 prior to the deposition of high-k gate dielectrics has been shown to be effective in achieving EOT value and preventing the boron penetration [31, 32]. However, this technique results in higher interface charge [34], which leads to more severe hysteresis and reduced channel mobility. Thereafter, we use the low-temperature NH_3 treatment process after the deposition of high-k gate dielectrics to incorporate nitrogen into high-k dielectrics. Compared to the methods of plasma and conventional nitridation at 600~700°C, this method can induce lesser defects and has extremely low thermal budget.

3.2 Experimental Procedure

The cross-sectional view and key experimental procedures of the test structure are shown in Fig. 3-1. Briefly, MOS capacitors were formed on 6-inch p-type Si wafers with 8~10Ω-cm nominal resistivity. Local oxidation of silicon (LOCOS) was

first performed for isolation. After standard RCA clean process, a rapid thermal oxidation (RTO) treatment was performed to grow a thin oxide layer on Si surface in a rapid thermal oxidation system at 800 °C for 3 sec in pure O_2 ambient. After RTO surface treatment, wafers were divided into three groups. Process split table of the samples are shown in Table 3-1. Samples were split to receive the low temperature NH_3 treatment at 400 °C for 5 min in the chamber. The first group, which did not NH_3 treatment, was defined as the control. The second group that received the low temperature NH_3 treatment immediately after the RTO treatment is called the bottom nitridation (BN) split. The third group that received the low temperature NH_3 treatment after the HfO_2 deposition is called the top nitridation (TN) split. The thickness of HfO_2 films was targeted at 30 nm, which was controlled by the pulse number. The deposition rate was extracted by depositing thick HfO_2 films and measuring thickness with n&k analyzer. Because the system was originally designed for 200 nm wafers, a quartz carrier was adapted so that our 150 nm wafers could be handled. All samples were then treated by rapid thermal annealing for 60 sec in N_2 ambient at various temperatures between 600~700 °C. Detailed split conditions are summarized in Table 3-1. Afterwards, a 2000 Å thick TiN metal gate was deposited by physical vapor deposition (PVD). Finally, a 500nm thick Al was deposited at wafer backside to ensure good electrical contact for measurements.

For electrical and reliability characterizations, a precision impedance meter model Agilent 4284 was used for C-V measurement and a semiconductor parameter analyzer of model Agilent 4156C was used for I-V measurement. High frequency C-V measurement was performed at 100kHz, with small ac signal of Vrms=25mv. In general, the bias voltage was swept from inversion to accumulation. Due to the high leakage current of most of these thin gate dielectrics, parallel circuit model was employed.

In this thesis, we used a program to obtain EOT (equivalent oxide thickness). NCSU CVC program was one of the popular programs in the world, which could be used to obtain precise EOT value.

3.3 Results and Discussion

In this section, we will discussion the effects of the low-temperature NH_3 treatment on the electrical properties of HfO_2 films deposited by MOCVD subjected to various RTA temperatures.

3.3.1 Electrical properties of HfO_2 gate dielectrics

3.3.1.1 C-V ＆ I-V characteristics

The effects of various post-deposition rapid thermal annealing on the high frequency capacitance-voltage (C-V) characteristics of HfO_2 films are shown in Figs.

3-2, 3-3, 3-4 for control, TN, and BN splits, respectively. These C-V curves were swept from inversion to accumulation. It can be seen that there is a shoulder in the C-V curves corresponding to the depletion region, especially for the as-deposited samples without post-deposition RTA. This shoulder suggests the presence of large amount of interface states [34]. For samples treated with RTA at 600-700°C for 60sec, the shoulder becomes much smoother. Moreover, both TN and BN treatment methods do not degrade EOT.

Fig. 3-5 displays J-V curves of the control sample with various RTA temperatures. It can be seen that higher RTA temperatures lead to higher leakage current and lower breakdown voltage. The degradation brought about by RTA is thought to be due to the crystallization of HfO_2 thin films at higher PDA temperature [49], which is supported by TEM results to be discussed later in this chapter. The results from the J-V curves are different from the results in C-V curves. Specifically, while RTA treatment at higher temperature (i.e., 600 and 700 ^{o}C) improves C-V characteristics and reduces the shoulder, it degrades leakage and breakdown characteristics.

Fig.3-6 shows the J-V characteristics of the BN samples with various RTA treatments. Again, leakage current degrades with high-temperature RTA treatment for the BN samples. The leakage currents are even higher than the control samples

annealed at high RTA temperatures (i.e., 600 and 700 °C). It is interesting to note that no occurrence of breakdown behavior was observed for the TN sample annealed at 700°C, even up to – 8V bias. The leakage degradation of BN treatment may be due to a lot of defects induced in the underneath RTO.

J-V characteristics of the TN samples are shown in Fig. 3-7. In comparison with the control and BN samples, the TN samples perform well both in the breakdown voltage and the leakage current density, and the TN sample with 700 °C RTA is better than the TN sample with 600°C RTA treatment. Remarkably, higher RTA temperature does not degrade J-V characteristics of the samples with TN treatment. It is believed that the TN treatment not only increases the crystallization temperature but also helps improve the thermal stability, which is consistent with the result in the literature [46]. TN treatment seems to be beneficial in improving the performance of HfO_2 gate dielectrics.

It was evidently observed that with nitrogen incorporation, the TN samples exhibit higher breakdown field. More importantly, the samples subject to the combination of TN and 700°C PDA exhibit the highest breakdown voltage among all samples, while those without TN display increasingly severe degradation in the breakdown voltage as the PDA temperature is increased. We hypothesize that the bond network of the HfO_2 film is strengthened by the nitrogen incorporation during

high-temperature PDA process similar to the case in SiO_2. On the other hand, the weakness caused by the high temperature annealing for the samples without TN echoes the fact that the crystallization of HfO_2 will create more grain boundaries and those boundaries can be easily broken during high field stress.

The comparison of leakage current density among the control, BN and TN samples at RTA 700°C are shown in Figs. 3-8, and 3-9 for the J-V curves and Weibull plots, respectively. The TN samples have lower leakage current and higher breakdown voltage than both the control and BN samples. Specifically, there are two orders of magnitude in leakage current reduction with respect to the control samples at –1.5V, and the improvement is even larger compared to the BN samples at –1.5V. Conspicuously, the BN treatment does not improve the characteristics of J-V curves but instead degrade the performance compared to the control samples. Obviously, this method does not serve the purpose of improving HfO_2 gate dielectric.

Our results clearly show that TN can effectively suppress the leakage increase at higher PDA temperatures because the incorporation of nitrogen can help improve thermal stability of HfO_2 and enhance the crystallization temperature [50]-[53].

Since the TN samples with high RTA temperature are superior to both the BN and control samples in terms of leakage current density and breakdown voltage. In the following discussion, we will focus on the TN and control samples.

3.3.2 Transmission electron microscopy (TEM)

The TEM images of the control samples are shown in Figs.3-10(a)-(c) for as-deposited, 600 ^{0}C RTA, and 700 ^{0}C RTA, respectively. For the sample with no RTA and 600 ^{0}C RTA, an interfacial layer of about 13.5 Å exists between the HfO_2 thin film and Si substrate. The thickness of HfO_2 films is about 30Å, which is very close to the target value. The dielectric constant is calculated to be about 12. From the results of the control samples with higher temperature RTA treatment (i.e., 600 and 700 °C), it can be seen that many crystalline grains appear in the HfO_2 gate dielectrics. Thus, HfO_2 films do not maintain amorphous phase after higher temperature RTA.

For the control samples annealed at 700°C, a thicker interfacial layer of about 17 Å is formed. This is because HfO_2 is not a good barrier against oxygen diffusion, so RTA in N_2 ambient can also cause the formation of an interfacial layer [47][48]. From the TEM picture, we can see that interfacial layers become thicker with higher RTA, and must be carefully controlled to maintain a low EOT value. The gate leakage current also has to be well controlled.

Fig. 3-10 (d) shows TN sample with 700 °C RTA treatment. A thin interfacial layer (13.6 Å) is maintained between HfO_2 and Si substrate, which is much thinner than that in the control sample with 700 ^{o}C RTA. In addition, no discernible crystalline phase is observed. The TN treatment therefore appears to be effective in

maintaining the desirable physical properties of the high-k films. From all TEM results, we can see that the interface between the HfO_2 film and Si substrate or TiN electrode is very sharp. This reveals that the HfO_2 films deposited by MOCVD do have good quality and smoothness.

3.3.3 Frequency dispersion

C-V curves measured at multiple frequencies of the control samples are presented in Figs.3-11(a)-(c) for as-deposited, 600 ^{0}C RTA, and 700 ^{0}C RTA, respectively. Frequency dispersion of accumulation capacitance was measured at –1V to avoid errors due to the leakage current. From Fig.3-11(a), there is significant frequency dispersion in the depletion region which is indicative of the presence of large amount of interface states [38]. The frequency dispersion in the depletion region decreases for samples with higher RTA temperature (i.e., 600°C, 700°C), because high-temperature RTA could reduce the interface state density. However, the dispersion in the accumulation region becomes larger at higher RTA temperatures. It might be attributed to the higher leakage current density after annealing at higher RTA temperatures which would lead to worse series-resistance effects [36,37]. From the results in Figs. 3-11(a)-(c), it can be found that higher temperature RTA helps reduce the interface states and the C-V curves become smoother.

Figs. 3-12 (a)-(c) show the C-V curves measured at multiple frequencies of the TN samples for as-deposited, 600 ^{0}C RTA, and 700 ^{0}C RTA, respectively. Significant frequency dispersion still exists in the depletion region of the as-deposited sample without RTA treatment. After high-temperature RTA, the frequency dispersion becomes much less. Compared to the control samples annealed at 600 and 700°C, the dispersion in the accumulation region of TN samples is reduced. This is because the leakage current density of the TN samples is smaller than the control samples, so the series-resistance effects are less effective [36]. So the TN treatment results in moderate improvement in frequency dispersion.

3.3.4 Reliability characteristics

Fig.3-13 shows the Weibull plots of dielectric breakdown field for the control samples with various RTA treatments. The dielectric breakdown field improves after 600 ^{0}C RTA treatment over the as-deposited sample. However it degrades from 20 MV/cm observed on the control to 16 (MV/cm). This can be explained by the film crystallization at higher RTA temperatures discussed previously. So too high a temperature RTA is detrimental to the reliability of the gate dielectric. The phase of gate dielectrics may change from amorphous to crystalline.

Fig. 3-14 presents the Weibull plots of breakdown field for the TN samples with

various RTA treatments. The breakdown field of the TN samples improves, rather than degrades, with increasing RTA temperature. The average breakdown field is over 20 MV/cm for those with the 700°C RTA treatment. This is because TN treatment increases thermal stability and therefore breakdown field. From the Weibull plot, the distributions of the control samples and TN samples are extremely tight. This reveals that the uniformity does not degrade after TN treatment. The good uniformity of these two samples indicates that the MOCVD system has good uniformity.

Stress induced leakage current (SILC) is an important concern in scaling gate oxide thickness, because it can decrease DRAM refresh times, EEPROM data retention, and MOSFET off-state power dissipation. SILC is mainly cause by the trap assisted tunneling effect, and trap generation rate is an index of estimation for SILC. The SILC results of control and TN samples under constant field (15.8MV/cm) stressing are shown in Figs. 3-15(a)-(c), and 3-16(a)-(c) for as-deposited, 600 ^{0}C RTA, 700 ^{0}C RTA, respectively. All samples were stressed under constant field and the J-V curves were monitored at different stressing interval. For the control samples, gate current increases dramatically after stress. This phenomenon becomes more severe after high-temperature RTA treatment. From the results shown in Figs. 3-16(a)-(c) for the TN samples, SILC is not greatly reduced over the control samples, even after high-temperature RTA treatment. This indicates that TN treatment can reduce the traps

generated during the stress, as the nitrogen incorporated in the films serves to repair the traps. In order to evaluate the results, we plot the trap generation rates ((J-Jo)/Jo) % (J at Vg=-1V) as a function of stress time for the control and TN samples with various RTA treatments. As shown in Fig. 3-17, the control samples suffer severe SILC issues. With TN treatment, however, the samples show much reduced stress induced leakage current (SILC) behavior.

As discussed in previous session, TN samples show higher breakdown field, crystalline retardation feature, and reduced leakage current while maintaining the same equivalent oxide thickness. In order to investigate the charge trapping properties, constant-voltage stressing was performed on the control and TN samples, and the results are shown in Figs. 3-18(a)-(c), and 3-19(a)-(c). It can be seen that all high-frequency C-V curves shift to the left after stress, indicating that positive charges are being generated in the gate dielectrics. Flatband voltage shift is defined as $\Delta V_{FB} = V_{FB1} - V_{FB2}$, where V_{FB1} is the flatband voltage prior to stress, V_{FB2} is the flatband voltage after stress. From the results of Figs. 3-18(a)-(c), and 3-19(a)-(c), the TN samples also show better reliability against stress, because TN samples depict less flatband shift than the control samples after different stress times, due again to better thermal stability as discussed previously.

From the discussion in Chapter 1, high-k films have to possess good thermal

stability, which means that the gate leakage shall not increase significantly after high temperature annealing. The J-V curves as a function of temperature are shown in Fig. 3-20(a)-(c), and 3-21(a)-(c). The control samples depict severe temperature effect and the effect becomes more severe after high-temperature RTA. Compared to the control samples, the TN samples have negligible temperature effect even with high-temperature RTA. This suggests that there are fewer traps in the TN samples, so the leakage mechanism is not dominated by Frenkel-Pool mechanism that is temperature dependent.

3.3.5 Summary

In this chapter, we have investigated the electrical characteristics of the low-temperature (i.e., 400 ^{0}C) NH_3 treatment with various RTA temperatures in terms of leakage current density, breakdown field and reliability. The low-temperature NH_3 (400°C) treatment could reduce the thermal budge compared to the conventional nitridation at higher temperatures (600~700°C).

Two low-temperature nitridation methods were used on HfO_2 gate dielectrics. The bottom nitridation (BN) samples did not show improvement on electrical properties. In contrast, the top nitridation (TN) method in which the low-temperature nitridation was performed after HfO_2 deposition could improve the electrical properties, thermal stability. In addition, trap density, temperature effect, SILC and

reliability were also improved compared to the BN and control samples. Therefore, TN method appears to be a promising technique to further improve the dielectric properties of high-k films.

Chapter 4

Conclusions and Suggestions for Future Work

4.1 Conclusions

In this thesis, electrical characteristics of La_2O_3, Pr_2O_3 and HfO_2 gate dielectrics have been investigated.

Firstly, La_2O_3 gate dielectrics were fabricated by PVD method using e-gun system. Samples with RTO pre-treatment and rapid thermal annealing have been investigated. Our experimental results show that samples with RTO pre-treatment have better performance than the control samples. Although our experimental results are still far from satisfactory, it did give us some basic characteristics of La_2O_3 gate dielectrics. And our results show that the RTO pre-treatment is very important to make better La_2O_3 gate dielectrics.

From the results of Pr_2O_3 gate dielectrics, this high-k material could be scaled down to about 15Å and the leakage current density is very small compared to SiO_2. Sintering was performed to reduce hysteresis of Pr_2O_3 gate dielectric. Our results show that sintering could reduce hysteresis dramatically, however, the films show increased EOT and leakage current. It appears therefore that there is still much work

that need to be done to overcome these drawbacks. Despite its infancy and scarcity in data, Pr_2O_3 gate dielectric still seems to be quite promising.

Finally, a new low-temperature (~ 400℃) NH_3 treatment on the characteristics of HfO_2/SiO_2 gate stack with TiN gate electrode were studied in this work. HfO_2 films were deposited using AIXTRON Tricent® MOCVD system. The effective electrical oxide thickness (EOT) for the samples with low temperature NH_3 treatment under various ambient RTA processes is investigated. It was clearly observed that the distortion occurred in C-V curves can be significantly suppressed with higher PDA temperatures and low-temperature NH_3 treatment can help alleviate the distortion at lower temperature range. Compared to control samples at higher RTA temperature, the samples with TN treatment reveal excellent characteristics on the aspects of leakage current density, breakdown field, SILC, and thermal stability.

The low-temperature NH_3 treatment can significantly reduces the trap generation rate as compared to the samples without the treatment. Specifically, the sample with higher temperature PDA (700°C) still exhibits extremely low trap generation rate, which means that the low-temperature NH_3 treatment can dramatically improve the thermal stability of thin HfO_2 film.

4.1 Future Work

In this work, we have fabricated MOS capacitors with La_2O_3 and Pr_2O_3 gate dielectrics. In the future, more efforts should be paid on studying and finding out other treatment methods that could improve the electrical properties.

For the low-temperature NH_3 treatment on HfO_2 films, it seems to be an effective method to improve HfO_2 films. This work can be extended to MOSFETs to investigate electrical characteristics such mobility, subthreshold swing.

References

[1] H. Iwai," Ultra thin gate oxides-Performance and reliability," in IEDM Tech. Dig., 1998, pp. 163-166

[2] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, " Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide MOSFETs," IEEE Electron Device Lett., vol. 18, pp. 206-209, May 1997.

[3] H. Iwai, " Downsizing of silicon MOSFETs beyond 0.1 μ m,"Microelectron. J., vol.29, pp. 671-678, Apr. 1998.

[4] B. Yu, H. Wang, C. Ricobene, Q. Xiang, and M.R. Lin," Limits of gate oxide scaling in nano-transistors," in VLSI Tech. Dig., 2000, pp.39-40.

[5] S. A. Campbell, D. C. Gilmer, X. C. Wang, H. S. Kim, and J. Yan," MOS transistors fabricated with high permittivity TiO dielectrics,"*IEEE Trans. Electron Devices*, vol. 44, pp. 104–109, May 1997.

[6] W. J. Qi, R. Nieh, B. H. Lee, K. Onishi, and L. Kang, "Performance of MOSFETs with ultra-thin ZrO and Zr silicate gate dielectrics," in *VLSI Tech. Dig.*, 2000, pp. 15–16.

[7] A. Chin, Y. H.Wu, S. B. Chen, C. C. Lias, andW. J. Chen, "High quality La_2O_3 and Al $_2O_3$ gate dielectrics with equivalent oxide thickness 5–10A," in *VLSI Tech. Dig.*, 2000, pp. 13–14.

[8] B. Cheng, M. Cao, R. Rao, A. Inani, P. V. Voorde, W. M. Greene, J. M.C. Stork, Z. Yu, P. Zeitzoff, and J. C. S. Woo, “The impact of high-K gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs,” *IEEE Trans. Electron Devices*, vol. 46, pp. 1537–1544, July 1999.

[9] B.Cheng et al, “The impact of high-/spl kappa/ gate dielectrics and metal gate electrodes on sub-100nm MOSFETs”, IEEE Tran. Electron Device, 46, 1537, (1999).

[10] G. D. Wilk, R. M. Wallace, J. M. Anthony, “High-K gate dielectrics:Current status and materials properties considerations,” Journal of Applied Physics, vol. 89, no. 10, pp. 5243, 33p, 05/15/2001.

[11] H.- S. P.Wong, “Beyond the conventional transistor.;” IBM Journal of Research ＆ Development, vol. 46, no. 2/3, pp. 133, Mar/May2002.

[12] P. K. Roy and I. C. Kizilyalli, “Stacked high-k gate dielectric for gigascale integration of metal-oxide-semiconductor technologies” Applied Physics Letters —June 1, 1998—Volume 72, Issue 22, pp.2835-2837.

[13] Jack C.Lee, “Ultra-thin gate dielectrics and high-?dielectrics.”, IEEE EDS vanguard series of independent short courses.

[14] H.S. Nalwa, “Handbook of low and high dielectric constant materials and their applications.”, Academic Press 1999.

[15] L. Manchanda, M. L. Green, R. B. van Dover, M. D. Morris, A. Kerber, Y. Hu, J.-P. Han, P. J. Silverman, T. W. Sorsch, G. Weber, V. Donnelly, K. Pelhos, F. Klemens, N. A. Ciampa, A. Kornblit, Y. O. Kim, J. E. Bower, D. Barr, D. Barr, E. Ferry, D. Jacobson, J. Eng, B. Busch and H. Schulte, "Si-doped aluminates for high temperature metal-gate CMOS: Zr-Al-Si-O, a Novel gate dielectric for low power applications", IEDM Tech. Dig.,pp.23-26(2000).

[16] C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "MOS characteristics of ultra thin rapid thermal CVD ZrO_2 AND Zr silicate gate dielectrics", IEDM Tech. Dig., pp.27-30 (20000).

[17] S. J. Lee, H. F. Luan, W. P. Bai, C. H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "High quality ultra thin CVD HfO_2 gate stack with poly-Si gate electrode", IEDM Tech. Dig., pp.31-34 (2000)

[18] L. Kang, K. Onishi, Y. Jeon, B. H. Lee, C. Kang, W.-J. Qi, R. Nieh, S.r Gopalan, R. Choi, and J. C. Lee, " MOSFET devices with polysilicon on single-layer HfO_2 high-k dielectrics", IEDM Tech. Dig., pp.35-38 (2000)

[19] B. H. Lee, R. Choi, L Kang, S. Gopalan, R. Nieh, K. Onishi, Y. Jeon, W.-J. Qi, C. KANG AND j. c. Lee, "characteristics of TaN gate MOSFET with ultrathin hafnium oxide(8A-12 A)", IEDM Tech. Dig., pp.39-42 (2000)

[20] A. Chin, Y. H.Wu, S. B. Chen, C. C. Lias, andW. J. Chen, "High quality La_2O_3

and Al $_2O_3$ gate dielectrics with equivalent oxide thickness 5–10A," in *VLSI Tech. Dig.*, 2000, pp. 13–14.

[21] H.J. Osten, J.P. Liu, P. Gaworzewski, E. Bugiel, ND p. Zaumseil, "Hgh-k gate dielectrics with ultra-low leakage current based on praseodymium oxide", IEDM Tech. Dig., pp. 653-656 (2000).

[22] J. A. Gupta, D. Landheer, J. P. McCaffrey, and G. I. Sproule, "Gadolinium silicate gate dielectric films with sub-1.5nm equivalent oxide thickness", Appl. Phys. Lett., 78,pp. 1718-1720 (2001)

[23] S. Jeon, K. Im, H. Yang, H. Lee, H. Sim, S. Choi, T. Jang, and H. Hwang., "Excellent Electrical characteristics of Lanthanide (Pr, Nd, Sm, Gd, and Dy)) oxide and Lanthanide-doped Oxide for MOS Gate Dielectric Applications", IEDM Tech. Dig.,pp471-471 (2001)

[24] J. R. Hauser, " Gate Dielectrics for Sub-100 nm CMOS", IEDM Short Course on Sub-100nm CMOS (1999).

[25] R. D. Shannon, "Dielectrics polarization of ions in oxides and fluorides", J. Appl. Phys., 73, pp.348-366 (1993)

[26] K. J. Hubbard and D. G. Schlom, " Thermodynamic stability of binary oxides in contact with silicon", J. Mater. Res.,, 11, pp. 2757-2776 (1996)

[27] R. D. Shannon, M. A. Subramanian, T. H. Allik, H. Kimura, M. R. Kokta, M. H.

Randles, and G. R. Rossman, “Dielectric constants of yttrium and rare-earth garnets, the polarizability of gallium oxide, and the oxide additivity rule”, J. Appl. Phys., 67, pp.3798-3802 (1990).

[28] D Xue, K Betzler and H Hesse, “ Dielectric constants of binary rare-earth compounds”, J. Phys.: Condens. Matter, 12, pp. 3113-3118 (2000).

[29] B. H. Lee et al., “MOSCAP and MOSFET characteristics using ZrO_2 gate dielectric deposited directly on Si”, IEDM Tech. Dig., p. 133, 1999.

[30] B. H. Lee et al., “Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8-12 A)”, IEDM Tech. Dig., p. 39, 2000.

[31] R. Choi et, “High-quality Ultra-thin HfO_2 Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation, “ Symp VLSI tech., 2001, p. 15.

[32] K. Onishi et al., “Dopant Penetration Effects on Polysilicon Gate HfO_2 MOSFET’S “, VLSI Tech. Dig.p.131, 2001.

[33] H.-J. Cho, D-G. Park, et al., “ Characteristics of TaOxNy Gate Dielectric with Improved Thermal Stability”, Jpn. J. Appl. Phys. Vol. 40, p. 2814, 2001.

[34] M. O. Andersson, P. Lundgren, O. Engstrom, and K. R. Farmer, Microelectron. Eng. 22, 235 (1993).

[35] S. M. Sze, Physics of Semiconductor Devices (Wiley, New York, 1981).

[36] E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and

Technology (Wiley, New York, 1982).

[37] S. Y. Hou, J. Kwo, R. K. Watts, J. Y. Cheng, and D. K. Fork, Appl. Phys. Lett. 67, 1387 (1995).

[38] V. K. Bhat, K. N. Bhat, and A. Subhramanyam, J. Electron. Mater. 29, 399 (2000).

[39] The International Technology Roadmap for Semiconductors (Semiconductor Industry Association, Texas 1999).

[40] G. D. Wilk, R. M. Wallance, and J. M. Anthony, J. Appl. Phys. 89, 5243 (2001).

[41] W. J. Qi, R. Nieh, B. H. Lee, L. G. Kang, Y. Jeon, and J. C. Lee, Appl. Phys. Lett. 77, 3269 (2000).

[42] M. Houssa, R. Degraeve, P. W. Mertens, M. M. Heyns, J. S. Jeon, A. Halliyal, and B. Ogle, J. Appl. Phys. 86, 6462 (1999).

[43] J. A. Gupta, D. Landheer, J. P. McCaffrey, and G. I. Sproule, Appl. Phys. Lett. 78, 1718 (2001).

[44] M. Copel, E. Cartier, and F. M. Ross, Appl. Phys. Lett. 78, 1607 (2001).

[45] K. Kukli, K. Forsgren, M. Ritala, M. Leskela, J. Aarik, and A. Harsta, “Dielectric properties of zirconium oxide grown by atomic layer deposition from idodide precursor,” Jj. Electrochem. Soc., vol 148, pp. F227-F232, 2001.

[46] H. –J, C. S. Kang, K. Onishi et al, IEDM Tech. Dig., p. 665, 2001.

[47] M. Copel et al., APL 76, 436 (2000)

[48] B. H. et al., APL 76, 1926 (2000)

[49] L. Kang, K. Onishi, Y. Jeon, B. H. Lee, C. Kang, W.-J. Qi, R. Nieh, S. Gopalan, R. Choi, and Jack C. Lee, *Tech. Dig. – Int. Electron Devices Meet*, 39 (2000)..

[50] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi and A. Nishiyama, *Tech. Dig. – Int. Electron Devices Meet*, 849 (2002).

[51] H.-J. Cho, C. Y. Kang, C. S. Kang, R. Choi, Y. H. Kim, M. S. Akbar, C. H. Choi, S. J. Rhee, and J. C. Lee, *IEEE Semiconductor Device Research Symposium*, 68 (2003).

[52] Y. Morisaki, T. Aoyama, Y. Sugita, K. Irino, T. Sugii, and T. Nakamura, *Tech. Dig. – Int. Electron Devices Meet*, 861 (2002).

[53] M. Koyama, K. Suguro, M. Yoshiki, Y. Kamimuta, M. Koike, M. Ohse, C. Hongo, and A. Nishiyama, *Tech. Dig. – Int. Electron Devices Meet*, 459 (2001).

Material Requirement of High-k Gate Dielectrics

Criteria	Requirements
EOT scalability <10Å	**Dielectric constant > 15**
Negligible FIBL effect	**Dielectric constant < 60**
Leakage current < 1 A/cm^2	**Bandgap > 5 eV** **Barrier height > 1 eV**
Thermal stability	**No silicidation and reduction**
Hysteresis	**< 20 mv**
Dispersion	**< 1 %/decade**
Interface state density	**< 10^{11} /eV cm^2**
Mobility	**> 85 % of SiO_2**
Reliability	**> 10 years**

Table.1-1 Criteria and requirements for high-k dielectric materials to be used as gate dielectric.[4]

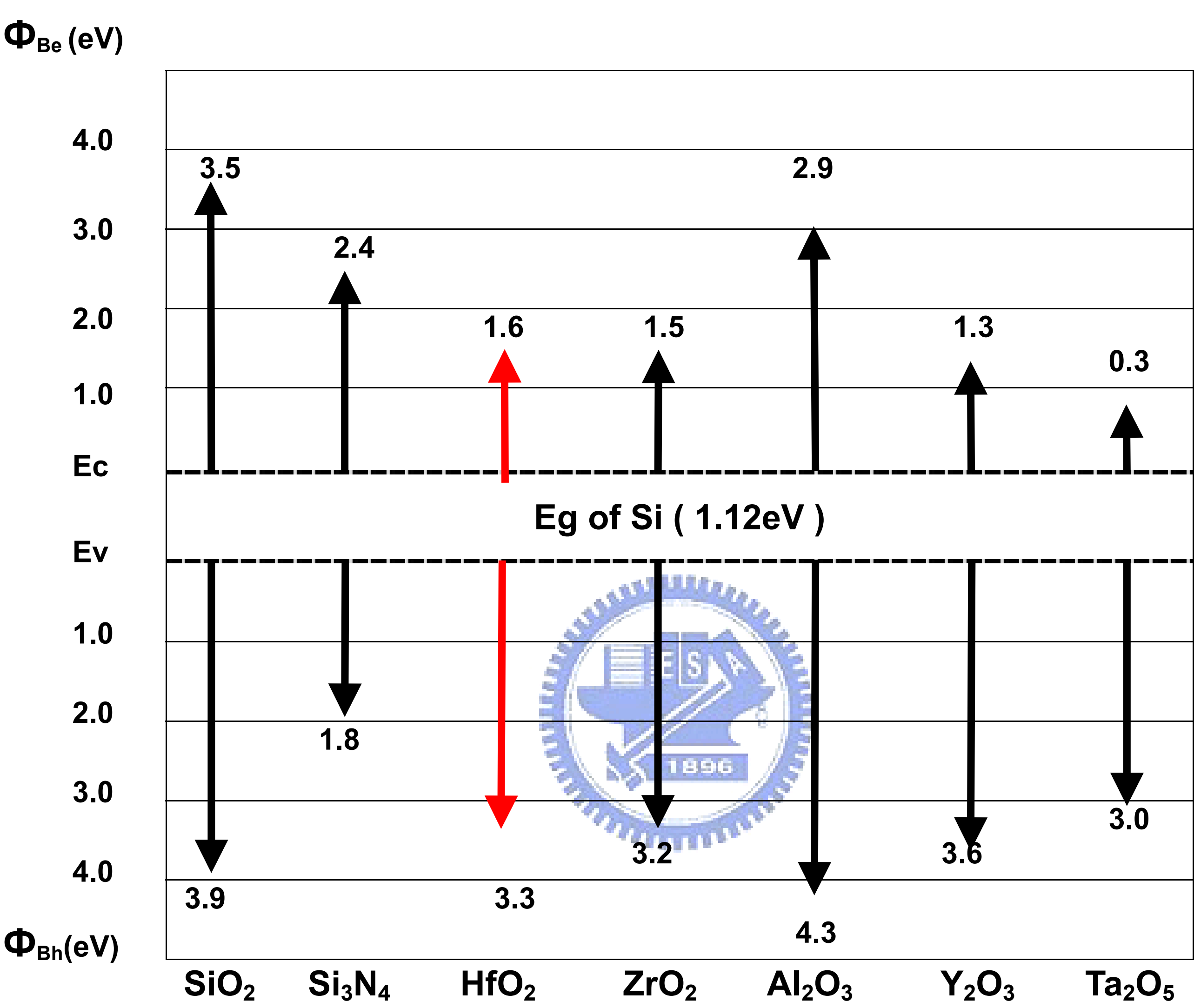


Fig 1-1 Bandgaps of some well-known high-k materials [4]

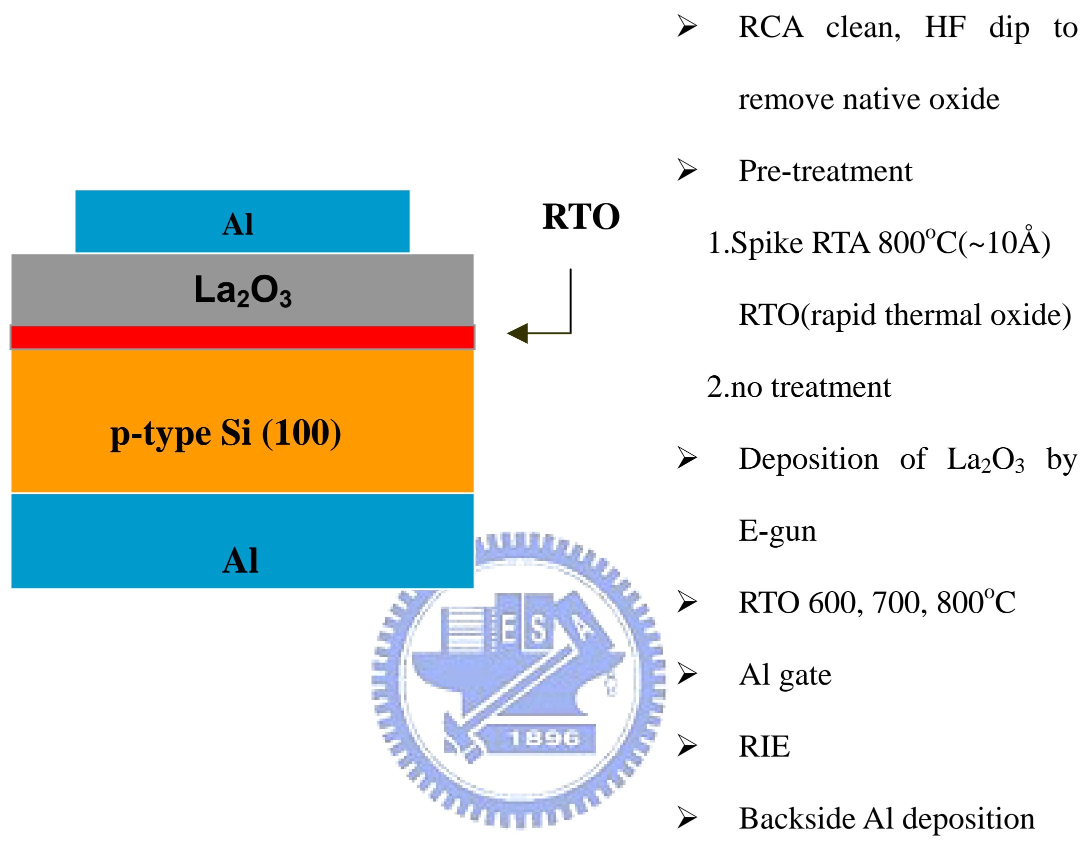


Fig.2-1. Cross-sectional view and key experimental procedures of the test structure.

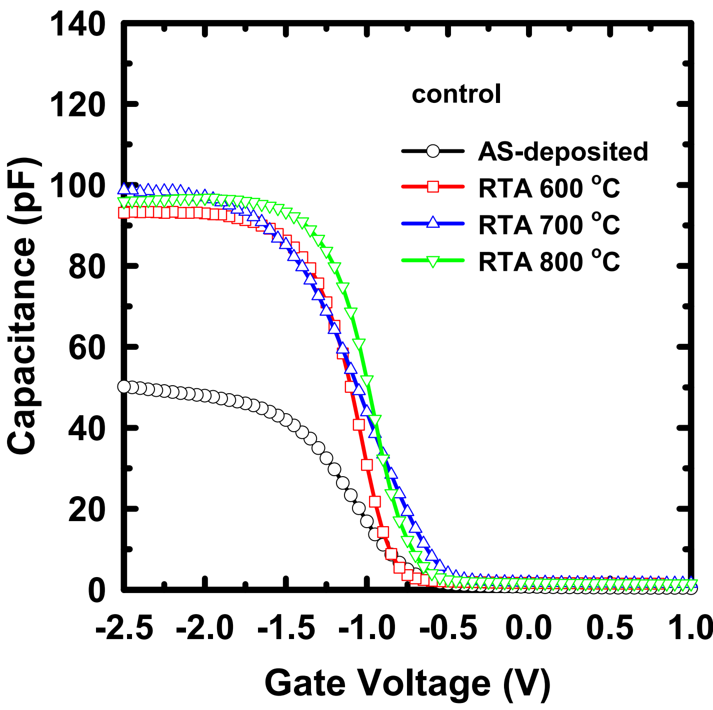


Fig.2-2. C-V characteristics of La_2O_3 films fabricated with different PDA for control samples.

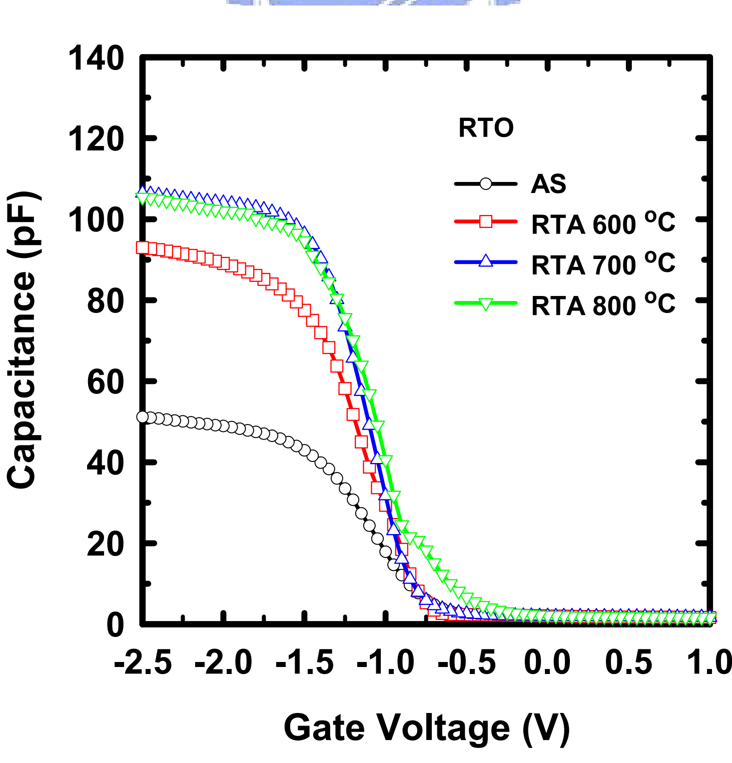


Fig.2-3. C-V characteristics of La_2O_3 films fabricated with different PDA for RTO-treated samples.

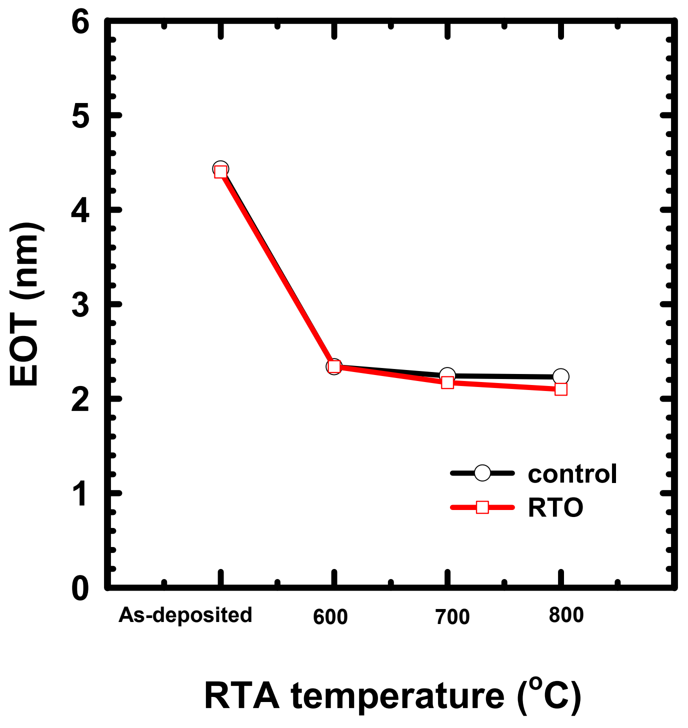


Fig.2-4. EOT for various RTA temperatures.

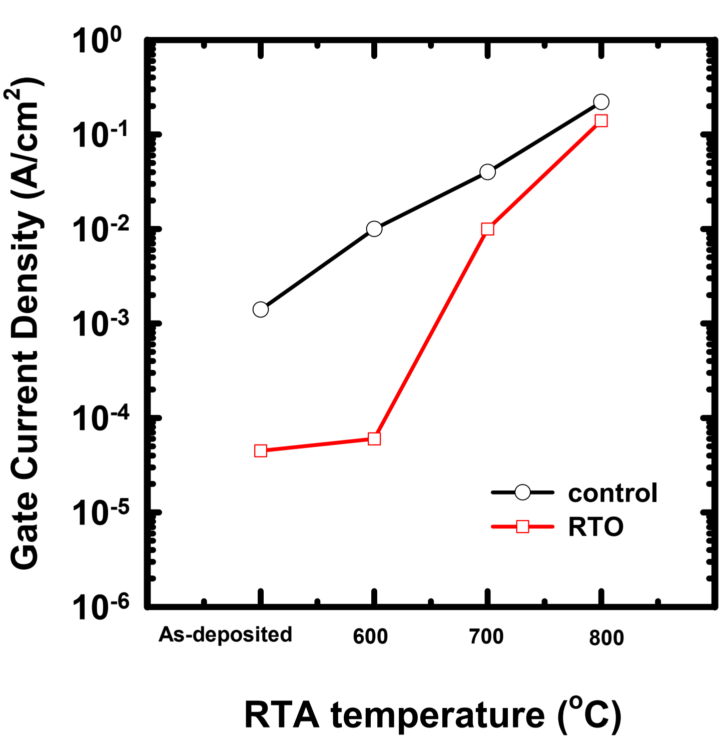


Fig.2-5. Leakage current density for various RTA temperatures.

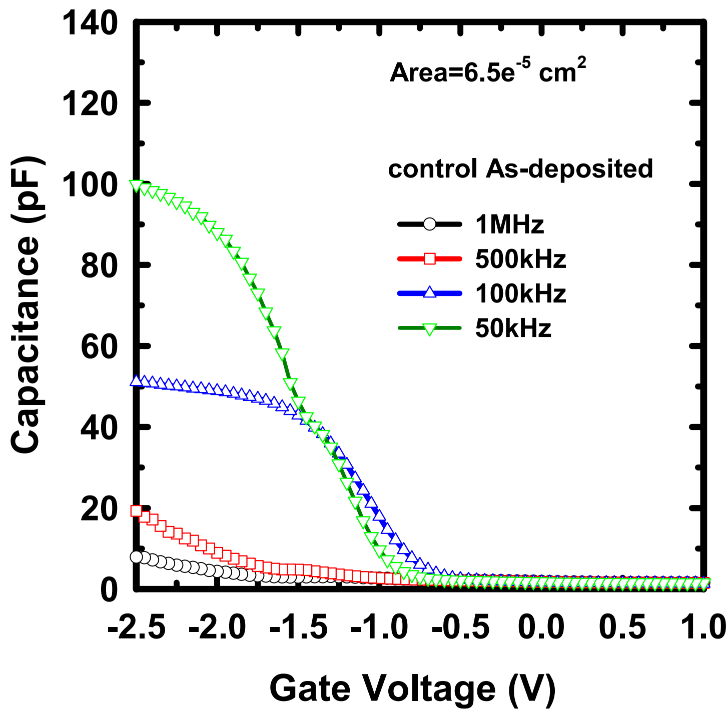


Fig.2-6(a) C-V curves measured at multiple frequencies for control samples without RTA.

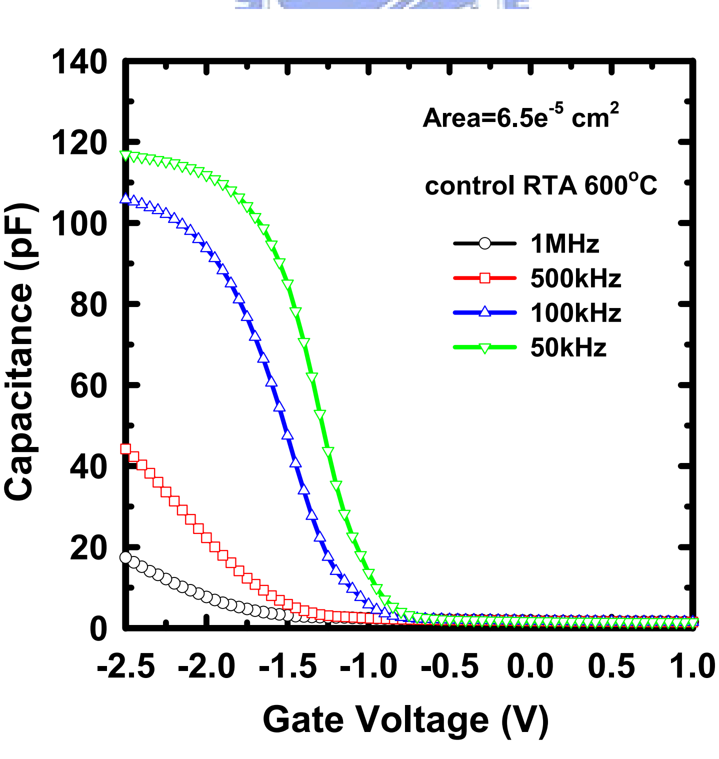


Fig.2-6(b) C-V curves measured at multiple frequencies for control samples with 600°C RTA.

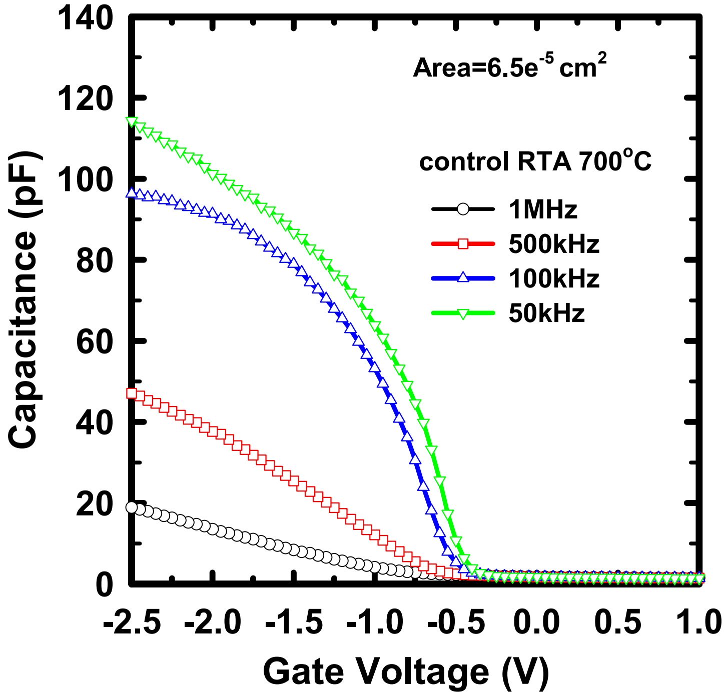


Fig.2-6(c) C-V curves measured at multiple frequencies for control samples with 700℃ RTA.

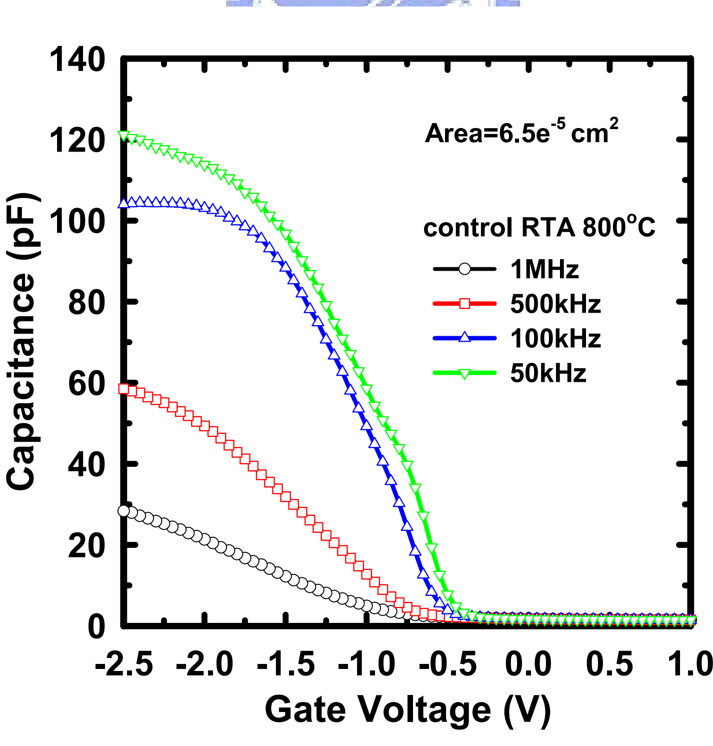


Fig.2-6(d) C-V curves measured at multiple frequencies for control samples with 800℃ RTA.

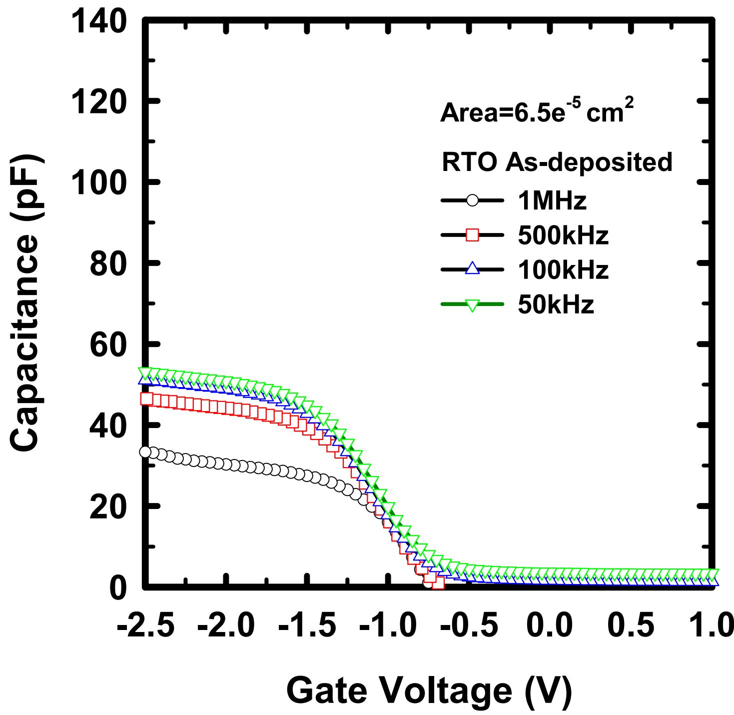


Fig.2-7.(a) C-V curves measured at multiple frequencies for RTO samples without RTA .

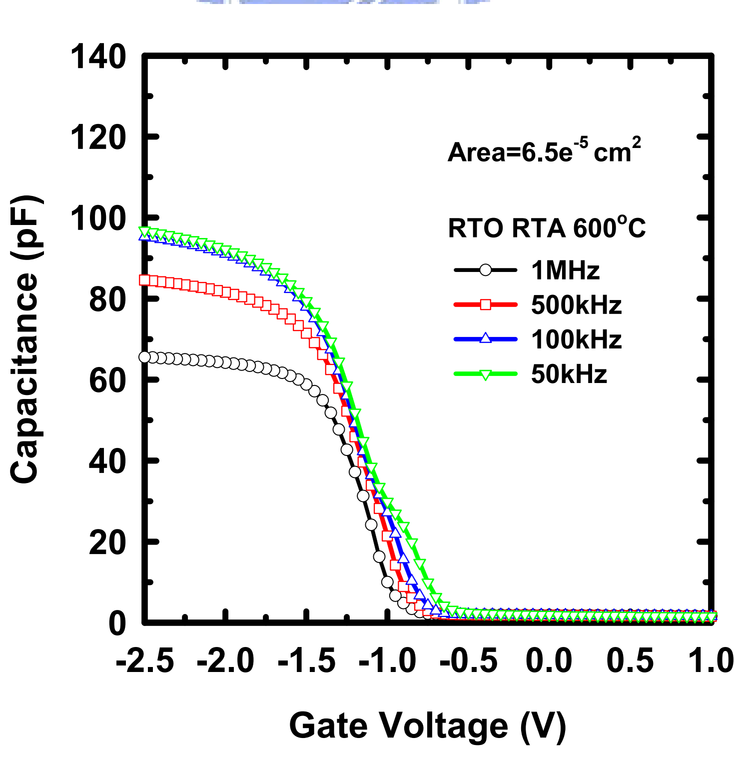


Fig.2-7(b) C-V curves measured at multiple frequencies for RTO samples with 600°C RTA.

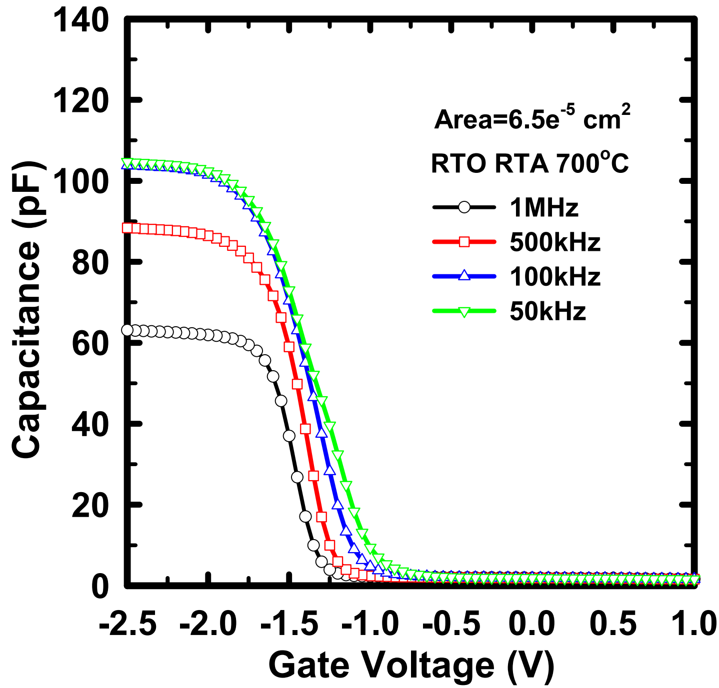


Fig.2-7(c) C-V curves measured at multiple frequencies for RTO samples with 700°C RTA.

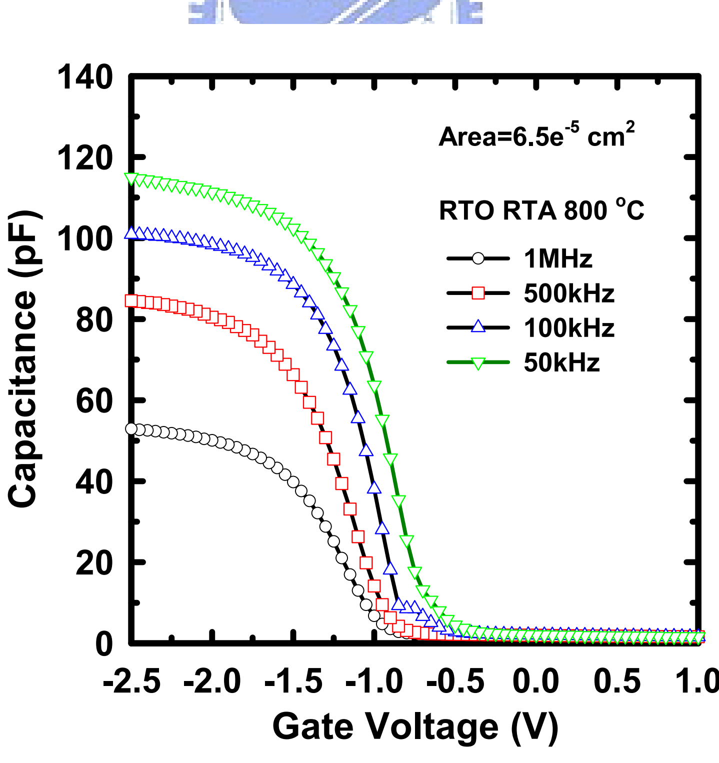


Fig.2-7(d) C-V curves measured at multiple frequencies for RTO samples with 800°C RTA.

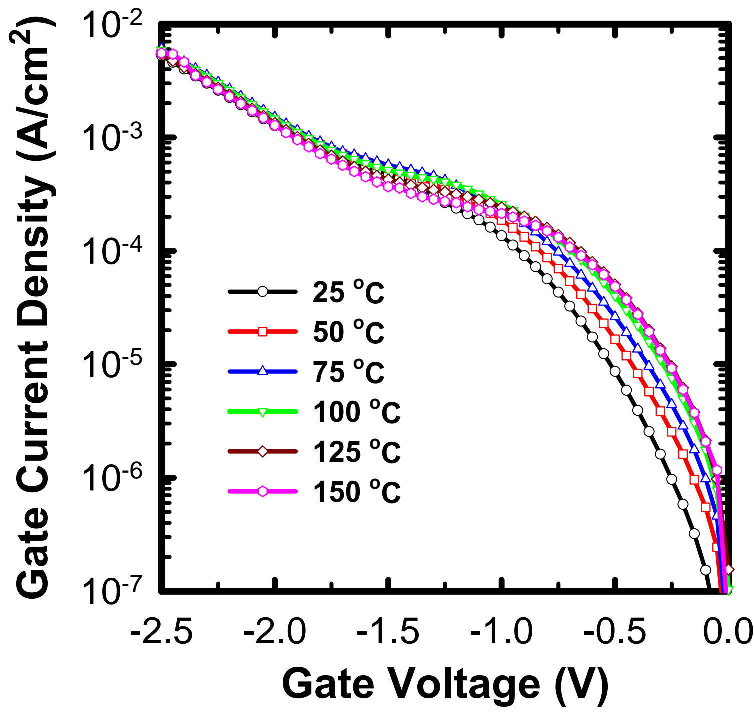


Fig.2-8(a) J-V characteristics as a function of temperature.

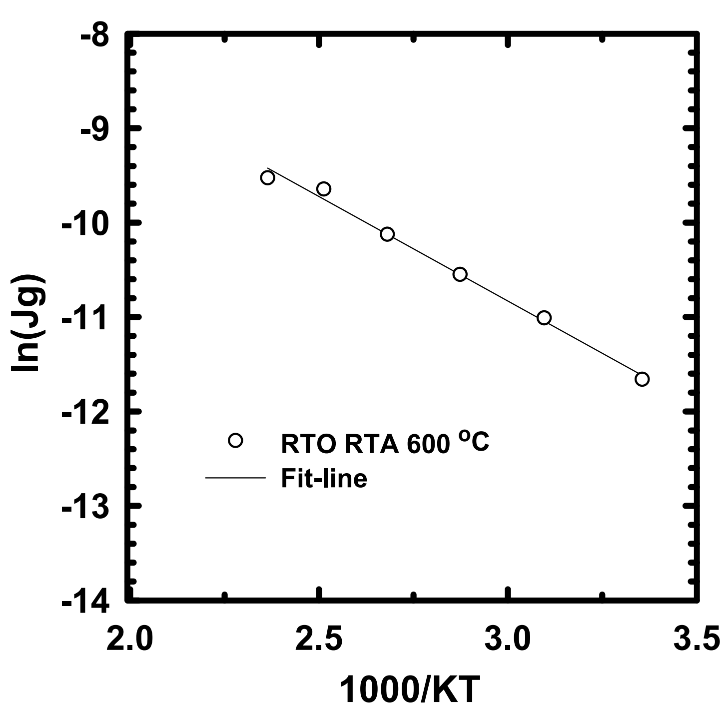


Fig.2-8(b) Leakage current at –0.5V plotted as a functionof inverse temperature, the solid line is a fit to the experimental data.

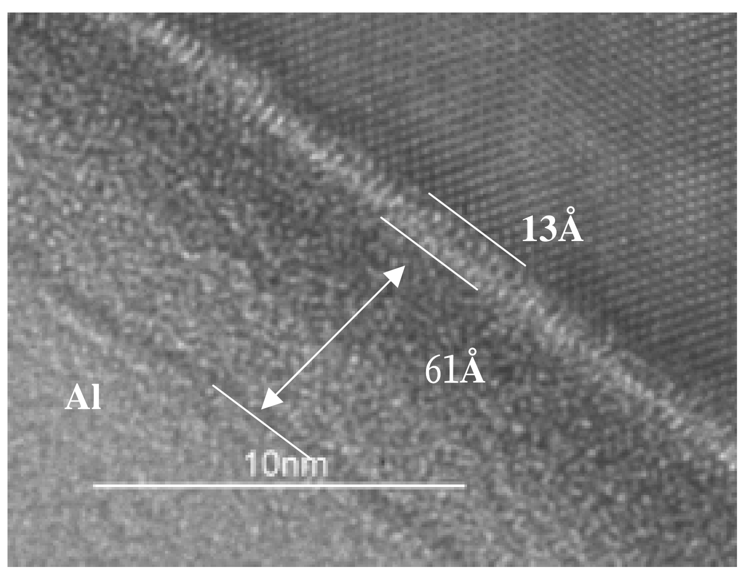


Fig.2-9 (a)TEM image of control sample without RTA treatment.

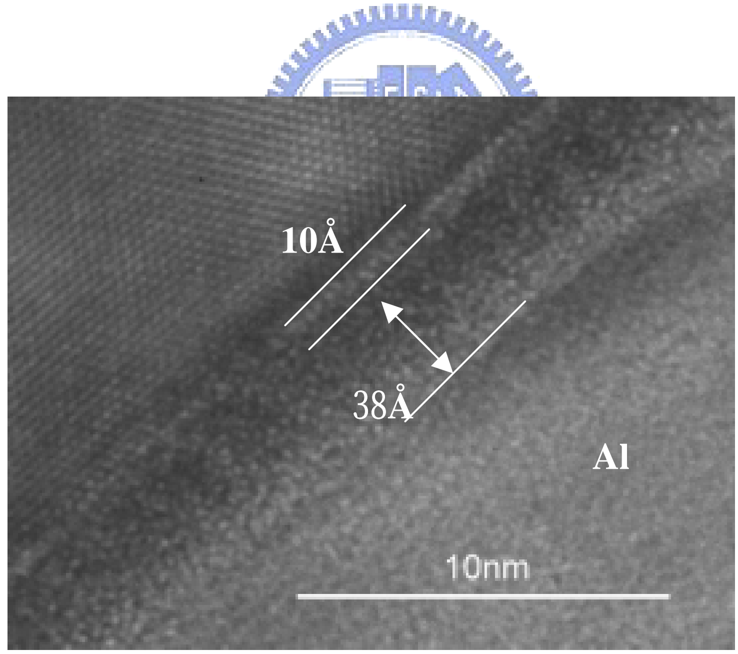


Fig.2-9(b). TEM image of control sample with 600°C RTA.

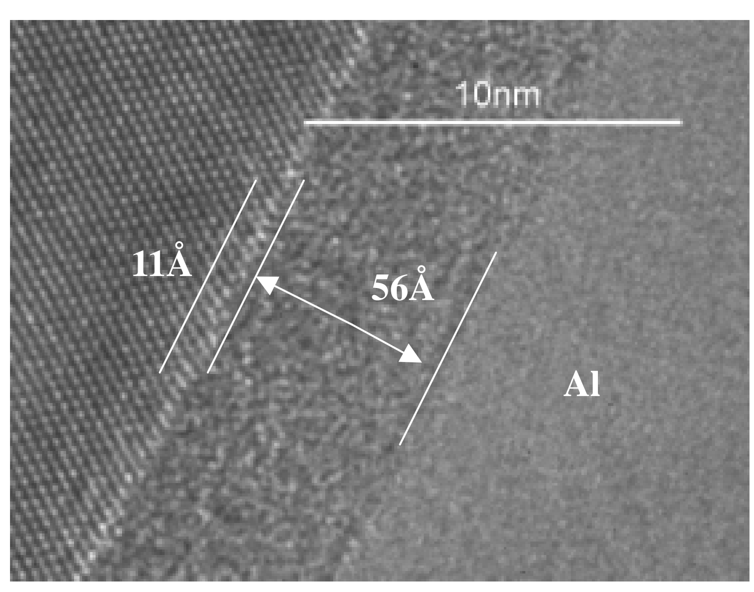


Fig.2-9 (c). TEM image of RTO sample with 600°C RTA.

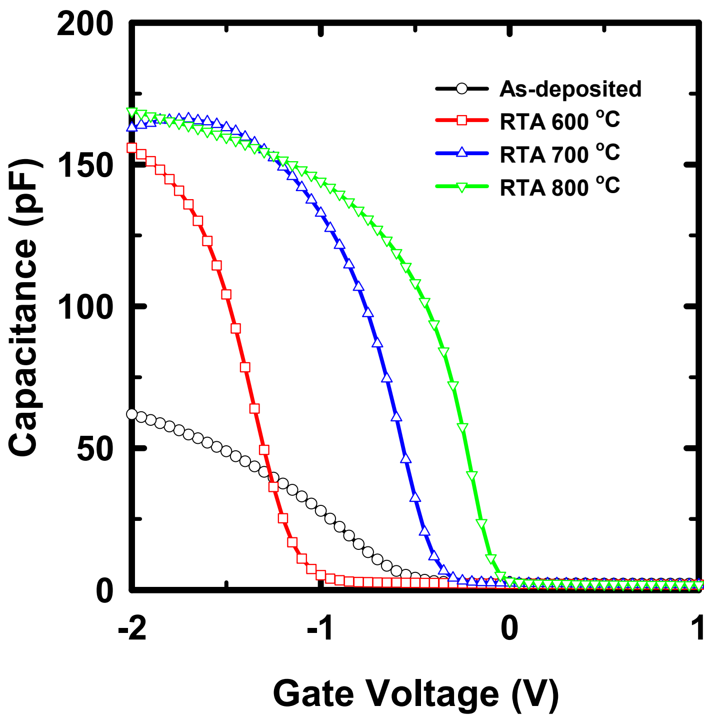


Fig.2-10(a) C-V characteristics of Pr_2O_3 films with various RTA PDA and no sintering.

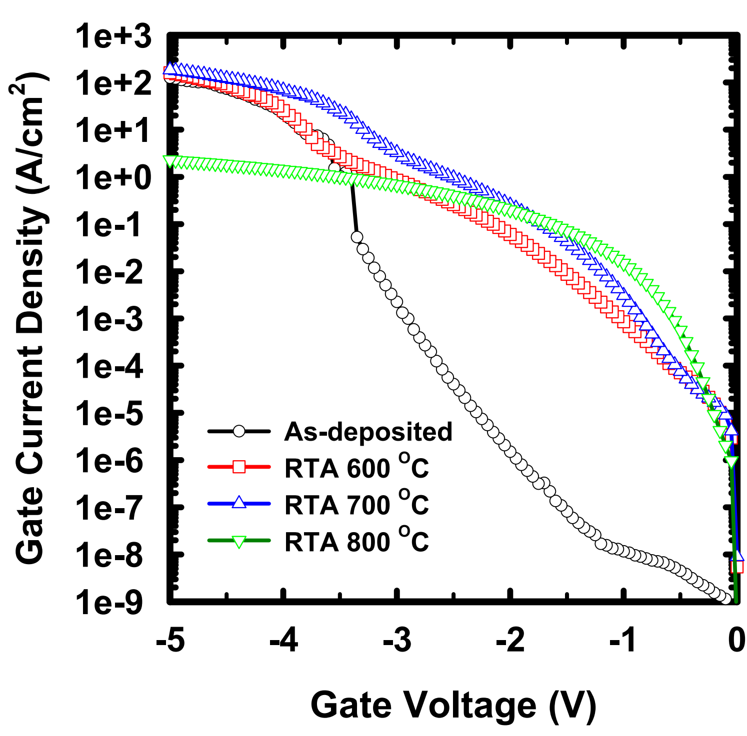


Fig. 2-10(b): Gate current density vs. gate voltage. The plot shows J-V characteristics of Pr_2O_3 gate dielectrics.

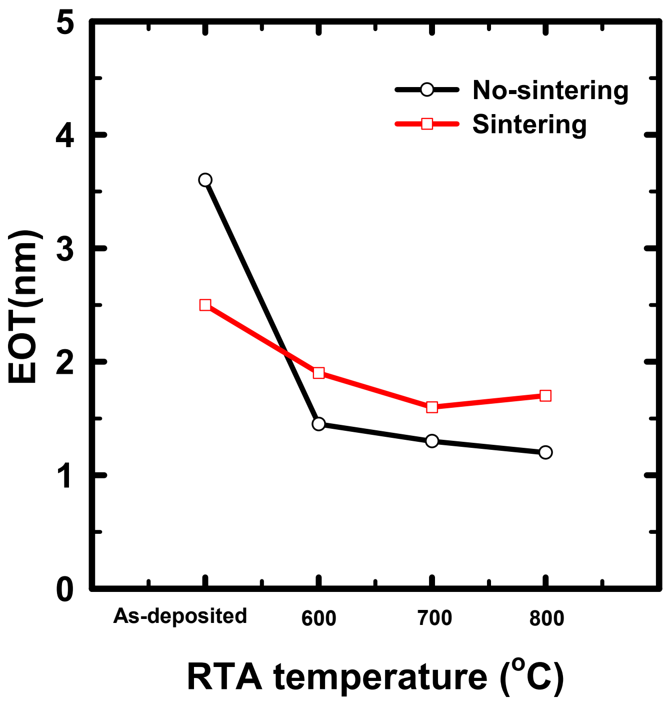


Fig.2-11 EOT variation of samples with sintering and no-sintering according to annealing temperature N2 for 60s.

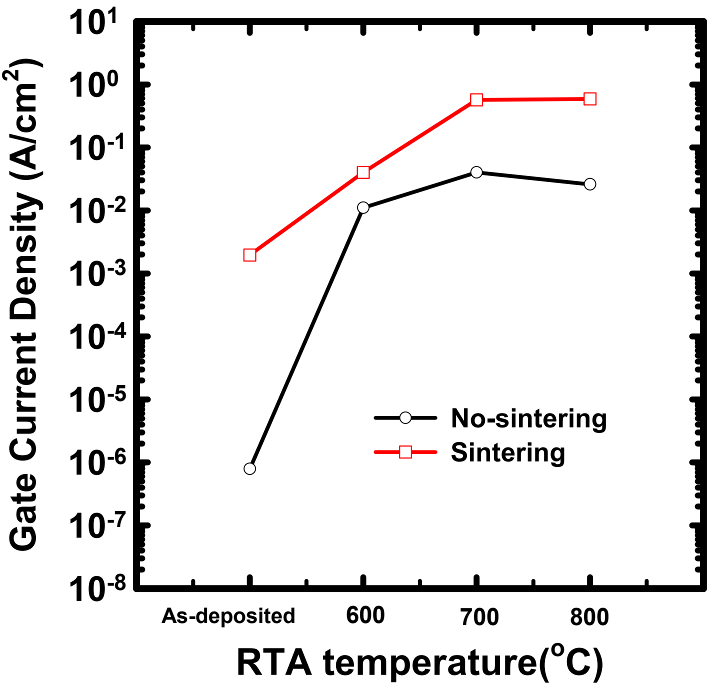


Fig.2-12. Leakage current density variation of samples with sintering and no sintering according to annealing temperature N2 for 60s.

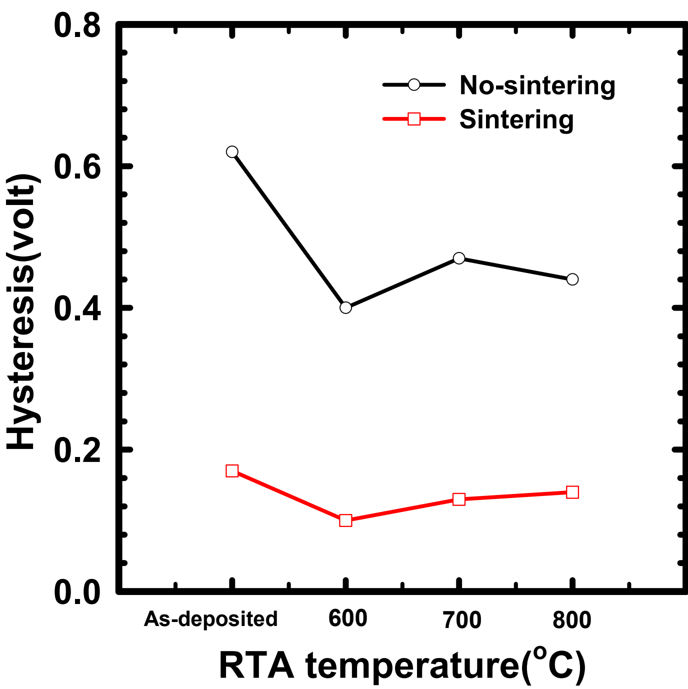


Fig.2-13. Hysteresis as a function of RTA temperature for samples with (square) and without (circle) sintering.

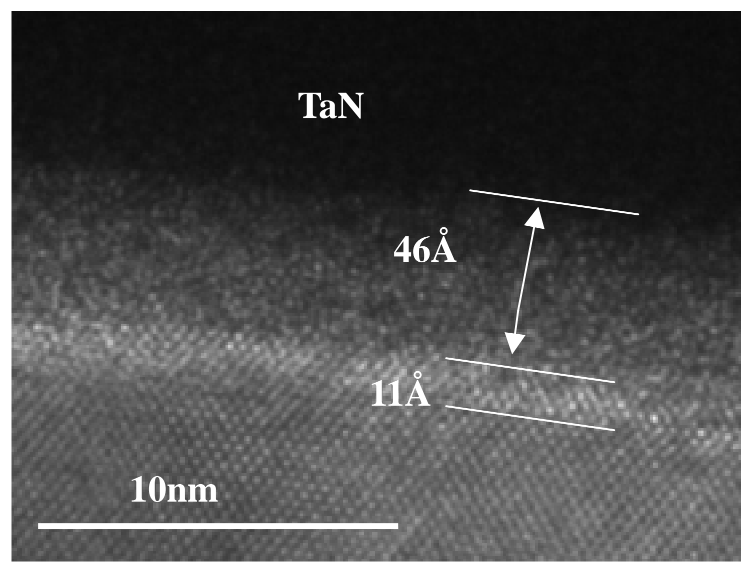


Fig.2-14 (a) TEM image of sample without RTA treatment.

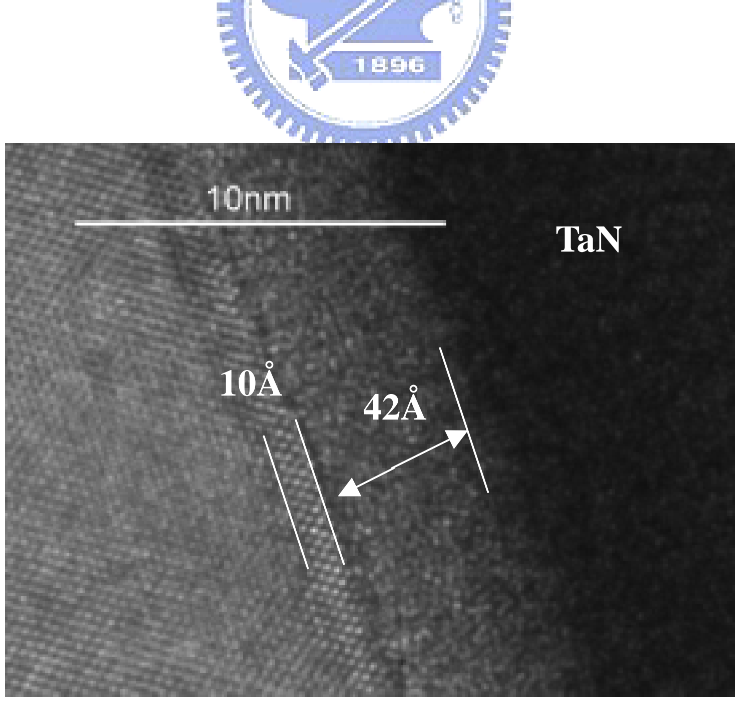
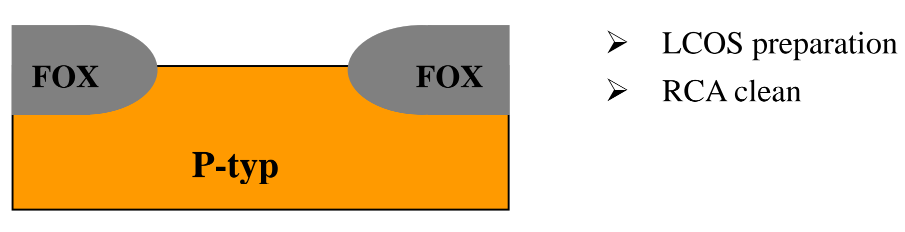


Fig.2-14 (b) TEM image of sample with RTA treatment at 600°C



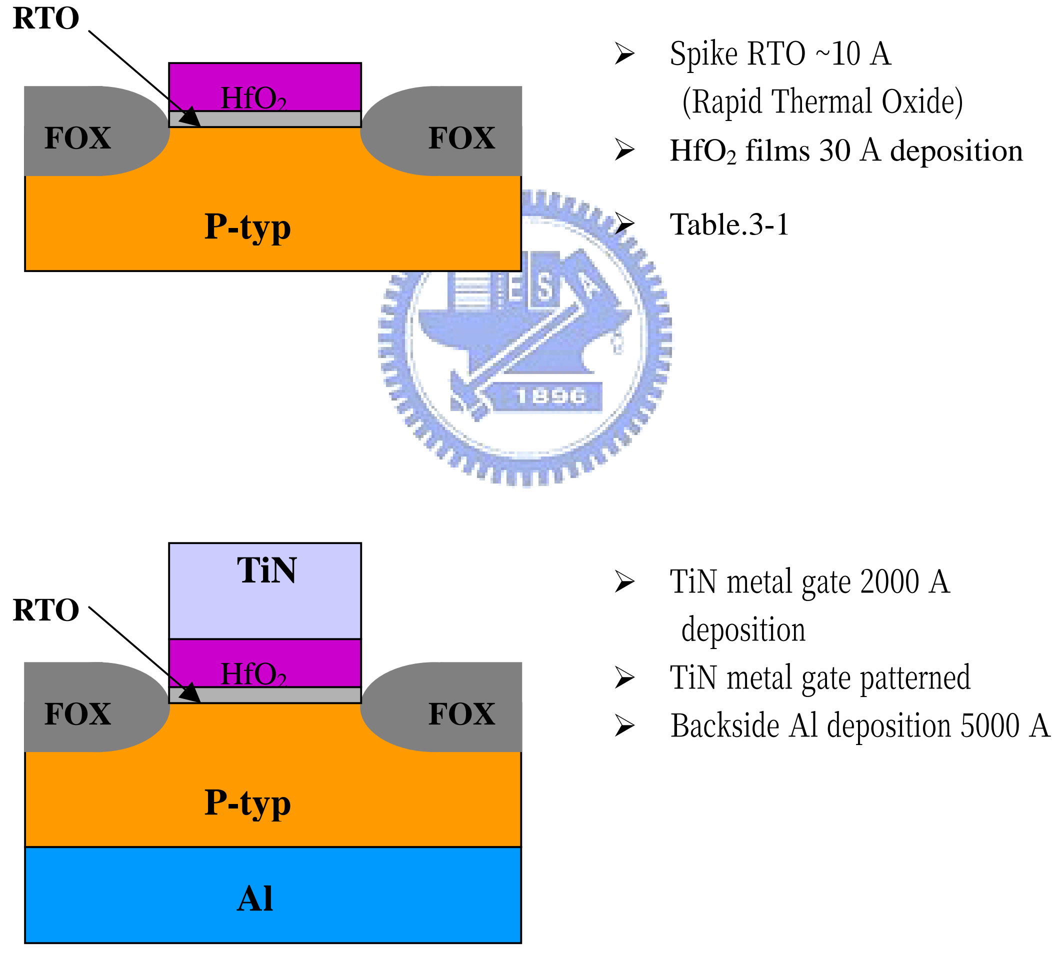


Fig. 3-1. Cross-sectional view and key experimental procedures of the test structure.

sample	control	Bottom Nitridation (BN)	Top Nitridation (TN)
Capacitor structure RTO layer Nitridation layer	HfO_2 Si	HfO_2 Si	HfO_2 Si

Table. 3-1 Split conditins

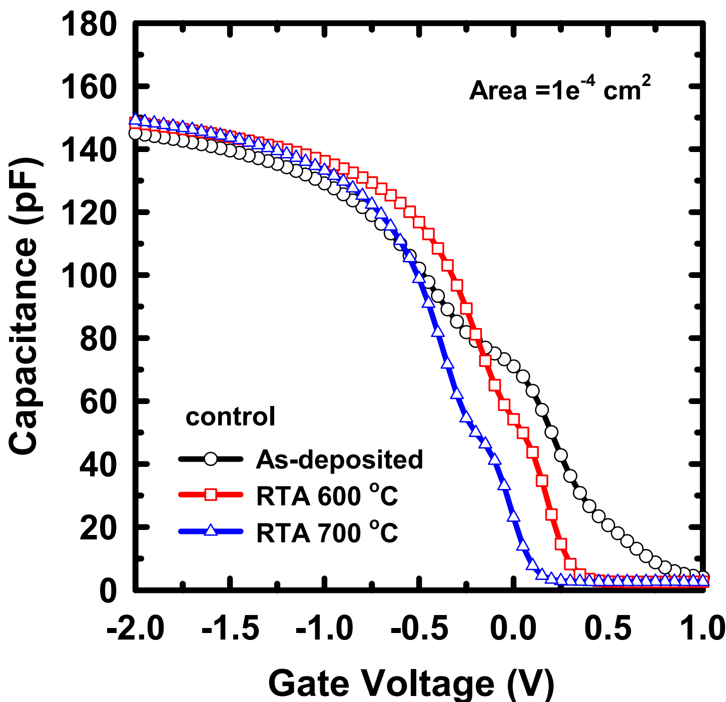


Fig. 3-2: Gate capacitance vs. gate voltage. The plot shows high frequency C-V curves of the control samples with various RTA temperatures

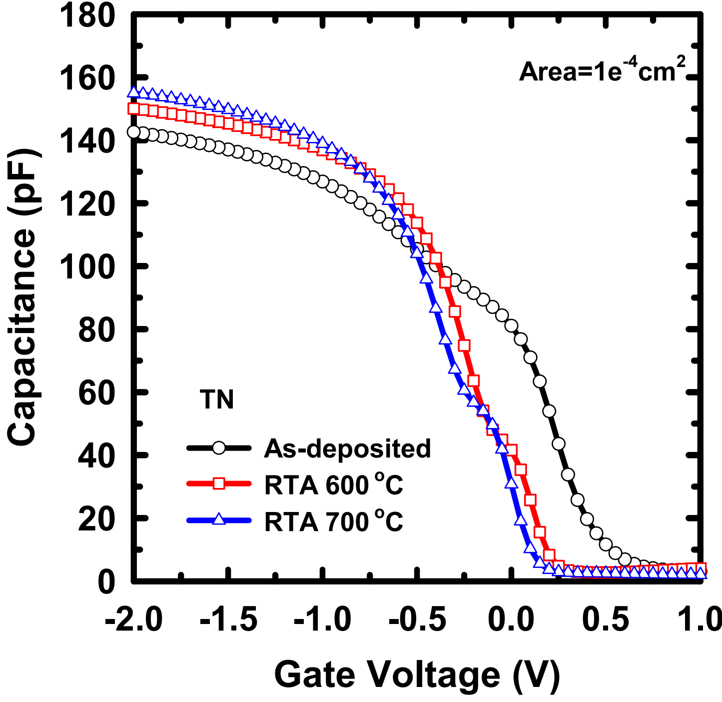


Fig. 3-3: Gate capacitance vs. gate voltage. The plot shows high frequency C-V curves of the TN samples with various RTA temperatures

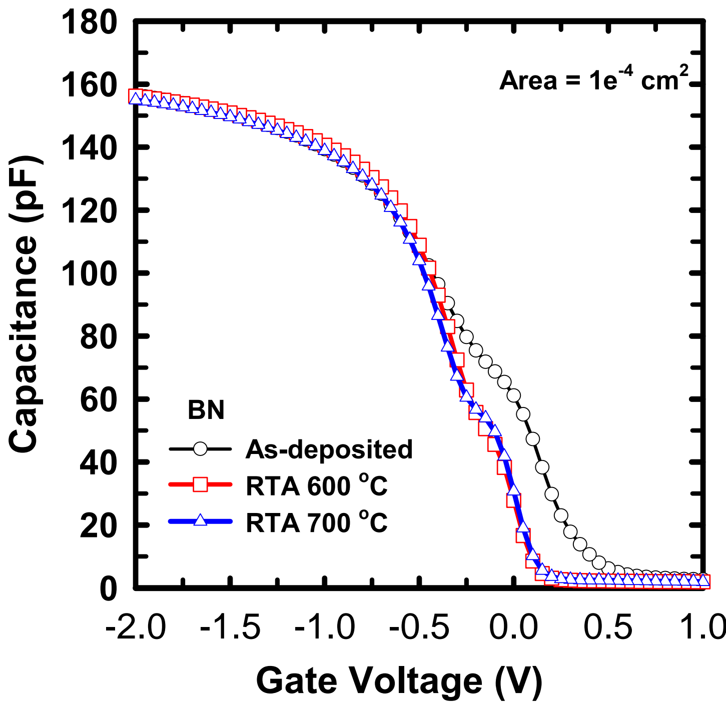


Fig. 3-4: Gate capacitance vs. gate voltage. The plot shows high frequency C-V curves of the BN samples with various RTA temperatures

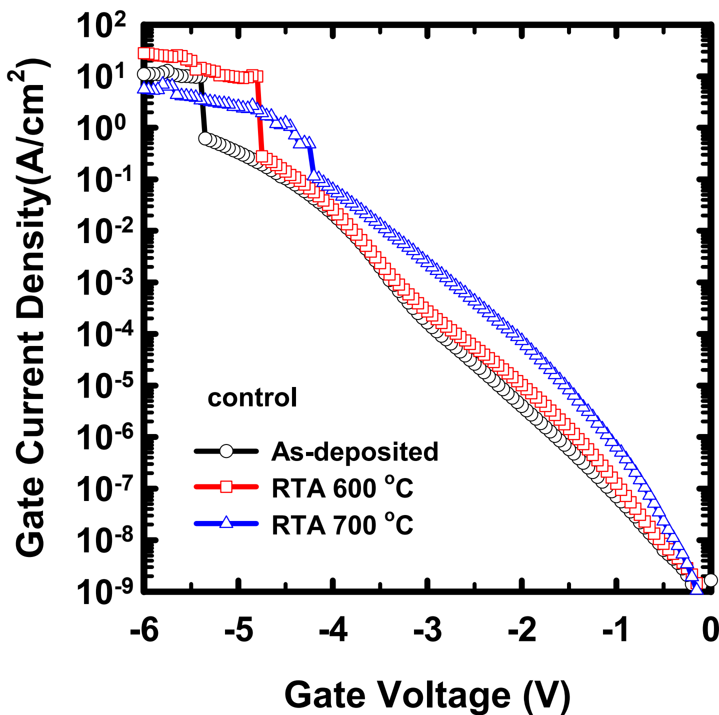


Fig. 3-5: J-V characteristics of the control samples with various RTA temperatures.

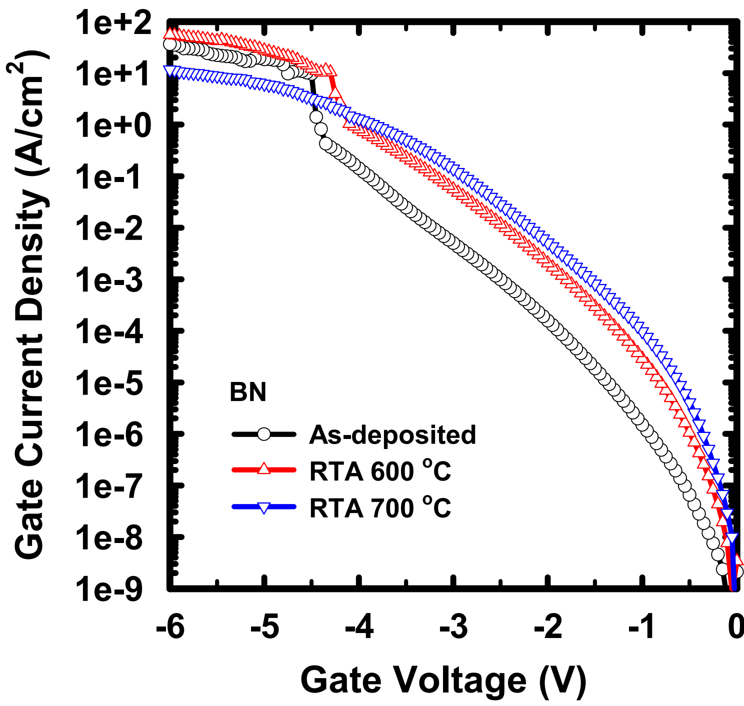


Fig. 3-6: J-V characteristics of the BN samples with various RTA temperatures.

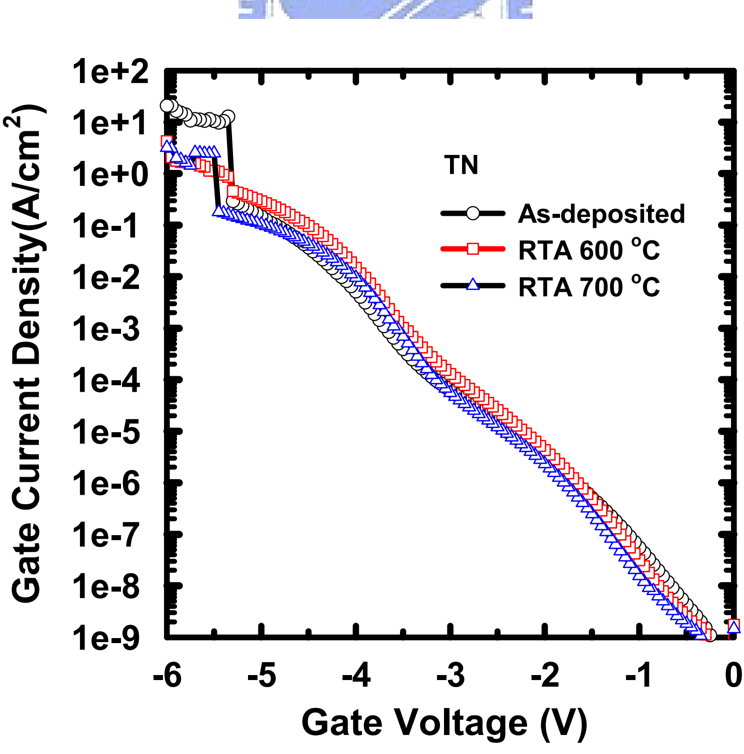


Fig. 3-7: J-V characteristics of the TN samples with various RTA temperatures.

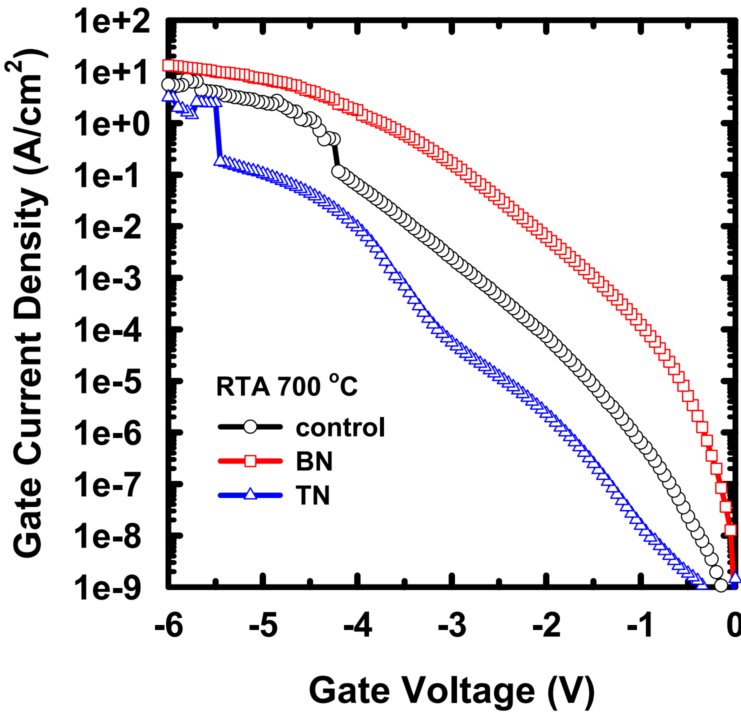


Fig. 3-8: The comparison of leakage current density among the control, BN and TN samples at RTA 700°C.

1896

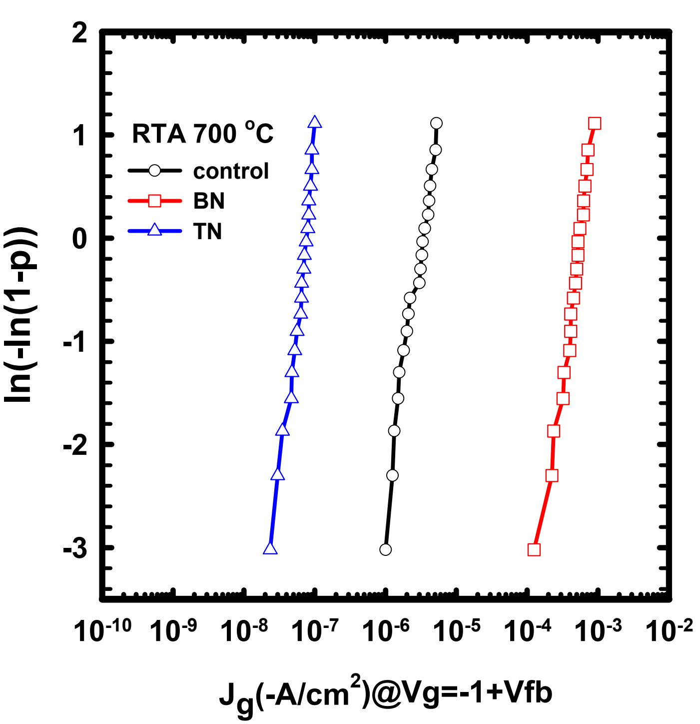


Fig. 3-9: The leakage current distribution of different treatment at 700°C.

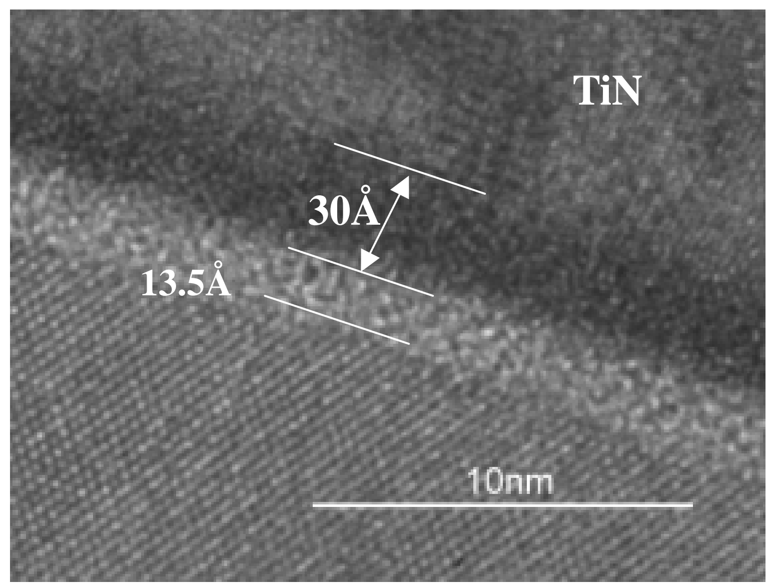


Fig.3-10(a) TEM image of control samples without RTA treatment.

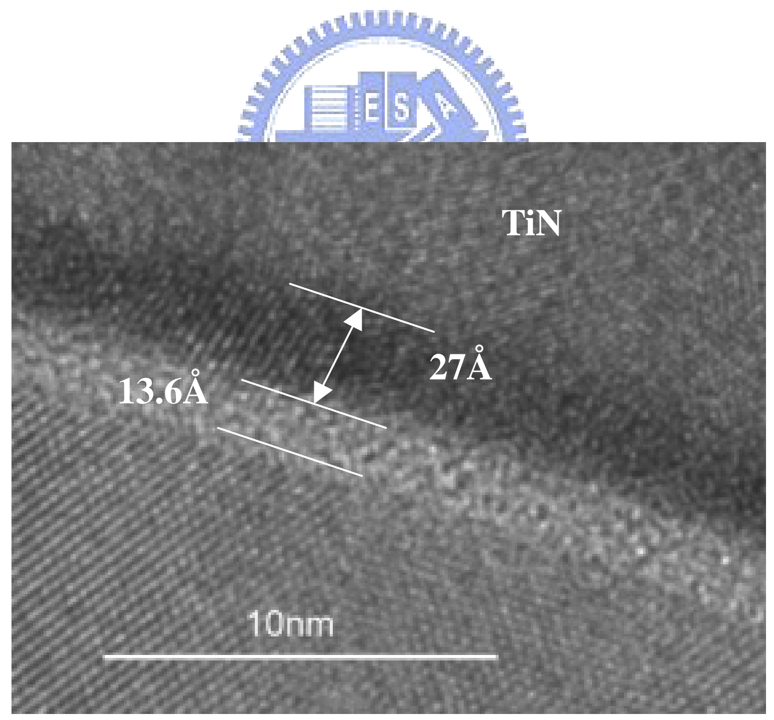


Fig.3-10 (b) TEM image of control samples with RTA at 600 ^{o}C .

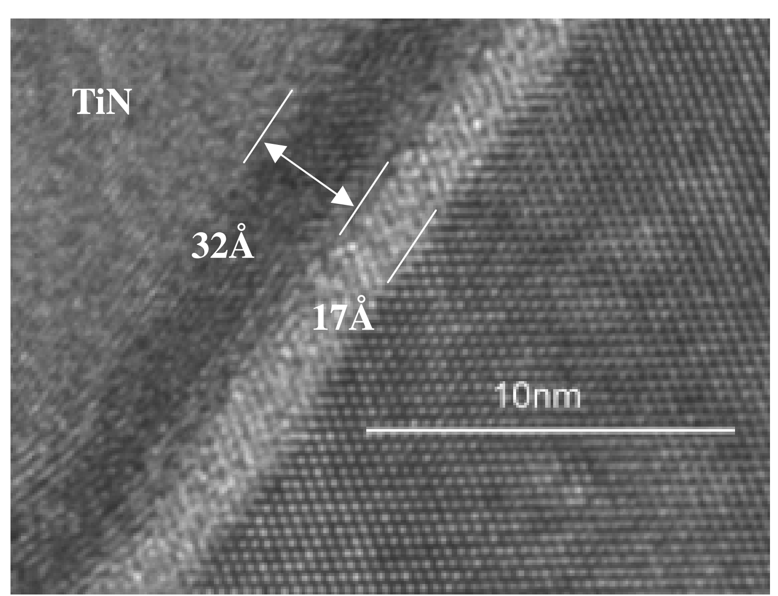


Fig.3-10(c) TEM image of control samples with RTA at 700 ^{o}C .

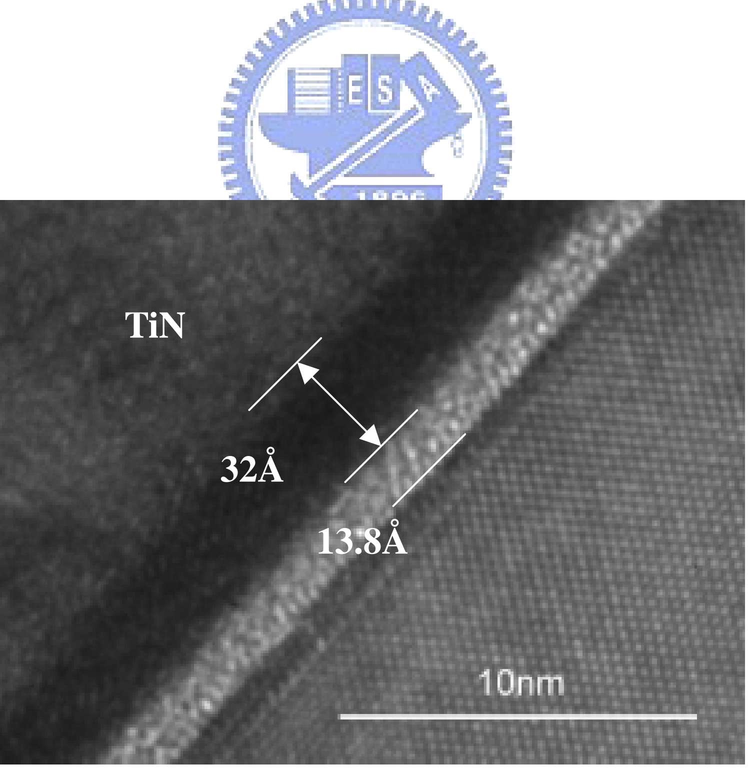


Fig.3-10 (d) TEM image of TN samples with RTA at 700 ^{o}C .

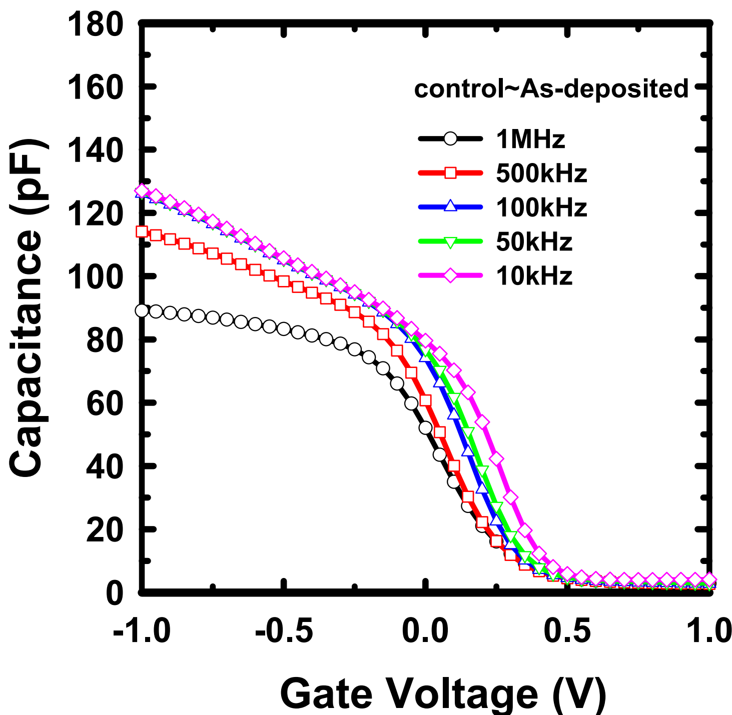


Fig.3-11(a) C-V curves measured at multiple frequencies of control samples without RTA.

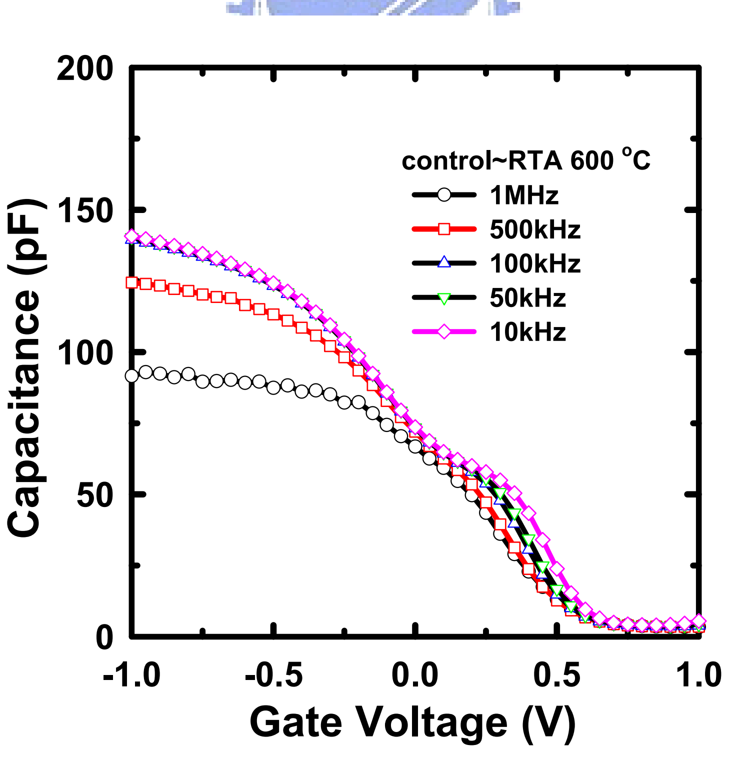


Fig.3-11(b) C-V curves measured at multiple frequencies of control samples with RTA at 600°C.

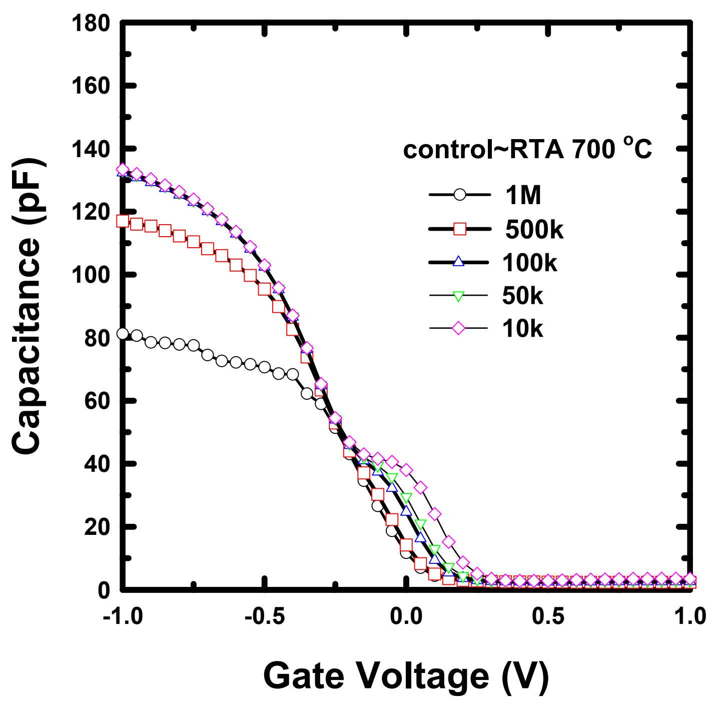


Fig.3-11(c) C-V curves measured at multiple frequencies of control samples with RTA at 700℃.

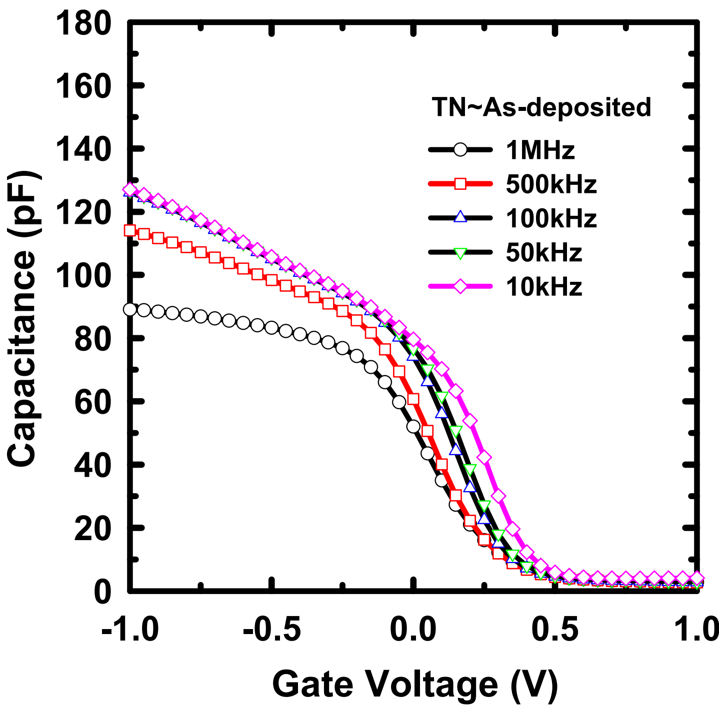


Fig.3-12(a) C-V curves measured at multiple frequencies of TN samples without RTA.

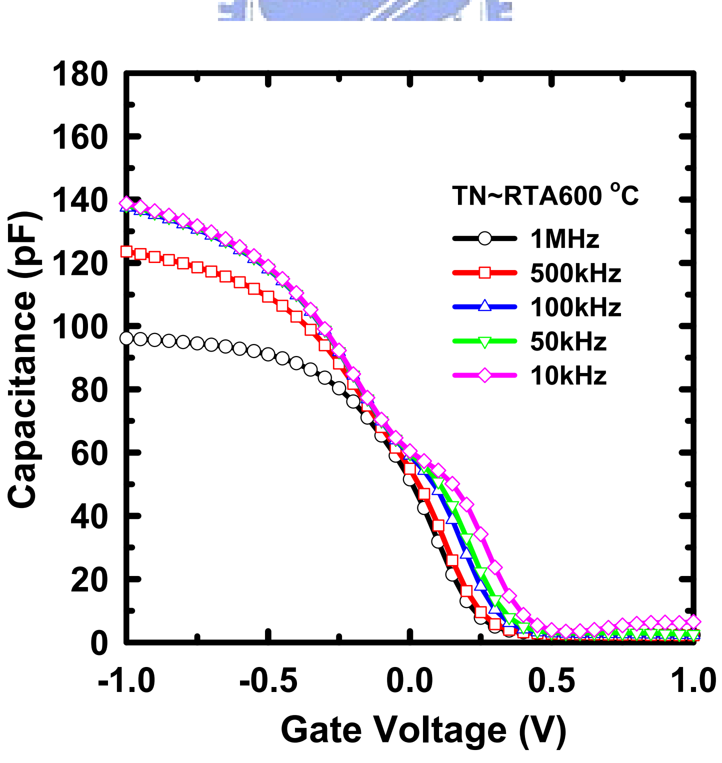


Fig.3-12(b) C-V curves measured at multiple frequencies of TN samples with RTA at 600°C.

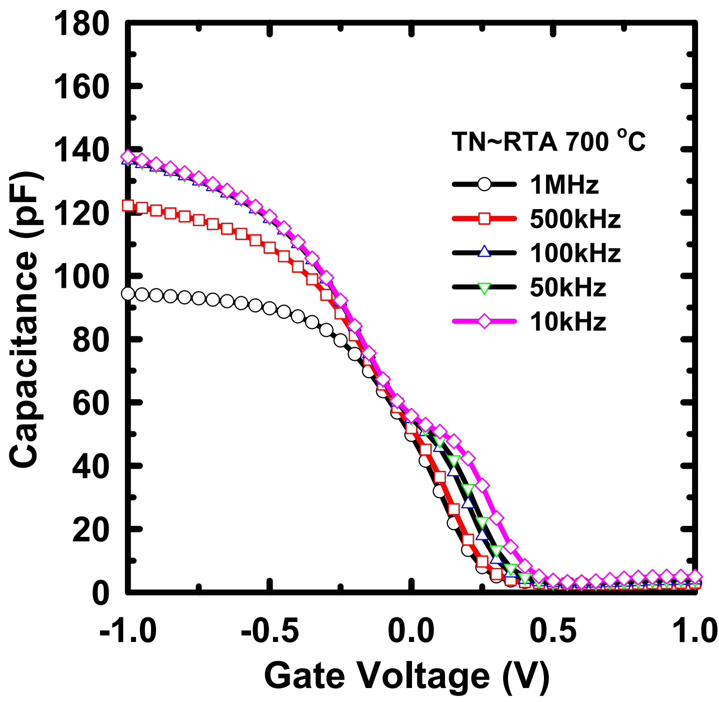


Fig.3-12(c) C-V curves measured at multiple frequencies of TN samples with RTA at 700°C.

1896

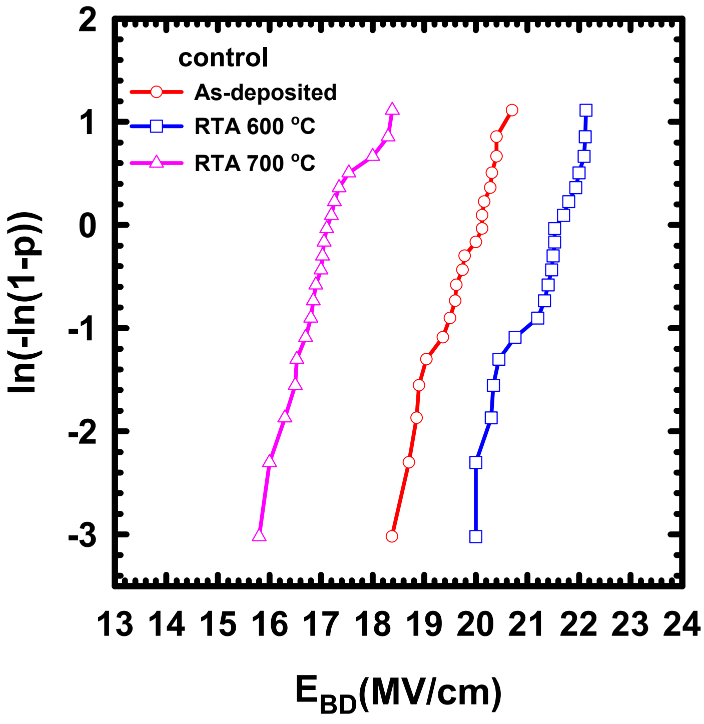


Fig.3-13 The Weibull plot shows the breakdown field for the control samples.

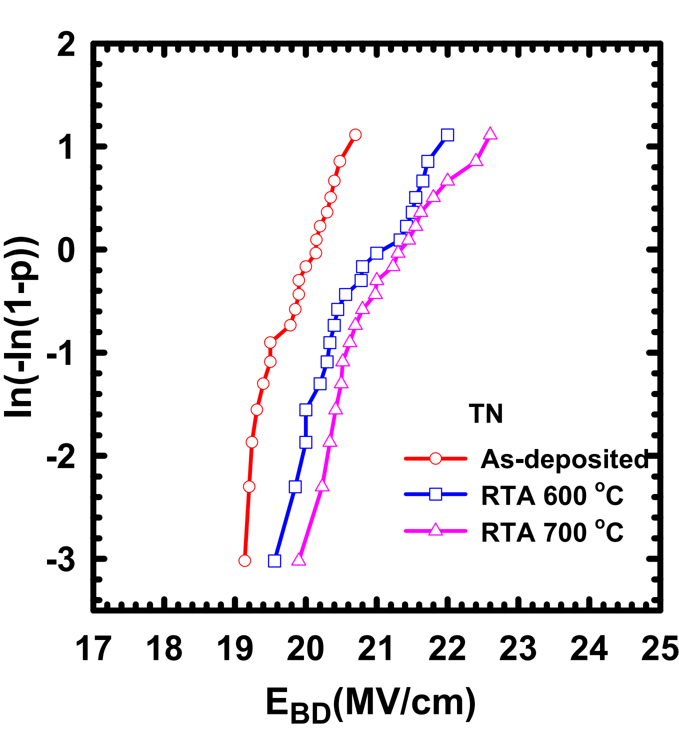


Fig.3-14 The Weibull plot shows the breakdown field for the TN samples.

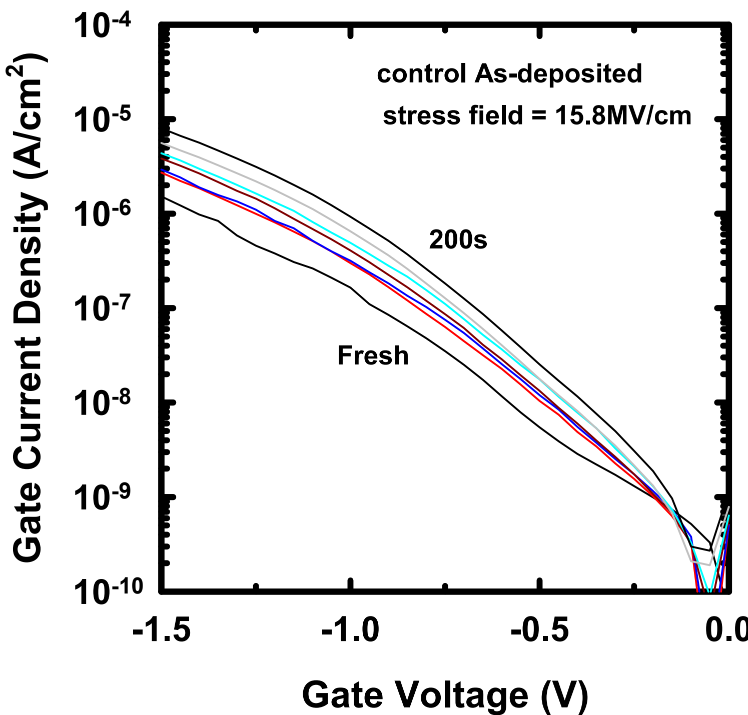


Fig.3-15(a) SILC result of control sample under constant field (15.8MV/cm)stressing for as-deposited.

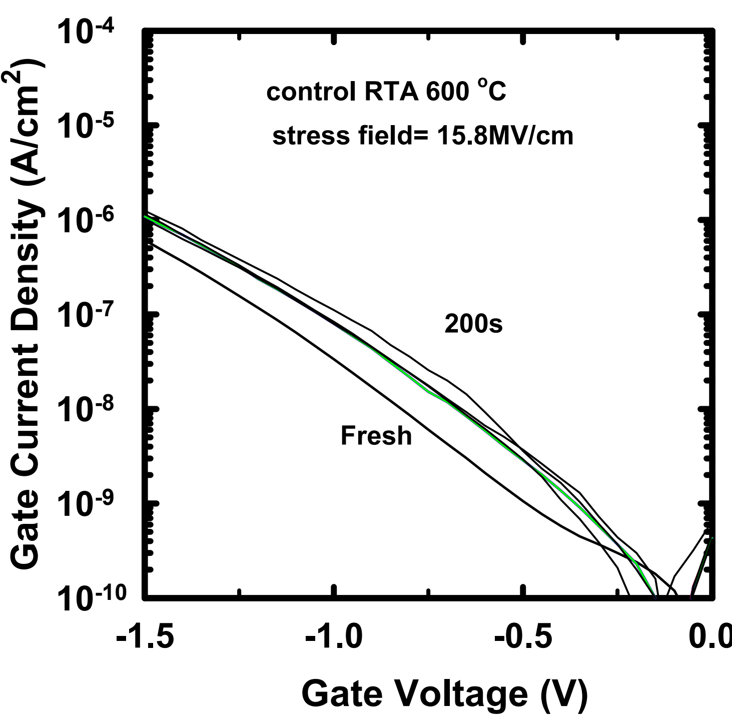


Fig.3-15(b) SILC result of control sample under constant field (15.8MV/cm) stressing for 600℃ RTA.

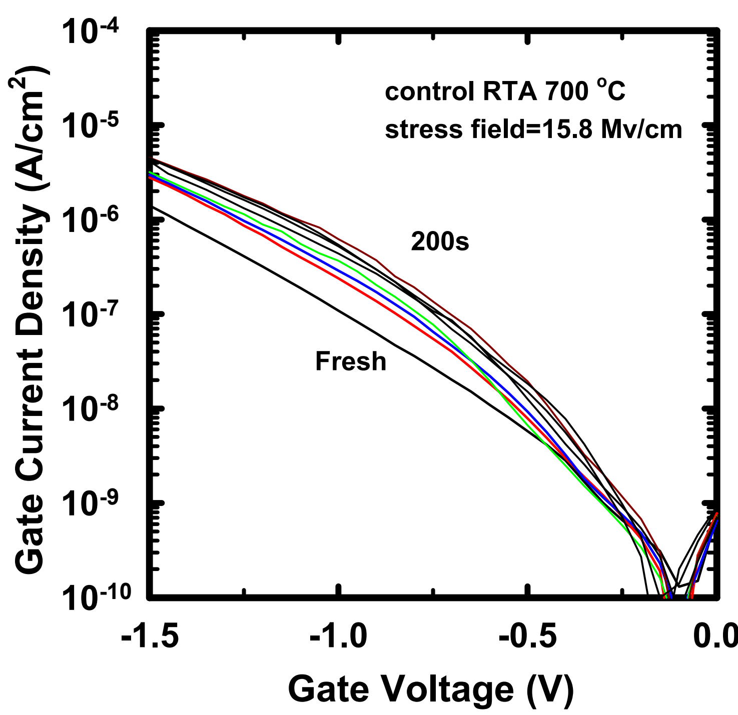


Fig.3-15(c) SILC result of control samples under constant field (15.8MV/cm) stressing for 700℃ RTA.

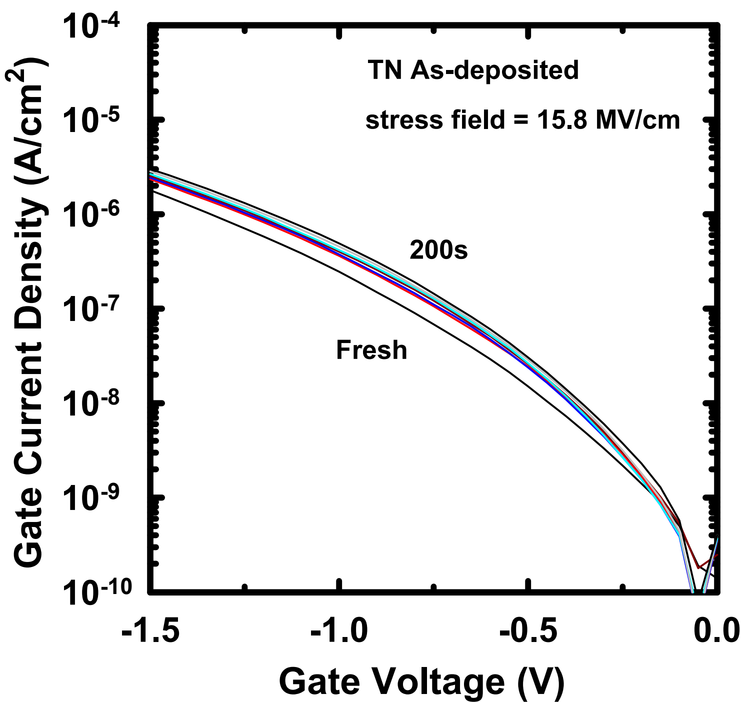


Fig.3-16(a) SILC result of TN samples under constant field (15.8MV/cm) stressing for as-deposited.

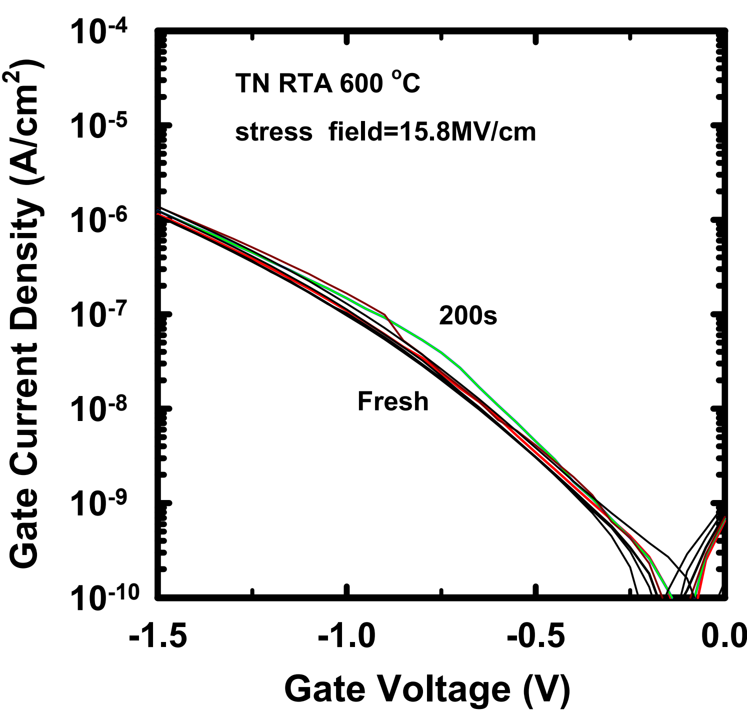


Fig.3-16(b) SILC result of TN samples under constant field (15.8MV/cm) stressing for 600°C RTA.

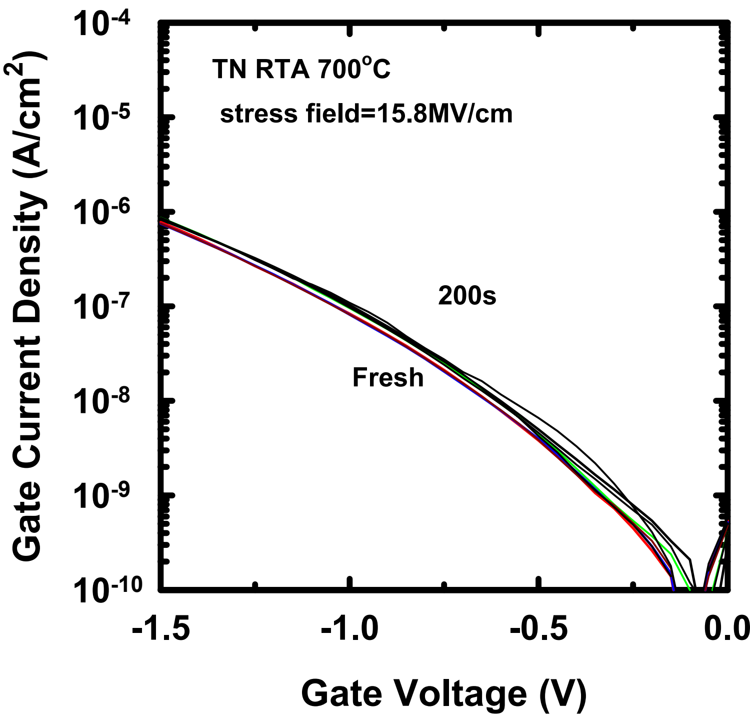


Fig.3-16(c) SILC result of TN samples under constant field (15.8MV/cm) stressing for 700℃ RTA.

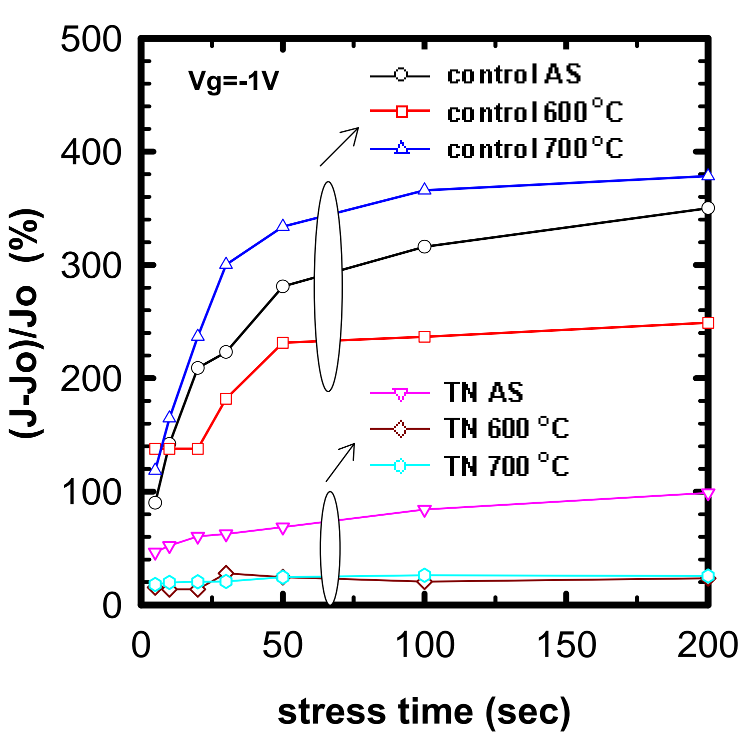


Fig.3-17 Trap generation rate ((J-Jo)/Jo)% (J at Vg=-1V)against stress time for control and TN samples with various RTA treatments.

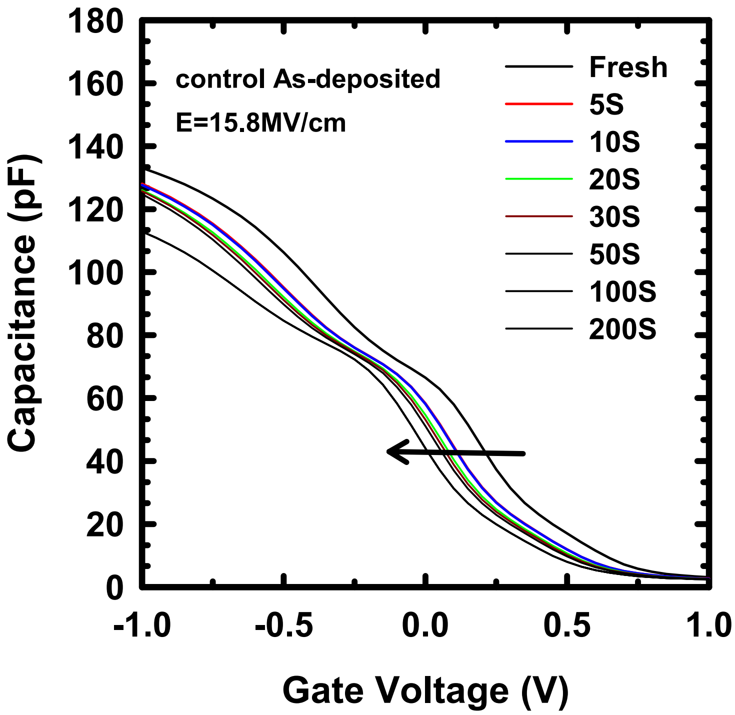


Fig.3-18(a) The C-V curves before and after constant voltage stress in HfO_2 gate dielectrics for control sample without RTA treatment

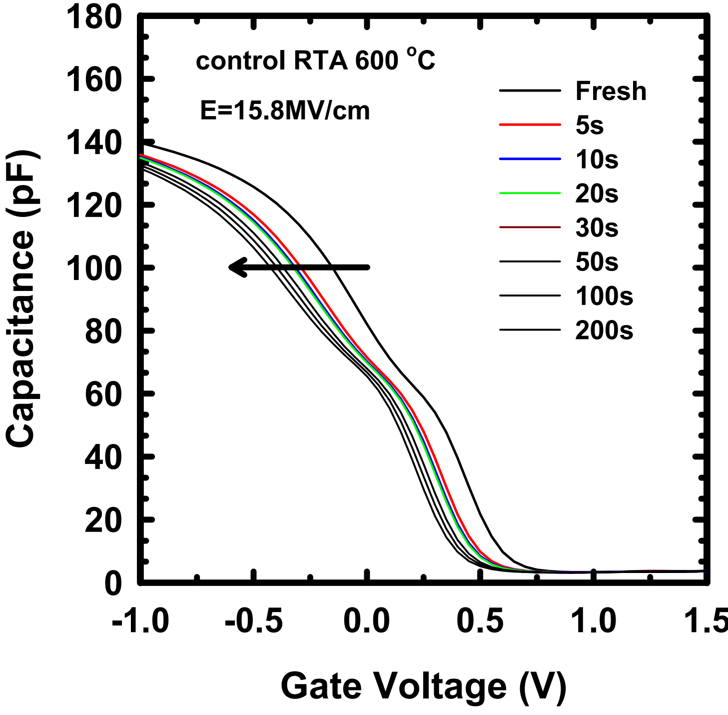


Fig.3-18(b) The C-V curves before and after constant voltage stress in HfO_2 gate dielectrics for control sample with 600 °C RTA.

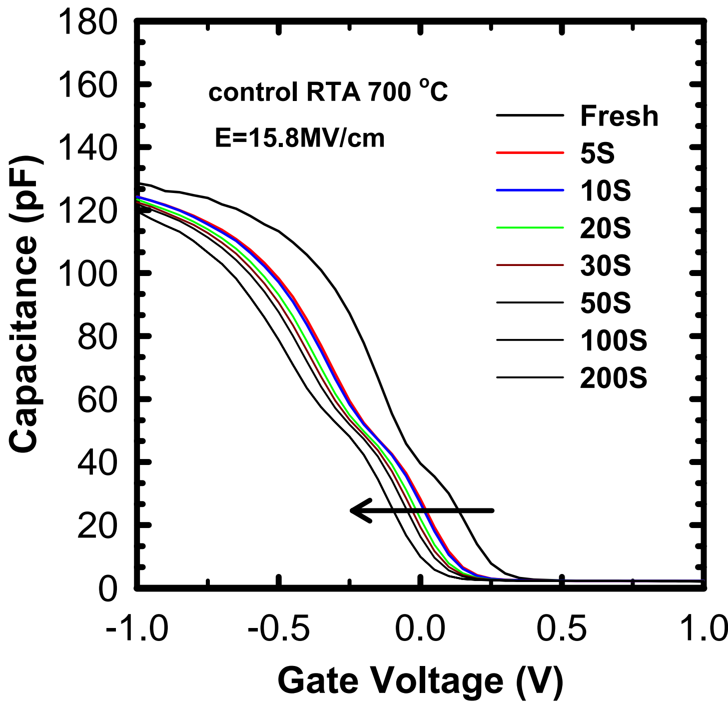


Fig.3-18(c) The C-V curves before and after constant voltage stress in HfO_2 gate dielectrics for control sample with 700 °C RTA.

ES 1896

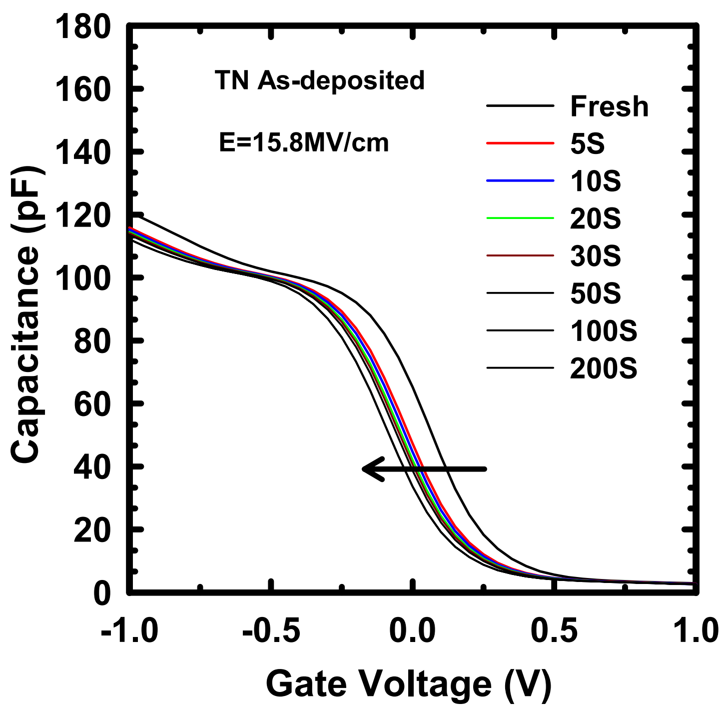


Fig.3-19(a) The C-V curves before and after constant voltage stress in HfO_2 gate dielectrics for TN sample without RTA .

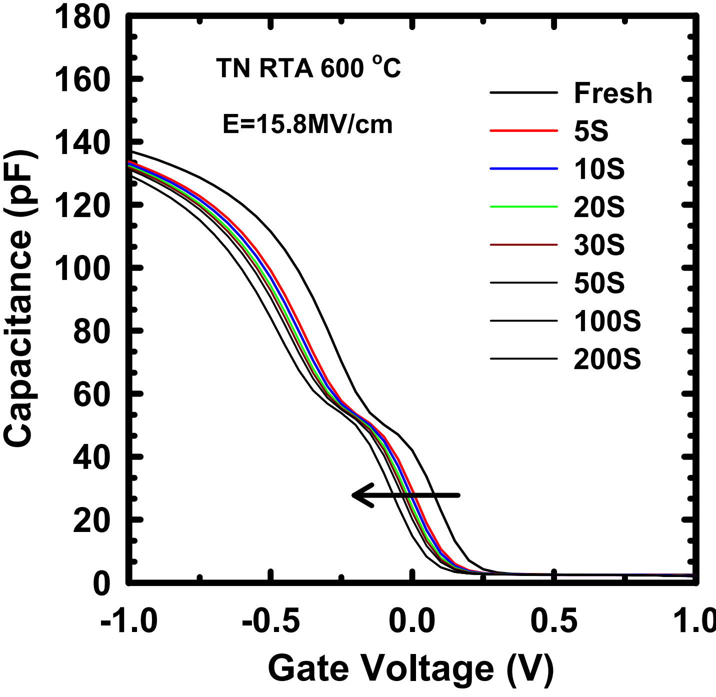


Fig.3-19(b) The C-V curves before and after constant voltage stress in HfO_2 gate dielectrics for TN sample with 600 ^{o}C RTA.

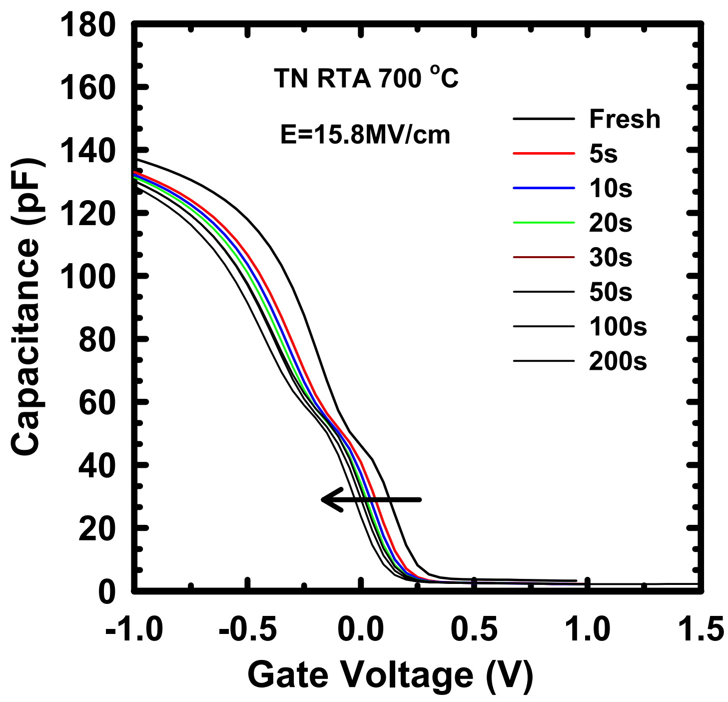


Fig.3-19(c) The C-V curves before and after constant voltage stress in HfO_2 gate dielectrics for TN sample with 700 °C RTA.

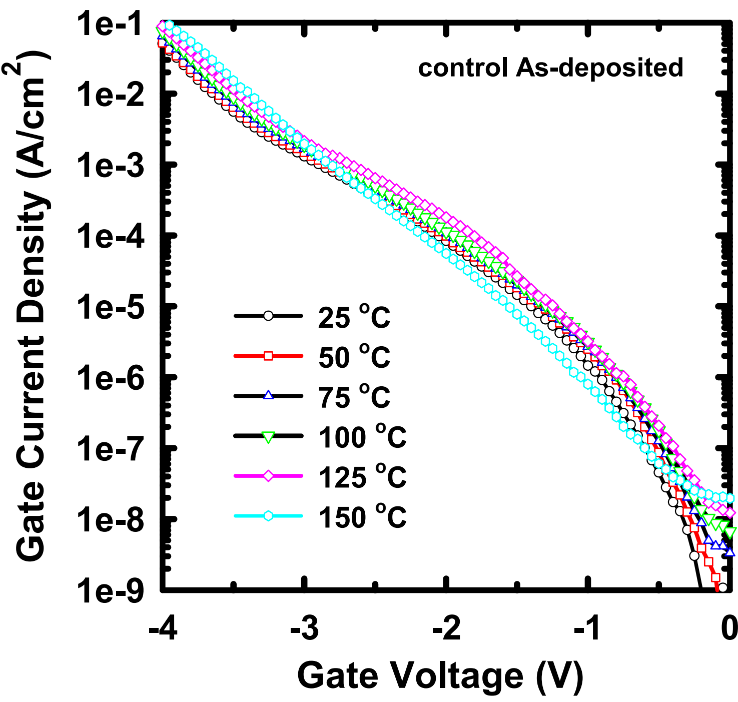


Fig.3-20 (a) J-V curves as a function of temperature for control samples without RTA treatment.

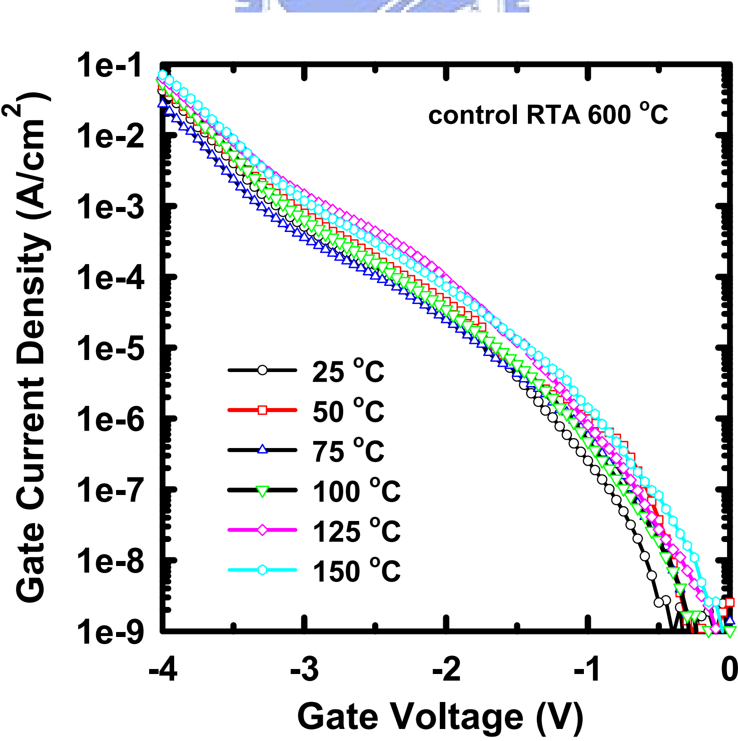


Fig.3-20 (b) J-V curves as a function of temperature for control samples with 600 ^{o}C RTA.

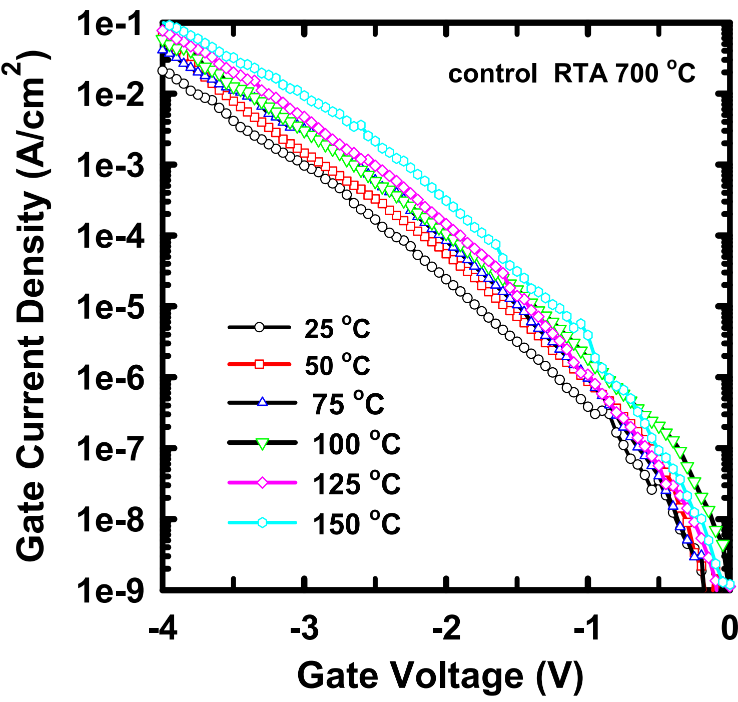


Fig.3-20 (c) J-V curves as a function of temperature for control samples with 700 °C RTA.

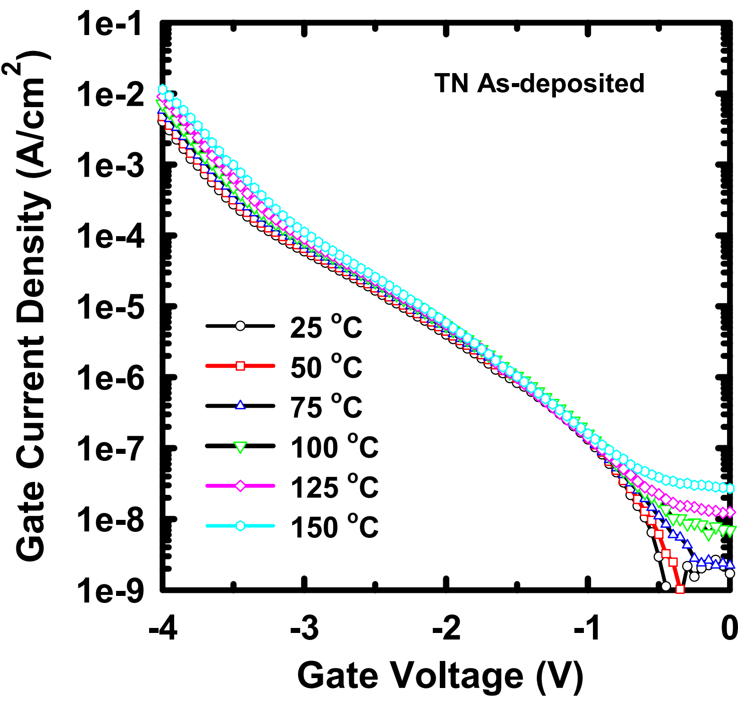


Fig.3-21 (a) J-V curves as a function of temperature for TN samples without RTA.

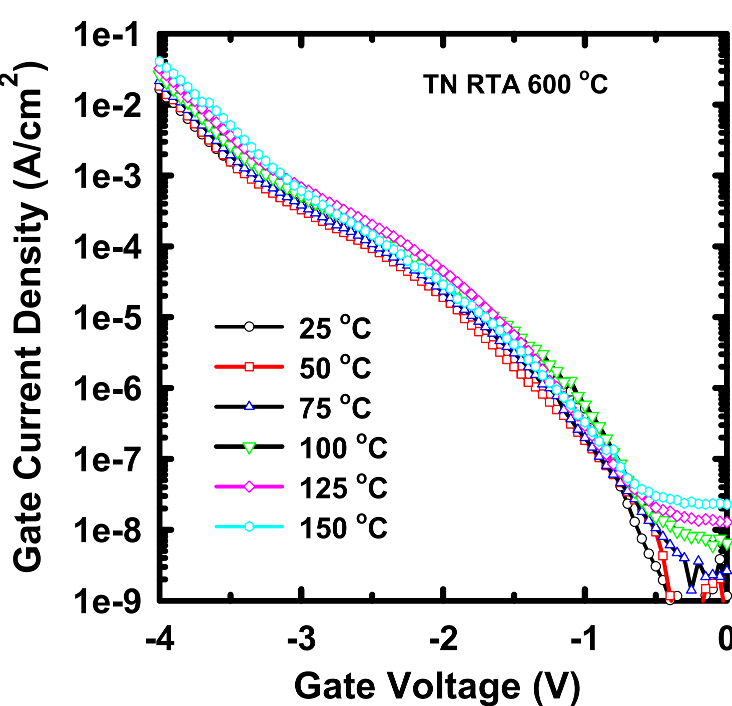


Fig.3-21 (b) J-V curves as a function of temperature for TN samples with 600°C RTA.

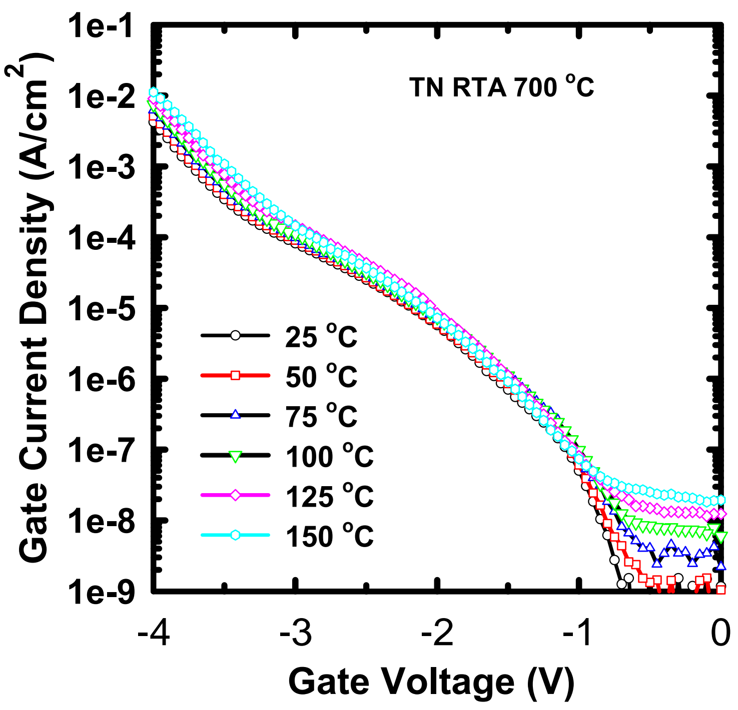


Fig.3-21 (c) J-V curves as a function of temperature for TN samples with 700°C RTA.

簡歷

姓名：林盈彰

姓別：男

年齡：24 歲　（民國 69 年 05 月 04 日）

籍貫：台灣省 彰化縣

現址：彰化縣埔心鄉東門村員鹿路二段 335 號

學歷：國立成功大學　（87 年 9 月~ 91 年 6 月）

國立交通大學電子研究所碩士班固態組 91 年 9 月~ 93 年 6 月）

論文題目：氧化鑭，氧化鐠及氧化鉿介電層特性之研究

The Study of Electrical Properties on La_2O_3, Pr_2O_3 and HfO_2 Gate Dielectrics