國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

高介電常數射頻金屬-絕緣層-金屬電容及其電容值變動之研究

The Investigation of the Variation of the Capacitance of High-κ RF Metal-Insulator-Metal Capacitors

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中華民國九十三年六月

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摘要

隨著互補式金氧半電晶體元件的特徵尺寸持續地微縮，閘極介電質（目前主流為二氧化矽）的厚度也隨之減少以保持住電容值，使得電晶體元件的驅動電流保持在可接受的大小。半導體工會組織所訂定的半導體技術未來指標中指出，在 2003 至 2005 年時，等效閘極介電質的厚度將會減少至將近 1.5 奈米。然而降低二氧化矽的厚度至如此小的尺寸時，將會導致量子穿遂漏電流的發生，且此漏電流的大小會隨著厚度的減少而成指數性地增加。因此，高介電常數介電質為一個解決此問題的適當替代物，除了可避免介電質厚度的降低以減少漏電流外，且可和互補式金氧半電晶體的製程整合在一起，並可達到與二氧化矽等效的電容值。

在此，我們研究使用高介電質『氧化鋁鉭』於金氧金（MIM）電容且整合在 400°C 的後段製程上。在高頻時，為了達到高電容密度、微小的電容值下降率

和低漏電流，所以使用此高介電質『氧化鋁鉭』。此高電容密度的電容可以有效地減少在射頻積體電路上晶片的大小。除了高電容值密度外，我們還測得了氧化鋁鉭金氧金電容的電壓係數（VCC）與溫度係數（TCC）隨著頻率的增加而迅速遞減。而當操作頻率到達 1 GHz 時，與電壓相關的電容值變動率將小於萬分之二，此一性質可保證於精確的射頻電容電路應用中。

我們同時也解釋了此電壓相關的電容變化值與介電質厚度及頻率的相依性，並且也說明了氧化鋁鉭金半金電容的電容值與溫度的相關性。以『自由載子注入模型』為基礎，可通盤地瞭解（1）介電質厚度 t 與電容值變動的相依性，此為電場極化的本質特性所導致的。(2)頻率與溫度對電容值變動的相關，這些均是由於絕緣層內電荷的遷移率改變造成了偶極的鬆弛時間不同所導致的。

除此之外，我們已量測與分析了從 10 KHz 到 10 GHz 的電容值對於電壓與頻率的變化率，並且對於鬆弛時間加入了一項與頻率相關的因子來解釋電容值變動的降低，此模型也可被應用於預測之後的電容值變化率。

The Investigation of the Variation of the Capacitance of High-κ RF Metal-Insulator-Metal Capacitors

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Abstract

As the feature sizes of complementary metal-oxide-semiconductor (CMOS) devices are scaled downward, the gate dielectric thickness must also decrease to maintain a value of capacitance to keep device drive current at an acceptable level. The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) indicates that by the year 2003~2005, the equivalent thickness of the gate dielectric will need to be approximately 1.5 nm. Reducing the thickness of SiO_2 to these dimensions will result in an exponential increase of direct tunneling leakage current. A suitable replacement dielectric with a high relative permittivity κ (or dielectric constant) must exhibit low leakage current, have the

ability to be integrated into a CMOS process flow, and exhibit at least the same equivalent capacitance of SiO_2.

We have studied the metal-insulator-metal (MIM) capacitors integrity using high-κ Al doped TaO_x dielectrics formed under 400°C backend process. Using high-κ Al doped TaO_x dielectric, we have obtained record high MIM capacitance density of 17 fF/μm^2 at 100 KHz, small 5% capacitance reduction to radio frequency (RF) range, and low leakage current density of 8.9×10^{-7} A/cm^2. This very high capacitance density with good MIM capacitor characteristics can significantly reduce the chip size of radio frequency integrated circuits (RF ICs).

In additional to the very high capacitor density of 17 fF/μm^2 at 100 kHz, the measured voltage-coefficient of capacitor (VCC) and temperature-coefficient of capacitor (TCC) of Al doped TaO_x MIM capacitors decrease rapidly with increasing frequency. Excellent normalized voltage-dependent capacitor variation ($\Delta C/C$) ≤ 200 ppm is obtained at these capacitors as frequency reaching 1 GHz, which can ensure precision capacitor circuit application at RF regime with drastically reduced capacitor size.

We also explain the dependence of normalized voltage-dependent capacitor variation $\Delta C/C$-V on dielectric thickness and frequency, below 1 MHz, as well as temperature dependence of capacitance of Al doped TaO_x MIM capacitors. Based on free carrier injection model, a unified understanding is achieved: (1) the dielectric thickness (t) dependence ΔC/C is an intrinsic property due to electric field polarization, (2) the frequency dependence of ΔC/C and temperature dependence of capacitance are all due to change of relaxation time with different carrier mobility in insulator.

We have measured and analyzed the normalized frequency-dependent voltage-dependence of capacitance (ΔC/C-V), from 10 KHz to 10 GHz. We modified a free carrier injection model having a frequency dependent $[1+(f/f_0)^2]^{-1/2}$ pre-factor for relaxation time (τ), to explain the reduction of ΔC/C in the GHz range. This model is also applied to predict the ΔC/C for future applications.

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MIM capacitors. The experimental data can be fitted by an emission current model.

Fig. 7-4. Measured and simulated ΔC/C-V data assuming a nearly constant t. Although good agreement is obtained at 10 KHz and 1 MHz, the assumption fails to account for the 1 GHz and 10 GHz data.

Fig. 7-5. Modified carrier relaxation time as a function of frequency using a $[1+(f/f_0)2]-1/2$ pre-factor.

Fig. 7-6. Measured and simulated ΔC/C using the frequency dependent relaxation time shown in Fig. 7-5.

Chapter 1

Introduction

1.1 The Choice of High-κ Dielectric to Reduce Device Size and Cost

As continuously scaling down the very large scale integration technology (VLSI Tech.), both the cut-off frequency f_T and the device size of radio-frequency metal-oxide-semiconductor field effect transistors (RF MOSFETs) become improved and can be used for wireless communication [1.1]-[1.3]. However, the chip size and cost of RF circuits are not scaled considerably because of the large occupied area of non-scaled passive RF devices. Among various passive devices, the metal-insulator-metal (MIM) capacitors [1.4]-[1.11] are widely used in RF circuits for impedance matching and DC (Direct Current) filtering and occupied a large portion of circuit area. Therefore, a higher capacitor density is required to achieve the small size and cost. Since the capacitor density in MIM device is equal to $\varepsilon_0\kappa/t_d$, the use of high dielectric-constant (κ) metal-oxide materials [1.12]-[1.18] and reducing the dielectric thickness (t_d) are the methods to increase the capacitor density. However, the using high-κ dielectric is preferred because the reducing t_d will increase the capacitor leakage current density and loss tangent exponentially due to electron tunneling. According to the International Technology Roadmap for Semiconductors (ITRS), the choice of high-κ dielectric [1.17]-[1.19] is a key technology in increasing the capacitor density and in scaling down the chip size of analog and RF ICs. In additional to the higher κ, the dielectric must have good quality with low defect density related leakage current when formed under 400°C for VLSI backend process integration [1.16]. We have increased the capacitance density to 17 fF/μm^2 using high-κ Al doped TaO$_x$. Low leakage current density of 8.9×10^{-7} A/cm^2 is also obtained. This excellent result suggests the developed high-κ MIM capacitor can be used for RF circuit with largely reduced device size.

1.2 Small Variation of Capacitance for the Precision Capacitor Circuit Application at RF Regime

In addition to high capacitor density and Quality (Q)-factors, high-κ MIM capacitors should have good low voltage coefficient (VCC) or small voltage-dependence of the normalized capacitance variation (ΔC/C) from intermediate- frequency (IF) to radio-frequency (RF). The required low ΔC/C or VCC is listed in the ITRS roadmap because it is important for designing the analog/RF circuits under sweep voltages. The variation, ΔC/C, at RF frequencies is crucial since the operation frequencies of advanced analog circuits are now in the GHz range.

However, the commercially available capacitor meters operate at frequencies up to only 1 MHz. To overcome this difficulty, we introduce a new method of calculating

ΔC/C from the measured scattering-parameters (S-parameters) using RF circuit theorem [1.18]. We use this approach to measure high-κ Al doped TaO_x capacitors which have very high capacitance density (17 fF/μm^2). The ΔC/C decreases rapidly with increasing frequency to only 196 ppm in the GHz range.

We have investigated the normalized voltage-dependent capacitor variation (ΔC/C) or voltage-coefficient of capacitance (VCC) and temperature-coefficient of capacitor (TCC) of Al doped TaO_x high-κ dielectrics from IF to RF frequencies, which are important factors for precision circuit matching. We have found that the ΔC/C of Al doped TaO_x capacitors decreases rapidly to a small value ≤ 200 ppm with increasing frequency into GHz regime. Therefore, these high-κ dielectric capacitors can be used for precision circuits at RF frequencies [1.20].

1.3 The Mechanism of the Variation of the Capacitance

MIM capacitors attract more and more attentions recently in Si analog/RF circuit applications because of its low parasitic capacitance, low voltage coefficient, high quality factor in RF regime [1.21]-[1.23]. In MIM capacitors, one of the great challenges is to achieve small VCC. Though experimental results of VCC variation such as thickness effects have been reported [1.22]-[1.26], the mechanism of VCC dependence remains under study. Here, we present a unified understanding of voltage, thickness, and temperature dependence based on the free carrier injection model [1.27]-[1.28]. The model can also be used to understand other high-κ materials.

1.4 A Modified Model for the Variation of the Capacitance above 1 MHz

Although the free carrier injection model [1.27]-[1.28] describes the voltage-dependence of normalized capacitance variation (ΔC/C) for high-κ MIM capacitors, the reduction of ΔC/C at GHz frequencies does not agree with the assumption of a constant relaxation time, τ. This may be due to the dipole effects. We propose a modified free-carrier injection model having a frequency dependent $[1+(f/f_0)^2]^{-1/2}$ pre-factor for τ, to model the ΔC/C vs. V for high-κ MIM capacitors. The agreement between measured and modeled ΔC/C-V data suggests that the effective relaxation time (which dipole effects were considered) is feasible for modification of the free-carrier injection model.

The small ΔC/C variation at RF frequencies is highly desirable for high speed analog and RF circuit, while the high capacitance density for the high-κ MIM capacitors permit further scaling down of chip sizes and reducing the cost.

Chapter 2

Research of High-κ Dielectrics

2.1 The Overview of High-κ Dielectrics Research

2.1.1 Introduction

Research activities in alternative high-κ gate dielectrics for CMOS devices have greatly intensified in the past few years. This is due in large part to the 1997 ITRS document that projected the requirement of gate oxide thicknesses below 1 nm by the year 2012 and for 50nm device gate lengths. While considerable progress has been made, much work still remains in finding a replacement high-κ gate stack.

The replacement of SiO_2 by alternative dielectrics is a formidable task and we must consider the task as an integrated task involving not only the gate dielectric but the equally important fields of interface between gate dielectric and silicon, the gate contact material and the gate dielectric. Especially important is the dielectric – silicon interface because it has very essential influences on the MOS channel mobility and driving current of MOS devices. The interfaces of the gate dielectric – silicon and gate material - gate dielectric will form interfacial layers as shown in Fig. 2-1. It will degrade the characteristics far away form the expected.

2.1.2 Motivation

The primary motivation of high-κ gate dielectrics for CMOS is the potential for reducing the gate-to-channel tunneling current while maintaining the same induced channel conductive layer. A high-κ gate dielectric can be made physically thicker than SiO_2 for the same gate capacitance. In terms of reducing quantum tunneling current, the important material's parameter combination is the square root of the procedure of dielectric effective mass and the barrier height and the direct product of the dielectric constant. While the barrier heights of alternative dielectrics tend to be lower than SiO_2, this is more than compensated by the increased dielectric constant and thickness. At this time a wide range of alternative dielectrics have been shown to result in reduced tunneling currents for the same "equivalent" oxide thickness (EOT) and several have shown leakage current of below $1 A/cm^2$ at the 1 nm EOT value. The most promising high-κ dielectrics so far evaluated in capacitor form include the Group ⅢB oxides HfO_2 and ZrO_2 and Group ⅣB oxides La_2O_3 and Y_2O_3. The aluminates and silicates of these dielectrics are also of interest, because they have higher crystallization temperature than the pure oxides and it may also be easier to obtain a good dielectric – silicon interface with these compounds. Extensive research on these dielectrics has demonstrated the promising properties of these materials with regard to near ideal C-V characteristics and low gate leakage. Several deposition methods are being pursued and have demonstrated good capacitor results including (a) reactive ion sputtering [2.1]-[2.2], (b) physical deposition and oxidation [2.3], (c) Molecular Beam Epitaxy (MBE) [2.4], (d) Metal Organic Chemical Vapor Deposition (MOCVD) [2.5]-[2.6], (e) Low Pressure CVD (LPCVD), (f) Plasma Enhanced CVD (PECVD) [2.7]-[2.8], and (g) rapid thermal CVD. Atomic layer deposition (ALD) is also a potential long term manufacturing technique for achieving very uniform films over large areas as will be required in manufacturing.

2.1.3 Introduction of Metal Gate

Improved gate electrode materials are also essential to push to the limits of CMOS technology, because of finite depletion layer width encountered in a poly-silicon gate named poly depletion. Thus a major part of the gate stack research involves compatible gate electrode materials for the various high-κ gate dielectrics. These problems as well as the interface problems must be researched as a combined problem to meet the ITRS CMOS requirements. Metal gate electrodes are highly desirable to eliminate poly depletion problems, however to meet threshold voltage requirements, two metals are required to replace both n^+ and p^+ polysilicon. While potential metals are available with appropriate work functions, most elemental metals are highly reactive not only on the potential high-κ dielectrics, but also on SiO_2 as well. However, potential metal gate materials have been identified and studied and at present the most promising have been Ta, TaN_x, and $TaSi_xN_y$ for an n^+ replacement and Ru and RuO_2 for a p^+ replacement. These have been studied not only in capacitor structures, but in FET structures.

2.1.4 Effect of Interface

Another field of great importance is the electrical properties of high-κ - silicon interface. The key parameters degrading surface mobility such as interface charges and surface roughness can not be adequately determined from capacitor structures. The amount of interface charge which is needed to significantly degrade the surface mobility will cause a very small shift in flat band voltage as observed on capacitor structures. Now many people have a major effort in fabricating and characterizing n - channel and p – channel FETs in order to evaluate these key interface parameters. Several device runs have shown very promising results with mobility vs. field curves approaching the values achieved with good thermal oxides. In other case, however, significant degradation in mobility has been observed due to either interface charges and/or surface roughness. By appropriately modeling the interface mobility, we can determine the major physical effects resulting in the mobility degradation.

A final field of great importance in the high-κ gate stack field is the reliability of the gate stack under voltage and temperature stress. Since good stack results have only recently begun to be obtained, only preliminary results are available on the potential reliability of complete high-κ gate stacks.

2.2 The Characteristics of High-κ Dielectrics

2.2.1 Introduction

Many materials systems are currently under consideration as potential replacements for SiO_2 as the gate dielectric material for sub-0.1 μm CMOS technology. A systematic consideration of the required properties of gate dielectrics indicates that the key guidelines foe selecting an alternative gate dielectric are (a) permittivity, band gap, and band alignment to silicon, (b) thermodynamic stability, (c) film morphology, (d) interface quality, (e) compatibility with the current or expected materials to be used in processing for CMOS devices, (f) process compatibility, and (g) reliability. Many dielectrics appear favorable in some of these fields, but very few materials are promising with respect to all of these guidelines,

In general, high-κ dielectrics often exhibit smaller band gap, weaker bond, and higher defect density than SiO_2. Fig. 2-2 shows the comparison of relevant properties for high-κ candidates. The high-κ dielectric with the same effective oxide thickness (EOT) with SiO_2 still shows lower leakage current than SiO_2 by several orders [2.9]. That is why high-κ dielectrics have drawn much attention for future technology.

Recently, some high-κ dielectrics have been widely studied and the characteristics and issues of those materials have also been reported. The high-κ dielectrics show good performances are always accompanied by another drawbacks. Issues to be discussed include processing, dielectric constant, capacitance, band gap, tunneling current, and reliability. Finding out the most suitable high-κ dielectrics for the use of device and altering the device structure or process to meet the requirement of the high-speed device are significant tasks to implant high k dielectrics to the next VLSI generation.

2.2.2 Processing and Thermal Budgets of high-κ material

An ideal gate dielectric would be formed directly on silicon without reacting with the silicon and metal electrode during deposition or subsequent processing at elevated temperatures in a standard CMOS fabrication process. The reaction of the dielectric with silicon during temperature cycles subsequent to deposition is governed by thermodynamics. Hubbard and Schlom performed an extensive theoretical study of thermodynamic stability of binary oxides in contact with silicon [2.10].

Binary oxides that were shown to be thermodynamically stable on silicon included Y_2O_3, ZrO_2, HfO_2 and Al_2O_3. Dielectrics such as TiO2 and Ta2O5 are not thermodynamically stable on silicon and thus form an interfacial layer [2.10]-[2.11]. Interaction of the dielectric with the polysilicon or metal gate electrode is also a large concern.

Although a dielectric may be thermodynamically stable in contact with silicon, an interfacial layer can still form during its deposition. Many materials that are stable on silicon, such as HfO_2 and ZrO_2, are efficient diffusers of oxygen so that post-deposition annealing in an oxidizing ambient can also cause the formation of an interfacial layer [2.12]. Such an interfacial layer has been identified as a silicon oxide or a silicate. It has been reported that NH_3-based interfacial layer can be effective in suppressing the diffusion of O_2 and the subsequent growth of silicon oxide [2.13]. In some studies it has been shown that a silicate interfacial layer can be beneficial in reducing interface trap density and improving reliability [2.14].

The formation of an interfacial oxide layer during deposition is dependent on kinetics and the relative reaction rates between the oxidation of silicon and the deposition of high-κ material, which is extremely dependent on the type of deposition process used. Another issue with high temperature annealing is crystallization. Although polysilicon materials may have undesired effects such as grain boundaries and roughness that impact on properties such as leakage current, it has been suggested that materials deposited in a perfectly crystalline form may be desirable [2.15].

2.2.3 Dielectric constant and capacitance

Approximate κ values for some representative gate dielectrics are shown in Fig. 2-2. These values of κ are very approximate because of the stacked nature of many of the films and of the close relationship of κ to properties such as crystallite and composition that are difficult to measure accurately. Many times, the κ of a bulk crystal is measured and used for the κ of a thin amorphous film of the material.

The capacitance density of a film depends not only on the κ and thickness of the material but also on that of an interfacial oxide layer. Fig. 2-3 shows equivalent oxide thickness for a stacked dielectric comprised of a layer of SiO_2 and a layer of a high- κ dielectric. EOT is the equivalent thickness of SiO_2 that would produce the same capacitance-voltage curve as that obtained from an alternate dielectric system. Dielectrics having EOTs as small as 1.0 nm have been developed. In order to achieve small EOTs, the interfacial oxide thickness must be controlled. The κ of the interfacial layer present in many dielectrics has been determined to be higher than that of pure SiO_2, presumably due to the presence of metal in the interfacial layer [2.11] or silicate formation [2.3].

2.2.4 Bandgap and Tunneling Current

Approximate bandgaps for some of the candidate high-κ gate dielectrics are also shown in Fig.2-2. Although bandgap is sometimes determined using optical measurements, the bandgap measured electrically may be different than that measured optically because optical transitions are almost exclusively direct. The electron tunneling current flowing through a dielectric depends not only on bandgap but on barrier height. Although a material may have a large bandgap, the conduction band offset between materials may be small [2.16]. Electrical bandgap tends to decrease with increasing κ resulting in tradeoffs associated with the tunnel current [2.16].

Results also suggest that it is more beneficial to have a material with a lower κ and a barrier height slightly larger than the expected supply voltage, than to have a material with a larger κ and a lower barrier height. This is due to the tunneling current being proportional to the area of the tunnel barrier which depends on the thickness of the material and its barrier height.

For gate dielectric stacks, modeling results indicate that the tunnel current depends strongly on injection polarity due to the asymmetry of the band diagram. Also, an interfacial oxide layer can significantly increase the tunneling current if the electrons tunnel through the oxide layer first [2.17].

Although much of the modeling of current through high-κ dielectrics assumed pure tunneling as the mechanism, most dielectrics exhibit some form of trap-assisted current [2.18]. As an example, Fig. 2-4 shows the temperature dependence of leakage current for a PECVD nitride film. The nitride film exhibits the temperature dependence stronger than that expected for pure tunneling, but weaker than the expected for Frenkel-Poole transport, which may suggest the trap-assisted phenomena.

2.3 The Choice of High-κ Dielectrics

2.3.1 Introduction

New high-κ materials that have been extensively discussed range from simple metal oxides like TaO_x and TiO_x that benefit from ease of processing to more complex materials such as $(Ba,Sr)TiO_3$ that have a higher dielectric constant but also present greater processing challenges. Here we extend the scope of materials considered to include new classes of mixed metal oxides that combine the improved dielectric properties of binary and ternary systems with the ease of processing of simple metal oxides. Some of the most exciting materials we have discovered include Ta-Al-O alloys for gate oxides, and we also use it for metal-insulator-metal capacitors.

Amorphous TaO_x has been used previously [2.19] to extend the scaling of SiO_2, but been found to crystallize during the rapid thermal anneals (RTA) used for dopant activation and interface state passivation in Si. The crystallites have lateral dimensions comparable to the gate length which can result in excessive surface roughness and fluctuations in threshold voltage. This crystallization transition also results in excessive growth of SiO_2 at the a-TaO_x/Si (a-TaO_x: amorphous TiO_x) and the a-TaO_x/poly-Si interface (Fig. 2-5) and can lead to deterioration of the gate capacitance (Fig. 2-6).

We have found that the crystallization transition can be suppressed by adding Al or Si to the a-TaO_x film, as shown in Fig. 2-7. The electrical properties of $Ta_{1-y}Al_yO_x$ for $0.1 < y < 0.4$ are superior to those of undoped TaO_x (Fig. 2-8) although the dielectric constant is can be reduced (Fig. 2-9). The concentrations of Al required to improve the thermal stability and electrical properties should not significantly effect the dielectric constant.

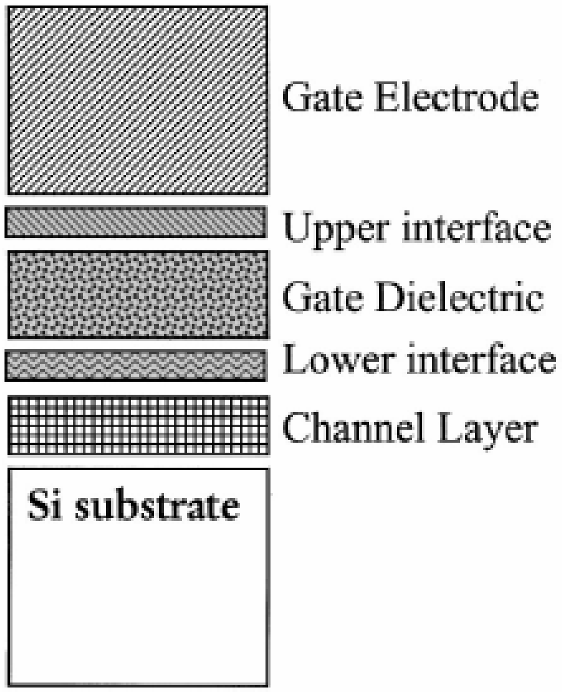
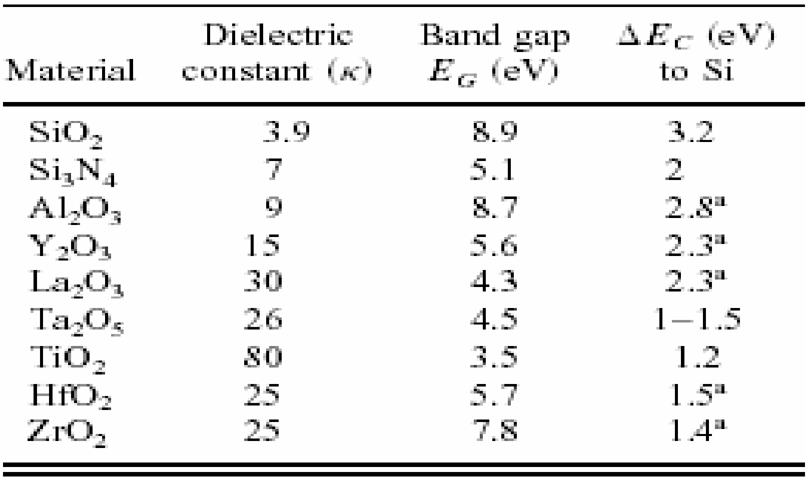


Fig. 2-1. Schematic of important regions of a field effect transistor gate stack [2.20].



Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si
SiO_2	3.9	8.9	3.2
Si_3N_4	7	5.1	2
Al_2O_3	9	8.7	2.8[a]
Y_2O_3	15	5.6	2.3[a]
La_2O_3	30	4.3	2.3[a]
Ta_2O_5	26	4.5	1–1.5
TiO_2	80	3.5	1.2
HfO_2	25	5.7	1.5[a]
ZrO_2	25	7.8	1.4[a]

Fig. 2-2. Comparison of relevant properties for high-κ candidates [2.20].

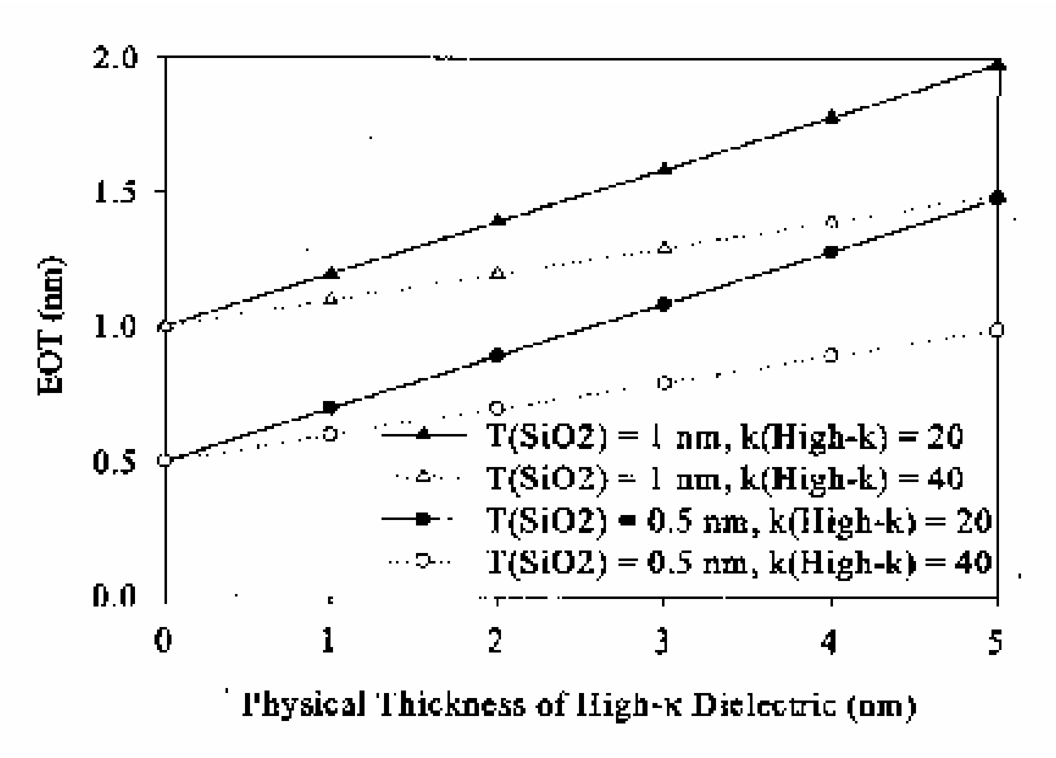


Fig. 2-3. EOT for a stacked dielectric comprised of a high-κ dielectric and SiO_2 [2.21].

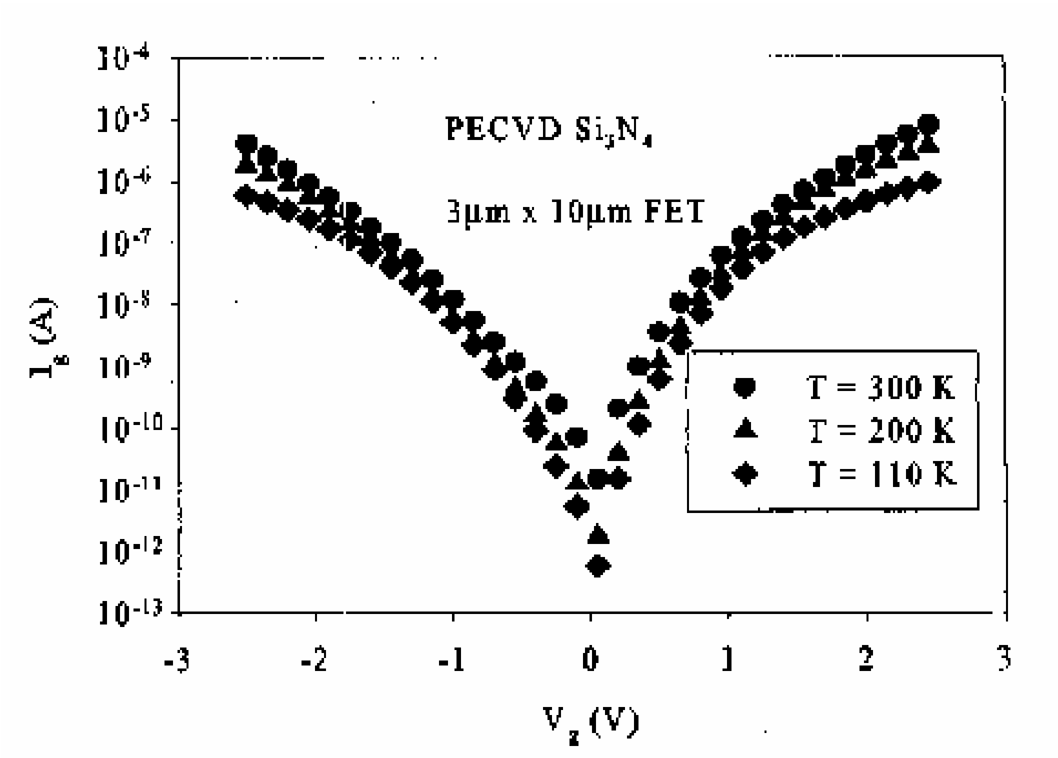


Fig. 2-4. Gate current density for a film at several measurement temperatures [2.21].

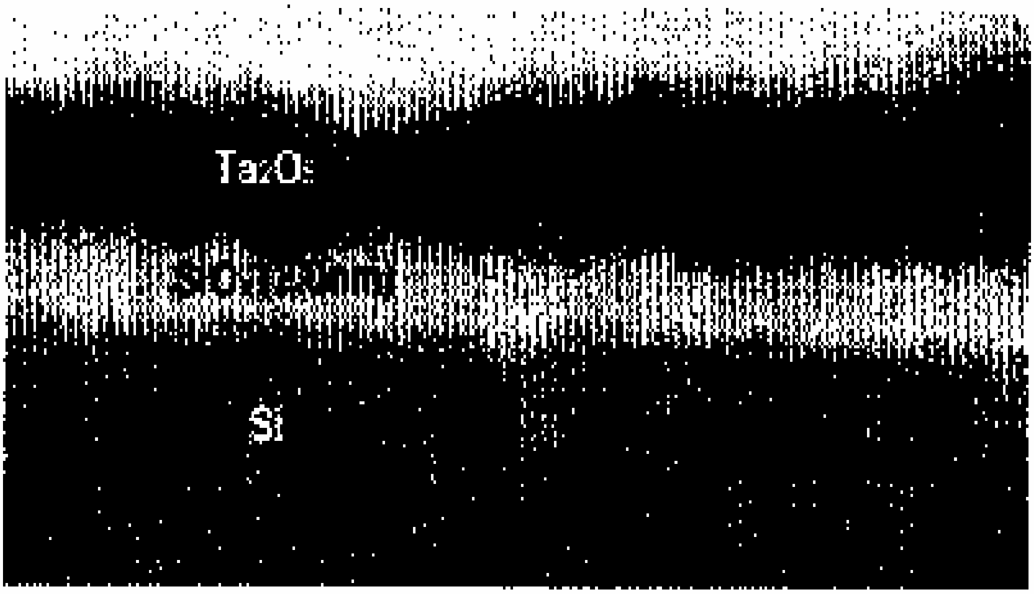


Fig. 2-5. TEM cross section of 7 nm Ta_2O_5 on silicon. The 2.0 nm film is a $SiTa_xO_y$ interfacial region [2.22].

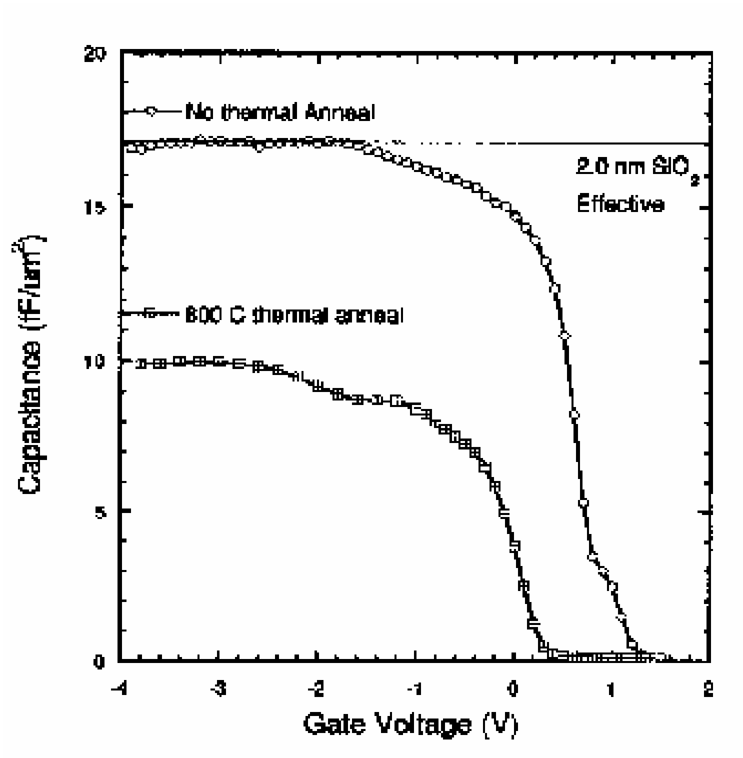


Fig. 2-6. Reduction of gate capacitance due to formation of SiO_2 interfacial layer after 800°C crystallization [2.22].

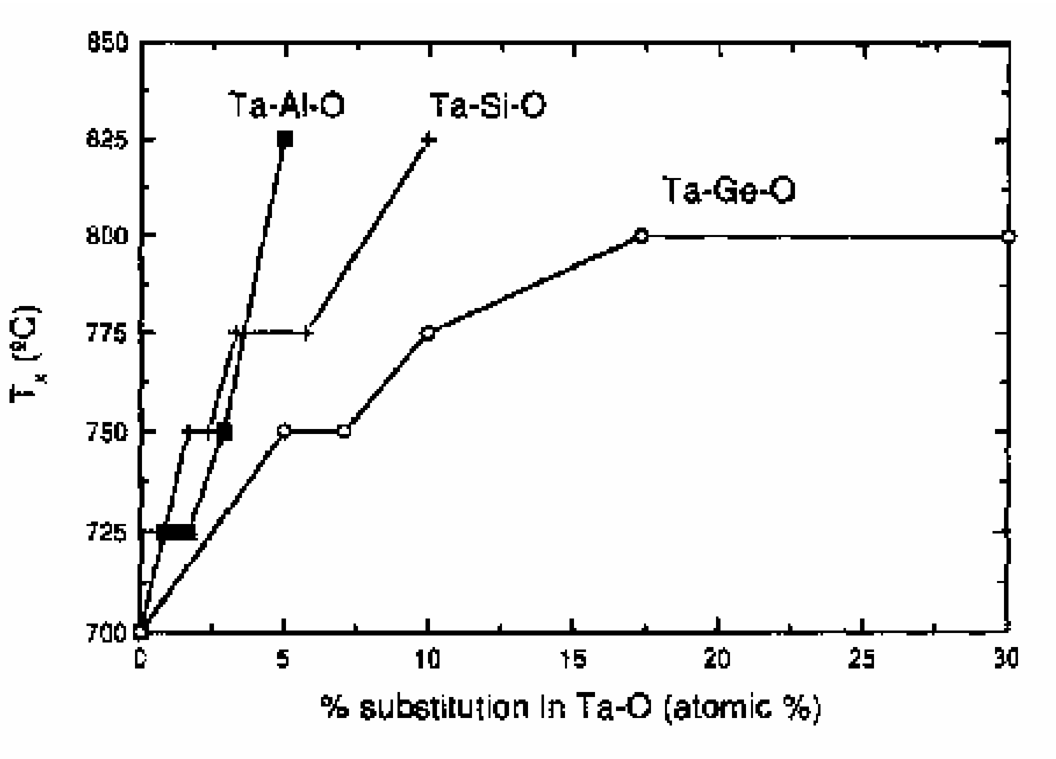


Fig. 2-7. Crystallization temperature of Ta-M-O as a function of Al, Si, or Ge content. A very strong increase in T_x with Al content is observed [2.22].

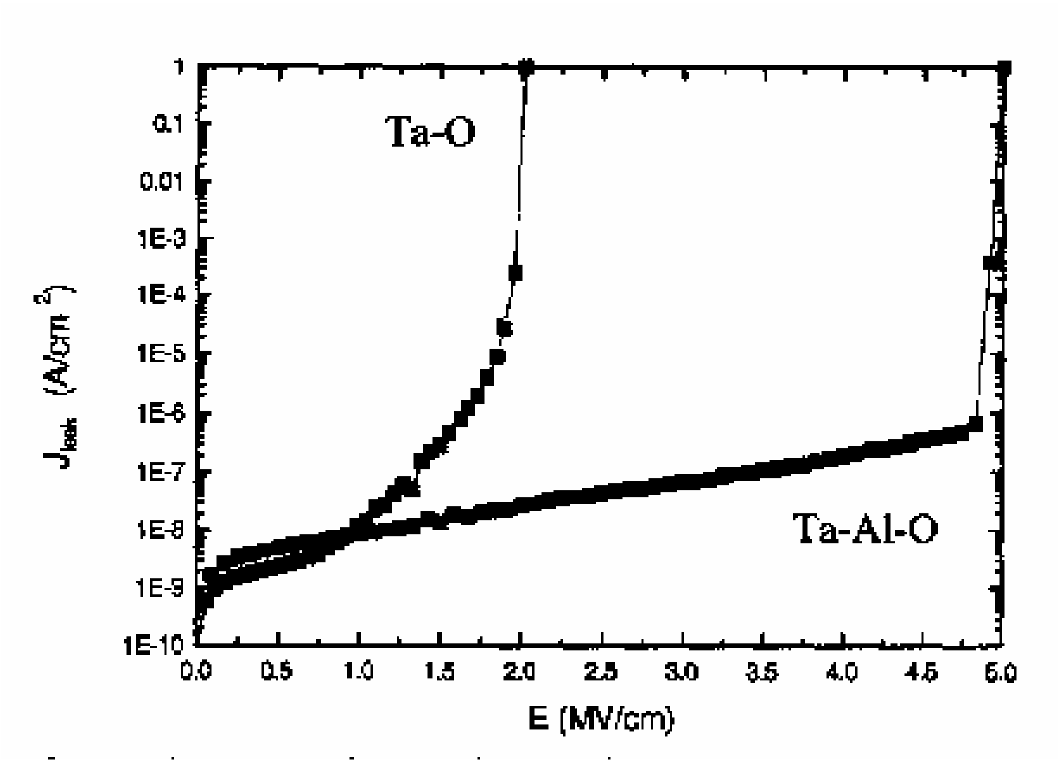


Fig. 2-8. Current-voltage relations for Ta-Al-O showing the improvement of electrical properties of Ta_2O_5 with addition of Al [2.22].

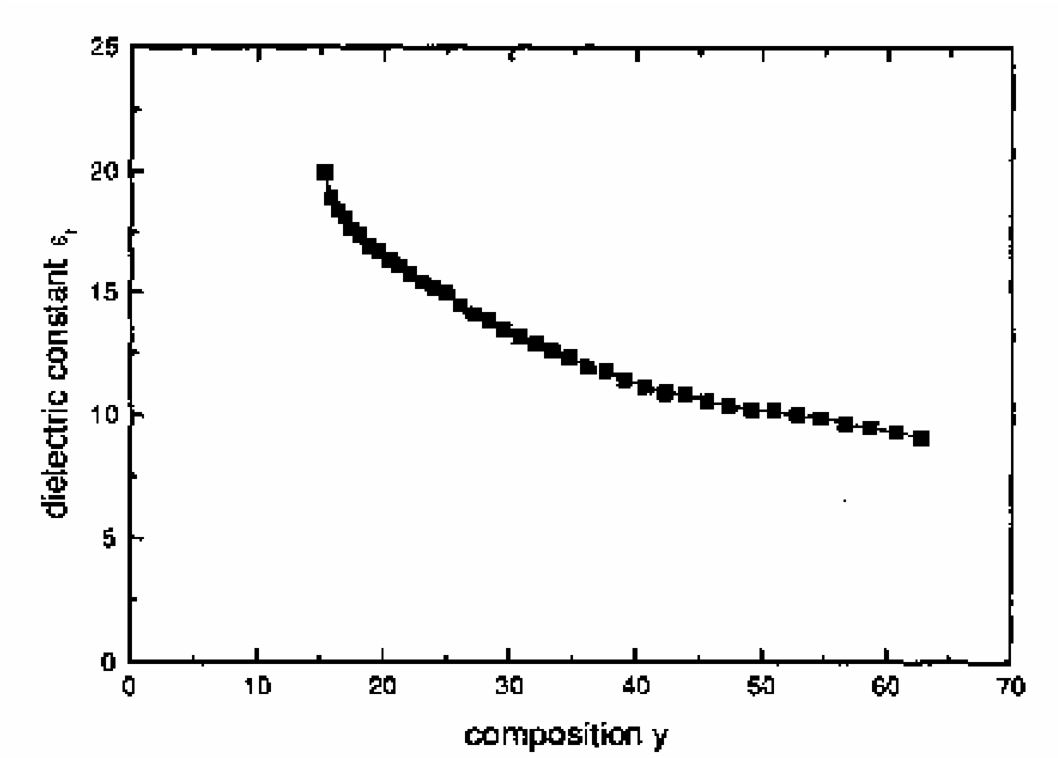


Fig. 2-9. Dielectric constant of Ta-Al-O as a function of Al concentration in the sputtered films [2.22].

Chapter 3

Experimental Procedure of High-κ MIM Capacitor with Al doped TaO_x Dielectrics

3.0 Microwave Layout Rules for On-wafer Measurement

◆ Mechanical

1. GSG Configuration

Metal pads must be laid out with ground-signal-ground (GSG) probe configuration as shown in Fig. 3-1.

2. Pad Pitch：

All pads contacted by an individual probe must be collinear with a constant center-to-center pad pitch of 150 μm as shown in Fig. 3-2.

3. Pad Size

The minimum pad size is 50μm × 50 μm as shown in Fig. 3-2.

4. Passivation Window

The minimum passivation window size is 96μm × 96 μm. The passivation window must be larger than the probe contact. If the pad metalization is above the final passivation layer, this rule does not apply.

5. Parallel-Row Pad Spacing

The minimum center-to-center pad spacing between facing probes is 150 μm as shown in Fig. 3-2. Note that this spacing is based on the assumption of 750 μm of probe vertical overtravel.

6. Pad Height Variation

The minimum pad height variation in a row of pads contacted by one probe is 0.5 μm.

7. Planarity Requirements

The maximum overall planar deviation of a row of pads contacted by one probe, with respect to the backside of the substrate is 2/1000.

◆ **Electrical**

Maximum Rated Current

The maximum dc current in port 1 is 0.1 ampere while that in port 2 is 0.5 ampere and the maximum dc current per contact is 0.5 ampere.

3.1 The Fabrication Process Flow of Al doped TaO_x MIM Capacitors

The MIM capacitors were fabricated using 4-in p-type or n-type Si wafers. To integrate the high-κ capacitors into VLSI backend process, we started with 500 nm isolation oxide deposition on Si wafers by Wet Oxide furnace. The bottom electrode of MIM capacitor was formed by Electron-gun (E-gun) on the isolation oxide using Pt/Ti (Pt/Ti = 90nm/10nm) bi-layer metals as shown in Fig. 3-3. The bottom electrode was also patterned using Lift-off technology to form the coplanar transmission line for RF measurement. A plasma-enhanced chemical vapor deposition (PECVD) passivation oxide was deposited for isolation and followed by patterning the active capacitor region as shown in Fig. 3-4. Then high-κ Al doped TaO_x was formed by depositing Al and Ta (Al:Ta = 1:8) metals on Pt electrode followed by oxidation at 400 ^oC [3.1] for 45 min and subsequent annealing for 15 min. The above process fits well the low thermal budget requirement of current VLSI backend integration. Various different thicknesses from 11.5 to 25.5 nm are formed and confirmed by ellipsometer measurement. The reason for doping AlO_y into TaO_z is to preserve the merit of good MIM capacitor integrity by adding Al_2O_3 dielectric. Addition of Al_2O_3 [3.2] to Ta_2O_5 reduces the leakage current, although this results in a slightly lower κ-value [3.3]-[3.4]. Then via hole was patterned shown in Fig. 3-5. Finally, Al metal was deposited on high-κ dielectrics followed by patterning to form the top electrode of MIM capacitor and coplanar transmission line for RF measurements shown in Fig. 3-6. The typical MIM capacitor area is 50 μm × 50 μm. Fig. 3-7 and Fig. 3-8 show the MIM capacitor cross-section view and layout view, respectively.

The detailed fabrication process flow is listed as follows：

1. (100) orientation n-type or p-type Si wafer.
2. Initial cleaning (RCA clean).

3. Thermal wet oxidation at 1036 ^{o}C to grow 500 nm thermal SiO2 in furnace.

4. Depositing Pt/Ti (Pt/Ti = 90nm/10nm) bi-layer metals, Ti first, by E-gun, then employing Lift-off technology.

5. A PECVD passivation oxide 100nm was deposited for isolation and followed by patterning the active capacitor region.

6. Then high-κ Al doped TaO_x was formed by depositing Al and Ta (Al:Ta = 1:8) metals on Pt electrode.

7. Following by oxidation at 400 ^{o}C for 45 min and subsequent annealing for 15 min in furnace.

8. Then via hole was patterned.

9. Finally, Al metal was deposited on high-κ dielectrics by thermal coater followed by patterning to form the top electrode of MIM capacitor and coplanar transmission line.

3.2 The Measurement of Al doped TaO_x MIM Capacitors

The high-κ MIM capacitors were characterized using an HP4284A precision LCR meter from 10 KHz to 1 MHz. Above 1 MHz the S-parameters (Fig. 3-9) were measured using an HP8510C network analyzer (from 200 MHz to 20 GHz). Additional “OPEN” dummy device [3.5] shown in Fig. 3-10 were measured to de-embed the parasitic capacitance in the RF layout of the MIM capacitor. A similar method was used for RF noise analysis in 0.18 to 0.13 μm MOSFETs [3.6]. So the measured S-parameters were de-embedded from a dummy device and the RF frequency capacitance plus parasitic parameters were extracted using an equivalent circuit model shown in Fig. 3-11. The parasitic pad, series inductor and resistor in transmission line are de-embedded from a same line length through transmission line [3.7]-[3.8].

3.3 De-embedding Theory

When circuits or devices work at high frequencies, many parasitic effects will happen. For example, a signal applied on one metal line, the potential of this metal line at any point is equal if the wavelength of signal is long enough, compared with metal line. But the potential of the metal line at any potential will be different when the wavelength of signal can compare with the metal line or shorter, i.e. high frequency signal. Hence, a metal line was regarded as a resistor at low frequency or resistor plus parasitic inductance and capacitance parameters at high frequency in an equivalent circuit model. In order to measure this MIM capacitance, we must layout additional probe pads and signal lines for measurement. However, these added potions will generate additional parasitic effects. So we must de-embed these parasitic parameters to get the intrinsic high frequency capacitance. Fig. 3-12 shows the equivalent circuit of a RF MIM capacitor device at high frequency.

As devices were measured approach microwave frequency, we can not directly measure the lump circuit components, like RLC (resistance, inductance and capacitance), because of parasitic effects. Scattering-parameters (S-parameters) were obtained in general [3.9]. According to microwave theorem [3.9], we can transform the S-parameters into an equivalent circuit model to extract the component that we want.

Among added portions for measurement, the parasitic capacitance effects dominate in probe pads. We can transform both of the measured S-parameters of MIM capacitors and “OPEN” dummy device into admittance parameters (Y-parameters). Then we de-embed the parasitic capacitance effects form the MIM capacitor by Y_{MIM}-Y_{OPEN}. So we can get the de-embedded S-parameters from the transformation of de-embedded Y-parameters. We have de-embedded the parasitic shunt capacitance effects due to the probe pads of MIM capacitor. Then, we use an equivalent circuit method to simulate the de-embedded S-parameter shown in Fig. 3-9 to extract each components of the equivalent circuit model shown in Fig. 3-11 by Series Ⅳ. From this, we can obtain the RF capacitance of MIM capacitor.

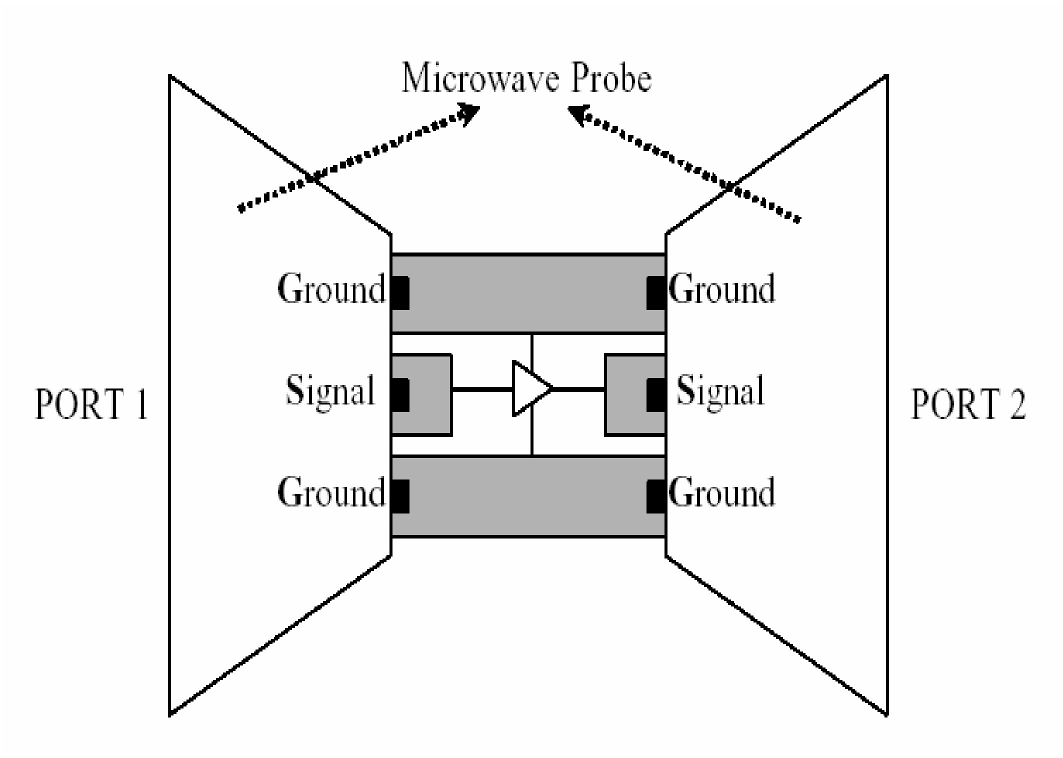


Fig. 3-1. Typical layout suitable for coplanar probing with ground-signal-ground (GSG) probe configuration

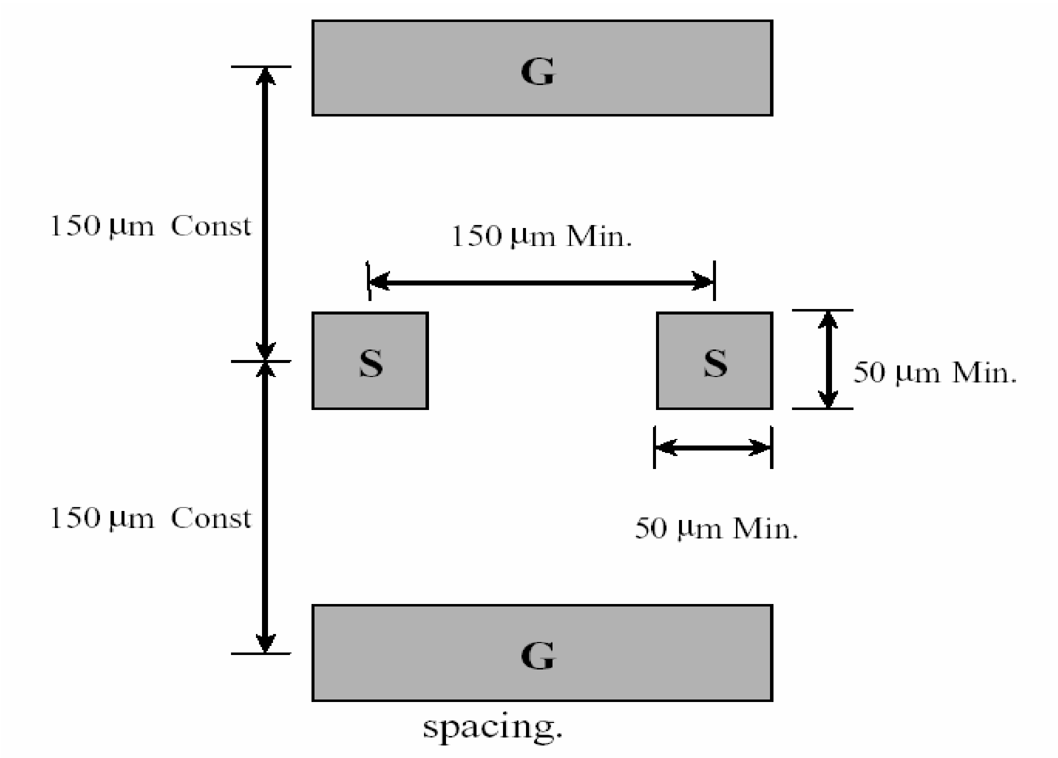


Fig. 3-2. Constant pitch, minimum pad size and minimum parallel-row pad.

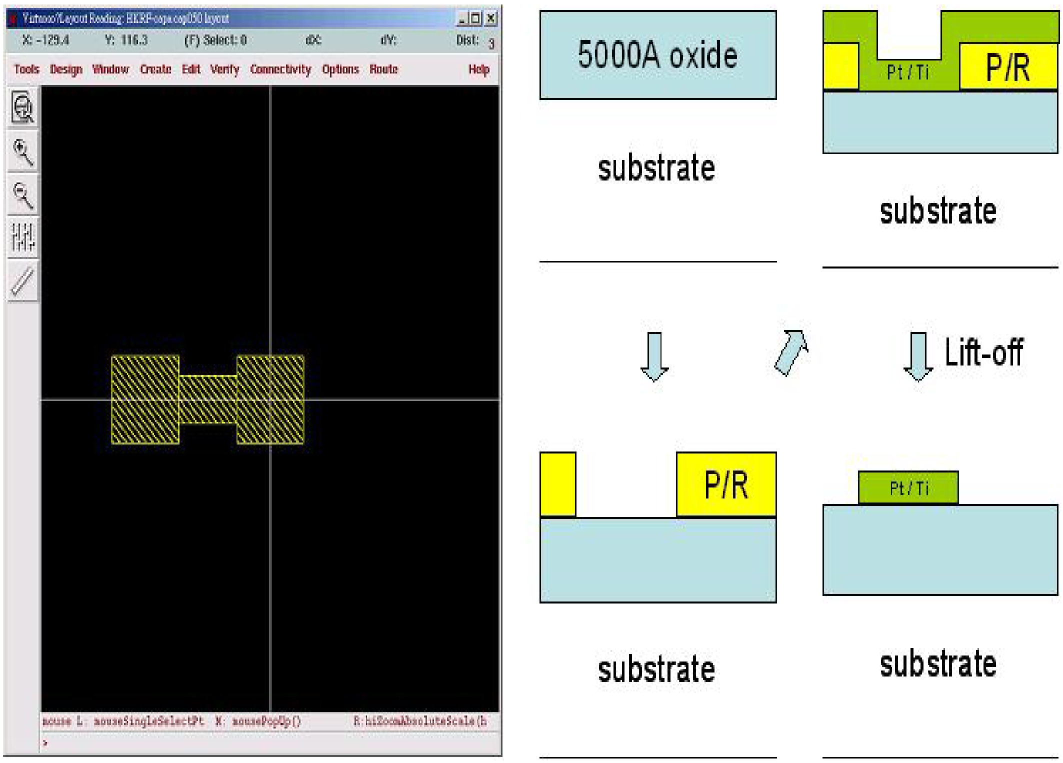


Fig. 3-3. Mask #1 (bottom electrode) of layout and process flow of the RF MIM capacitor.

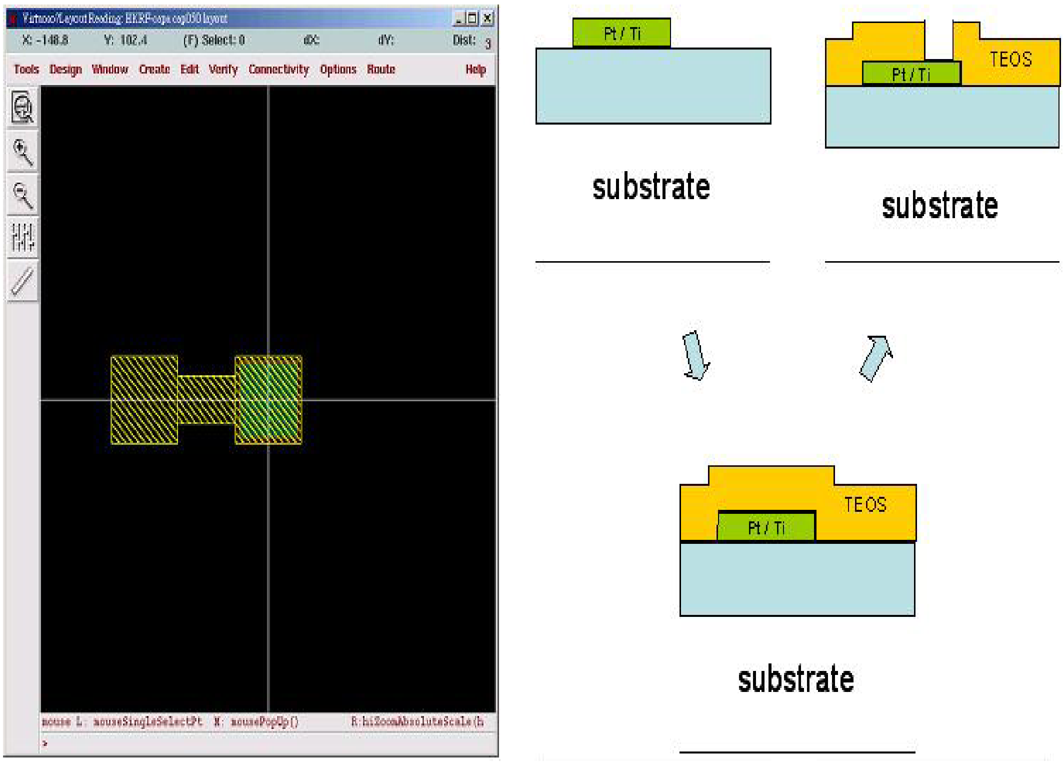


Fig. 3-4. Mask #2 (Active Region) of layout and process flow of the RF MIM capacitor.

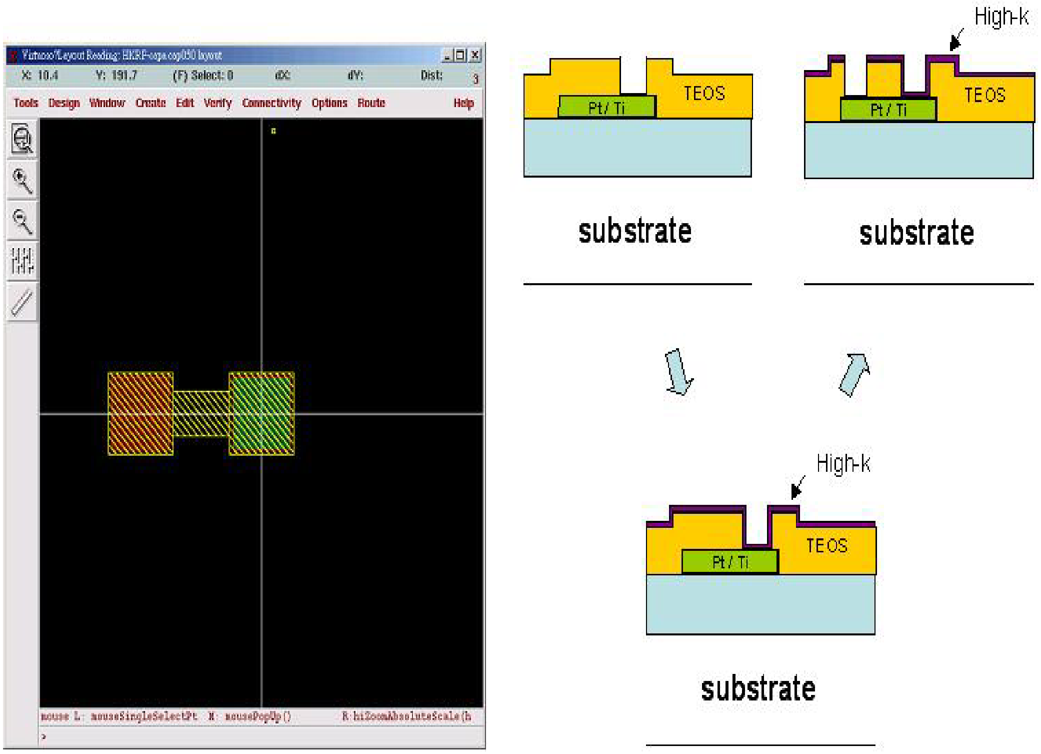
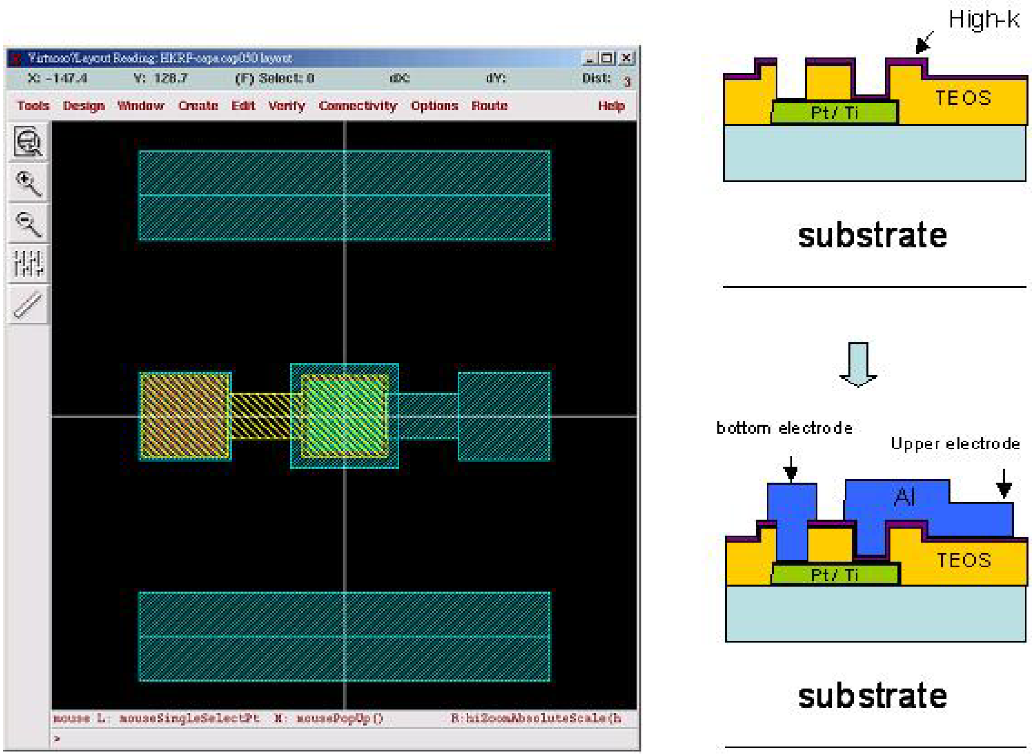


Fig. 3-5. Mask #3 (Via hole) of layout and process flow of the RF MIM capacitor.



```
mouse L: mouseSingleSelectPt  M: mousePopUp()        R:hiZoomAbsoluteScale(h
>
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Fig. 3-6. Mask #4 (upper electrode) of layout and process flow of the RF MIM capacitor.

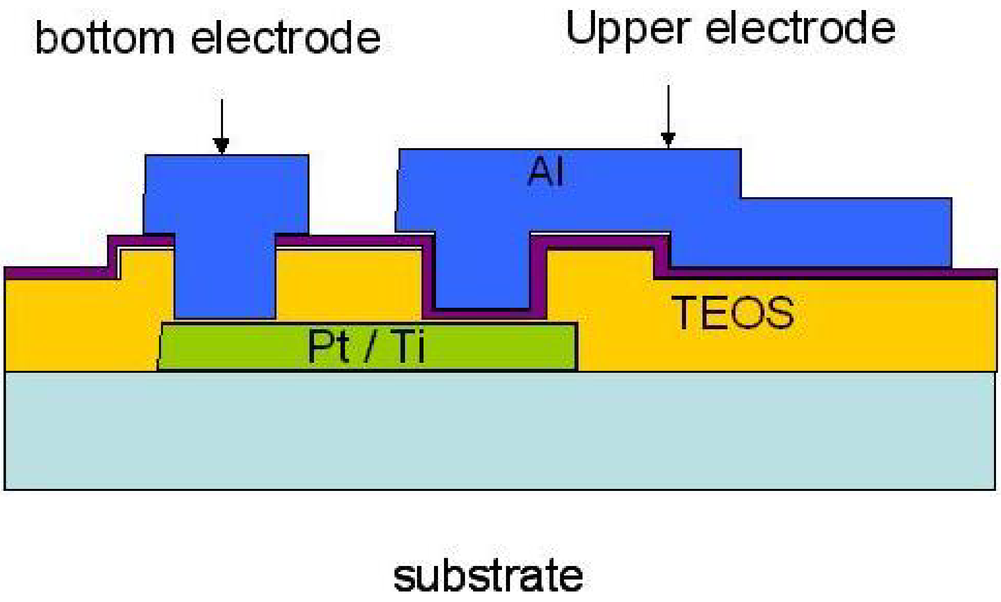


Fig. 3-7. The RF MIM capacitor cross section view.

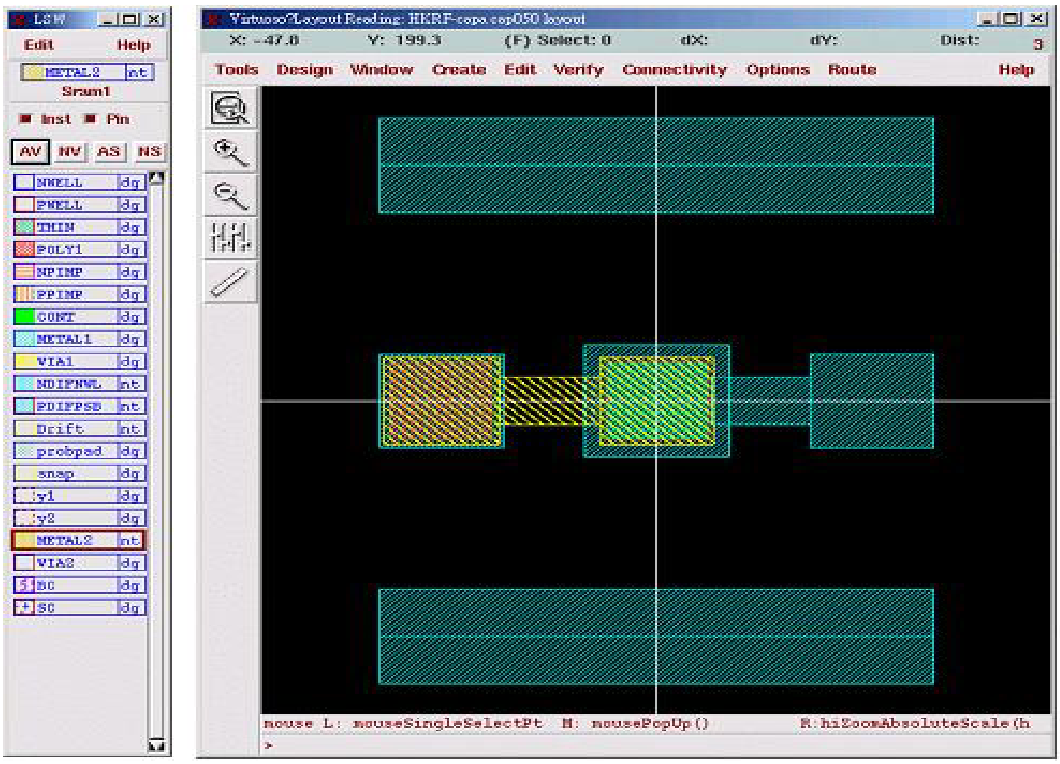


Fig. 3-8. The RF MIM capacitor layout view.

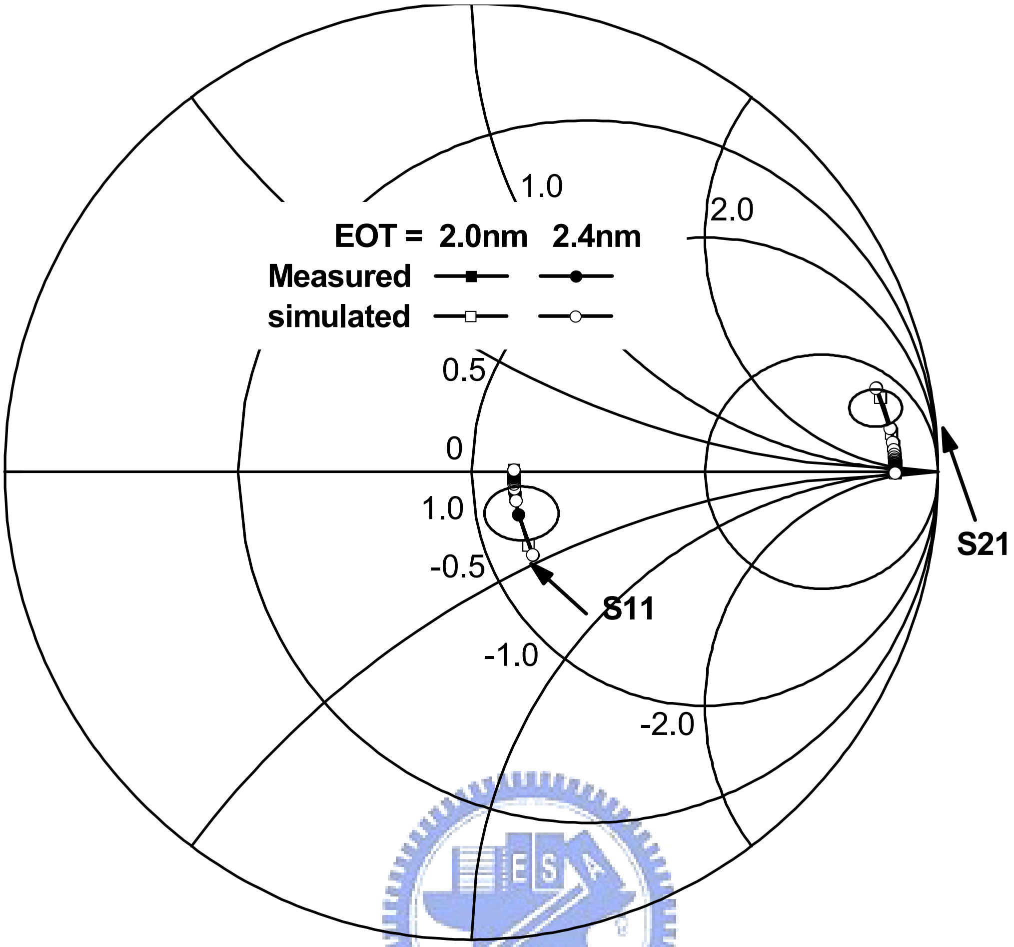


Fig. 3-9. Measured and simulated scattering parameters of 2.0 and 2.4 nm EOT Al doped TaO_x MIM capacitors.

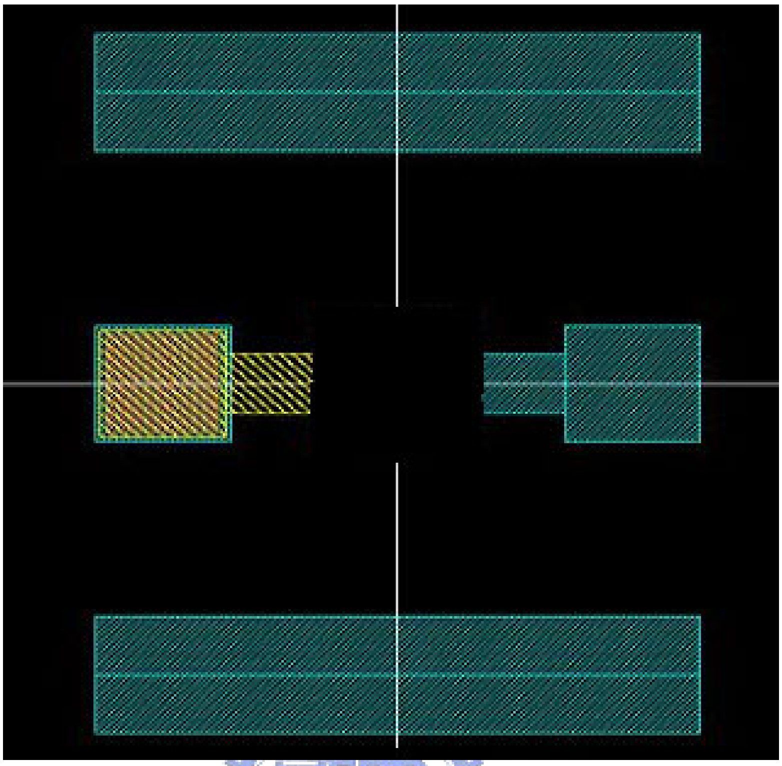


Fig. 3-10. The "OPEN" dummy structure for the device under test (DUT) modeled in the shunt configuration.

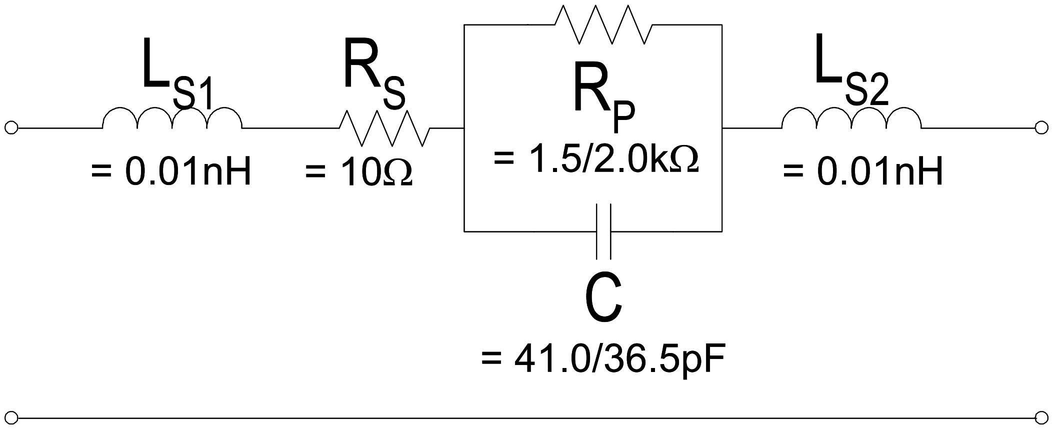


Fig. 3-11. The equivalent circuit model and numerical values of elements for capacitor simulation at RF regime.

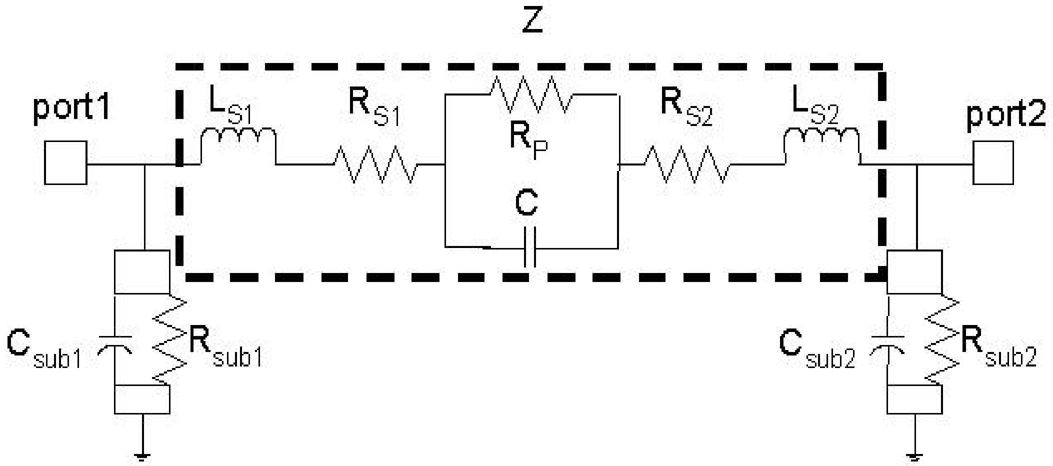


Fig. 3-12. The equivalent circuit model of MIM capacitor at RF regime.

Chapter 4

The Characteristics of High-κ MIM Capacitor with Al doped TaO_x Dielectrics

4.1 Capacitor Characteristics

For precision analog circuit applications, the MIM capacitors need to be useful over wide range of frequencies. To further study the RF frequency characteristics, we have measured the S-parameters up to 20 GHz. Fig. 4-1 shows the measured (de-embedded) and modeled S-parameters for Al doped TaO_x MIM capacitors, where the modeled data is from the equivalent circuit model shown in Fig. 4-2. The R_S, L_S, R_P, and C in the model are the parasitic series resistor, series inductor, parallel resistor, and capacitor, respectively. Good agreement between measured and modeled data is obtained that suggesting the good accuracy of physically based equivalent circuit model for both capacitors with different thickness, which can be used for capacitance extraction.

The capacitance values were measured directly using the LCR meter from 10 KHz to 1 MHz and calculated from the measured (de-embedded) S-parameters up to 20 GHz using the equation [4.1]:

$$\frac{\Delta C}{C} = \frac{Z_0(2 + Z(C)/Z_0)^2}{2R_P^2} j\omega C^2 (R_P + 1/j\omega C)^2 \Delta(S_{21}) \qquad (1)$$

$$Z(C) = R_S + j\omega(L_{S1} + L_{S2}) + \frac{R_P / j\omega C}{R_P + 1/ j\omega C} \qquad (2)$$

$$S_{21} = \frac{2}{2 + Z(C)/Z_0} \qquad (3)$$

We can use the equation (1) to derive the capacitance densities at different frequencies. Z(C) in equation (2) is the total impedance in the equivalent circuit model of Fig. 4-2 and Z_0 is the characteristic impedance of transmission line. The RF frequency ΔC/C in equation (1) is obtained by differentiating the measured S_{21} in equation (3), where shows the relation between the S_{21} and total impedance Z(C). Fig. 4-3 shows that the derived ΔC/C decreases rapidly with increasing frequency, which is advantageous for high frequency analog/RF circuits.

Figs. 4-4 and 4-5 show the C-V characteristics and ΔC/C for Al doped TaO_x MIM capacitors with physical thickness of 11.5 and 14.0 nm, respectively. Capacitance densities at RF regime have been extracted in pervious work using equivalent modeling circuit fitting from measured S-parameters [4.2]-[4.4] and are also plotted in the figure. At 100 kHz frequency, high capacitor density of 17 and 15 fF/μm^2 are measured for 11.5 and 14 nm respectively, and a κ value of 22 is obtained for Al doped TaO_x dielectrics. The equivalent-oxide thickness (EOT, $t_{eq}=\kappa_{ox}*t_{high-\kappa}/\kappa_{high-\kappa}$) values for these high-density capacitors are calculated to be 2.0 and 2.4 nm for 11.5 and 14.0 nm physical dielectric, respectively. Fig. 4-6 shows the J-V characteristics of Al doped TaO_x MIM capacitors. The asymmetrical J-V and breakdown voltages under positive and negative bias are due to the different work function of top Al and bottom Pt electrodes. The leakage current is increased by trading off the increasing capacitance density, and values of 4.5×10^{-7} and 8.9×10^{-7} A/cm^2 are measured at -2 V for respective EOT of 2.4 and 2.0 nm. The leakage current, 8.9×10^{-7} A/cm^2, is low enough for circuit applications. This arises because the high capacitor density requires using only a small area. This is shown by the small leakage current of 5.2×10^{-12} A of a large 10 pF capacitor, which is even smaller than the leakage current of a 0.13-μm MOSFET [4.5]. Note that ΔC/C in Fig. 4-3 decreases with increasing frequency. This is an advantage at the high operational frequencies of analog/RF circuits.

Fig. 4-7 shows the frequency dependence of both the capacitance and Q-factor for high-κ Al doped TaO_x MIM capacitors. Below 1 MHz, the Q-factor was derived from the measured loss tangent using 1/tanδ. At higher frequencies an equivalent circuit model was used to determine the C value and the Q-factor from the measured S-parameters.

Only a small capacitance reduction (5%) occurs from 10 KHz to 10 GHz, which is attractive for RF applications. The Q-factor increase up to ~ 8 GHz is due to the resonance of the MIM capacitor with a parasitic inductor. The relatively low resonant frequency of ~8 GHz arises from the very large capacitance (42.5 pF) and the residual inductance, even after de-embedding. A Q-factor of ~ 40 before resonance for the 17 fF/μm^2 capacitors is a desirable characteristic. The high capacitance density, low leakage current, small frequency dependence and good Q-factor for these Al doped TaO_x MIM capacitors are useful and important for analog and RF circuit applications.

4.2 The Normalized Capacitance Variation ΔC/C and Voltage Coefficient of Capacitance VCC

To further study the frequency dependence of ΔC/C and related quadratic VCC (α), we have plotted ΔC/C and α as a function of frequency in Fig. 4-8. The relation between α and ΔC/C is expressed in the following equation:

$$\frac{\Delta C}{C}\times 10^6 = \left[\frac{C(V)-C(0)}{C(0)}\right]_{ppm} = \alpha V^2 + \beta V \tag{4}$$

The β is the linear VCC, which is less important than α by using circuit cancellation method [4.6]. Again, the ΔC/C and α decrease monotonically with increasing frequency. Small ΔC/C ≤ 120 ppm and α ≤ 280 ppm/V^2 are obtained with increasing frequency into GHz regime indicating that the high-κ MIM capacitors can be used for precision circuits with GHz operation frequency. Such high frequency is required since the operation speed of MOSFET continuously increases with device scaling down and the commercially available CPU circuit is already several GHz.

We have also plotted the ΔC/C and α as a function of 1/C (or equivalent to t_d since $1/C=t_d/\varepsilon_0\kappa$) in Fig. 4-9. Both ΔC/C and α decrease with increasing frequency similar to the trend shown in Fig. 4-8. In addition, the ΔC/C and α decrease with increasing ln(1/C) or ln(t_d) regardless the using different high-κ dielectrics [4.7]. Although the detailed physics to explain such dependence is still under investigation, possible reason may be related to the leakage current through dielectric and/or carrier trapping or de-trapping inside the high-κ dielectric.

4.3 The Temperature Coefficient of Capacitor TCC

In additional to the requirement of small ΔC/C and α dependence on voltage, the small TCC is another important factor for precision analog circuit application. Figs. 4-10 and 4-11 show the respective ΔC/C versus temperature and TCC of the Al doped TaO_x capacitors at different frequencies with two different dielectric thicknesses of 3.3 and 4.8nm EOT. The temperature dependent ΔC/C decreases with increasing frequency that is consistent with the decreasing trend in Fig. 4-8. The ΔC/C in both high-κ capacitors increases with increasing temperature that shows the same trend with other dielectric capacitors published in the literature [4.8].

We have further plotted the TCC as a function of 1/C (or equivalent to t_d) in Fig. 4-12 from the measured temperature dependence on ΔC/C. The TCC is also higher at thinner thickness and decreases monotonically with increasing frequency from 10 kHz to 1 MHz. It is noticed that the TCC in both high-κ dielectrics decreases rapidly with increasing ln(1/C), and the extrapolated data is close to previous TCC data of HfO_2 [4.7] at the same 1/C. Such exponential dependence of TCC on 1/C or t_d is similar to the dependence of $\Delta C/C$ and α on ln(1/C) in Fig. 4-9. Although the physical meanings are currently under study, possible reason may still be related to the leakage current through dielectric and/or carrier trapping or de-trapping inside the high-κ dielectric due to their temperature dependence in physics.

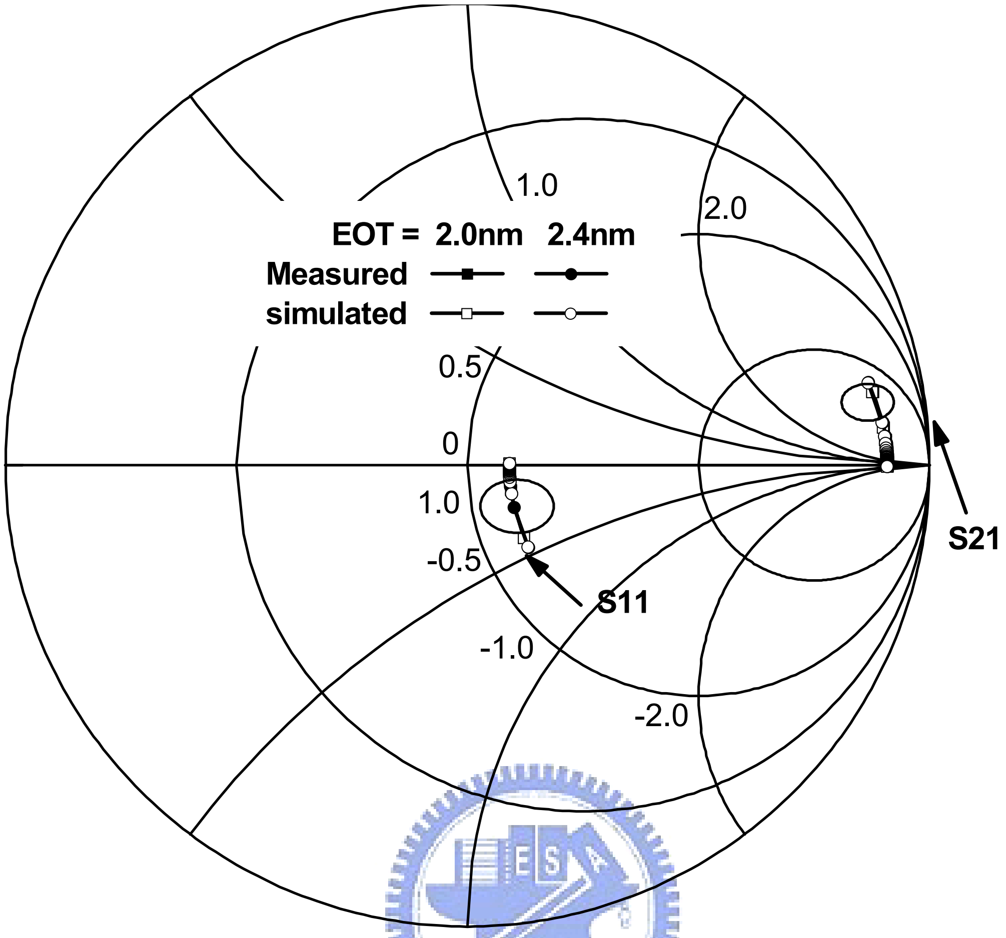


Fig. 4-1. Measured and simulated scattering parameters of 2.0 and 2.4 nm EOT Al doped TaO_x MIM capacitors at RF regime.

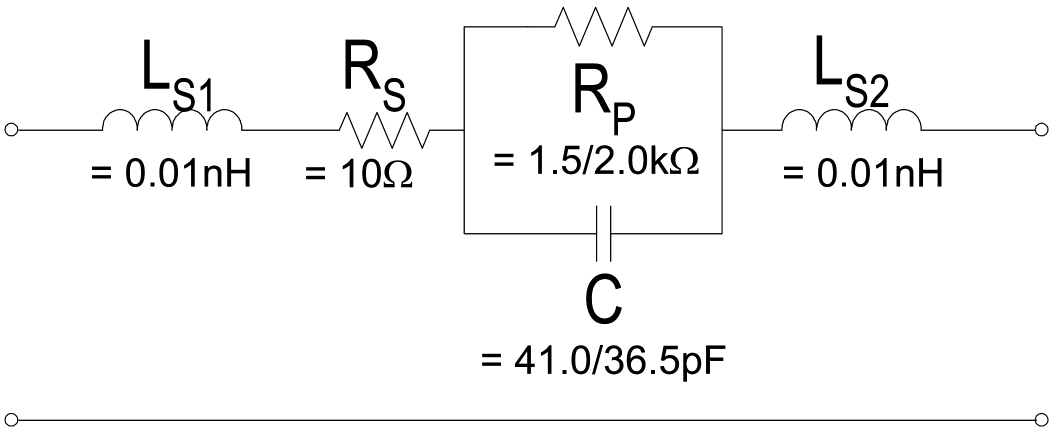


Fig. 4-2. The equivalent circuit model and numerical values of elements for capacitor simulation at RF regime.

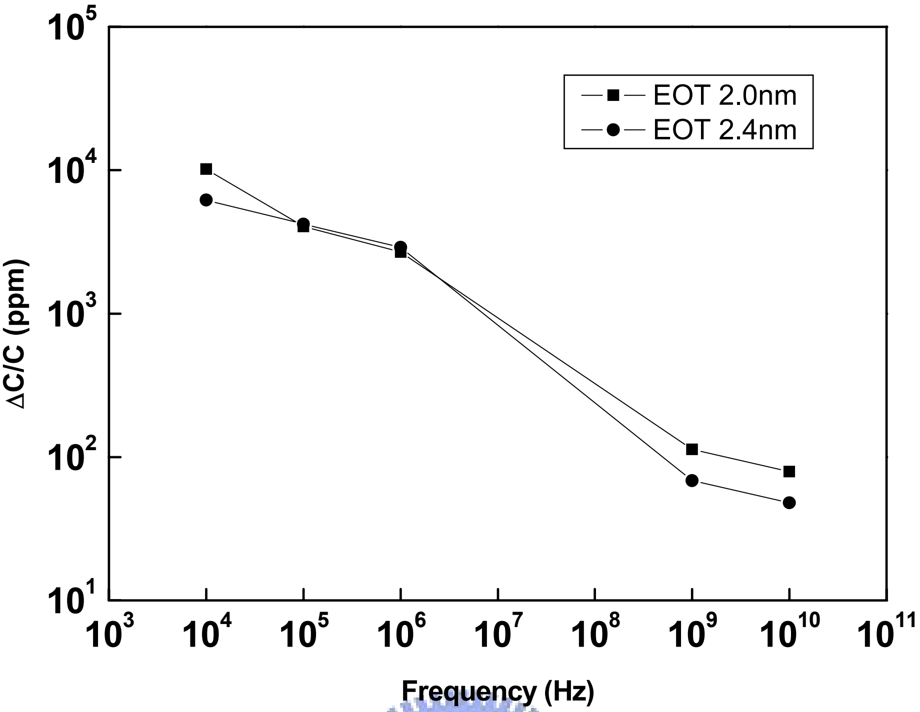


Fig. 4-3. The ΔC/C of Al doped TaO_x MIM capacitors as a function of frequency. It is notice that the ΔC/C decrease with increasing frequency.

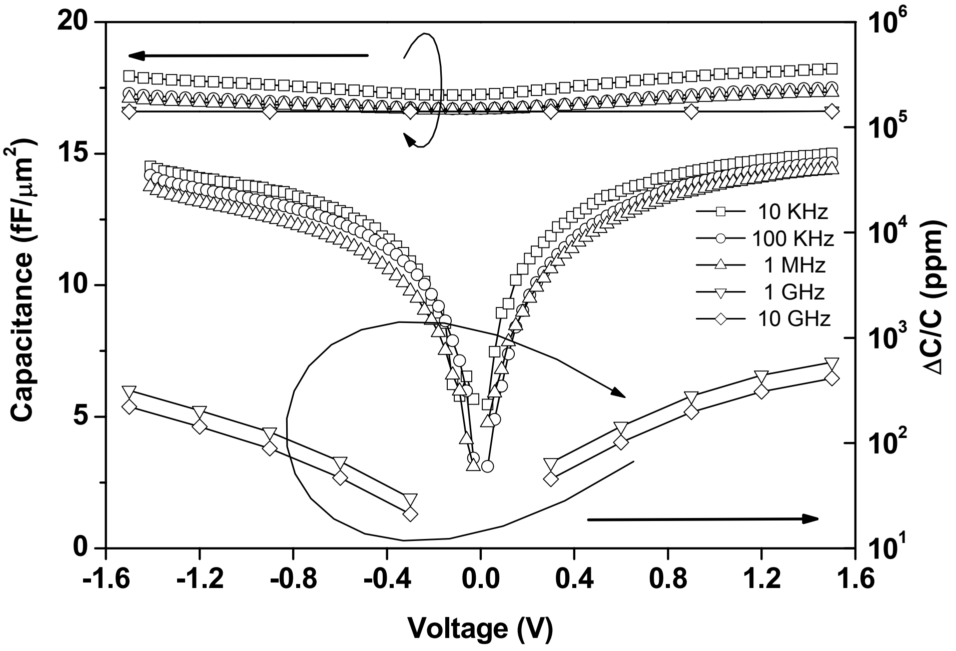


Fig. 4-4 C-V and ΔC/C-V characteristics of MIM capacitors with 2.0 EOT Al doped TaO_x dielectrics at different frequencies from 10 KHz to 10 GHz. The voltage is applied to the bottom Pt electrode. Measured area is 50mm × 50mm.

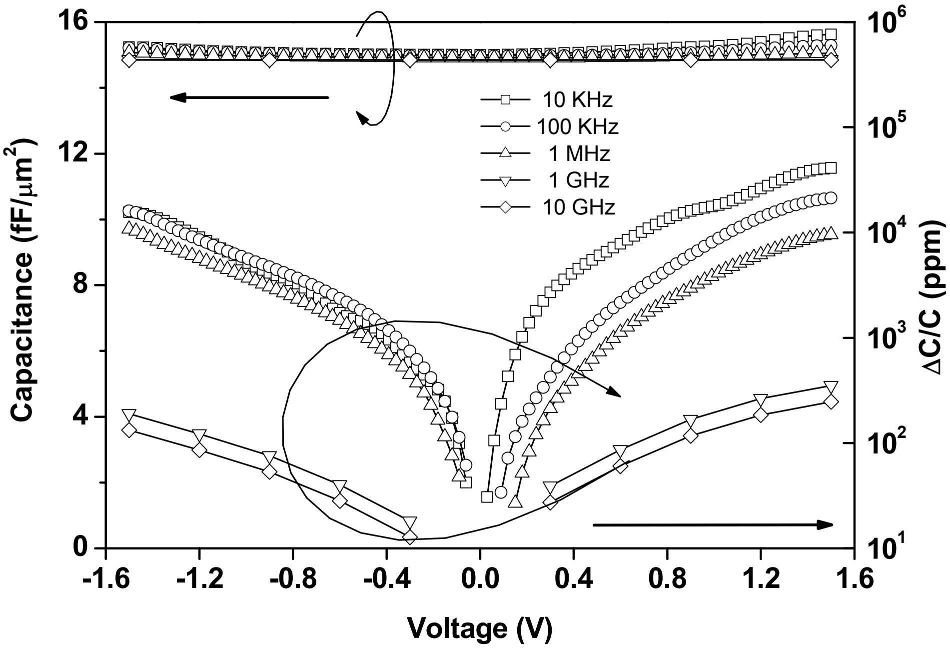


Fig. 4-5. C-V and ΔC/C-V characteristics of MIM capacitors 2.4 nm EOT Al doped TaO_x dielectrics at different frequencies from 10 KHz to 10 GHz. The voltage is applied to the bottom Pt electrode. Measured area is 50mm × 50mm.

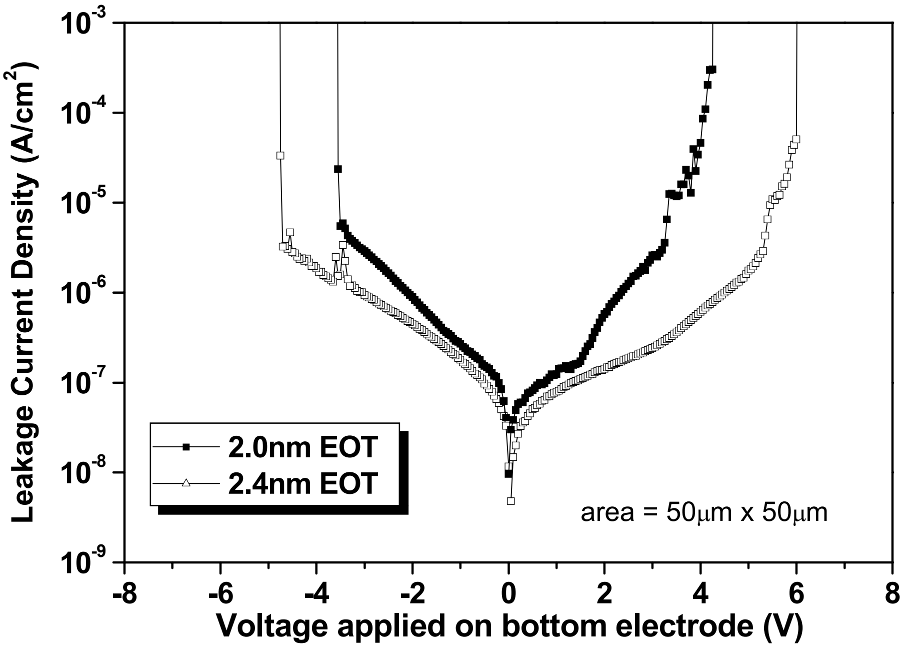


Fig. 4-6. J-V characteristics of 2.0 and 2.4 nm EOT Al doped TaO_x MIM capacitors. The asymmetric J-V and breakdown voltages are due to the different bottom Pt and top Al electrodes.

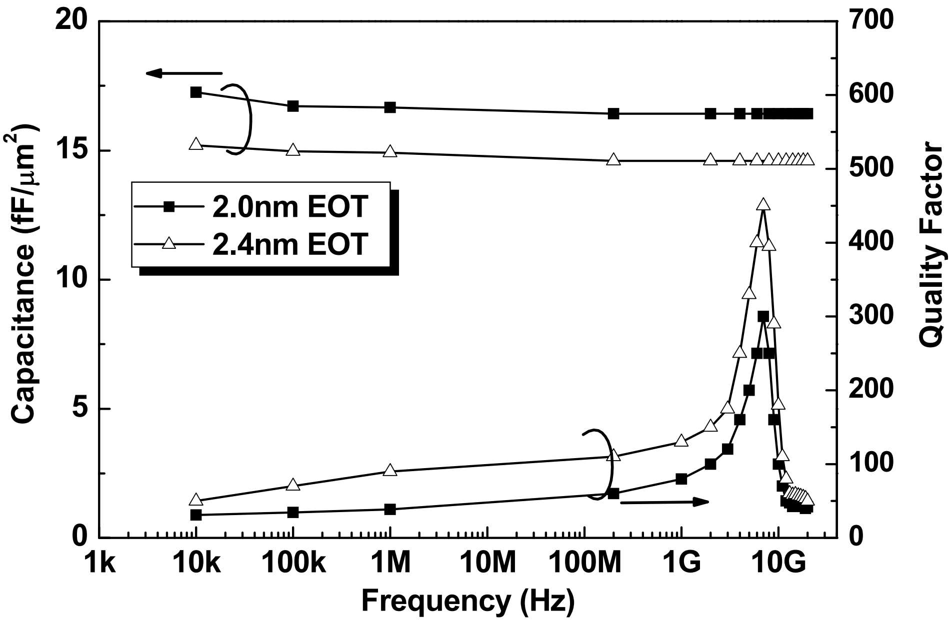


Fig. 4-7. The frequency dependent capacitance and Q-factor of 2.0 and 2.4 nm EOT Al doped TaO_x MIM capacitors.

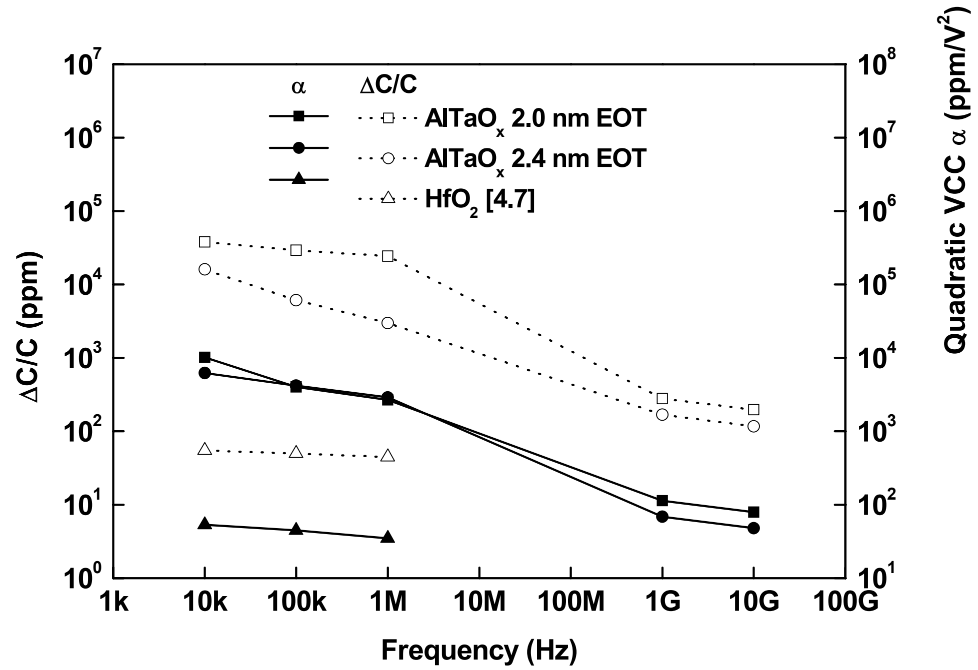


Fig. 4-8. The ΔC/C and a of Al doped TaO_x MIM capacitors as a function of frequency. It is notice that the ΔC/C and a decrease with increasing frequency.

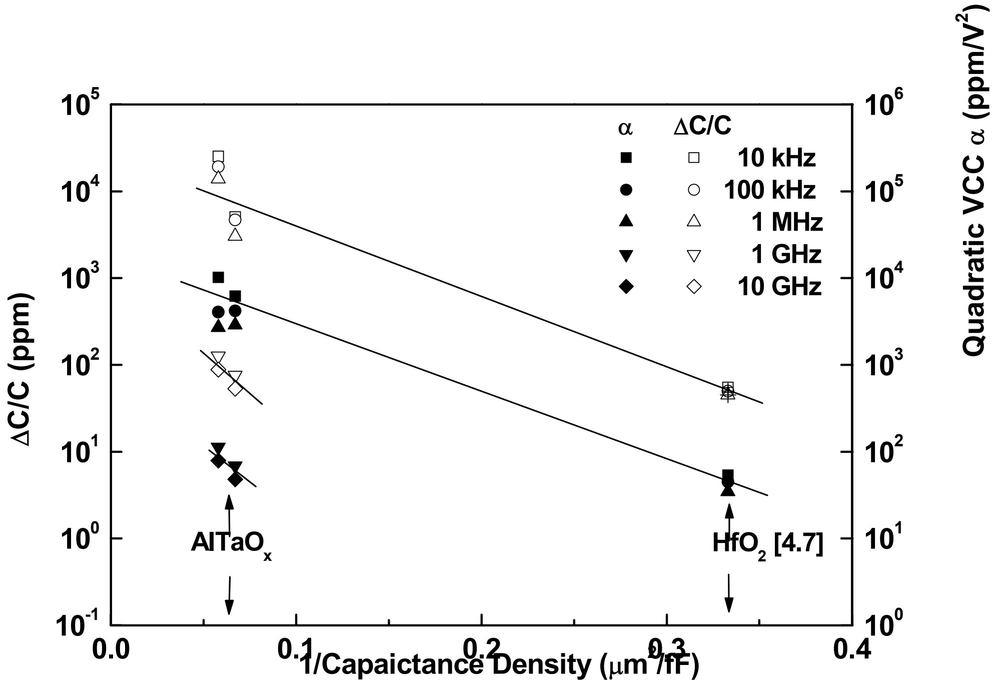


Fig. 4-9. The ΔC/C and α of Al doped TaO_x MIM capacitors as a function of 1/C. It is notice that the ΔC/C and αdecrease monotonically with ln(1/C).

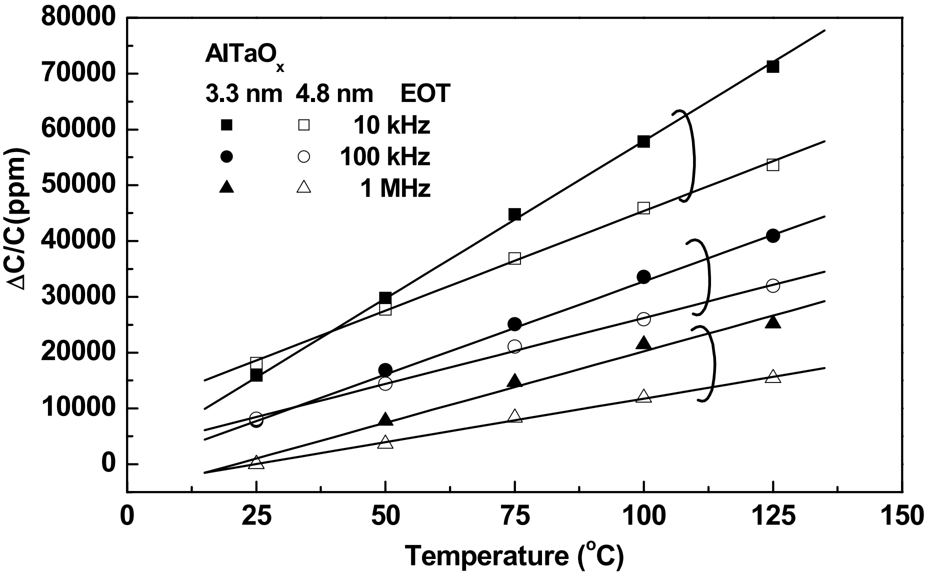


Fig. 4-10. The ΔC/C as a function of temperature of Al doped TaO_x MIM capacitors.

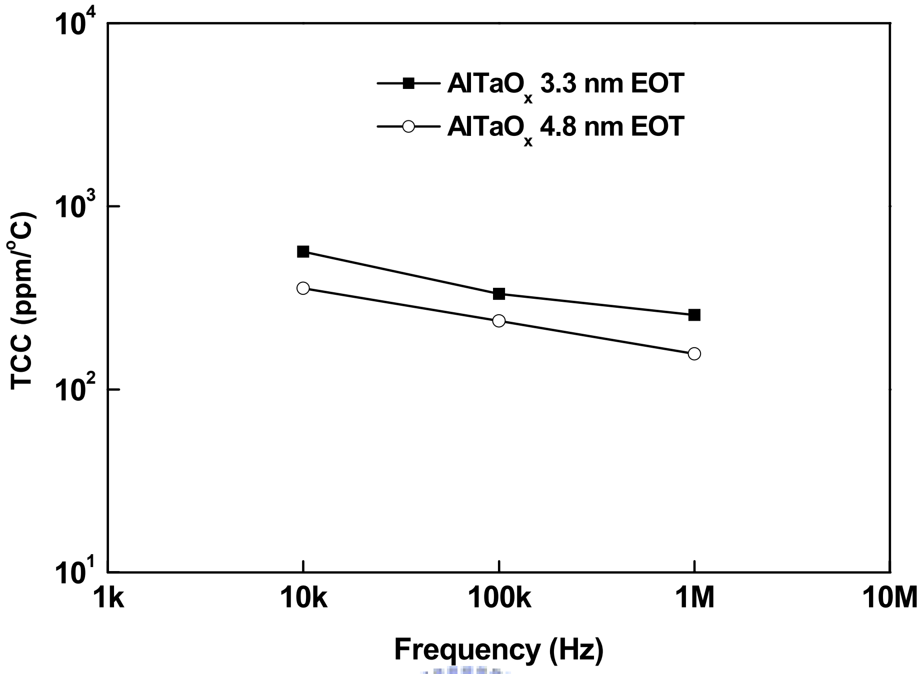


Fig. 4-11. The TCC as a function of frequency of Al doped TaO$_x$ MIM capacitors.

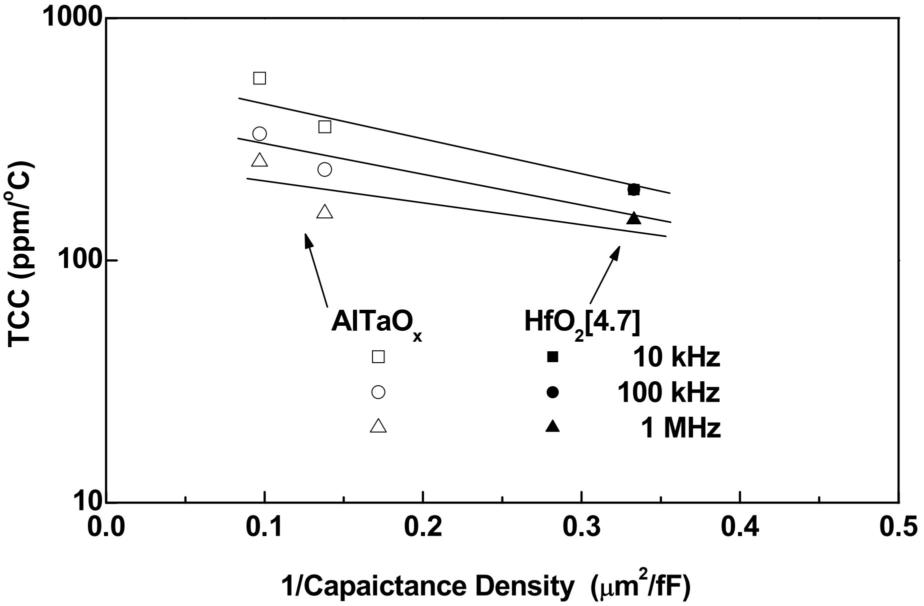


Fig. 4-12. The TCC of Al doped TaO_x MIM capacitors as a function of 1/C. TCC decreases monotonically with ln(1/C).

Chapter 5

The Theorem of the Variation of Dielectric Constant

5.1 Introduction of Free-carrier Relaxation

After recalling the background of Debye's relation for dipole relaxation, we give a detail presentation for the derivation of the complex dielectric constant due to the contribution of space charges that made of free carriers able to move between blocking electrodes. Then we propose experimental tests of the model to discuss the formal analog between the relaxation of a collection of permanent dipoles and that of space charges.

5.2 Debye Formula

Dipole relaxation within the meaning of Debye is a purely viscous process without elastic forces of recovery. A typical equation for such a phenomenon is, for example, that which describes the speed ν of a particle of mass m after the application of a constant force F in a viscous medium. Exerting a friction force fv on the particle to move:

$$m\frac{dv}{dt} = F - fv \qquad (1)$$

If the particle, having charge Q, is in a field E, then the force F is qE. The relation

(1) can be written in the form:

$$\frac{dv}{dt} = \frac{v_s - v}{\tau} \tag{2}$$

where $\tau = m/f$ and v_s is the speed limit (static) $v_s = F/f$ taken by the particle. By analogy, we can write for polarization by P_{or}, orientation of whole dipoles in thermal balance:

$$\frac{dP_{or}}{dt} = \frac{1}{\tau}[P_s - P_i - P_{or}(t)] \tag{3}$$

here, τ indicates the dipolar relaxation time, P_s is the end value (static) of polarization in a continuous-current field and P_i is the initial value which corresponds to quasi-instantaneous polarization due to the dependent electrons and ions ($P_{or} \rightarrow P_s - P_i$ in a constant field).

Let us imagine now that the particles (or, by analogy, dipoles) are in an alternate field of the form:

$$E = E_0\ e^{i\omega t} \tag{4}$$

In alternative mode, all the variables, and in particular polarization by P_{or} orientation, oscillate sinusoidal with the pulsation ω, so that we can write:

$$P_{or}(t) = |P_{or}|\ e^{i\omega t} \tag{5}$$

We can directly obtain (if not rigorously) the formula of Debye while replacing in (3) dP_{or}/dt by his value $i\omega P_{or}$ drawn from (5):

$$i\omega\tau\ P_{or} = P_s - P_i - P_{or} \tag{6}$$

We derive that:

$$P_{or}(\omega) = \frac{P_s - P_i}{1 + i\omega\tau} \tag{7}$$

so that the total polarization P(ω), sum of instantaneous polarization P_i and the polarization of P_{or}, is written:

$$P(\omega) = P_i + \frac{P_s - P_i}{1 + i\omega\tau} \tag{8}$$

By admitting that the local field of the dipoles is equal to the field applied. One has, by definition of the permittivities:

$$P^*(\omega) = (\varepsilon^* - \varepsilon_0)E \tag{9}$$

$$P_i(\omega) = (\varepsilon_\infty - \varepsilon_0)E \tag{10}$$

and

$$P_s(\omega) = (\varepsilon_s - \varepsilon_0)E \tag{11}$$

so that the relation (8) becomes:

$$\varepsilon^*(\omega) = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1 + i\omega\tau} \tag{12}$$

the relation (12) is the famous formula of Debye.

5.3 Polarization by Space Charges

In the traditional treatments of the interfacial polarization of the Maxwell-Wagner type, one admits that the movement of the instantaneous charges in material does not affect the uniform distribution of the field. In fact, the changes accumulate in the electrodes, in which they discharge more or less easily. It results from the gradients of concentration which tend to be opposed to accumulation. Briefly, the model treated initially by Mac Donald [5.1], who makes the following assumptions:

1. The material contains completely ionized fixed centers (for example, energy levels of impurities very close to the conduction band) and, mobility μ of free electrons in equal concentration.
2. The electrodes are completely blocking so that the current of electrons at the balance of the electrodes (x = ± d) are null.

In the absence of field applied, the free electrons, uniformly distributed in the sample, compensate for the load of the positive ionized centers everywhere, so that the sample is neutral. In the presence of a continuous-current field applied, the electrons are distributed in the sample under the combined action of the field and the diffusion which tends to be opposed to their accumulation to the electrodes.

If ρ(x) is the density of charge to balance with depth *x* in the sample index, average polarization is written:

$$P = \sum p \qquad (13)$$

$$P = \frac{1}{2d}\int_{-d}^{d} x\rho(x)\ dx \qquad (14)$$

If the direction of the field applied is then reversed, the electrons are distributed again and the situation develops towards a new balance where $\rho'(x) = -\rho(x)$. Therefore, the new macroscopic dipole and polarization are opposed to the precedent.

We thus attend a phenomenon similar to a dipolar relieving of Debye type, occurring in a sample that becomes from initially homogeneous (statistically) to heterogeneous under the action of the field. This is represented on figure 5-1.

5.4 Calculation of Polarization into Alternative Field

Following, we will study the dynamic balance of the system when the sample is subjected to an alternate field of pulsation ω and rather low amplitude so that the system remains linear, and consequently that the variables (time and space) are separable. In fact, it is more about a limit on the tension applied (at ordinary temperature).

We concern for the uniform concentration n_0 and their mobility μ of free electrons (and centers) in the absence of alternating field. Under the terms of the assumptions, the total number of electrons per unit area of the sample, thickness 2d, is equal to $2dn_0$ in the presence of the alternate field.

That is to say:

$$E_a = A_a e^{i\omega t} \qquad (15)$$

the alternate field applied, whose amplitude A_a assumes lower than *KT/2*. The concentration of charge at x-coordinate x is not very different from n_0, so that the difference $n - n_0$ oscillates with the pulsation ω and we can write:

$$n(x,t) = n_0 + \nu(x)\ e^{i\omega t} \qquad (16)$$

In the same way, the potential V(x,t) and the field E(x,t) take the respective forms:

$$V(x,t) = \varphi(x)\ e^{i\omega t} \qquad (17)$$

and

$$E(x,t) = A(x)\ e^{i\omega t} \qquad (18)$$

Of course, the factors ν(x), φ(x) and A(x) are complex quantities. The complex permittivity ε*(ω) of the sample is by definition:

$$\varepsilon^* = \varepsilon + \frac{P(\omega)}{A_a} \qquad (19)$$

where polarization P, defined by (14), results from the excess of density ν(x), given by (16).

Calculation of ν(x) is the current of particles and the number of charges crossing to x-coordinate x, by unit time, unit area of the x-plane. It is the sum of the drift current nμE and the diffusion current -- D∇n:

$$j(x,t) = -\mu n \frac{\partial V}{\partial x} - D\frac{\partial n}{\partial x} \qquad (20)$$

so that the conservation equation:

$$\frac{\partial n}{\partial t} = -\frac{\partial j}{\partial x}$$

becomes

$$\frac{\partial n}{\partial t} = \mu \frac{\partial}{\partial x}(n\frac{\partial V}{\partial x}) + D\frac{\partial^2 n}{\partial x^2} \qquad (21)$$

While introducing the values of n and V into (21), given from (16) and (17) respectively, we can obtain:

$$i\omega v = \mu n_0 \frac{d^2\varphi}{dx^2} + D\frac{d^2 v}{dx^2} + \mu\frac{d}{dx}(v\frac{d\varphi}{dx})e^{i\omega t} \qquad (22)$$

Since ν is small compared with n_0, the third term of the member of right-hand side of (22) is negligible compared with the first two terms. In addition, the Poisson's equation is written here:

$$\frac{d^2\varphi}{dx^2} = -\frac{e}{\varepsilon}v \qquad (23)$$

and, while combining (23) with the simplified equation (22), we can obtain:

$$(i\omega + \frac{\mu e n_0}{\varepsilon})v = D\frac{d^2 v}{dx^2} \qquad (24)$$

Then we regard $\mu e n_0/\varepsilon = \sigma/\varepsilon$ as the reverse of the relaxation time τ of material, (24) is written in the form:

$$\frac{d^2 v}{dx^2} = \frac{1+i\omega\tau}{D\tau}v \qquad (25)$$

By using the variable complexes reduced:

$$X = \sqrt{\frac{1+i\omega\tau}{D\tau}}x = \frac{Z}{L}x$$

where $Z = (1+i\omega\tau)^{1/2}$ and $L = (D\tau)^{1/2}$ is the length of Debye,

$$\frac{d^2 v}{dX^2} = v \qquad (26)$$

This equation has as a general solution:

$$v = v_1\ e^{X} + v_2\ e^{-X}$$

but the conservation of the instantaneous charges implies:

$$\int_{-d}^{d} v(x)\ dx = 0$$

It indicates $\nu_2 = -\nu_1$, so that the solution physically acceptable for ν(x) is:

$$v(x) = 2\ v_1\ \sinh(\frac{Z}{L}x) = 2\ v_1\ \sinh X \qquad (27)$$

By integrating (23), we can obtain:

$$A(x) = \frac{2ev_1\ L}{\varepsilon\ Z}\cosh X + A_0 \qquad (28)$$

and the constant A_0 results from the boundary condition imposed by the potential applied:

$$\int_{-d}^{d} A(x)\ dx = 2A_a d$$

which is written:

$$\frac{2ev_1}{\varepsilon}(\frac{L}{Z})^2 \sinh Y + A_0 d = A_a d \qquad (29)$$

where we posed:

$$Y = X(d) = (d/L)\ Z =$$
$$= \frac{\delta}{\sqrt{2}}[(\sqrt{1+\omega^2\tau^2}+1)^{1/2} + i(\sqrt{1+\omega^2\tau^2}-1)^{1/2}]$$

was left that (28) takes the form:

$$A(X) = A_a + \frac{2edv_1}{\varepsilon\ Y}(\cosh X - \frac{\sinh Y}{Y}) \qquad (30)$$

Finally, ν_1 can be obtained by writing that the current of particles in x = d (X = Y) is null, since the electrodes are blocking:

$$n\mu A(Y) - D\frac{Z}{L}\left(\frac{dv}{dX}\right)_Y = 0 \tag{31}$$

Taking (27) and (30) into account, (31) is written:

$$A_a + \frac{2edv_1}{\varepsilon\ Y}\left(\cosh Y - \frac{\sinh Y}{Y}\right) = \frac{2DZv_1}{n\mu L}\cosh Y \tag{32}$$

By remembering that n ~ n_0 and using the written accounts above between L, D, μ and n, (32) takes the form:

$$A_a = \frac{2ev_1}{\varepsilon}\left[\left(LZ - \frac{L}{Z}\right)\cosh Y + \frac{L}{Z}\frac{\sinh Y}{Y}\right] \tag{33}$$

and like LZ – L/Z = iωτL/Z, the relation above gives ν_1, and consequently:

$$v(x) = 2v_1\ \sinh X = \frac{\varepsilon Z A_a}{eL}\frac{\sinh X}{i\omega\tau\cosh Y + \sinh Y/Y} \tag{34}$$

Consequently, the polarization given by (14) becomes:

$$P(\omega) = \frac{\varepsilon A_a}{Y}\frac{\int_0^Y X\cosh X\ dX}{i\omega\tau\cosh Y + \sinh Y/Y} \tag{35}$$

After integration of the numerator:

$$P(\omega) = \varepsilon A_a\frac{\cosh Y - \sinh Y/Y}{i\omega\tau\cosh Y + \sinh Y/Y} \tag{36}$$

While returning to the definition of $P(\omega)$ (19), we have finally obtained:

$$\varepsilon^* = \varepsilon\frac{1 + i\omega\tau}{i\omega\tau + \tanh Y/Y} \tag{37}$$

The relation (37) was extended by Meaudre and Mesnard [5.2]-[5.3] if we take account of the existence of traps in material. Y must be modified.

5.5 Distribution of the Field

It results from the relations (31) and (33) that:

$$A(X)=\frac{i\omega\tau\cosh Y+\cosh X}{i\omega\tau\cosh Y+\sinh Y/Y}A_a \tag{38}$$

The module of A(X) is various with δ and ωτ. We observe that for a given value of δ, the field is more distorted (especially close to the electrodes) when ωτ is small.

The following relations give φ(*x*), A(*x*) and ν(*x*):

$$\varphi(x)=-\frac{i\omega\tau X\cosh Y+\sinh X}{i\omega\tau Y\cosh Y+\sinh Y}dA_a \tag{39}$$

$$A(X)=\frac{i\omega\tau\cosh Y+\cosh X}{i\omega\tau\cosh Y+\sinh Y/Y}A_a \tag{38}$$

$$v(x)=\frac{\sinh X}{i\omega\tau Y\cosh Y+\sinh Y}\frac{\varepsilon Y^2}{ed}A_a \tag{34'}$$

where X=(*x*/L)Z.

It results from the preceding formulas that φ(x) and ν(x) are dependent using the relation:

$$\varphi(x)+\frac{ed^2}{\varepsilon Y^2}v(x)=-\frac{i\omega\tau}{i\omega\tau+\tanh Y/Y}xA_a \tag{40}$$

At low frequency (ωτ << 1), the member of right-hand side of (40) is very small, so that:

$$\varphi(x)\cong-\frac{ed^2}{\varepsilon Y^2}v(x) \tag{41}$$

With high frequency (ωτ >> 1), it becomes comparable with xA_a. As the field inside the sample is distorted a little at high frequency, we can pose:

$$-xA_a=(1-\eta)\varphi(x)$$

with $\eta \ll 1$.

We conclude from it that:

$$\varphi(x) \cong -\frac{ed^2}{\eta \varepsilon Y^2 v(x)} \qquad (41')$$

The relations (41) and (41') show that φ is proportional to ν whatever the frequency except in the vicinity of the electrodes.

The electrodes are partially blocking. -- If the electrodes are partially blocking, one can admit that the current with x = d (and, by symmetry, with x = -d) is proportional to the local density of load at the interface:

$$j(d) = \gamma D \frac{v(Y)}{d} = \gamma D \frac{Z}{L} \frac{v(Y)}{Y} \qquad (42)$$

where γ is a coefficient without dimension and characterizing the ability of the electrode blocking [5.4] ($\gamma = 0$ for a blocking electrode). Then the equation (31) becomes:

$$n\mu A(Y) - D\frac{Z}{L}\left(\frac{dv}{dX}\right)_Y = \gamma D \frac{Z}{L} \frac{v(Y)}{Y} \qquad (43)$$

While using (27) and (30), and replacing ν_1 by ν'in these relations, (43) becomes:

$$A_a + \frac{edv'}{\varepsilon Y}\left(\cosh Y - \frac{\sinh Y}{Y}\right) = \frac{DZv'}{n\mu L}\left(\cosh Y + \gamma \frac{\sinh Y}{Y}\right)$$

then

$$A_a = \frac{eLv'}{\varepsilon Z}\left[i\omega\tau \cosh Y + (\gamma Z^2 + 1)\frac{Y}{\sinh Y}\right] \qquad (44)$$

We define $\nu'(x) = \nu' \sinh x$:

$$v'(x) = \frac{\varepsilon Z A_a}{eL} \frac{\sinh X}{i\omega\tau \cosh Y + (\gamma Z^2 + 1)\sinh Y / Y} \tag{45}$$

Having ν(*x*), we can obtain *P*(ω) like the work previously we do and find ε* :

$$\varepsilon^*(\omega) = \varepsilon \frac{(1 + i\omega\tau)(1 + \gamma \tanh Y / Y)}{i\omega\tau + [(1 + i\omega\tau)\gamma + 1)] \tanh Y / Y} \tag{46}$$

Therefore, we have obtained the useful equations (37) and (46) to analyze the frequency-dependent permittivity ε* in the next chapter.

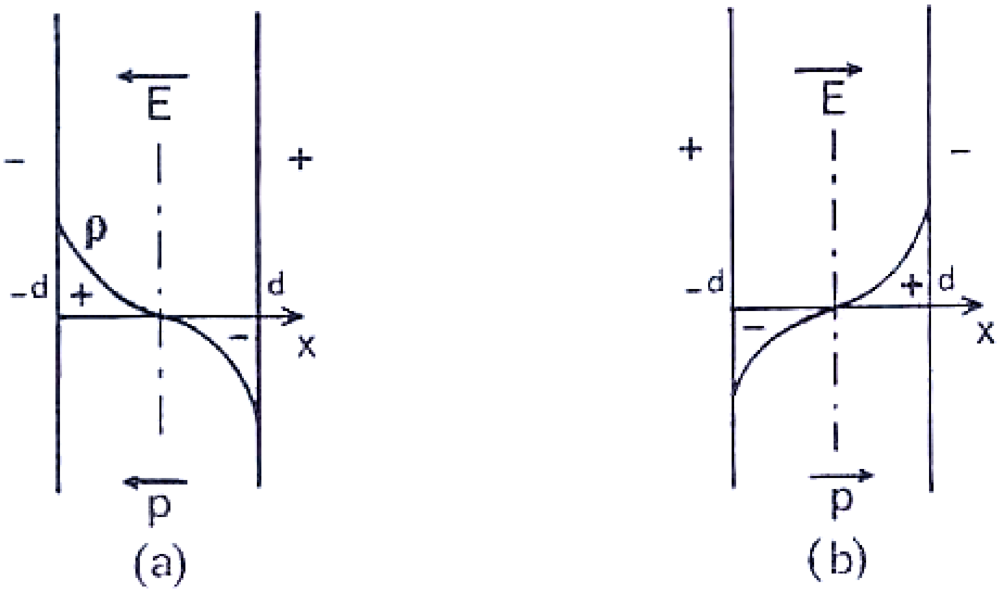


Fig. 5-1. Switching of the macroscopic dipole by reversal of the applied field.

Chapter 6

The Unified Understanding and Prediction of High-κ Al doped TaO_x Metal-Insulator-Metal Capacitors

6.1 Introduction

In MIM capacitors, one of the great challenges is to achieve small voltage coefficient of capacitance (VCC). Though experimental results of VCC variation such as thickness effects have been reported [6.1]-[6.6], the mechanism of VCC dependence remains unclear. Here we present a unified understanding of voltage based on the free carrier injection model. And the model can also be used to understand other high-κ materials. So we will use this model to characterize the high-κ Al doped TaO_x and compare with the most popular high-κ HfO_2.

6.2 The Free Carrier Injection Model

Fig. 6-1 shows the free carrier injection model, which attributes capacitance variation to injected carriers [6.7]. The excess charges in the insulator layer will follow the alternating signal with a relaxation time (τ) that depends on the mobility of carrier (μ), excess carrier density (n), and dielectric constant (ε). A higher relaxation time means the carriers are more difficult to follow the alternating signal. Fig. 6-2 (a) and (b) show the leakage current of 11.5 nm Al doped TaO_x and 30 nm HfO_2 MIM capacitors [6.3], respectively. Fig. 6-3 (a) and (b) show that the model fits very well with measured C-V curve of Al doped TaO_x and HfO_2 MIM capacitors, respectively.

6.3 Thickness Dependence

Fig. 6-4 (a) and (b) show the linear dependence of carrier concentration pre-factor (n_0) of Al doped TaO_x and HfO_2 MIM capacitors on thickness, respectively. Simulated normalized capacitances (ΔC/C) as a function of voltage with different thickness are shown in Fig. 6-5 (a) and (b). Fig. 6-6 (a) and (b) suggest thickness dependence of quadratic VCC of Al doped TaO_x and HfO_2 MIM capacitors have a relation of $\alpha \propto t^{-n}$ shown in Fig. 6-7, which is consistent with the report in [6.6]. This thickness effect is due to E-field reduction with increased thickness. It is also found from Fig. 6-6 (b) that, after accounting the thickness dependence of n_0, the decreasing of quadratic VCC with thickness is slower, which implies the limitation of high-κ materials for analog applications where small VCC is needed.

6.4 Frequency Dependence

From the model itself, there is no frequency dependence of VCC. To fit the frequency dependence of VCC, the change of mobility at different frequencies need to be considered. Fig. 6-8 (a) and (b) show the measured quadratic VCC and fitted carrier mobility at different frequencies. It is found that both the quadratic VCC and the fitted carrier mobility decrease with the frequency. Simulated normalized capacitances as a function of voltage at different frequencies are shown in Fig. 6-9. It is believed that the carrier mobility becomes smaller with increasing frequency, which leads to a higher relaxation time and a smaller capacitance variation.

6.5 Stress Induced Voltage Coefficient of Capacitance

Fig. 6-10 and Fig. 6-11 show that, for thick HfO_2 MIM capacitors, both stress induced leakage current and quadratic VCC changes slightly with stress time. In comparison, Fig. 6-12 and Fig. 6-13 show that, for thin HfO_2 MIM capacitors, both the leakage current and quadratic VCC changes quite significantly with stress time. The results imply that both stress induced leakage current (SILC) and the variation of quadratic VCC are correlated to each other. With the increase of stress time, carrier mobility (μ) could be modulated to be smaller by the stress generated traps, and further leads to a higher relaxation time and a smaller capacitance variation.

$$C = \frac{\varepsilon'}{t}$$

$$\varepsilon^* = \varepsilon' - j\varepsilon'' = \varepsilon \frac{1 + j\omega\tau}{j\omega\tau + \frac{\tanh(A)}{A}}$$

where,

$$A = \sqrt{\frac{1 + j\omega\tau}{D\tau}}\left(\frac{t}{2}\right)$$

$$D = \mu kT / q$$

$$\tau = \frac{\varepsilon}{\mu q n}$$

$$n = n' \exp\left(\frac{\beta_s \sqrt{E}}{2kT}\right)$$

$$J(E) \propto \exp\left(\frac{-q\psi_B}{kT}\right) \exp\left(\frac{\beta_s \sqrt{E}}{2kT}\right)$$

τ: relaxation time

μ: carrier mobility in insulator

n’: pre-factor of effective carrier concentration

β_s: β factor in current emission

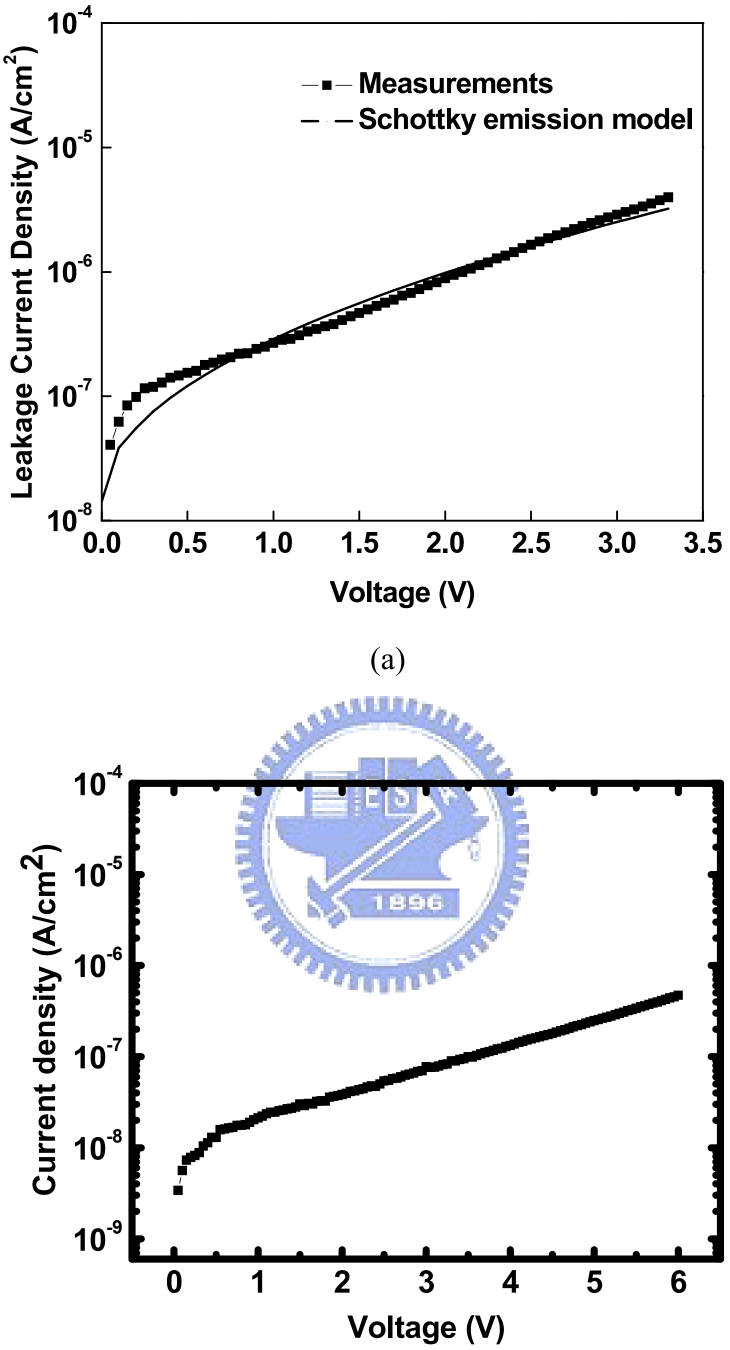
T: temperature

t: thickness of insulator

ω: frequency (=$2\pi f$)

J: leakage current density

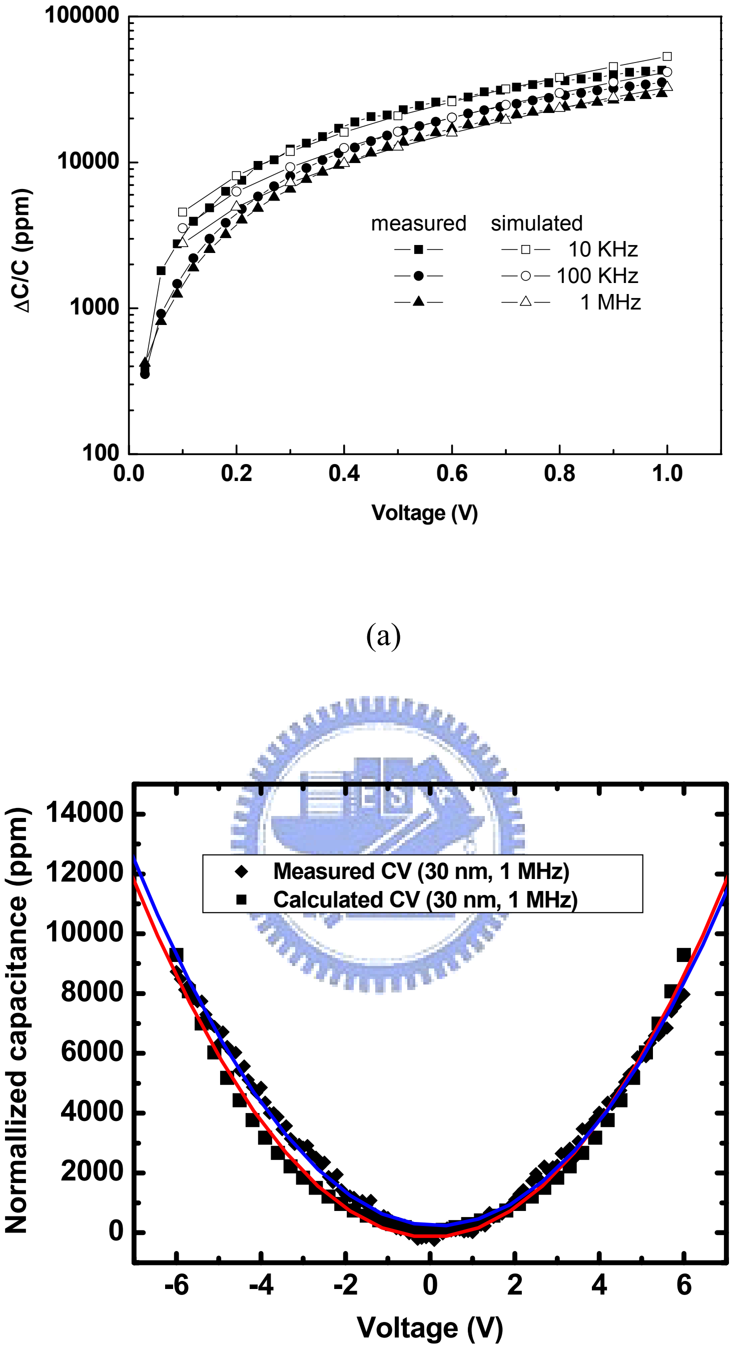
Fig. 6-1. Free carrier injection model to analyze the frequency-dependent $\Delta C/C$.



(a)

(b)

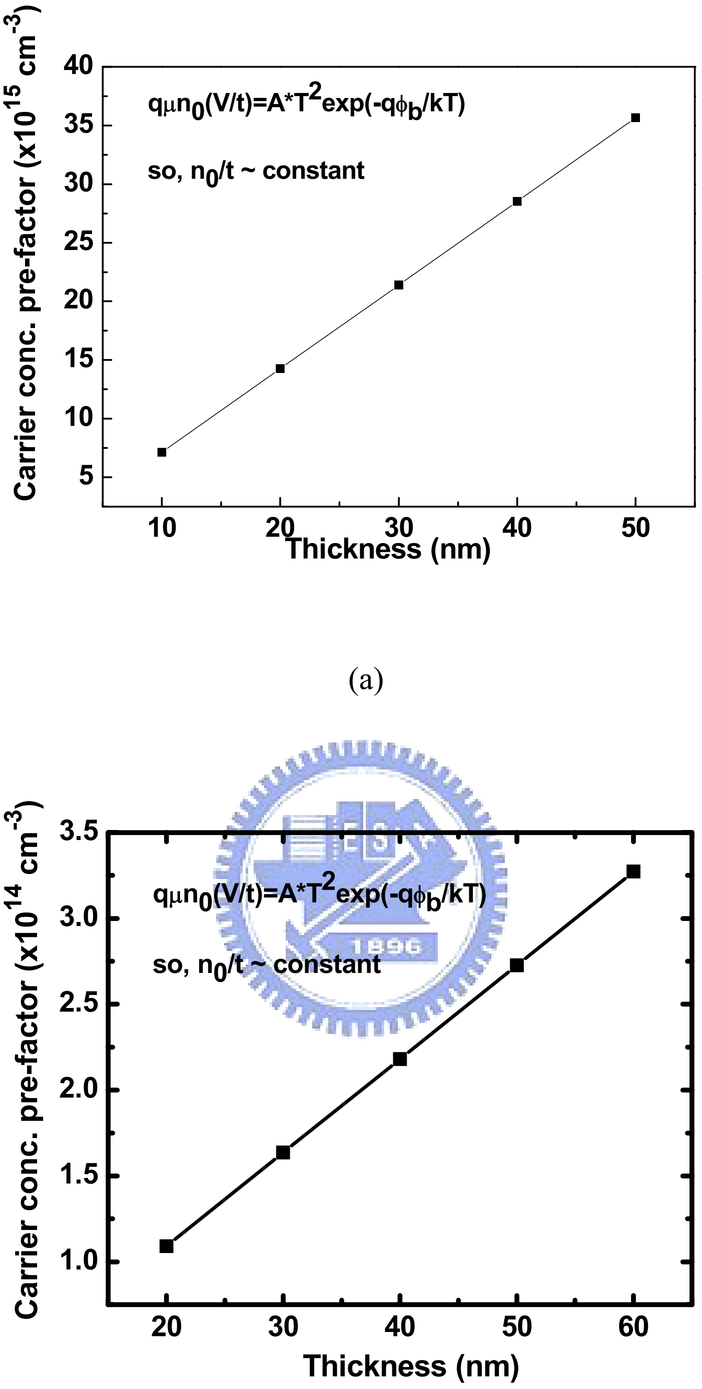
Fig. 6-2. The measured and simulated J-V characteristic of high-κ (a) Al doped TaO_x and (b) HfO_2 [6.8] MIM capacitors. The experimental data can be fitted by an emission current model.



(a)

(b)

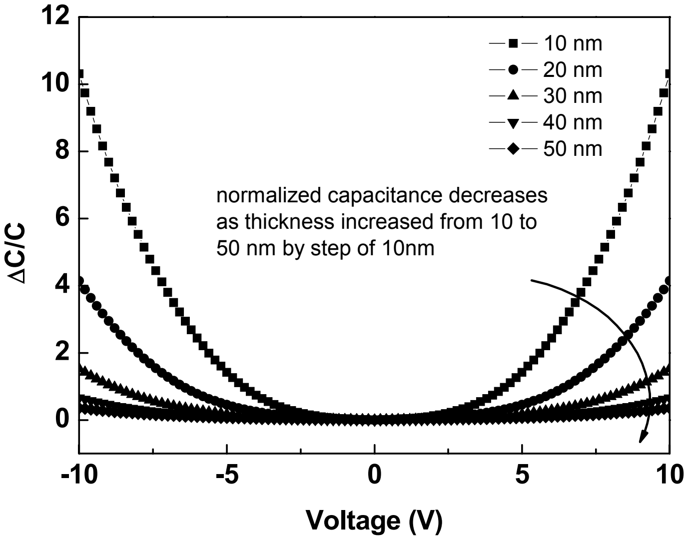
Fig. 6-3. Measured and simulated normalized capacitance of high-κ (a) Al doped TaO_x and (b) HfO_2 [6.8] MIM capacitors as a function of voltage. n_0 and μ are extracted by fitting the measured data.



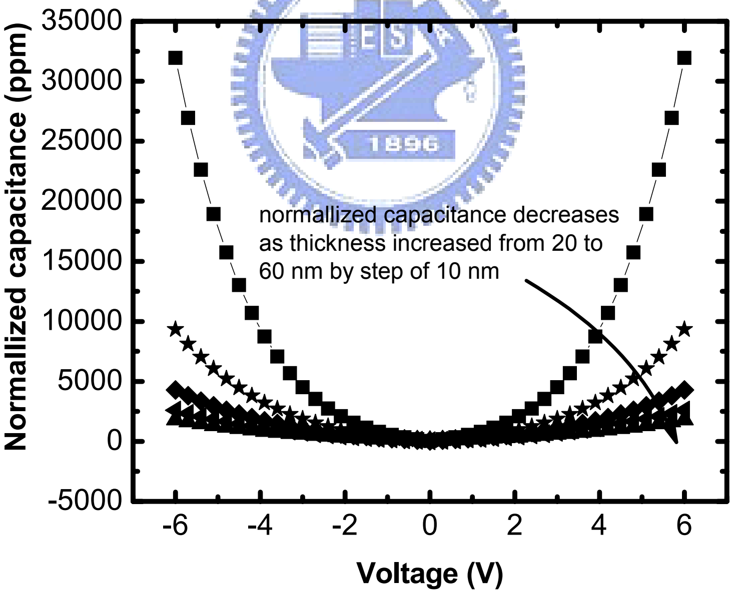
(a)

(b)

Fig. 6-4. Dependence of carrier concentration pre-factor of high-κ (a) Al doped TaO_x and (b) HfO_2 [6.8] MIM capacitors on thickness.

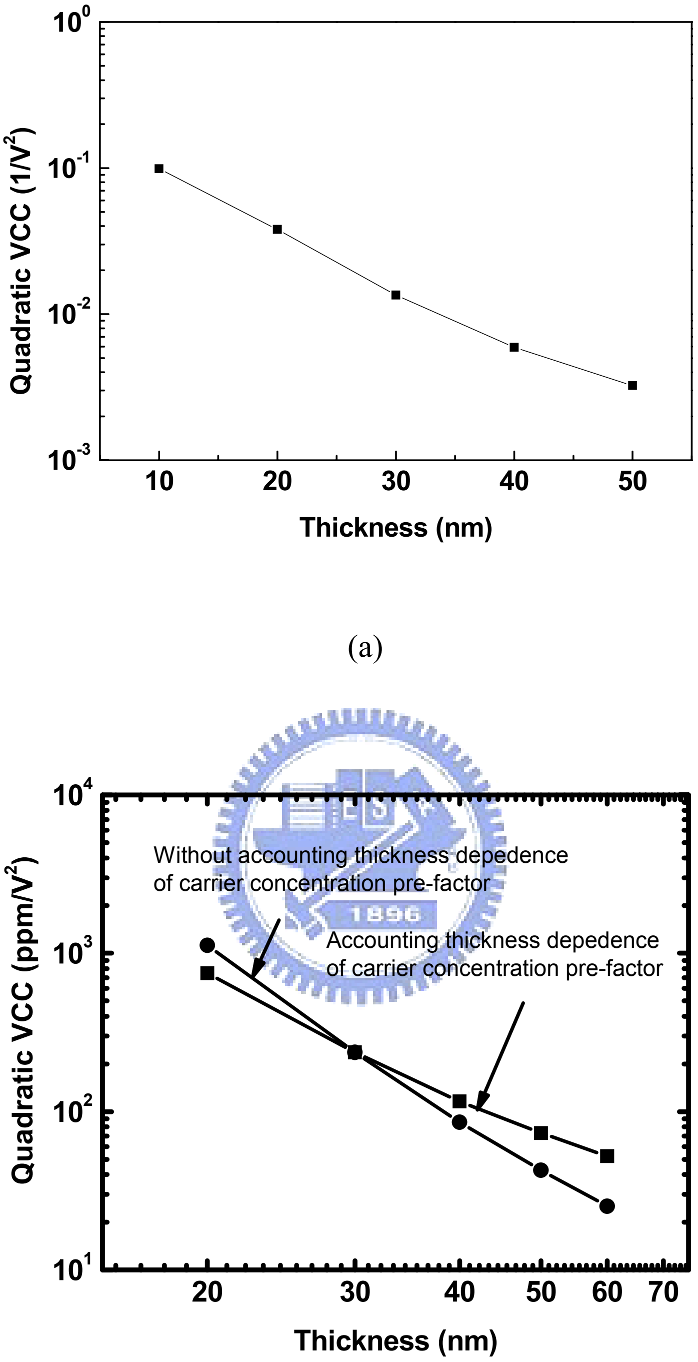


(a)



(b)

Fig. 6-5. Simulated normalized capacitance as a function of voltage for different thickness of 20, 30, 40, 50, and 60 nm of high-κ (a) Al doped TaO_x and (b) HfO_2 [6.8] MIM capacitors.



(a)

(b)

Fig. 6-6. Quadratic VCC of high-κ (a) Al doped TaO_x and (b) HfO_2 [6.8] MIM capacitors as a function thickness.

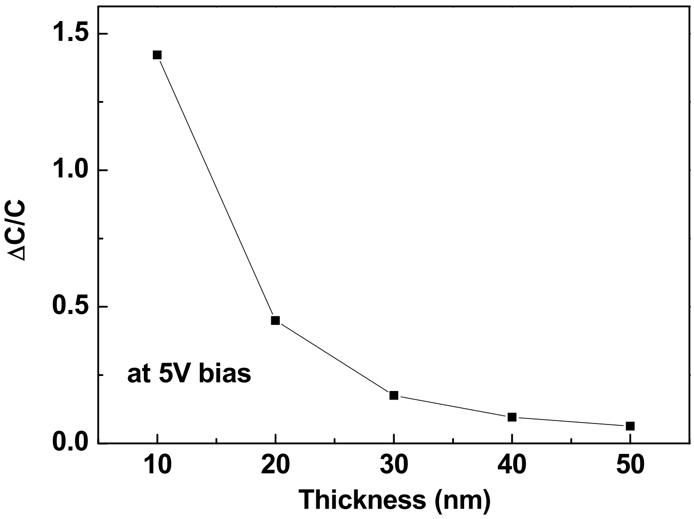
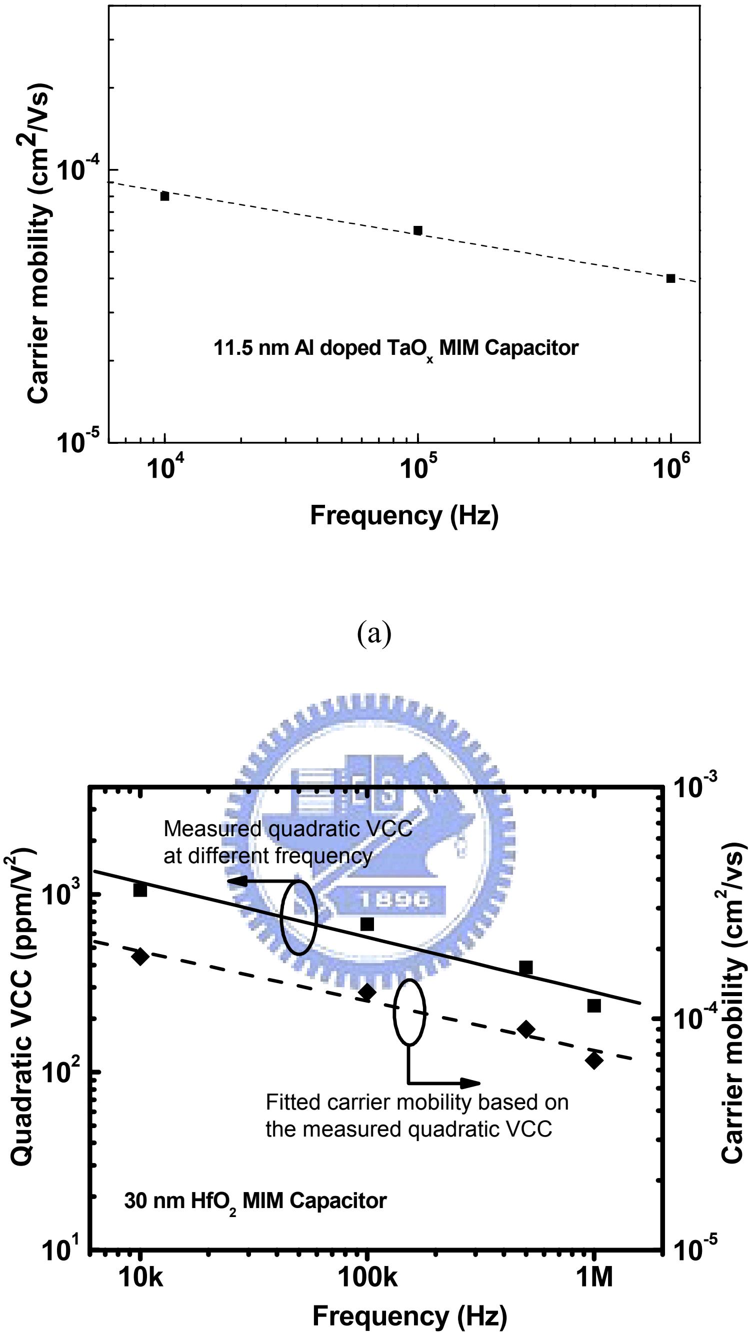


Fig. 6-7. Quadratic VCC of high-κ Al doped TaO_x MIM capacitors as a function thickness.



(a)

(b)

Fig. 6-8. Quadratic VCC and fitted carrier mobility of high-κ (a) Al doped TaO_x and (b) HfO_2 [6.8] MIM capacitors as a function of frequency.

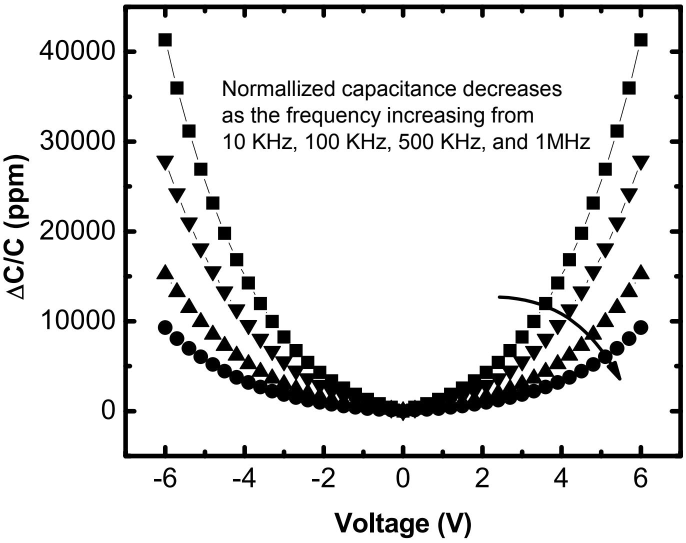


Fig. 6-9. Simulated normalized capacitance as a function of voltage for 30 nm HfO_2 MIM capacitors at for different frequencies of 10K, 100K, 500K, and 1MHz [6.8].

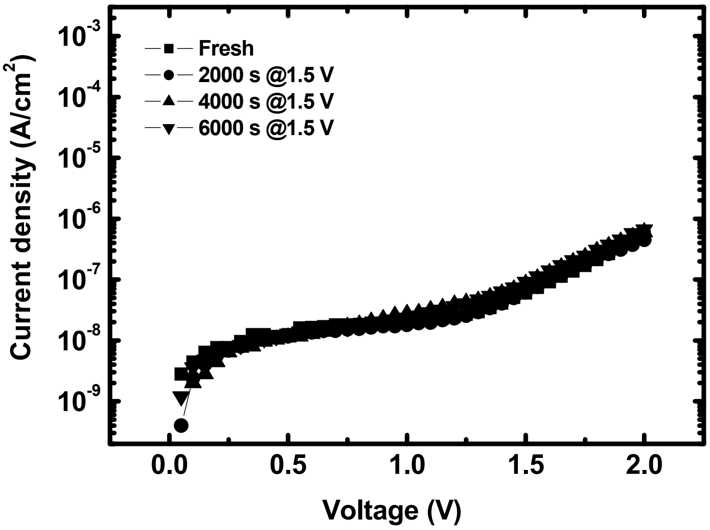


Fig. 6-10. Stress induced leakage current of thick HfO_2 MIM capacitor [6.8].

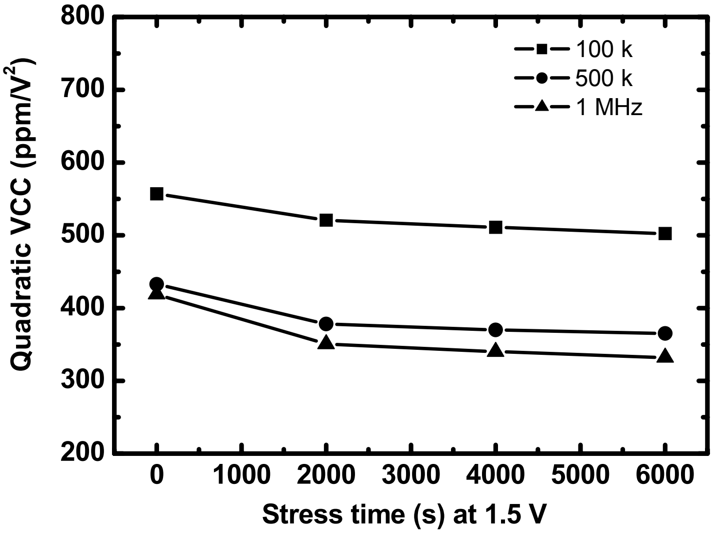


Fig. 6-11. Stress induced quadratic VCC of thick HfO_2 MIM capacitor [6.8].

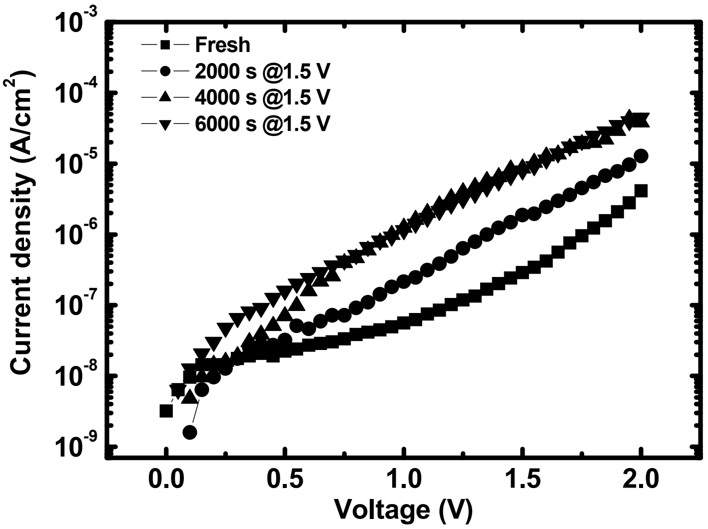


Fig. 6-12. Stress induced leakage current of thin HfO_2 MIM capacitor [6.8].

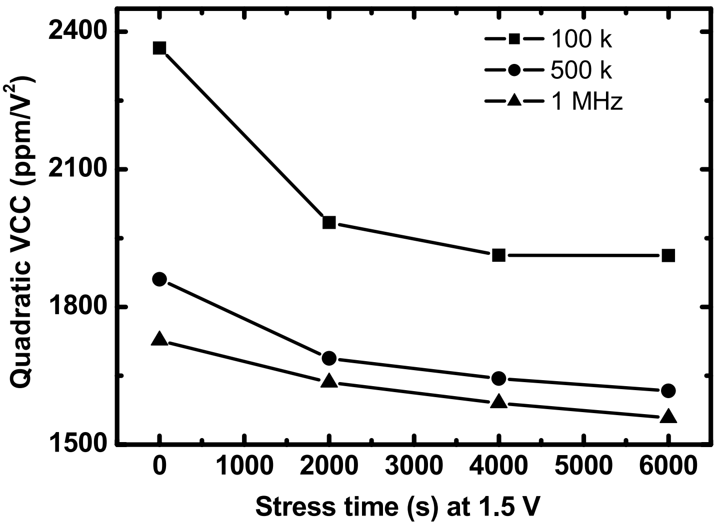


Fig. 6-13. Stress induced quadratic VCC of thin HfO_2 film MIM capacitor

[6.8].

Chapter 7

The Analysis of High-κ MIM Capacitor with Al doped TaO_x Dielectrics

7.1 Reviewing the Work Before

The MIM capacitors were fabricated using high-κAl doped TaO_x dielectrics described previously, where record high capacitance density of 17 fF/μm^2 was obtained. Fig. 7-1 shows the C-V characteristics as well as the ΔC/C values. These data were obtained using an LCR meter from 10 KHz and 1 MHz, and calculated from measured S-parameters for the 1 to 10 GHz range, using

$$\frac{\Delta C}{C} = \frac{Z_0(2 + Z(C) / Z_0)^2}{2R_P^2} j\omega C^2 (R_P + 1 / j\omega C)^2 \Delta(S_{21}) \tag{1}$$

Fig. 7-2 shows that the ΔC/C decreases rapidly with increasing frequency, which is advantageous for high frequency analog/RF circuits.

A free carrier injection model may be used to analyze the frequency dependence of ΔC/C [7.1]-[7.2]. The capacitor density is related to real part of the complex dielectric constant (ε') and thickness (t)

$$C = \frac{\varepsilon'}{t} \tag{2}$$

The complex dielectric constant (ε^*) is

$$\varepsilon^* = \varepsilon' - j\varepsilon'' = \varepsilon \frac{1 + j\omega\tau}{j\omega\tau + \frac{\tanh(A)}{A}} \tag{3}$$

Here A is given by

$$A = \sqrt{\frac{1 + j\omega\tau}{D\tau}(\frac{t}{2})} \tag{4}$$

where D is the diffusion coefficient.

The carriers in the MIM capacitor dielectric will follow an alternating signal depending on τ, which is related to the carrier mobility (μ) and density (n) by

$$\tau = \frac{\varepsilon}{\mu q n} \tag{5}$$

with n derived from the leakage current and is a function of electric field (E)

$$n(E) = n' \exp(\frac{\beta_s \sqrt{E}}{2kT}) \tag{6}$$

7.2 Analysis of the Variation of Capacitance

To examine the field dependence of the carrier density, we first analyze the leakage current. Fig. 7-3 shows the measured and modeled leakage currents. The leakage current of ~9×10^{-7} A/cm^2 at -2 V is low enough for circuit applications, since the capacitor area would be small and high density (17 fF/μm^2). high. The J-V curve can be fitted accurately using the emission current equation:

$$J(E) \propto \exp(\frac{-q\Psi_B}{kT}) \exp(\frac{\beta_s \sqrt{E}}{2kT}) \tag{7}$$

Thus the free carrier injection model should be validity in the following analysis.

In Fig. 7-4 we show the measured and calculated ΔC/C-V over the 10 KHz to 10

GHz frequency range. In the free carrier injection model, a nearly constant, weak frequency dependent τ was used. This assumption is often used when analyzing ΔC/C-V data for MIM capacitors [7.1]-[7.2]. Although the agreement between measured and modeled ΔC/C-V at 10 KHz and 1 MHz is reasonable, the simulated curve deviates from the data at GHz frequencies and much over-estimates the ΔC/C-V decrease.

To fit the measured ΔC/C-V over the whole frequency range requires that decreases with increasing frequency. In Fig. 7-5 we show the relaxation time needed to explain the data and the curve

$$\tau = \frac{\varepsilon}{\mu q n}\sqrt{\frac{1}{1+(f/f_0)^2}} \tag{9}$$

where f_0 is a constant frequency. Using this variation of τ the simulated curves in Fig. 7-6 agree well with the ΔC/C-V data. This is due to the fact that in the free carrier injection model, we neglected the contribution of the dipole relaxation to the capacitance. The dipole effects are known to be particular important in ferroelectrics crystals and contribute strongly to the nonlinear dielectric response [7.2] and thus to the ΔC/C variations. The contribution of dipole effects can be observed even at infrared frequency, while the free carrier effects become negligible at frequencies higher than about 1 MHz. The frequency dependence of τ represented by $[1+(f/f_0)^2]^{-1/2}$ has the same form as that for a FET's voltage gain [7.3]-[7.4]. This suggests that the reduction of ΔC/C with increasing frequency can be understood simply by similar physics - the injected carriers into the MIM capacitor cannot follow the increasing frequency and cause ΔC/C or the transistor's gain to decrease.

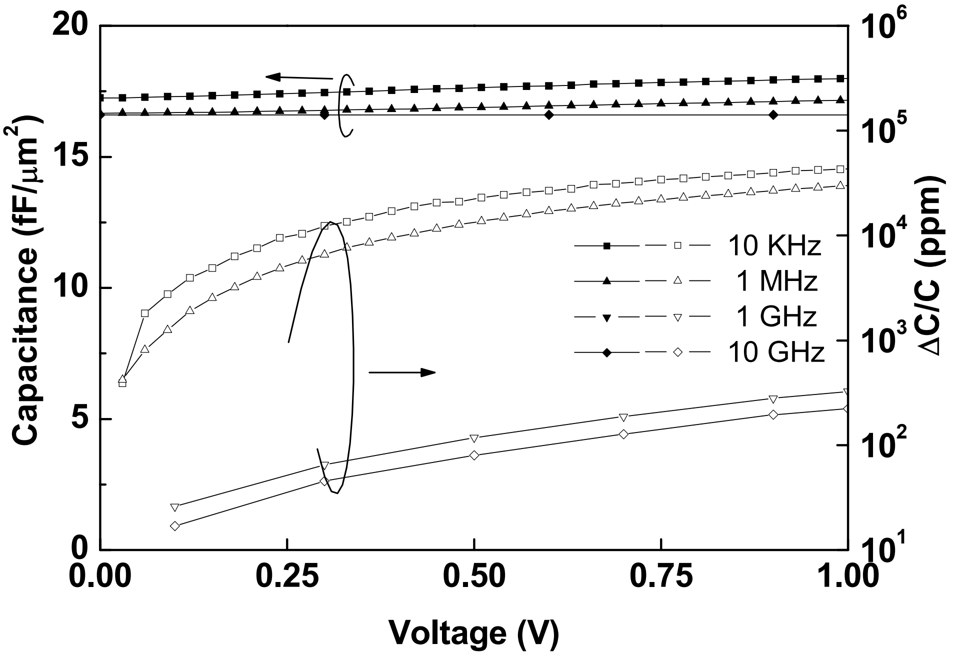


Fig. 7-1. C-V and ΔC/C-V characteristics of high-k Al doped TaO_x MIM capacitors at different frequencies.

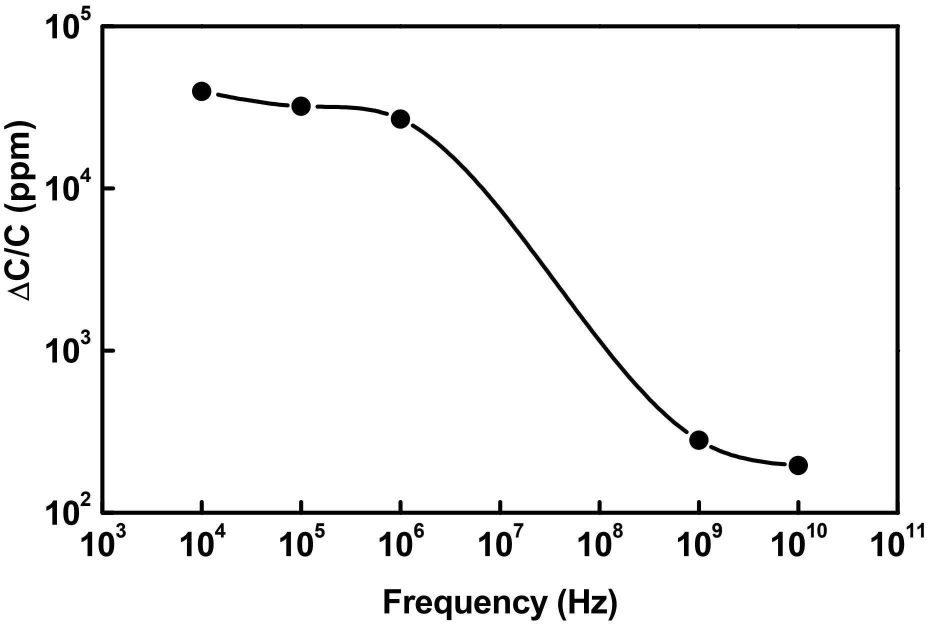


Fig. 7-2. ΔC/C of Al doped TaO_x MIM capacitors at different frequencies.

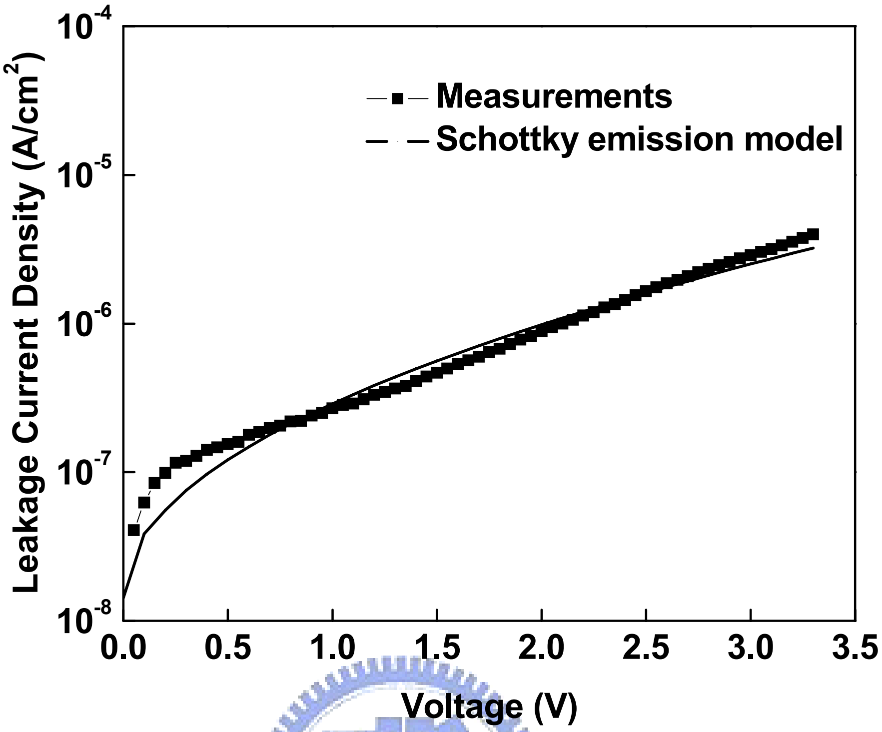


Fig. 7-3. The measured and simulated J-V characteristic of high-k Al doped TaO_x MIM capacitors. The experimental data can be fitted by an emission current model.

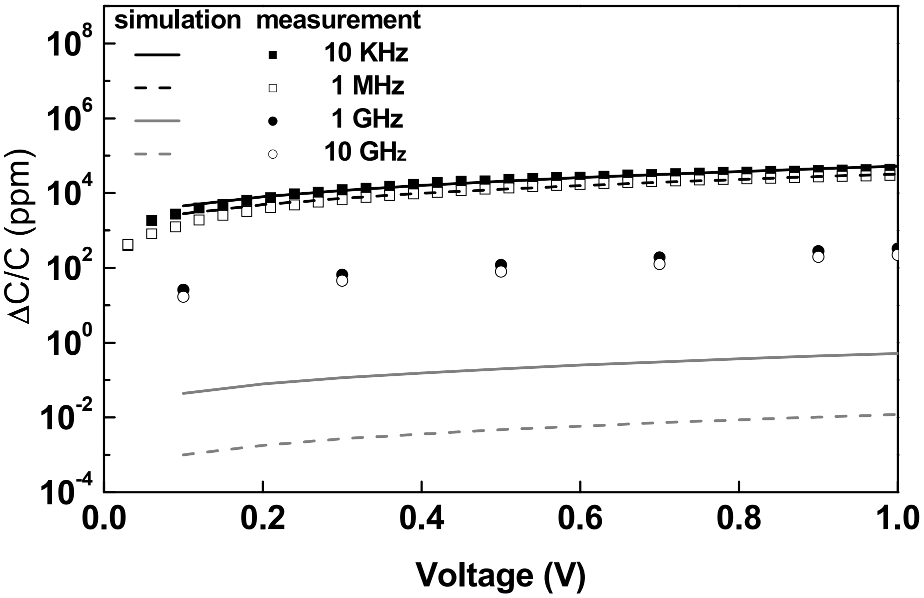


Fig. 7-4. Measured and simulated ΔC/C-V data assuming a nearly constant t. Although good agreement is obtained at 10 KHz and 1 MHz, the assumption fails to account for the 1 GHz and 10 GHz data.

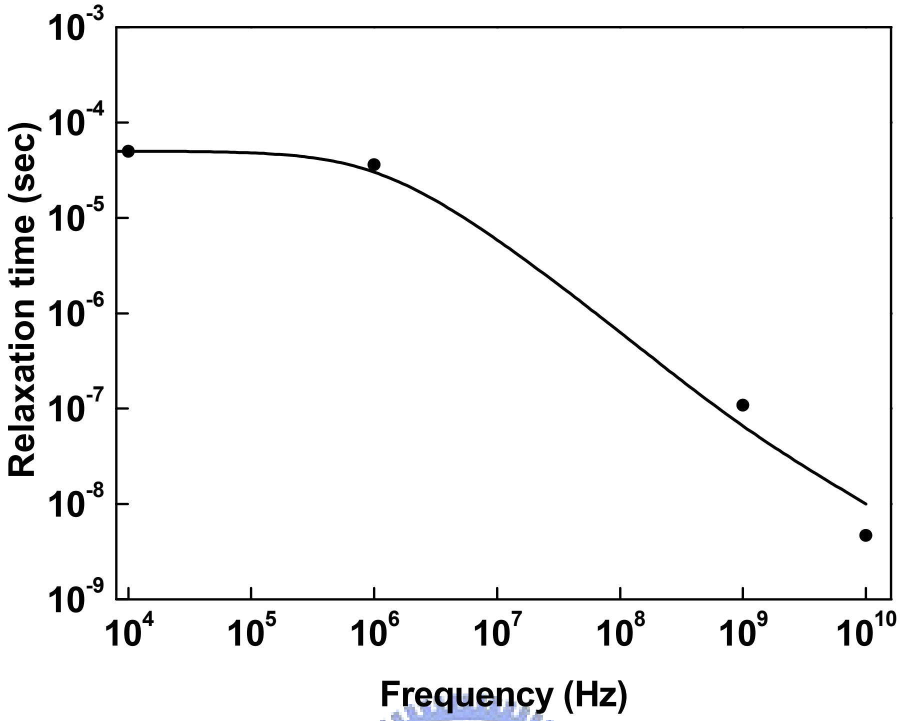


Fig. 7-5. Modified carrier relaxation time as a function of frequency using a $[1+(f/f_0)2]$-1/2 pre-factor.

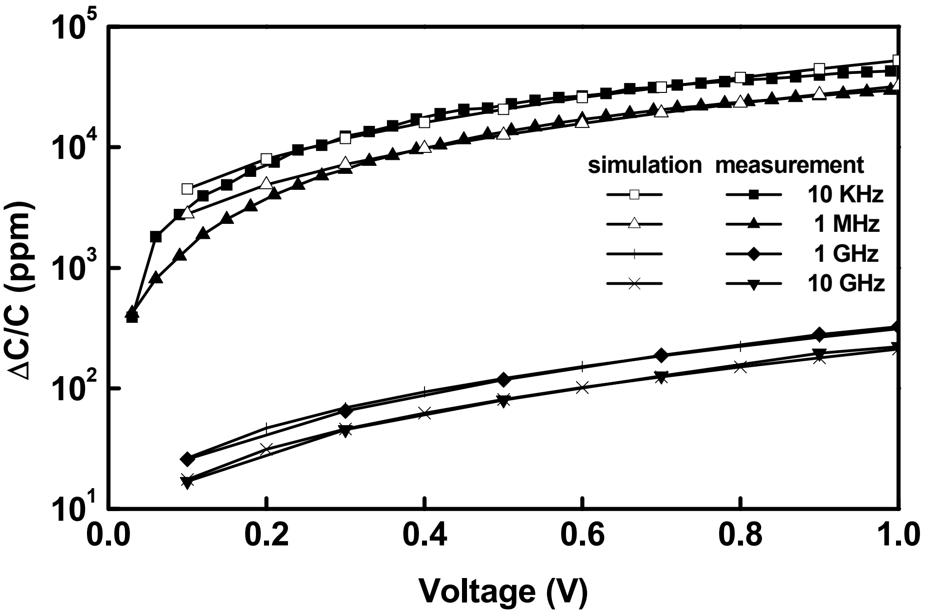


Fig. 7-6. Measured and simulated ΔC/C using the frequency dependent relaxation time shown in Fig. 7-5.

Chapter 8

The Conclusion of High-κ MIM Capacitor with Al doped TaO_x Dielectrics

8.1 Conclusion

We have achieved record high 17 fF/μm^2 capacitance density, small 5% capacitance reduction to RF frequency range, small $\Delta C/C \le 120$ ppm at 1 GHz, and low leakage current of 8.9×10^{-7} A/cm^2 using high-κ Al doped TaO_x MIM capacitors and processed at 400^{o}C. This high capacitance density with good device integrity can greatly reduce the chip size of RF circuits and be useful for precision circuit application at high frequencies.

We also show the space charge relaxation in the dielectrics and use it to derive the free carrier injection model to describe the frequency-dependence and voltage-dependence of capacitance ($\Delta C/C$) for high-κ MIM capacitors.

Although the free carrier injection model can fit well the voltage-dependence of capacitance ($\Delta C/C$) for high-κ MIM capacitors, the nearly constant relaxation time (τ) assumption can not match the measured fast reduction of $\Delta C/C$ as frequency increases into GHz regime. We using a modified free carrier injection model with an additional pre-factor to account for the frequency dependence of the relaxation time, good agreement between the frequency dependence of the measured and modeled voltage dependence of the capacitance, $\Delta C/C$-V, has been obtained for high-κ Al doped TaO_x MIM capacitors. This simple model should be helpful in simulations of circuits that include MIM high-κ dielectric capacitors.

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論文題目：

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