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碩 士 論 文

深次微米部分空乏型矽在絕緣層上金氧半場
效電晶體之低頻雜訊特性研究

Low-Frequency Noise Characterization of Deep Submicron Partially-Depleted SOI MOSFETs

研 究 生 ： 胡 心 卉

指導教授 ： 張 俊 彥 博士

陳 坤 明 博士

中 華 民 國 九 十 三 年 六 月

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研 究 生：胡 心 卉　　Student：Hsin-Hui Hu

指導教授：張 俊 彥 博士　　Advisor：Dr. Chun-Yen Chang

陳 坤 明 博士　　Dr. Kun-Ming Chen

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摘要

近年來，由於矽在絕緣層上互補式金氧半場效電晶體(SOI CMOS)的先天結構優勢，使其成為積體數位以及射頻應用方面的新選擇。然而，由部分空乏型 SOI 金氧半場效電晶體中的基體懸浮效應抑或界面陷阱所產生的低頻雜訊卻會在電路或是系統中造成問題。此外，它也是射頻類比電路中一項重要的評量指標。在本篇論文中，我們將探討部分空乏型 SOI 金氧半場效電晶體的低頻雜訊分別在基體懸浮和基體接地時，隨汲極偏壓、溫度、通道長度變化的特性。實驗中，我們使用 HP4156A 半導體參數分析儀來量測元件的電流電壓特性。而低頻雜訊的量測則是同時結合了 BTA9812 雜訊分析儀以及 HP35670A 動態訊號分析儀來完成。

在基體懸浮元件中，由於基體懸浮效應，因此可以觀察到一個似羅倫茲雜訊過沖(Lorentzian-like noise overshoot)；此雜訊過沖在較高的汲極偏壓、溫度以及較短的通道長度下會被抑制。這裡我們採用一種以汲極到基體接面漏電所產生的散彈雜音(shot noise)和源極到基體阻抗，彼此間之交互作用為基礎的模型來解釋所觀察到的雜訊行為。在基體接地的元件中，雜訊過沖會被抑制住，而且只能觀察到閃爍雜音(flicker noise)。由閘極所看入的閃爍雜音在線性區正比於所施加的閘極電壓平方以及反必於通道長度，並且和溫度的改變無關。這表示，部分空乏型元件中的閃爍雜音主要是由通道中陷阱所產生的移動率擾動所造成的。

此外，在論文中也探討了熱載子效應對 SOI 元件中低頻雜訊的影響。在經過熱載子應力之後，由於閘極引發的汲極漏電流(GIDL)增加，使得基體懸浮元件中的似羅倫茲雜訊過沖會往較高的頻率移動，而雜訊的平台值會減小。再者，經過熱載子應力後，如果交換源極和汲極，所量測到的雜訊過沖，將因基體懸浮效應的降低而被抑制。至於閃爍雜音，不論在基體懸浮元件還是基體接地元件中都會因為應力後介面缺陷態的增加而增加。

Low-Frequency Noise Characterization of Deep Submicron Partially-Depleted SOI MOSFETs

Student: Hsin-Hui Hu

Advisor: Dr. Chun-Yen Chang
Dr. Kun-Ming Chen

Institute of Electronics
National Chiao Tung University

Abstract

In recent years, SOI CMOS have been proposed as a candidate for integrated digital and RF applications due to its inherent predominance. However, the low-frequency noise in partially depleted (PD) SOI MOSFETs due to floating-body effect or interface trap would cause problems in circuit or system, and also be an important figure-of-merit for RF analog circuits. In this thesis, we investigate the low-frequency noise characteristics of PD SOI MOSFETs with floating-body structure and source-to-body-connected structure at various drain biases, temperatures, and channel lengths. The current-voltage characteristics of devices were measured using HP4156A semiconductor parameter analyzer. The low-frequency noise measurements were performed using a BTA9812B noise analyzer in conjunction with an HP35670A dynamic signal analyzer.

For floating-body devices, a Lorentzian-like noise overshoot was observed due to floating body effect. The noise overshoot can be suppressed at high drain bias, high temperature, and short channel length. A model based on the interaction between the shot noise of the drain-body junction leakage and the source-body impedance has been adopted to explain the noise behavior. For source-to-body-connected structure, the noise overshoot was

suppressed and only 1/*f* noise existed. The input-referred 1/*f* noise is proportional to the square of gate drive voltage and the reciprocal of gate length in linear operation, and is independent of temperature. It suggests that the 1/*f* noise in PD devices is dominated by the trap-induced mobility fluctuation in the channel.

The hot-carrier effect on the low-frequency noise of SOI devices has also been studies in this thesis. After hot-carrier stress, the Lorentzian-like noise overshoot in floating-body device moves to higher frequencies and the plateau of the noise overshoot reduces due to the increase of gate-induced-drain-leakage current. Moreover, as the source and drain interchanged, the noise overshoot can be eliminated with the reduction of floating body effect after stress. For both floating-body and source-to-body-connected devices, the 1/*f* noise increases after stress due to the increase of interface states.

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Chapter 1

Introduction

1.1 Characteristic of Silicon-On-Insulator MOSFETs

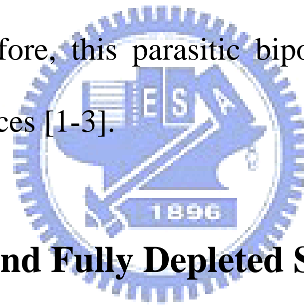
1.1.1 Merit of SOI MOSFETs

Silicon-on-insulator (SOI) CMOS technology is currently considered a likely candidate for integrated digital and RF circuit applications, since it provides full dielectric isolation and reduced junction capacitance as compared to bulk-Si MOSFET. The substrate used in SOI technology includes silicon-on-sapphire, silicon-on-nitride, silicon-on-spinel, and silicon-on-oxide…etc., this insulator layer we discuss in this thesis is based on the oxide layer.

For SOI MOSFETs, the parasitic capacitances from drain to bulk and source to bulk are dominated by the buried oxide capacitance. Because the dielectric constant of buried oxide (ε_{ox}=3.9) is smaller than that of silicon (ε_{Si}=11.9), the junction located on buried oxide gives rise to a parasitic capacitance approximately three times smaller than that of a bulk junction. Therefore, the junction capacitances in SOI MOSFETs are smaller than those in bulk MOSFETs. As a result, the device has higher response speed and lower power consumption properties. Moreover, the isolation provided by the buried oxide has excellent immunity to against high energy particle illumination which results in the generation of electron-hole pairs and leads to a large amount of current. Hence, the leakage induced by radiation and the substrate junction of MOSFETs can be reduced. Besides, the thickness of the Si active layer can only be 50nm, which is good for producing ultra-shallow junctions to restrain the short channel effect. For SOI CMOS devices, because of the absence of the n-well and p-well, the

latch-up which caused by the parasitic npn and pnp BJTs in the well and the substrate will not happen. In addition, the isolation between devices can be performed by etching the Si film because of the thinner Si active layer only 50-200nm. Therefore, the SOI CMOS technology has a higher device density and a simple isolation process.

Although the buried oxide provides many advantages, it still leads to some drawbacks: self heating and floating body effect. The former is due to the low thermal conductivity of the buried oxide; hence it is less efficient to remove the excess heat than bulk MOSFETs. The later is because of a parasitic bipolar transistor in SOI MOSFETs. If we consider an n-channel device, the N^+ source, the P-type body and the N^+ drain indeed form the emitter, the base, and the collector of an NPN bipolar transistor. In a bulk device, the base of the bipolar transistor is usually grounded by means of a substrate contact. However, in an SOI device, the body (base) is usually left floating. Therefore, this parasitic bipolar transistor is the origin of several undesirable effects in SOI devices [1-3].



1.1.2 Partially Depleted and Fully Depleted SOI MOSFETs

According to the thickness of the silicon film, two types of devices can be distinguished: partially-depleted device (PD) and fully-depleted devices (FD), as shown in Fig. 1-1. If the silicon film is thick enough that the depletion region of the top portion and the bottom portion can not overlap, then there exists a piece of neutral region in the body. Such SOI MOSFETs is called PD device. On the contrary, if the silicon film is thin enough to let these two depletion regions overlap, this type of SOI MOSFETs is called FD device.

In PD SOI devices, because the depletion region is independent of the Si film thickness, the threshold voltage is insensitive to the film thickness and is the same as in a bulk transistor. However, the PD SOI devices will suffer floating body effect, which will be discussed in section 1.1.3, and create some undesirable phenomena. When the body is connected to ground, the floating body effect can be suppressed and the device is similar to bulk device. Moreover,

the suppression of the floating body effect with body contact can also reduce the kink-related excess noise in SOI MOSFETs at low frequency [4-5]. Although FD SOI MOSFETs have excellent performance compared with PD SOI devices, PD SOI technology is attractive for manufacturing because the substrate and source/drain doping engineering in bulk technology is applicable to PD devices, and the controllability over SOI film thickness is much better in PD SOI than in FD SOI technology.

In FD SOI devices, the produced one–dimensional character to the electric field line results in neutrally kink-free, if the back interface is not in accumulation. Generally speaking, the FD SOI devices have better DC properties, such as higher transconductance, smaller short channel effect, lower threshold voltage, and higher subthreshold swing, than the PD SOI devices. The larger gate control capability over the silicon film results in higher transconductance. And the smaller short channel effect which limits gate control of the channel in sub-micron devices is due to the one–dimensional field line. Besides, FD SOI devices are more suitable for the low power and low voltage applications according to reduced threshold voltage and parasitic capacitances. Owing to the thinner film in FD devices, shallower junctions could automatically be formed making reduced threshold voltage roll-off when devices shrink. However, owing to the relation of the depletion width and the Si film thickness, the threshold voltage is sensitive to the Si film thickness, and may vary with the process. Therefore the uniformity of SOI thickness also leads to the variation of threshold voltage from one device to another one or from this die to another die.

1.1.3 Floating-Body Effect

Owing to the buried oxide isolation, the charges caused by impact ionization store in the floating body, resulting in many undesirable phenomenons. These various phenomenons are generically referred to as *floating-body effects*.

The kink effect denotes an abrupt increase in the saturation current of partially depleted

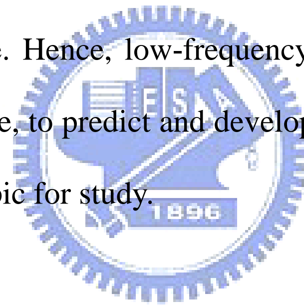
enhancement-mode SOI MOSFETs operated in strong inversion, as shown in Fig. 1-2. As the drain voltage increases, the impact ionization occurs, which leads to the generation of the electron and hole pairs. The electrons flow into the drain, and the holes flow into the body. Owing to the existence of buried oxide, the holes stored in the floating body will raise the body potential and let the threshold voltage to be reduced. Thereby causing an excess drain current and producing many more electron-hole pairs through the avalanche process. This positive feedback results in a sudden increase in drain current or "kink" in I_D-V_D characteristics. For source-to-body-connected PD device, the "kink" disappeared due to body contact (see Fig. 1-3). This suggests that the body contact can release the holes stored in the body and reduce the body potential.

The generation of majority carriers, holes, by impact ionization near the drain can give rise to an increase of body potential and decrease of the threshold voltage. Sometimes, a similar effect can occur at gate voltages lower than the threshold voltage. If the drain voltage is high enough, impact ionization can occur in the subthreshold region, even though the drain current is very small. When the gate voltage is increased, the weak inversion current can induce impact ionization in the high electric field region near the drain, resulting in the generation of the holes and the increase of the body potential. Therefore, the threshold voltage is reduced and the I_D-V_G curve shifts to the left, as shown in Fig. 1-4. For source-to-body-connected PD device, the holes can be released by body contact and the deviation can be suppressed as shown in Fig. 1-5 [6].

1.2 Motivation

Recently, the rapid growth of the portable communication market requires the miniaturization of the whole system with as little power consumption as possible, leading to the trend of the integration of systems on a single chip. Therefore, SOI CMOS is a potential

candidate for integrated digital and RF applications due to its reduced junction capacitances, and good isolation which let SOI has some superior properties: high speed, low power consumption, higher device density [7-8]. However, as opposed to such optimistic condition, there are some hurdles to overcome. One of the technical problems is related to the floating operation of the partially-depleted devices, when the impact-ionization current near the drain is generated for the sufficiently large drain voltage, it gives rise to the well known kink in the drain current. Associated with the kink is a drastic increase of the low-frequency noise in devices for analog circuit application. The low-frequency noise can be up-converted in RF homodyne mixers and voltage-controlled-oscillators (VCOs), resulting in phase noise [9]. It places a fundamental limit on signal detection and spectral purity. For low-voltage analog circuit operation, low-frequency noise becomes even more important, because it needs tighter control on circuit performance. Hence, low-frequency noise is an important figure-of-merit for RF analog circuit. Therefore, to predict and develop approaches to suppress the amount of noise in SOI is a significant topic for study.



1.3 Organization of the Thesis

This thesis is divided into six chapters. In chapter 2, the theory of the low-frequency noise in PD SOI MOSFETs including 1/*f* noise and kink related excess noise will be described in detail. In chapter 3, the low-frequency noise in PD SOI MOSFETs with floating-body and source-to-body-connected structures were measured. The noise characteristics of the devices at different channel lengths were discussed. In chapter 4, we discussed the low-frequency noise in PD SOI MOSFETs operating from linear region to saturation region at various temperatures. In chapter 5, the degradation of low-frequency noise in PD SOI MOSFETs after hot-carrier stress was discussed. Finally, some conclusions about the measured results and future work were given in Chapter6.

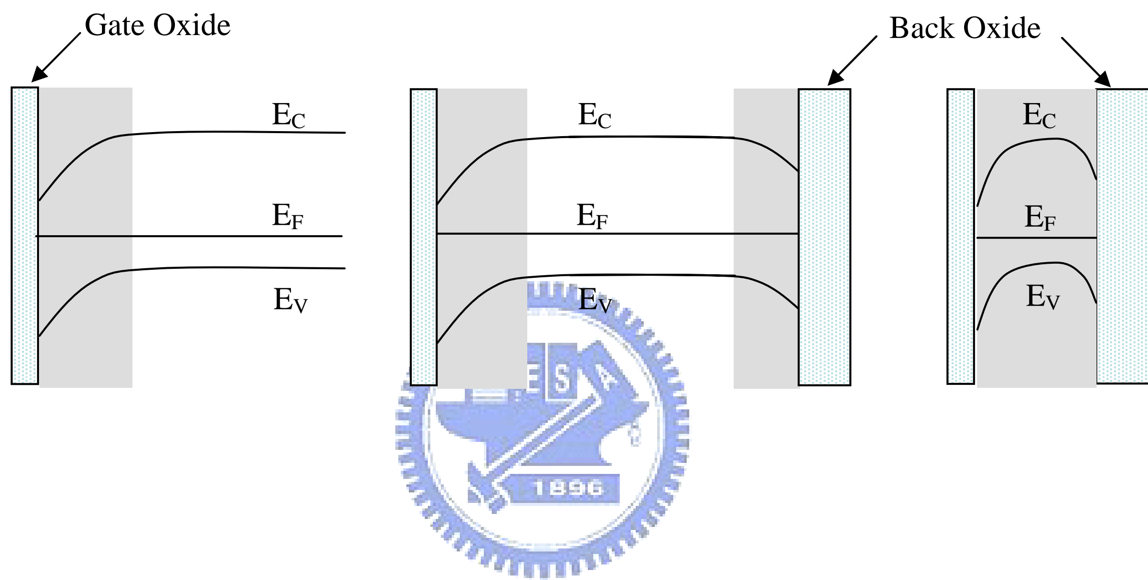


Fig. 1-1 Band diagram in (a) bulk, (b) PD SOI, and (c) FD SOI. The shaded areas represent the depleted region.

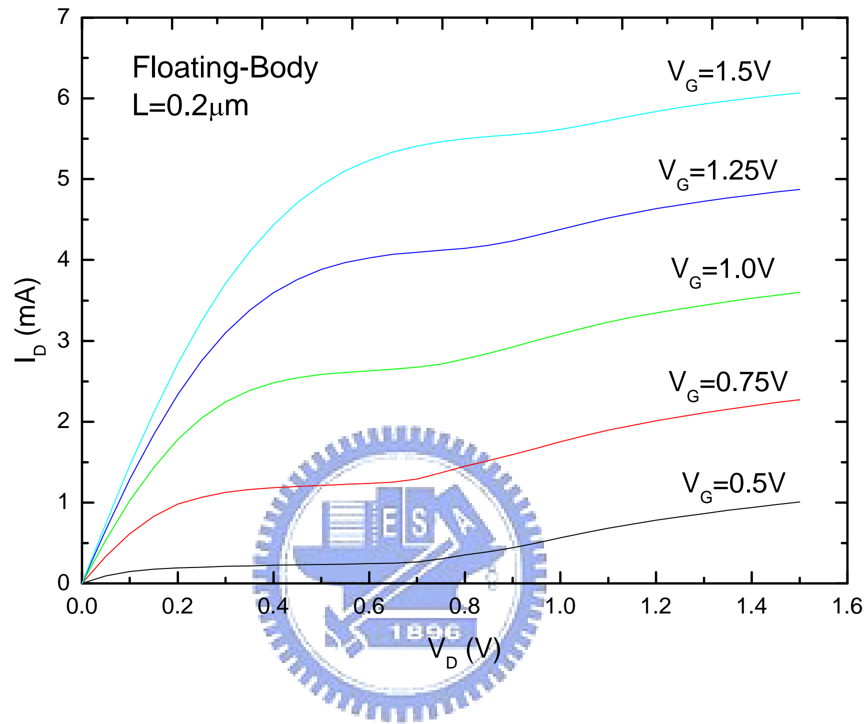


Fig. 1-2 I_D-V_D characteristic of a PD floating-body SOI MOSFET at different gate biases with L=0.2μm.

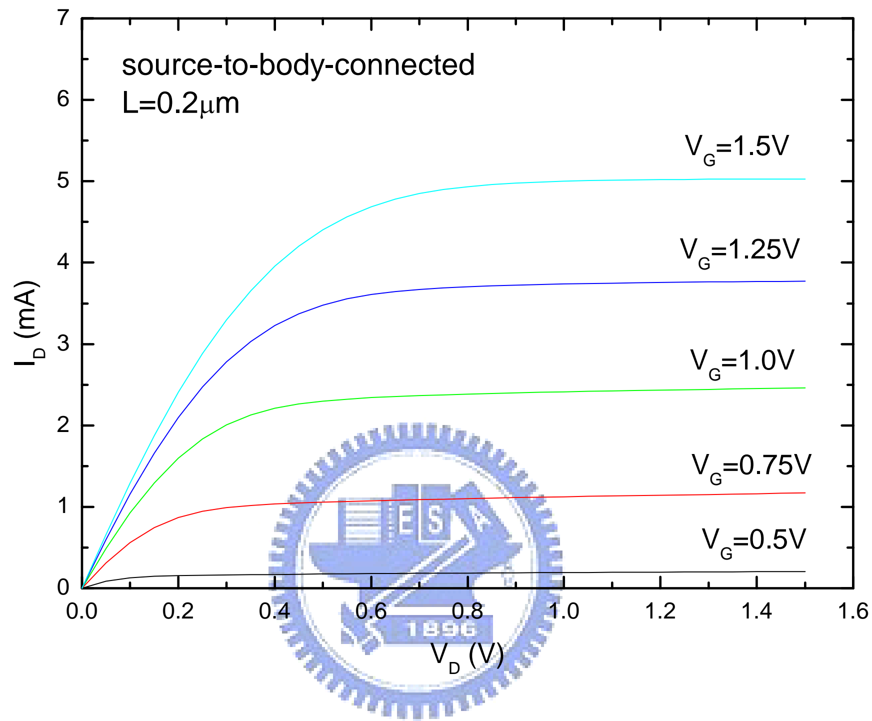


Fig. 1-3 I_D-V_D characteristic of a PD source-to-body-connected SOI MOSFET at different gate biases with L=0.2μm.

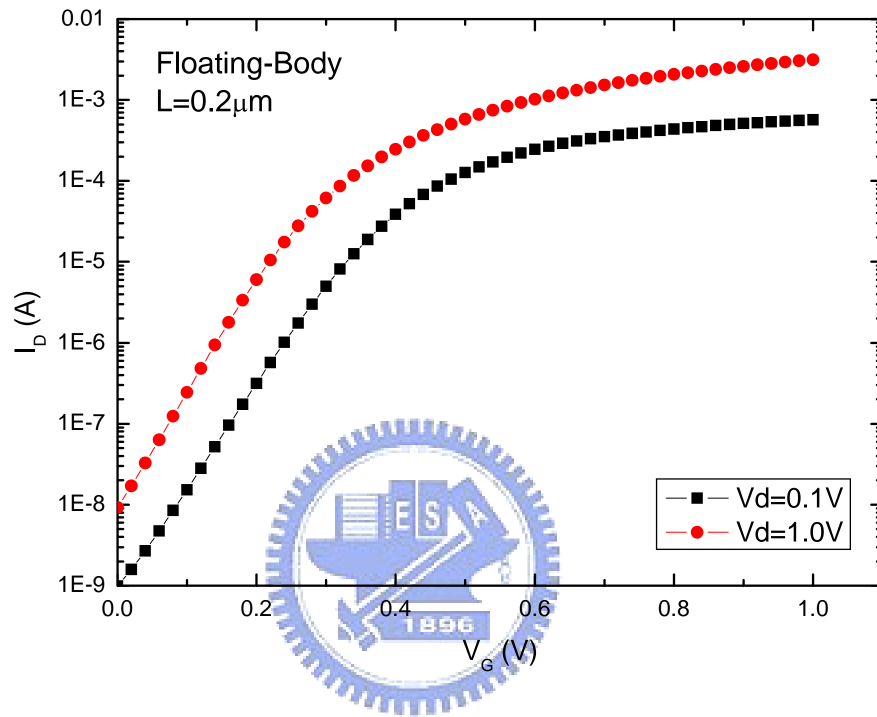


Fig. 1-4 I_D-V_G characteristic of a PD floating-body SOI MOSFET at V_D=0.1V and 1.0V with L=0.2μm.

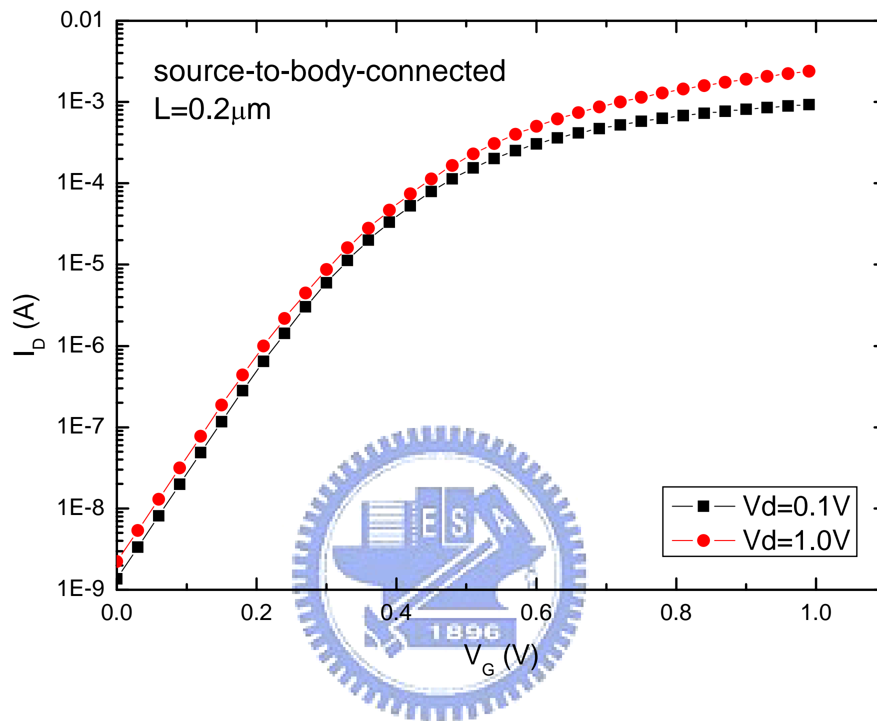


Fig. 1-5 I_D-V_G characteristic of a PD source-to-body-connected SOI MOSFET at V_D=0.1V and 1.0V with L=0.2μm.

Chapter 2

Theory of Low-Frequency Noise in PD SOI MOSFETs

The low-frequency noise in PD SOI MOSFETs includes 1/*f* noise and kink related excess noise (also called Lorentzian-like noise overshoot) as shown in Fig. 2-1 where kink related excess noise superimposed on the 1/*f* noise. Among the total, 1/*f* noise is associated with the conductance fluctuation in channel and kink-related excess noise is associated with the body potential fluctuation due to floating-body effect.

2.1 1/*f* noise in PD SOI MOSFETs

The 1/*f* noise in PD SOI MOSFETs is common to all types of MOSFETs. The source of this noise comes from a fluctuation in the conductivity. There are two competing models appeared in the literature to explain it: the McWhorter carrier number fluctuation theory and the Hooge mobility fluctuation theory. There is experimental evidence to support both theories, and thus the literature is mostly split into two camps over the issue.

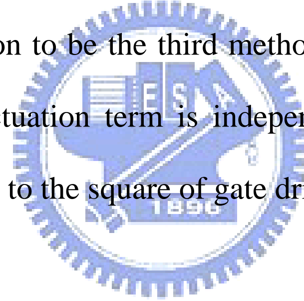
The number fluctuation theory is attributed to random trapping and detrapping processes of charges in the oxide traps near the Si-SiO_2 interface, i.e. the channel can exchange charges with the oxide traps through tunneling. Besides, this model is based on the concept of generation recombination noise and such kind of noise usually occurs at the interface or junction of semiconductors. Therefore, number fluctuation theory is a surface effect. The traditionally derived result of the number fluctuation model for uniform trap distribution is:

$$S_{VG} = \frac{kTq^2}{8WLC_{ox}^2\alpha} \cdot \frac{N_t(E_{fn})}{f} \quad \left(V^2/Hz\right) \tag{2-1}$$

where $\alpha = (2m_e^* \phi_B / \hbar^2)^{1/2}$ is typically taken to equal 10^8cm^{-1}, $N_t(E_{fn})$ is the oxide trap density adjacent to the electron quasi-Fermi level in silicon, and f is the frequency in Hertz. From equation (2-1), the gate voltage noise power spectral density is independence of the gate voltage and proportional to $1/WLC_{ox}^2$ [10].

The mobility fluctuation theory, based on Hooge's relation, is an empirical model able to fit noise data in homogeneous semiconductors and devices. Hooge considers the $1/f$ noise as a result of the fluctuation in bulk mobility and is no surface effect. When Hooge's relation is directly applied to MOSFET's, it predicts an equivalent gate voltage noise power spectral density which is proportional to $(V_{GS} - V_T)/(WLC_{ox})$ [11].

Except the model we discuss above, some people proposed the theory combining with number and mobility fluctuation to be the third method. And it becomes the popular one. In such models, the number fluctuation term is independence of gate bias; and the mobility fluctuation term is proportional to the square of gate drive voltage [10], [12].



2.2 Kink related excess noise in PD SOI MOSFETs

Due to the floating body, SOI MOSFETs exhibit a low frequency kink-related noise overshoot, which has a Lorentzian spectrum: a flat low-frequency plateau, with constant amplitude, followed by a $1/f^2$ roll-off. Therefore, the kink-related excess noise is also called Lorentzian-like noise. Several mechanisms have been proposed to explain this excess noise, such as trap-assisted generation- recombination (G-R) noise caused by the defects in body region [13], G-R noise induced by back interface state caused by the defects at bottom Si-SiO_2 interface [14], and shot noise amplified by the floating body effect [15]. In early years, owing to the worse process, the G-R noise is the main source of the excess noise. At present, the technology of the process is quite advanced, thus the defects in Si film and bottom Si-SiO_2 interface are fewer and fewer. Therefore, shot noises from source to body and drain to body

become the major sources. The shot noise sources from drain to body and source to body result from the drain-body junction leakage (I_L) and body-source diode current (I_{SB}) respectively (see Fig. 2-2). Although both are shot noises generated by flow of carriers surmounting energy barriers, they are independent noise sources. However, these two noises are basically the same, because in SOI I_L is roughly equal to I_{SB} as a result of current balancing in the body of SOI device. Here we defined the region, which the drain bias is smaller than the dc kink onset voltage, as “pre-kink region”. On the contrary, when the drain bias is larger than the dc kink onset voltage, the region is defined as “post-kink region” (see Fig. 2-3). In the pre-kink region, where the drain voltage is small, impact ionization can be neglected; therefore I_L is dominated by junction thermal generation current (I_G). In the post-kink region, where the drain voltage is large enough to lead to impact ionization, the I_L is dominated by impact ionization current (I_{ii}).

The shot noise originates in the I_L and I_{SB} are small in magnitude compared with flicker noise, but the high impedance of source-body junction caused by floating body effect significantly amplifies their magnitude and gives rise to the excess low-frequency noise in PD SOI MOSFET. From the shot noise model proposed by Jin [16], the shot noises can be express as ($2qI_{SB}+2qI_L$) which are a white noise. The source-body junction impedance (Z_{body}) is the parallel combination of r_{SB} and C_{BB}. These current fluctuations perturb the body voltage through the square of the body impedance with Lorentzian-like shape similar to a RC filter shown in Fig 2-4, and no longer be a white noise [17]. After that, these body voltage fluctuations transferred through the body effect to gate voltage power spectral density (V^2/Hz), as followed:

$$S_{VG,excess} = \overline{i}_{shot}^{2} \times | Z_{Body} |^2 \times \left(\frac{\partial V_{TH}}{\partial V_{BS}}\right)^2 = (2qI_{SB} + 2qI_L) \times \frac{{r_{SB}}^2}{1+\left(2\pi f \cdot r_{SB} C_{BB}\right)^2} \cdot \alpha^2$$

$$= 4q(nV_T)^2 \cdot \frac{1}{1+\left(f/f_0\right)^2} \cdot \frac{1}{I_L} \cdot \alpha^2 = \frac{4(nkT\alpha)^2}{qI_L} \cdot \frac{1}{1+\left(f/f_0\right)^2} \qquad (2\text{-}2)$$

where α (= ∂V_{TH}/∂V_{BS}, where V_{BS} is the body voltage) is the body factor, r_{SB} (≅ nV_T/I_L) is the

source-body junction resistance, C_{BB} is the body-ground capacitance, and $f_0 = qI_L/(2\pi\ nkTC_{BB})$. Therefore, the corner frequency f_0 is proportional to I_L and the plateau is proportional to $1/I_L$.

As the operation mode shifts from PD toward more FD operation, source-body junction diode saturation current, I_R (where source-body junction diode current $I_{SB}=I_R\cdot(\exp(V_{SB}/nV_T)-1)$) exponentially increases due to the reduced source-body junction barrier, as follows:

$$I_R(FD) = I_R(PD) \times e^{qV'_{BS}/kT} \tag{2-3}$$

where V'_{BS} is the reduced junction barrier potential. Exponential increase of I_R in FD SOI devices results in a significant decrease of source-body junction impedance Z_{body} (i.e. shot noise amplified gain). Therefore, the floating body effect is suppressed by an increase of I_R, and I_R has to be included in the excess noise model with a modification of $r'_{SB}=nV_T/(I_{SB}+I_R)$ as

$$\begin{aligned} S_{VG,excess} &= (2qI_{SB} + 2qI_L) \times \frac{r'^{\,2}_{SB}}{1+\left(2\pi f \cdot r'_{SB} C_{BB}\right)^2} \cdot \alpha^2 \\ &= 4q(nV_T)^2 \cdot \frac{1}{1+\left(f/f'_0\right)^2} \cdot \frac{I_L}{(I_R+I_L)^2} \cdot \alpha^2 \end{aligned} \tag{2-4}$$

where $f'_0=1/(2\pi\ r'_{SB}C_{BB})$ and is proportional to I_L+I_R. According to equation (2-3), as the operation toward more FD, I_R will increase and thus lead to the increase of f'_0 and reduction of the plateau. If the magnitude of plateau is smaller than $1/f$ noise, then we can observe only $1/f$ noise, i.e. the shot noise is suppressed.

The other way to reduce excess noise is using body contact. A good body contact provides another low-resistance discharge path for body charges, and the impedance of current fluctuation can drastically reduce (i.e. shot noise amplified gain can reduce), as follows:

$$R_B \parallel Z_{body} < Z_{body} \tag{2-5}$$

where R_B is the body path resistance. The criterion for low frequency noise optimization is to suppress the Lorentzian-like noise overshoot making it less than the underlying 1/*f* noise by decreasing the body transfer function at the desired biases.

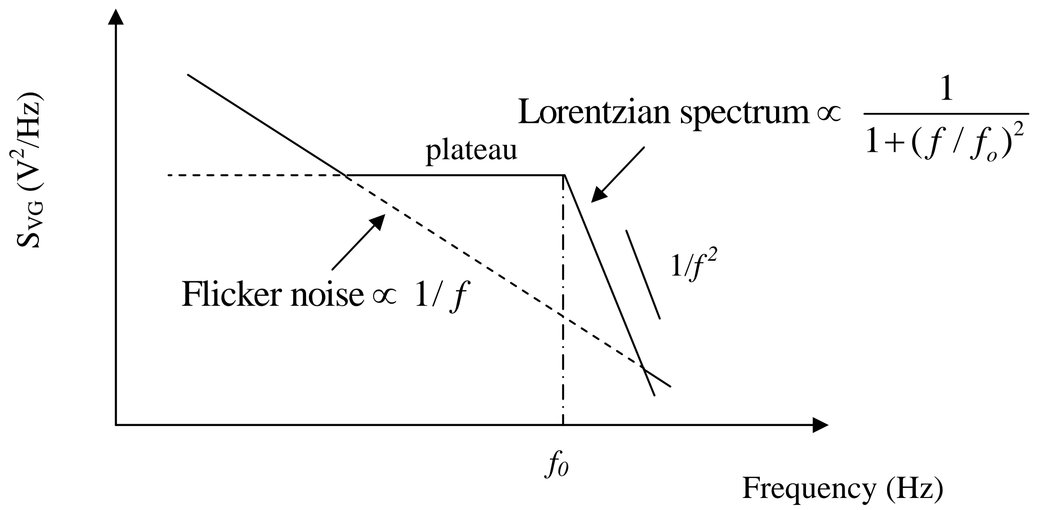


Fig. 2-1 Schematic plot of low frequency noise components

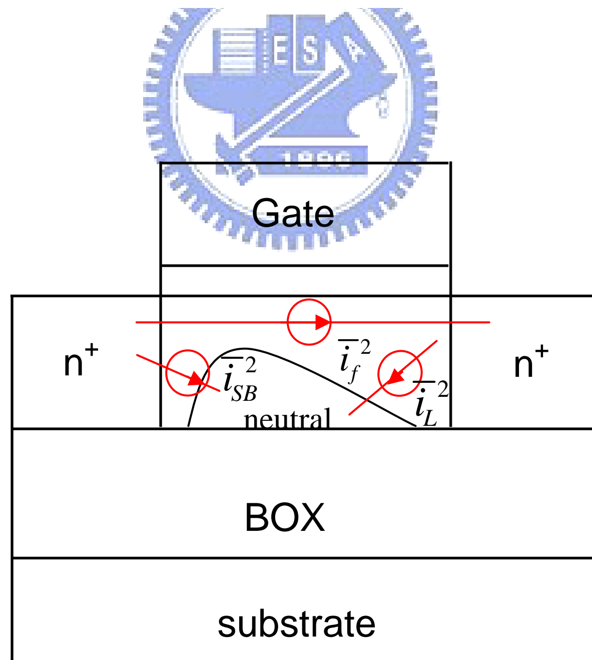


Fig. 2-2 Noise sources in a SOI MOSFET. $\overline{i_f}^2$:1/*f* noise

$\overline{i_{SB}}^2$: shot noise due to body-source diode current

$\overline{i_L}^2$: shot noise due to drain-body junction leakage

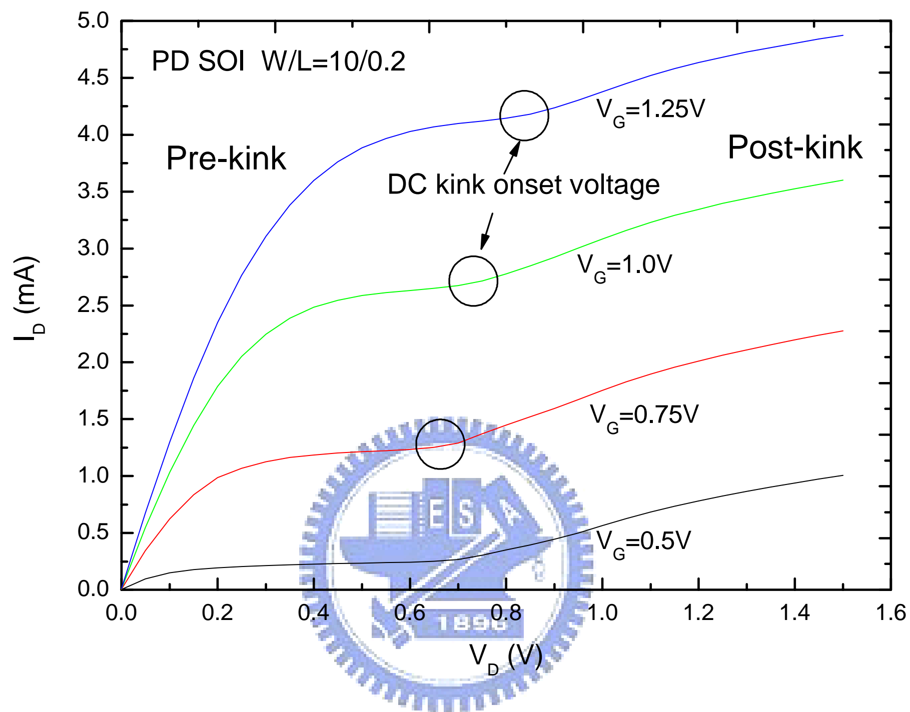


Fig. 2-3 I_D-V_D curves in floating body SOI MOSFET

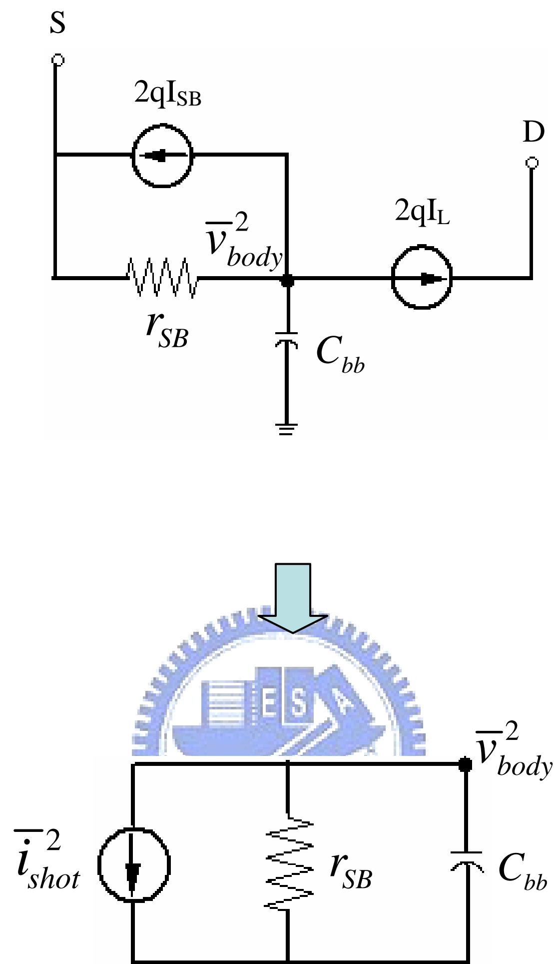


Fig. 2-4 Noise small-signal equivalent circuits for the floating body SOI MOSFET

Chapter 3

Characterization of Low-Frequency Noise in PD SOI MOSFETs

In this chapter, we describe the measurement methods for I-V and low-frequency noise characterization firstly. Then we discuss the noise characteristics of PD SOI MOSFETs with floating-body and source-to-body-connected structures. Because of the continuous scaling-down of devices for better performance, it is important to realize and model the low-frequency noise in SOI MOSFETs after channel shrinking for device process diagnosis and analog circuit simulation. Hence the influence of channel length on the low-frequency noise of PD SOI MOSFETs also has been investigated in this chapter.

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3.1 Devices under Test and Measurement Techniques

3.1.1 Devices under Test

The n-channel MOSFETs were fabricated on Separation by Implantation of Oxygen (SIMOX) substrates with 190nm thick Si active layers, 150nm thick buried oxides, and 1.6nm nitride gate oxides. The floating-body and source-to-body-connected transistors with oxide/SiN spacers and As^+-implanted source/drain junctions are partially depleted. After $CoSi_2$ salicidation, the devices were metalized using a typical backend flow.

3.1.2 I-V Measurement

The DC characteristics of PD SOI MOSFETs were measured using HP4145 or HP4156.

From the I_D-V_G curves, we extract the threshold voltage (V_{TH}), transconductance ($gm= dI_D /dV_G$) and body factor ($\alpha= dV_{TH} /dV_{BS}$) at different channel lengths. We also observed the kink effect from the I_D-V_G and I_D-V_D characteristics.

3.1.3 Noise Measurement

The HP4145, HP35670A Dynamic Signal Analyzer, and BTA9812 Noise Analyzer were employed to measure the low frequency noise at different channel lengths, where the measurement system was fully automated using a personal computer via HP-IB. The measurement frequency range is from 1Hz to 10 kHz, and the output drain current noise power spectrum would be extracted. We divide the output drain current noise power spectrum by the square of the transconductance to obtain the input-referred gate voltage noise power spectrum (i.e. $S_{VG}=S_{ID}/gm^2$).

The devices operate in linear operation are corresponding to a drain voltage V_{DS} = 0.1V. As the drain bias increases to about 0.4V, the devices enter the saturation region, both the data obtained before the kink occurring (V_{DS} = 0.8V) and after the kink occurring (V_{DS} = 1.0V) are shown.

3.2 Low-Frequency Noise in Floating-Body Devices

3.2.1 Low-Frequency Noise at Various Drain Voltages

The low-frequency noise characteristics of a floating-body PD SOI MOSFET at room temperature are shown in Fig. 3-1. Measured noise spectra exist a Lorentzian-like noise overshoot superimposed on the pure $1/f$ noise. The Lorentzian-like noise overshoot has a plateau followed by a $1/f^2$ roll-off at the corner frequency f_0, where the noise is 3 dB under the value at the plateau. The noise overshoot is specific to PD SOI MOSFETs due to the

floating-body effect. The plateau and corner frequency show a strong dependence on the drain bias. When the device operates at high drain bias, the $1/f$ noise, whose magnitude is inversely proportional to the frequency f, is visible at low frequency. It has been reported that the origin of $1/f$ noise is the carrier number fluctuation and the mobility fluctuation, which lead to the $1/f$ noise in MOSFETs.

The equation of the input-referred gate voltage noise proposed by Tseng [15] which we described in Chapter 2 is:

$$S_{VG,excess} = \frac{4(nkT\alpha)^2}{qI_L} \cdot \frac{1}{1+\left(f/f_0\right)^2} \tag{3-1}$$

where kT is the thermal energy, n is the junction ideality factor, q is the elementary charge, $\alpha\,(=dV_{TH}/dV_{BS})$ is the body factor, and I_L is the drain-body junction leakage. The corner frequency of the Lorentzian spectrum is given by $f_0 = qI_L / (2\pi nkTC_{bb})$, where C_{bb} is the capacitance associated to the body. Therefore the plateau is proportional to $1/I_L$, and f_0 is proportional to I_L. The increase of drain bias should increase the junction leakage current I_L, and thus lead to the increase of f_0 and the reduction of the plateau. As the drain bias increases to 1.2V, the impact ionization current will get higher too, and the I_L will increase significantly, so the noise overshoot will be suppressed below the $1/f$ noise in low frequency range.

3.2.2 Low-Frequency Noise at Various Channel Lengths

Fig. 3-2 shows the low-frequency noise characteristics of a floating-body PD SOI MOSFET operating at V_{DS}=1.0V, where the Lorentzian-like noise overshoot was observed explicitly at various channel lengths. When the channel length increases, the plateau increased and the corner frequency f_0 decreased [18]. Since the noise magnitude is related to the I_L, α, and C_{bb}, we extract their values from the plateau and corner frequency of the noise overshoot

in Fig. 3-3 by using equation (3-1). By analyzing the I_L, α, and C_{bb} at different channel lengths, the relation between noise magnitude and channel length can be obtained. For our device under test, the body factor α is nearly independent on channel length and drain bias, and its value is about 0.22. However, the I_L and C_{bb} are strong functions of channel length, as shown in Fig. 3-4 and Fig. 3-5. When V_{DS}=1.0 V, I_L is dominated by impact ionization current because the drain bias we gave exceeds the kink onset voltage. The substrate leakage current due to impact ionization can be expressed as:

$$I_{sub} = I_{DS} \cdot \alpha_i \cdot \Delta L \qquad (3\text{-}2)$$

where α_i is the ionization coefficient, the number of electron-hole pairs generated per unit distance; and ΔL is the length of the pinch-off region. As the channel length increases, the lateral field $((V_D\text{-}V_{Dsat})/L)$ decreases, causing a reduction of α_i. Besides the I_{DS} also decreases as the channel length increases. Therefore, the I_L is proportional to $1/L^{\gamma}$, where γ is affected by the total influence of I_{DS} and α_i, as shown in Fig.3-4. As the drain voltage reduces, and the device operates in the pre-kink region (V_{DS}=0.8 V), the extracted value of I_L is nearly independent on channel length as opposed to that at V_{DS}=1.0 V (see Fig. 3-4). It is because the I_L is dominated by the thermal generation current in pre-kink region and can be expressed as:

$$J_R = q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \frac{qn_iW}{\tau_e} \qquad (3\text{-}3)$$

Therefore, the I_L is independent on channel length. In Fig. 3-5, the C_{bb} increases monotonously with increasing the channel length. As the channel length increases, the capacitances from body to gate and body to substrate increase due to the increasing of channel area. However, the capacitances from body to source and body to drain are independent on channel length. Therefore, the slope of C_{bb} curve is less than unity.

3.3 Low-Frequency Noise in Body-to-Source-Connected Devices

The input noise spectrum of a body-to-source-connected PD device is shown in Fig. 3-6, where the channel length is 0.2 μm, and V_{DS}=0.1 V. We observed that the noise spectrum is dominated by 1/*f* noise. This suggests that the source-to-body connection can suppress the noise overshoot efficiently. This is because the body contact provides a low-resistance discharge path for body charges, where the source-body impedance reduces drastically by the parallel combination of R_B and Z_{body}. The R_B is the body path resistance and Z_{body} ($=r_{SB}/(1+j(2\pi f \cdot r_{SB}C_{BB}))$) is the source-body impedance [19]. Once the source-body impedance reduces by body contact, the shot noise amplified gain would be reduced. Therefore, only 1/*f* noise would be observed in source-to-body-connected devices.

In MOSFETs, the 1/*f* noise magnitude is usually related to the interface trap density between the silicon film and the gate oxide. A model, proposed by Gross [20], demonstrated that the noise in MOSFET is due to the fluctuation of the carrier number in the channel and that these fluctuations induce local correlated fluctuations in the channel mobility. When the device operates in linear region and a uniform distribution of oxide/silicon interface traps in activation energy is assumed, the input-referred voltage noise can be written as [20]:

$$S_{VG} \cong \frac{4q^2 x_0 (kT)^2 N_T(E_f)}{fWLC_{ox}^2}(1+\mu_0 SN)^2 \tag{3-4}$$

, where W, L, C_{ox}, μ_0, and S are the gate width, gate length, gate oxide capacitance, channel mobility, and scattering parameter, respectively. $N_T(E_f)$ is the trap number near Fermi energy E_f, and the traps lie in the oxide distributed over some region x_0 near the interface. N is the channel carrier number and is proportional to the gate drive voltage. From the equation (3-4), it is clear that the 1/*f* noise can stem from processing-induced variations in either the near-interface trap density N_T, or in the scattering parameter S, for fixed operation conditions

and device area. If the induced mobility fluctuation term $\mu_0SN << 1$, the induced mobility fluctuation can be neglected, and the noise power spectrum is independence of the gate drive voltage. On the contrary, if the term $\mu_0SN >> 1$, the noise magnitude is proportional to the square of gate drive voltage as shown in the Fig. 3-7. Hence, the $1/f$ noise component is dominated by induced mobility fluctuation. Fig. 3-8 shows the input noise spectrum versus channel length for a device operating at V_{DS}=0.1 V. As shown in Fig. 3-8, the input noise spectrum is proportional to $1/L$, which is consistent with the equation (3-4).

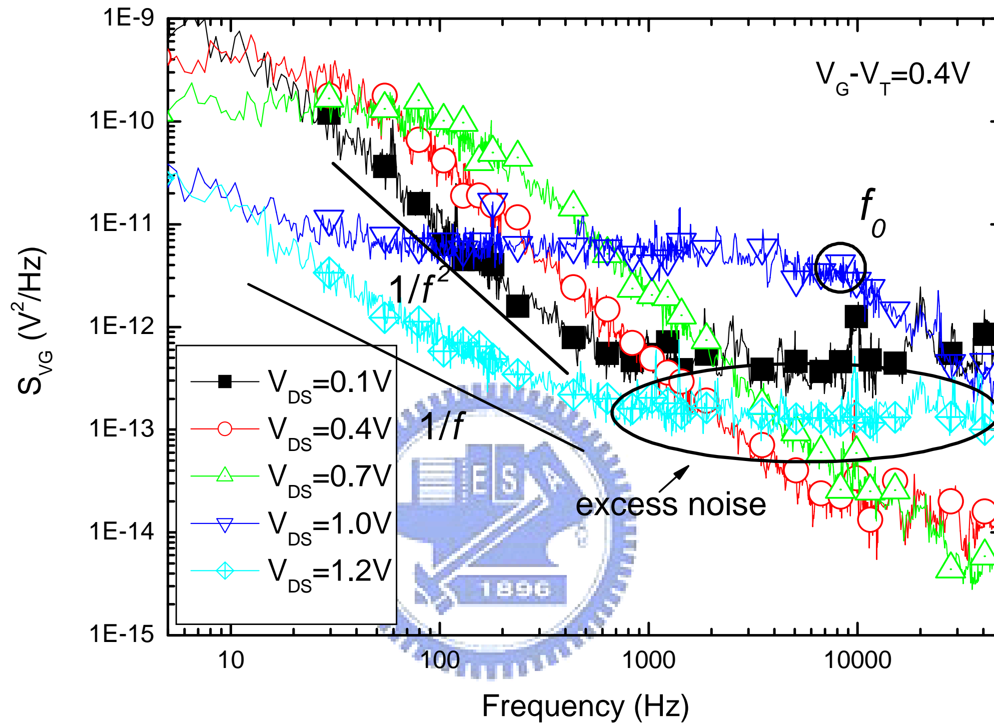


Fig. 3-1 Input referred noise spectra of a PD floating body SOI MOSFET with different drain biases.

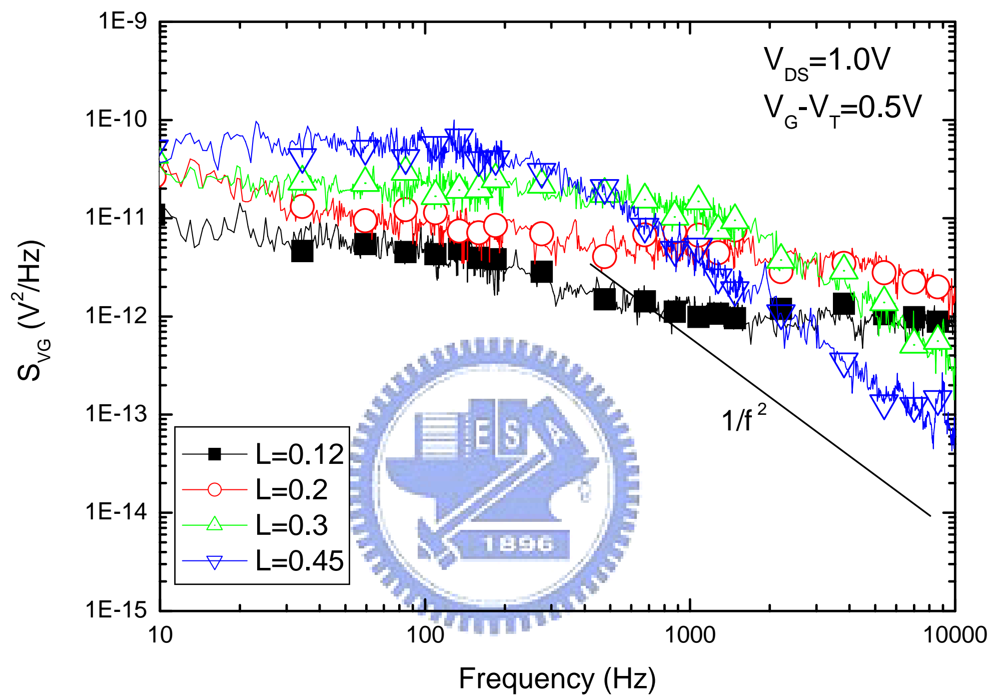


Fig. 3-2 Input-referred noise spectra of a PD floating-body SOI MOSFET at V_{DS} = 1.0V with different channel lengths.

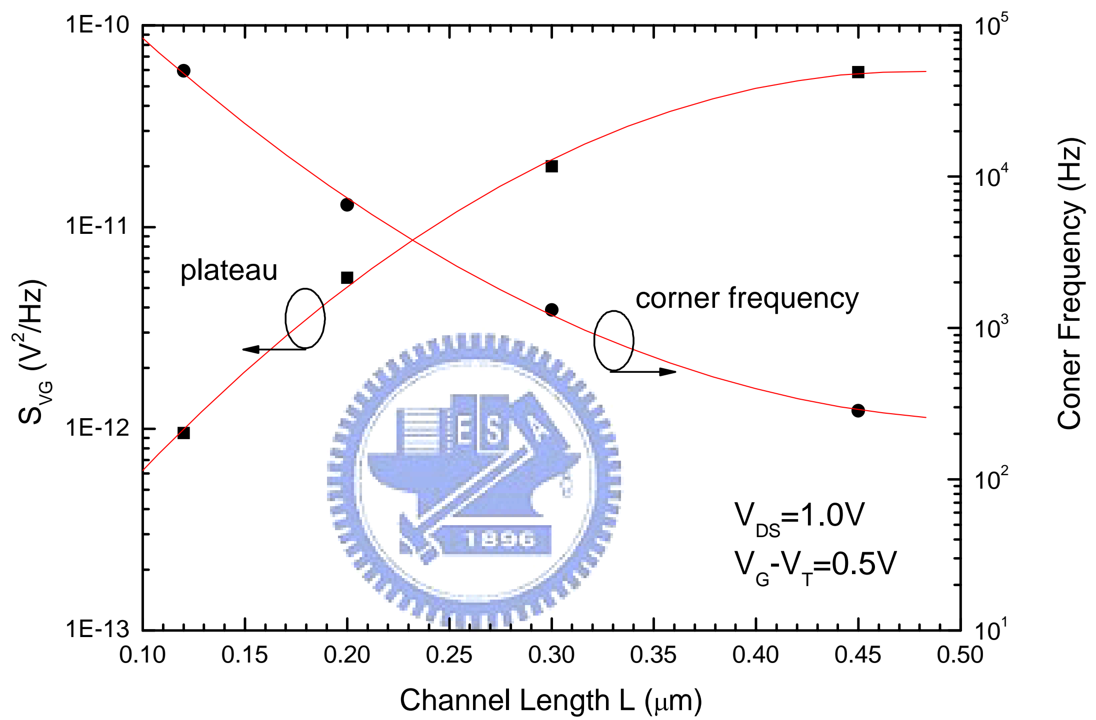


Fig. 3-3 Plateau and corner frequency of the input-referred noise for a PD floating-body SOI MOSFET at V_G-V_T = 0.5V and V_{DS} = 1.0V with different channel lengths.

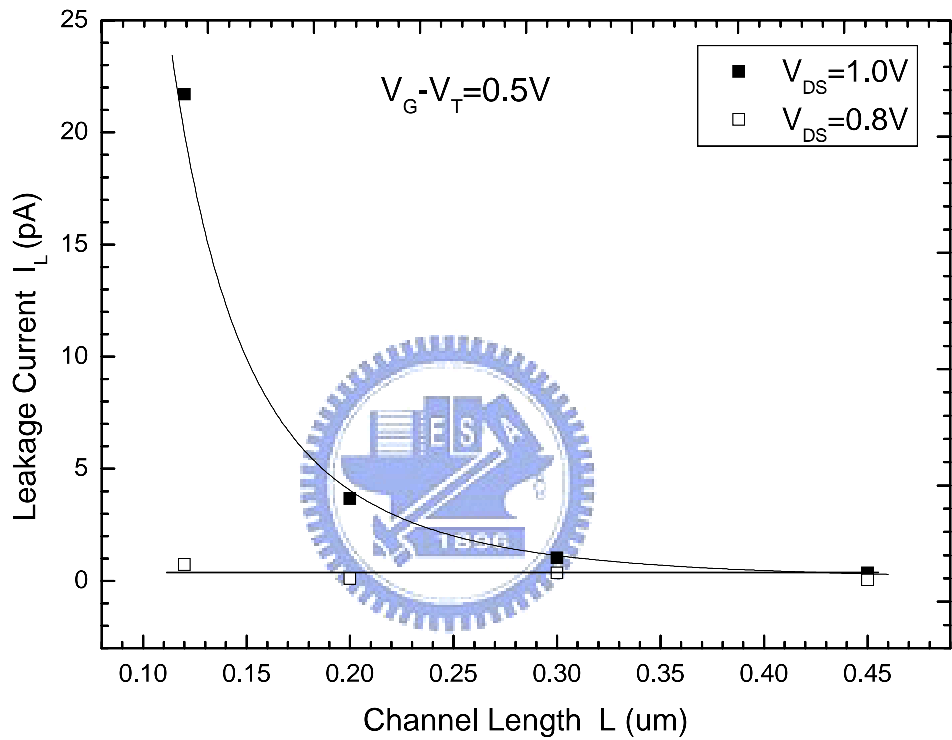


Fig. 3-4 Drain-body junction leakage current as functions of channel length for a PD floating-body SOI MOSFET with different drain voltages.

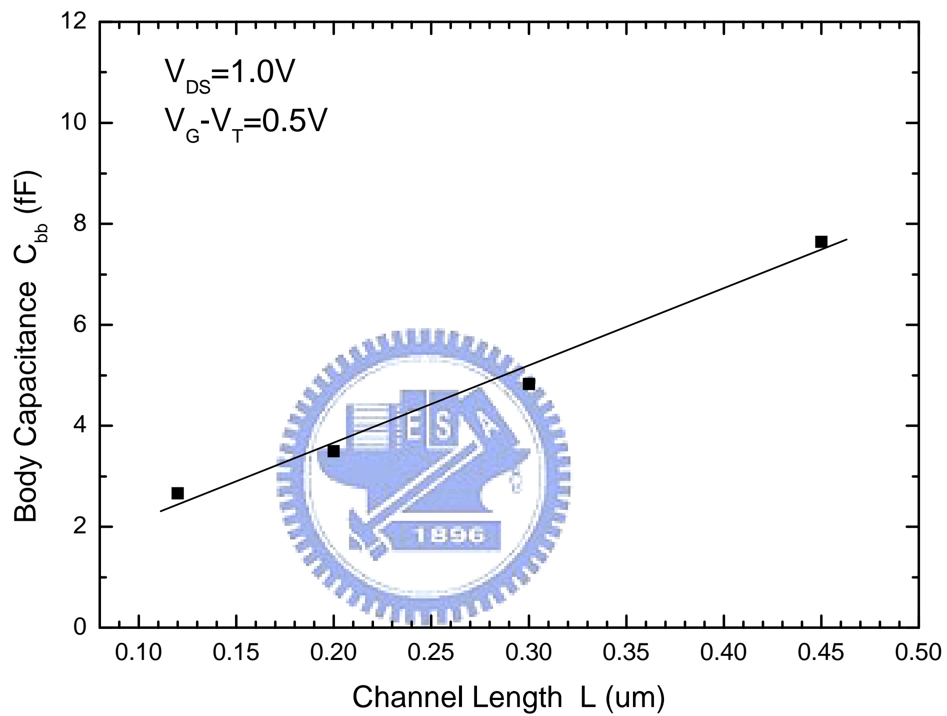


Fig. 3-5 Body capacitance as a function of channel length for a PD floating-body SOI MOSFET at V_G-V_T = 0.5 V and V_{DS} = 1.0V.

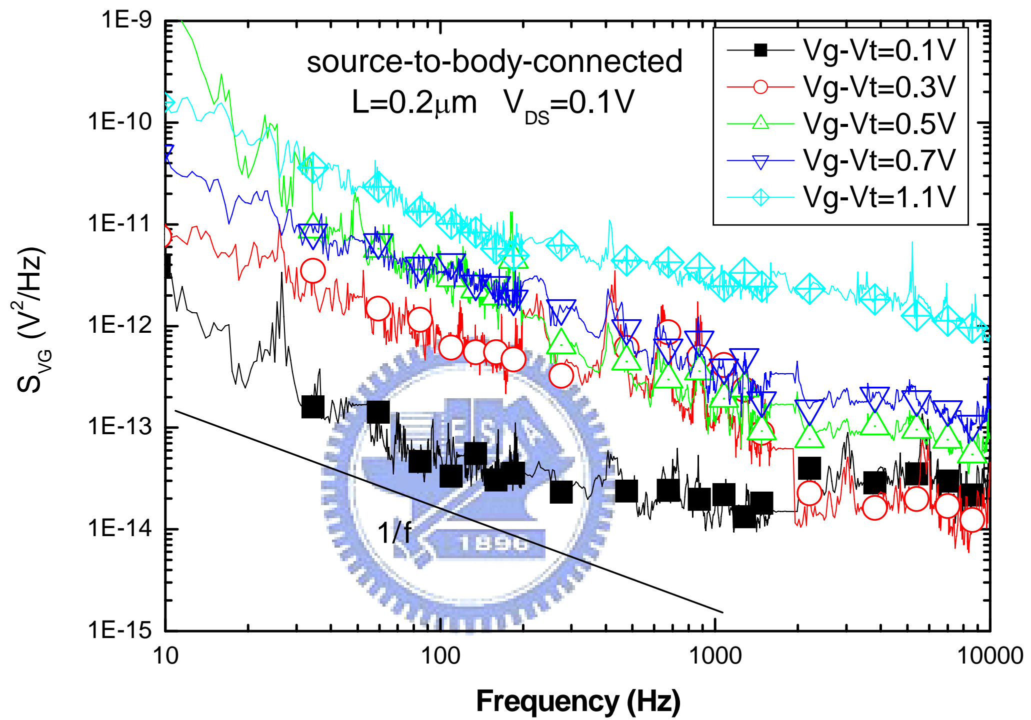


Fig. 3-6 Input-referred noise spectra of a PD source-to-body-connected SOI MOSFET at V_{DS} = 0.1V and L=0.2μm with different V_G-V_T.

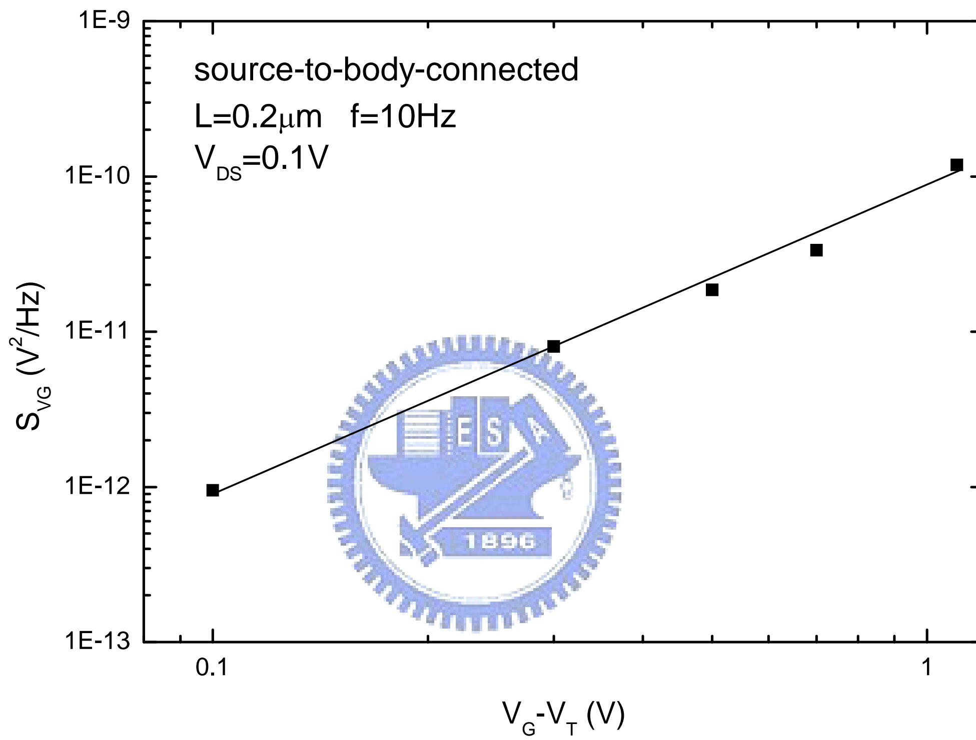


Fig. 3-7 The magnitude of input-referred noise as a function of gate voltage for a PD source-to-body-connected SOI MOSFET at V_{DS} = 0.1V, L=0.2μm and f=10Hz.

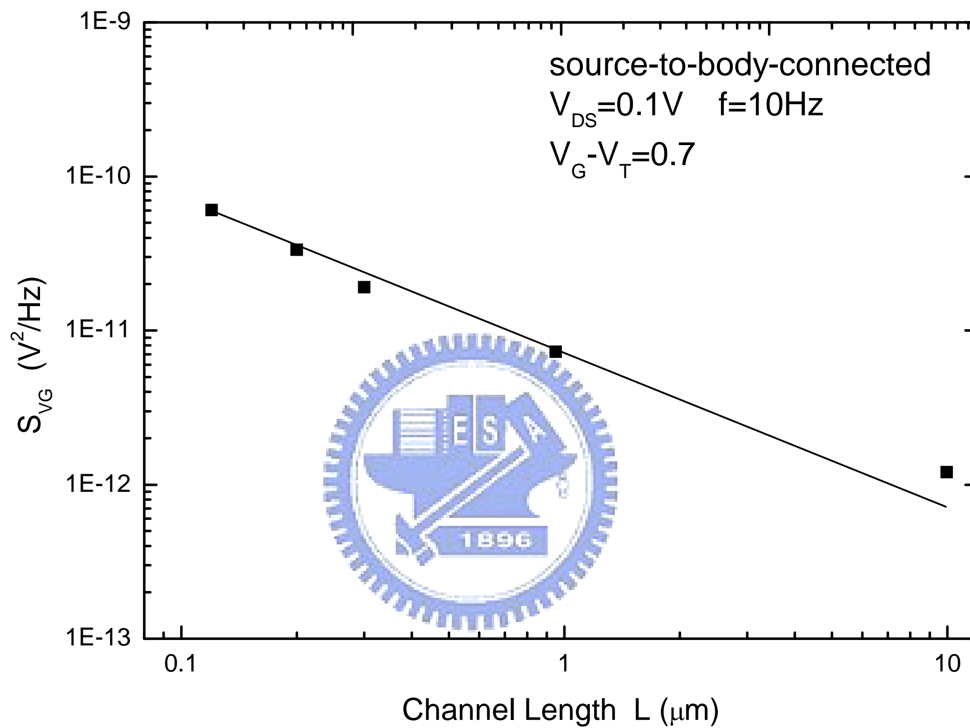


Fig. 3-8 The magnitude of input-referred noise as a function of channel length for a PD source-to-body-connected SOI MOSFET at V_{DS} = 0.1V and f=10Hz.

Chapter 4

Low-Frequency Noise in PD SOI MOSFETs at Various Temperatures

Because the SOI MOSFETs have higher thermal resistance, the channel temperature is higher than bulk devices with the same power dissipation. In addition, there is increasing demand for high-temperature electronics with CMOS technology. The temperature characteristics of SOI devices on analog applications should be studied [21], [22]. In this chapter, we use Temptronic TP03000 Thermal Controller to vary the temperature and investigate the influence on the low-frequency noise of PD SOI MOSFETs operating from linear region to saturation region. The noise characteristics of the devices with floating-body and source-to-body-connected structures have been discussed. The gate length and gate width of test devices are 0.2μm and 10μm, respectively.

The devices operate in linear operation are corresponding to a drain voltage V_{DS} = 0.1V. As the drain bias increases to about 0.4V, the devices enter the saturation region, both the data obtained before the kink occurring (V_{DS} = 0.8V) and after the kink occurring (V_{DS} = 1.2V) are shown.

4.1 Temperature Effect on Floating-Body PD Device

4.1.1 Operating in Linear Region

The low-frequency noise characteristics of a floating-body PD SOI MOSFET operating in the linear region (drain voltage V_{DS} = 0.1V) is given in Fig. 4-1. At T = 0°C, owing to such a low temperature and low drain bias, both the junction generation current and impact

ionization current have very low values, resulting in a higher plateau and lower f_0. Therefore, the noise overshoot only exists in low frequency range (f < 100Hz), and the $1/f$ noise dominates. As the temperature increases, the intrinsic carrier density ($n_i \propto T^{1.5} \cdot \exp(-1/T)$) significantly increases, resulting in a larger junction thermal generation current. This large junction generation current contributes to a lower plateau and higher f_0, thus the Lorentzian-like noise overshoot begins moving to higher frequency and exceeds the $1/f$ noise gradually, as shown in Fig. 4-1. With further increasing temperature to T = 150°C, the noise overshoot shifts to lower plateau and higher corner frequency due to the increase of junction generation current and a Lorentzian-like noise overshoot was observed explicitly.

4.1.2 Operating in Saturation Region and Pre-kink Region

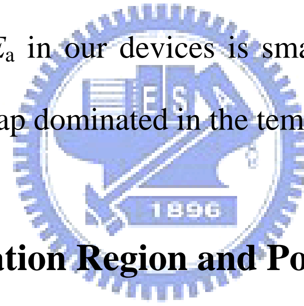
A similar phenomenon is observed in Fig. 4-2 for a floating-body device operating in saturation region before kink effect occurring (The kink voltage is about 0.9V), but an obvious noise overshoot has already appeared at T = 0°C due to the higher junction generation current than that in linear region. Since the junction leakage increases more rapidly at higher temperature, the magnitude of noise overshoot would be decreased drastically with the rise of temperature, as shown in Fig. 4-3.

To further see the effect of the I_L, α, and C_{bb} on the temperature behavior of the noise overshoot, we extract their values from the plateau and corner frequency of noise overshoot in Fig. 4-3 by using equation (3-1). We find that the body factor is nearly independent on temperature and drain bias, and its value is about 0.22. However, the I_L and C_{bb} are strong functions of temperature, as shown in Fig. 4-4. As the temperature increases, intrinsic carrier density increases, resulting in the decreasing of the depletion width, and therefore the C_{bb} increases monotonously. The exponential function of I_L with temperature indicates the thermal generation current dominates the junction current. From the plot of $\log(I_L)$ versus $1/T$

shown in Fig.4-5, the activation energy E_a for junction leakage can be extracted: E_a = 0.21eV at low temperature ($T \leq 75^0$C), and E_a = 0.42eV at high temperature. The equation of the junction leakage including ideal and nonideal cases can be expressed as:

$$J_R = q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \frac{qn_iW}{\tau_e} \tag{4-2}$$

The first term is the diffusion current, while the second term is the generation current due to the generation-recombination processes through the traps in the depletion region. If the junction leakage is dominated by the first term, owing to $J_{R1} \propto n_i^2 \propto \exp(-E_g/kT)$ (where bandgap energy E_g=1.1 eV), the value of E_a is approximately 1.1 eV. If the second term dominates, owing to the equation $J_{R2} \propto n_i \propto \exp(-E_g/2kT)$, the value of E_a is approximately 0.55 eV. Since the extracted E_a in our devices is smaller than 0.55 eV, it suggests that the thermal generation current is trap dominated in the temperature range of 0-150^{0}C [23].

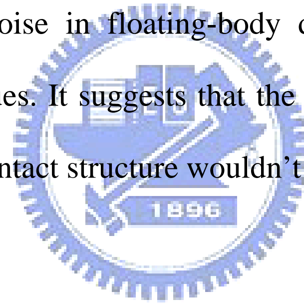


4.1.3 Operating in Saturation Region and Post-kink Region

As the device operates in the post-kink region (V_{DS}=1.2 V), the large junction leakage current makes the noise overshoot only exists in higher frequency (f > 1 kHz) and is approximately constant up to 75°C, as shown in Fig. 4-6. This is because the impact-ionization current generated near the drain overwhelms the thermal generation current and dominates the leakage current, and the impact-ionization current is less sensitive to temperature as compared to junction generation current [24]. Above 150°C, the drain to body junction generation current drastically increases and dominates leakage current, resulting in a lower plateau than the other temperature conditions. Except for the higher frequency, a pure 1/f noise has been observed over the range of measurement temperature. In addition, we find that the 1/f noise component is temperature-independent.

4.2 Temperature Effect on Body-to-Source-Connected PD Device

We may compare the noise measurements of floating-body SOI transistors with those of source-to-body-connected devices. As shown in Figs. 4-7 and 4-8, the input noise spectrum is dominated with $1/f$ noise component, and may contain small Lorentzian-like noise for some devices. This suggests that the noise overshoot can be suppressed by body contact. It is noted that the $1/f$ noise is independent of temperature as the case of floating-body device at high drain bias. From section 3.3 we know that the $1/f$ noise in SOI devices is dominated by induced mobility fluctuation, and the induced mobility fluctuation term $\mu_0 SN$ has a large effect on the variation of $1/f$ noise with temperature, yielding a relatively temperature-independent characteristic shown in Fig.4-7 and 4-8. We compare Figs. 4-6 and 4-8, the magnitudes of $1/f$ noise in floating-body devices and source-to-body-connected devices have approximate values. It suggests that the two types of devices have similar trap density. Therefore, the body contact structure wouldn't affect the gate oxide quality [25].



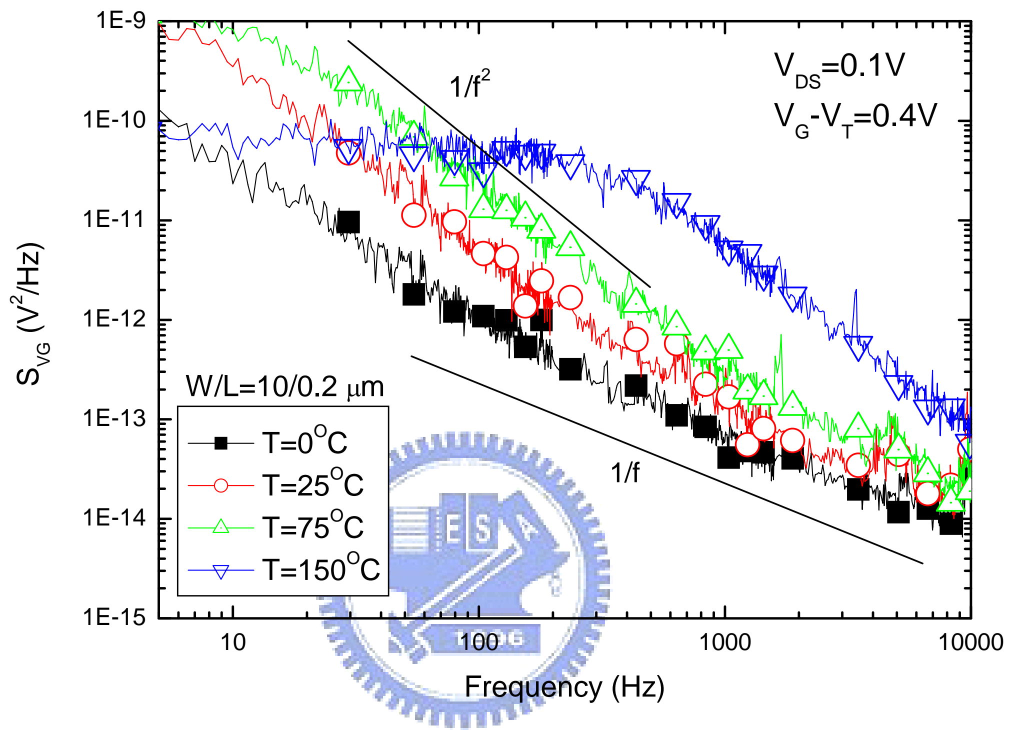


Fig. 4-1 Input-referred noise spectra of a PD floating-body SOI MOSFET at $V_{DS} = 0.1V$ with different temperatures.

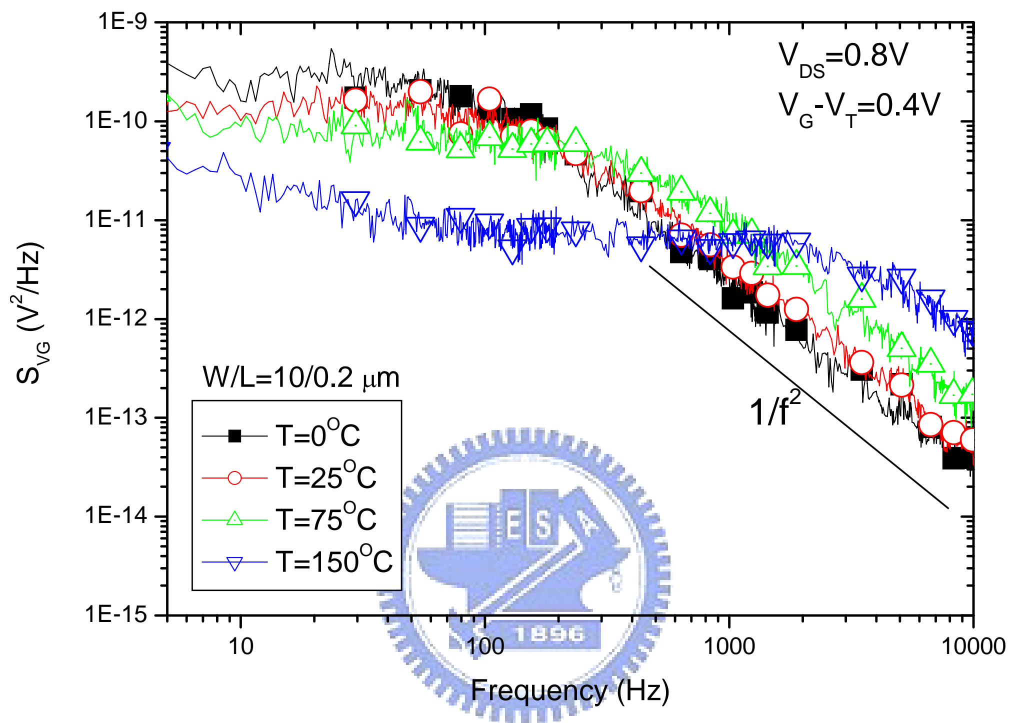


Fig. 4-2 Input-referred noise spectra of a PD floating-body SOI MOSFET at V_{DS} = 0.8V with different temperatures.

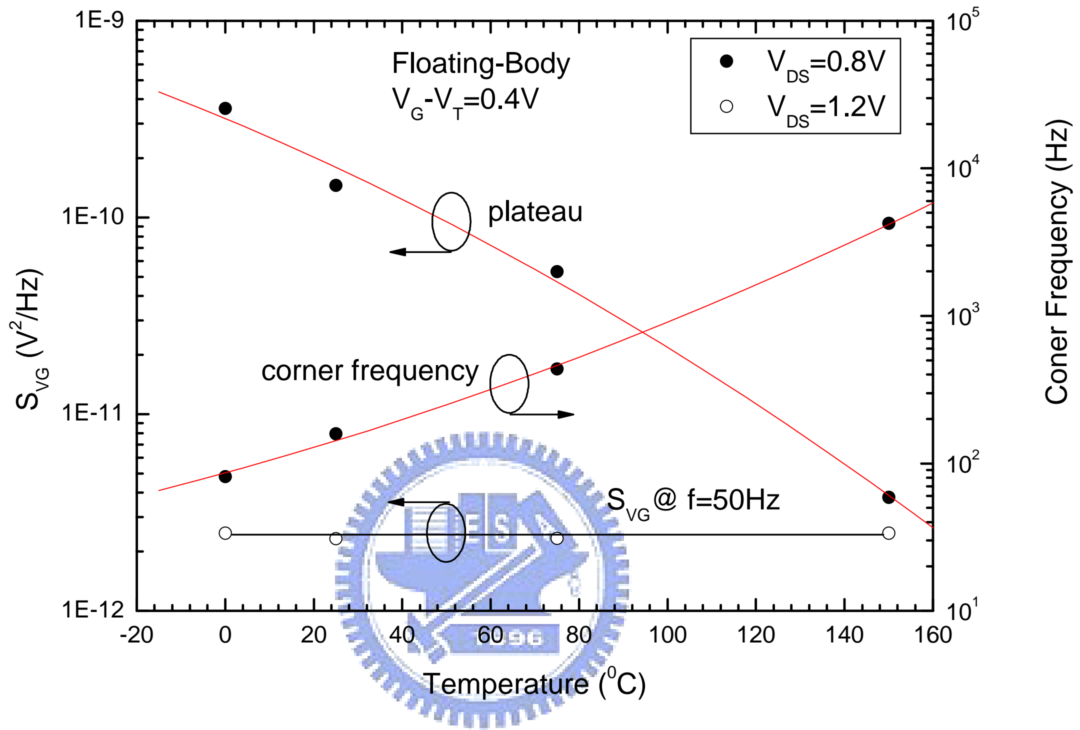


Fig. 4-3 Plateau and corner frequency of the input-referred noise for a PD floating-body SOI MOSFET at V_G-V_T = 0.4V and V_{DS} = 0.8V with different temperatures. Figure also shows the magnitude of the input-referred noise at f = 50Hz for a PD floating-body SOI MOSFET at V_G-V_T = 0.4V and V_{DS} = 1.2V.

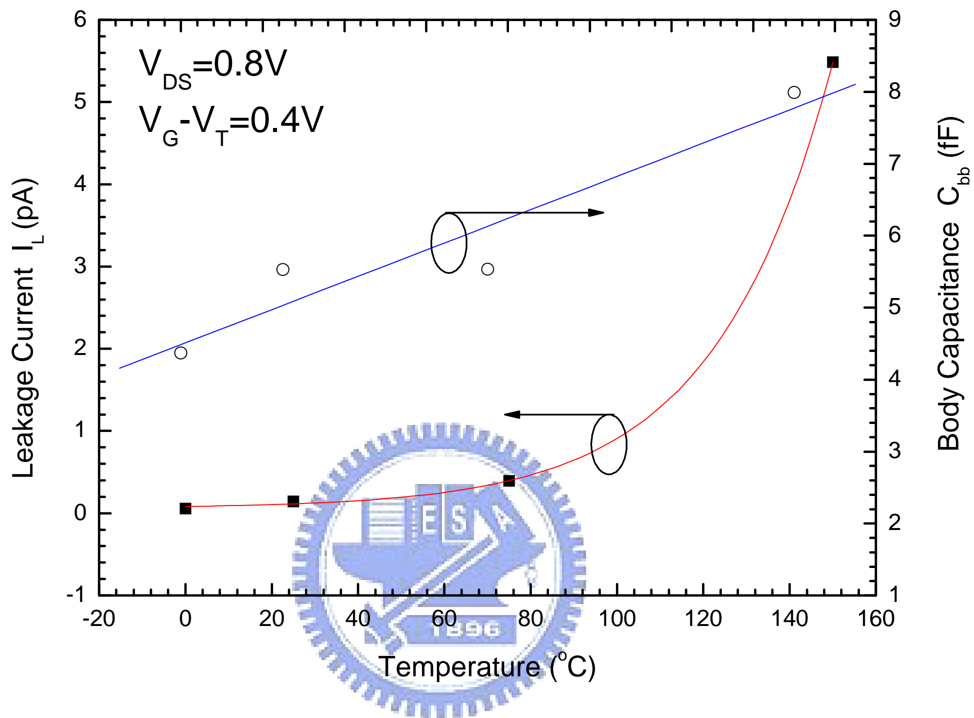


Fig. 4-4 Drain-body junction leakage and body capacitance as functions of temperature for a PD floating-body SOI MOSFET at V_G-V_T = 0.4V and V_{DS} = 0.8V.

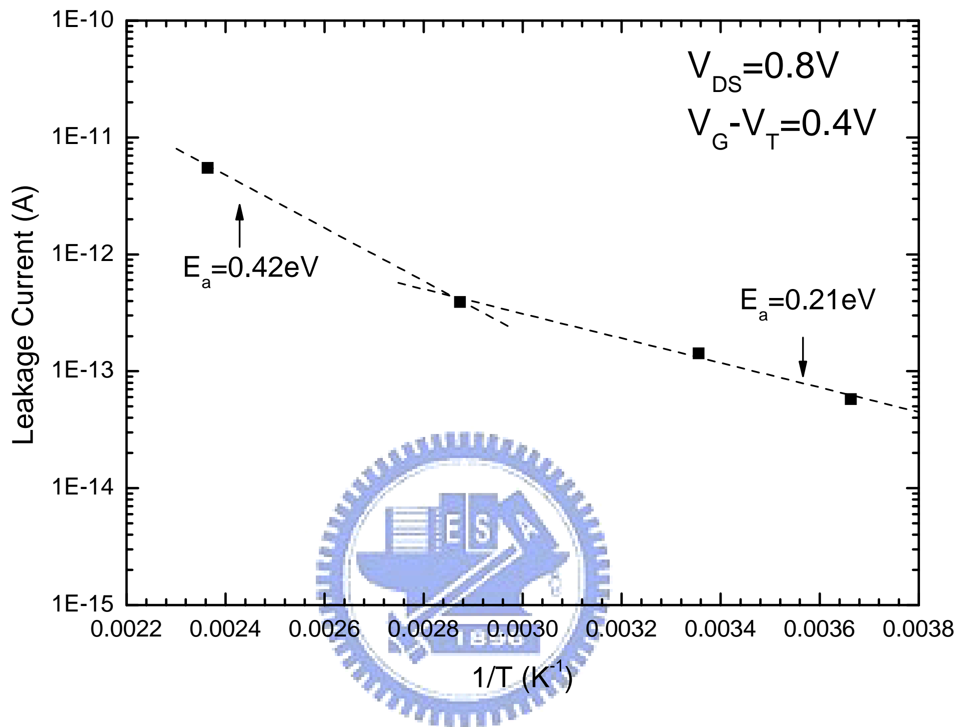


Fig. 4-5 Leakage current versus $1/T$ for a PD floating-body SOI MOSFET at V_G-V_T = 0.4V and V_{DS} = 0.8V.

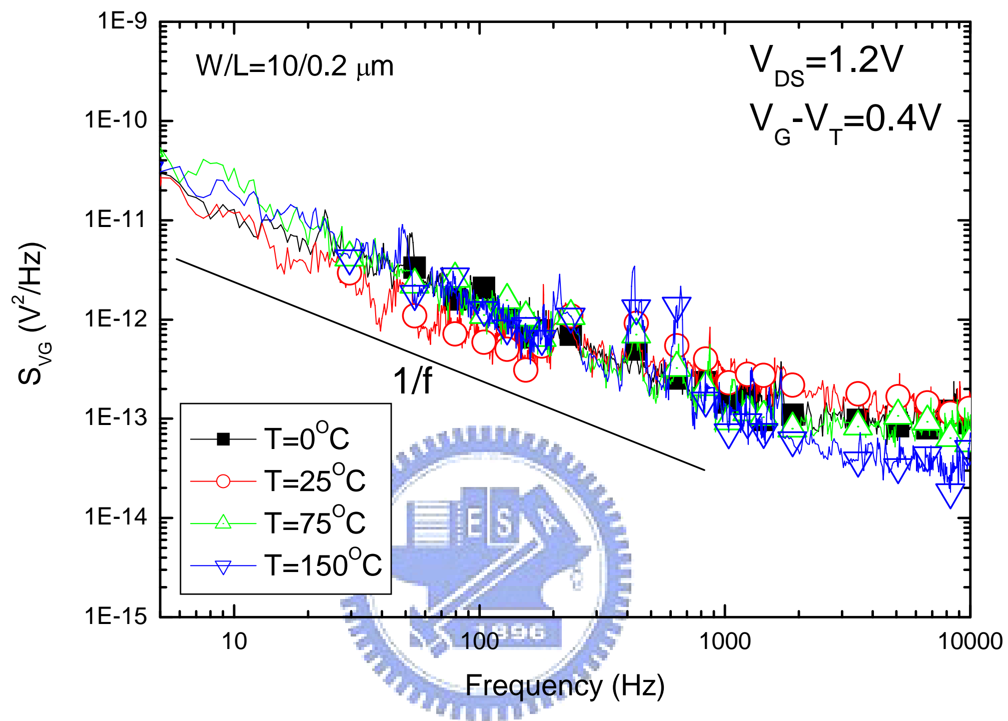


Fig. 4-6 Input-referred noise spectra of a PD floating-body SOI MOSFET at V_{DS} = 1.2V with different temperatures.

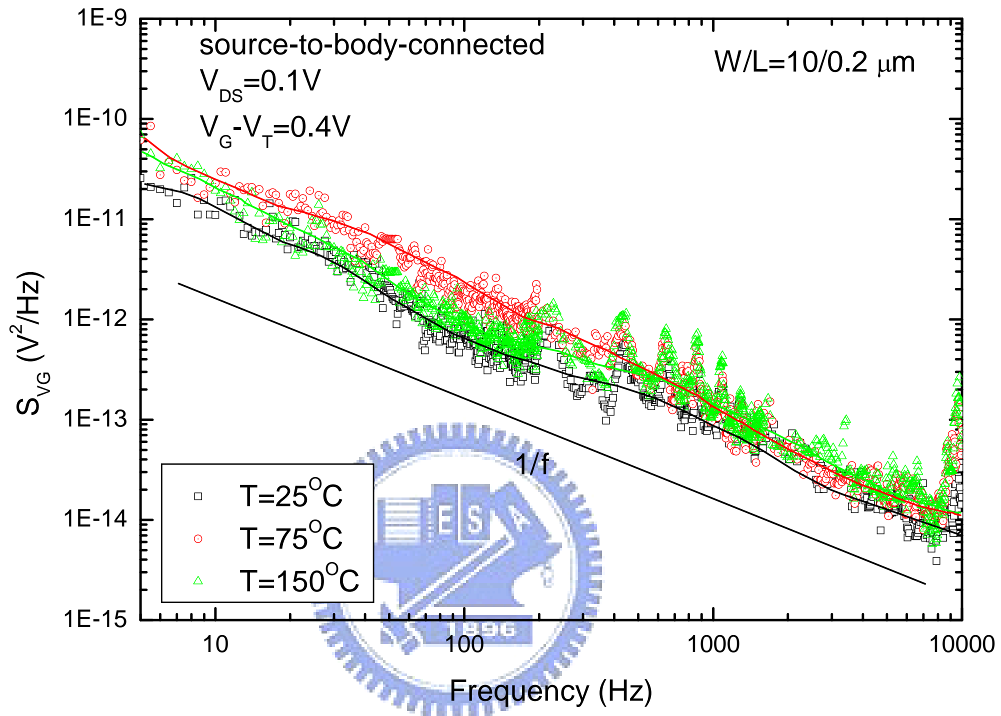


Fig. 4-7 Input-referred noise spectra of a PD source-to-body-connected SOI MOSFET at V_{DS} = 0.1V with different temperatures.

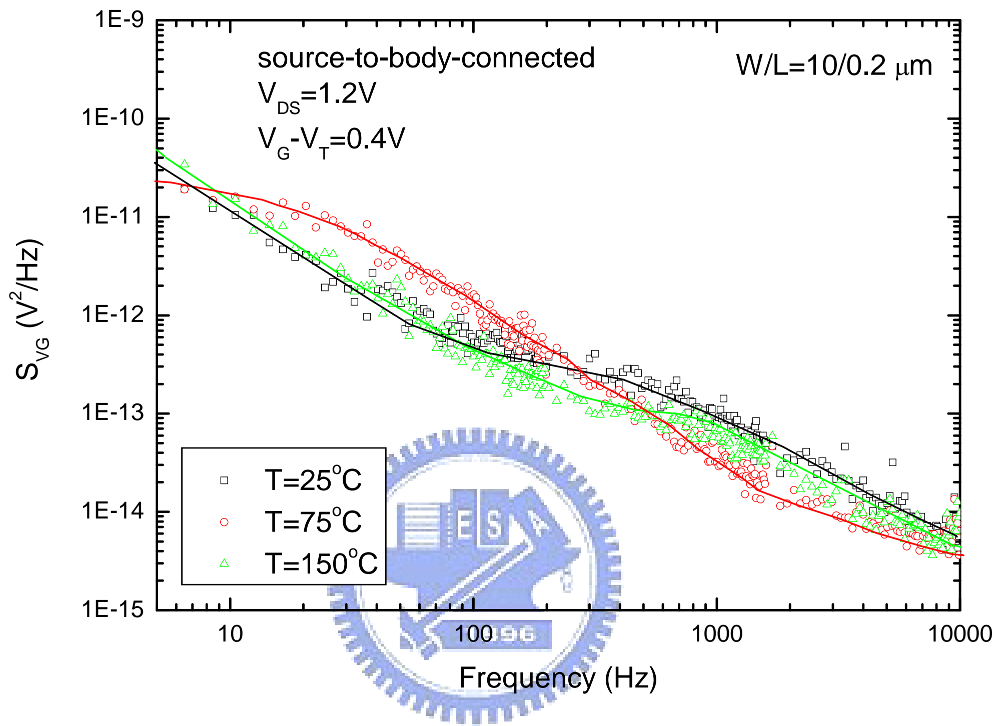


Fig. 4-8 Input-referred noise spectra of a PD source-to-body-connected SOI MOSFET at V_{DS} = 1.2V with different temperatures.

Chapter 5

Degradation of Low-Frequency Noise in PD SOI MOSFETs after Hot-Carrier Stress

With the reduction of device size to deep submicrometer dimensions, the problem of the quality of the gate oxide and its interface with the silicon substrate due to hot-carrier effect has been of increasing concern in the fabrication of SOI CMOS devices. Because the $1/f$ noise is sensitive to oxide charge and interface traps, it is good to monitor the device reliability by measuring the $1/f$ noise. In this chapter, we investigate the influence of hot-carrier stress on the low-frequency noise of PD SOI MOSFETs including $1/f$ noise and shot noise induced kink-related excess noise. The noise characteristics of the devices with floating-body and body-contact structures have been discussed.

5.1 Experiments

The n-channel MOSFETs were fabricated on SIMOX substrates with 205nm thick Si active layers, and 400nm thick buried oxides. Briefly, 450nm LOCOS field oxide was used for device isolation. After V_T-adjust implant and anti-punch through implant, a 4nm gate oxide and in-situ n^+-doped polysilicon gate were formed. The floating-body and body-contact devices with nitride spacer and As^+-implanted source/drain junctions are partially depleted. After NiSi salicidation, the devices were metalized using a typical backend flow.

The current-voltage characteristics of devices were measured using HP4156A semiconductor parameter analyzer. The low-frequency noise measurements in normal and

reverse (i.e., source and drain interchanged) modes were performed using a BTA9812B noise analyzer in conjunction with an HP35670A dynamic signal analyzer. The hot-carrier stress was applied at a drain voltage of V_{DS} = 4V and a gate voltage of V_G = 2V with a stressing time ranging from 0 to 1000 sec.

5.2 Hot-Carrier Effect on Floating-Body PD Device

Fig. 5-1 shows the low-frequency noise characteristics of a floating-body PD SOI MOSFET operating in the linear region (V_{DS} = 0.1V) before and after hot-carrier stress for 1000 seconds. The gate length and gate width of test devices are 0.4μm and 20μm, respectively. Owing to the low drain bias, the drain-body junction leakage is low, and the kink related excess noise was overwhelmed by the 1/*f* noise. After stress, there are two types of damages would affect the 1/*f* noise: interface states and oxide-trapped charge. In a stressed device, the energy transferred from the hot carriers to the Si/SiO_2 interface would break the bond at the interface and thus leads to the creation of the interface state. In n-MOS devices, only acceptor states which become negatively charged would cause an influence on it. When a charge is injected into the oxide after hot carrier stress, it can create a trap; and they are charged positively or negatively depending on this trap [26]. After stressing the device with 1000 seconds, the interface trap and oxide charge stem from hot carrier effect would be increased. From the model in chapter 2, the 1/*f* noise is proportional to the trap density N_t near the Fermi-level.

$$S_{VG} \propto N_t \qquad (5\text{-}1)$$

Therefore, the 1/*f* noise would be increased after hot-carrier stress, and the similar phenomenon can also be observed in reverse mode. It is noted that, the magnitude of 1/*f* noise in the normal mode and the reverse mode have approximate values. However, in saturation condition (V_{DS} = 2V), the magnitude of 1/*f* noise in the reverse mode is higher than that in the

normal mode, as shown in Fig. 5-2. Fig. 5-3 shows the hot-carrier degradation modes of a MOSFET operated in the linear and saturation regimes. In linear region, the effects of the trap are the same in both modes, nevertheless, in saturation region, the effect of the trap decreases in normal mode as the pinch-off region increases. For reverse mode operation, hot-carrier-induced interface traps are located on the source side, so the effect of the trap remains unchanged in saturation region [27], [28]. Therefore, the magnitude of the $1/f$ noise increased by hot-carrier stress in reverse mode is higher than that in normal mode.

Fig. 5-4 shows the low-frequency noise characteristics of a device operating in the saturation region and before kink effect occurring (V_{DS} =1.2V). A Lorentzian-like noise overshoot was observed explicitly before and after stress in normal mode. The noise overshoot comes from the interaction between the shot noise of the junction leakage and the source-body impedance, as illustrated in chapter 3. After stressing the device, the increased interface-trap density near the drain junction causes the increase of gate-induced-drain-leakage (GIDL) current in the low field region as shown in Fig. 5-5, and provides an additional current path due to the interface-trap assisted band-to-band tunneling mechanism; therefore, the trap-assisted drain-to-substrate leakage increases [29]. As discussed in chapter 3, when the drain-to-substrate leakage increases, the plateau of the kink-related excess noise will decrease, and the corner frequency will increase as shown in Fig. 5-4. In reverse mode, because the interface traps are located on the source side, the GIDL current would not be changed as shown in Fig. 5-6. Hence, the drain-to-substrate leakage would not be affected by stress and remain constant. However, the excess holes in body region due to the floating-body effect can effectively recombine through the interface traps near source with excess electrons due to the parasitic bipolar action. As a result, the floating-body effect is suppressed, thus the kink-related excess noise is suppressed. From Fig. 5-4, we only observe the $1/f$ noise after stress with reverse mode.

5.3 Hot-Carrier Effect on Body-Contact PD Device

To reduce floating body effect, the body contact structure is widely used in SOI CMOS technology. Hence we are also interested to know the hot-carrier effect on the performance of body-contact devices. Figs. 5-7 and 5-8 show the threshold voltage and drain current degradation respectively as a function of stress time in floating-body and body-contact devices. The gate length and gate width of test devices are 0.4μm and 20μm, respectively. It is noted that the degradation in body-contact device was larger than that in floating-body device. As the body voltage changes from high (floating-body device) to low (body-contact device), the vertical channel field increases, which means the channel electrons are pushed further toward the Si surface [30]. These hot channel electrons which closer to the Si surface would lead to greater Si surface damage. Therefore, the degradation which stems from hot-carrier stress was more serious in body-contact device. Figs. 5-9 and 5-10 show the low-frequency noise characteristics of a body-contact PD device operating in the linear and saturation region respectively. Because the body contact provides a low resistance leakage path, the shot noise amplified gain decreases, and the input noise spectrum is dominated with $1/f$ noise component. As the same with the floating–body devices, the $1/f$ noise would increase after hot-carrier stress due to the generation of the interface states and oxide charge.

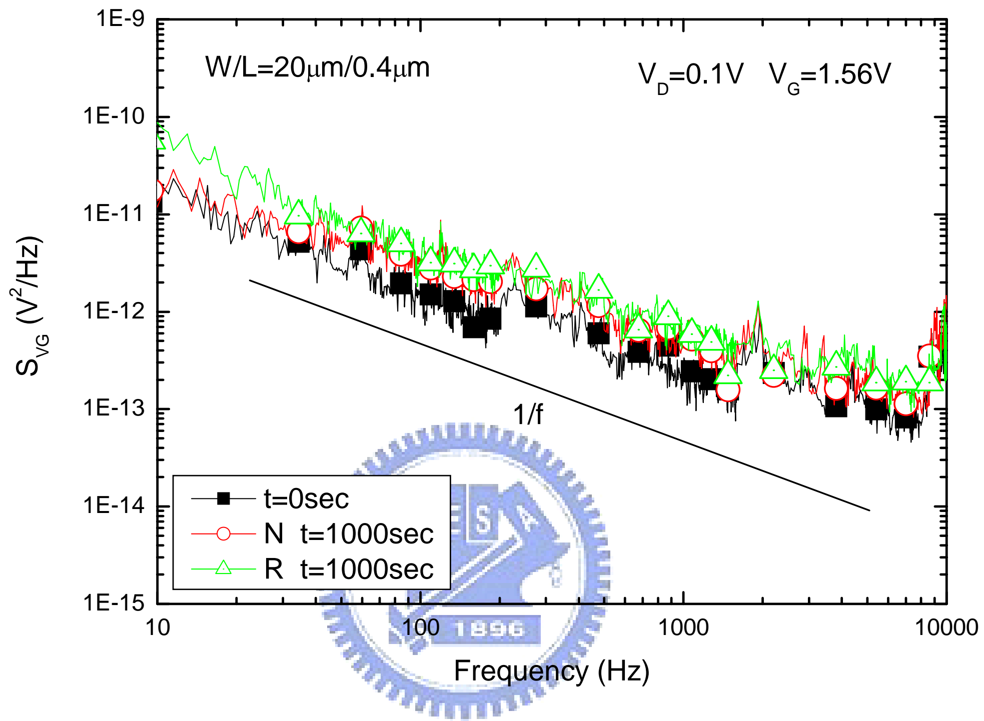


Fig. 5-1 Input-referred noise spectra of a PD floating-body SOI MOSFET at V_{DS} = 0.1V in normal and reverse modes before and after stress.

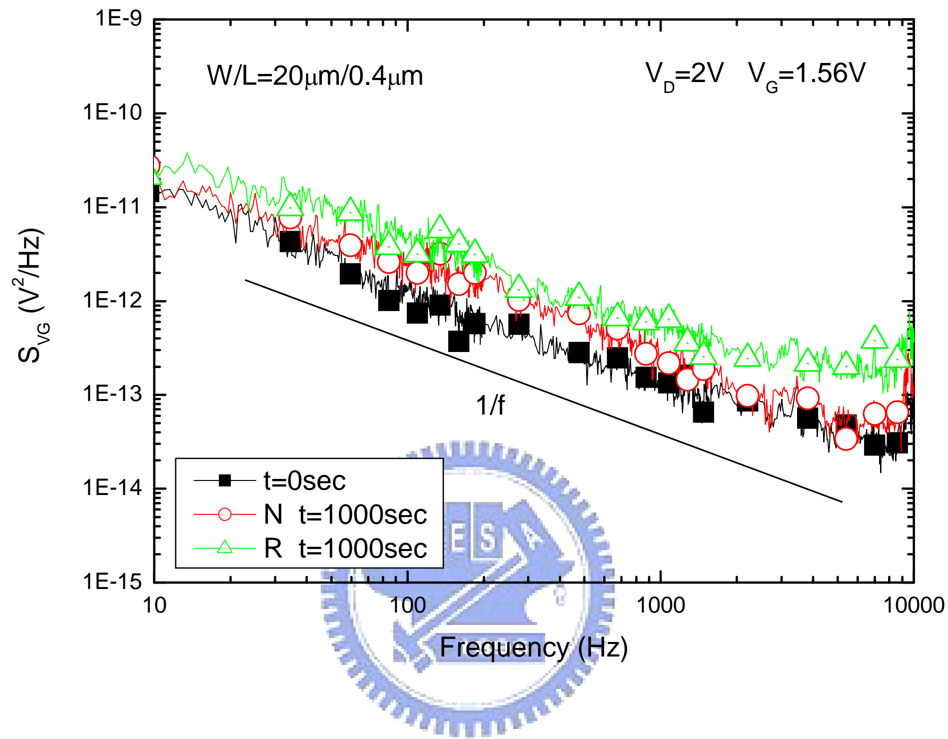


Fig. 5-2 Input-referred noise spectra of a PD floating-body SOI MOSFET at V_{DS} = 2V in normal and reverse modes before and after stress.

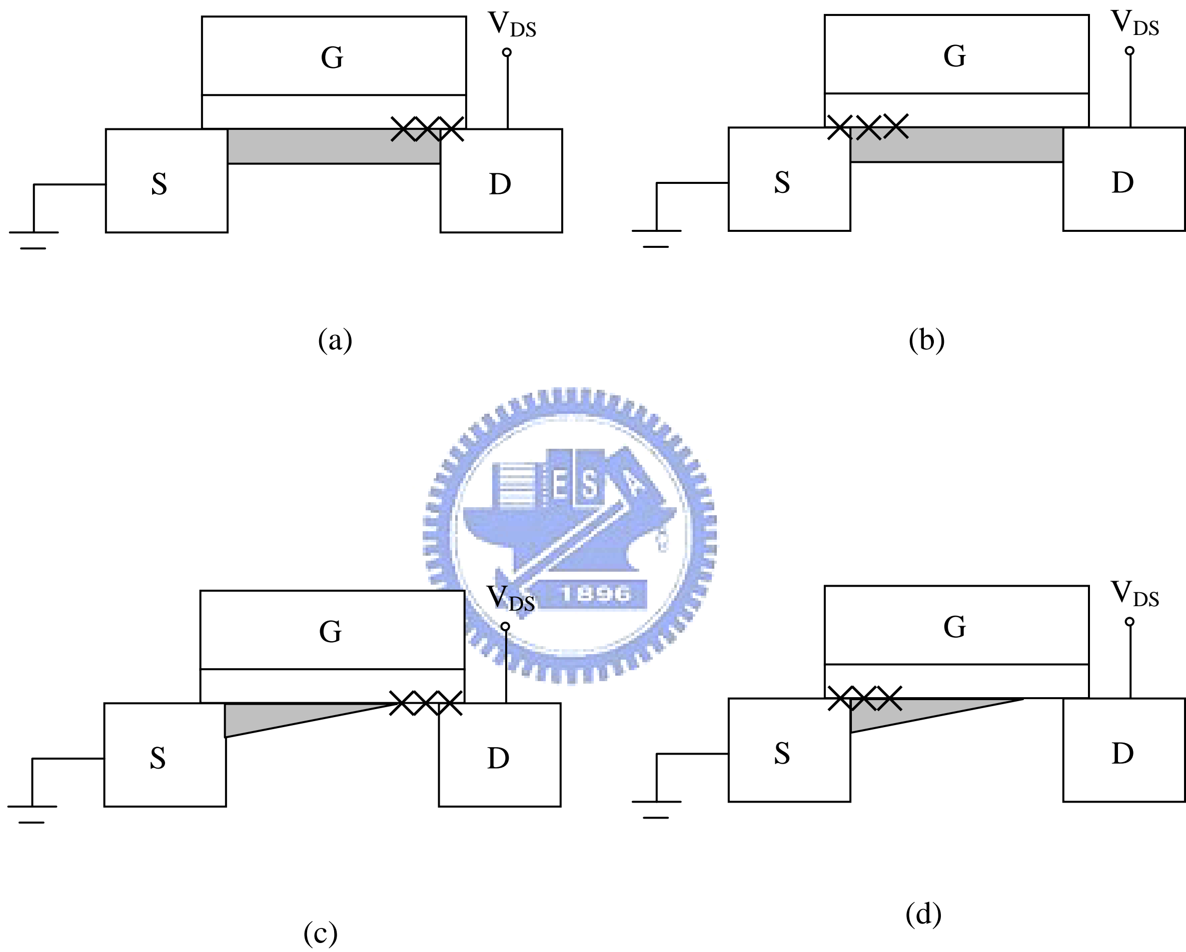


Fig. 5-3 Schematic diagrams of a MOSFET operated in (a) the normal mode and linear region; (b) the reverse mode and linear region; (c) the normal mode and saturation region; and (d) reverse mode and saturation region. The position of the interface trap is indicated symbolically by the cross (×)

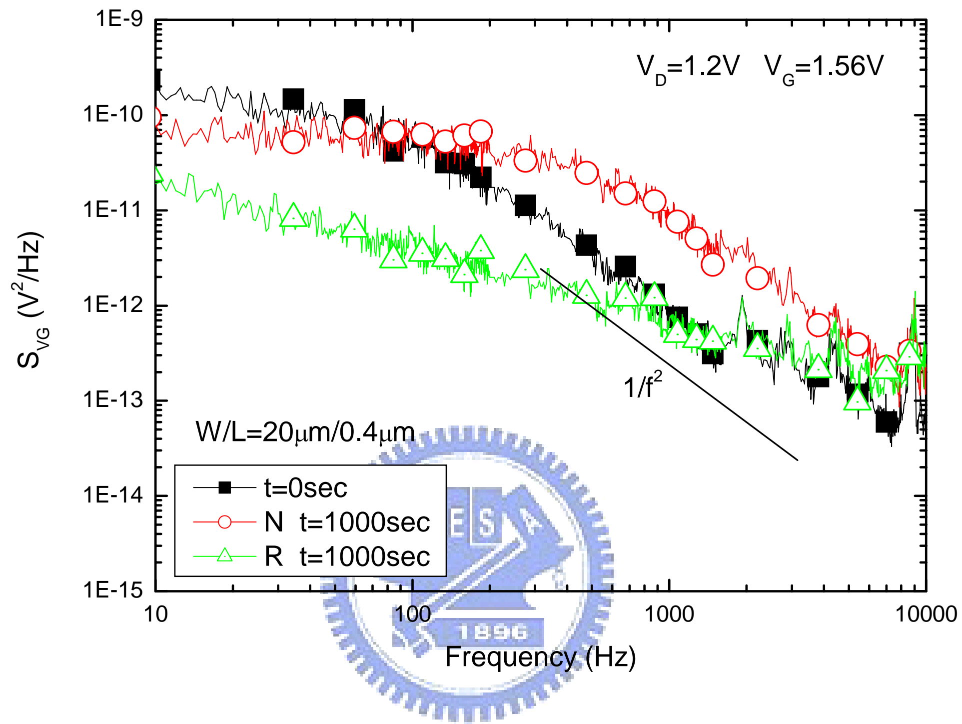


Fig. 5-4 Input-referred noise spectra of a PD floating-body SOI MOSFET at V_{DS} = 1.2V in normal and reverse mode before and after stress.

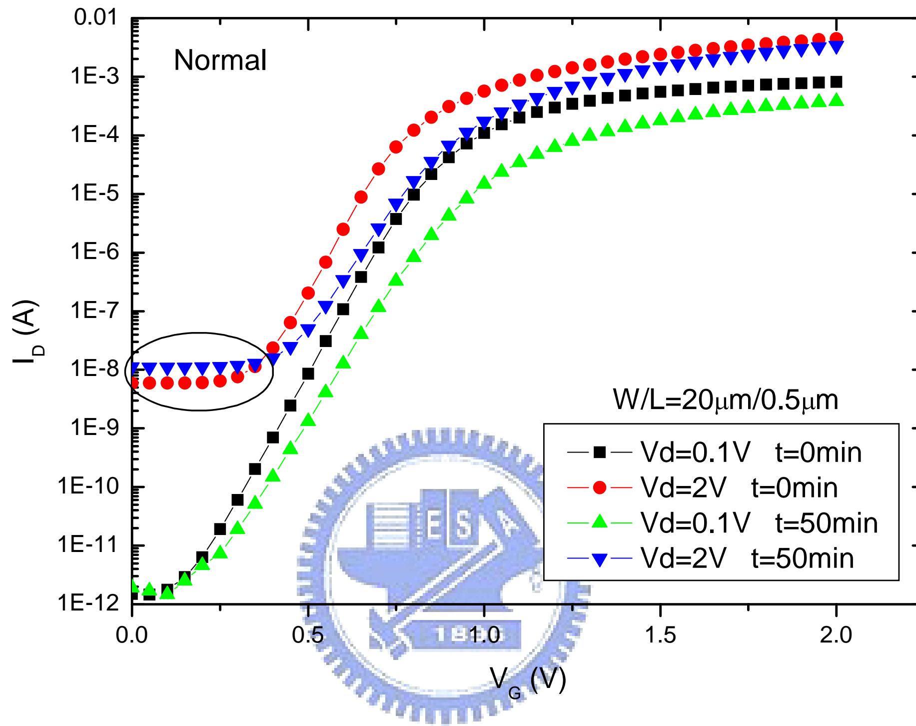


Fig. 5-5 I_D-V_G characteristic of a PD floating-body SOI MOSFET in normal mode before and after stress with W=20μm and L=0.5μm.

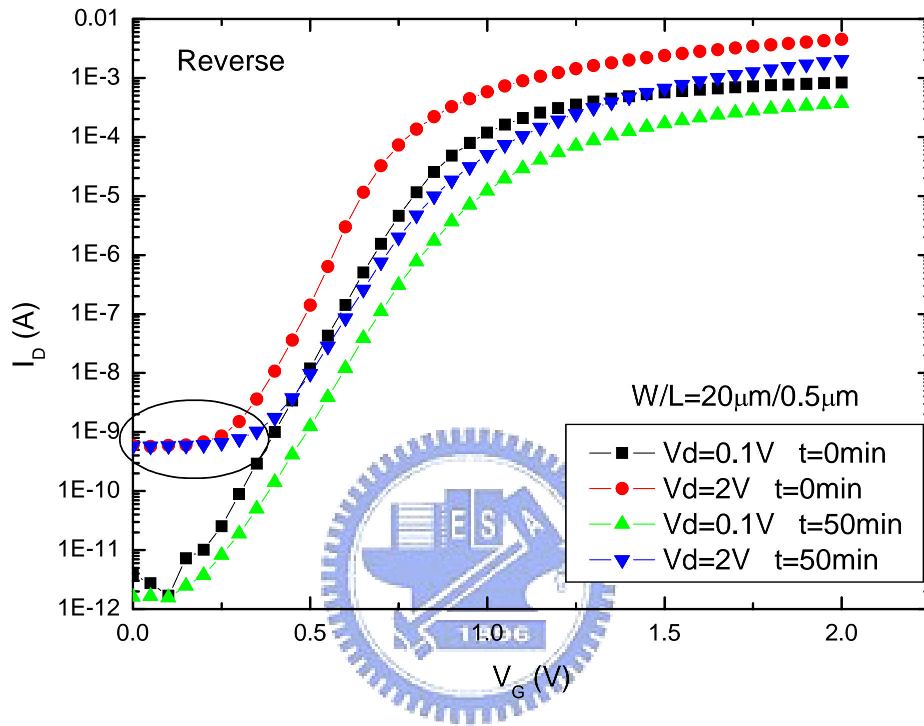


Fig. 5-6 I_D-V_G characteristic of a PD floating-body SOI MOSFET in reverse mode before and after stress with W=20μm and L=0.5μm.

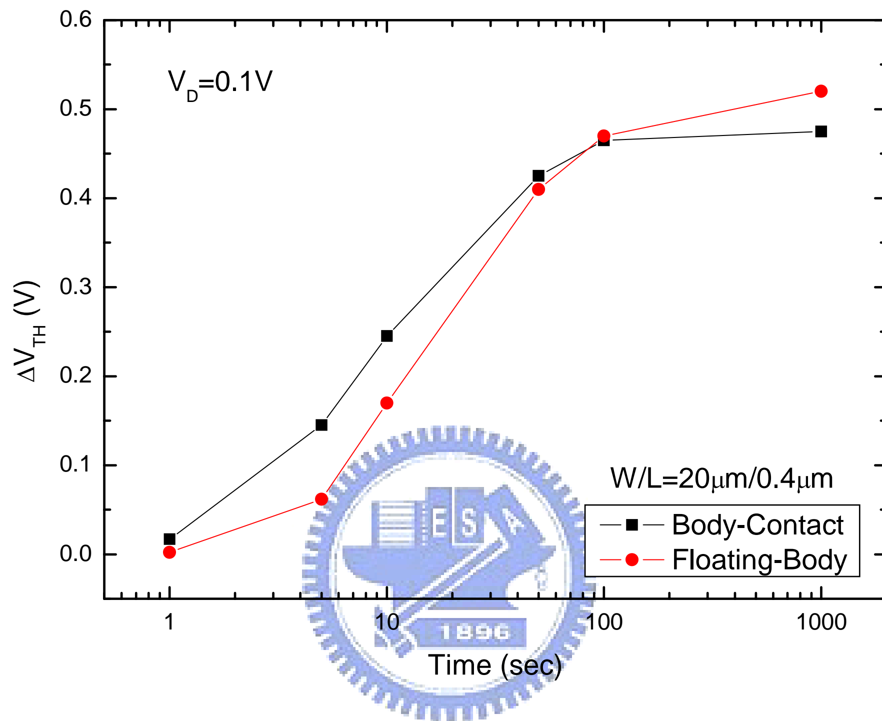


Fig. 5-7 Threshold voltage degradations as a function of stress time in floating-body and body-contact devices.

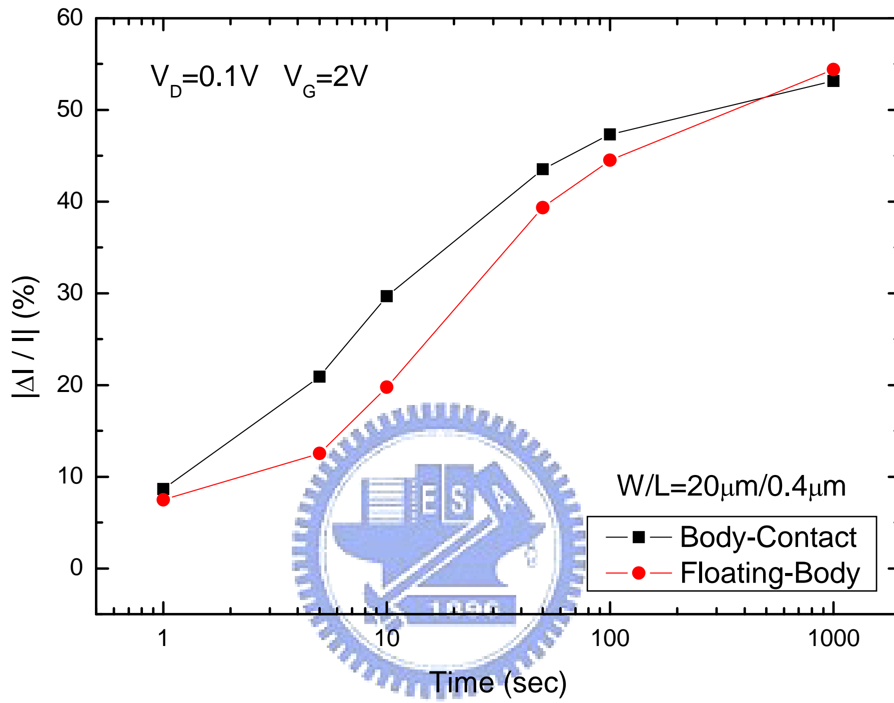


Fig. 5-8 Drain current degradations as a function of stress time in floating-body and body-contact devices.

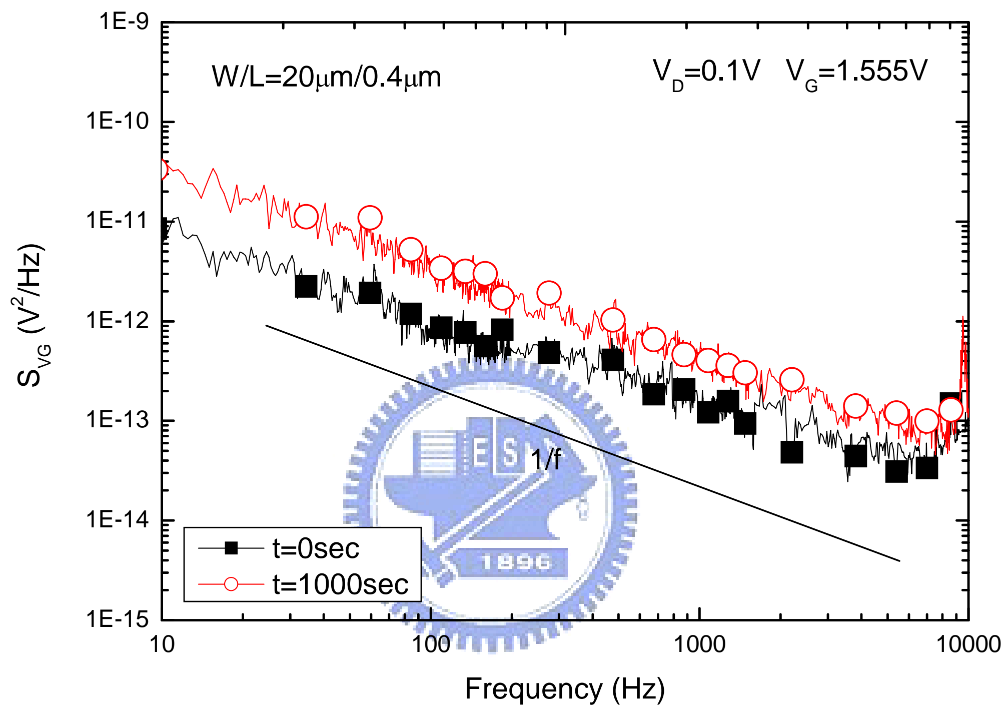


Fig. 5-9 Input-referred noise spectra of a PD body-contact SOI MOSFET at V_{DS} = 0.1V before and after stress.

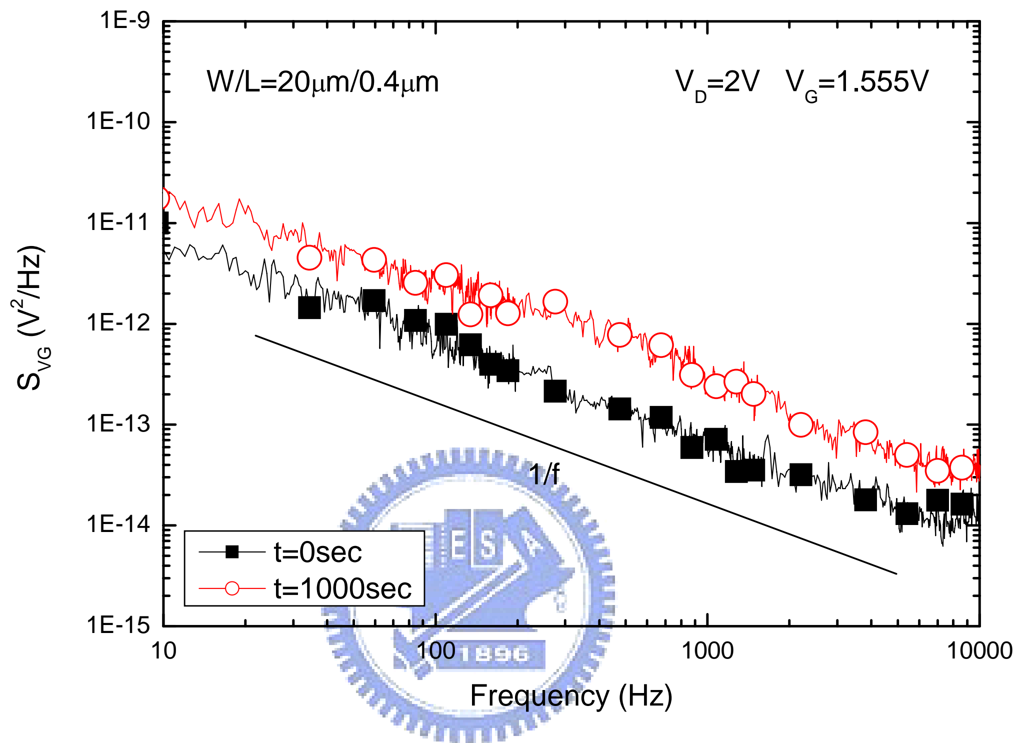


Fig. 5-10 Input-referred noise spectra of a PD body-contact SOI MOSFET at V_{DS} = 2V before and after stress.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The development trends of MOS devices are scaling down the device size and enhance the speed of operation. However, it results in many obstacles for bulk MOSFETs and is difficult to overcome. Therefore, the characteristics of high speed, low power consumption, higher device density possessed by SOI devices make it become the promising candidate for integrated digital and RF applications. In this thesis, the low-frequency noise characteristics of PD MOSFETs in SOI technology at various temperatures and channel lengths have been presented. For floating-body devices, the Lorentzian-like noise overshoot is observed due to the floating-body effect. The present of this additional component increases the noise of the transistors over a wide bandwidth, and might be a limitation in the noise performance of analog circuits in PD SOI technology. However, the noise overshoot can be reduced using a source-to-body-connected structure.

In our experiment, we observe that the plateau and corner frequency of the noise overshoot in floating-body devices will be affected by drain bias, temperature, and channel length. A model based on the interaction between the shot noise of the drain-body junction leakage and the source-body impedance has been adopted to explain the noise behavior. As the drain bias or temperature increases, junction leakage current increases, resulting in a lower plateau and higher corner frequency. On the contrary, as the channel length increases, junction leakage current decreases, resulting in a higher plateau and lower corner frequency. Therefore, the noise overshoot can be suppressed at high drain bias, high temperature, and short channel

length.

For floating-body devices, the Lorentzian-like noise overshoot has the highest magnitude in the saturation region before the kink occurs compared with those under other operation conditions. By extracting the temperature dependence of the junction leakage current from the noise overshoot, we know the leakage in pre-kink region is dominated with the trap-assisted generation current. Hence it is important to reduce the trap numbers near drain-body junction for lowering the noise overshoot. For source-to-body-connected structure, the input-referred $1/f$ noise is proportional to the square of gate drive voltage and $1/L$ in linear operation. And the $1/f$ noise is independent of temperature. It suggests that the $1/f$ noise in PD devices is dominated by the trap-induced mobility fluctuation in the channel.

The effect of hot-carrier stress on the low-frequency noise of SOI devices has also been studies in this thesis. After hot-carrier stress, the increase of GIDL current in floating-body device would result in a lower plateau and higher corner frequency for kink-related excess noise measured in normal mode. However, in reverse mode, the GIDL current remains unchanged, but the floating-body effect is suppressed after stress and thus the kink-related excess noise is suppressed. In addition, the $1/f$ noise would be increased after stress for both floating-body and source-to-body-connected devices.

6.2 Future Work

As the SOI device is popular in recent years, more and more researches are made for improving the device performance and getting more widely application. Hence, a more accurate low-frequency noise model of SOI MOSFETs is desired for the design of analog circuits such as mixer and VCO, which the phase noise is an important parameter. In the future, a complete large-signal model of SOI MOSFETs including $1/f$ noise and Lorentzian-like noise components will be established.

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簡　歷

姓　　名：胡 心 卉

性　　別：女

出 生 日 期：中華民國六十九年三月一日

籍　貫：台 北 市

地　址：台北市中山北路二段59巷45號16樓之6

學　歷：私立逢甲大學 電機系

87年 9~ 91年6月

國立交通大學 電子工程研究所碩士班

91年 9~ 93年6月

碩士論文題目：深次微米部分空乏型矽在絕緣層上金氧半場效電晶體之低頻雜訊特性研究

Low-Frequency Noise Characterization of Deep Submicron Partially-Depleted SOI MOSFETs