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A NEW GENERAL METHOD TO MODEL SIGNAL TIMING OF E/D NMOS LOGIC

CHUNG-YU WU AND YEN-TAI LIN

Department of Electronic Engineering and Institute of Electronics, National Chiao Tung University, 75 Po-Ai Street, Hsin-Chu 30039 Taiwan, Republic of China

SUMMARY

A new general modelling method for E/D NMOS logic is proposed and applied to the case of inverters. In this model, non-linear device currents in the large-signal equivalent circuit are reformulated by the curve-fitting technique. Then output voltage wave-forms are analytically solved region by region from the equivalent circuit. From the derived formulae, the rise/fall time and delay time can be calculated. Wide-range comparisons with SPICE simulation results were performed to verify the accuracy and the general applicability of the developed model. Two examples are given to demonstrate the applications of the developed timing model to timing analysis. It is shown that the model has a good accuracy for E/D inverters with a wide range of beta ratios, gate sizes, capacitive loads, input voltage wave-forms and device parameters. Moreover, the required CPU time and memory are small. These make the proposed modelling method an interesting approach to model E/D NMOS gates for CAD applications.

1. INTRODUCTION

As VLSI/ULSI MOS devices are scaled down to increase chip density, circuit complexity and operation speed, circuit design becomes a challenging task to retain the full benefit of scaling down while optimizing performance for a highly complicated circuit. Since signal delay is one of the fundamental characteristics of a digital MOS IC, many valuable approaches[1-20] have so far been taken to develop sophisticated timing models or macromodels which can aid the circuit design in many ways. They are:

(1) to provide a solid base for circuit optimization and automatic sizing[2,8,12,13]
(2) to provide CAD models for efficient timing analysis or verification on complicated VLSI/ULSI circuits with reasonable speed, computer memory and accuracy[5,9,12,15,16,21]
(3) to improve the accuracy of delay calculations in logic simulations[4,11]
(4) to provide a deep insight into the speed nature of digital MOS ICs.[7,14]

One interesting approach recently developed[1-14] is to derive delicate analytical timing models or macromodels for MOS digital gates using suitable device equations and equivalent circuits. In this approach, some models were specially developed for static CMOS gates[2,6,9,13,14] or domino CMOS,[8] while others[1,3-5,7,10-12] were developed for E/D NMOS logic gates. Unlike the conventional analytic models in textbooks, they all characterize output responses under non-step input excitations, rather than ideal step input, using different modelling methods.

For E/D NMOS gates, the delay was modelled by considering charging and discharging of capacitive loads[1,4,11] with averaged currents[11] or fixed currents,[1,4] by deriving accurate formulae from SPICE simulation results[12] or the gate transfer curve,[3] or by piecewise linearized circuits.[7] Specifically, the two modelling methods proposed by Simmons and Taylor[10] and Etiemble *et al.*[5] are based on the large-signal model with determined device resistances for the characterization of submicrometre oscillators and with simple device equations and linearized device parameters and wave-forms[5] respectively.

Other approaches for gate delay modelling are *RC* models which treat transistors as effective resistors[15,16] and bounding algorithms which seek upper and lower bounds for output responses of gates

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or interconnects.[17-20] Generally, these approaches make a trade-off between speed and accuracy of timing analysis.

All these works are important stages in timing model development. However, it is found that some key problems still have to be solved to achieve the four goals mentioned above. First, accurate device equations are required in a timing model to improve its accuracy. Secondly, the accuracy has to be definitely verified for a wide range of NMOS device dimensions and parameters. Thirdly, the modelling method has to be applicable to complex NMOS gates. Finally, the predetermined model parameters from either experimental measurements or fully transient circuit simulations have to be eliminated so that the model can be applied to optimization or autosizing. It is the purpose of this study to develop a new modelling approach for the E/D NMOS logic, which provides a direction to solve the above problem. Before introducing the new models, the inherent difficulty in modelling the E/D NMOS logic will be described.

According to our observations, the modelling work for E/D NMOS logic is far more difficult than that for CMOS, even in the case of a simple inverter. The difficulties originate from:

(1) wide ranges of device beta ratios and sizes which require a high model generality
(2) slower rising wave-forms which increase the latency and the initial delay[9,10] of the output falling wave-forms and complicate the timing behaviour
(3) faster falling wave-forms which enhance their sensitivities to input rising wave-forms.

We have tried to develop models of E/D NMOS inverters using the same method as in CMOS[6,9] and failed to obtain satisfactory accuracy for inverters with wide ranges of device dimensions and excitation inputs.

The new modelling method to be presented here overcomes the above difficulties partly by using the curve-fitting technique to accurately calculate the drain currents in transient operations and partly by modelling the initial delay which is related to the device subthreshold characteristics. In the characteristic wave-form case, the developed models have shown an error of less than 21% for the rise/fall time and a maximum error of 12% for pair delay times larger than 2 ns and 20% for pair delay times smaller than 2 ns. They have also shown an error as small as 4% for the total delay of a string of 12 inverters with arbitrary input excitation. Moreover, the models can be applied to E/D NMOS inverters with different beta ratios, device sizes, capacitive loads, device parameters, channel lengths (1·0 and 3·5 μm) and input excitations.

In the following sections, the new models are described. In deriving the models, characteristic wave-forms[7,9,10] which are close to the actual internal chip wave-forms are considered, but the models are shown to be applicable to arbitrary input cases. To check the model accuracy, extensive comparisons with SPICE simulations and error analysis were performed. Finally, two example circuits are analysed to demonstrate the model application.

2. TIMING MODEL

The notation used is given in Appendix I.

2.1. Formulation method

The general procedure to develop a timing model for the E/D NMOS logic starts by obtaining characteristic wave-forms[7,9,10,21] from SPICE[21] simulations. The operating regions of each MOSFET during the rising or falling period are then determined. According to the change of operating regions, the whole rising or falling time period is further divided into several regions. In each region, the large-signal equivalent circuit of the logic gate is constructed. To obtain analytical timing equations, the device current in each region is re-expressed as a simplified equation obtained by curve fitting to the theoretical current. The corresponding voltage-dependent capacitances are also linearized as the fixed capacitances at the centre point of each region. Using suitable boundary conditions, the whole expression for the output voltage during the rising or falling period can be solved. Rise/fall times and delay times are then solved

and extensive comparisons with SPICE simulation results are made to verify the accuracy. In the following subsections, the timing model of an E/D NMOS inverter will be derived as an illustrative example.

2.2. *Fall time*

Consider a string of identical E/D NMOS inverters as shown in Figure 1. If the input of the inverter string is excited by either a fast or a slow input, the output wave-forms after three or four stages gradually converge to the same shape, which is independent of the input excitation wave-forms. This repetitive wave-form, called the characteristic wave-form, has been noted in developing NMOS timing models.[7,9] Typical SPICE-simulated falling characteristic wave-forms for 1·0 μm E/D NMOS inverters are shown in Figure 2. It is seen that when the input voltage V_i rises from its undershooting valley voltage V_{vr} towards the supply voltage V_{DD}, the output voltage V_{o1} first overshoots to a peak voltage V_{pf} and then decreases towards the voltage V_L of logic '0'. Also indicated in the wave-forms are the fall time T_F, the fall delay T_{PHL} and the initial fall delay T_{DIF}. This initial delay plays a very important role in determining the pair delay of a logic gate, as will be seen later. Besides the input–output wave-forms of the driving stage, the wave-form of the output voltage V_{o2} in the load stage is also shown in Figure 2. The change of V_{o2} leads

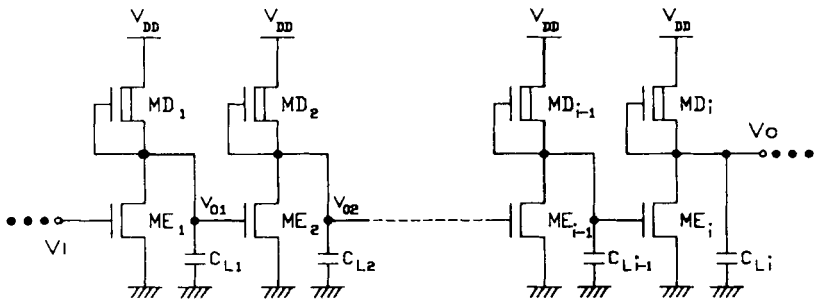

Figure 1. A chain of identical E/D NMOS inverters

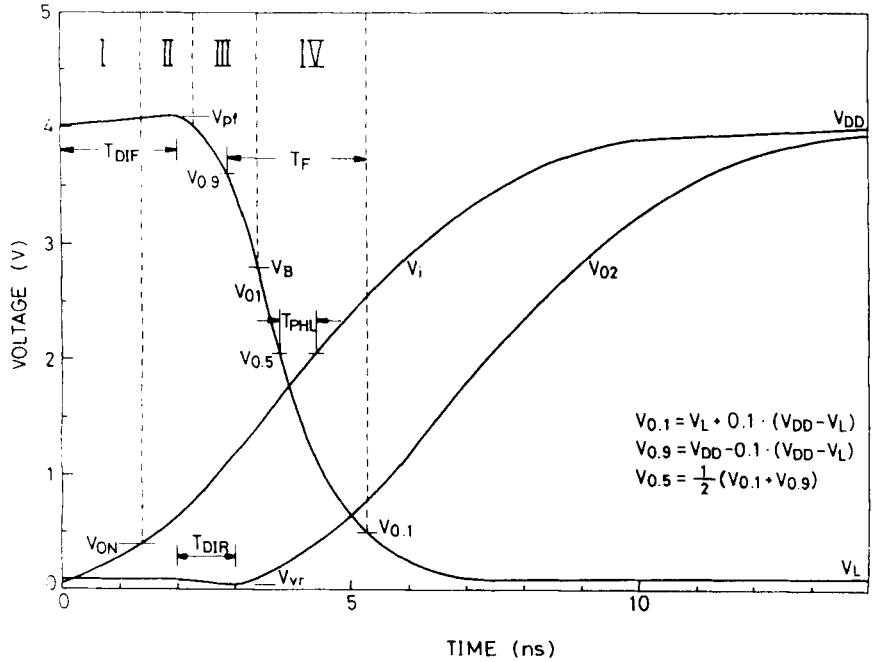

Figure 2. Typical simulated falling characteristic wave-form of a string of identical E/D NMOS inverters and its region partitions

to different device capacitances of M_{E2}, and thus to different loading capacitances of the driver stage, and must be considered.

According to the operating regions of the MOS devices in the driving stage, the falling wave-form of V_{o1} from $t = 0$ to $t = t_{0\cdot1}$ (i.e. $V_{o1} = V_{0\cdot1}$) is divided into four regions as shown in Figure 2. In region I, where V_i rises from V_{vr} to V_{ON1},[21] the enhancement NMOS M_{E1} of the driving inverter is operated in the subthreshold region because its gate–source voltage ($= V_i$) is smaller than its turn-on voltage V_{ON1}. The depletion NMOS M_{D1} is operated in the inverse linear region with its upper n^+ region connected to V_{DD} and the lower n^+ region connected to V_{o1}, which is higher than V_{DD} in region I because of overshooting. Thus, the source/drain nodes of M_{D1} are interchanged and it is operated in the linear region with a small V_{DS}. In the load stage, the MOS M_{E2} is in the linear region since V_{o1} ($= V_{GS2}$) is much higher than V_{o2} ($= V_{DS2}$).

In region II, the final boundary is set to the point where V_{o1} falls back to V_{DD} after overshooting. In this region, the operating region of the NMOS M_{E1} is changed from the subthreshold region into the saturation region, while those of M_{D1} and M_{E2} remain unchanged. Regions I and II are two specific regions with abnormal device operation and distinct transient behaviour. The pair delay, however, is dominated by these two regions and the corresponding regions in the rise time case. Thus they have to be carefully characterized. Regions III and IV also have their own device operation regions which, together with those of regions I and II, are given in Table I. The boundary between regions III and IV is at $V_{o1} = V_B$, where V_B is the saturation drain/source voltage of the depletion NMOS M_{D1} under the substrate bias. It can be calculated by using the suitable model equations in SPICE.

Generally, the large-signal equivalent circuit of an E/D NMOS inverter can be drawn as shown in Figure 3, where the device capacitances C_{1n1} (unused), C_{2n1} and C_{out} as well as the device currents I_{DD} and I_{DE} have different expressions in each of the four regions. The output capacitance C_{out} has three different parts, namely the device capacitances of M_{E1} and M_{D1}, the fixed external load capacitance C_L and the equivalent input capacitance of the load stage. Through the equivalent input capacitance in the load stage, the large-signal equivalent circuit for the fall time calculations can be decoupled and reduced to that of an inverter with a suitable C_{out}.

The wave-form of the input voltage V_i can be approximated by an exponential function with a single effective pole P_{1r} as

$$V_i(t) = D_{1r} \exp(-P_{1r}t) + D_{2r} \tag{1}$$

where P_{1r}, D_{1r} and D_{2r} are determined to match the wave-form at $V_i = V_{vr}$, $V_{0\cdot1}$ and V_B within the first three regions in Figure 2.

Region I. Based on equation (1), the time interval t_1 of region I, i.e. from $V_i = V_{vr}$ to $V_i = V_{ON1}$, can be expressed as

$$t_1 = -\frac{1}{P_{1r}} \ln\left(\frac{V_{ON1} - D_{2r}}{D_{1r}}\right) \tag{2}$$

Table I. Operating regions of the associated MOSFETs in E/D NMOS inverters

Regions		I	II	III	IV
Rise time case	M_{E1}	Linear	Saturation	Cut-off	—
	M_{D1}	Saturation	Saturation	Linear	—
	M_{E2}	Subthreshold	Saturation	Saturation to linear	—
Fall time case	M_{E1}	Subthreshold	Saturation	Saturation	Saturation†
	M_{D1}	Inverse linear	Inverse linear	Linear	Saturation
	M_{E2}	Linear	Linear	Linear	Saturation

† For the long-channel model ($L_{mask} = 3\cdot5\ \mu m$) this is replaced by the linear region.

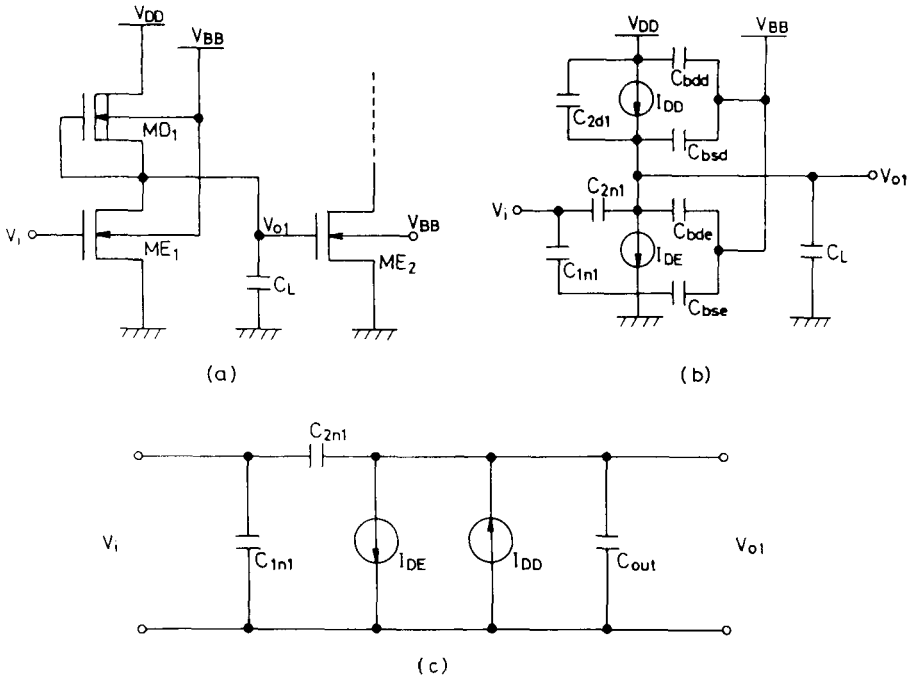

Figure 3. Large-signal equivalent circuit of an E/D NMOS inverter

According to the large-signal equivalent circuit of Figure 3, we have

$$C_{2n1}\frac{d}{dt}(V_{o1}-V_i)+C_{out}\frac{d}{dt}V_{o1}+I_{DE}-I_{DD}=0 \tag{3}$$

During t_1, the change of V_{o1} is much slower than that of V_i, so the term dV_{o1}/dt can be neglected as compared with dV_i/dt. The drain current I_{DE} at $t=t_1$ is calculated by using the subthreshold current equations listed in Table II. The drain current I_{DD} of the depletion NMOS M_{D1} at $t=t_1$ can be calculated by using the linear region current equations in Table II. Since $V_{GS}=V_{DS}=V_{o1}(t_1)-V_{DD}$ in M_{D1} and their values are very small, I_{DD} can be simplified as

$$I_{DD}(t_1)=-[B_2V_{o1}(t_1)+C_2] \tag{4a}$$

where

$$B_2=-\beta_{d1}[V_{bind1}+\tfrac{2}{3}\gamma_{sd1}(2\Phi_{Fd1}+V_{DD})^{0.5}] \tag{4b}$$

$$C_2=\beta_{d1}[V_{bind1}V_{DD}+\tfrac{2}{3}\gamma_{sd1}(2\Phi_{Fd1}+V_{DD})^{0.5}V_{DD}] \tag{4c}$$

$$\beta_{d1}=\frac{W_{d1}}{L_{d1}}\mu_{sd1}C_{od1} \tag{4c}$$

From the above considerations and using equations (4) and (1), equation (3) can be used to solve $V_{o1}(t_1)$, which is

$$V_{o1}(t_1)=\frac{1}{B_2}[C_{2n1}P_{1r}(D_{2r}-V_{ON1})-I_{DE}(t_1)-C_2] \tag{5}$$

where $C_{2n1}=C_{gdove1}W_{e1}$. It should be noted that when $V_i=V_{ON1}$ at $t=t_1$, V_{o1} has not yet reached the peak point, i.e. $V_{o1}(t_1)\neq V_{pf}$.

Table II. MOSFET current equations and junction capacitance equations used in the SPICE program

MOSFET current equations

(1) Subthreshold region:

$$I_{DS} = \beta\{[V_{ON} - V_{BIN} - (\eta/2)V_{DS}]V_{DS} - \tfrac{2}{3}\gamma_s[(2\phi_F + V_{DS} - V_{BS})^{3/2} - (2\phi_F - V_{BS})^{3/2}]\} \exp[q(V_{GS} - V_{ON})/nkT]$$

(2) Linear region:

$$I_{DS} = \beta\{[V_{GS} - V_{BIN} - (\eta/2)V_{DS}]V_{DS} - \tfrac{2}{3}\gamma_s[(2\phi_F + V_{DS} - V_{BS})^{3/2} - (2\phi_F - V_{BS})^{3/2}]\}$$

(3) Saturation region:

$$I_{DS} = \beta\{[V_{GS} - V_{BIN} - (\eta/2)V_{dsat}]V_{dsat} - \tfrac{2}{3}\gamma_s[(2\phi_F + V_{dsat} - V_{BS})^{3/2} - (2\phi_F - V_{BS})^{3/2}]\}$$

where

$$\beta = \frac{W_{eff}}{L_{eff}}\mu_s\frac{\varepsilon_{SiO_2}}{T_{ox}}$$

MOSFET junction capacitance equations

$$C_{bs} = CJ\frac{AS}{(1 - V_{BS}/PB)^{MJ}} + CJSW\frac{PS}{(1 - V_{BS}/PB)^{MJSW}}$$

$$C_{bd} = CJ\frac{AD}{(1 - V_{BD}/PB)^{MJ}} + CJSW\frac{PD}{(1 - V_{BD}/PB)^{MJSW}}$$

Note: The parameters in this table are from SPICE level-2 device models.[21]

Region II. In region II, the device capacitances C_{2n1} and C_{out} can be expressed by using Meyer's model,[14] which is also used in SPICE. The expressions are given in Table III. In equation (2a) of Table III, the value $1 + |Av|$ is the factor used in Miller's theorem to calculate the equivalent input capacitance due to C_{2n2} of the load stage. In the load stage, although the MOS M_{E2} is operated in the linear region, its output voltage is nearly unchanged during the whole interval of region II and can be treated as shorted to ground in the large-signal analysis. This means $Av = 0$ in the capacitance calculation. The voltage-dependent source/drain junction capacitances in the above expressions are linearized by a fixed value calculated at a constant junction bias. This bias is chosen to be that at the central point of each region. The linearized junction capacitances C_{bde1} and C_{bdd1} in region II can be calculated from the SPICE equation with the reverse junction bias fixed at V_{DD} for linearization. Now, C_{2n1} and C_{out} become linear capacitances.

The MOS M_{E1} is operated in saturation and its drain current equation in SPICE is given in Table II. This equation is too complicated to be used in obtaining the analytic solution for $V_{o1}(t)$ from equation (3). Here we use a least-square curve-fitting method to model the current with a simplified formula which has a good accuracy and can be treated analytically in equation (3). In this method, the ranges of V_{GS} and V_{DS} for current calculations are determined first. In region II, the initial boundary is $V_i = V_{ON1}$ and $V_{o1} = V_{o1}(t_1)$ and the final boundary is $V_{o1} = V_{DD}$. The value of V_i at the first boundary of region II is greater than V_{ON1} and is unknown. For the purpose of current calculations, we assume that the value of V_i at the final boundary is $2V_{ON1}$, which is a good approximation. Then the above range is equally divided and four sets of V_i and V_{o1} (i.e. V_{GS} and V_{DS}) can be obtained. Using the four sets of voltages in the saturation current formulae to calculate the drain current and then using the least-square fitting method, we have

$$I_{DE}(t) = A_{2s}V_i^2(t) + A_{1s}V_i(t) + C_{1s} \tag{6}$$

where the constants A_{1s}, A_{2s} and C_{1s} are determined from the least-square fitting method with a typical error of 7%. In equation (6), the term $A_{2s}V_i^2(t)$ is mainly contributed by the term $V_{GS}V_{dsate}$ in the expression of the saturation current; since V_{dsate} is dependent upon $V_{GS} = V_i$, it is V_{GS}^2-dependent or V_i^2-dependent. Another current, $I_{DD}(t)$, has been characterized in equation (4) with t_1 replaced by t.

Table III. The corresponding output capacitance of an E/D NMOS inverter in the individual regions of rising/falling tme period

Fall time

Region II:

$$C_{2n1} = C_{gdove1} W_{e1} \tag{1}$$

$$C_{out} = C_{bde1} + C_{gsd1} + C_{gsovd1} W_{d1} + C_{gbovd1} L_{d1} + C_{bdd1} + (C_{gdove2} W_{e2} + C_{gde2})(1 + |Av|) + C_{gbove2} L_{e2} + C_{gsove2} W_{e2} + C_{gse2} + C_L \tag{2a}$$

$$C_{gde2} = \tfrac{2}{3} C_{oe2} [1 - V_{dsate2}^2/(2V_{dsate2} - V_L)^2] \tag{2b}$$

$$C_{gse2} = \tfrac{2}{3} C_{oe2} [1 - (V_{dsate2} - V_L)^2/(2V_{dsate2} - V_L)^2] \tag{2c}$$

$$C_{gsd1} = 0{\cdot}5\, C_{od1} \tag{2d}$$

$$Av = 0 \tag{2e}$$

$$C_{bde1} = CJ_{e1} \frac{AD_{e1}}{(1 + V_{DD}/PB_{e1})^{MJ_{e1}}} + CJSW_{e1} \frac{PD_{e1}}{(1 + V_{DD}/PB_{e1})^{MJSW_{e1}}} \tag{2f}$$

Region III:

$$C_{out} = C_{bde1} + C_{gdd1} + C_{gdovd1} W_{d1} + C_{gbovd1} L_{d1} + C_{bsd1} + (C_{gdove2} W_{e2} + C_{gde2})(1 + |Av|) + C_{gbove2} L_{e2} + C_{gsove2} W_{e2} + C_{gse2} + C_L \tag{3a}$$

$$C_{gde2} = \tfrac{1}{2} C_{oe2} \tag{3b}$$

$$C_{gse2} = 1/2\, C_{oe2} \tag{3c}$$

$$C_{gdd1} = \tfrac{2}{3} C_{od1} \{1 - V_{dsatd1}^2/[2V_{dsatd1} - (V_{DD} - V_{DS})]^2\} \tag{3d}$$

$$V_{DS} = 0{\cdot}5(V_{DD} + V_B) \tag{3e}$$

$$Av = 0 \tag{3f}$$

Rise time

Region I:

$$C_{out} = C_{bde1} + C_{gdd1} + C_{gdovd1} W_{d1} + C_{gbovd1} L_{d1} + C_{bsd1} + (C_{gdove2} W_{e2} + C_{gde2})(1 + |Av|) + C_{gbove2} L_{e2} + C_{gsove2} W_{e2} + C_{gse2} + C_{gbe2} + C_L \tag{4a}$$

$$Av = 0 \tag{4b}$$

$$C_{gdd1} = 0 \tag{4c}$$

$$C_{gde2} = 0 \tag{4d}$$

$$C_{gse2} = \tfrac{2}{3} C_{oe2} - \tfrac{4}{3} [(V_{ON2} - V_{GS2})/2\phi_{fe}] C_{oe2} \tag{4e}$$

$$C_{gbe2} = [(V_{ON2} - V_{GS2})/2\phi_{fe}] C_{oe2} \tag{4f}$$

$$V_{GS2} = V_{o1} = 0{\cdot}5(V_L + V_{ON2}) \tag{4g}$$

Region III:

$$C_{gde2} = \tfrac{1}{4} C_{oe2} \tag{5a}$$

$$C_{gse2} = \tfrac{1}{2}(\tfrac{1}{2} C_{oe2} + \tfrac{2}{3} C_{oe2}) \tag{5b}$$

$$C_{gdd1} = \tfrac{2}{3} C_{od1} \left(1 - \frac{V_{dsatd1}^2}{\{2V_{dsatd1} - [V_{DD} - 0{\cdot}5(V_{0{\cdot}9} + V_B)]\}^2}\right) \tag{5c}$$

$$Av = -1 \tag{5d}$$

The V_{o1} in the s-domain can be solved from the equivalent circuit. The detailed procedure is given in Appendix II. Taking the inverse Laplace transformation of $V_{o1}(s)$, $V_{o1}(t)$ in region II is solved as

$$V_{o1}(t) = F_1 e^{-2P_1 t} + F_2 e^{-P_2 t} + F_3 e^{-P_3 t} + F_4 \tag{7}$$

Letting $dV_{o1}(t_2)/dt = 0$, the time t_2 when V_{o1} reaches the overshooting peak V_{pf} can be obtained. Therefore the initial fall delay T_{DIF} can be expressed as $T_{DIF} = t_1 + t_2$. Additionally, the input voltage used as the initial value $V_{i3}^{(0)}$ of region III is calculated at $V_{o1} = V_{DD}$.

Region III. In region III, the MOS M_{D1} returns to normal operation with its gate and source shorted together and provides a current to charge the output capacitive load. However, the pull-down current I_{DE} has exceeded the pull-up current I_{DD} and their difference becomes more and more prominent, leading to an output voltage falling down faster than rising up. This is because the driving capability of the MOS M_{E1} is larger than that of M_{D1} owing to the larger beta ratio which is necessary to retain a reasonable noise margin. As seen in Figure 2, the MOS M_{E1} is operated in the saturation region whereas the MOS M_{D1} is operated in the linear region during the time interval of region III. The value of $|Av|$ is empirically fixed to be zero according to the changes of V_{o1} and V_{o2} in region III.

The large-signal equivalent circuit is similar to Figure 3 and the Kirchhoff's Current Laws (KCL) equation is the same as equation (16) of Appendix II except that I_{DD} is expressed as

$$I_{DD}(t) = \begin{cases} B_{2l}V_{o1}(t) + C_{2l} & \text{(linear region)} \quad (8a) \\ B_{2s}V_{o1}(t) + C_{2s} & \text{(saturation region)} \quad (8b) \end{cases}$$

The least-square current-fitting method is also applied to model the depletion MOS current with $V_{GS} = 0$. The currents in both saturation and linear regions can be linearized by straight lines whose equations are given by (8).

With four different sets of voltages within the range from $V_i = V_{i3}^{(0)}$ to $V_i = V_B + 2V_{ON1}$, another current, I_{DE}, is expressed by using the curve-fitting method in the same way as for equation (6) in region II. Although the final boundary of V_i may deviate slightly from the chosen value, equation (6) can still accurately characterize the drain current of M_{E1}. In other words, the approximation of the device current is less sensitive to the final boundary condition. The induced error is then tolerable.

Except that the gate–drain capacitance C_{2n1} can still be expressed by equation (1) of Table III, the contribution of device capacitances to C_{out} is different from that in region II, mainly caused by the MOS M_{D1} now with its gate shorted to its source. C_{out} is expressed as listed in Table III. Note that the value of V_{DS} at the central point of region II is taken to linearize C_{gd1}, C_{bde1} and C_{bsd1}. In addition, Av is set to zero as discussed before. It should be noted that Meyer's capacitance model in SPICE has been adopted to express the gate–drain capacitance C_{gd1}, which changes continuously from the highly linear region to the slightly linear region of M_{D1}. On the other hand, the capacitances C_{gde2} and C_{gse2} are assumed to be $\frac{1}{2}C_{oe2}$, a good approximation for the MOS M_{E2} in the highly linear region with a large V_{GS}. After capacitance linearization, all capacitances become linear. The output $V_{o1}(t)$ in region III is then expressed as equation (7) with $P_f = -B_{2l}/C_T$. The time T_{F1} from $V_{0.9}$ to V_B is then calculated from $V_{o1}(t)$.

Region IV. In region IV, the operation of inverters with short-channel devices ($L_{mask} = 1.0\ \mu m$) is different from that of inverters with long-channel devices ($L_{mask} = 3.5\ \mu m$). From SPICE transient data, we find that even though V_i is raised to a high level in region IV, the saturation voltage V_{dsate1} for short-channel devices is still very small. Thus in region IV, the MOS M_{E1} is mostly operated in saturation. However, for long-channel devices, the MOS M_{E1} changes its operation region from the saturation region to the linear region instead. From SPICE DC analysis, the saturation voltage V_{dsate} of $1.0\ \mu m$ enhancement NMOS at $V_{GS} = V_{DD}$ is about 0·67 V, implying that the MOS M_{E1} is always operated in saturation even when the output voltage has fallen to $V_{0.1}$. But for $3.5\ \mu m$ enhancement NMOS, the saturation voltage V_{dsate} is about 2·3 V when $V_{GS} = V_{DD}$. Thus the MOS M_{E1} changes its operation region to the linear region when the output voltage falls below 2·3 V. In developing this timing model, both the above cases were considered, but only the short-channel case is discussed in the following analysis.

According to the output response derived in region III, the value of V_i at $V_{o1} = V_B$ can be obtained, which is the initial boundary of region IV. Because of the same operation region of the MOS M_{E1} in both regions III and IV, equation (6) is still used to approximate the pull-down current I_{DE}. The pull-up current I_{DD} has the same form as equation (8b).

In region IV, the expression of C_{out} is similar to equation (3a) of Table III except that M_{D1} is operated in the saturation region and the voltage gain Av should be considered. The gate–drain capacitance C_{gd1} is now equal to zero. The voltage gain Av is empirically determined to be -0.5. In addition, because the

MOS M_{E2} is in saturation, we have

$$C_{gde2} = 0 \tag{9a}$$

$$C_{gse2} = \tfrac{2}{3} C_{oe2} \tag{9b}$$

For the input voltage V_i, the expression of equation (1) is used but with D_{1r}, D_{2r} and P_{1r} replaced by E_{1r}, E_{2r} and P_{2r}. These three new constants can be obtained from the calculation of the rise wave-form in region II. The resulting formula is the same as equation (7) but with $P_f = -B_{2s}/C_T$. From the formula, the time interval T_{F2} from V_B to $V_{0\cdot1}$ can be determined.

Combining both output responses in regions III and IV, we obtain the fall time T_F as

$$T_F = T_{F1} + T_{F2} \tag{10}$$

Note that T_F is a function of the rise poles P_{1r} and P_{2r}.

2.3. *Rise time*

In the rise time case, the simulated characteristic wave-forms are shown in Figure 4 with three divided regions. The operation regions of the associated MOS devices in each region are listed in Table I. Note that the MOS M_{E1} in the driver stage is turned off for most of regions II and III. Thus the input waveform has only a limited effect on the rising output, as already recognized in Reference 10.

Region 1. The purpose of defining region I is to calculate the initial rise delay. From Figure 4, it is seen that when V_i falls quickly from V_{pf} to V_L, the output voltage of the driver stage initially at V_L first undershoots to a valley voltage V_{vr} and then rises slowly towards V_{DD}. This undershoot is related to the inital rise delay T_{DIR}. Because all the device currents in this region are extremely small, the input wave-form near the peak point is fairly importnat for the initial delay calculation and has to be accurately modelled. Thus the wave-forms in regions II and III of the falling wave-form are taken into account and approximated by the following single-pole response:

$$V_i(t) = (V_{pf} - V_L)\exp(-P_{1f}t) + V_L \tag{11a}$$

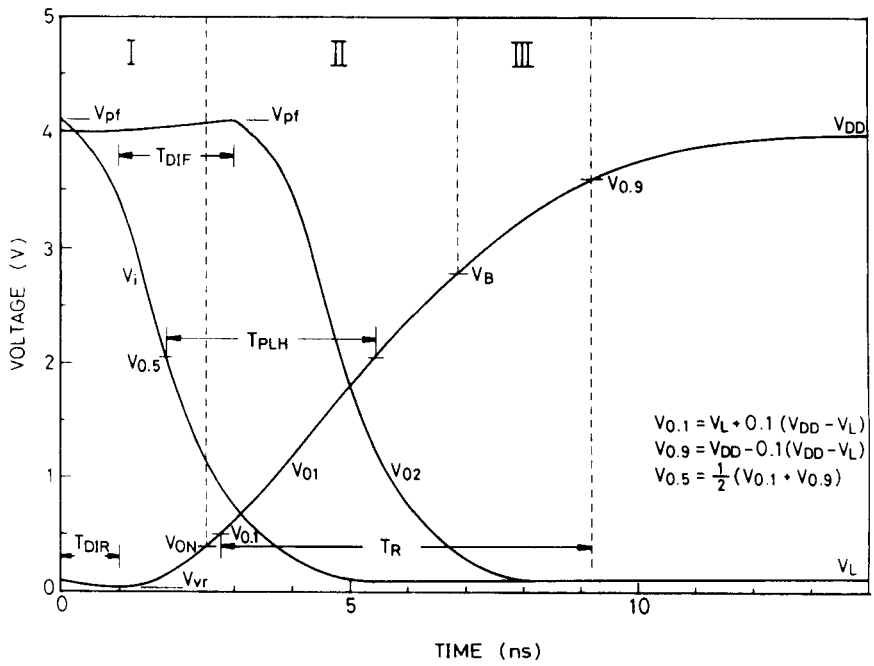

Figure 4. Typical simulated rising characteristic wave-form of a string of identical E/D NMOS inverters and its region partitions

To find the effective pole P_{1f}, we choose the point at $t = t_B$ when $V_i = V_B$ as the matching point. Thus P_{1f} can be solved as

$$P_{1f} = \frac{1}{t_B} \ln\left(\frac{V_{pf} - V_L}{V_B - V_L}\right) \tag{11b}$$

where V_B and t_B have been modelled in the fall time case. It is found that this approximation can dramatically improve the accuracy of the initial delay calculation.

In region I, the depletion current of M_{D1} is still the same as equation (8) in the saturation region. Because the MOS M_{E2} in the load stage is cut off, its output voltage is nearly unchanged so that the miller effect can be neglected (i.e. $Av = 0$). On the other hand, the MOS M_{E1} is in the linear region and its drain current as shown in Table II includes the $V_i V_{o1}(V_{GS} V_{DS})$ term. This term has to be linearized to obtain the analytical expression for the output voltage. It is found that simple linearization of $A_{11}V_i + B_{11}V_{o1}$ is unable to linearize the $V_i V_{o1}$ term with a good accuracy. Instead, the following expression to decouple the $V_i V_{o1}$ term is proposed and has proved to be satisfactory:

$$I_{DE}(s) = A_{21}V_i^2 + A_{11}V_i + B_{11}V_{o1} + C_{11}/s \tag{12}$$

where the coefficients A_{11}, A_{21}, B_{11} and C_{11} are calculated by using the least-square fitting method with four sets of (V_i, V_{o1}) equally divided in region I. In equation (12), the V_i^2 dependence is caused by the strong dependence of the output wave-form V_{o1} upon the input V_i during the voltage undershoot.

The large-signal equivalent circuit in the rise time case is the same as shown in Figure 3 but with different device capacitances according to the different device operation regions. The general form of the total output capacitance is given in Table III. For accurate calculations, the weak inversion of the MOS M_{E2} should be taken into consideration. Its gate–source and gate–bulk capacitances[21] are also listed in Table III. In equations (5b) and (5c) of Table III, V_{GS2} represents the midpoint of the output wave-form in region I, which is used for linearization. Substituting equation (4) of Table III, equations (8) and (12) into equation (16) of Appendix II, we obtain an expression of the output voltage wave-form similar to that in equation (7). The initial rise delay T_{DIR} can be obtained by taking $dV_{o1}(T_{DIR})/dt = 0$. Thus the pair delay is expressed as

$$T_{PD} = T_{DIF} + T_{DIR} \tag{13}$$

Additionally, the input voltage at $V_{o1} = V_{ON2}$ is found, which serves as the initial value of region II.

Region II. The MOS M_{E1} in region II is not always off. For inverters with a particular beta ratio, it may be operated in saturation. Thus the MOS M_{E1} is assumed to be in saturation and its current equation is approximated by equation (6). If the device is off, the resulting equation (6) will be very small. Thus the above two cases can be characterized as well. From Table I, the MOS M_{D1} is in saturation. Its current expression is given in equation (8).

In the calculations of regions II and III, the fall pole in equation (11a) is replaced by P_{2f}, which is determined as

$$P_{2f} = \frac{1}{T_F} \ln(9) \tag{14}$$

As seen in Figure 3, the capacitance C_{2n1} is the same as that in region I. The output capacitive load C_{out} can be expressed as equation (4a) of Table III without the terms C_{gbe2}, C_{gdd1} and C_{gde2}. The term Av is set to -1. Since the MOS M_{E2} is operated in the saturation region, the gate–source capacitance C_{gse2} is estimated to be $\frac{2}{3}C_{oe2}$. Then the output expression can be solved similarly to that in equation (7). The time interval from $V_{o1} = V_{0\cdot1}$ to $V_{o1} = V_B$, which is called T_{R1}, can then be obtained.

Region III. The analysis of region III is much simpler than that of any other region. The MOS M_{E1} is definitely cut off; only the MOS M_{D1}, operated in the linear region, charges the output capacitive load.

Its current is expressed in equation (8). As may be seen from SPICE transient data, it is found that the MOS M_{E2} in the load stage is operated in saturation first and then in the linear region. To simplify the analysis, the capacitances in the two regions are averaged. The resulting expressions are listed in Table III. The calculated output response is solved similarly to that in equation (7). Thus the time interval T_{R2} between $V_{o1} = V_B$ and $V_{o1} = V_{0.9}$ can be calculated. Finally, the rise time T_R is obtained as

$$T_R = T_{R1} + T_{R2} \tag{15}$$

Note that T_R is a function of the fall poles P_{1f} and P_{2f}. Numerical iterations are thus required to solve T_R and T_F. The iteration method is described below.

2.4. Calculation method

Since the rising output wave-form is nearly indpendent of the input wave-form, we can roughly calculate the rise time T_R and the rise poles P_{1r} and P_{2r} by assuming that the MOS M_{E1} is off and only the MOS M_{D1} charges the output capacitive load with a step input excitation, i.e. $P_{1f}, P_{2f} \to \infty$. The solved rise poles are then used as the initial guess in the fall time calculations. After the fall time T_F has been obtained from the calculation, it is transformed into the fall poles P_{1f} and P_{2f} in equations (11b) and (14) respectively. These are then used in the rise time calculation to obtain a new T_R. The iterations are stopped when the error between two successive iterations has been reduced to a specified value. Then all the timing data (T_R, T_F, T_{DIR}, T_{DIF}, T_{PD}, T_{PLH}, T_{PHL}, etc.) can be obtained. Generally, the number of iterations is less than three with a final error of 5% between two successive iterations. Thus the computer time consumed is quite small.

3. COMPARISONS WITH SPICE SIMULATION RESULTS

To verify the accuracy of the modelling method, we used the same device current and capacitance equations as in SPICE, and SPICE simulations were performed for comparisons. Wide-range comparisons are given to verify the generality of the models in characterizing inverters with different beta ratios, sizes, device parameters, input wave-forms and capacitive loads. Some of the comparisons will be presented in this section.

There are three kinds of error sources in this timing model. The first is due to the linearization on various voltage-dependent MOSFET channel capacitances and p–n junction capacitances. The second arises from the single-pole assumption for the input wave-forms used in the calculations of output responses. The last is due to the drain current approximation. The effects of these error sources will be investigated later.

In Figure 5 we show the rise time, fall time and delay time of characteristic wave-forms in 1·0 μm E/D NMOS inverters with different capacitive loads. Similar data for 3·5 μm E/D NMOS inverters are listed in Table IV for different size factors S. It is seen from these comparisons that for large fixed capacitive loads C_L ($C_L \geqslant 0{\cdot}1$ pF for 1·0 μm and $C_L \geqslant 0{\cdot}5$ pF for 3·5 μm) and $S = 1$, the calculation errors of rise time and pair delay are below 12%, while those of fall time are below 8%. This is because all the internal device capacitances become negligible compared with the load capacitance C_L. Thus the error in this case is from the drain current and input wave-form approximations. It is also shown that for small-size inverters with $S = 1$ and large C_L, the errors remain nearly the same for different C_L values. However, for $S = 10$ the internal device capacitances contribute another error source and the errors deviate when C_L changes.

Listed in Table V are the calculation results of this work and the model developed by Auvergne *et al.*[11] for 3·5 μm inverters. It is found that the errors are comparable in the two models for $\alpha = 3$, but for small and large values of α the error of Reference 11 is worse. The possible cause is the assumption of a ramp input, the oversimplifying expressions of device currents and the rough definition of device operations as discussed in Reference 11.

It is known that process variations in E/D NMOS are quite large. Thus the accuracy of a timing model

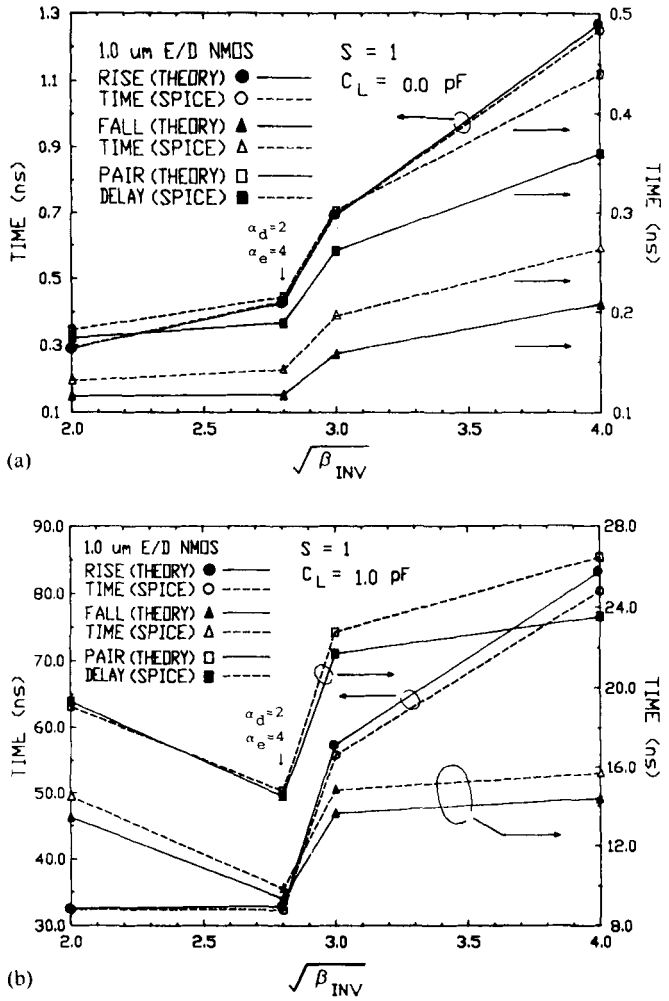

Figure 5. Comparisons of calculated SPICE simulated rise/fall/delay times of 1·0 μm E/D NMOS inverters: (a) $C_L = 0$ pF; (b) $C_L = 1{\cdot}0$ pF. All inverters are designed with $\alpha_d = \alpha_e = \sqrt{\beta_{INV}}$ except the one indicated in the figure

Table IV. Errors of rise/fall/delay times in the case of characteristic wave-forms for 3·5 μm E/D NMOS inverters with different sizes and different capacitive loads

		S	1·0				10·0	
		α_d	2·0	4·0	1·0	16·0	2·0	4·0
Dimension		α_e	2·0	4·0	16·0	1·0	2·0	4·0
Error (%)	0 pF	T_R	1·65	5·27	−4·92	20·78	10·57	14·87
		T_F	2·03	−8·35	−14·76	1·08	−4·09	0·73
		T_{PD}	−1·65	2·16	−17·46	−7·91	−13·77	1·48
	0·5 pF	T_R	2·79	7·69	0·35	11·21	9·74	15·10
		T_F	4·63	−4·23	−7·69	−2·96	0·20	0·57
		T_{PD}	3·90	−1·62	−10·79	−5·05	−10·87	−1·44
	2·0 pF	T_R	3·10	8·21	1·14	10·13	9·15	12·87
		T_F	4·71	−3·63	−5·42	−3·10	4·94	2·02
		T_{PD}	4·20	−9·96	−8·22	−11·66	−6·90	3·15

$\alpha_d = L_d/W_d$; $\alpha_e = W_e/L_e$; $S = L_e/3{\cdot}5\ \mu m = W_d/3{\cdot}5\ \mu m$.

Table V. Comparisons of SPICE simulated pair delay times with those calculated by the models in Reference 11 and this work

Type		Pair delay T_{pd} (ns)		
α	S	SPICE	Ref. 11	This work
2	1	53·03	37·05	55·26
3	1	69·33	80·16	64·10
4	1	83·53	123·32	75·12
2	10	139·59	83·31	129·96
3	10	204·34	203·96	195·27
4	10	279·89	364·47	288·69

$\alpha = L_d/W_d = L_e/W_e$; $S = L_e/3{\cdot}5\ \mu m = W_d/3{\cdot}5\ \mu m$; $C_L = 2{\cdot}0$ pF.

has to be retained under these variations. To test the capability of the developed timing model in this respect, extensive comparisons between SPICE simulation and model calculation results were made for inverters with different values of the device parameters. Some of the comparisons are listed in Table VI for a 3·5 μm E/D NMOS inverter with a beta ratio of 9. In this table, the variations in V_{TO}, T_{ox}, U_O and V_{MAX} (SPICE[21] parameters) as well as two different variation cases, called the fast case and the worst case, are considered. The resulting error is similar to that in the normal case. Thus the developed model is still applicable under these inevitable process variations. This generality comes from the fact that all the SPICE device parameters are considered in the timing model.

In the developed timing models, although the equations are derived from consideration of the characteristic wave-form, the effect of input wave-forms is considered through the use of the least-square curve-fitting method. The timing models can therefore handle the non-characteristic wave-form cases mentioned above. To show the capability of this timing model to deal with step input excitations, examples are given in Table VII for inverters with different beta ratios and capacitive loads. In this table, we calculate the propagation rise/fall delay instead of the initial rise/fall delay, because it is the delay of the stage connected to the external input. As shown in Table VII, the maximum error is less than 33% for rise/fall times and less than 29% for propagation rise/fall delays.

The simulated and calculated signal timings for the exponential input as a function of the normalized

Table VI. Errors introduced from variations of threshold voltage; gate oxide thickness, mobility and maximal drift velocity for an E/D NMOS inverter with different load capacitance, including fast-speed case and worst-performance case

Error (%)		ΔV_{TO}(V)		ΔT_{ox}(Å)		ΔU_O ($m^2/V-s$)		ΔV_{MAX} ($m\,s^{-1}$)		Fast case	Worst case
		−0·16	+0·16	−60	+60	−50	+50	-2×10^4	$+2\times10^4$		
0 pF	T_R	4·83	4·57	4·44	5·04	4·81	4·69	5·42	5·08	4·69	5·01
	T_F	−4·71	−2·81	−4·30	−3·01	−3·26	−3·60	−3·82	−3·63	−5·49	−1·85
	T_{PD}	−8·04	2·51	−11·59	−12·00	−11·88	−11·47	−11·14	−11·89	−8·19	3·76
0·5 pF	T_R	6·78	7·28	7·50	7·48	7·34	7·39	6·78	7·54	7·15	7·33
	T_F	−1·10	0·31	−0·80	0·06	0·04	−1·29	−1·40	−0·97	−1·19	0·96
	T_{PD}	−8·70	−0·41	−7·95	−7·50	−8·06	−7·39	−6·54	−7·81	9·83	0·44
2·0 pF	T_R	7·49	7·87	7·29	7·74	7·90	7·64	7·09	8·17	7·69	6·80
	T_F	−0·58	1·44	−0·37	1·06	1·11	0·54	0·67	0·17	−0·80	0·25
	T_{PD}	9·93	−2·90	−7·75	−7·35	−7·43	−7·33	−5·93	−7·73	10·81	−2·23

$L_d = 10{\cdot}5\ \mu m$; $W_d = 3{\cdot}5\ \mu m$; $L_e = 3{\cdot}5\ \mu m$; $W_e = 10{\cdot}5\ \mu m$.

Table VII. Errors of rise/fall/delay times of E/D NMOS inverters with different load capacitances and driven by a step input

	α	2				4			
	C_L (pF)	0	0·5	1·0	2·0	0	0·5	1·0	2·0
T_R (ns)	SPICE	2·32	23·63	44·91	87·53	8·10	54·91	101·80	195·40
	Theory	2·11	23·23	44·19	86·46	7·87	57·47	107·05	206·70
	Error(%)	−9·15	−1·68	−1·61	−1·23	−2·80	4·67	5·15	5·78
T_F (ns)	SPICE	0·746	7·43	14·16	27·63	0·44	2·79	5·32	9·78
	Theory	0·501	5·19	9·86	19·19	0·41	2·77	5·12	9·80
	Error(%)	−32·82	−30·15	−30·37	−30·56	−6·87	−0·79	−3·88	0·17
T_{PLH} (ns)	SPICE	0·920	9·46	17·93	34·86	4·68	25·78	47·40	90·62
	Theory	1·136	11·72	22·27	43·29	4·53	30·24	56·08	107·57
	Error(%)	14·48	23·86	24·19	24·17	−4·81	17·32	18·30	18.70
T_{PHL} (ns)	SPICE	0.270	2.67	5.04	9.82	0.200	1.27	2.32	4.55
	Theory	0.194	1.92	3.64	7.08	0.157	1.01	1.86	3.55
	Error(%)	−28.20	−28.25	−27.82	−27.90	−21.41	−20.78	−19.99	−21.90

$\alpha = L_d/W_d = W_e/L_e$; $L_e = W_d = 3{\cdot}5$ μm.

Table VIII. Timing data obtained from this work and SPICE for a chain of 12-stage E/D NMOS inverters with different capacitive loads and driven both by a step input and a ramp input ($T_F = 80$ ns)

Stage		Step input			Ramp input		
		SPICE(ns)	Theory(ns)	Error(%)	SPICE(ns)	Theory(ns)	Error(%)
0·2 pF	T_R	18·58	19·13	2·98	30·55	20·14	−34·08
	T_{DIT}	0·20	0·00	−100·00	0·56	1·64	192·22
0·4 pF	T_F	9·33	7·91	−15·24	13·09	8·64	−34·03
	T_{DIT}	1·10	1·06	−3·78	59·84	69·81	16·67
0·6 pF	T_R	45·78	47·27	3·25	46·10	47·16	2·30
	T_{DIT}	1·40	1·69	20·88	59·84	70·49	17·80
0·8 pF	T_F	19·01	17·34	−8·79	18·62	17·38	−6·65
	T_{DIT}	14·30	15·44	7·98	85·84	85·01	−0·97
1·0 pF	T_R	73·11	75·33	3·04	73·17	75·13	2·68
	T_{DIT}	14·30	16·49	15·33	85·84	86·09	0·29
2·0 pF	T_F	34·66	33·01	−4·76	35·13	33·06	−5·89
	T_{DIT}	41·60	43·83	5·36	111·30	113·44	1·92
1·0 pF	T_R	73·74	75·47	2·34	73·92	75·50	2·14
	T_{DIT}	41·60	45·25	8·77	111·30	114·88	3·22
0·8 pF	T_F	25·05	22·90	−8·58	25·00	22·87	−8·53
	T_{DIT}	89·60	94·74	5·74	161·20	164·51	2·05
0·6 pF	T_R	46·58	47·11	1·15	46·77	47·03	0·55
	T_{DIT}	89·60	95·98	7·12	161·20	165·74	2·82
0·4 pF	T_F	15·70	13·44	−14·42	15·92	13·44	−15·55
	T_{DIT}	125·60	126·86	1·01	192·40	196·58	2·18
0·2 pF	T_R	19·97	18·94	−5·16	20·08	18·94	−5·70
	T_{DIT}	125·60	127·65	1·63	193·00	197·37	2·26
1·2 pF	T_F	14·26	13·03	−8·63	14·53	13·03	−10·35
	T_{DIT}	146·10	141·20	−3·35	216·15	216·90	0·35
T_{DT}		163·10	157·80	−3·25	183·50	177·49	−3·27
CPU time (s)		782·69	11·48		818·66	12·80	

$L_d = 10{\cdot}5$ μm; $W_d = 3{\cdot}5$ μm; $L_e = 3{\cdot}5$ μm; $W_e = 10{\cdot}5$ μm.

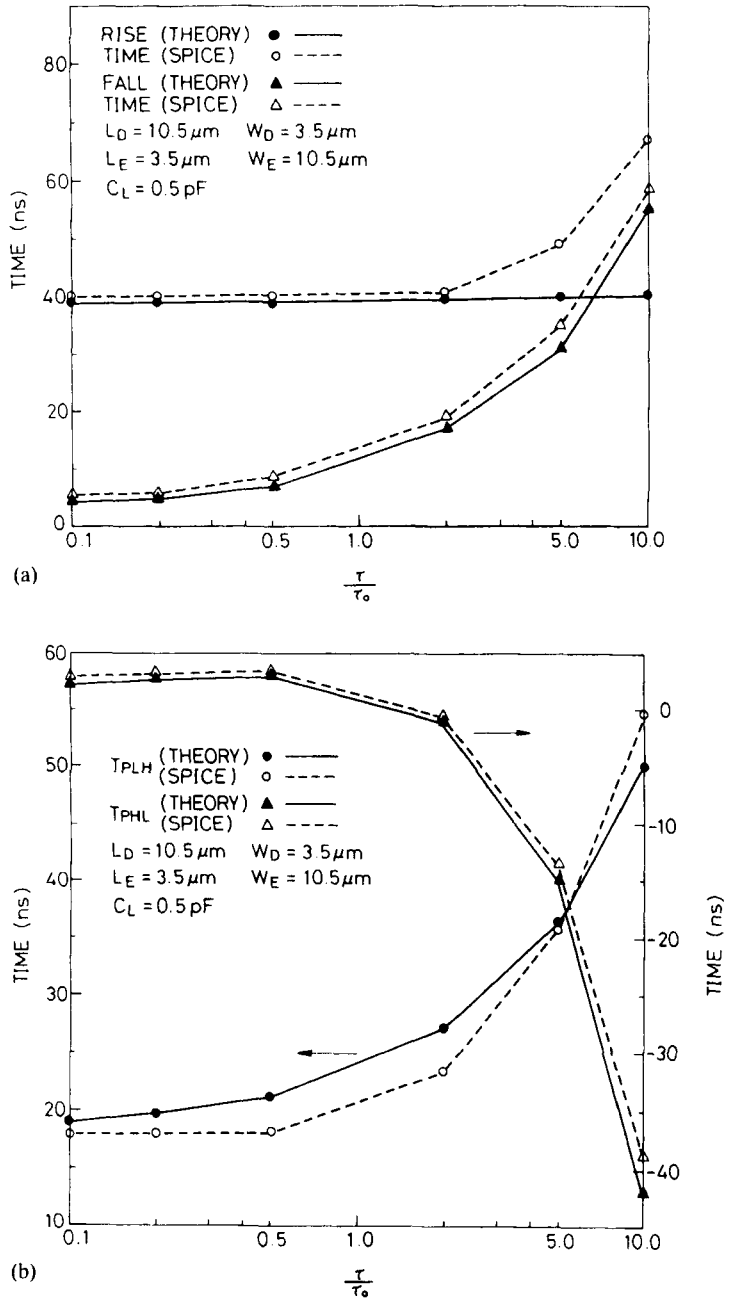

Figure 6. Rise/fall/delay times of 3·5 μm E/D NMOS inverters with exponential inputs

transition time τ/τ_0 are shown in Figure 6. Similar error characteristics are also found in the ramp input case. The normalized transition time, which ranges from 0·1 to 10, incudes both the fast input and the slow input excitations. The calculation method is similar except that the input wave-form function is known. In the case of exponential inputs in Figure 6, less than 17% error is obtained for $\tau/\tau_0 < 1$. However, when $\tau/\tau_0 > 1$, the error in the rise times increases to -39% because of the inadequate device operation assumed in region III of the rise time. The magnitude of the propagation fall delay in the case of $\tau/\tau_0 = 2$ in Figure 6(b) is too small and thus introduces a large error (160%). Fortunately, the

contribution of this term to the pair delay is negligible and can be ignored. From the above comparisons, it is shown that the proposed timing models can be applied to any input wave-forms up to 10 times as fast or slow as the characteristic wave-form.

4. APPLICATION EXAMPLE

As an application example of the developed timing models in timing analysis, the signal timing of a chain of 12-inverter stages with different capacitive loads is calculated. The signal timings under both step input and slow ramp input ($T_F = 80$ ns) excitations are shown in Table VIII. It is seen that the rise/fall times in these two cases have an error of less than 16% except for the first two stages in the ramp input case. In the case of step input excitations, the total initial delay T_{DIT} introduces an error of -100% in the first stage; this then gradually converges to below 9% after the sixth stage and finally the error of the total propagation delay reduces to less than 4% at the output. Similar error characteristics are found in the case of ramp input excitations.

The consumed CPU time on a personal computer is also listed at the end of Table VIII. Obviously, timing analysis or simulation using the timing models is about 65 times faster than that using SPICE. Moreover, the required memory is also quite small compared with that for SPICE.

5. CONCLUSION AND DISCUSSION

Based upon the large-signal equivalent circuit and s-domain analysis, a general method is proposed to model the signal timing of E/D NMOS logic analytically. Since the E/D NMOS logic has a wide range of device sizes and beta ratios, the device currents are characterized by the least-square curve-fitting technique. This increases the accuracy of the device current calculations and leads to an analytical timing model. In addition, the initial delay, which has a wide range of values even for inverters, is modelled in detail by considering the small device current.

By applying the proposed modelling method to E/D NMOS inverters, their rise time, fall time and delay time have been successfully expressed by analytical equations. Extensive comparisons with SPICE simulation results have shown that the derived general models have a good accuracy for inverters with different device dimensions, inverter sizes, capacitive loads, beta ratios, device parameters and input excitation wave-forms. The required CPU time and memory for the calculation are quite small. Two examples are given to demonstrate the applications of the derived methods in timing analysis of E/D NMOS inverters.

Although the proposed modelling method is only applied to the case of E/D NMOS inverters in this paper, it can be applied to other E/D NMOS gates such as NAND, NOR, etc. Since the timing models derived from the proposed method are analytical, their applications to automatic sizing and optimization of E/D NMOS logic gates are highly expected.

APPENDIX I: NOTATION

Av	voltage gain
$C_{bde(d)i}$	bulk–drain p–n junction capacitance of an enhancement (depletion) n-channel MOSFET in the ith inverter stage
$C_{bse(d)i}$	bulk–source p–n junction capacitance of an enhancement (depletion) n-channel MOSFET in the ith inverter stage
$C_{gbove(d)i}$	gate–bulk overlap capacitance of an enhancement (depletion) n-channel MOSFET in the ith inverter stage
$C_{gdove(d)i}$	gate–drain overlap capacitance of an enhancement (depletion) n-channel MOSFET in the ith inverter stage
$C_{gsove(d)i}$	gate–source overlap capacitance of an enhancement (depletion) n-channel MOSFET in the ith inverter stage

C_L fixed load capacitance of an inverter stage
$C_{oe(d)i}$ channel oxide capacitance of an enhancement (depletion) n-channel MOSFET in the ith inverter stage
$L_{e(d)i}$ mask channel length of an enhancement (depletion) n-channel MOSFET in the ith inverter stage
$L_{effe(d)i}$ effective channel length of an enhancement (depletion) n-channel MOSFET in the ith inverter stage
L_{mask} mask channel length of the MOSFET
S size factor of an E/D NMOS inverter
T_B the time when $V_{o1} = V_B$ in the fall time calculation
$T_{DIF(R)}$ time interval from undershooting valley (overshooting peak) of the rising (falling) input to overshooting peak (undershooting valley) of the falling (rising) output
T_{DIT} total initial delays from the first stage to a referred stage in Table VIII
T_{DT} total propagation delay between the point the input voltage changes to $V_{0\cdot5}$ and the point the output voltage of the last stage changes to $V_{0\cdot5}$ in Table VIII
$T_{PHL(LH)}$ time interval from the rising (falling) input voltage at $V_{0\cdot5}$ to the falling (rising) output voltage at $V_{0\cdot5}$
$T_{F(R)}$ fall (rise) time defined as the interval of a falling signal from $V_{0\cdot9}(V_{0\cdot1})$ to $V_{0\cdot1}(V_{0\cdot9})$
$t_{0\cdot1}$ the time when the output voltage is equal to $V_{0\cdot1}$
V_B the output boundary of the saturation and linear regions for the gate–source-shorted depletion n-channel MOSFET in an inverter
V_{DD} power supply voltage
$V_{dsate(d)}$ saturation voltage of an enhancement (depletion) n-channel MOSFET
V_L voltage level of the logic state '0'
$V_{1x}^{(0)}$ initial voltage in region x of the falling characteristic wave-form
V_{ONi} turn-on voltage of an enhancement n-channel MOSFET in the ith inverter stage
$V_{pf(vr)}$ voltage at overshooting peak (undershooting valley) of the falling (rising) characteristic wave-form
$V_{0\cdot1}$ the voltage $V_L + 0\cdot1(V_{DD} - V_L)$
$V_{0\cdot9}$ the voltage $V_{DD} - 0\cdot1(V_{DD} - V_L)$
$V_{0\cdot5}$ the voltage $\frac{1}{2}(V_{0\cdot1} + V_{0\cdot9})$
$W_{e(d)i}$ mask channel width of an enhancement (depletion) n-channel MOSFET in the ith inverter stage
$W_{effe(d)i}$ effective channel width of an enhancement (depletion) n-channel MOSFET in the ith inverter stage
β_{INV} beta ratio of the E/D NMOS inverter, $\beta_{INV} = (W_e/L_e)/(W_d/L_d)$
α square root of the beta ratio, i.e. $\alpha = \sqrt{\beta_{INV}}$
α_d the ratio L_d/W_d of a depletion n-channel MOSFET
α_e the ratio W_e/L_e of an enhancement n-channel MOSFET
$\Phi_{Fe(d)i}$ Fermi potential of the enhancement (depletion) n-channel MOSFET in the ith inverter stage
τ transition time of an input signal
τ_0 transition time of the characteristic wave-form
$\mu_{se(d)i}$ effective surface mobility of the enhancement (depletion) n-channel MOSFET in the ith inverter stage

APPENDIX II

As seen in Figure 3, substituting equations (1), (4) and (6) in equation (3) and taking the Laplace transformation with the initial values of V_i and V_{o1} as V_{ON1} and $V_{o1}(t_1)$ respectively, we have

$$C_{2n1}\{s(V_i - V_{o1}) - [V_{ON1} - V_{o1}(t_1)]\} + I_{DD}(s) = I_{DE}(s) + C_{out}[sV_{o1} - V_{o1}(t_1)] \tag{16}$$

It should be emphasized here that in finding $I_{DE}(s)$, $V_i^2(t)$ is first calculated from equation (1) and then transformed into the s-domain. Thus $V_i^2(s)$ in $I_{DE}(s)$ is not $V_i(s)V_i(s)$. The solved and factored $V_{o1}(s)$

from equation (16) is

$$V_{o1}(s) = \frac{F_1}{s + 2P_{1r}} + \frac{F_2}{s + P_{1r}} + \frac{F_3}{s + P_f} + \frac{F_4}{s} \tag{17}$$

where

$$F_1 = \frac{A_{2s}D_{1r}^2}{C_T(2P_{1r} - P_f)} \tag{18}$$

$$F_2 = \frac{D_{1r}C_{2n1}P_{1r} + 2A_{2s}D_{1r}D_{2r} + A_{1s}D_{1r}}{C_T(P_{1r} - P_f)} \tag{19}$$

$$F_3 = \frac{1}{C_T}\left((D_{1r} + D_{2r})C_{2n1} + Q_0 - \frac{C_2 - A_{2s}D_{2r}^2 - A_{1s}D_{2r} - C_{1s}}{P_f} - \frac{D_{1r}C_{2n1}P_{1r} + 2A_{2s}D_{1r}D_{2r} + A_{1s}D_{1r}}{P_{1r} - P_f} - \frac{A_{2s}D_{1r}^2}{2P_{1r} - P_f}\right) \tag{20}$$

$$F_4 = \frac{C_2 - A_{2s}D_{2r}^2 - A_{1s}D_{2r} - C_{1s}}{C_T P_f} \tag{21}$$

$$C_T = C_{out} + C_{2n1} \tag{22}$$

$$P_f = -B_2/C_T \tag{23}$$

$$Q_0 = C_T V_{o1}^{(0)} - C_{2n1} V_{i2}^{(0)} \tag{24}$$

REFERENCES

1. E. Seewann, 'Switching speed of MOS inverters', *IEEE J. Solid-State Circuits*, **SC-15**, 246–252 (1980).
2. A. Kanuma, 'CMOS circuit optimization', *Solid-State Electron.*, **26**, 47–58 (1983).
3. M. Horowitz, 'Timing models for MOS circuits', *Ph.D. Dissertation*, Stanford University, 1983.
4. T. Tokuda, K. Okazaki, K. Sakashita, I. Ohkura and T. Enomoto, 'Delay-time modeling for ED MOS logic LSI', *IEEE Trans. Computer-Aided Design*, **CAD-2**, 129–134 (1983).
5. D. Etiemble, V. Adeline, N. H. Duyet and J. C. Ballegeer, 'Micro-computer oriented algorithms for delay evaluation of MOS gates', in *Proc. 21st Design Automation Conf.*, 1984, pp. 358–364.
6. C. Y. Wu and J. S. Hwang, 'Efficient timing models for characteristic waveforms of CMOS logic gates', in *Proc. 27th Midwest Symp. on Circuits and Systems*, 1984, pp. 574–578.
7. R. J. Bayruns, R. L. Johnston, D. L. Fraser, Jr. and S.-C. Fang, 'Delay analysis of Si NMOS Gbit/s logic circuits', *IEEE J. Solid-State Circuits*, **SC-19**, 755–764 (1984).
8. J. A. Pretorius, A. S. Shubat and C. A. T. Salama, 'Analysis and design optimization of domino CMOS logic with application to standard cells', *IEEE J. Solid-State Circuits*, **SC-20**, 523–530 (1985).
9. C.-Y. Wu, J.-S. Hwang, C. Chang and C.-C. Chang, 'An efficient timing model for CMOS combinational logic gates', *IEEE Trans. Computer-Aided Design*, **CAD-4**, 636–650 (1985).
10. J. G. Simmons and G. W. Taylor, 'An analytical treatment of the performance of submicrometer FET logic', *IEEE J. Solid-State Circuits*, **SC-20**, 1242–1251 (1985).
11. D. Auvergne, G. Cambon, D. Deschacht, M. Robert, G. Sagnes and V. Tempier, 'Delay-time evaluation in ED MOS logic LSI', *IEEE J. Solid-State Circuits*, **SC-21**, 337–343 (1986).
12. M. D. Matson and L. A. Glasser, 'Macromodeling and optimization of digital MOS VLSI circuits', *IEEE Trans. Computer-Aided Design*, **CAD-5**, 659–678 (1986).
13. N. Hedenstierna and K. O. Jeppson, 'CMOS circuit speed and buffer optimization', *IEEE Trans. Computer-Aided Design*, **CAD-6**, 270–281 (1987).
14. C. Y. Wu and M. C. Chiau, submitted to *IEEE Trans. CAD Integ. Circ. Syst.*
15. J. K. Ousterhout, 'A switch-level timing verifier for digital MOS VLSI', *IEEE Trans. Computer-Aided Design*, **CAD-4**, 336–349 (1985).
16. N. P. Jouppi, 'TV: An nMOS timing analyzer', in *Proc. 3rd Caltech Conf.*, 1983, pp. 403–410.
17. L. A. Glasser, 'The analog behavior of digital integrated circuits', in *Proc. 18th Design Automation Conf.*, 1981, pp. 603–612.
18. J. Rubinstein, P. Penfield and M. Horowitz, 'Signal delays in *RC* tree networks', *IEEE Trans. Computer-Aided Design*, **CAD-2**, 202–211 (1983).
19. J. L. Wyatt, Jr. and Q. Yu, 'Signal delay in *RC* meshes, trees and lines', in *Proc. 1984 Int. Conf. Computer-Aided Design IEEE*, 1984, pp. 15–17.
20. C. A. Zukowski, 'Bounding enhancements for VLSI circuit simulation', *Ph.D. Dissertation*, MIT, 1985.
21. A. Vladimirescu and S. Liu, 'The simulation of MOS integrated circuits using SPICE2', *Electronic Res. Lab. Memo. UCB/ERL-M80/7*, University of California, Berkeley, 1980.