國立交通大學

電子工程學系 電子工程所碩士班

碩 士 論 文

氨氣電漿處理對複晶矽薄膜電晶體之電特性影響探討

Investigations of NH_3 Plasma Treatment on the Electrical Characteristics of Poly-Si Thin Film Transistors

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摘要

利用複晶矽薄膜電晶體(poly-Si TFTs)製作畫素元件及週邊驅動電路並將它積體化於大面積玻璃基板已成為未來製造主動式矩陣液晶顯示器的趨勢。目前複晶矽薄膜電晶體的異常漏電流是一個待解決且刻不容緩的議題。在本論文中，我們使用氮化矽(Si_3N_4)當作底部閘極之絕緣層，探討經氨氣電漿處理後氫原子與氮原子能夠累積在電晶體的通道內之效應，如此可進一步在汲極接面中填補通道的缺陷數量，可更有效降低元件漏電流之情形。除此之外，我們利用表面電位顯微鏡(KFM)來描述經氨氣電漿處理前後汲極接面能帶圖的變化情形，且此與複晶矽電晶體的異常漏電流有關聯。另一方面，我們也探討了長時間作氨氣電漿處理後，對複晶矽薄膜電晶體電特性之影響。對離子而言要穿透氮化矽薄膜是困難的。因此，此效應造成使用氮化矽與二氧化矽作為複晶矽電晶體的閘極絕緣層之不同行為。

Investigations of NH_3 Plasma Treatment on the Electrical Characteristics of Poly-Si Thin Film Transistors

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Abstract

Utilizing polycrystalline silicon thin-film transistors (poly-Si TFTs) as pixel switching elements and peripheral driver circuits is the future trend for manufacturing active-matrix liquid-crystal displays (AMLCDs). Currently, the anomalous leakage current of poly-Si TFTs is an important issue. In this thesis, we used Si_3N_4 as the insulator of bottom-gated TFTs to investigate the effects of nitrogen and hydrogen radicals accumulated within the channel by NH_3 plasma treatment. A reduction of the leakage current was observed because of effectively defect reduction in the drain junction. Furthermore, variations of the profiles of energy band in the drain junction before and after NH_3 plasma treatment are characterized by Kelvin Probe Force Microscope (KFM), and are used to associate with the anomalous leakage current of poly-Si TFTs. On the other hand, the influence of long-time NH_3 plasma treatment on the electrical characteristics of poly-Si TFTs is studied. It is hard for atomic ions to penetrate into the Si_3N_4 layer. Therefore, the effect results in the different behaviors of poly-Si TFTs with Si_3N_4 and SiO_2 as the gate insulators.

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Contents

Chinese Abstract i
English Abstract ii
Acknowledgment iii
Contents iv
Table Captions vi
Figure Captions vii

Chapter 1 Introduction

1.1 General Background and Motivation 1
1.2 Organization of Thesis 4

Chapter 2 Investigatios of Defect Passivation in the Drain Junction on the Leakage Current of Poly-Si TFTs

2.1 Introduction 6
2.2 Experiment Details
2.2.1 Fabrication of bottom-gated P-type poly-Si TFTs using SPC crystallization ••8
2.2.2 Sample for ESCA/SIMS analysis 11
2.2.3 Sample for Kelvin Probe Force Microscope (KFM) analysis 13
2.3 Results and Discussions
2.3.1 Physical mechanism on the leakage current 14
2.3.2 Hydrogenation effect on high V_{DS} leakage current and physical property analysis 16
2.3.3 Hydrogenation effect on low V_{DS} leakage current and physical property analysis 19
2.4 Summary 21

Table Captions

Table 2.1 The electrical characteristics of bottom-gated poly-Si TFTs before and after NH_3 plasma hydrogenation.

Table 2.2 The electrical characteristics of p-type top-gated poly-Si TFTs using SPC/ELA techniques before and after NH_3 plasma hydrogenation.

Table 2.3 The electrical characteristics of n-type top-gated poly-Si TFTs using SPC/ELA techniques before and after NH_3 plasma hydrogenation.

Figure Captions

Chapter 1

Figure 1.1 The equivalent circuit diagrams of the pixel and its layout in AMLCDs.

Chapter 2

Figure 2.1 Key process flows of p-type bottom-gated poly-Si TFTs.

Figure 2.2 Key process flows of SIMS/ESCA samples.

Figure 2.3 Key process flows of KFM samples.

Figure 2.4 Schematic illustration of the leakage current model in poly-Si TFT.

Figure 2.5 (a) Transfer characteristics for comparison of p-type bottom-gated TFTs using SPC/ELA before and after hydrogenation at V_{DS}= -0.1 V. Sample A (gate oxide), B (gate nitride) treat 360 min, and 300min NH_3 plasma passivation, respectively.

Figure 2.5 (b) Transfer characteristics for comparison of p-type bottom-gated TFTs using SPC/ELA before and after hydrogenation at V_{DS}= -5 V. Sample A (gate oxide), B (gate nitride) treat 360 min, and 300min NH_3 plasma passivation, respectively.

Figure 2.6 (a) Transfer characteristics for comparison of p-type top-gated TFTs using SPC/ELA before and after hydrogenation at V_{DS}= -0.1 V. Both of SPC (gate oxide) and ELA (gate oxide) samples treat 300min NH_3 plasma passivation.

Figure 2.6 (b) Transfer characteristics for comparison of p-type top-gated TFTs using SPC/ELA before and after hydrogenation at V_{DS}= -5 V. Both of SPC (gate oxide) and ELA (gate oxide) samples treat 300min NH_3 plasma passivation.

Figure 2.7 (a) Transfer characteristics for comparison of n-type top-gated TFTs before and after hydrogenation at V_{DS}= 0.1 V. SPC and ELA samples treat 300 min, and 360 min NH_3 plasma passivation, respectively.

Figure 2.7 (b) Transfer characteristics for comparison of n-type top-gated TFTs before

and after hydrogenation at V_{DS}= 5 V. SPC and ELA samples treat 300 min, and 360 min NH_3 plasma passivation, respectively.

Figure 2.8 (a) The SIMS profiles of SiN for sample C (gate dielectric: SiO_2) and D (gate dielectric: Si_3N_4) with 240 min, and 480 min NH_3 plasma treatment.

Figure 2.8 (b) The SIMS profiles of hydrogen concentration for sample C (SiO_2) and D (Si_3N_4) with 240 min, and 480 min NH_3 plasma treatment.

Figure 2.8 (c) The SIMS profiles of oxygen concentration for sample C (SiO_2) and D (Si_3N_4) before and after 240 min, and 480 min NH_3 plasma treatment.

Figure 2.9 (a) The ESCA (XPS) profiles of silicon binding energy for sample C (SiO_2) before and after 120 min, and 480 min NH_3 plasma treatment.

Figure 2.9 (b) The ESCA (XPS) profiles of silicon binding energy for sample D (Si_3N_4) before and after 120 min, and 480 min NH_3 plasma treatment.

Figure 2.10 (a) The variation of surface potential for sample E (P^+/i junction) before NH_3 plasma treatment was measured by KFM.

Figure 2.10 (b) The variation of surface potential for sample E (P^+/i junction) before NH_3 plasma treatment of 6 h was measured by KFM.

Figure 2.11 Schematic illustrations of defect-reduction in the drain junction.

Chapter 3

Figure 3.1 Possible pathways for hydrogen migration from a gaseous source to the active channel region of a top-gated poly-Si TFT structure.

Figure 3.2 Key process flows of the bottom-gated poly-Si TFTs using SPC processes.

Figure 3.3 Key process flows of the top-gated poly-Si TFTs using SPC/ELA processes.

Figure 3.4 Subthreshold Swing determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 10μm and L= 2 μm p-type bottom-gated poly-TFTs

Figure 3.5 (a) Threshold voltage determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 5 μm p-type bottom-gated poly-TFTs.

Figure 3.5 (b) Threshold voltage determined at V_{DS}= -0.1V as function of NH_3 plasma

passivation time for W= 20μm and L= 5 μm p-type top-gated poly-TFTs.

Figure 3.5 (c) Threshold voltage determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 10μm n-type poly-TFTs.

Figure 3.6 (a) Mobility determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 10μm and L= 2 μm p-type bottom-gated poly-TFTs.

Figure 3.6 (b) Mobility determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 10 μm p-type top-gated poly-TFTs.

Figure 3.6 (c) Mobility determined at V_{DS}= 0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 5 μm n-type poly-TFTs.

Figure 3.7 (a) The leakage currrent determined at V_{DS}= -5V as function of NH_3 plasma passivation time for W= 10μm and L= 2 μm p-type bottom-gated poly-TFTs.

Figure 3.7 (b) The leakage currrent determined at V_{DS}= -5V as function of NH_3 plasma passivation time for W= 20μm and L= 10 μm p-type top-gated poly-TFTs.

Figure 3.8 (a) Effective trap density determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 5 μm p-type bottom-gated poly-TFTs.

Figure 3.8 (b) Effective trap density determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 2 μm p-type top-gated poly-TFTs.

Chapter 1

Introduction

1.1 General Background and Motivation

In 1962, the first thin-film transistors (TFTs) were proposed by Weimer [1.1]. Subsequently, in 1966 Fa et al. first fabricated polycrystalline silicon thin-film transistors (poly-Si TFTs) [1.2]. Meanwhile, there had been many reports investigating Poly-Si TFTs, such as TFT conduction mechanisms, device structures, fabrication processes and reliability. In 1983, the first practical application of poly-Si TFTs to liquid-crystal displays (LCDs) was announced for full-color pocket TVs [1.3], and commercialized in 1984 as the world's first. Rencently, the polysilicon process has been widely developed to produce several kinds of products such as notebook [1.4], cell phone, personal digital assistance (PDA), high-density static random access memories (SRAMs) [1-5], active-matrix organic light emitting displays (AMOLEDs) and active-matrix LCDs (AMLCDs)[1-6]-[1-8], etc. Among them, AMLCDs are being developed due to the possibilities of integrating peripheral driver circuits of poly-Si TFTs. Fig. 1-1 shows a circuit diagram of AMLCDs.

Poly-Si TFTs are fabricated on large area glass substrates are important

pixel-switching devices of AMLCDs. Their electrical characteristics are poor than that of single-crystal silicon MOSFETs. Because there are many trap states existing inside the active channel. These defects at the grain boundaries as well as inside the grains are well known to degrade device performance [1-9]-[1-10]. In addition to area quartz substrates, large area glass substrates must be produced in the low temperature processes (LTP) below 575℃ for low cost requirements. Unlike early days, poly-Si TFTs were fabricated by high temperature processes (HTP) above 900℃ for high carrier mobility.

Owing to the poor thermal tolerance of low cost glass substrates, many techniques about crystallization of amorphous silicon (α-Si) in low temperature have been proposed. Generally speaking, there are three crystallization methods to forming poly-Si channel layer[1-11]. The first method is called solid phase crystallization (SPC) [1-12]-[1-15]. SPC is an effective method for forming poly-Si films with uniform and large grain sizes, but many crystalline defects appear at grain boundaries as well as inside the grains, such as twins and stacking faults. Additionally, SPC needs long time (about 20 hrs or longer) [1-14] to finish the crystallization of amorphous silicon by using low temperature (600℃) furnace, so there is a trade-off between performance and throughput. The second method is called, metal-induced lateral crystallization (MILC) [1-16]-[1-19],

which is a method for shortening crystallization time and reducing crystallization temperature to less than 550℃. For example, nickel (Ni)-induced crystallization obtained needle-shaped single crystal 1μm long and 0.1μm wide [1-17]. Because of the excellent crystallinity of these needles, the on-state current (I_{on}) is further improved. In terms of off state current (I_{off}) and device reliability, MILC may lead to degrade device performance due to metal impurities remaining in the active channel. The third method is, excimer laser annealing (ELA)[1-20]-[1-23], which recently is a promising candidate for producing high performance of LTPS TFTs. Amorphous silicon films are heated to the melting point within several tens of nanoseconds by excimer laser irradiation, and then are transformed into polycrystalline Silicon films without thermally damaging the glass substrates. ELA processes create smaller grain size than SPC processes, but there are few intragrain defects within the poly-Si grains. Therefore, the electrical characteristics of ELA poly-Si TFTs are much better than that of SPC poly-Si TFTs, such as over 7 orders magnitude of the on/off current ratio, high field-effect mobilities, low subthreshold swing (SS)[1-24]. However it is hard to avoid the formation of hillocks and protrusions during excimer laser crystallization, resulting in a rough surface of poly-Si films and degrading the reliability of ELA poly-Si TFTs. This is the reasons why poly-Si TFTs cannot be scaled down [1-25].

Many reports have shown that hydrogen (H_2) and ammonia (NH_3) plasma passivation not only compensated defects at the grain boundaries as well as inside the grains, but also reduced trap densities at the gate-insulator/poly-Si channel interfaces [1-26]-[1-28]. The atomic hydrogen can passivate dangling bonds in the poly-Si channel, remarkably improving device characteristics. However, NH_3 plasma treatment can further improve device characteristics as compared with H_2 plasma treatment [1-29]. In addition, pure oxygen (O_2) and nitrogen (N_2) plasma passivation are other effective techniques to improve the characteristics of the poly-Si TFTs. In this study, we will discuss effects of NH_3 plasma passivation time on device performance, including the top and bottom gated poly-Si TFTs fabricated using SPC and ELA technique.

1.2 Organization of This Thesis:

In this thesis, we concentrate our efforts on influences of NH_3 plasma passivation on the electrical characteristics of p-type poly-Si thin film transistors. Chapter 1 describes the background and motivation. In chapter 2, the leakage current models are introduced and the correlations between the leakage current at the high/low fields and hydrogenation are investigated. We also verified physical properties from SIMS, KFM, and ESCA.

In chapter 3, bottom-gated poly-Si TFTs are fabricated by SPC techniques and

top-gated ones also fabricated by SPC and ELA techniques. We studied the NH_3-plasm-passivation rates on the device parameters, including V_{th}, SS, μ_{FE}, I_{off}, and N_t (effective trap density). We also investigated dependences of various passivation times on the deep and tail states. At last, in chapter 4, a conclusion is given for this thesis, and some future works extended from our investigation are proposed.

Chapter 2

Investigations of Defect Passivation in the Drain Junction on the Leakage current of Poly-Si TFTs

2.1 Introduction

Poly-Si TFTs play an important role in large-area electronics. This is due to the possibility of fabricating both NMOS and PMOS devices. In addition to being capable of driving high current [2-1], compared to the amorphous silicon TFTs, poly-Si TFTs offers the flexibility of integrating peripheral driver circuits on glass substrates to interface with AMLCDs. Despite this achievement, the leakage current still imposes a limit on the duration of video information that remains on a pixel before it must be refreshed. In most applications, a major problem is the anomalous leakage current of poly-Si TFTs. From pervious studies [2-2], the dominate mechanism of the leakage current is thermionic emission when devices are biased at low drain fields (V_{DS}= -0.1V). Thermionic field emission dominates device leakage current at moderately high drain fields. At high drain bias (V_{DS} > -5V), tunneling was observed to be responsible for leakage current mechanism. At low drain fields, the leakage current depends on the trap

distribution and on the fabrication process of the active film. At high drain fields, the leakage current becomes almost independent of material quality [2-3]. In terms of high temperature effects, thermionic enhanced emission (Poole-Frenkel effect) and TAT (trap assisted tunneling) play a major role in the whole range of applied gate biases. At room temperature, all the above effects contribute to the leakage current.

In fact, the leakage current is exponentially dependent on the electric field of the drain junction and directly proportional to the grain-boundary trap density of the drain junction. A lightly doped drain (LDD) structure can effectively reduce the lateral electric field in the drain junction both in steady-state and in transient conditions [2-4]-[2-6], but LDD structure introduces extra source/drain series resistances degrading the on-state current and the speed of devices. In general, the leakage current decreases as the length of LDD increases. On the contrary, an active-gate structure only reduces the lateral electric field in transient condition. Furthermore, the peak of electric field under the typical timing conditions is substantially larger than that in steady-state conditions. A CMTFT (conductivity modulated TFT) shows lower leakage current than conventional offset drain TFT without current pinching problems. This result is contributed to introduce a larger channel series resistance, resulting in a reduction in the lateral electric field at the channel/offset drain junction when a CMTFT is turned off

[2-7]. As the drain voltage is further raised, the leakage current of the CMTFT shows higher current than conventional poly-Si TFT. This increase in leakage current is basically due to the turn-on the $P^+/i/N^+$ diode. It was reported that a significant reduction in leakage current in the thick drain structure is obtained compared to a thin drain structure [2-8]. This reduction in the leakage current is due to the reduction of the lateral electric field in the poly-Si TFT with thicker junction depth. However, thicker film devices have the disadvantages of larger grain-boundary trap density, lower mobility, and lower on-state current compared to thinner film devices [2-9]. For thin active layers [2-10], there is insufficient active layer thickness for complete band bending, resulting in less charges being trapped and hence an improvement in the density of state. This decrease in leakage current is due to the easier formation of a p-channel, which suppresses the generation volume more effectively.

In this chapter, we try to understand how the defect reduction in the drain junction affects the leakage current of poly-Si TFTs. Variations of the drain junction before and after NH_3 plasma treatment are characterized by Kelvin Probe Force Microscope (KFM).

2.2 Experiment Details

2.2.1 Fabrication of bottom-gated P-type poly-Si TFTs using SPC

crystallization

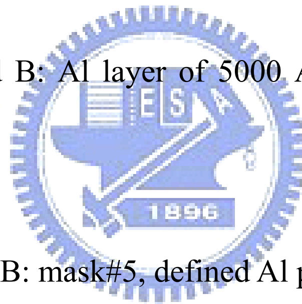
Two types of samples were fabricated called Sample A (SiO_2) and Sample B (Si_3N_4). The key process flows as shown in Fig. 2.1. A 1.5μm thermal Oxide was grown on bare Si wafer as a buffer layer. Then a phosphorous-doped α-Si of 1000Å was deposited at 550℃ in a low pressure chemical vapor deposition (LPCVD, vertical furnace) system. The phosphorous-doped α-Si film was annealed at 900℃ for 2 h and then patterned. A 813Å thick tetraethyl orthosilicate (TEOS) oxide layer was deposited by plasma enhance chemical vapor deposition (PECVD) system as a gate dielectric of sample A. A 1021Å thick nitride (Si_3N_4) layer was deposited by LPCVD system as a gate dielectric of sample B. A 91 nm α-Si layers were deposited as the active layers of sample A and B. Ion implantation was then performed to form the regions of source and drain using photoresists (P.R) as hard mask, afterward, furnace annealing at 600℃ for 24 h in N_2 ambient was carried out to recrystallize the Si films. After defining the active regions, a 3000Å passivation TEOS SiO_2 layer was deposited by LPCVD system. Finally, the contact holes were opened and the Al films were deposited and then defined. The detail process flows are listed as follow:

1. Initial RCA clean

2. 1.5μm thermal Oxide: wet oxidation, 978℃.

3. A phosphorous-doped α-Si layer of 1000Å was deposited *in situ* : vertical furnace, decomposed SiH_4 gases, 550℃.
4. Thermal annealing at 900℃ for 2 h.
5. Mask #1: Gate pattern was defined and etched by anisotropic plasma etching.
6. P.R striped and side-wall polymers were removed by standard clean Ⅱ (SC-Ⅱ).
7. RCA cleaning without final HF-dip.
8. Sample A: A TEOS oxide (SiO_2)layer of 813Å was deposited by PECVD at 350℃ as gate insulator.
9. Sample B: A nitride (Si_3N_4) layer of 1021Å was deposited by LPCVD at 600℃ as gate insulator.
10. Sample A and B: amorphous silicon layer of 910 Å were deposited by LPCVD at 550℃.
11. Sample A and B: mask #2, photoresists were defined for ion implantation.
12. Sample A and B: ion implantation, B, 15KeV, 1×10^{16} cm^{-2}.
13. Sample A and B :Photoresists were striped.
14. Sample A and B: post-implantation annealing, 600℃, 24 hrs.

15. Sample A and B: mask #3, active region were defined and etched by Poly-RIE.
16. Sample A and B : Photoresists were striped and RCA cleaning without final HF-dip.
17. Sample A and B: TEOS oxide passivation layers of 3000Å were deposited by LPCVD at 695℃.
18. Sample A and B: mask#4, opened contact hole by BOE wet etching.
19. Sample A and B: Photoresists were striped and dipped HF
20. Sample A and B: Al layer of 5000 Å were sputtered by thermal coater as electrodes.
21. Sample A and B: mask#5, defined Al pad.
22. Sample A and B: Al sintering, 400℃, 30min.



2.2.2 Sample for ESCA/SIMS analysis

Two types of samples were fabricated called Sample C (SiO_2) and Sample D (Si_3N_4). The key process flows as shown in Fig. 2.3. A 1.5μm thermal Oxide was grown on the bare Si wafer as a buffer layer. Then a 1000Å α-Si was deposited at 550℃ in a LPCVD (vertical furnace) system. Sample C was deposited a 1000Å TEOS oxide by PECVD system. Sample D was deposited a 1021Å Si_3N_4 layer by LPCVD system. Both

sample C and D were deposited the 500Å amorphous Si layer by LPCVD system. Finally, a passivation TEOS SiO_2 of 3000Å was deposited by LPCVD system. After NH_3 plasma treatment for 4, and 8 h, the passivation oxides of both samples were removed by buffered oxide etching (BOE) solutions.

The detail process flow is listed as flow:

1. Initial RCA clean
2. 1.5μm thermal Oxide: wet oxidation, 978℃.
3. A α-Si layer of 1000Å was deposited: vertical furnace, decomposition of SiH_4 gases, 550℃.

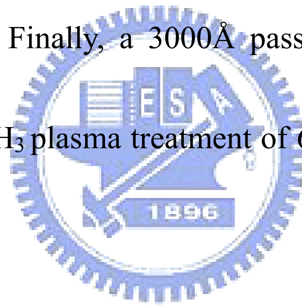
4. Sample C: A TEOS oxide (SiO_2) layer of 1000Å was deposited by LPCVD at 600℃.
5. Sample D: A nitride (Si_3N_4) layer of 1021Å was deposited by LPCVD at 600℃.
6. Sample C and D: A amorphous silicon layer of 500 Å were deposited by LPCVD at 550℃.
7. Sample C and D: RCA cleaning without final HF-dip.
8. Sample C and D: A TEOS oxide (SiO_2) passivation layer of 3000Å was deposited by LPCVD at 695℃.

9. Sample C and D: NH_3 plasma treatment with various time.

10. Sample C and D: A passivation layer (SiO_2) was removed by BOE.

2.2.3 Sample for Kelvin Probe Force Microscope (KFM) analysis

Two types of samples were fabricated called Sample E (boron-doped). The key process flows as shown in Fig. 2.3. A 1.5μm thermal oxide was grown on the bare Si wafer as a buffer layer. A α-Si of 1000Å was then deposited at 550℃ in a LPCVD (vertical furnace) system. Sample E was implanted by born ions at an energy of 15KeV and dose of 1E16 cm^{-2}. Finally, a 3000Å passivation TEOS SiO_2 was deposited by LPCVD system. After NH_3 plasma treatment of 6 h, the passivation oxide was removed by BOE solutions.



The detail process flow is listed as flow:

1. Initial RCA clean
2. 1.5 μm thermal Oxide: wet oxidation, 1050℃.
3. A α-Si layer of 1000Å was deposited: LPCVD, decomposition of SiH_4 gases, 550℃.
4. Sample E: ion implantation, B, dose = 1E16 cm^{-2}, 15 Kev.
5. RCA cleaning.
6. Post-implantation annealing, 600℃, 24hr.

7. A TEOS oxide (SiO_2) passivation layer of 3000Å was deposited by LPCVD at 695℃.

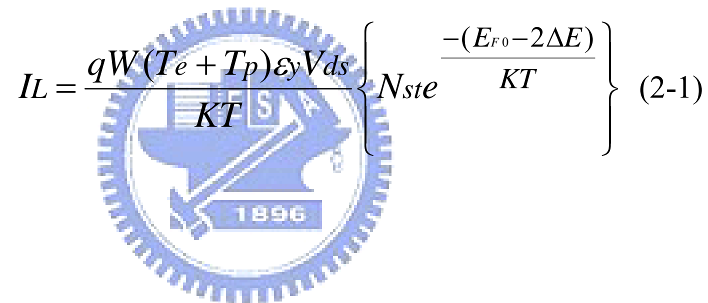
8. NH_3 plasma treatment of 6 h: 700sccm, 200W.

9. A passivation layer (SiO_2) was removed by BOE.

2.3 Results and Discussions:

2.3.1 Physical mechanism on the leakage current

For a thin film transistor, the leakage current can be expressed as [2-2]



$$I_L = \frac{qW(T_e + T_p)\varepsilon_y V_{ds}}{KT}\left\{ N_{st} e^{\frac{-(E_{F0}-2\Delta E)}{KT}} \right\} \quad (2\text{-}1)$$

where,

q is the electron charge.

W is the channel width.

k is the Boltzman’s constant.

T is the temperature.

Te is the electron tunneling probability.

Tp is the hole tunneling probability.

ε_y is a lateral electric field in the drain depletion region.

N_{st} is the trap density (/cm^3/eV)

E_{F0} is approximately half the bandgap.

ΔE is the drain grain boundary traps with respect to midgap.

The leakage current model: as electrons from valence band are captured by the traps via any of the three processes (i.e., thermionic emission, thermionic field emission, and tunneling), the holes generated are swept to the drain and they result in leakage current. For the trap to remain active, it must emit the captured electrons to the conduction band. Those electrons accumulate in the channel, and increase electrical potential with respect to source (assume source is grounded). As a result, these electrons flow into the source where they recombine with holes supplied by the ground. In equation (2-1), it can effectively reduce the leakage current by decreasing lateral electric field and effective grain boundary trap density at the channel/drain junction region. At a low drain field (-0.1V), the lowest activation energy is about $E_g/2$, thermionic emission is the dominate leakage mechanism at low field. This is the process step (1) in Fig. 2.4. As the drain bias increases (more negative), the drain depletion field increases and activation energy decreases. This suggests that the high field in the drain depletion region has reduced the barrier. As such, the dominant leakage current mechanism is thermionic field emission and is represented by process (2) in Fig. 2.4. Further increase of the drain bias put activation energy below 0.1eV. Since $Ea < 0.1eV$ present almost no barrier to the carrier

motion, the dominant leakage mechanism is pure tunneling.

2.3.2 Hydrogenation effect on high-V_{DS} leakage current and physical property analysis

Fig. 2.5 (a) and (b) shows the transfer characteristics for comparison of bottom-gated poly-Si TFTs with SPC/ELA before and after NH_3 plasma passivation at V_{DS}= -0.1, and -5 V, respectively. After hydrogenation, the electrical characteristics of the three types of the poly-Si TFTs have been improved as listed in table 2.1. The minimum leakage current of sample A is decreased from 260 pA to 0.2 pA. Sample B is decreased from 196 pA to 0.15 pA. One can see that sample B after NH_3 plasma passivation has a lower leakage current than that of sample A at high lateral electric fields (V_{DS}= -5 V) as shown in Fig. 2.5 (b). This reduction in the leakage current is ascribed to defect reduction in the drain junction because nitrogen and hydrogen radicals can effectively accumulate at the Si_3N_4/channel interface as shown in Fig. 2.8 (a) and (b). In Fig. 2.8 (a), the peak value of nitrogen concentration in sample D (gate dielectric: Si_3N_4) is increased from 1.61×10^{18} to 4.38×10^{21} after NH_3 plasma treatment of 8 h. It is obviously that [SiN] of sample D is remarkably larger than that of sample C (gate dielectric: SiO_2) near the dielectric/channel interface. It is also interesting that the concentrations of SiN at Si_3N_4 layers are unchanged after NH_3 plasma treatment of 4 h

and 8 h. Inversely, the concentration of SiN at SiO_2 layers increases as comparing to sample D of 4 h and 8 h. In Fig 2.8 (b), we observed that the hydrogen concentration of sample D had a larger value than that of sample C after NH_3 plasma treatment of 8 h, especially at the gate dielectric/channel interface. It is also interesting that [H] of sample D with NH_3 plasma treatment of 4 h is about the same in the nitride layer as compared to NH_3 plasma treatment of 8 h. Contrary to sample C, [H] with NH_3 plasma treatment of 8 h is significantly increased in the oxide layer as compared that with NH_3 plasma treatment of 4 h. This result implies that the nitride layer can effectively prevent nitrogen and hydrogen atoms from downward diffusing. Conversely, nitrogen and hydrogen atoms can diffuse into the oxide layer through the channel region via hydrogenation processes. As mentioned above, the numbers of hydrogen/nitrogen atoms in the channel region with Si_3N_4 as gate insulator is larger than that with TEOS SiO_2 as gate insulator. Therefore, a bottom-gated poly-Si TFT with Si_3N_4 as gate insulator can further reduce defect states in the drain junction as well as at the channel/dielectric interface, and obtains lower leakage current at near zero gate bias. In KFM analysis, the difference of the surface potential between P^+/i is 40 mV before NH_3 plasma treatment as shown in Fig. 2.10. After NH_3 plasma treatment of 6 h, it becomes 186 mV. As a result, the surface potential increases the magnitude of 146 mV resulting from NH_3

plasma treatment. In Fig. 2.11, the rises in the surface potential lead to increase the depletion width in the drain junction. This is attributed to that defect states before NH_3 passivation can not generate carriers in the depletion region. After NH_3 passivation, the passivated defects have abilities to generate active carriers resulting in extra depletion width. This result make further reduce the leakage current due to defect reduction in the drain junction. Hence, we proposed "defect-reduction controlled regime" in Fig. 2.5 (b). At a high drain field, the leakage current is dominated by tunneling mechanism and independent of the defect reduction. In other words, sample B and A have similar magnitude of the leakage current at high drain fields. We proposed "tunneling-controlled regime". However, grain-boundary defects results in deep states affecting the leakage current. In other words, fewer deep states cause lower leakage current. The similar phenomena with respect to the off-sate current were also found in Fig. 2.6 (b) and 2.7 (b). The electrical characteristics of p- and n-type top-gated poly-Si TFTs are respectively listed in Table 2.2 and 2.3.

In comparison of the on-state currents (Fig. 2.5 (b)), Sample A has larger turn-on current than sample B after hydrogenation. The on-state current is dominated by donor-like tail states originated from strained bonds at the channel/dielectric interface. This is well known that stresses at the Si_3N_4/poly-Si interface are larger than the

SiO_2/poly-Si interface due to larger differences in thermal expansion coefficient between SiO_2 and poly-Si. Although the larger number of hydrogen and nitrogen atoms are blocked at the Si_3N_4/poly-Si interface (Fig. 2.8 (a), (b)) after NH_3 plasma treatments, most of these atoms can easily passivate deep states originating from dangling bonds at the channel/dielectric interface. For this reason, the number of donor-like tail states at Si_3N_4/poly-Si interface after NH_3 hydrogenation is still larger than at the SiO_2/poly-Si interface. Therefore, the on-state current of sample A after NH_3 hydrogenation is larger than that of sample B. In terms of the degree of the improved on-state current, Sample B (gate nitride) is higher than sample A (gate oxide) due to the larger number of hydrogen and nitrogen atoms are blocked at the Si_3N_4/poly-Si interface. For the conventional TFT using ELA techniques (Fig. 2.6 (b) and 2.7 (b)), the on-state current is almost same before and after NH_3 plasma passivation. This slightly improvement is attributed to very small number of the donor-like tail states (*i.e.*, in-grain defects) exist at the SiO_2/poly-Si interface as well as within the channel.

2.3.3 Hydrogenation effect on low-V_{DS} leakage current and physical property analysis

In a p-channel device, the leakage current at low V_{DS} depends on the total density of states at midgap and on the density of states in the upper half of the gap [2-10]. For a

p-type TFT in low field regime, the leakage current of three types of samples all decrease after NH_3 plasma passivation (Fig. 2.5 (a)). At such a low drain field, we found that the leakage current of the bottom-gated TFT (Fig. 2.5(a)) after hydrogenation is slightly decrease as compared to that of the top-gated TFT (Fig. 2.6(a) and Fig.2.7 (a)). This result suggests that the passivation path of the bottom-gated device is shorter than the top-gated device. For the bottom-gated TFTs, the number of the tail states within the channel can be further passivated by hydrogen and nitrogen atoms as compared to the top-gated TFTs. Therefore, the bottom-gated TFT still has a slightly reduction of the leakage current at a low drain field after NH_3 hydrogenation. On the Contrary to top-gated TFTs, the leakage currents before and after NH3 hydrogenation are still independent of V_{GS} as shown in Fig. 2.6 (a) and 2.7 (a). From previous works [2-7], thicker films produced by SPC or direct poly-Si deposition are known to exhibit a minimum (at $V_{GS,\,min}$) in their transfer characteristic for low V_{DS}, and for $V_{GS} < V_{GS,\,min}$ the current becomes independent of V_{GS}. In these conditions, the contribution of thermally-generated carriers becomes dominant. As a result, we suggest that the leakage currents of bottom-gated TFTs at a low drain field still depend on defect reduction, not independent of V_{GS}.

In an undoped polysilicon TFT, the flat band voltage (V_{FB}) is essentially the gate

voltage at which the induced charges equal the trapped charges [2-11]. In Fig. 2.5 (b) and 2.6 (b), V_{FB} began at more negative gate bias before hydrogenation and then moved toward near zero gate bias. It shown that there is a larger density of traps at the dielectric/channel interface as well as within the channel, and a more negative gate bias induces larger concentration of the holes filling with the larger traps before hydrogenation. After hydrogenation, V_{FB} is approximately at zero gate bias, indicating that the reduction of trap density can be completely filled with smaller concentration of holes.

Fig. 2.7 (a) and (b) show the transfer characteristics for comparison of n-type top-gated poly-Si TFTs using SPC/ELA before and after NH_3 plasma passivation at V_{DS}= 0.1, and 5 V, respectively. In a low drain field, the leakage current before and after NH_3 hydrogenation is independent of V_{GS} and density of states. Contrary to a high drain field, the leakage current before and after NH_3 plasma passivation is dependent of V_{GS} and density of states. At a lower field, the leakage current is dominated by thermionic emission, while thermionic field emission and tunneling become dominant at a higher field.

2.4 Summary

Thermionic emission is the dominate leakage current mechanism at a low drain

field (V_{DS}= -0.1V) while thermionic field emission dominate at moderately high drain field. At high drain bias (V_{DS}> -5 V), tunneling was observed to be responsible for leakage current mechanism. We can effectively reduce the leakage current by decreasing lateral electric field and effective grain-boundary trap states in the drain junction, especially in the deep states.

From SIMS analysis, we found that a Si_3N_4 layer as the gate insulator of bottom-gated TFTs effectively attains an accumulation of hydrogen and hydrogen atoms within the channel region after NH_3 plasma treatment as compared to a SiO_2 layer as the gate insulator of bottom-gated TFTs, indicating a reduction of more deep states in the channel region. As a result, Si_3N_4 is a diffusion barrier for nitrogen and hydrogen radicals. After NH_3 plasma treatment, we also verified that the increasing depletion width results from raising the surface potential by using KFM analysis. The increasing depletion width implies defect reduction in the drain junction and causes further reduction of the leakage current. Hence, we propose "defect-reduction controlled regime". When the leakage current approaches to together, we call "tunneling controlled regime". After NH_3 plasma hydrogenation, the p-type bottom-gated TFT with Si_3N_4 dielectric not only further reduces the leakage current at a high drain field (V_{DS}= -5V) as compared to the TFT with SiO_2 dielectric but also slightly decreases at a low drain field.

The leakage current strongly depends on the number of the acceptor-like deep states at positive gate bias. We also found that the leakage current of the bottom-gated TFT has a slightly reduction at a low field after NH_3 plasma passivation. Contrary to the top-gated TFT, the leakage current is independent of V_{GS} after NH_3 plasma passivation. We suggest that the bottom-gated TFT has a shorter diffusing path of hydrogen diffusion than the top-gated one, and obtains the higher degree of reducing deep states. Therefore, the bottom-gated TFT still has a slightly reduction of the leakage current at a low drain field after hydrogenation.

Chapter 3

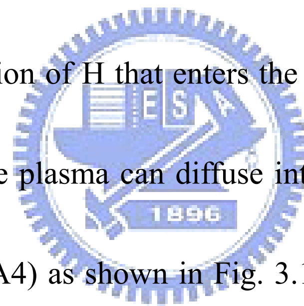
Influence of Long-time NH_3 Plasma Treatment on the Electrical Characteristics of Poly-Si TFTs

3.1 Introduction

Poly-Si TFTs are widely used in various applications, and will figure prominently in future high-resolution, high-performance flat-pannel display (FPD) technology [3-1]. Poly-Si TFTs as peripheral driver circuits can be directly integrated onto AMLCD substrates. High-performance poly-Si TFTs are capable of improving display reliability by reducing connections to external chips and make manufacturing costs down by reducing externally required chips. In poly-Si TFTs, however, grain boundaries and intragrain defects bring a profound influence on device characteristics and carrier transport.

It is well known that hydrogenation tends to terminate the grain-boundary dangling bonds with hydrogen, remarkably improving the electrical characteristics of poly-Si TFTs, especially in leakage current (I_{off}), subthreshold swing (SS), threshold voltage (V_{th}) [3-2]. Hydrogenation is a well-accepted technique for reducing trap state densities

at SiO_2/poly-Si interface and grain boundaries of the poly-Si channel films, thereby lowering the grain boundaries potential barrier. Hydrogenation by plasma discharge [3-3]-[3-4], by the deposition of hydrogen-containing nitride film [3-5], or by H^+ ion implantation [3-6] have been reported to improve the performance of poly-Si TFTs. In general, the activation energy for diffusion of an impurity along a grain boundary is lower than that for diffusion within the lattice [3-7]. Consequently, grain boundaries could be expected to act as "diffusion pipes" for the rapid migration of hydrogen into polycrystalline silicon. It is further shown that an oxide overlayer significantly attenuates the concentration of H that enters the poly-Si from a plasma discharge. As a result, hydrogen from the plasma can diffuse into the active channel region by several possible pathways (A1~A4) as shown in Fig. 3.1. High diffusion rates in poly-Si grain boundaries prefer path A1 and A2 while a reduced diffusion favors A2 and A4. However, it had been shown that the hydrogenated poly-Si TFTs suffer a low hot-carrier endurance [3-8] [3-9] and a low thermal stability. Hydrogen passivation is stable at 150℃, channel hot-electron stress at high temperature appears to create additional grain-boundary traps, by breaking Si-H bonds at grain boundaries of the drain junction. The acceptor-type fast interface states are generated by hot-electrons, which break Si-H bounds at the interface as well as at the grain boundary. In order to meet the requirement



of integrating fabrication of the entire display circuitry (i.e., LCD's driver and active matrix elements) into glass substrates, the device parameter of the poly-Si TFTs must be optimized.

Choi *et al*. exhibited that the grain boundary and in-grain defects result in the continuous distribution of trap states in the forbidden bandgap [3-10]. The deep states, which originate from the dangling bonds in grain boundaries, influence the threshold voltage (V_{th}) and the subthreshold swing (SS). The tail states, which originate from the in-grain defects, affect the field-effect mobility (μ_{FE}) and the leakage current (I_{off}). Because of the density of the in-grain defects in the low temperature SPC poly-Si TFTs is very high, it takes a long time to accumulate the sufficient concentration of hydrogen to eliminate the trap states, especially in tail states.

However, many reports have been proposed that NH_3 plasma and H_2 plasma treatment both can effectively promote the performance of poly-Si TFTs, but further improvement in NH_3 plasma passivation [3-11]. Poly-Si TFTs after NH_3 plasma treatment obtain better device performances, including a dearease of the leakage current (I_{off}), an increase of the field-effect mobility (μ_{FE}), a decline of the subthreshold swing (SS) and an improvement on/off current ratio (I_{on}/I_{off}) than those after H_2 plasma treatment. These further improvements are attributed to the atomic hydrogen passivating

the dangling bonds and in-grain defects, to the nitrogen piling up at SiO_2/channel interface, and to the strong Si-N bond terminating the dangling bonds at the grain boundaries as well as inside the grain. In this chapter, we investigate the influence of long-time NH_3 plasma treatment on the electrical characteristics of poly-si TFTs.

3.2 Experiments for Long-time NH_3 Plasma Treatment

3.2.1 Fabrication of bottom-gated poly-Si TFTs using SPC processes

Two types of samples were fabricated called Sample A (SiO_2) and Sample B (Si_3N_4). A 1.5 μm thermal Oxide was grown on bare Si wafer as a buffer layer. Then a phosphorous-doped α-Si of 1000Å was deposited at 550 ℃ in LPCVD system. The phosphorous-doped α-Si film was annealed at 900 ℃ for 2 h and then patterned. A 813Å thick TEOS oxide was deposited by PECVD system as a gate dielectric of sample A. A 1021Å thick Si_3N_4 layer was deposited by LPCVD system as a gate dielectric of sample B. A 910 Å α-Si layers were deposited as the active layers of sample A and B. After defining photoresists, sample A and B was implanted (Boron, 15 KeV, 1×10^{16} cm^{-2}) to form the source and drain, and then furnace annealing at 600℃ for 24 h in N_2 ambient was carried out to recrystallize the Si films. After defining the active regions, a 3000Å passivation TEOS SiO_2 was deposited by LPCVD system. Finally, the contact holes were opened and the Al films were deposited and then defined. NH_3 plasma

passivation was performed in a parallel-plate plasma reactor at 350℃ with a RF power of 200 W, 300 mTorr, and 700 sccm. As mentioned above, key process flows are illustrated in Fig. 3.2.

3.2.2 Fabrication of top-gated poly-Si TFTs using SPC/ELA processes

The poly-Si TFTs were fabricated on the thermally oxidized silicon wafer. A 1000 Å thick α-Si was deposited at 550 ℃ by LPCVD, and then sample D and E were annealed at 600 ℃ for 24 hr in N_2 ambient. Sample F and G were crystallized into poly-Si films by a KrF excimer laser irradiation in vacuum (~10-3 Torr) at room temperature with an energy density of 390 mJ/cm^2. After defining the active islands, a 1000Å TEOS SiO_2 was deposited by the LPCVD. Another 3000 Å of thick amorphous Si was deposited at 550 ℃ by LPCVD system and patterned as gate electrodes. A self-align ion implantation was performed to form source, drain, and gate electrodes (for sample D and F: phosphorus, 35 KeV, 1×10^{16} cm^{-2}; for sample E and G: Boron, 15 KeV, 1×10^{16} cm^{-2}). After post-implantation annealing, a 3000Å passivation TEOS SiO_2 was deposited by LPCVD system. Finally, the contact holes were opened and the Al films were deposited and then defined. NH_3 plasma passivation was performed in a parallel-plate plasma reactor at 350℃ with a RF power of 200 W, 300 mTorr, and 700 sccm. As mentioned above, key process flows are illustrated in Fig. 3.3.

3.3 Results and Discussions

3.3.1 Hydrogenation effects on the threshold voltage and subthreshold swing

The threshold voltage is defined as the gate voltage at a fixed drain current $I_{DS} = I_{DN} \times (W/L)$, where I_{DN} is a normalized drain current [3-12]. V_{th} is affected by the total number of active trap states between the bulk Fermi-level and the surface Fermi-level position. The bulk Fermi level is slightly above midgap since undoped polysilicon is slightly n-type. For conventional top-gated poly-Si, V_{th} and SS are improved without an obvious hydrogenation onset period. These two parameters are more sensitive to the deep states near midgap [3-12]. In terms of the passivation rate in SS (Fig. 3.4), both of SiO_2 and Si_3N_4 samples reach the saturation region after NH_3 plasma passivation of 30 min, indicating NH_3 plasma passivated the deep states is faster than tail states. From SIMS analysis, the concentration of H and N atoms for Si_3N_4 dielectric inside the channel is comparable to that of SiO_2. Hence, SS for Si_3N_4 dielectric can achieve saturation region as soon as SiO_2 dielectric due to pre-dominating by the deep states within the channel. Here the effects of the interface states were assumed to be negligible because of the much higher bulk defect density presenting in polysilicon. It is also noted that poly-Si TFTs with Si_3N_4 dielectrics have larger saturated value of SS than that of

SiO_2 dielectrics (Fig. 3.4). After most of deep states within the channel are compensated, the saturating SS is dominated by the number of dangling bonds at the insulator/channel interface. This is well known that Si_3N_4 has larger interface states than SiO_2 due to larger stresses existing in the Si_3N_4/poly-Si interfacee.

For p-type bottom-gated TFTs using SPC processes, V_{th} (passivation curves of SiO_2 dielectric) reach saturations at 90 min as shown in Fig. 3.5 (a). It implies that the numbers of deep states in the bulk oxide are compensated by H atoms, leading to a faster passivation rate. Contrary to use Si_3N_4 dielectrics, V_{th} is continuously improved by NH_3 plasma treatment without saturation. This result is consistent with SIMS analysis. The significantly accumulation of nitrogen and hydrogen radicals reduces the more deep states within the channel. Although the number of dangling bonds within the channel is almost equal as fabricated, Si_3N_4/poly-Si interface has lager deep states than SiO_2/poly-Si interface. As a result, the bottom-gated TFT with Si_3N_4 dielectric has a larger saturated value of V_{th}. We also found that poly-Si TFTs using ELA processes have the fastest passivation rate (*i.e.*, 30 min). This is because ELA processes result in fewer number of the deep states than that of SPC processes. Similar response in V_{th} was founded in Fig. 3.5 (b) an (c).

3.3.2 Hydrogenation effects on the field-effect mobility and the

leakage current

At the turn-on condition near V_{th}, μ_{FE} (for n-type) is strongly influenced by the density of trap states at or above the surface Fermi-level position (the bulk Fermi level away from the interface plus the surface potential) above mid-gap [3-12]. The number of strained bonds is roughly a factor of 100 more than the number of dangling bonds at a grain boundary. Hydrogen bonding in dangling bonds is far stronger than to the strained bonds (above 2eV greater binding energy than the bond-centered interstitial site) [3-14]. Hence, during passivation, as hydrogen traps and detraps at various sites, it will remain in dangling-bond sites for a significantly longer period than the tail states. Only when the hydrogen concentration is as large as to fill both the deep dangling bond states and the tail states will significant fraction of the tail states be passivated. It takes time to accumulate the necessary concentration of hydrogen. In Fig. 3.6 (a), the mobility increases to the saturation point after NH_3 plasma passivation of 90 min for SiO_2 dielectrics. In other words, a Si_3N_4 layer has a slower hydrogenation rate than SiO_2 dielectric. According to analytic results of SIMS, using Si_3N_4 as the gate dielectric has a larger accumulation of hydrogen and nitrogen atoms at the interface but is slightly smaller concentrations within the channel. The donor-like tail states are weakly passivated by significant number of hydrogen and nitrogen atoms. It means that the

mobility is still dominated by the donor-like tail states at the interface in this case. For using Si_3N_4 as gate insulator, the field-effect mobility continuously increases without saturation occurs. It is described to Si_3N_4 resist nitrogen and hydrogen radicals downward diffusing. Therefore, the further reduction of the tail states was obtained and the field-effect mobility continuous improves. It is also found that poly-Si TFTs using SPC processes have slower hydrogenation rate than that of ELA processes as shown in Fig. 3.6 (b). The propagation of nitrogen and hydrogen radicals inside the grain is slower than that at the grain boundary due to lower binding energy in the tail states. However, SPC processes result in larger tail state densities than ELA processes [3-10], hence nitrogen and hydrogen radicals need a longer time to passivate the tail states of poly-Si TFT using SPC processes. Similar phenomena are also found in Fig. 3.6 (c).

Because of strong dependence of the leakage current with positive gate bias (for p-type) via band-tail assisted thermionic-field emission, the minimum current denotes the dominating carrier transport changing from electrons to holes as V_{GS} is increased more negative. At the minimum leakage current (with V_{GS} closest to the subthreshold regime), the conduction and valence bands are nearly flat, with the Fermi level positioned at about mid-gap. The majority of holes are trapped at mid-gap grain boundary states (above the Fermi level) [3-15]. For using Si_3N_4 and SiO_2 as gate

dielectric, reduction of the minimum leakage current has an almost same passivation rate (*i.e.*, reaching the saturation point at the same time) as shown in Fig. 3.7 (a). We suggest that most of the acceptor-like tail states exist in the channel region near the drain, dominating the minimum leakage current. We also found that the saturation time of acceptor-like tail states is shorter than that of donor-like tail states by comparing Si_3N_4 curve of Fig. 3.7 (a) and 3.6 (a). Contrary to oxide, both of two tail states have almost same saturation time. The previous study [3-13] suggests that the donor-like tail states close to valance band (governing turn-on mobility) and acceptor-like tail states close to conduction band (influencing the leakage current) are responding to plasma hydrogenation at approximately the same rate with the same onset period. For bottom-gated TFTs using Si_3N_4 dielectrics, the donor-like tail states is larger at the interface than that of oxide. Hence, it needs a longer time to passivate such defects.

3.3.3 Hydrogenation effects on the effective trap density

The trap density, which can be determined by the theory established by Levinson *et. al*. [3-16], is based on Seto's theory [3-17]. For a thin film transistor, the source-drain current I_{DS} can be given as following:

$$I_{DS} = \frac{W}{L} C_{ox} V_{DS} \mu_{FE} V_{GS} \exp\left(\frac{-q^3 N_t^{\,2} t}{8\varepsilon_{si} kT C_{ox} V_{GS}} \right) \text{---------------------(Eq. 3-1)}$$

where,

μ_{FE} is the field-effect mobility of the carriers.

q is the electron charge.

K is the Boltzmann's constant.

T is the temperature.

N_t is the trap-state density per unit area.

t is the channel thickness.

This expression, first developed by Levinson et al., is a standard MOSFET's equation with an activated mobility, which depends on the grain boundary barrier height as introduced by Seto. Levinson et al. assumed that the channel thickness was constant and equal to the thickness of poly-Si film. This simplifying assumption is permissible only for very thin film (t < 100 Å). The trap-state density can be obtained by extracting a straight line on the plot of $\ln(I_{DS}/V_{GS})$ versus $1/V_{GS}$ at low source-drain voltage and high gate voltage. Proano et al.[3-15] thought that a better approximation is to calculate the gate induced carrier channel thickness by solving Poisson's equation for an undoped material and to define the channel thickness as a thickness which 80 percent of the total charge induced by the gate. Doing so, one obtains

$$t_{ch} = \frac{\left\{ 8kTt_{ox}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}} \right\}}{q(V_{GS} - V_{FB})} \quad \text{------(Eq. 3-2)}$$

, which varies inversely with (V_{GS}-V_{FB}). This predicts, by substituting Eq. 3-2 into Eq. 3-1, that ln[I_{DS}/(V_{GS}-V_{FB})] varies linearly with 1/$(V_{GS}-V_{FB})^2$. We used the gate voltage at which minimum leakage current occurs as the V_{FB}. Then, Effective trap-density N_t can be determined from the square root of the slope.

$$N_t = \frac{C_{ox}}{q}\left(\frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}\right)^{\frac{1}{4}}\sqrt{|slope|} \text{ --(Eq3-3)}$$

Since the characteristics of poly-Si TFTs are very sensitive to the distribution of the trap states. The deep states is generated from the dangling bonds located mainly at the grain boundaries, while the tail states is caused by the stain bonds of in-grain defects inside the grain. For a SiO_2 dielectric, the effective trap density is dramatically decreased from 1.13×10^{13} to 3.78×10^{12} after 90min NH_3 plasma passivation and becomes saturated condition as shown in Fig. 3.8 (a). However, for a Si3N4 dielectric, the effective trap density decreased from 1.77×10^{13} to 1.04×10^{13} after 300 min NH3 plasma passivation. As a result, it is obviously that the effective trap density continuously reduced by blocking hydrogen and nitrogen atoms. Contrary to ELA sample, we also found that the effective trap density is rapid down to saturation region due to less defect states as fabricated. For top-gated devices, ELA processes also have a faster hydrogenation rate than SPC processes (Fig. 3.8 (b)).

3.4 Summary

In general, we have been known that threshold voltage and subthreshold swing being affected the numbers of the deep states in the channel. For bottom-gated poly-Si TFTs with Si_3N_4 as a gate insulator, SS has a fast passivation rate as soon as SiO_2 dielectrics. The interesting phenomena result from effectively accumulation of H and N atoms in the channel region, and causing significantly reduction of the dangling bonds within the channel. In terms of V_{th}, the slower passivation rate of Si_3N_4 dielectric was found than that of SiO_2 dielectric. The H and N atoms can downward diffuse into oxide region and compensate oxide charges in bulk SiO_2 because the passivation rates for oxide and nitride inside the channel are roughly identical. Contrary to Si_3N_4 dielectrics, most of H and N atoms are blocked within the channel. Hence, no saturations were found in improving V_{th} during NH_3 plasma passivation. For the top-gated TFTs, the passivation rates of V_{th} are dominated by channel qualities. ELA processes have the faster passivation rates than SPC processes due to fewer numbers of the dangling bonds.

The field-effect mobility of using Si_3N_4 as a gate insulator has a slower passivation rate than that of the SiO_2 dielectric. The donor-like tail states for using Si_3N_4 dielectric are difficultly passivated by significant concentration of hydrogen and nitrogen atoms. It means that the field-effect mobility is still dominated by the donor-like tail states at the

interface, in other words, the mobility is weakly depend on substantial incorporation of hydrogen and nitrogen atoms. But for Si_3N_4 dielectrics, the field-effect mobility continuously improves without saturations during NH_3 plasma passivation. In terms of the minimum leakage current, both of Si_3N_4 and SiO_2 dielectrics have nearly fast passivation rates. Because the minimum leakage current originates from the acceptor-like tail states near the drain junction within the channel, indicating same reduction rates of the tail states in the drain junction. We also found that top-gated poly-Si TFTs using ELA processes have the faster passivation rate in mobility and the minimum leakage current.

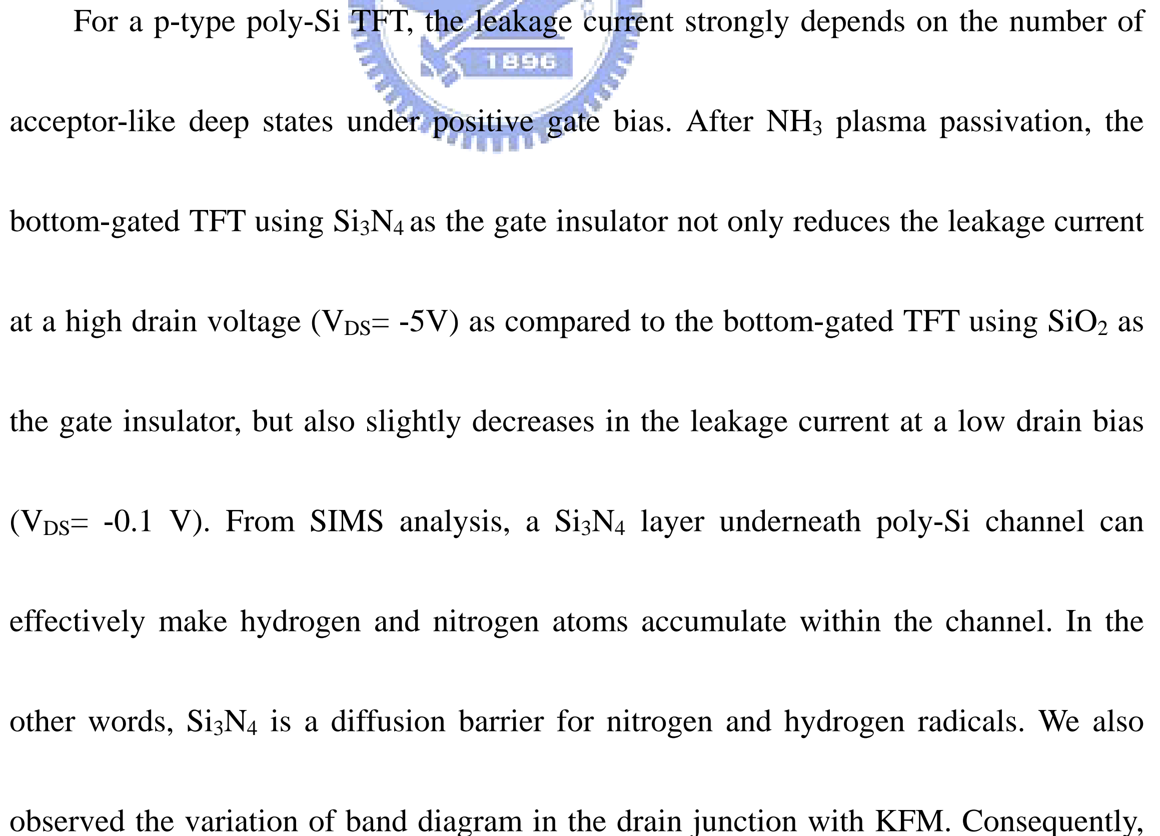
N_t represents the total effective trap states exist in the channel region when fully on state. Consisting with SIMS analysis, Si_3N_4 dielectrics observed that the effective trap density continuously reduced by blocking hydrogen and nitrogen atoms when passivation time further increasing. Contrary to SiO_2 dielectrics, N_t achieved the saturation regime after NH_3 plasma passivation of 90 min due to H and N atoms can downward diffuse into oxide layer. For ELA processes, N_t still has a faster passivation rate than SPC because of fewer defects present.

Chapter 4

Conclusions

4.1 Conclusions

In this thesis, we utilized Si_3N_4 and SiO_2 as the insulator of bottom-gated poly-Si TFTs to investigate the reduction of the leakage current by NH_3 plasma treatment. Furthermore, we also investigated influences of long-time NH_3 plasma treatment on the electrical characteristics of poly-Si TFTs.



For a p-type poly-Si TFT, the leakage current strongly depends on the number of acceptor-like deep states under positive gate bias. After NH_3 plasma passivation, the bottom-gated TFT using Si_3N_4 as the gate insulator not only reduces the leakage current at a high drain voltage (V_{DS}= -5V) as compared to the bottom-gated TFT using SiO_2 as the gate insulator, but also slightly decreases in the leakage current at a low drain bias (V_{DS}= -0.1 V). From SIMS analysis, a Si_3N_4 layer underneath poly-Si channel can effectively make hydrogen and nitrogen atoms accumulate within the channel. In the other words, Si_3N_4 is a diffusion barrier for nitrogen and hydrogen radicals. We also observed the variation of band diagram in the drain junction with KFM. Consequently,

the increasing depletion width indicates defect reduction in the drain junction leading to improve the leakage current. After NH_3 plasma passivation, the leakage current of poly-Si TFTs using Si_3N_4 as the insulator of bottom-gated poly-Si TFTs was about one order of magnitude lower than that using SiO_2 as the insulator of bottom-gated poly-Si TFTs. We say that defect-reduction control dominates the difference of the leakage current. When two of the leakage currents approach to together at high drain fields, the tunneling control is responsible for the mechanism.

In general, we have been known that the threshold voltage and the subthreshold swing are affected by the number of the deep states in the channel. For bottom-gated poly-Si TFTs with Si_3N_4 as the gate insulator, SS has a fast passivation rate as soon as using SiO_2 as insulator of bottom-gated poly-Si TFT. In the initial stage, it implies that the passivation rates of the deep states inside the channel are roughly identical for SiO_2 and Si_3N_4 films. But in terms of V_{th}, it has a slower passivation rate than using SiO_2 as the insulator. This result is suggests that hydrogen and nitrogen atoms can downward diffuse into oxide layer, and oxide charges are compensated by these atoms in bulk SiO_2. Contrary to use Si_3N_4 dielectrics, V_{th} is continuously improved by NH_3 plasma treatment without saturation. This result is consistent with SIMS analysis. The significantly accumulation of nitrogen and hydrogen radicals reduces the more deep

states within the channel. We also found that top-gated poly-Si TFTs using ELA techniques obtained the faster passivation rate in V_{th} as compared to SPC ones due to fewer dangling bonds as devices are fabricated.

The mobility of poly-Si TFT with Si_3N_4 as the bottom-gated insulator has a slower passivation rate than that of using SiO_2 as the bottom-gated insulator. It means that the mobility of the bottom-gated TFT is still dominated by the number of donor-like tail states at the interface as devices are fabricated. As a result, using Si_3N_4 films with NH_3 plasma treatment needs a longer time to passivate those defects at the interface. For using Si_3N_4 as gate insulator, the field-effect mobility continuously increases without saturation occurs. It is described to Si_3N_4 resist nitrogen and hydrogen radicals downward diffusing. Therefore, the further reduction of the tail states was obtained and the field-effect mobility continuous improves. However, in terms of the minimum leakage current, both of Si_3N_4 and SiO_2 dielectrics have nearly fast passivation rates. Because the minimum leakage current originates from acceptor-like tail states in the drain junction, it indicates same defect-reduction rates of the tail states in the drain junction with short-time NH_3 plasma treatment. When long-time NH3 plasma is applied, the leakage current of poly-Si TFTs with Si_3N_4 as bottom-gated insulator has a lower value at more positive gate bias than that of using SiO_2 as the bottom-gated insulator.

We also shown that top-gated poly-Si TFTs using ELA processes have faster passivation rates in mobility and in the minimum leakage current than that of using SPC processes. N_t represents the total effective trap states existing in the channel region when devices are biased under on state. Consisting with SIMS analysis, using Si_3N_4 films underneath poly-Si channel has a continuously reduction of effective trap density with long-time NH_3 plasma treatment. Contrary to SiO_2 dielectrics, N_t achieves the saturation region after NH_3 plasma treatment of 90 min. As mentioned above, using Si_3N_4 films underneath poly-Si channel is good for poly-Si TFTs by long-time NH_3 plasma treatment.

4.2 Future Works

It is the future trend for AMLCDs to fabricate low temperature poly-Si TFTs on low-cost glass substrates. For LTPS TFTs using ELA techniques, there are still some problems which shold be solved. We introduce these issues in three parts:

(1) Improving the surface roughness: The surface roughness increases with increasing laser energy density and cause degradation of off-state current and reliability for the ELA poly-Si TFTs [1-25]. Meanwhile, the gate oxide can not scale down due to the surface roughness enhances local electric fields in the oxide. We suggest that CMP and etching-back

Chapter 3 Influence of Long-time NH3 Plasma Treatment on the Electrical Characteristics of poly-Si TFTs

3.1 Introduction 24

3.2 Experiments for Long-time NH_3 Plasma Treatment

3.2.1 Fabrication of bottom-gated poly-Si TFTs using SPC processes 27

3.2.2 Fabrication of top-gated poly-Si TFTs using SPC/ELA processes 28

3.3 Results and Discussions

3.3.1 Hydrogenation effects on the threshold voltage and subthreshold swing 29

3.3.2 Hydrogenation effects on the field-effect mobility and the leakage current 30

3.3.3 Hydrogenation effects on the effective trap density 33

3.4 Summary 36

Chapter 4 Conclusions

4.1 Conclusions 38

4.2 Future Works 41

References 43

Table List 51

Figure List 53

Publications 94

Vita 95

techniques may be candidates for solving surface roughness.

(2) Lowering the leakage current: poly-Si TFTs with high off-state current degrade the contrast ratio of display because of the loss of video information before the frame is being refreshed. Reducing the numbers of the trap states in the drain junction and decreasing the lateral electric field near the drain junction are effective ways to reduce the leakage current.

(3) Avoiding device-to-device variation: a random distribution of grain boundaries in the channel makes a great impact on the uniformity of device performance. To further control the performance of laser-crystallized poly-Si TFTs, the number of grain boundaries in the drain junction has to be considered.

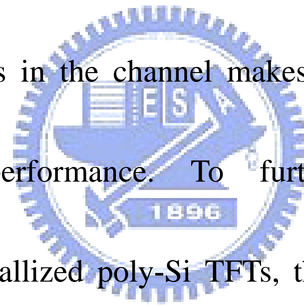


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Table 2.1

The electrical characteristics of bottom-gated poly-Si TFTs before and after NH_3 plasma hydrogenation.

Sample	Gate dielectric	V_{th} (V)	Mobility (cm^2/V-s)	SS (mV/dec)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}
Sample A (SPC) before hydrogenation	SiO_2	-23.6	2.4	1916	8.1E-6	2.6E-10	3.12E+4
Sample A (SPC) after 360min hydrogenation	SiO_2	-8.64	9.3	334	2.28E-4	1.9E-13	1.2E+9
Sample B (SPC) before hydrogenation	Si_3N_4	-27.3	0.1	1832	4.19E-7	1.96E-10	2.13E+3
Sample B (SPC) after 300min hydrogenation	Si_3N_4	-9.3	2.1	242	5.15E-5	1.5E-13	3.43E+8

Table 2.2

The electrical characteristics of p-type top-gated poly-Si TFTs using SPC/ELA techniques before and after NH_3 plasma hydrogenation.

Sample	Gate dielectric	V_{th} (V)	Mobility (cm^2/V-s)	SS (mV/dec)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}
SPC before hydrogenation	SiO_2	-23.8	10.5	756	2.8E-5	2.4E-11	1.18E+6
SPC after 300min hydrogenation	SiO_2	-11.5	18.9	406	1.2E-4	1.8E-13	6.9E+8
ELA before hydrogenation	SiO_2	-15.7	30.8	294	1.9E-4	3.9E-12	4.71E+7
ELA after 240min hydrogenation	SiO_2	-3.15	41.1	272	4.1E-4	8E-14	5.1E+9

Table 2.3

The electrical characteristics of n-type top-gated poly-Si TFTs using SPC/ELA techniques before and after NH_3 plasma hydrogenation.

Sample	Gate dielectric	V_{th} (V)	Mobility (cm^2/V-s)	SS (mV/dec)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}
SPC before hydrogenation	SiO_2	14.8	12.28	2097	4E-5	4.3E-11	9.3E+5
SPC after 300min hydrogenation	SiO_2	2.43	32.5	792	4.1E-4	2.1E-11	1.95E+7
ELA before hydrogenation	SiO_2	2.4	50.5	632	7.4E-4	2.6E-12	2.87E+8
ELA after 240min hydrogenation	SiO_2	-1.8	66.8	319	1.2E-3	5E-14	2.36E+10

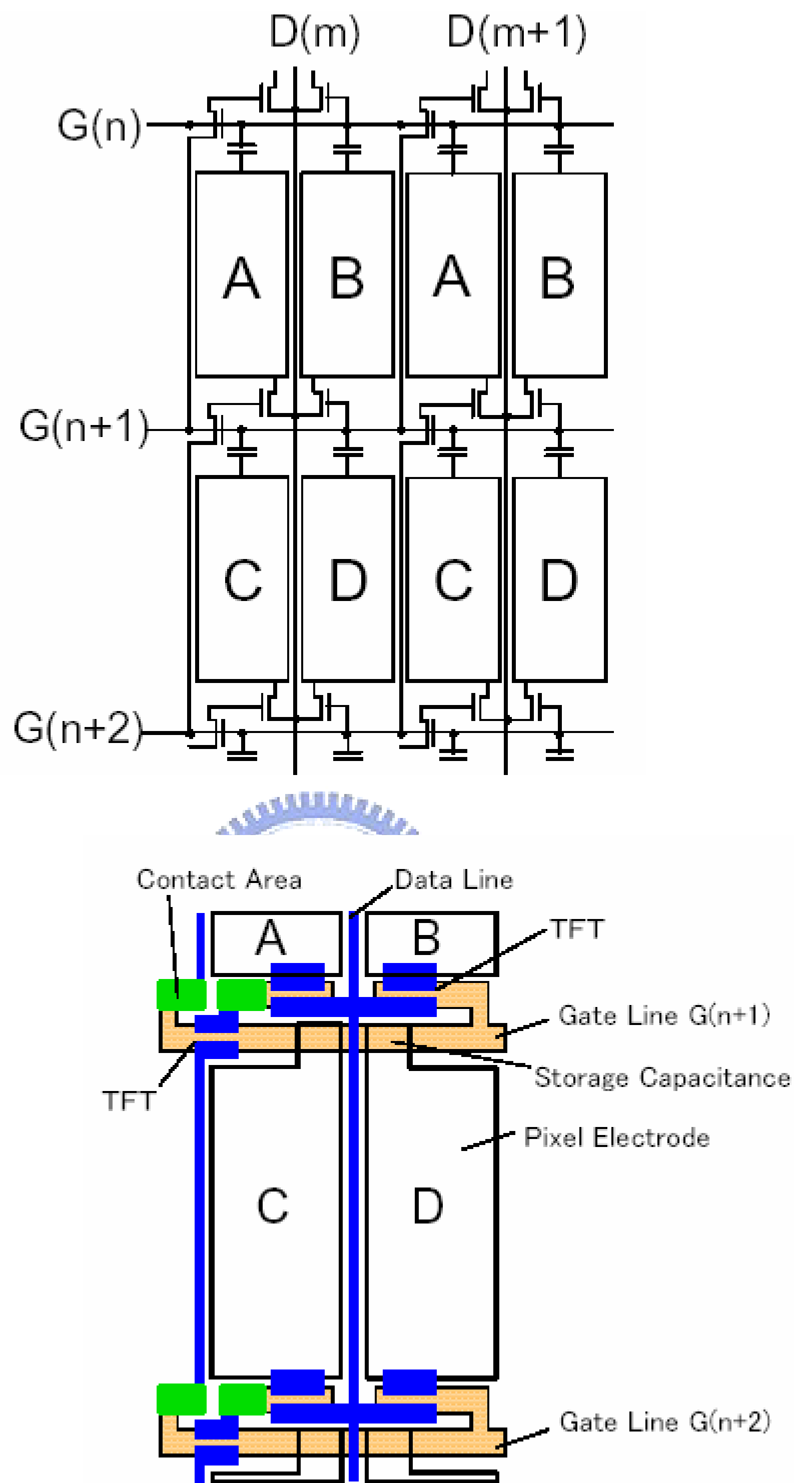


Figure 1.1 The equivalent circuit diagrams of the pixel and its layout in AMLCDs.

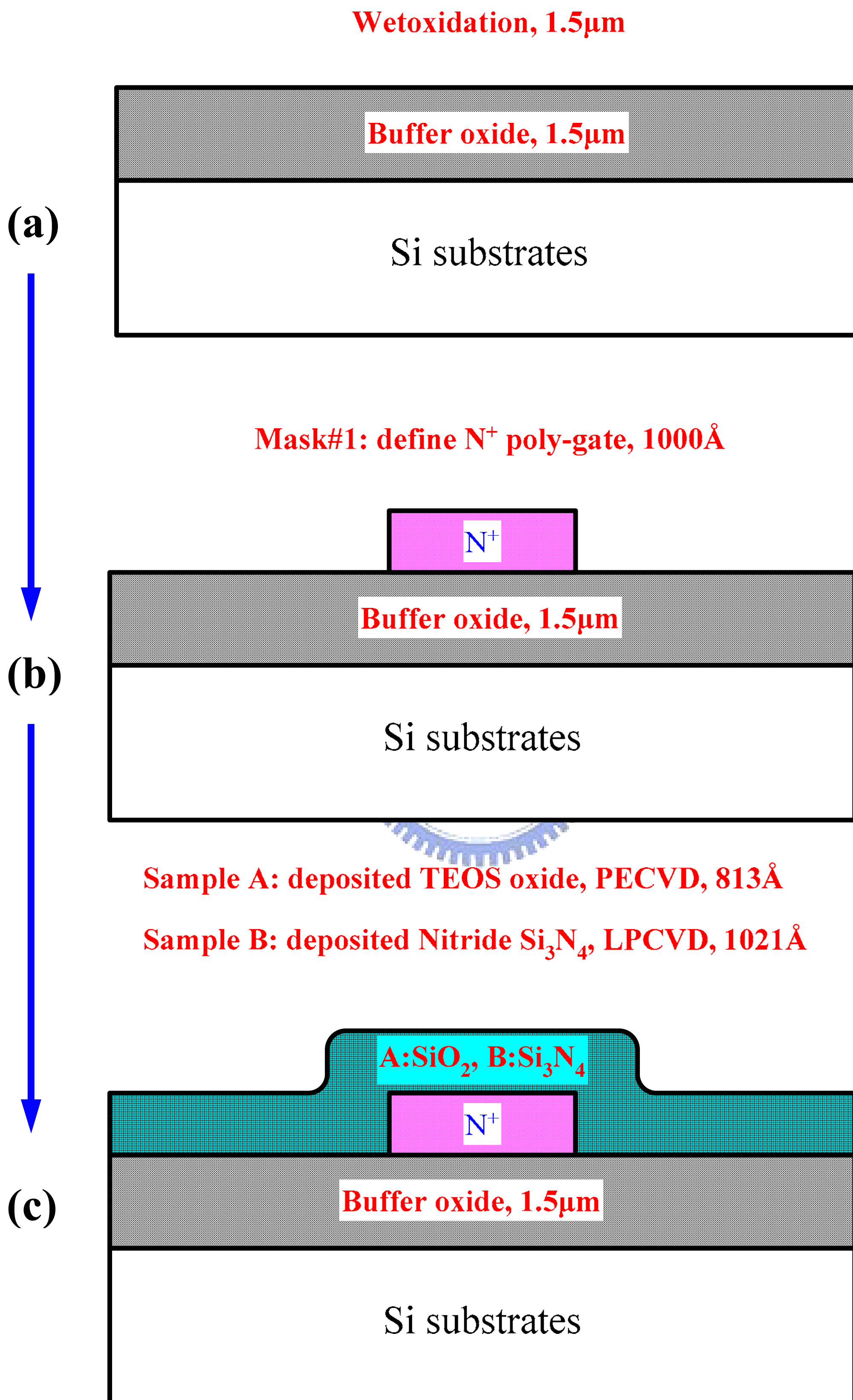


Figure 2.1 Key process flows of p-type bottom-gated poly-Si TFTs.

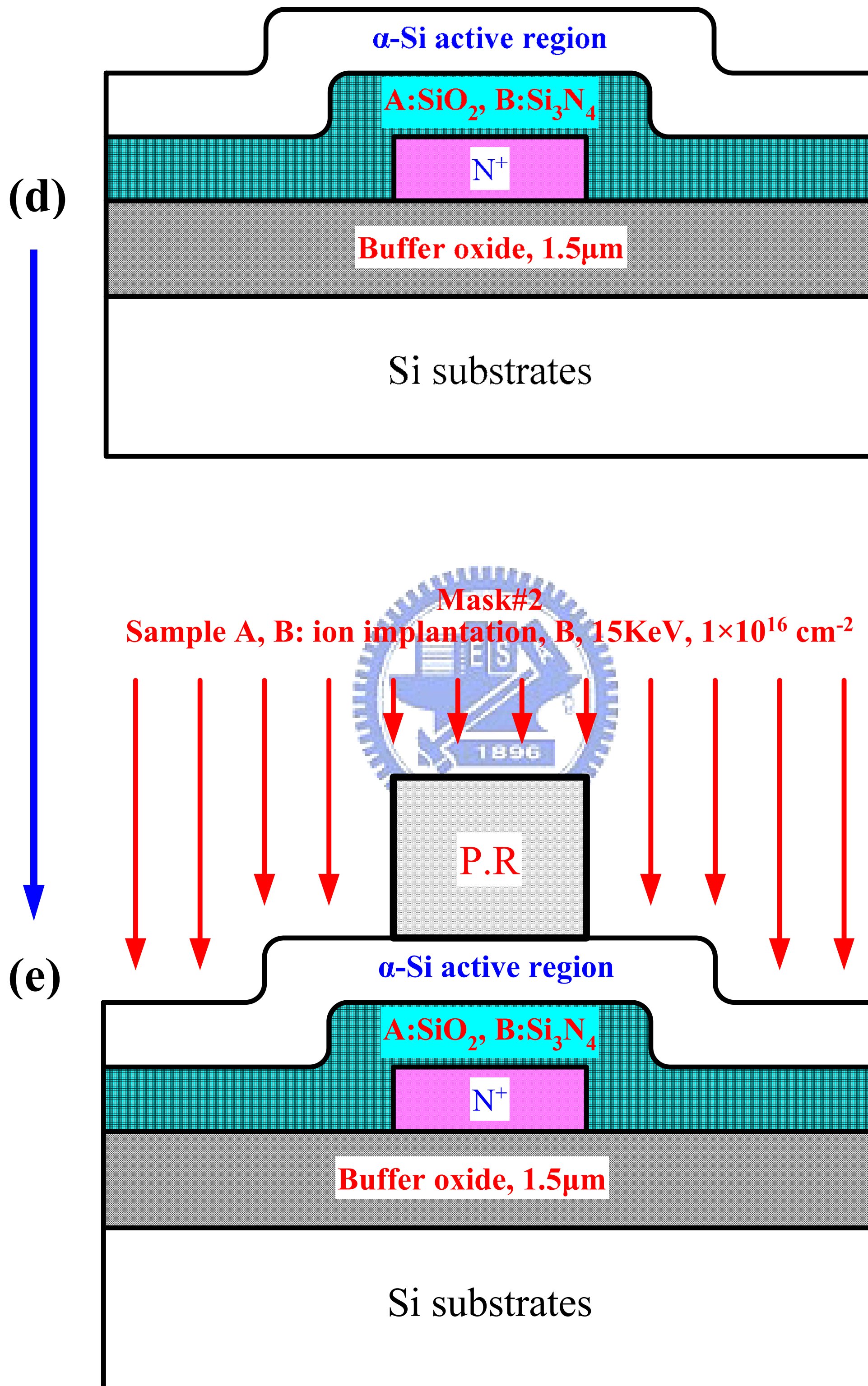
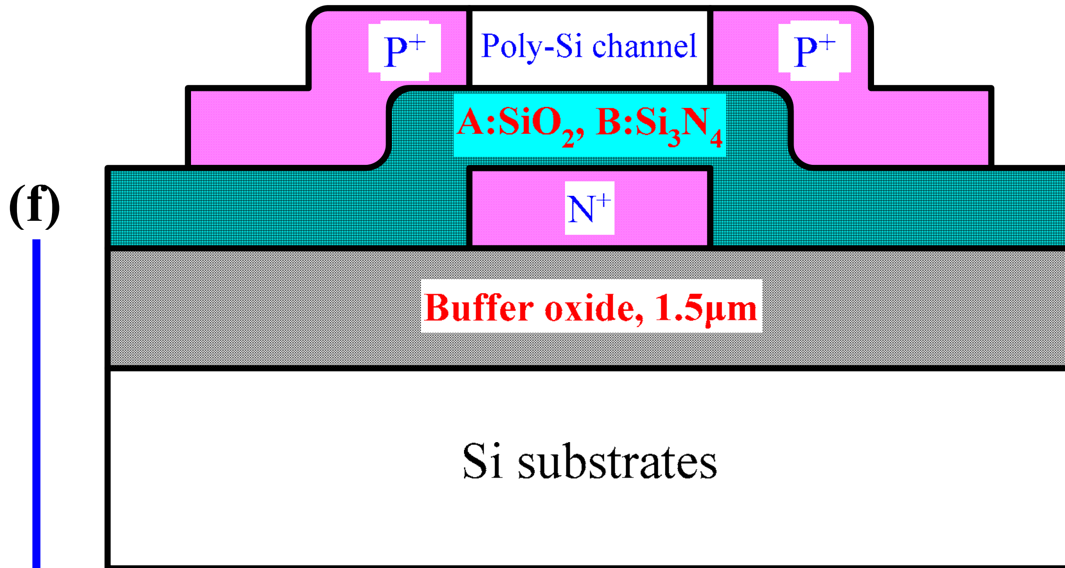


Figure 2.1 Key process flows of p-type bottom-gated poly-Si TFTs.

Mask#3
Sample A, B: define active region



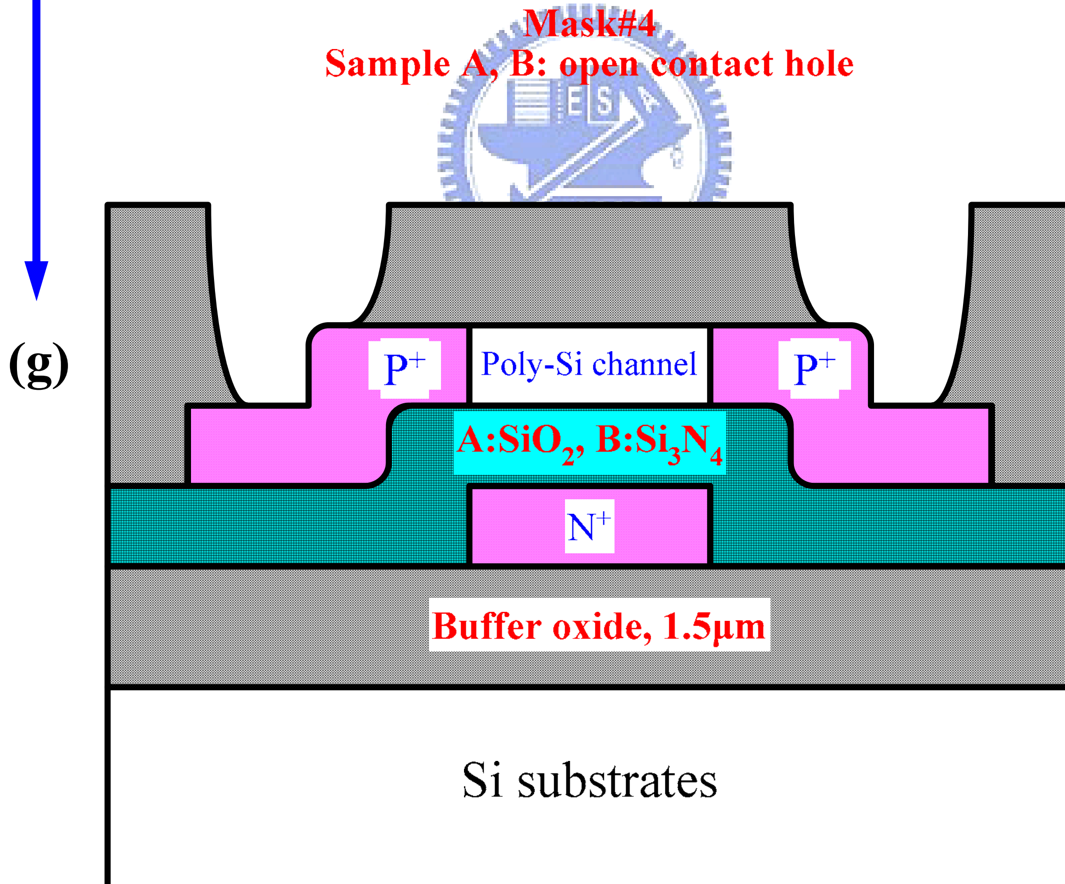


Figure 2.1 Key process flows of the p-type bottom-gated poly-Si TFTs.

Mask#5
Sample A, B: define Al pattern

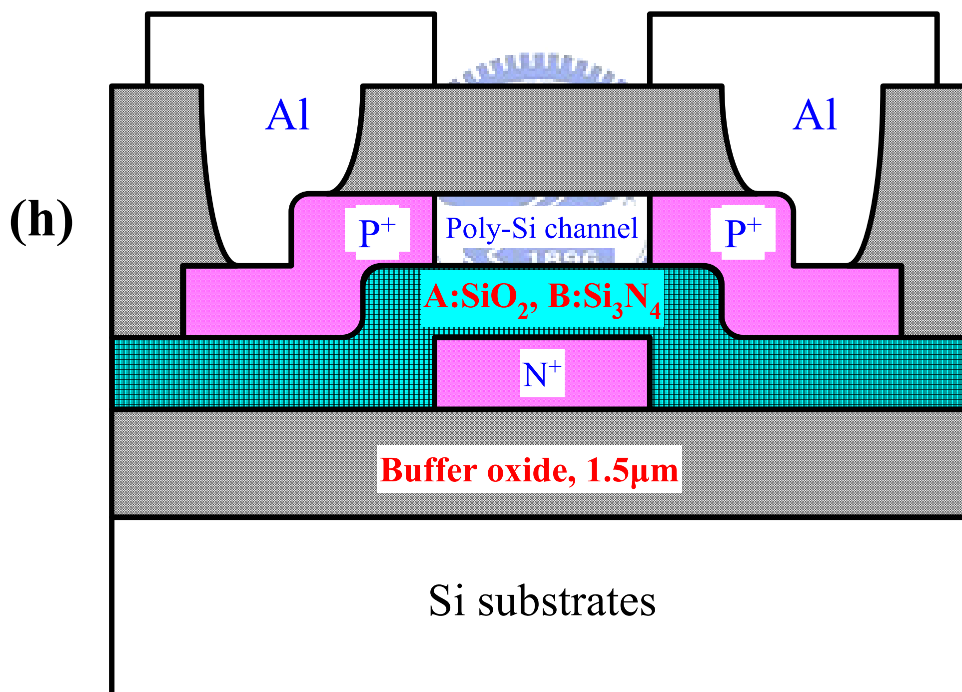


Figure 2.1 Key process flows of the p-type bottom-gated poly-Si TFTs.

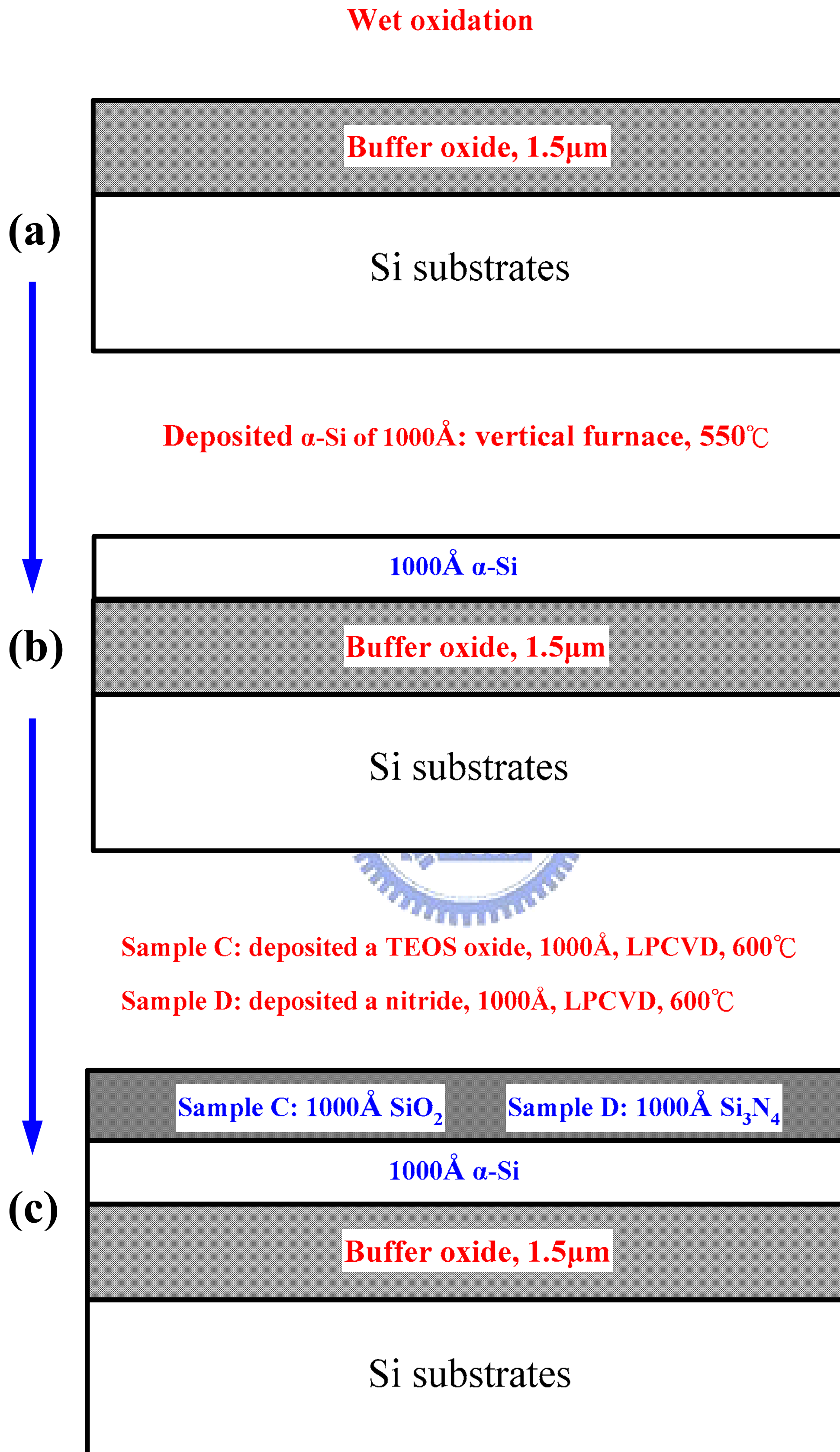
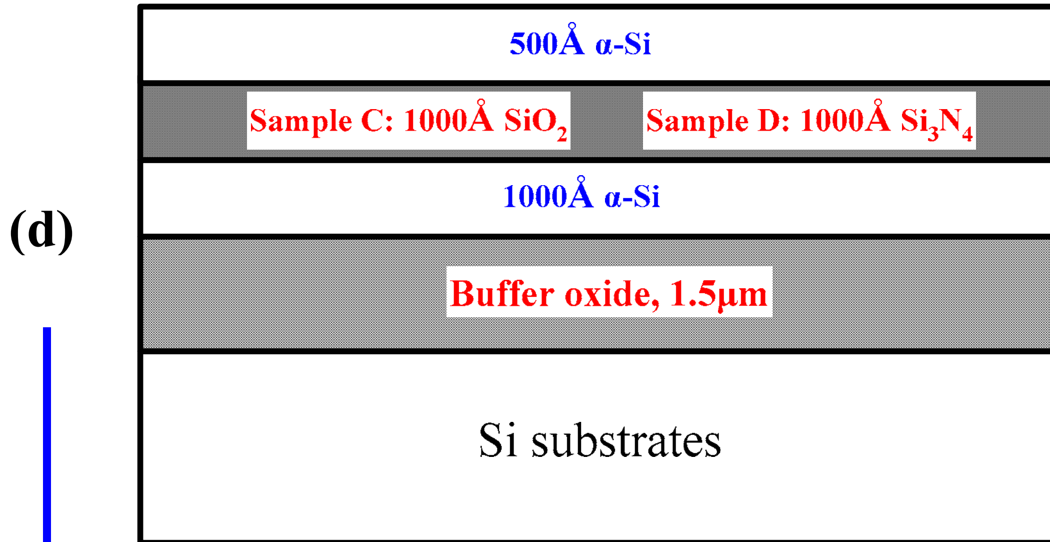


Figure 2.2 Key process flows of SIMS/ESCA samples.

Deposited α-Si of 500Å: vertical furnace, 550℃



Deposited a TEOS oxide layer of 3000Å: LPCVD, 695℃

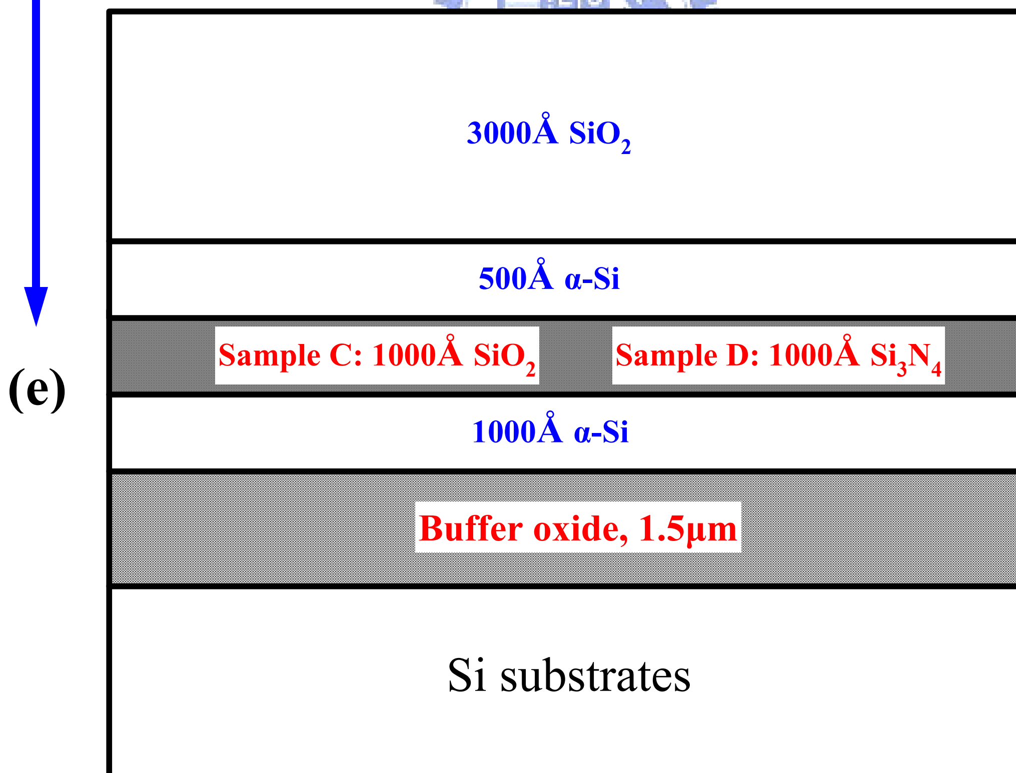


Figure 2.2 Key process flows of SIMS/ESCA samples.

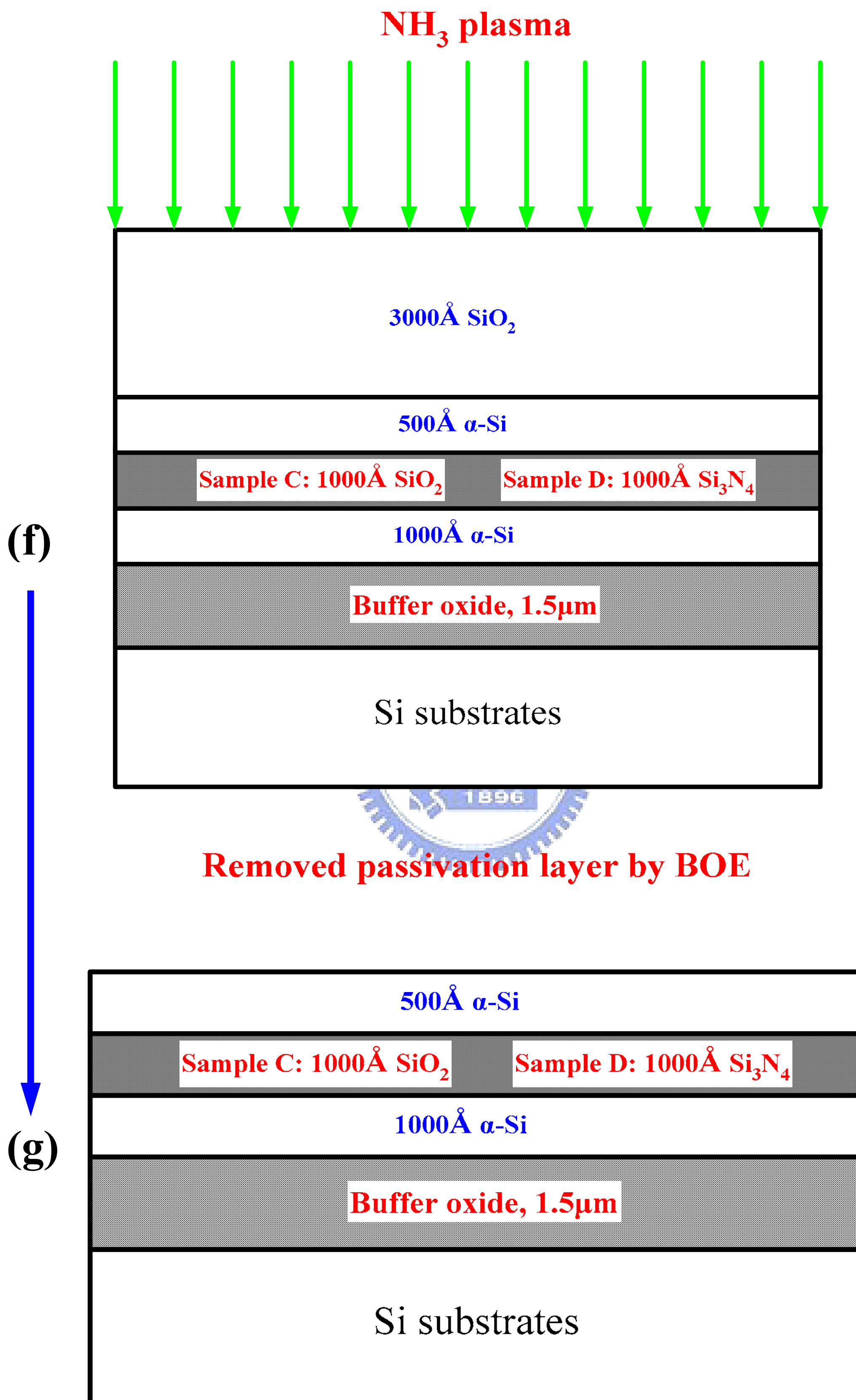


Figure 2.2 Key process flows of SIMS/ESCA samples.

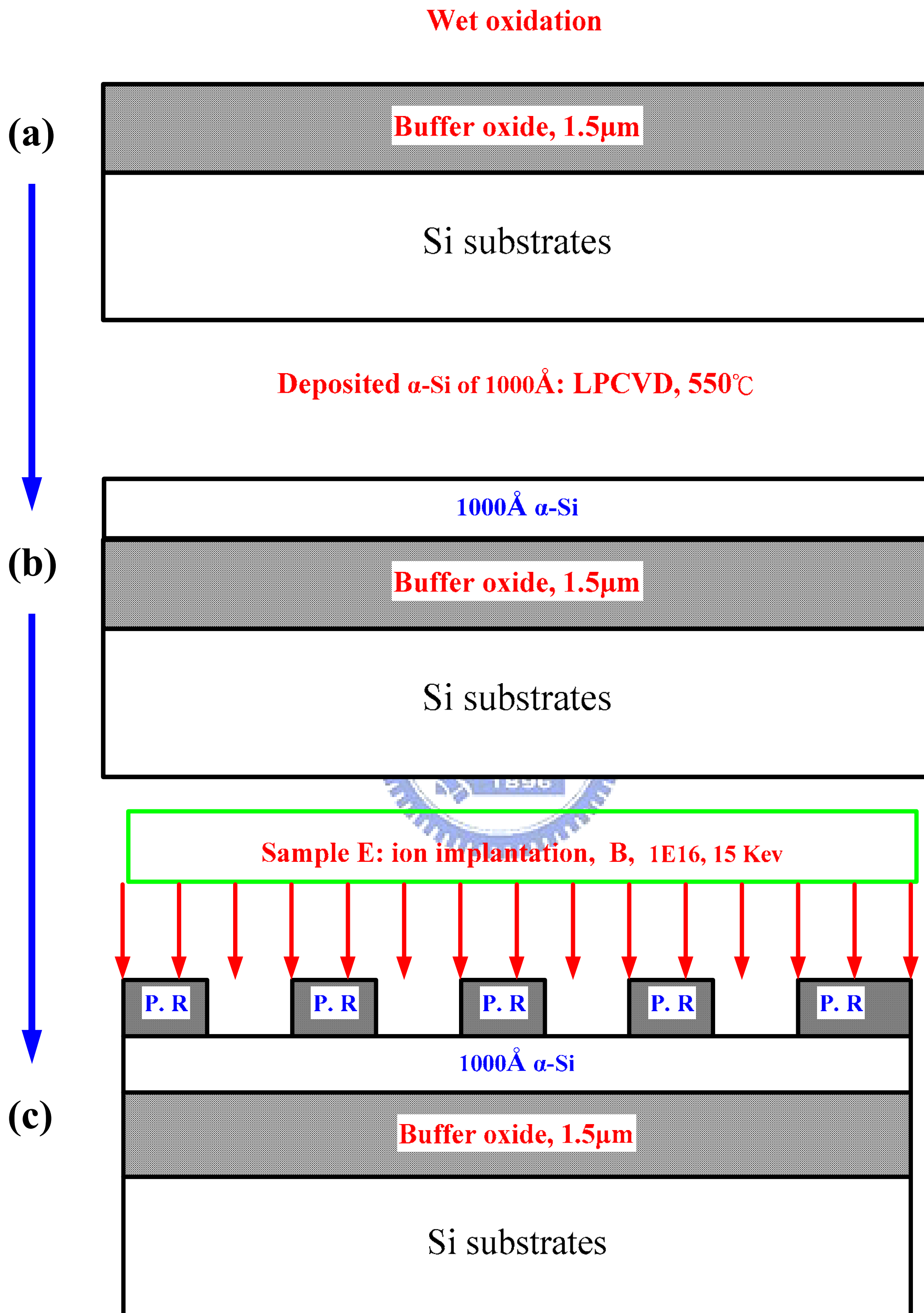


Figure 2.3 Key process flows of KFM samples.

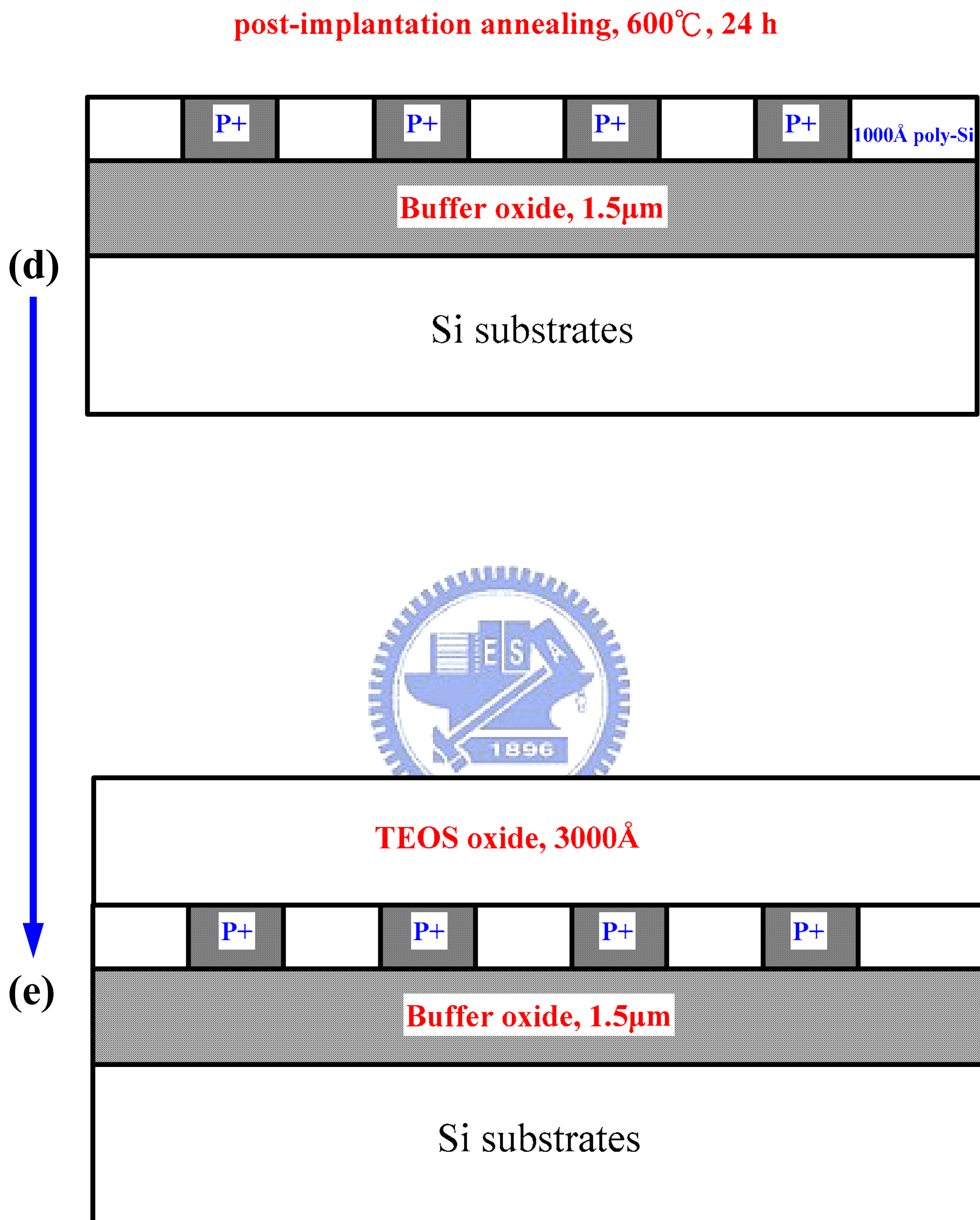


Figure 2.3 Key process flows of KFM samples.

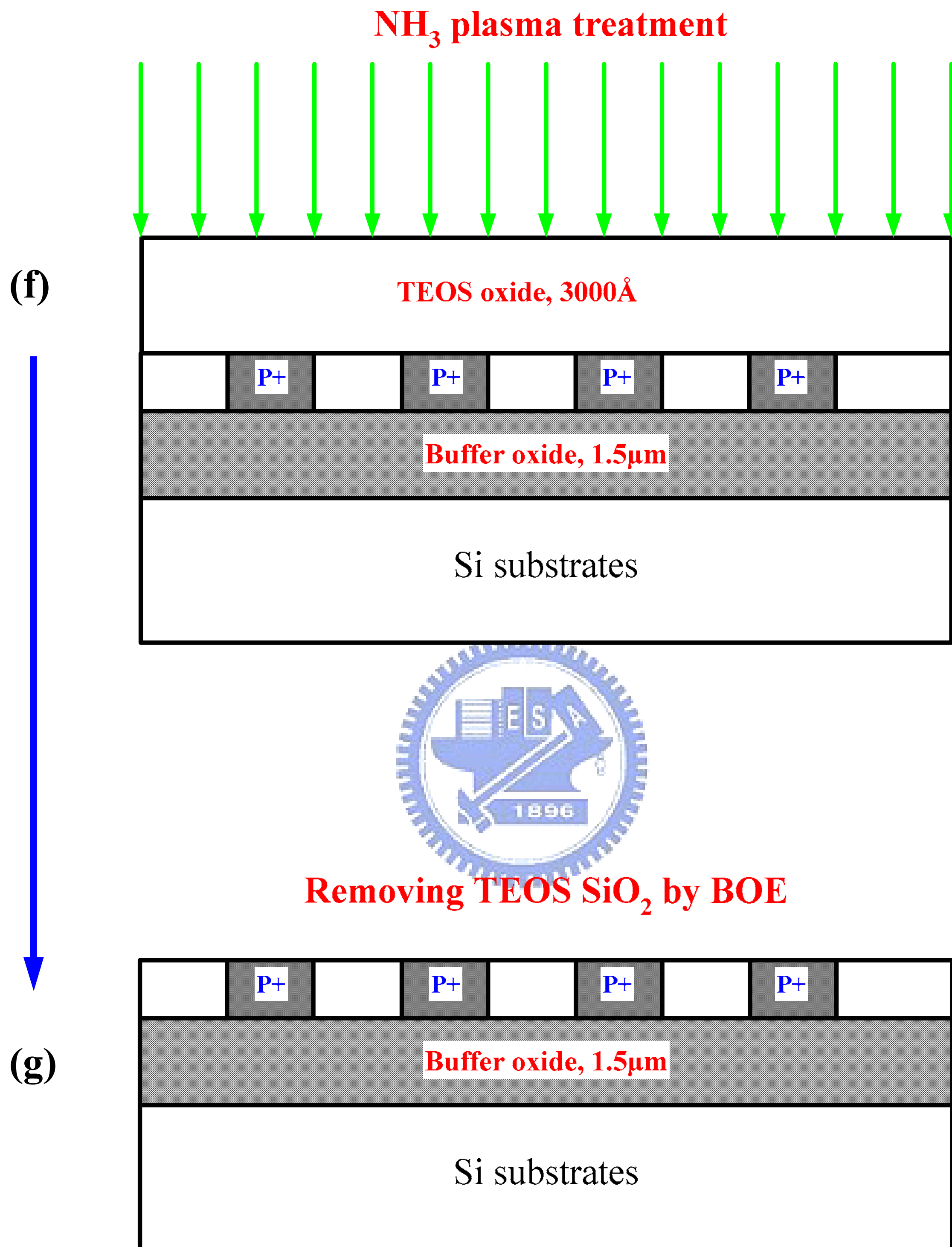


Figure 2.3 Key process flows of KFM samples.

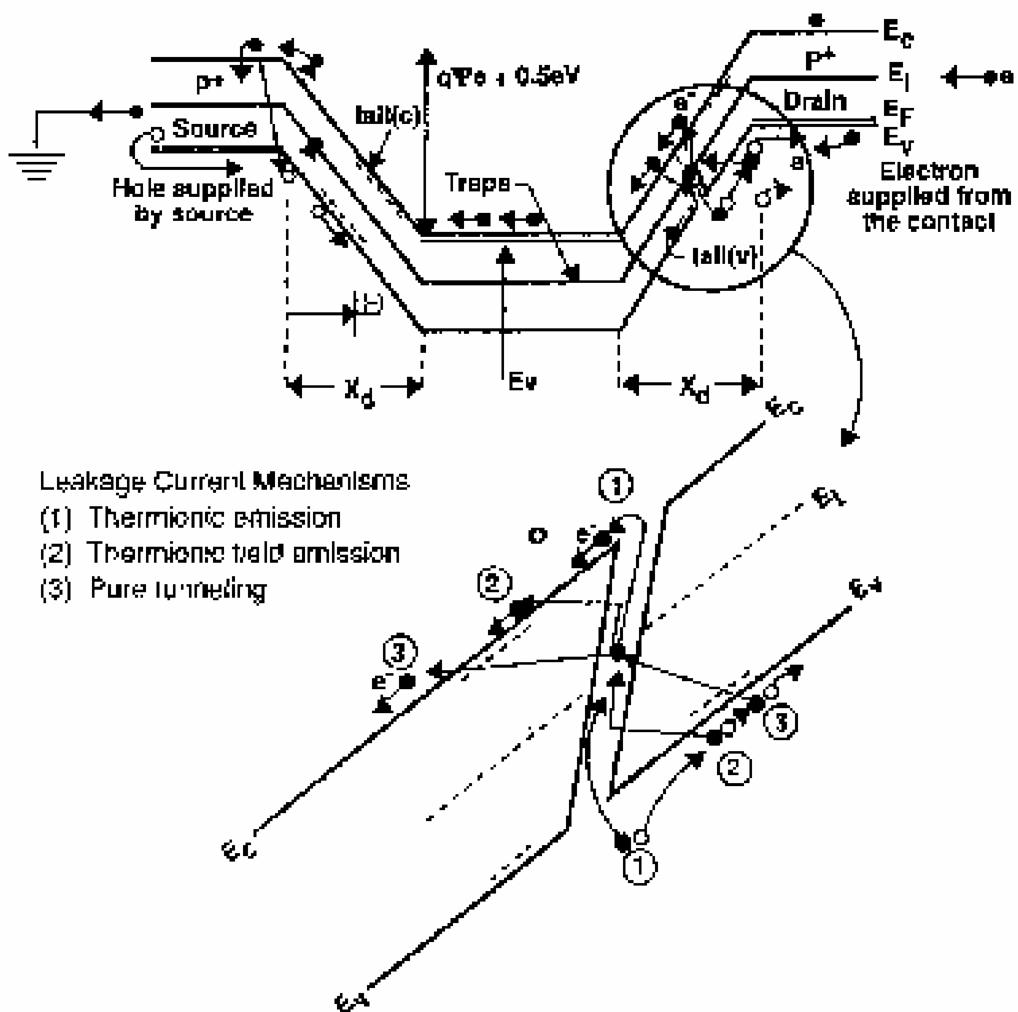
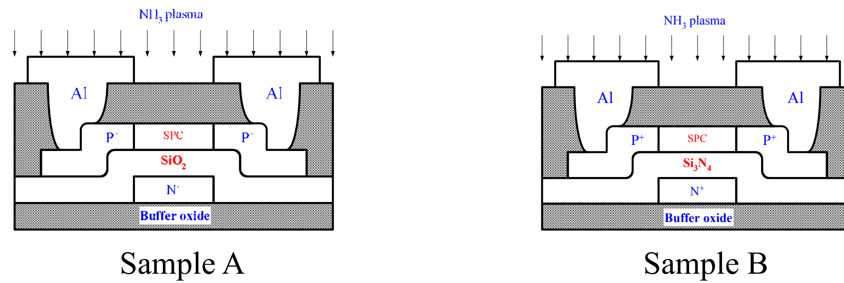


Figure 2.4 Schematic illustration of the leakage current model in poly-Si TFTs.

Sample A Sample B

Figure 2.5 (a) Transfer characteristics for comparison of p-type bottom-gated TFTs using SPC/ELA before and after hydrogenation at V_{DS}= -0.1 V. Sample A (gate oxide), and B (gate nitride) treat 360 min, and 300min NH_3 plasma passivation, respectively.



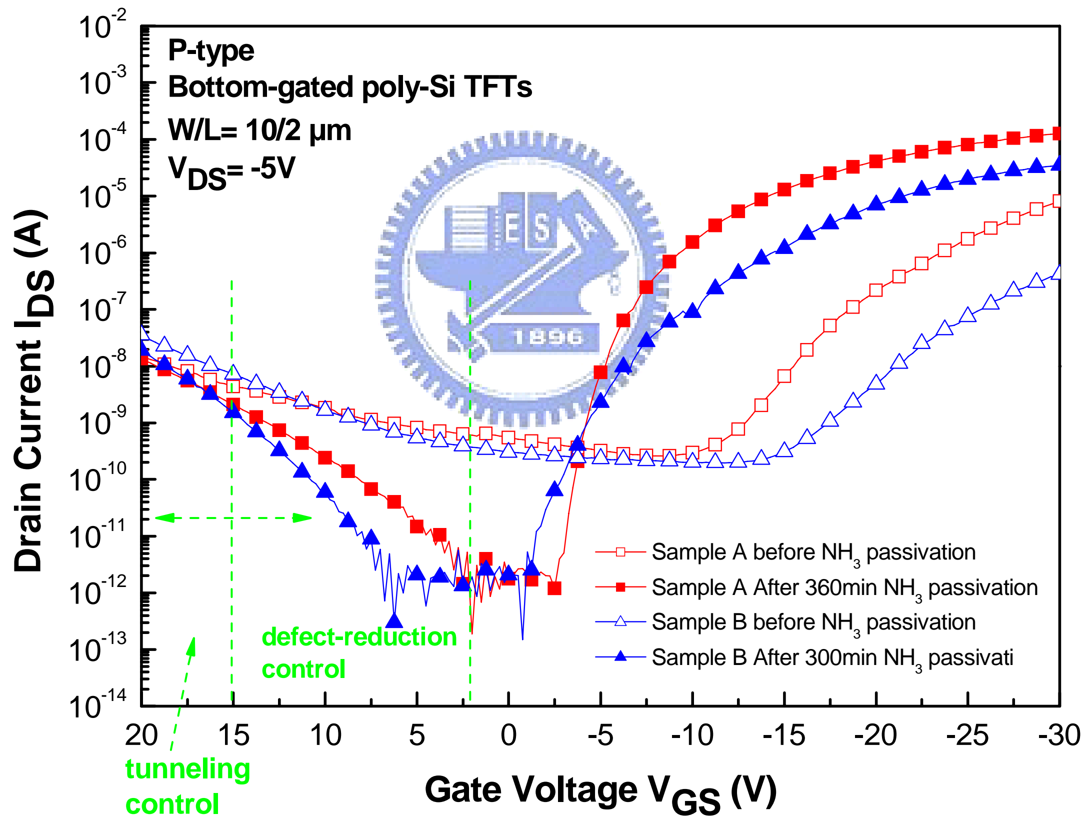
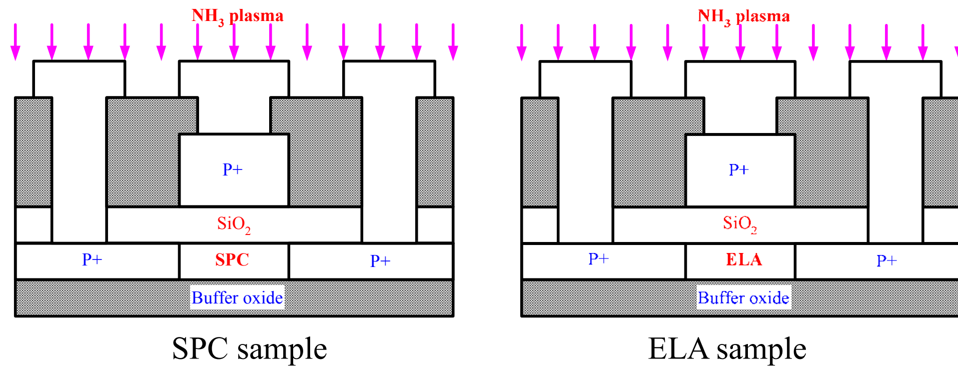


Figure 2.5 (b) Transfer characteristics for comparison of p-type bottom-gated TFTs using SPC/ELA before and after hydrogenation at V_{DS}= -5 V. Sample A (gate oxide), and B (gate nitride) treat 360 min, and 300min NH_3 plasma passivation, respectively.



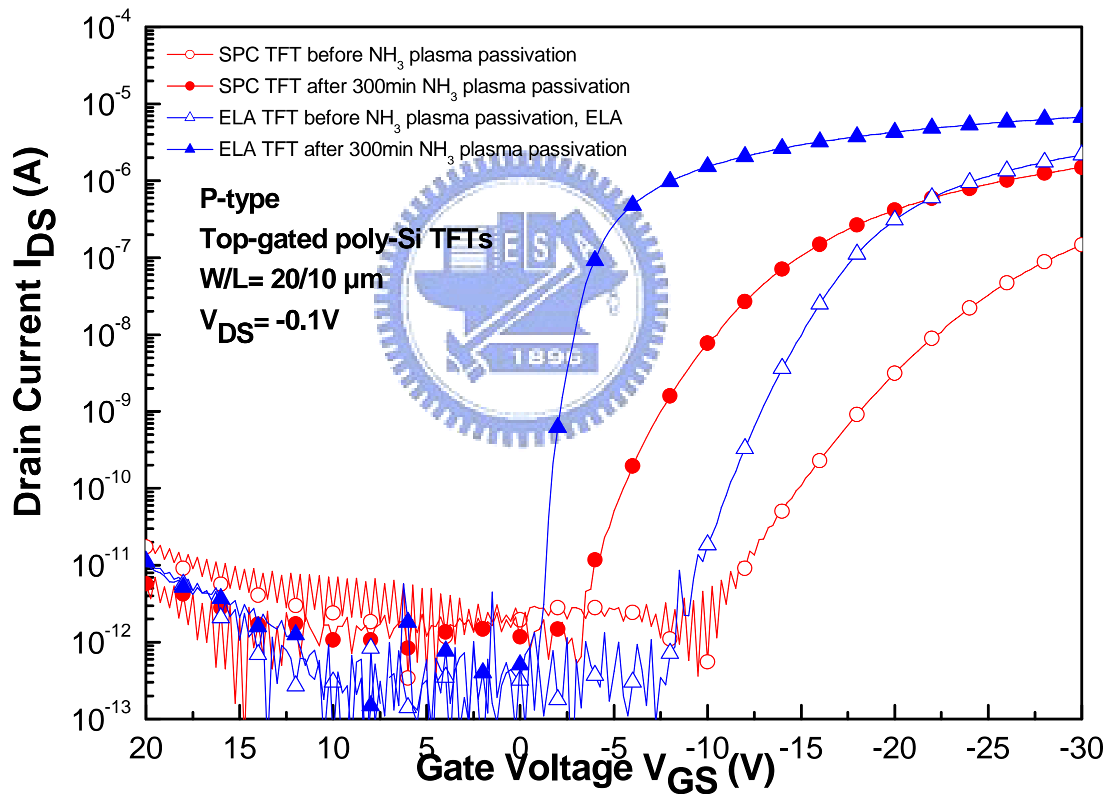
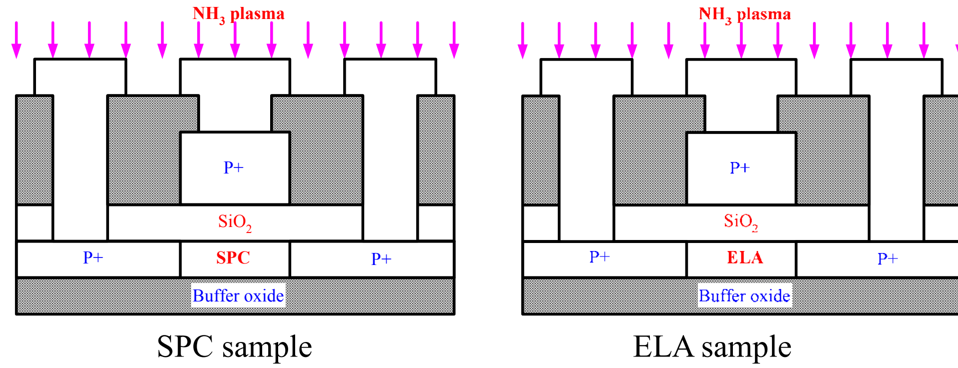


Figure 2.6 (a) Transfer characteristics for comparison of p-type top-gated TFTs using SPC/ELA before and after hydrogenation at V_{DS}= -0.1 V. Both of SPC (gate oxide) and ELA (gate oxide) samples treat 300min NH_3 plasma passivation.



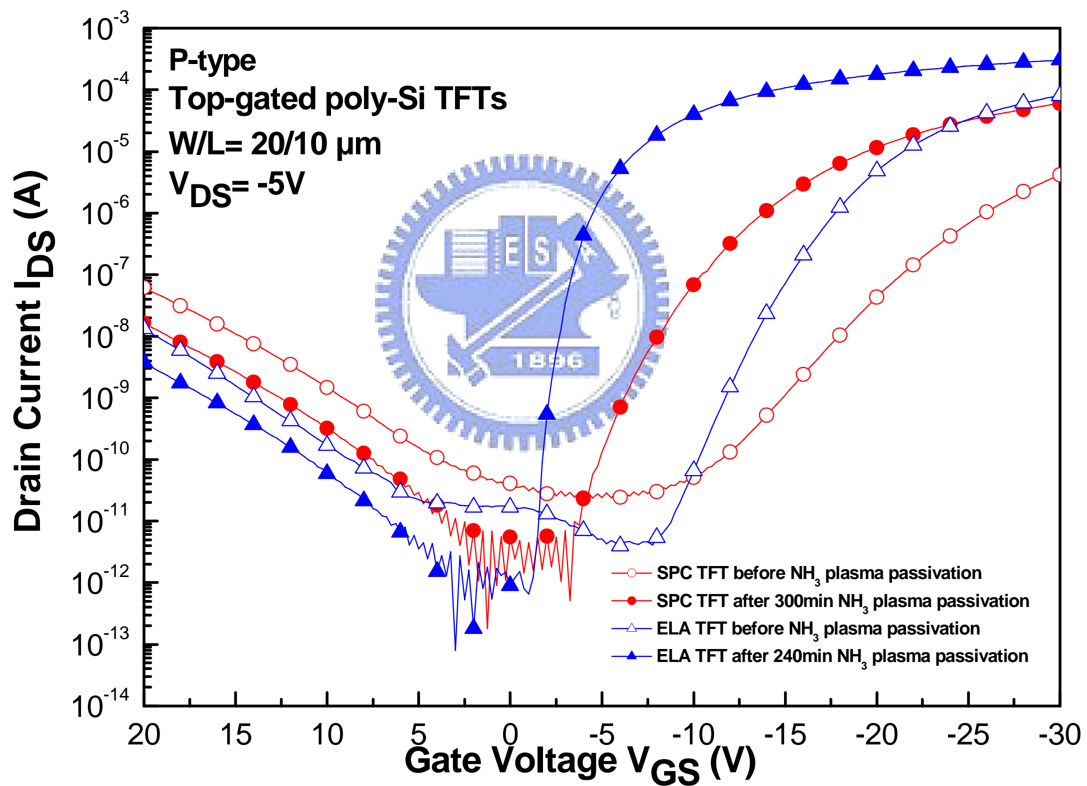
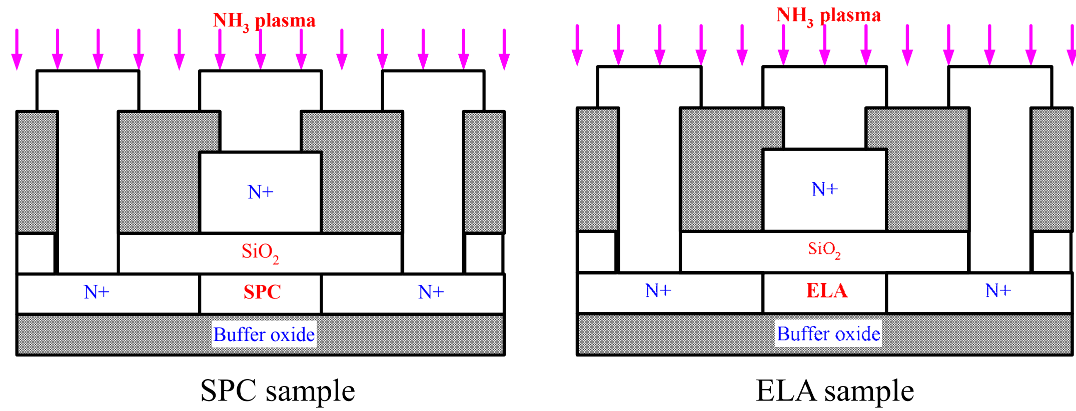


Figure 2.6 (b) Transfer characteristics for comparison of p-type top-gated TFTs using SPC/ELA before and after hydrogenation at V_{DS}= -5 V. Both of SPC (gate oxide) and ELA (gate oxide) samples treat 300min NH_3 plasma passivation.



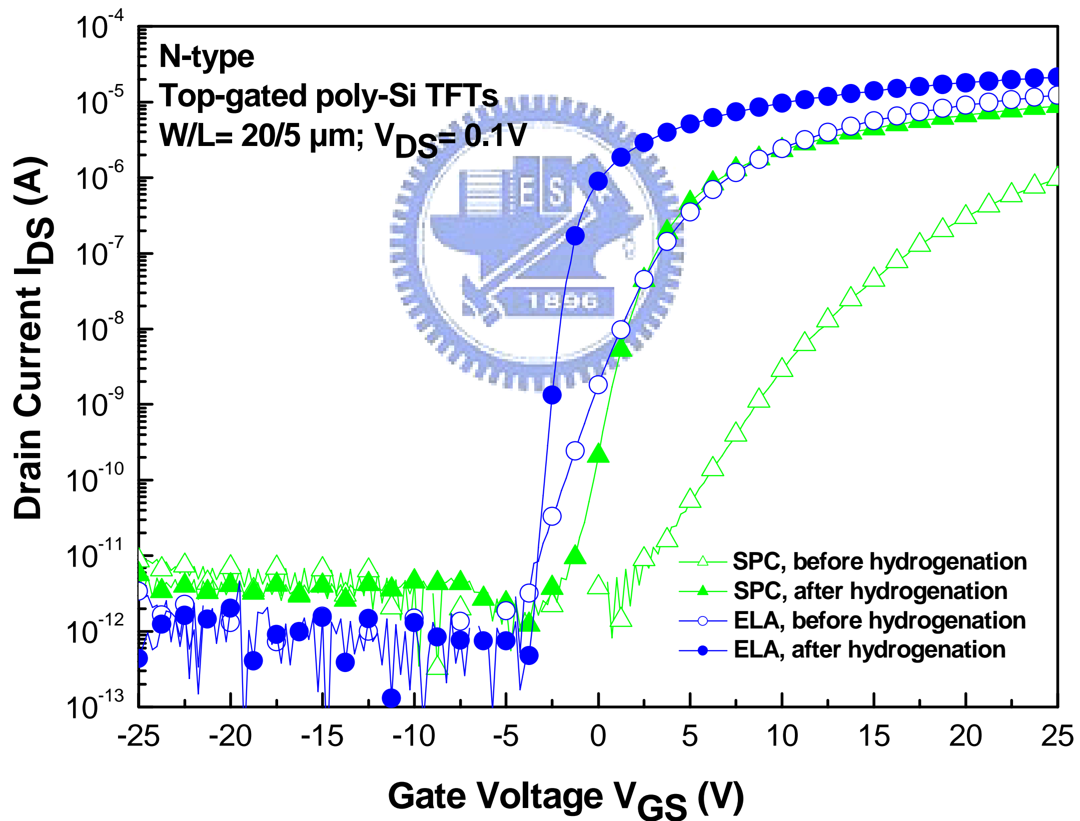
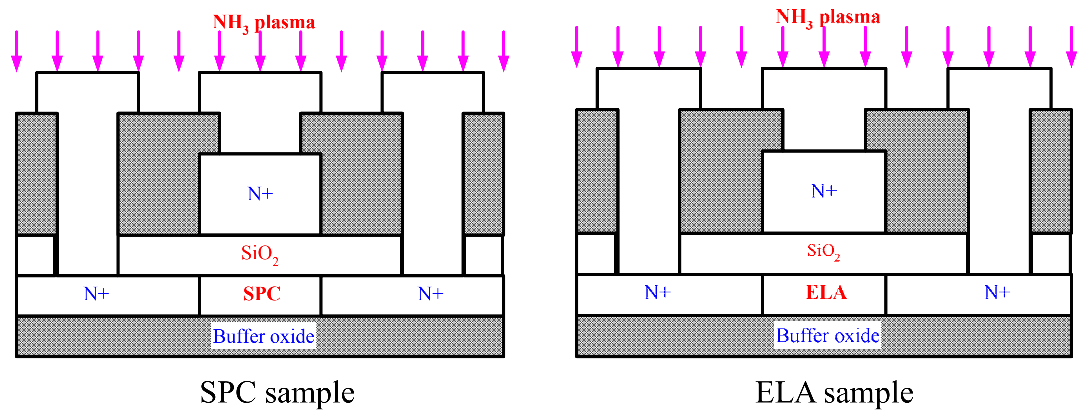


Figure 2.7 (a) Transfer characteristics for comparison of n-type top-gated TFTs before and after hydrogenation at V_{DS}= 0.1 V. SPC and ELA samples treat 300 min, and 360 min NH_3 plasma passivation, respectively.



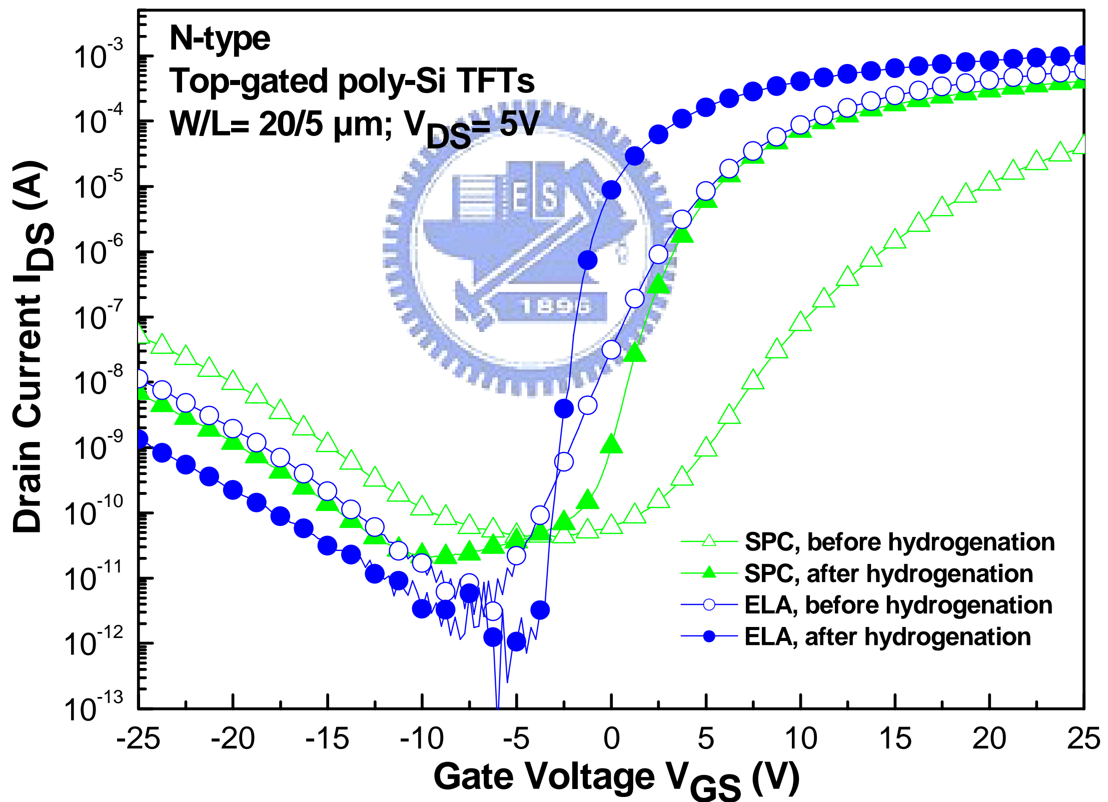
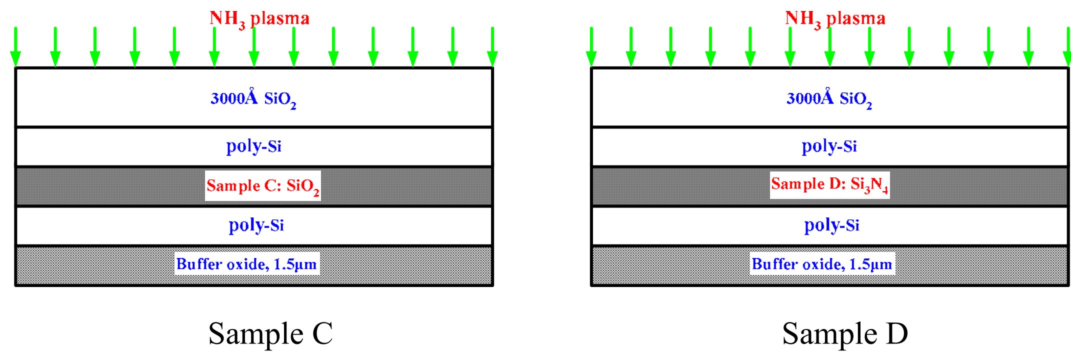


Figure 2.7 (b) Transfer characteristics for comparison of n-type top-gated TFTs before and after hydrogenation at V_{DS}= 5 V. SPC and ELA samples treat 300 min, and 360 min NH_3 plasma passivation, respectively.



Sample C Sample D

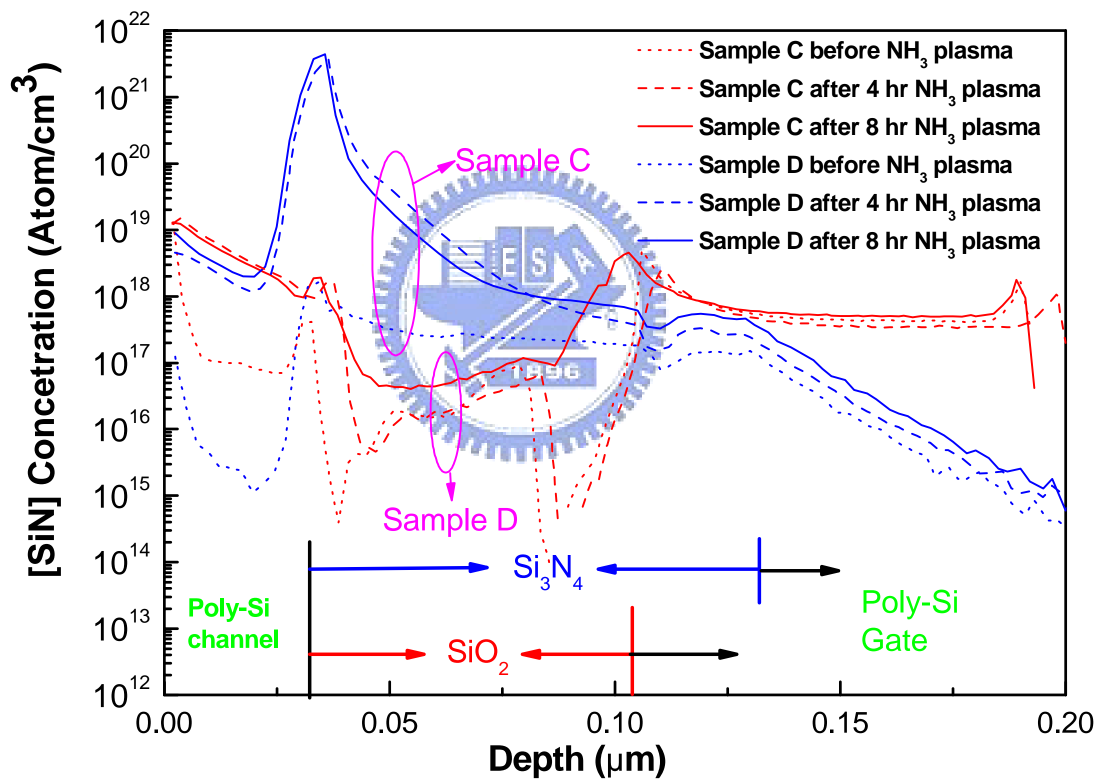
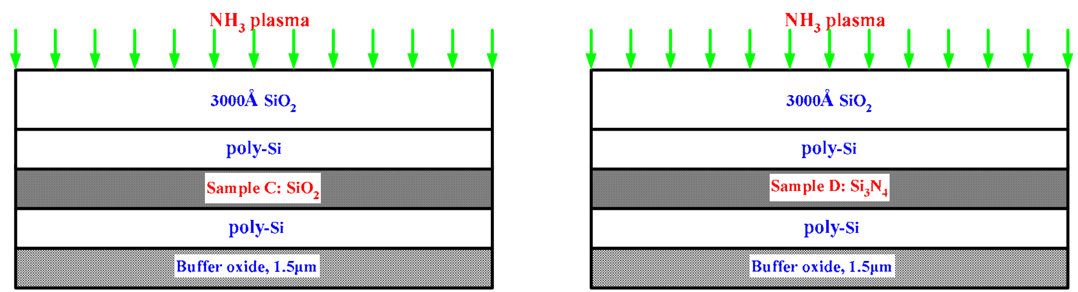


Figure 2.8 (a) The SIMS profiles of SiN for sample C (gate dielectric: SiO_2) and D (gate dielectric: Si_3N_4) with 240 min, and 480 min NH_3 plasma treatment.



Sample C Sample D

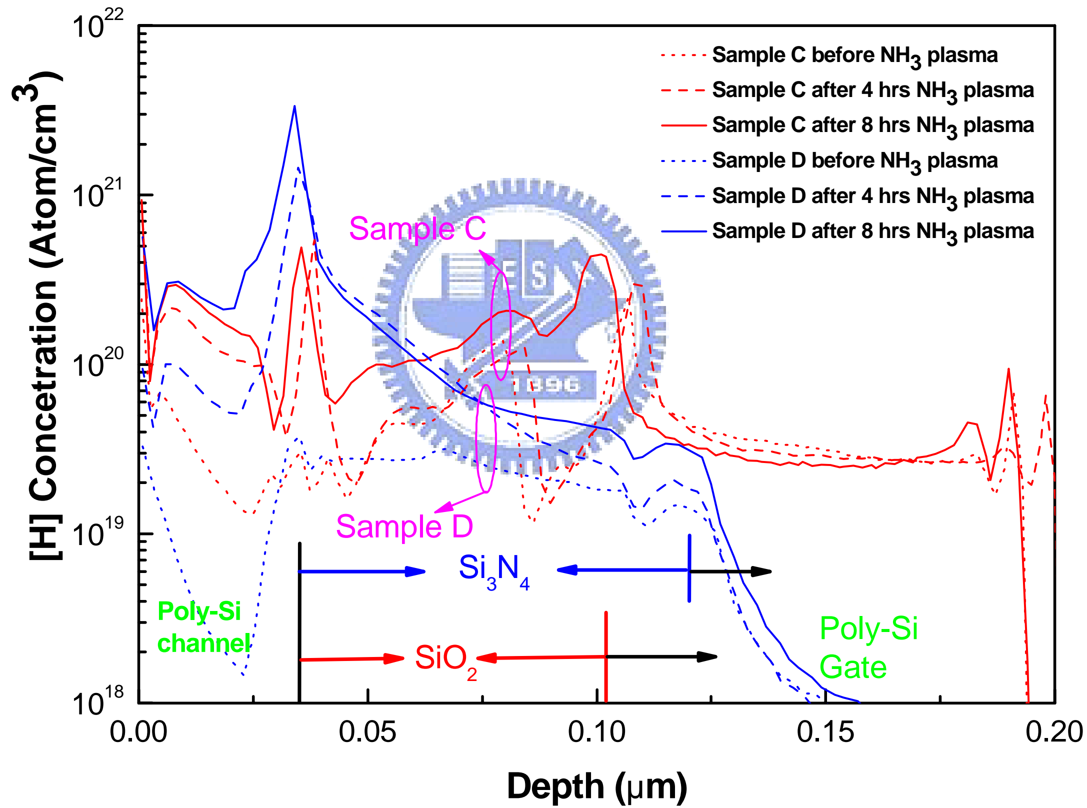
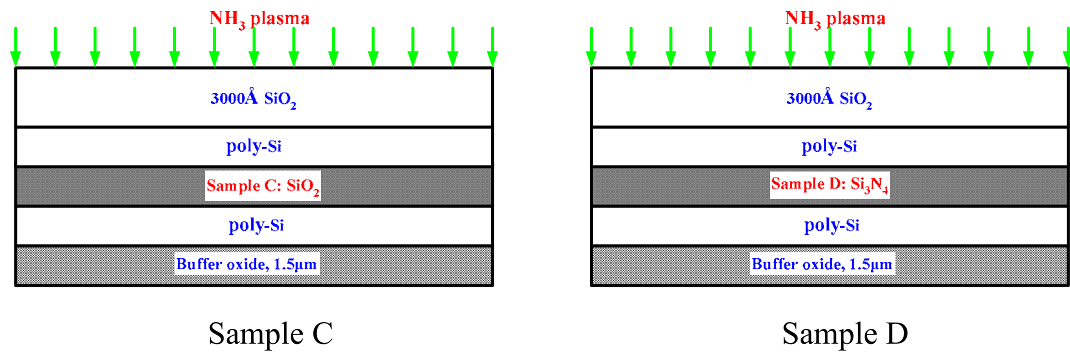


Figure 2.8 (b) The SIMS profiles of hydrogen concentration for sample C (gate dielectric: SiO_2) and D (gate dielectric: Si_3N_4) with 240 min, and 480 min NH_3 plasma treatment.



Sample C   Sample D

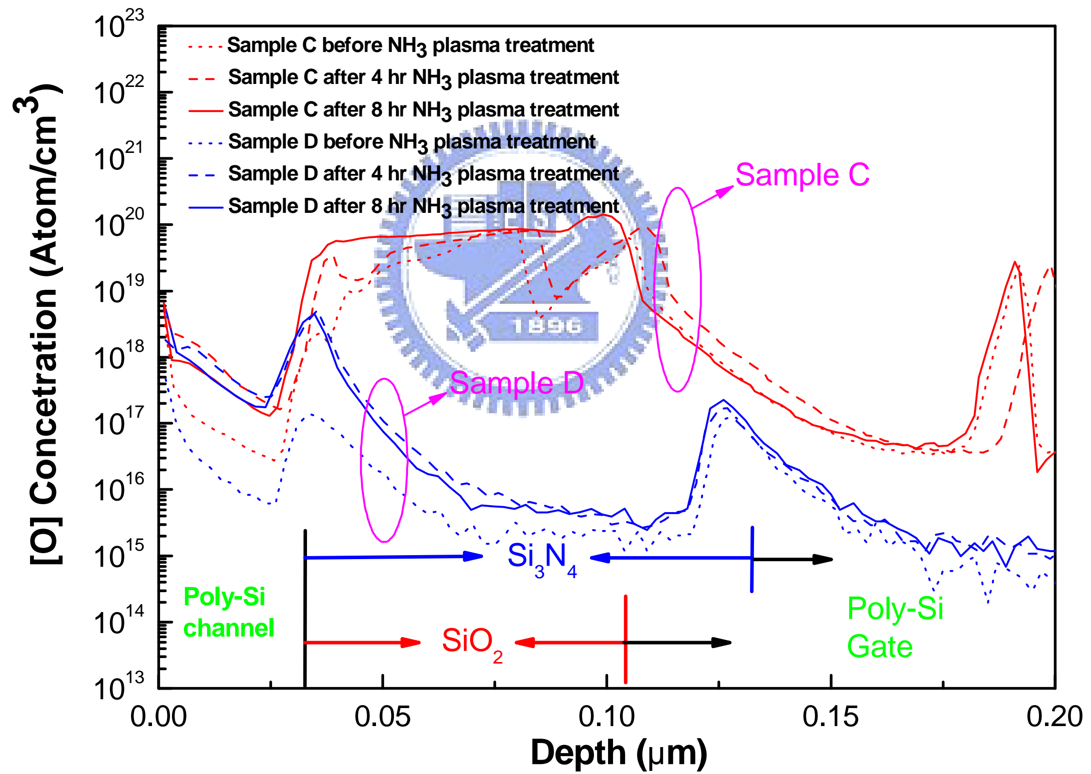
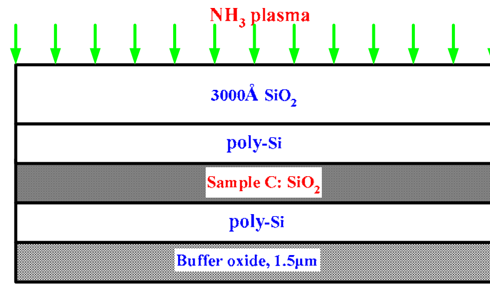


Figure 2.8 (c) The SIMS profiles of oxygen concentration for sample C (gate dielectric: SiO_2) and D (gate dielectric: Si_3N_4) before and after 240 min, and 480 min NH_3 plasma treatment.



Sample C

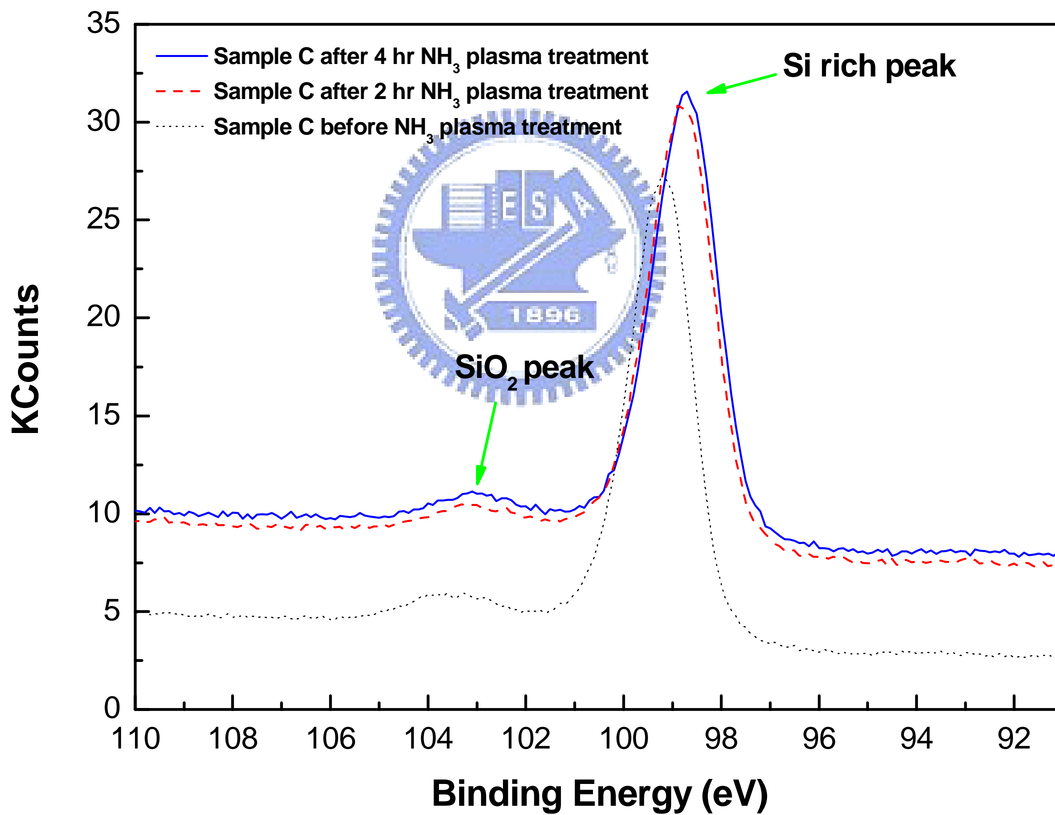
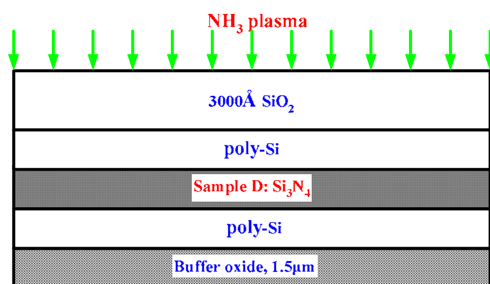


Figure 2.9 (a) The ESCA (XPS) profiles of silicon binding energy for sample C (SiO_2) before and after 120 min, and 480 min NH_3 plasma treatment.



Sample D

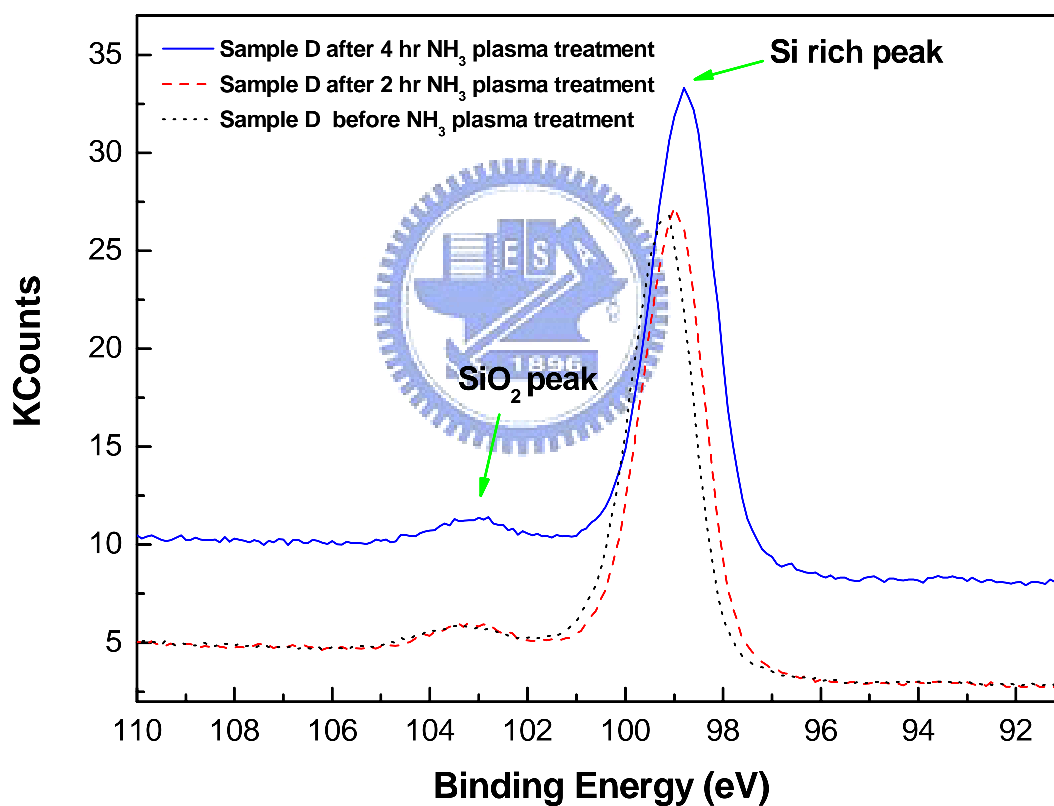


Figure 2.9 (b) The ESCA (XPS) profiles of silicon binding energy for sample D (Si_3N_4) before and after 120 min, and 480 min NH_3 plasma treatment.

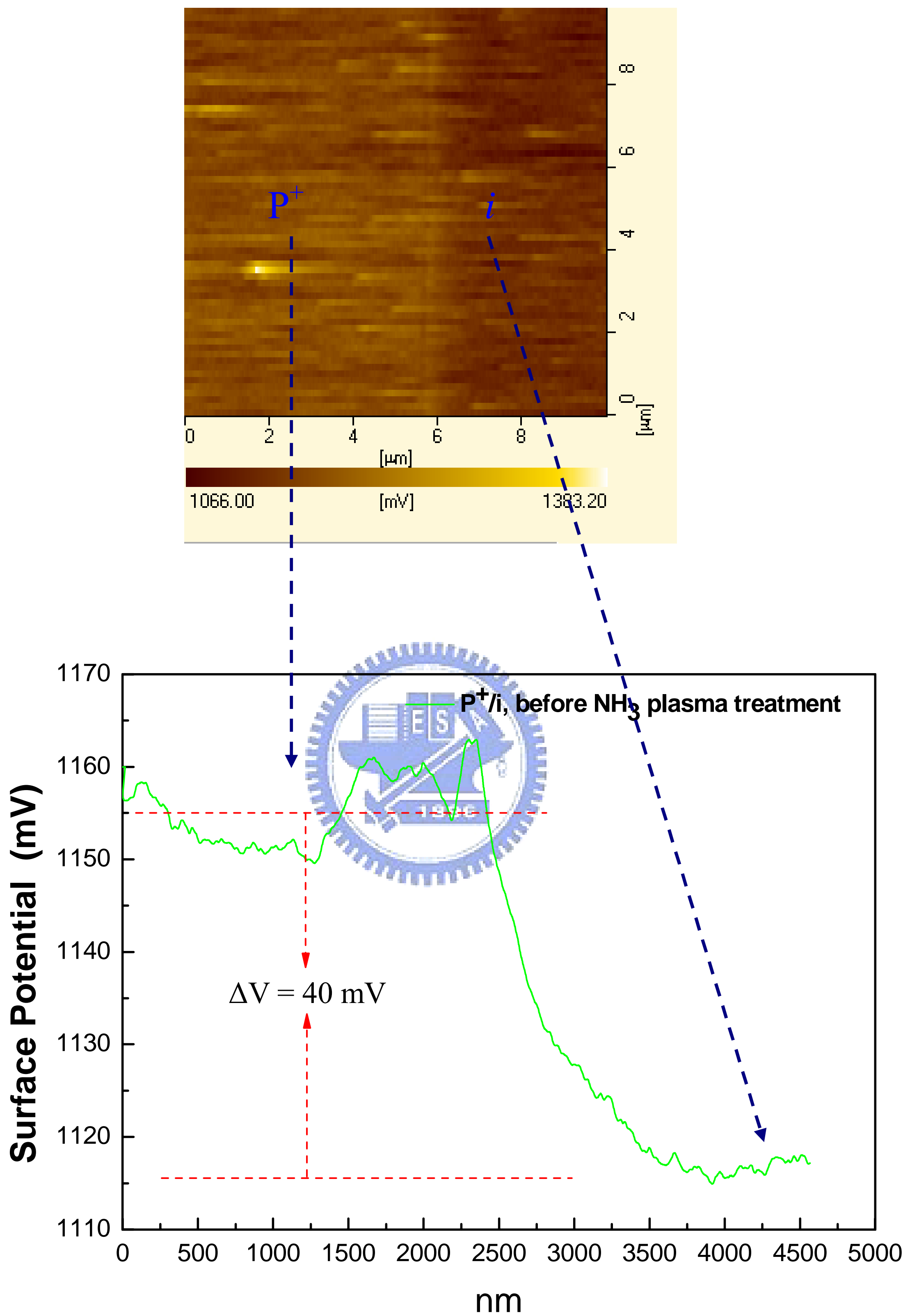


Figure 2.10 (a) The variation of surface potential for sample E (P^+/i junction) before NH_3 plasma treatment was measured by KFM.

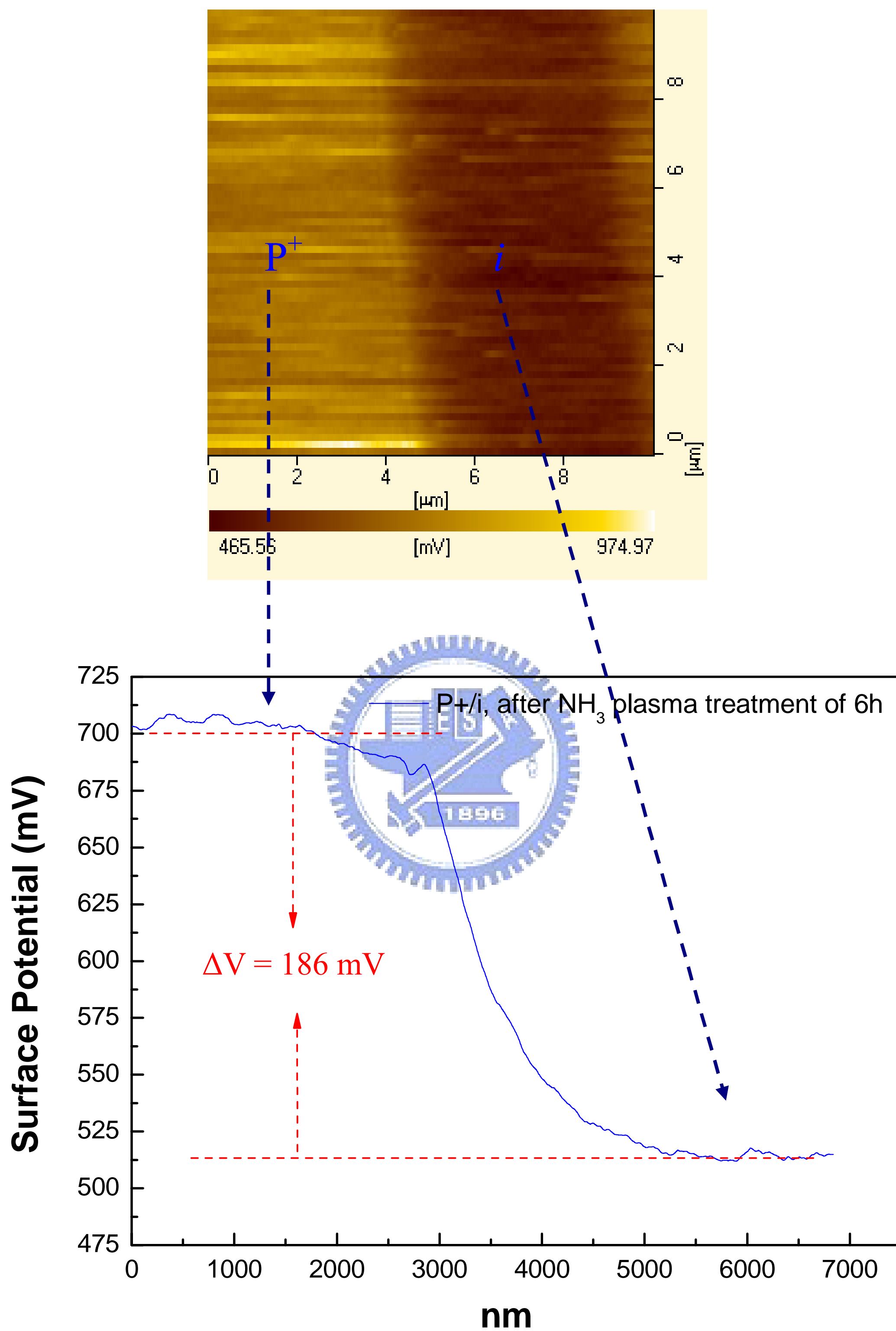


Figure 2.10 (b) The variation of surface potential for sample E (P^+/*i* junction) after NH_3 plasma treatment of 6 h was measured by KFM.

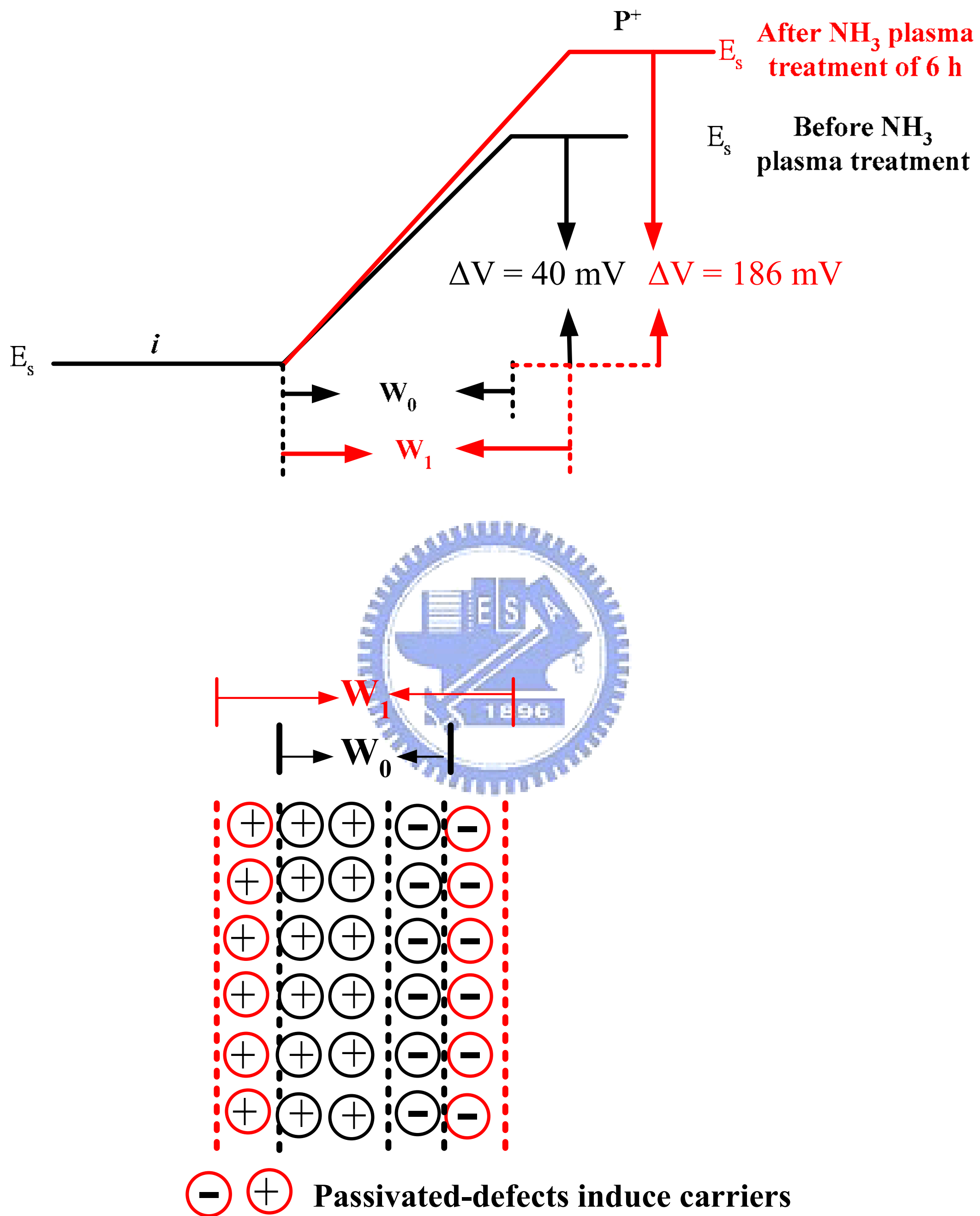


Figure 2.11 Schematic illustrations of defect-reduction in the drain junction.

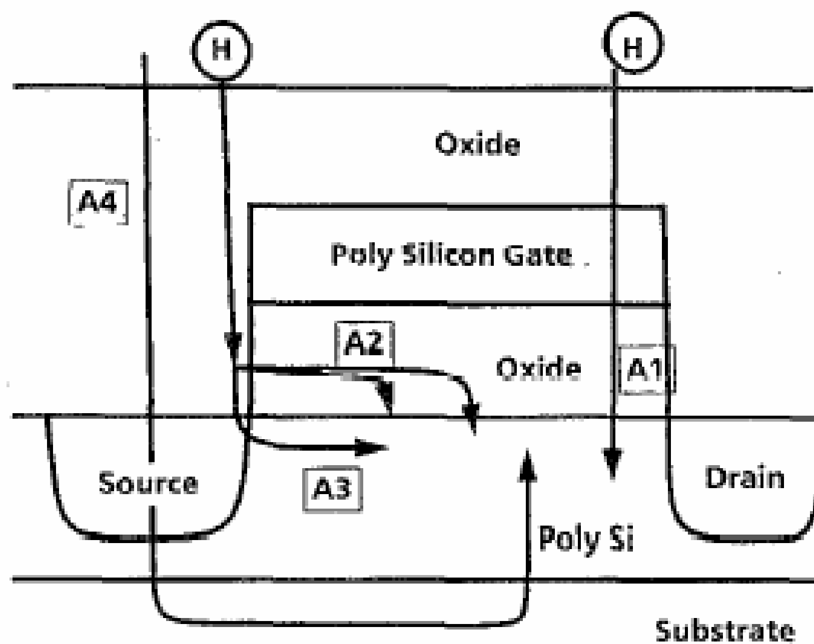
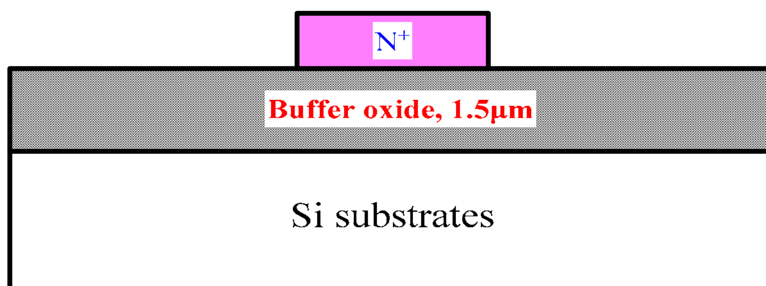
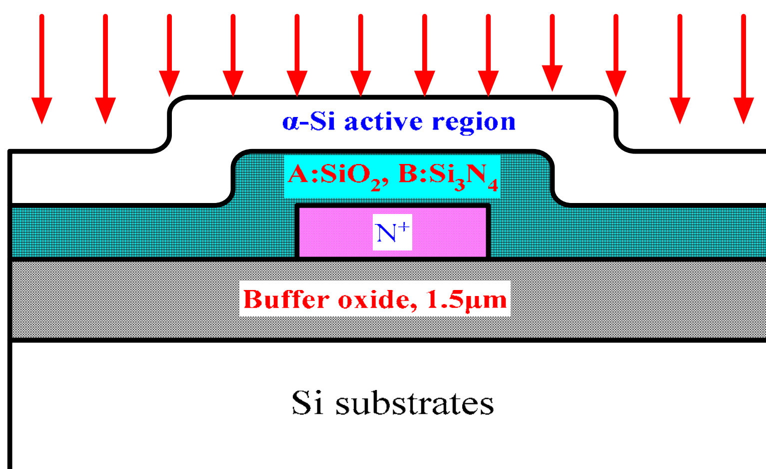


Figure 3.1 Possible pathways for hydrogen migration from a gaseous source to the active channel region of a top-gated poly-Si TFT structure.





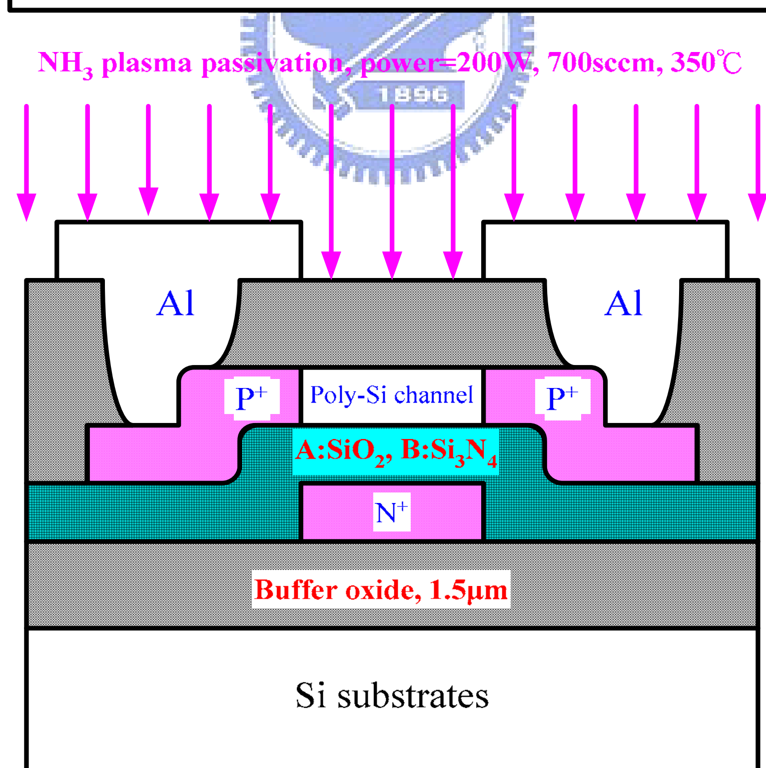
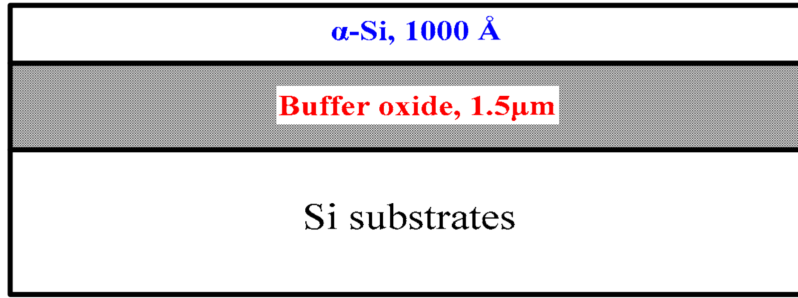
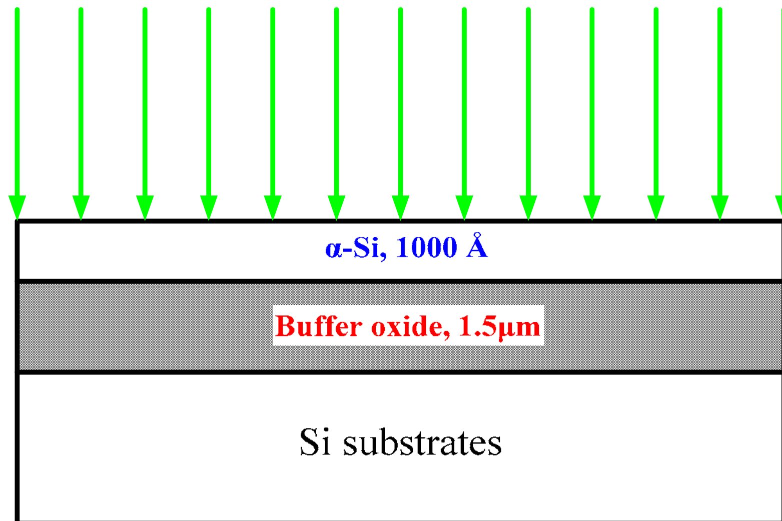


Figure 3.2 Key process flows of the bottom-gated poly-Si TFTs using SPC processes.

Sample D, E, F, and G: deposited α-Si, LPCVD, 1000Å



Sample F, and G: excimer laser annealing



Sample D, and E: annealing at 600℃ for 24 hr

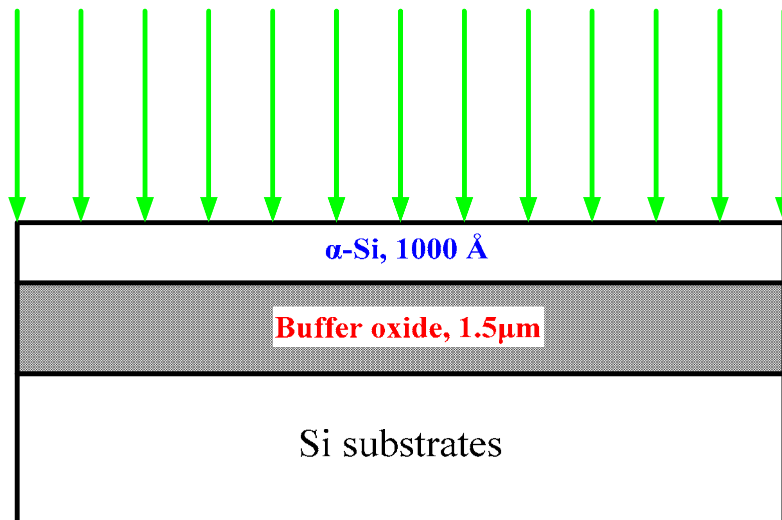
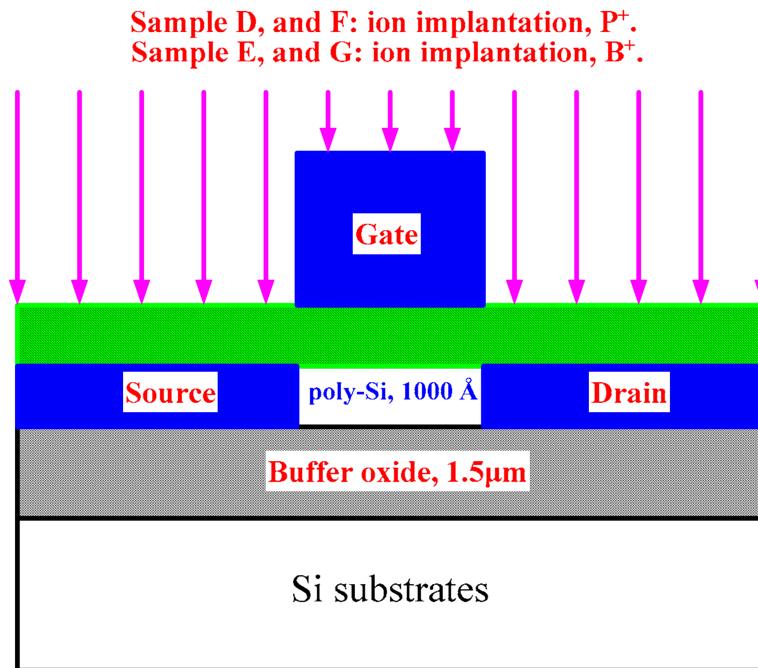


Figure 3.3 Key process flows of the top-gated poly-Si TFTs using SPC/ELA processes.



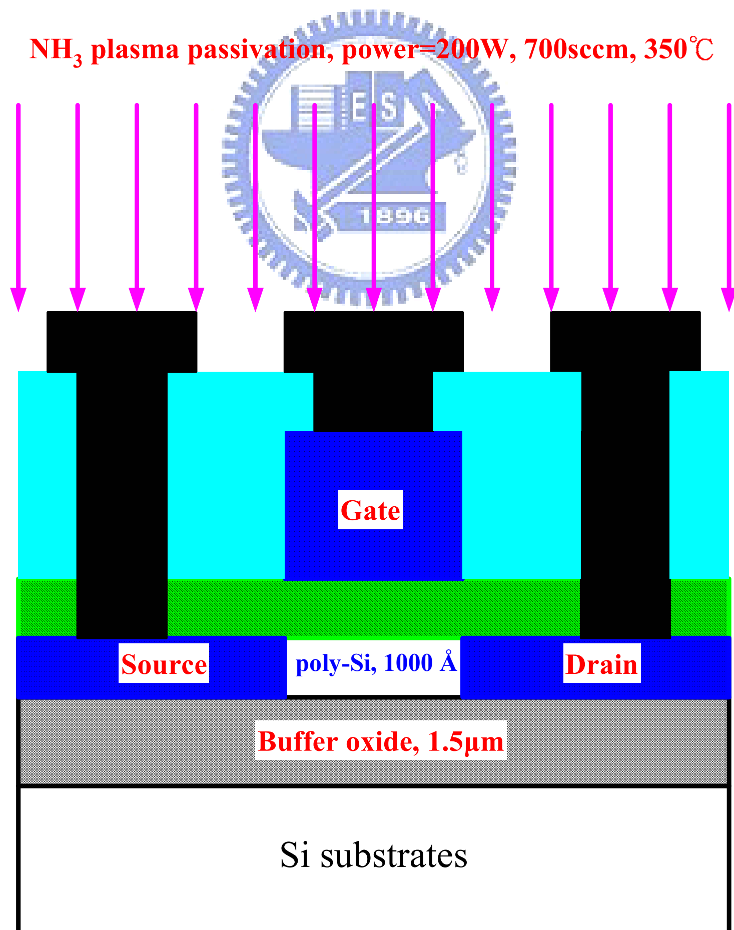
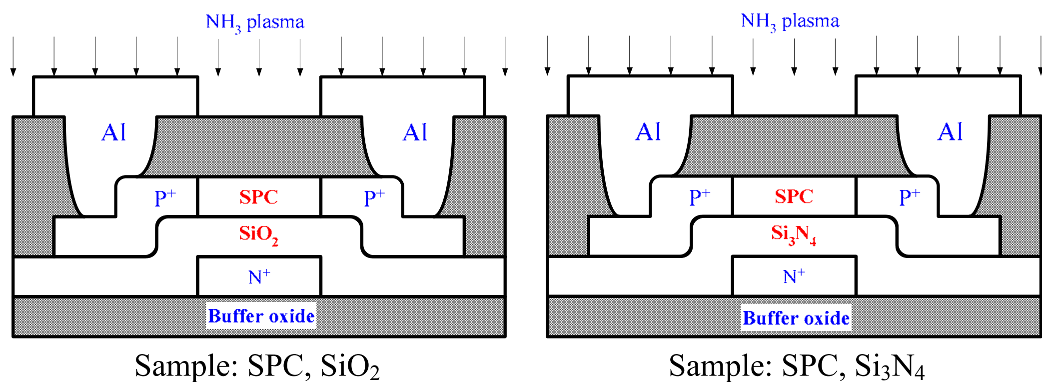


Figure 3.3 Key process flows of the top-gated poly-Si TFTs using SPC/ELA processes.



Sample: SPC, SiO_2 Sample: SPC, Si_3N_4

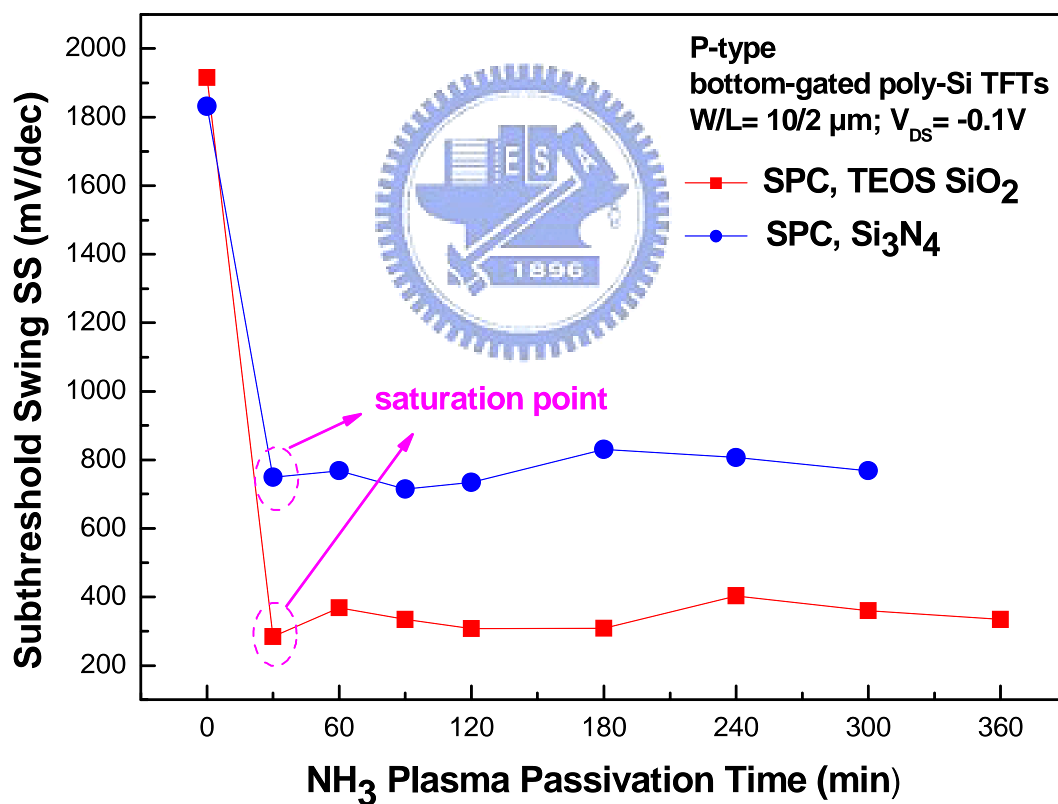
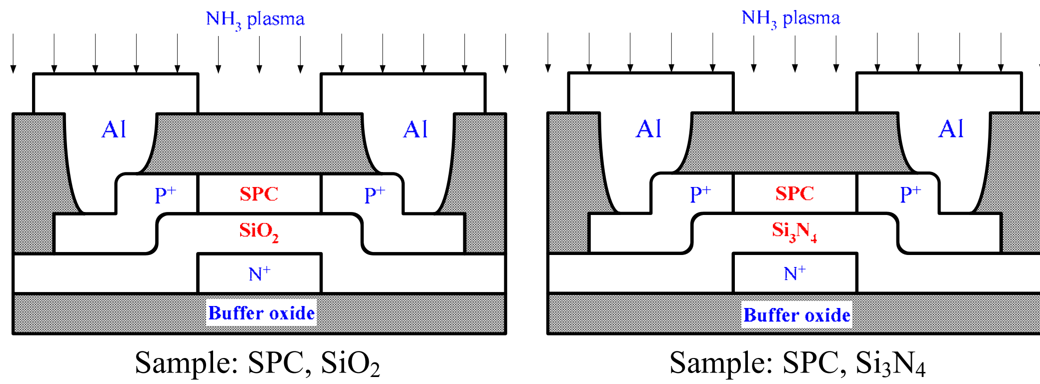


Figure 3.4 Subthreshold Swing determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 10 μm and L= 2 μm p-type bottom-gated poly-TFTs.



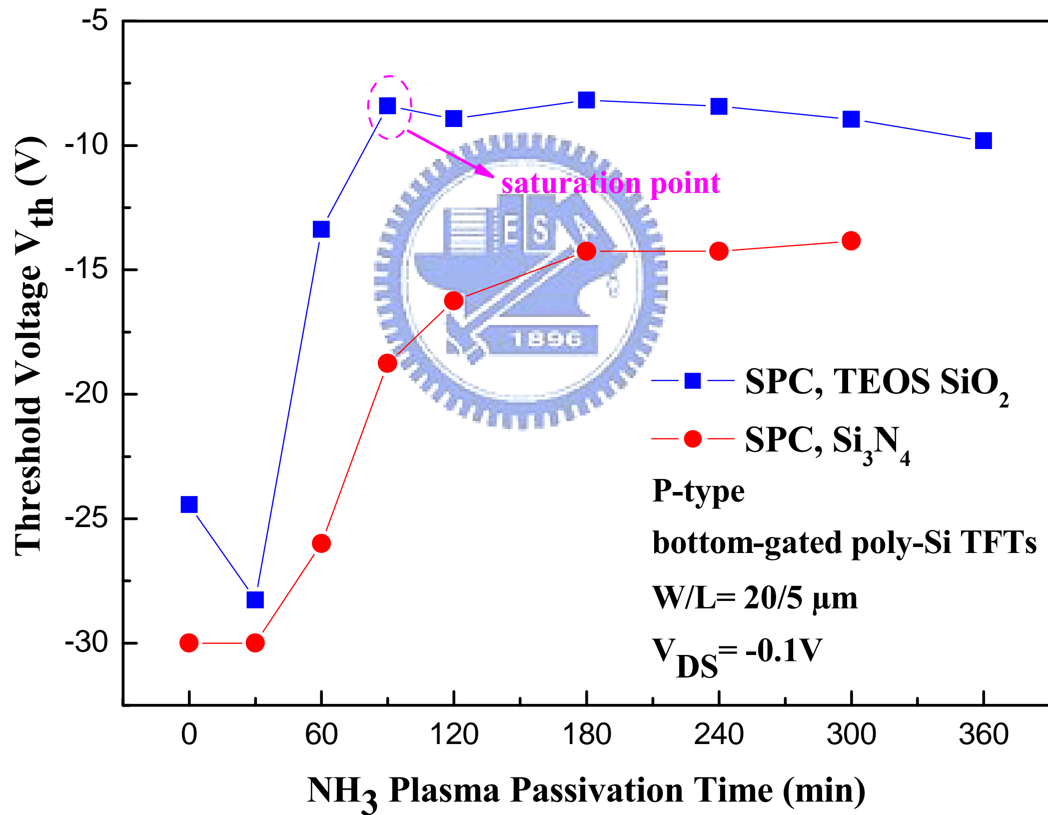
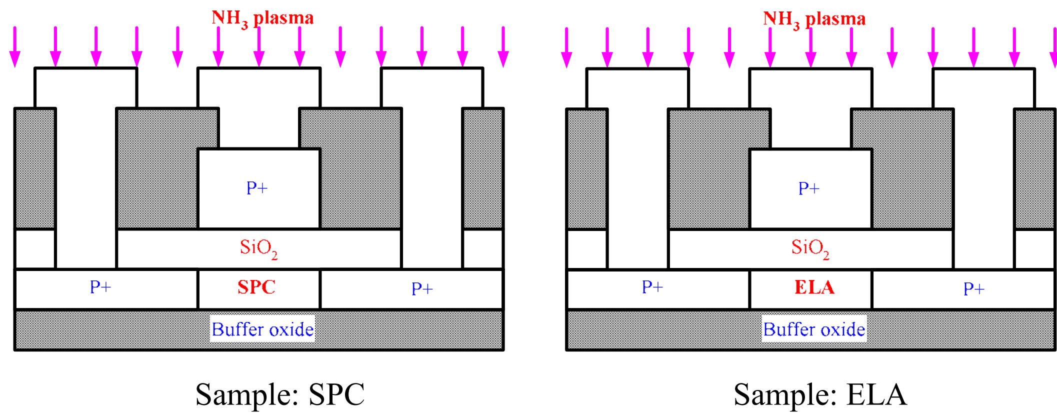


Figure 3.5 (a) Threshold voltage determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20 μm and L= 5 μm p-type bottom-gated poly-TFTs.



Sample: SPC Sample: ELA

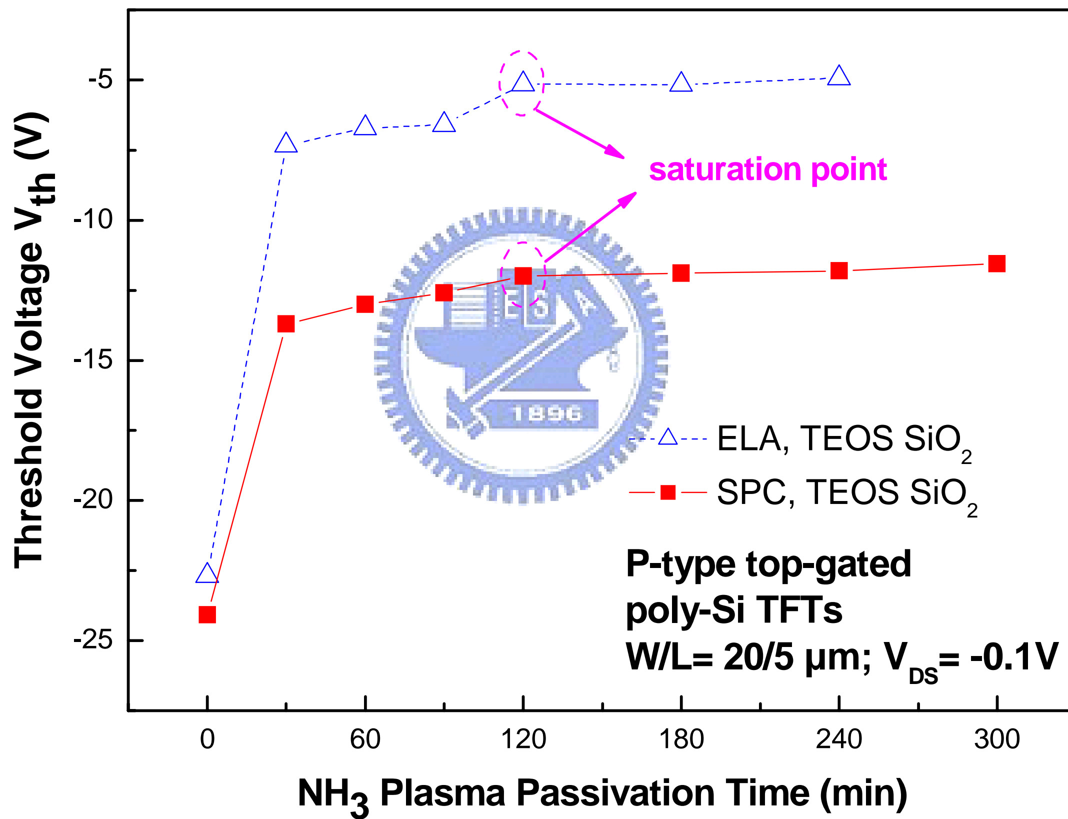
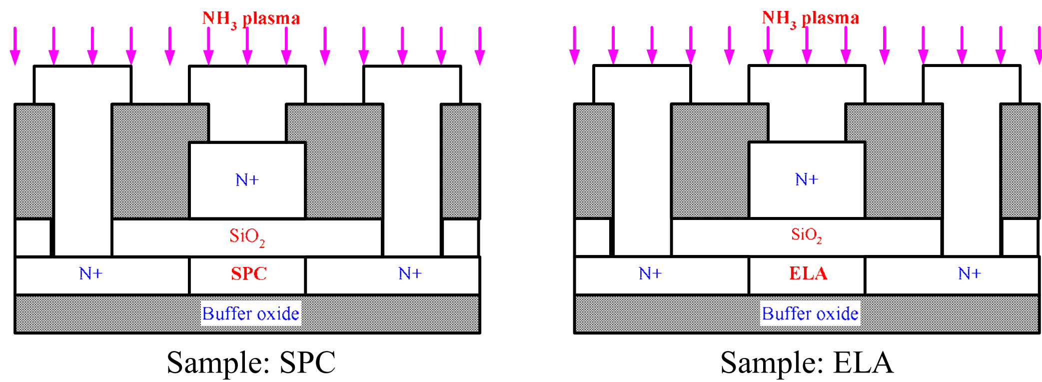


Figure 3.5 (b) Threshold voltage determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 5 μm p-type top-gated poly-TFTs.



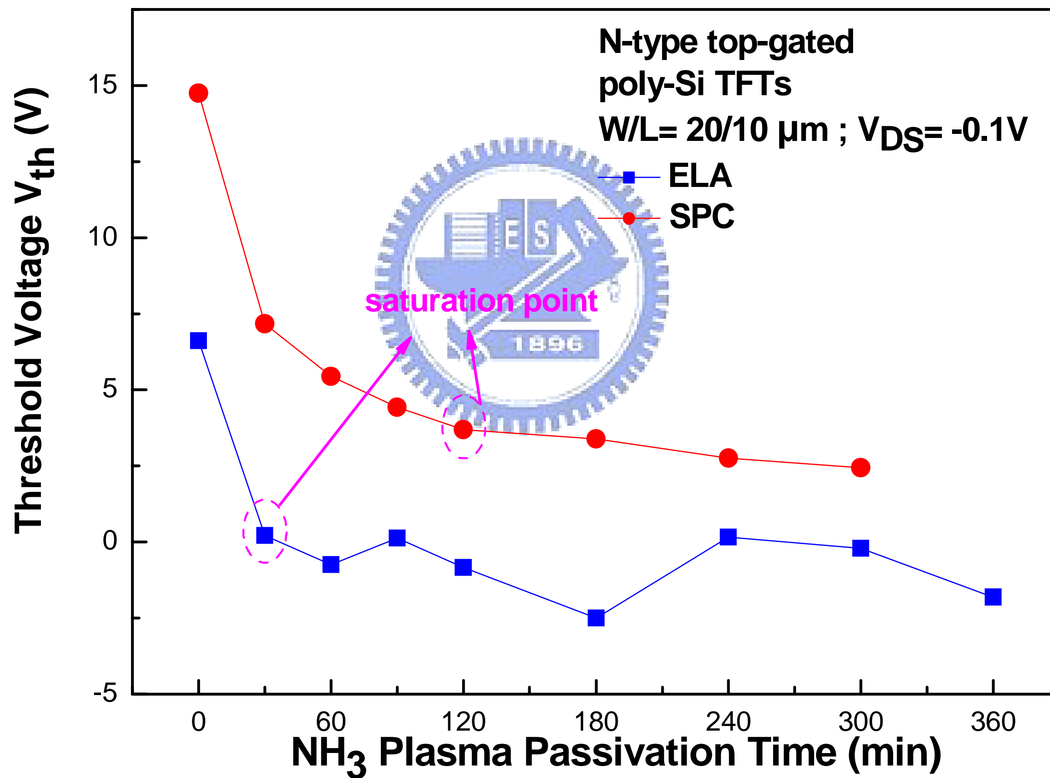
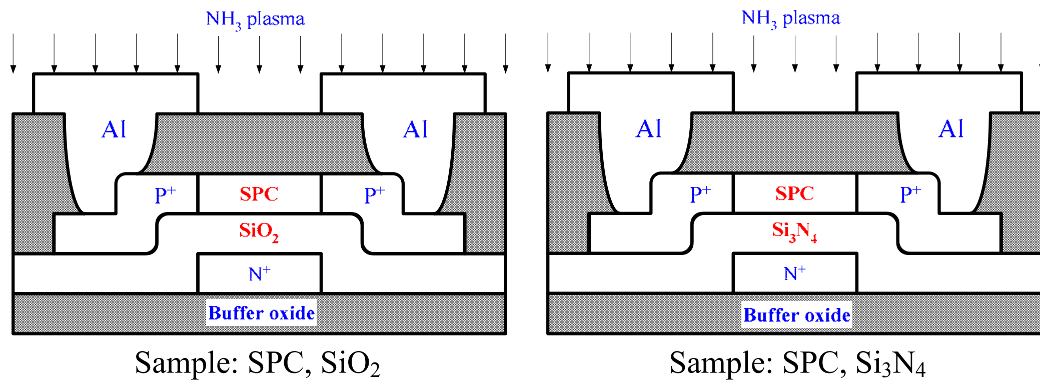


Figure 3.5 (c) Threshold voltage determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 10μm n-type poly-TFTs.



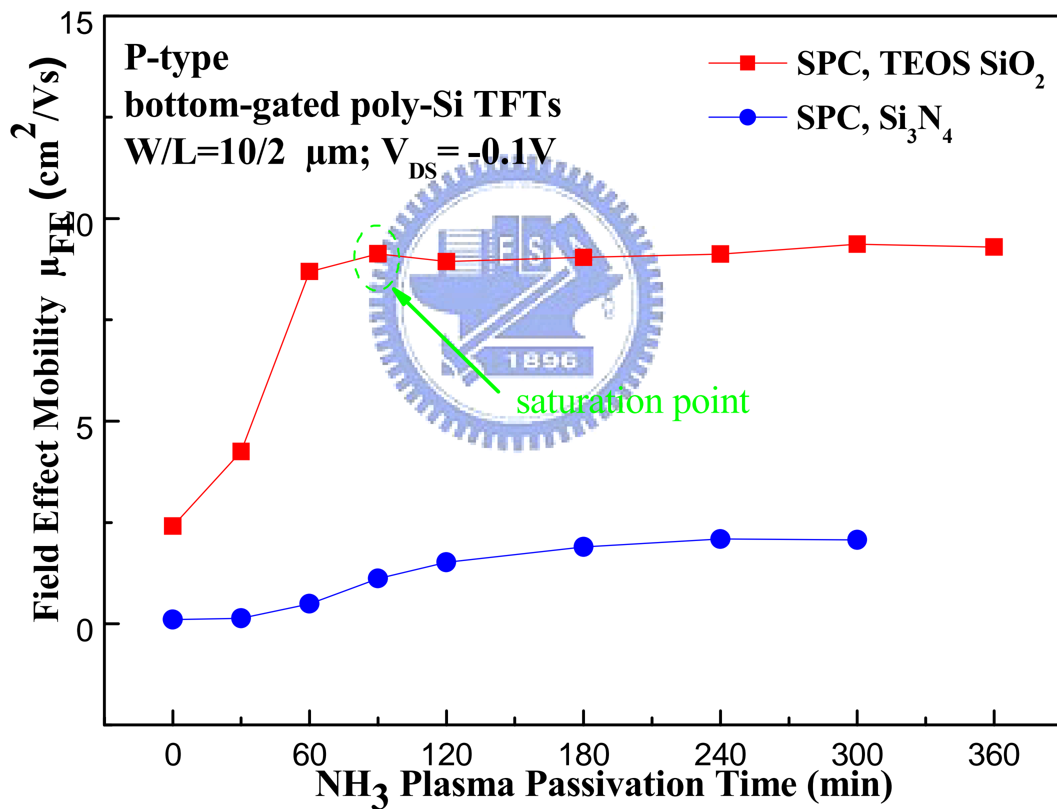
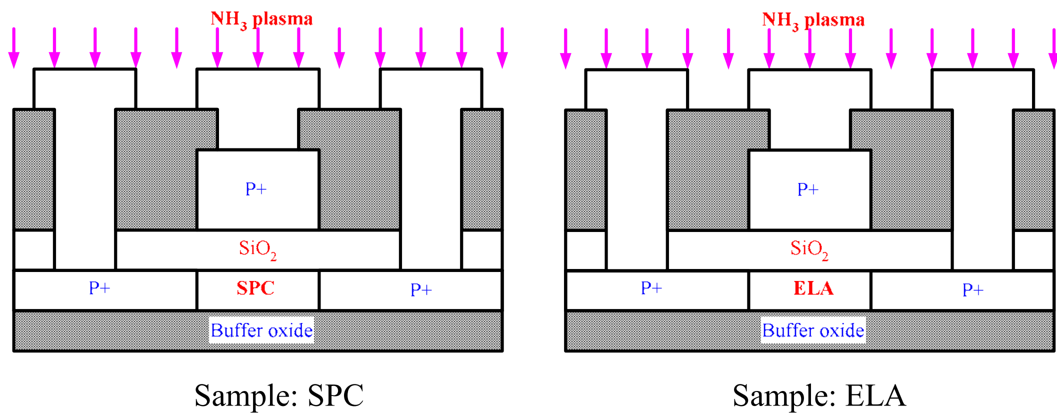


Figure 3.6 (a) Mobility determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 10μm and L= 2 μm p-type bottom-gated poly-TFTs.



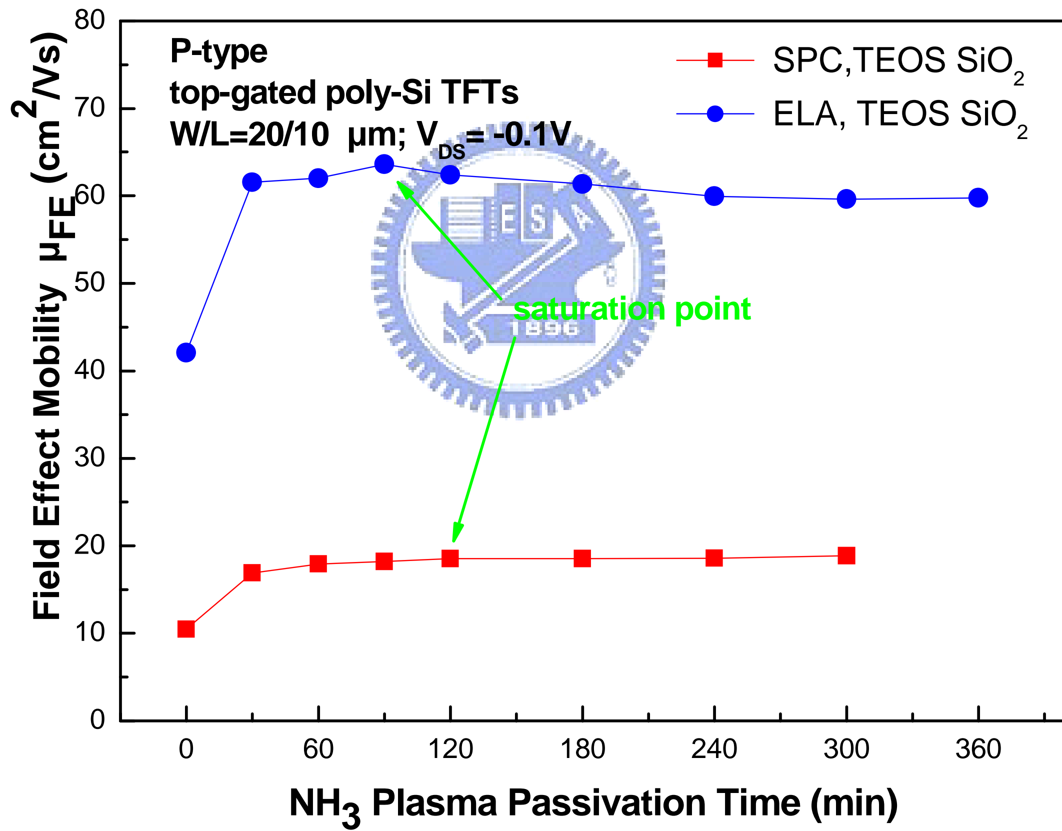
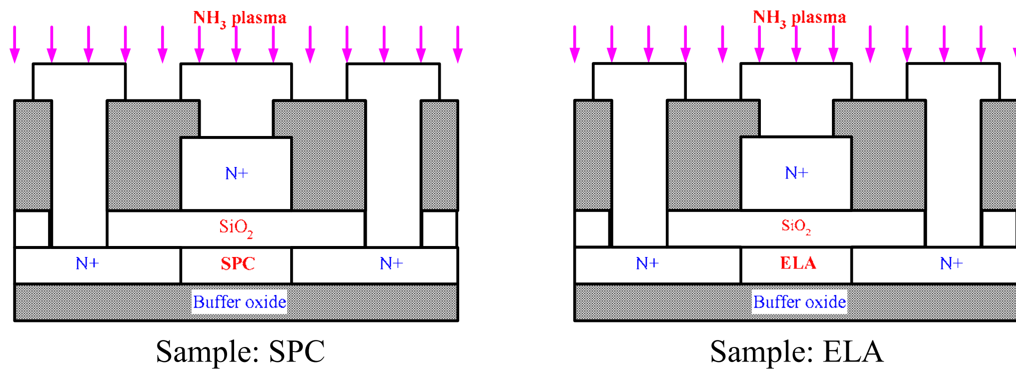


Figure 3.6 (b) Mobility determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 10 μm p-type top-gated poly-TFTs.



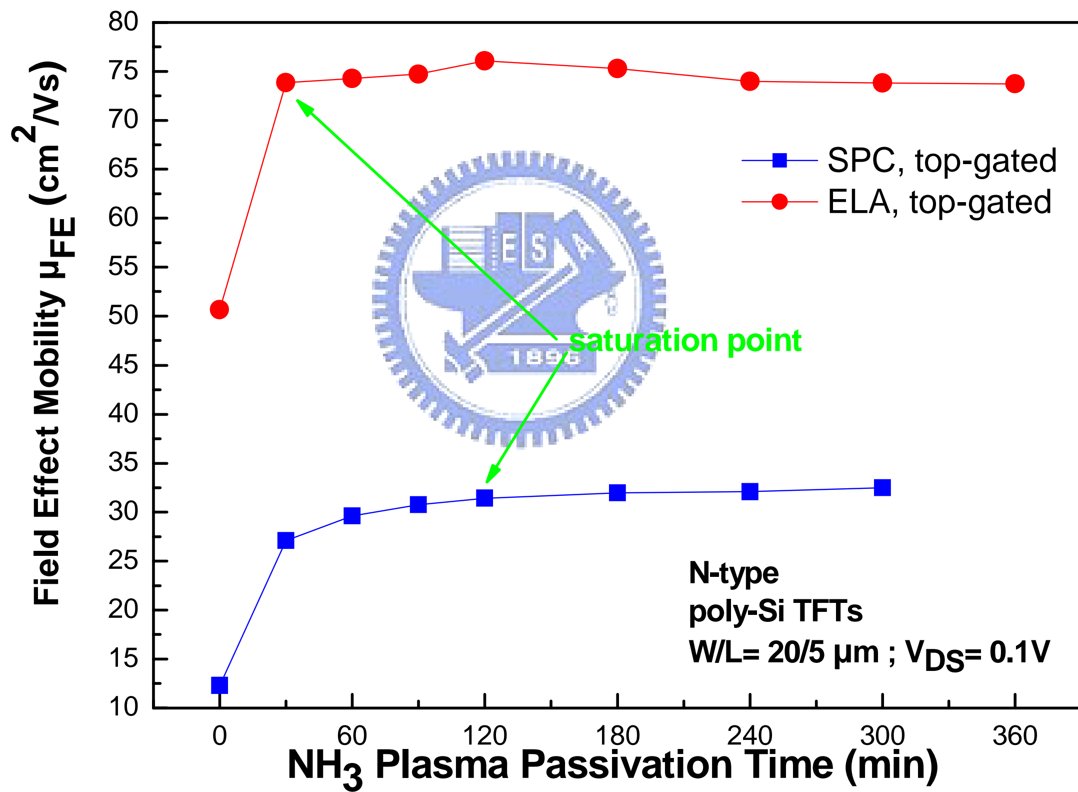
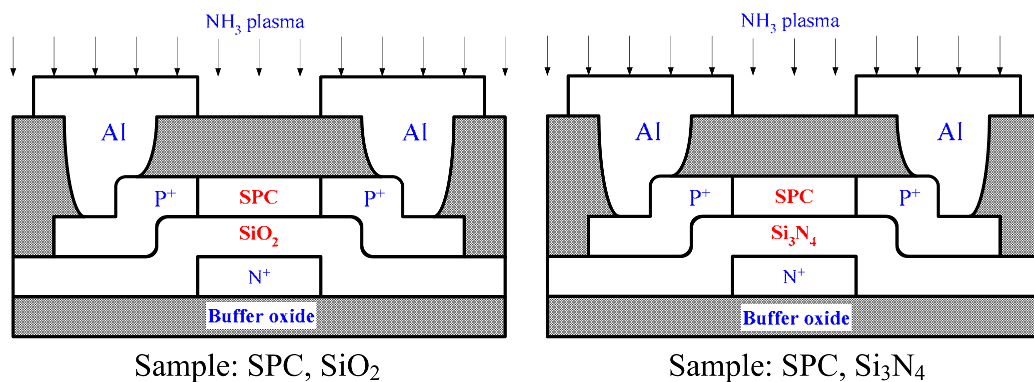


Figure 3.6 (c) Mobility determined at V_{DS}= 0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 5 μm n-type poly-TFTs.



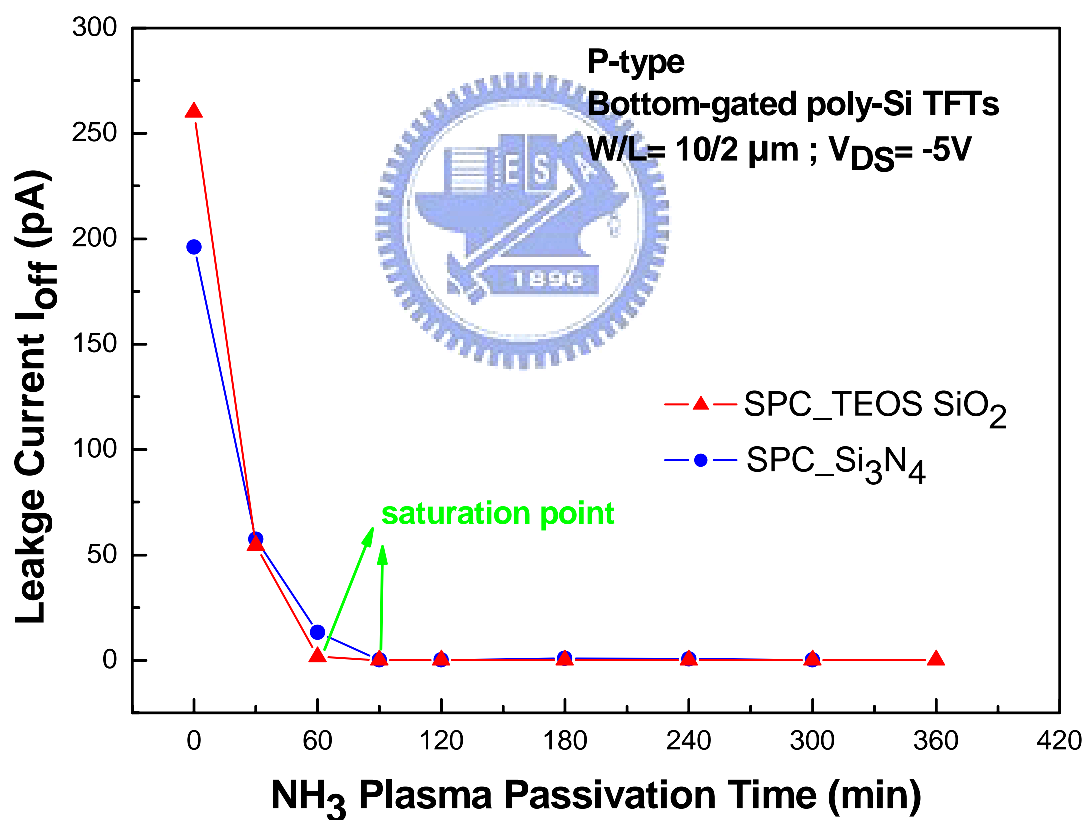
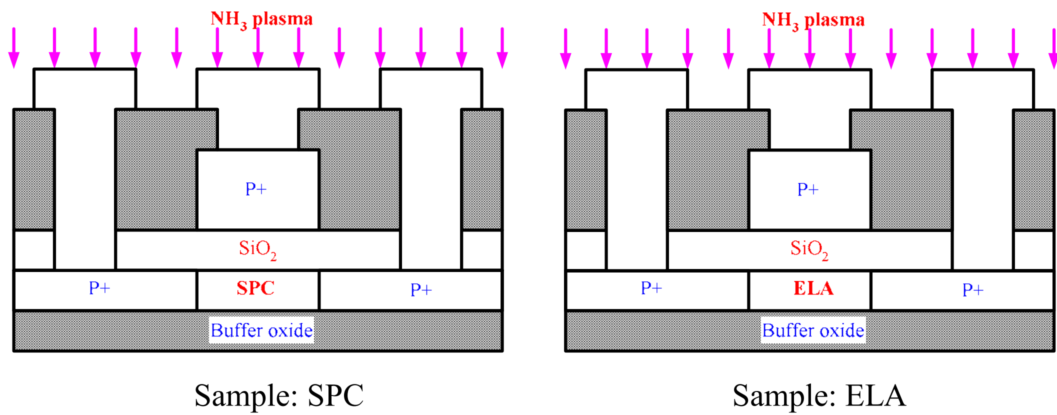


Figure 3.7 (a) The leakage currrent determined at V_{DS}= -5V as function of NH_3 plasma passivation time for W= 10μm and L= 2 μm p-type bottom-gated poly-TFTs.



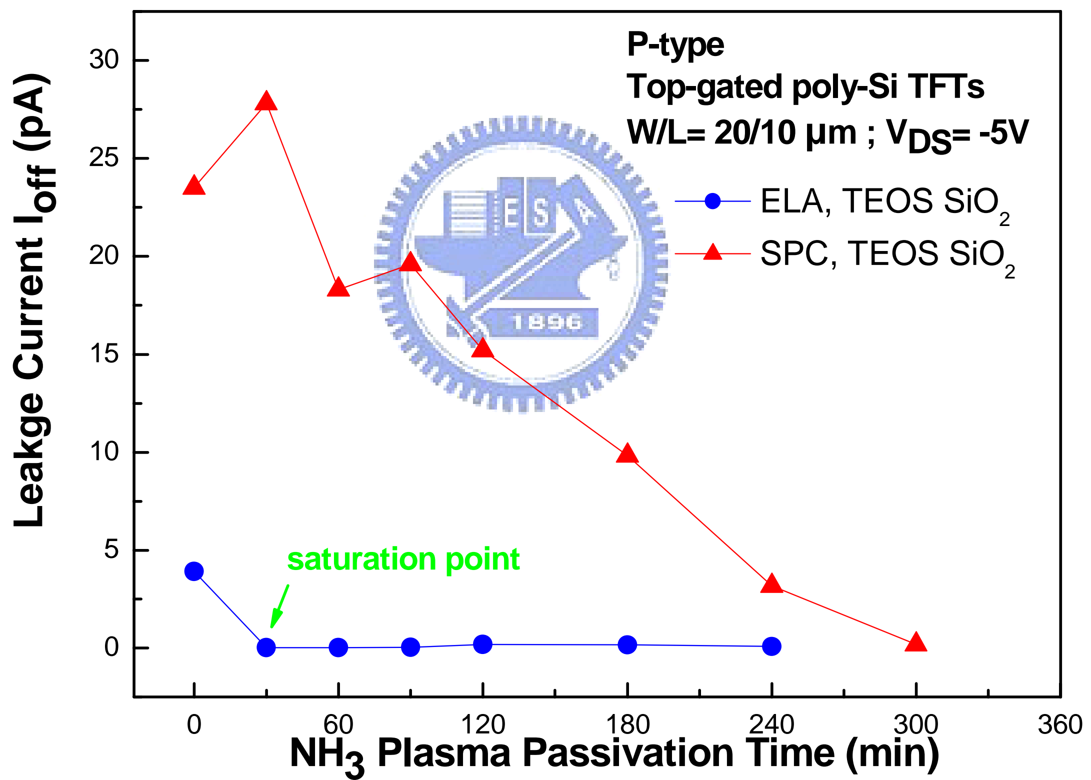
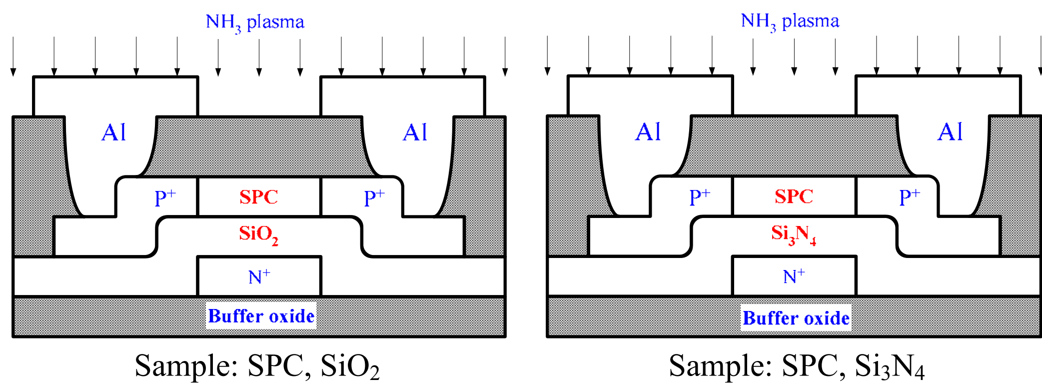


Figure 3.7 (b) The leakage currrent determined at V_{DS}= -5V as function of NH_3 plasma passivation time for W= 20μm and L= 10 μm p-type top-gated poly-TFTs.



Sample: SPC, SiO_2 Sample: SPC, Si_3N_4

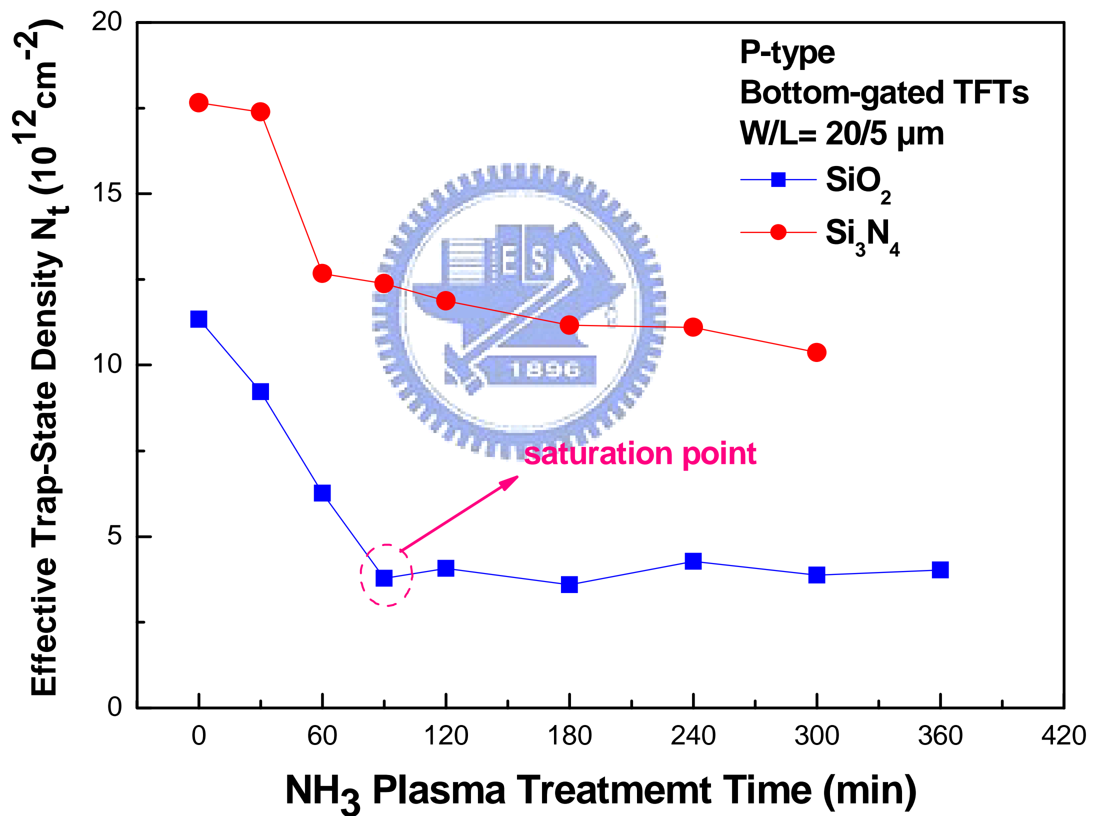
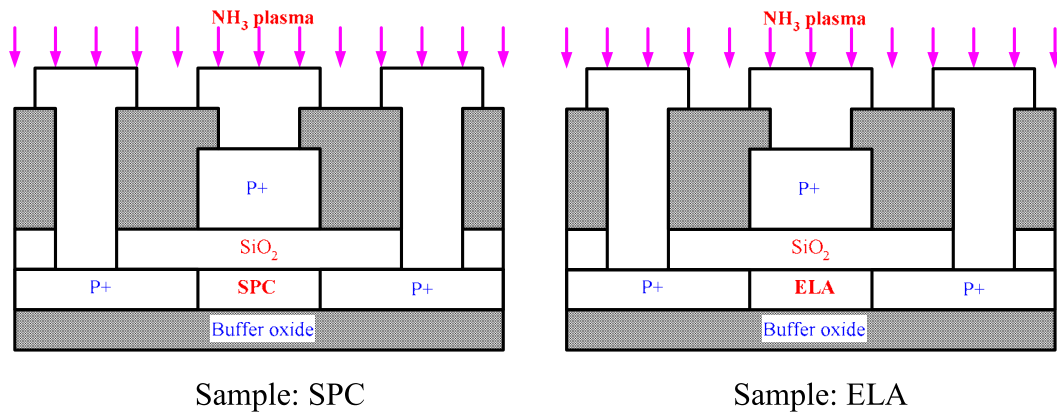


Figure 3.8 (a) Effective trap density determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 5 μm p-type bottom-gated poly-TFTs.



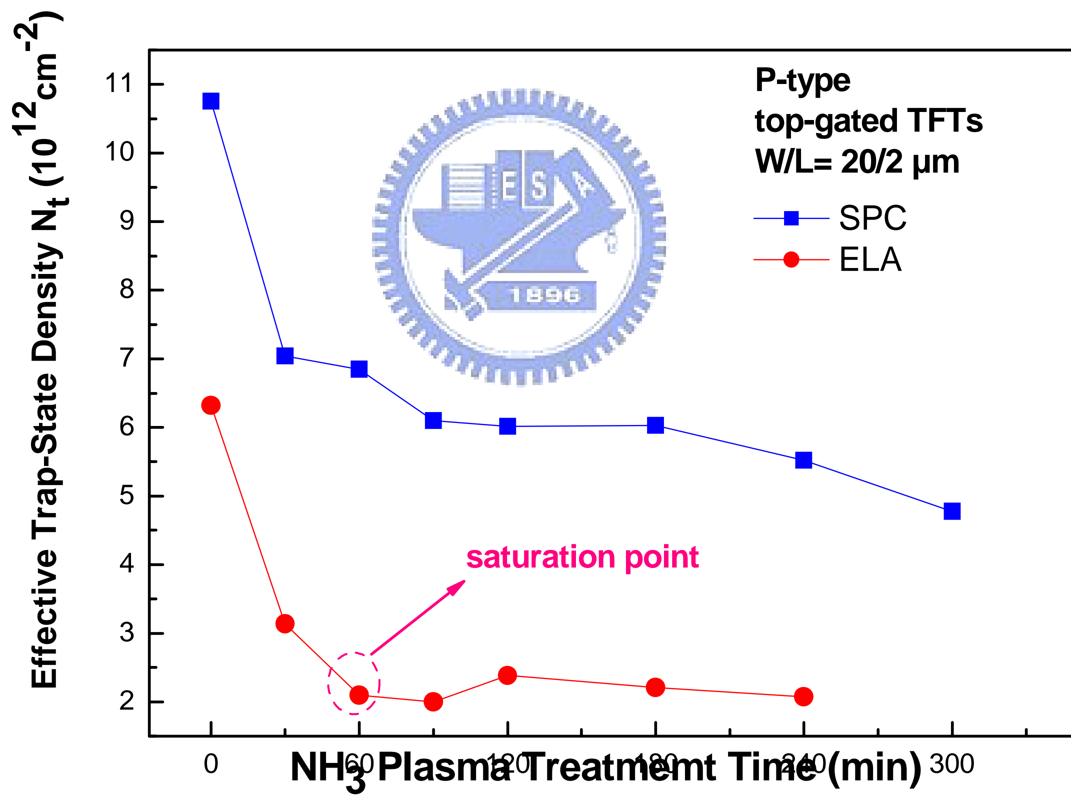


Figure 3.8 (b) Effective trap density determined at V_{DS}= -0.1V as function of NH_3 plasma passivation time for W= 20μm and L= 2 μm p-type top-gated poly-TFTs.

Publications

1. Tien-Fu Chen, Ching-Fa Yeh, **Chun-Yen Liu**, and Jen-Chung Lou, ”A novel crystallization method for fabrication high-performance poly-Si thin film transistors,” *EDMS*, p. 913, Nov. 21-22 2003.

2. Tien-Fu Chen, Ching-Fa Yeh, **Chun-Yen Liu**, and Jen-Chung Lou, “A Novel Four-Mask-Processed Poly-Si TFT Fabricated Using Excimer Laser Crystallization of an Edge-Thickened _-Si Active Island,” *IEEE, electron Device Letters*, vol. 25, p. 396, 2004.

Vita

Chun-Yen Liu was born on September 5, 1975 in Hsin-Chu County, Taiwan, R. O. C.. He received the B.S. degree in civil engineering at Chung-Yuan Christian University (CYCU), Chung-Li, Taiwan, R. O. C., in 1997. He is currently working toward the M.S. degree in Electronic Engineering at Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, R. O. C.. The topic of this thesis is **"**Influences of Various NH3-plasma-passivation Time on the Performance of P-channel Poly-Si Thin Film Transistors".