國立交通大學

電子工程學系電子研究所碩士班

碩士論文

一種分析薄膜電晶體內完整能帶隙態位密度分佈的新穎方法

A NOVEL METHOD TO ANALYZE FULL BAND-GAP DENSITY OF STATES DISTRIBUTION IN THIN FILM TRANSISTORS

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摘　　要

在本篇論文中，我們提出一種創新的分析薄膜電晶體通道層內能帶隙態位密度(DOS)分佈的方法，利用此方法我們可以在單一元件中一次求得全能帶隙的態位密度分佈，不僅簡化量測與分析程序，同時也大幅降低製造成本與分析時間。

傳統若要求得全能帶隙缺陷密度分佈，必須分別製作 N 型和 P 型的薄膜電晶體才能獲得。在本論文中，我們利用一種具有電場感應汲極之蕭特基薄膜電晶體元件，可以實現完整能帶隙之薄膜態位密度分析。由於電場感應汲極之蕭特基薄膜電晶體在靠近汲極端有一電性接面(electrical junction)區，利用其上方的副閘極的偏壓可以感應出不同極性的電性接面，並藉此使單一元件可變換地操作在 N 或 P

通道模式。利用此一雙向操作(ambipolar)能力，再結合場效電導(field effect conductance)法，可以在單一元件中求出費米能階上、下的完整能帶隙缺陷密度分佈，而不必分別製作 N 及 P 通道模式的元件，如此將可大幅降低製作成本，並增加分析便利性。

此外，我們也在實驗中發現，在室溫下量測 N 通道和 P 通道的源極電流與閘極電壓特性，其交叉點的閘極電壓與傳統利用變溫方法求得的平帶電壓(flat-band voltage)幾為一致。經由實驗中不同製程與結構的元件一再的比對，均證實此現象的存在，因此我們提出利用此方式量測通道層內的平帶電壓，如此將可避免傳統變溫方法的耗時與繁複，大幅簡化程序並節省時間。

利用此方法，我們可以分析在不同的製程條件下薄膜的缺陷密度分佈。由於薄膜電晶體的電特性強烈受到通道中缺陷態位密度的影響。因此，透過我們提出的方法，能讓我們對薄膜電晶體的元件特性有更深入的瞭解，也有助於業界量產所須對薄膜電晶體元件的模式分析及電路設計與模擬的工作。

A novel method to analyze full-band gap state density distribution in thin film transistors

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Abstract

In this thesis, we propose a novel method to acquire the full band-gap density-of-state (DOS) in the channel layer of a thin-film transistor (TFT). In this new approach, only a single Schottky barrier thin-film transistor (SB-TFT) device is characterized, in contrast to the conventional methods that require both n- and p-channel devices for characterization. In a SB-TFT with field-induced drain (FID), an electrical drain junction is set between the channel portion underneath the main-gate and the metallic drain. A sub-gate lying above the electrical drain junction is used to adjust the polarity and resistance of the electrical junction, enabling the ambipolar operation of the device. Field-effect conductance (FEC) method is applied to analyze the ambipolar subthreshold current-voltage characteristics and acquire full band-gap DOS.

Experimentally, we have also observed that the gate voltage at the intersection point of n- and p-channel subthreshold current-voltage characteristics coincides well

with the flat-band voltage measured using the conventional temperature method. We thus propose to exploit this new finding, in lieu of the conventional method, to extract the flat-band voltage, which further simplify our methodology, as only two current-voltage measurements at room temperature are needed for the construction of full band-gap DOS.

Our proposed method has been demonstrated to be useful on characterizing and understanding the impacts of different process treatments on the device characteristics. Accompanied with its simplicity and significant saving of both analysis cost and time, this method could be vital to TFT device modeling and circuit simulation works for both R&D and practical manufacturing.

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Contents

Table Captions

Figure Captions

List of symbols

E	Energy
d	Polysilicon thickness
E_F	Fermi energy
k	Boltzmann constant
n	electron concentration
n_0	Equilibrium electron concentration
Ng(E)	Density of gap states (DOS)
q	Electronic charge
t_{ox}	Gate dielectric thickness
Xo	Unmodulated bulk length (or depletion width in the channel)
k	Boltzmann constant
T	Temperature (K)
V_{FB}	Flat band voltage
V_G	Gate voltage
Vth	Threshold voltage
ε_{ox}	Gate dielectric constant
ε_{si}	Silicon dielectric constant
μ	Electron mobility
ϕ	band bending
ϕ s	surface band bending of the channel
ρ	charge density
G	conductance
G_0	conductance at flat band condition

Chapter 1

Introduction

1.1 Background and motivation

Thin-film transistors (TFT), which employ a thin semiconductor film on an insulating substrate as the active device channel, was first demonstrated in 1961 by Dr. P. K. Weimer in RCA. With its simplicity in structure and fabrication, applications of thin-film transistors in image sensors and displays become more and more popular. Interest in low temperature poly-Si TFT has been growing rapidly over the last decade. This is due to a much higher mobility and drive current of poly-Si TFTs, compared to amorphous Si counterparts, which enables the integration of peripheral circuits on the same panel in active matrix liquid crystal displays (AMLCD) manufacturing [1].

The electrical properties of polycrystalline semiconductor devices are strongly affected by defects such as dangling bonds and strained bonds located at the grain boundaries [2-3]. An understanding of the nature, energy distribution, density, and behavior of these defects is important for the development of polycrystalline TFTs. Several approaches have been developed to determine the density of gap states (DOS) in polycrystalline devices, such as capacitance-voltage method [4], the doping dependence of conductivity [5], and the field effect conductance (FEC) method [6-7]. Among them, only the field effect conductance method is compatible with modern poly-Si TFT samples. A theoretical interpretation of the field effect conductance method was given by Suziki et al [8] to calculate the DOS of amorphous Si TFTs [9]. The technique has been extensively applied to a-Si:H devices and provides adequate information on the DOS in spite of some interpretation difficulties, such as the

differentiation between bulk and interface states. In the case of poly-Si TFTs, the method has also been proven to be sensitive enough to account for the effect of film morphology and differences in device processing [10]-[11], thereby providing an essential tool for the analysis of poly-Si thin film transistors.

However, there are also several issues associated with the field-effect conductance method. In particular, the distributions of gap states in upper (Ei ~ Ec) and lower (Ei ~ Ev) half of band-gap are obtained using n- type and p- channel devices, respectively. This limitation necessitates the use of at least two separate devices with different channel types to obtain full band-gap density of state analysis. Moreover, measurements need to be performed at various temperatures in order to determine the flat-band voltage (for details, please refer to the method description in the next chapter).

In this work, we propose a novel method to determine the full band-gap density of states of poly-Si channel using only a single device. The new method is successfully demonstrated on a novel Schottky barrier (SB) TFT device with field-induced drain (FID) that our group has developed previously [12]-[16]. The SB-TFT device exhibits an ambipolar operation capability, i.e., both n- and p- channel operation modes could be achieved in a single device. By exploiting this unique characteristic, we can perform the field effect conductance method to acquire the full-band gap state density distribution using only a single device. Experimentally, we also found that the flat-band voltage could be acquired by simply characterizing the ambipolar current-voltage (I-V) characteristics, without resorting to various temperature measurements. The extracted value is very close to that obtained by the temperature method, while the measurement scheme is greatly simplified.

1.2 Thesis outline

This thesis is organized as follows：

In Chapter 2, theoretical background of the FEC analysis, operation principles and the fabrication of the FID SB-TFT are described. Firstly, we introduce the theory of using the field-effect conductance to determine the gap state density used in conventional poly-Si TFT. Secondly, ambipolar operation of the FID SB-TFT is presented. Thirdly, the device fabrication flow is described.

In Chapter 3, experimental results are presented and discussed. Special attentions are paid to the determination of the flat-band voltage, and the effects of applied bias, recrytallization methods, hydrogenation, and the silicide materials.

Finally, we summarize our achievements and give conclusions in Chapter 4.

Chapter 2

Realization of Full Band-Gap DOS Analysis Using A Single Device

2.1 Field Effect Conductance Method

As mentioned in the last chapter, the performance of poly-Si TFTs is strongly affected by defects in the poly-Si channel. Characterization and analysis of DOS is thus essential for understanding the device characteristics as well as its dependence on the processing conditions. Moreover, accurate DOS is required for the modeling of poly-Si TFT characteristics. It has been shown that field effect conductance (FEC) method can serve this purpose. In this chapter, we will first briefly review its theoretical background.

FEC method was original proposed for characterizing the DOS in a-Si TFTs. When applied to poly-Si TFTs, the presence of grain boundaries in the channel could be of great concern. Fortunately, it has been proven that, when the grain size is small enough (compared to the channel length), the poly-Si channel film can be modeled using the "effective-medium" approach [6], in which the existence of grain boundary defects and intragranular defects are assumed to be uniformly distributed throughout the material. Under this assumption, the band bending is a solution of the one-dimensional Poisson's equation.

$$\frac{d^2\psi}{dx^2}\Big|_{x=0} = -\frac{\rho(\chi)}{\varepsilon_{Si}} \qquad (2\text{-}1)$$

The meanings of the symbols could be found in the List of Symbol (page [XII]).

ρ (x), charge density per unit volume, can be expressed by

$$\rho(\psi) = -q\int_{Ev}^{Ec} Ng(E) f(E - E_F - q\psi)dE + q\int_{Ev}^{Ec} Ng(E) f(E - E_F)dE \qquad (2\text{-}2)$$

The first term denotes acceptor-like states, which are neutral when empty and negatively charged when filled with electrons. The second term denotes donor-like states, which are positively charged when empty and neutral when filled with electrons. For sufficiently low temperatures, all states below the Fermi level are filled and all states above the Fermi level are empty. Eqn. (2-2) can be written (zero-temperature approximation)：

$$\rho(\psi) = -q\int_{E_F}^{E_F+q\psi} Ng(E)dE \qquad (2\text{-}3)$$

where *Ng(E)* is the gap-state density (per unit volume). Multiplying by $2\cdot\partial\psi/\partial x$ and integrating from x=0 (oxide-semiconductor interface) to x=Xo (unmodulated bulk, see Fig. 2.1)：

$$\left(\frac{d\psi}{dx}|_{x=0}\right)^2 = \frac{2q}{\varepsilon_{Si}}\int_0^{\psi_s} d\phi \int_{E_F}^{E_F+q\psi} Ng(E)dE \qquad (2\text{-}4)$$

where ϕ_s is the band bending at x=0 (surface potential) ,and $\left(\frac{d\psi}{dx}|_{x=0}\right)$ is the electric field at the surface. The gap-state density is then given by

$$Ng(E_F + \psi_s) = \frac{\varepsilon_{Si}}{2q}\frac{\partial^2}{\partial\psi_s^{\,2}}\left(\frac{d\psi}{dx}|_{x=0}\right)^2 \qquad (2\text{-}5)$$

The electric field at the semiconductor surface is given, in the absence of surface states,

$$\frac{d\psi}{dx}|_{x=0} = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{V_{ox}}{t_{ox}} = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{V_G - V_{FB} - \psi_S}{t_{ox}} \qquad (2\text{-}6)$$

From Eqns. (2-5) and (2-6), the gap-state density can be determined if the relationship between V_G and ϕ_s and bulk Fermi energy are known. The relationship between V_G and ϕ_s can be determined by the following two methods.

The incremental method

By assuming that the transport is by electrons, the field conductance is defined as [8]

$$G = G_0 - \frac{G_0}{d}\int_0^{\psi_s} \frac{\exp(q\psi / KT) - 1}{d\psi / dx} d\psi \tag{2-7}$$

where d is the poly-Si film thickness and G_o is the conductance for the flat band condition. The conductance is defined as the derivative of drain current with respect to the gate voltage at a fixed drain voltage. Differentiating Eqn. (2-7) with respect to the surface potential gives

$$\frac{dG}{d\psi_s} = -\frac{G_0}{d} \cdot \frac{\exp(q\psi / KT) - 1}{d\psi / dx|_{x=0}} \tag{2-8}$$

By substituting Eqn. (2-6) into Eqn. (2-8), the following approximation expression is obtained:

$$\frac{d\psi_s}{dG} = \frac{1}{G_0} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{d}{t_{0x}} \cdot \frac{V_G - V_{FB} - \psi_s}{\exp(q\psi_s / KT) - 1} \tag{2-9}$$

Actually, Eqn. (2-9) can be expressed by the differential form:

$$\psi_{s,i+1} = \psi_{s,i} + \frac{G_{i+1} - G_i}{G_0} \cdot \frac{d}{t_{0x}} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_{G,i} - V_{FB} - \psi_{S,i}}{\exp(q\psi_{S,i} / KT) - 1} \tag{2-10}$$

which can be used to construct the ϕ_s against V_G relationship.

The temperature method

This method is based on the temperature dependence of dG/dV_G. From Eqns. (2-8) and (2-6), and $dG/dV_G=(dG/d\psi_S)(d\psi_S/dG)$, one can obtain the following expression:

$$dG/dV_G = G_0 \frac{\varepsilon_{0x}}{d_{Si} \cdot t_{0x}} \cdot \frac{\exp[(E_F - E_C + q\psi) / KT]}{\rho(\psi_s)} \equiv k \cdot e^{(-\Delta E / KT)} \tag{2-11}$$

Both E_F and ϕ_s in the above equation are expected to be temperature dependent. This

dependence is due to the variation of Eg with T and to the so-called statistical shift. The latter is due to the fact that the total density of electrons (trapped plus free electrons) is a constant, so that Eg must shift with T in order to compensate for the temperature dependence of the Fermi function. Since all terms on the right-hand side, with the exception of exp(q ϕ_s/kT), have a weak temperature dependence, ϕ_s can be determined from log(dG/dV$_G$) versus 1/T plot. The temperature analysis also allows the determination of an important parameter, namely, the flat band voltage. Following the method proposed by Weisfield and Anderson [17], the following expression is obtained for small ϕ_s.

$$\frac{d\log G}{dV_G} \cong \frac{\varepsilon_{0x}}{t_{0x}} \cdot \frac{1}{qkTN_0}\left[1+\frac{1}{2}\left(\frac{q\psi_s}{KT}\right)+O\left(\frac{q\psi_s}{KT}\right)^2 \ldots\right] \qquad (2\text{-}12)$$

where N_o is the DOS at the Fermi level under flat band condition. V$_{FB}$ is then determined as the gate voltage where T(dlogG/dV$_G$) is temperature independent. Fig. 2.2 summarizes the flow chart using conventional FEC scheme to determine the DOS. It should be noted here that both p- and n-channel devices are needed for full band-gap DOS characterization.

2.2 Operation of Ambipolar TFT

In this study we propose a new approach that utilizes only a single FID SB-TFT to achieve the full band-gap DOS characterization. Here we briefly describe the structure and operation of FID SB-TFT device. Cross-sections for two types of device are shown in Fig. 2.3. The device features metallic silicide junctions and a metal field-plate, also called sub-gate, lying over the passivation oxide. Offset regions in the channel are formed in both drain and source sides. It is the key to achieve excellent ambipolar characteristics without suffering from the severe off-state leakage. In this

study, the source-side offset region is defined by a self-aligned sidewall spacer, while the drain-side offset region is formed by either sidewall spacer or by an extra lithography step. In the latter case (Fig. 2.3 (b)), the length of the offset region, X_D, is defined by the mask. In this work, most samples use $Cosi_2$ as the source and drain material to exploit its near-mid-gap work function. With near-mid-gap work function, the barrier height between electrons and holes is comparable (Note: barrier height for electron is slightly higher than for hole in this case), resulting in near symmetrical I-V characteristics. Issues regarding the barrier height of silicde on the DOS measurement will be addressed in Chap. 3.

During device operation, a proper fixed voltage is applied to the field-plate to form an electrical drain extension under the field-plate region. The device can be set for n- and p-channel operations with positive and negative biases, respectively. With appropriate bias and polarity applied on other electrodes (i.e., main gate, and drain), excellent ambipolar transfer characteristics could be achieved. The unique ambipolar characteristics are exploited in our approach to extract full band gap DOS using only a single device.

2.3 Device Fabrication

The key processing flow of the proposed structure is shown in Fig. 2.4. Detailed processing is described below.

- Poly-Si channel deposition

1. Si wafers capped with thick thermal oxide were employed to serve as a substitution for the glass-like substrate used in the active matrix liquid crystal display (AMLCD).

2. An amorphous silicon channel layer (50nm) was deposited at 550°C by low temperature chemical vapor deposition (LPCVD). For some splits, as-deposited poly-Si was used instead.
3. The amorphous silicon layer was then transformed to polysilicon layer either by solid phase crystallization (SPC) method or excimer laser annealing (ELA). For the solid phase crystallization, wafers were re-crystallized at 600°C in N_2 ambient for 24 hours.

● Gate oxide formation

1. The active area was defined using a G-line stepper.
2. LPTEOS gate oxide (50nm) was deposited, followed by deposition of poly-Si gate layer (200nm).
3. The poly-Si gate layer was subsequently doped by arsenic ion implantation, and then activated in N_2 ambient for 24 hours.
4. The n^+ poly gate layer was then patterned to form the main gate.

● Offset region definition

1. Deposition of LPTEOS oxide layer (200nm).
2. Photolithograhic and plasma etch steps were used to define the offset region.

● Schottky source/drain formation

The source/drain was formed by self-aligned silicidation (salicidation):

1. Sputter deposition of a thin Co layer (20nm) capped with TiN (30nm).
2. Rapid thermal annealing (RTA) was performed at 550°C for 30 seconds to form silicide.
3. The non-reacted metals were removed by selective wet etching (H_2SO_4 :

H_2O_2=3:1 for 10 minutes at 120°C).

4. Deposition of plasma enhanced TEOS (PE-TEOS, 200nm) to serve as passivation oxide.

● Contact hole and metal pad formation

1. A lithographic step was used to pattern 90x90 μm^2 contact holes.
2. Contact hole etching was performed in an ANELVA ILD-4100 dry etcher.
3. Sputter deposition of a 300nm Al film.
4. Patterning of metal pads.
5. Post metal annealing was performed at 400°C for 30 minutes in N_2 ambient.

● Plasma hydrogenation

Wafers received a NH_3 plasma treatment in a PECVD chamber for 1 hour at 250°C.

Chapter 3

Analysis of Full Band-Gap DOS in FID-SB TFT Structure

3.1 Determination of DOS Using Temperature and Incremental Methods

Figure 2.2 shows the flow chart for the determination of DOS used in field effect conduction method. First of all, we have to obtain the flat-band voltage of the device. The flat band voltage can be determined by the temperature (i.e., activation energy) method with Equation (2-12)

$$\frac{d\log G}{dV_G} \cong \frac{\varepsilon_{0x}}{t_{0x}} \cdot \frac{1}{qkTN_0}\left[1+\frac{1}{2}\left(\frac{q\psi_s}{KT}\right)+O\left(\frac{q\psi_s}{KT}\right)^2 \ldots\right] \qquad (2\text{-}12)$$

From the above equation, the flat-band voltage can be determined by the V_G when the product Tx($d$logG/dV$_G$) is temperature independent (because surface potential is zero). Figures 3.1 (a) and (b) show the characteristics of T x ($d$logG/dV$_G$) against 1000/T performed on a FID SBTFT under n- and p-channel operation modes, respectively. From the two figures, the flat-band voltage is determined to be around -2.1V that is almost independent of the temperature in either p- or n-channel operation.

Once the flat-band voltage is obtained, the relationship between the gate voltage V_G and surface potential φ_s could be established by either incremental method or the temperature method mentioned in Chap. 2. Next, we first use the incremental method to obtain this relationship, as shown below:

$$\psi_{s,i+1} = \psi_{s,i} + \frac{G_{i+1}-G_i}{G_0} \cdot \frac{d}{t_{0x}} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_{G,i}-V_{FB}-\psi_{S,i}}{\exp(q\psi_{S,i}/KT)-1} \qquad (2\text{-}10)$$

Here we use the Visual Basic Language to obtain the solution of this equation. After the flat-band voltage and the relationship between gate voltage and the surface potential are determined, Matlab language is adopted to obtain the gap-state density. Fig. 3.2 shows an example of the DOS versus energy level in the gap. In this case the channel is solid phase crystallization (SPC) poly-Si film. The channel width is 20um, and the channel length is 2um. The upper- and lower-half gap density is obtained by biasing the device into the n- and p-channel operation modes, respectively.

Next, we show how the temperature method is performed to obtain the relationship between the gate voltage and surface potential. This method is based on the temperature dependence of conductance at different gate voltages. Figure 3.3 shows the characteristics of drain current versus gate voltage measured at different temperatures. It can be seen that the on-current becomes larger as the temperature gets higher, simply due to a higher thermionic emission. Figure 3.4 shows the Arrhenius plot of dG/dV_G against 1000/T at different applied gate voltages. The slope of each straight line defines the activation energy, Ea. Figure 3.5 shows the characteristics of activation energy against gate voltage. As the gate voltage is increased, activation energy falls due to increasing carrier density (and thus lower barrier height). From the equation $Ea= E_{cb}-E_{F0}-q\phi_s$ stated in Chap. 2 and the results obtained in Fig. 3.5, we can obtain the relationship between the gate voltage and surface potential. As a consequence, the gap-state density distribution could be obtained. Figure 3.6 shows and compares the DOS versus energy level in the gap obtained by the temperature method and incremental method. The results are in reasonable agreement with each other. Nevertheless, in most cases it is observed that the data obtained from the temperature method show more fluctuation in the mid-gap region. This is ascribed to the dramatically lowering in measured current as temperature is reduced. In some instances the current is close to or even below the limit of the measurement system.

Thus, it is preferable to use the incremental method, rather than the temperature method, to determine the relationship between the surface potential and gate voltage.

3.2 Effect of Applied Drain Bias

Here we address the effect of drain bias on the measurement results. The measurements were carried out for n-channel operation by sweeping gate voltages from –3 to +6V, and for p-channel operation by sweeping gate voltages from –1 to –10 V, with drain voltages $|V_{DS}|$= 0.1V or 5V, and sub-gate voltage |Vsub|=50V. Figure 3.7 shows the characteristics of the I_D-V_G for the FID SB-TFT with $CoSi_2$ S/D material. The channel film is SPC poly-Si film. As can be seen in the figure, the on-current in n-channel operation is more sensitive to V_{DS} than p-channel operation, owing to the higher barrier height of electrons than holes at the $CoSi_2$/Si contact. The extracted DOS results are shown in Fig. 3.8. It is observed that the DOS remains unaffected in the mid-gap regime, but increases significantly near the band edge when $|V_{DS}|$ is set at 0.1V, especially for the conduction band edge. It was shown previously that the increase in $|V_{DS}|$ could decrease the source-side carrier tunneling distance [12]-[14], and thus the parasitic resistance. As the Fermi level moves toward the band edge, the operation is near threshold and becomes more sensitive to the contact resistance. As a result, the DOS is overestimated when $|V_{DS}|$ is not sufficiently high.

3.3 Effects of the channel length

Figures 3.9~3.12 shows the ambipolar transfer characteristics and correspondingly extracted DOS for four devices with self-aligned spacer and channel length ranging from 0.8 to 5 μm. The on-current measured at $|V_{DS}|$ = 0.1 V as a function of channel length for these devices is shown in Fig. 3.13. The on current

becomes larger as the channel length becomes shorter due to reduced channel resistance. However, the n-mode current is almost independent of channel length when channel length is lager than 1 μm, indicating the significance of contact resistance due to larger electron barrier height. In these measurements, the mid-gap DOS is almost the same (about $1.2x10^{18}$ $eV^{-1}cm^{-3}$), while the tail DOS is strongly dependent of the applied bias conditions. Figure 3.14 (a) & (b) compare the DOS results among devices with different channel length and $|V_{DS}|$ of 5 V. It can be seen that reasonable agreement is achieved among these devices, indicating that $|V_{DS}|$ of 5 V is sufficient large so the effects of parasitic resistance is insignificant.

3.4 Effects of drain-side extension length

Figure 3.15 (a) shows the ambipolar transfer characteristics of device with self-aligned and non-self-aligned (X_D = 3 μm) FID length under $|V_{DS}|$ of 0.1V. The extracted DOS results are shown in Fig.3.15 (b). It can be seen that the on-state current is significantly lower for device with X_D of 3 μm. This is apparently due to the larger parasitic resistance in the FID region and thus leads to an overestimation of tail DOS, as shown in Fig.3.15 (b). Such disparity can, again, be removed by increasing the $|V_{DS}|$ to 5 V, as shown in Fig.3.16.

3.5 Effects of measurement temperature

Figure 3.17 shows that the ambipolar transfer characteristics of a device characterized at 25°C and 55°C. The on-state current is larger at 55°C than 25°C, owing to the enhanced conduction of thermionic emission at higher temperature. The extracted DOS results are shown in Fig.3.18. We can see that the results are in reasonable agreement with each other, indicating that the zero-temperature

approximation mentioned in Chap. 2 stands in the characterized temperature range.

3.6 Results comparison with conventional approach

Figure 3.19 shows and compares the DOS results extracted by performing the characterization process on a FID SB-TFT and two conventional TFTs (i.e., p- and n-channel TFTs with degenerately doped S/D) with same channel material, which is as-deposited poly-Si films. It can be seen that results are similar which validates the DOS data deduced from the FID SB-TFT structure, even though only a single device is used in our proposed methodology.

3.7 Effects of channel crystallization treatment

The electrical performance of poly-Si TFTs strongly depends on the quality of the polysilicon film. Methods such as direct deposition of polysilicon film by low-pressure chemical vapor deposition (as-deposited poly-Si), low-temperature solid phase crystallization (SPC) of amorphous silicon, and excimer laser annealing (ELA) crystallization methods, have been carried out in this work to examine their crystallinity and its consequence on the DOS characteristics. Fig.3.20 shows the DOS extracted from samples with SPC and as-deposited poly-Si channels. Both samples received 1-hour NH_3 plasma treatment. It is seen that the SPC channel shows less DOS than the as-deposited poly-Si counterparts. This is primary due to the larger grain size of SPC sample than that of as-deposited poly-Si, as characterized by the transmission electron microscopy (TEM) results shown in Fig.3.21. From both electrical and physical characterization confirm that the SPC film indeed has larger grain size and better quality than the as-deposited poly-Si film.

Figure 3.22 shows the DOS comparison between the ELA and SPC samples The results indicates that the ELA treatment could further reduced the DOS. Figure

3.23(a) and (b) show the TEM micrographs of the SPC and ELA samples, respectively. We can clearly see that the grain size of ELA film much larger than that of SPC film, and resulting in the reduced DOS shown in Fig.3.23.

3.8 Effects of plasma hydrogenation

It was shown previously that deep trap states located near the mid gap mainly arise from dangling bond defects (predominated situated in grain boundary regions) whereas tail states may arise from distorted bond defects (predominated inside the grains) [18]. These traps could be effectively reduced after performing a hydrogenation treatment on the fabricated devices. Moreover, the relative passivation efficiencies on different types of defects can be determined and compared by comparing the DOS before and after hydrogenation. Fig.3.24 shows and compares the ambipolar transfer characteristics of the SPC samples before and after 1 hour NH_3 plasma treatment. After plasma treatment, the on current is increased while the subthreshold swing is improved. The corresponding DOS results are shown in Fig.3.25. As can be seen in the figure, a hump appears near mid-gap before hydrogenation, presumably caused by the dangling bonds situated in grain boundaries. Hydrogenation reduces in the mid-gap state density by one order of magnitude (from 10^{19} to 10^{18} $eV^{-1}cm^{-3}$). This results in improved subthreshold swing and on current. It can also be seen that, although the mid-gap state density is reduced dramatically after plasma hydrogenation, the tail state density near both valence and conduction band edges are only affected slightly. This indicates that the plasma treatment passivates the dangling bond more effectively. It may need more time to reduce the tail state density, as pointed out in Ref.18.

Figure 3.26 shows and compares the DOS of devices with as-deposited poly-Si

channel before and after plasma hydrogenation. Similarly, the DOS is reduced, though the improvement on tail states seems to be more significant, as comparing to the SPC case shown in Fig. 3.25. This phenomenon is not fully understood at this stage and maybe presumably be related to the column grain texture with the smaller grain size. Table.2 lists DOS of the devices before and after plasma hydrogenation.

3.9 Effects of silicide material

Figure 3.27 shows the ambipolar transfer characteristics of FID SB-TFT device with PtSi Source/Drain. We can see that the on current is larger in p-channel operation than in n-channel operation. This is due to the lower barrier height for holes (~0.24eV) than for electrons (~0.88eV) in the case of the PtSi/Si contact. As a result the contact resistance will be significant for n-channel operation. The extracted DOS is shown in Fig.3.28 together with that obtained from the device with $CoSi_2$ S/D. We can see that the upper-band DOS is obviously overestimated for device with PtSi S/D, owing to the high parasitic resistance presenting at the silicide junction. Thus, for full-band gap DOS analysis, it is essential to choose the mid-gap silicide material to obtain accurate gap state density distribution.

3.10 Analysis of full band-gap DOS in SB poly-Si FinFET

Recently, our group proposed poly-Si SB-TFT with nano-scale channel width featuring silicided Schottky barrier source/drain with field-induced source/drain extension. This device is also called poly-Si SB FinFET. The process flow of fabricating these nano-scale devices is similar to that of fabricating conventional structures except three notable differences: First, e-beam lithography was employed for device patterning throughout the fabrication. Secondly, the etching selectivity of

poly-Si to SiO_2 must be high enough to ensure that the poly-Si channel is not damaged during the process. The etching selectivity in both main etch and over etch steps are larger than 100, which is suitable for nano-scale gate patterning with ultra-thin gate dielectric layer. Thirdly, 10nm-thick sacrificial oxide is needed to remove the damage created by dry-etching processes on the sidewall surface of the poly-Si fin.

In this section we characterize and examine the DOS of the poly-Si SB FinFET. Two splits of samples, denoted as SA- and NSA-series, were characterized. The top view of the SA-series devices with 15nm offset length is shown in Fig. 3.29(a). This device employs a self-aligned sidewall spacer to define the offset region. The top and side views of the NSA-series devices with 1μm offset length in both drain and source sides (X_D and X_S) are shown in Figs. 3.29(b) ~ (d). An extra mask was employed to define the 1μm offset channel region. It is worth noting that these devices actually have a triple-gate structure, as can be seen in Fig. 3.29(d) which shows the cross-sectional view along the B---B' direction in Fig 3.29 (b). As a result, the effective channel width should be the sum of the Si Fin width (50nm) plus twice of the Si thickness (50nm).

Figure 3.30 shows the ambipolar transfer characteristics of FinFET structure at sub-gate voltage Vsub=2V and 5V. The on-state current increases as the sub-gate voltage increases. To explain this trend, Fig.3.31 shows the band diagram near source side. As the sub-gate bias increases, the source-side field emission current is enhanced by the narrowed tunneling width and therefore higher on-current. Fig.3.32 and Fig.3.33 show the ambipolar transfer characteristics of different channel width. The device with a wide (i.e., 5um) channel width serves as the "de facto" planar structure. While the other nanoscale device with three fins, each fin having a width of 50 nm and height of 50 nm, represents an effective channel width of 450 nm. We can see that

the poly-Si SB FinFET exhibits much steeper subthreshold swing as comparing to the device with planer with. Fig.3.35 shows the ambipolar transfer characteristics and Tx(d(logG)/dV_G) against 1000/T, from which we can deduce that the flat band is around –0.4V. Fig.3.35 shows the extracted DOS of the planar structure (W=5um) and FinFET (W=0.45um) structure. It can be seen the DOS is smaller in the FinFET structure than in the planar structure. This is because the FinFET has a channel thickness that is narrower than the depletion length and thus the effective DOS within the channel is lowered. In other words, the controllability of gate bias on adjusting the channel potential is promoted when a nano-scale fin channel is employed, and thus the subthreshold swing is improved.

3.11 A New & Simpler Methodology to Determine Flat-Band Voltage

Precisely determine the flat-band voltage is essential for building the relationship between DOS and the energy level inside the gap. As mentioned above, in order to achieve this purpose, a number of measurements of the conductance need to be performed at various temperatures. Moreover, in conventional approach, the process should be conducted separately on p- and n-channel devices. It is thus very tedious and time-consuming. In this work, we experimentally found that the flat-band voltage obtained using the above method is actually very close to the gate voltage at the intersection point of p- and n-mode I-V curves measured at room temperature. An example is provided by the results shown in Figs.3.1 and 3.3. We can see that the p- and n-mode I-V curves at 25 ^oC intersected at V_G ~ -2V, which is very close to the result obtained in Fig.3.1 (V_{FB} ~ -2.1 V). We thus propose a way and simpler to determine the flat-band voltage by simply measuring the gate voltage at the

intersection point of p- and n-mode I-V curves measured at room temperature using a SB TFT. To validate this method, a number of samples were characterized and the results are summarized in Fig.3.36. We can see that the difference between the conventional method and our method is indeed small. To take advantage of this simpler method, we modify the flow chart for analysis of full band-gap DOS using the SB TFT in Fig.3.37. This scheme greatly simplify the process of conventional approach shown in Fig.2.2, since only two I-V measurements performed at room temperature on a single device performed at room temperature is required for the analysis.

Chapter 4

Conclusions and Future Work

4.1 Conclusions

In this work, we have proposed and successfully demonstrated a novel approach to obtain the full band-gap DOS in the channel of TFT devices. In this approach, the field-effect conductance method is performed on an SB poly-Si TFT which has the capability of ambipolar operation. Both incremental and temperature methods are adopted on the SB and conventional devices to construct the relationship between DOS and the energy level in the gap. For devices with the same channel material, the results are in good agreement among the different measurement schemes, indicating that the novel approach is very reliable.

We have also characterized the dependence of both electrical and structural parameters on the measurement results in order to set suitable test conditions. Our results indicate that the parasitic resistance presenting in the channel would result in an overestimation of tail state density. Accurate DOS extraction can be obtained by employing sufficiently high drain and sub-gate biases and short electrical junction. In addition, near-mid-gap silicide material such as $CoSi_2$ is desirable for reliable full band-gap DOS analysis.

We have also characterized the effect of process treatments including re-crystallization and plasma hydrogenation steps on the DOS characteristics. Their impacts could be clearly identified using the new approach. Benefits of using a nano-scale Fin channel for promotion of the controllability of gate voltage over the channel potential is also clearly demonstrated.

Finally, we show that the flat-band voltage could be obtained by simply measuring the gate voltage at the intersection point of p- and n-mode I-V curves. The overall process is thus greatly simplified and cost-saving compared to conventional approach, since only two I-V measurements performed on a single device at room temperature are all that are needed. We strongly believe that the novel method is extremely useful for practical applications.

4.2 Future Work

Since our method provides a simple and efficient way to map the full band-gap density of states of the channel material, it will be a very powerful tool in the development and production of thim film transistors. We believe our method could be applied to TFT technologies using poly-SiGe or organic channel materials. The method would be efficient in understanding the impact of process treatment on the device characteristics and on addressing some material issues such as the impurity contamination and segregation in the channel. With specially designed test structures, the method may also be useful to characterizing the reliability issues of TFT devices such as the hot-carrier induced damage effects.

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Type		$CoSi_2$	
		P-channel	N-channel
S.S. (mV/dec)	|Vd|=0.1	832	680
	|Vd|=5	710	770
Ioff (|Vd|=5)		4.8E-12	4.6E-12
Ion (|Vd|=5)		1.0E-07	3.9E-08
Ion/Ioff (|Vd|=5)		2.2E+04	1.3E+04
Ioff (|Vd|=0.1)		2.6E-13	2.8E-13
Ion (|Vd|=0.1)		1.3E-08	1.7E-09
Ion/Ioff (|Vd|=0.1)		4.9E+04	6.0E+03
V_{FB}		-2.1V	-2.1V

Table.1 The extracted device parameters of $CoSi_2$ Source/Drain material.

Gap state density \channel film		Solid Phase Crystallization (SPC)	As-deposited	Excimer Laser Annealing (ELA)
Mid-gap state Density ($eV^{-1}cm^{-3}$)	Before Hydrogenation	~$8x10^{18}$	$2.2x10^{19}$	$5.4x10^{17}$
	After Hydrogenation	~$2x10^{18}$	$7.8x10^{18}$	
Tail-state density ($eV^{-1}cm^{-3}$)	Before Hydrogenation	$5.6x10^{20}$	$3.5x10^{21}$	$6.8x10^{19}$
	After Hydrogenation	~$2.1x10^{20}$	$7.3x10^{20}$	

Table.2 Gap state density of different channel films.

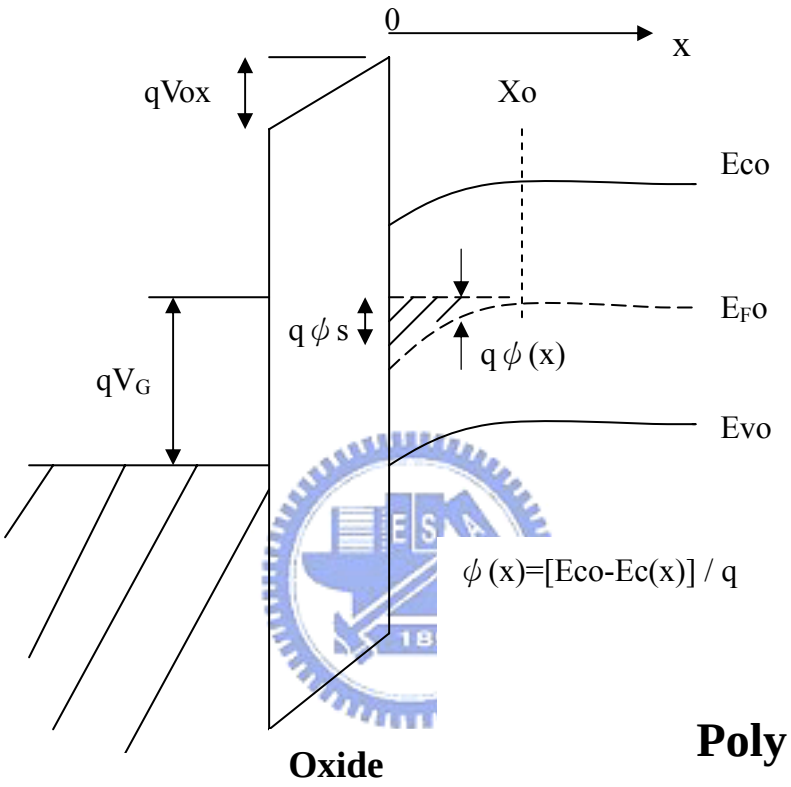


Fig.2.1 1-D Band scheme of a gate-oxide-poly-Si channel structure. x is 0 at the oxide/poly-Si interface.

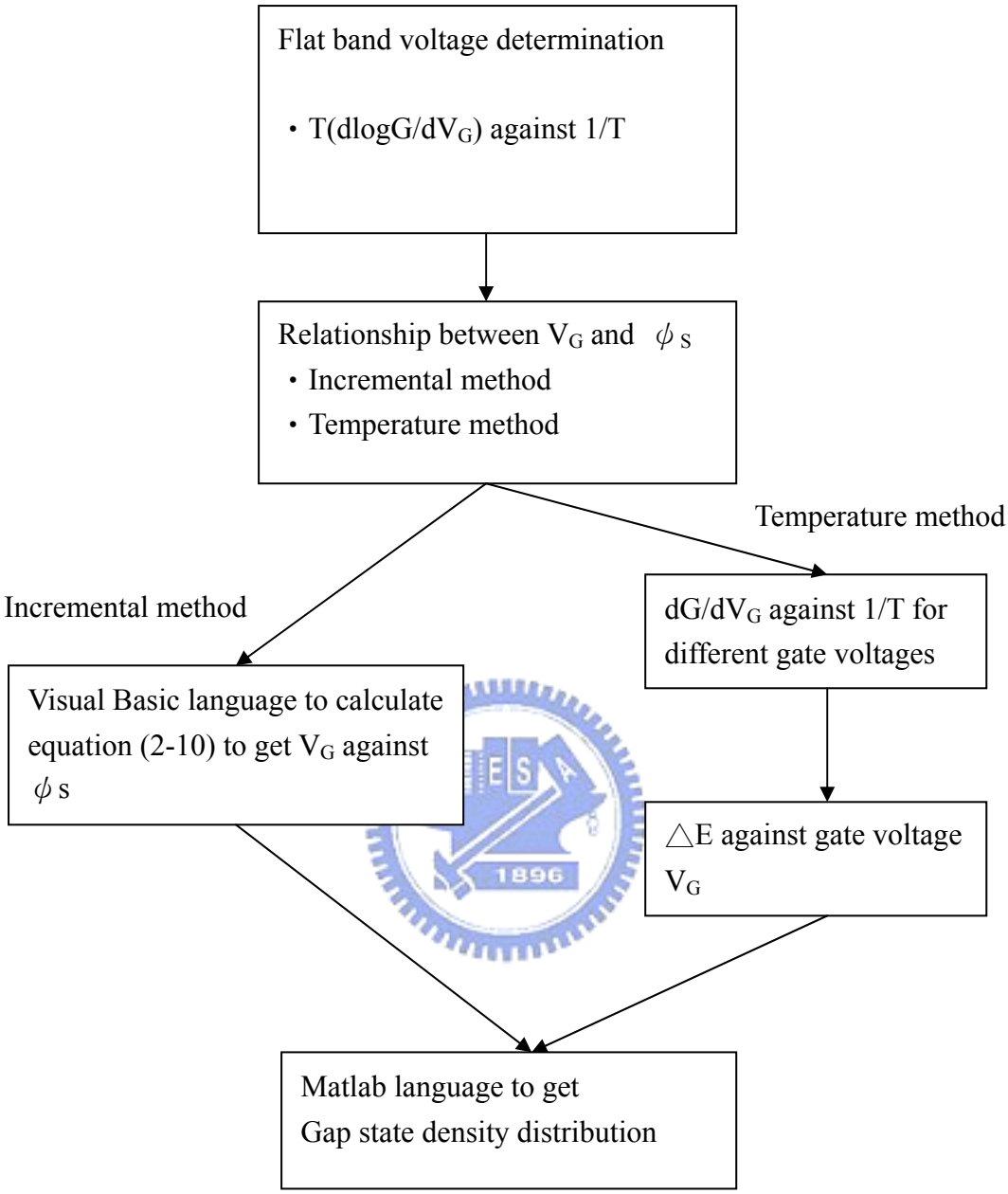


Fig.2.2 Flow chart for determination of DOS using conventional approach.

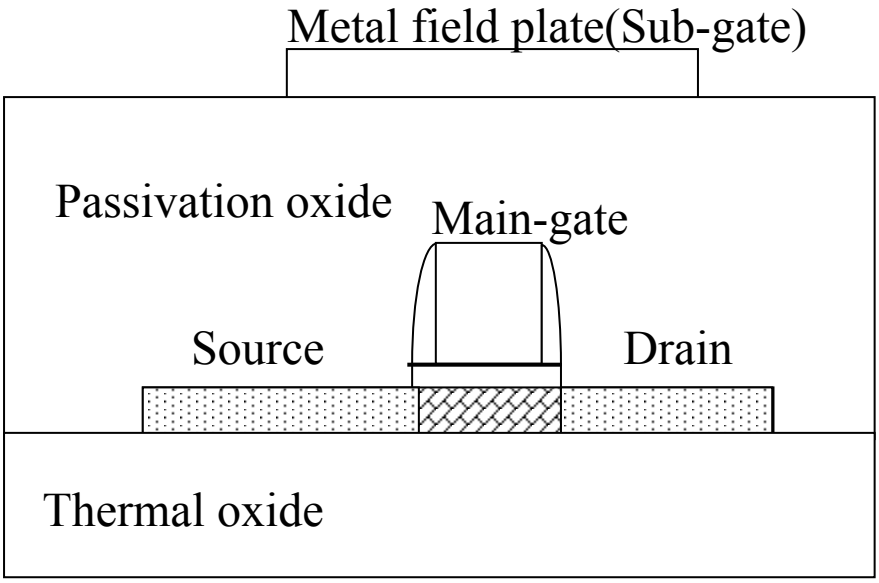


Fig.2.3 (a) Self-aligned cross section of FID SB-TFT.

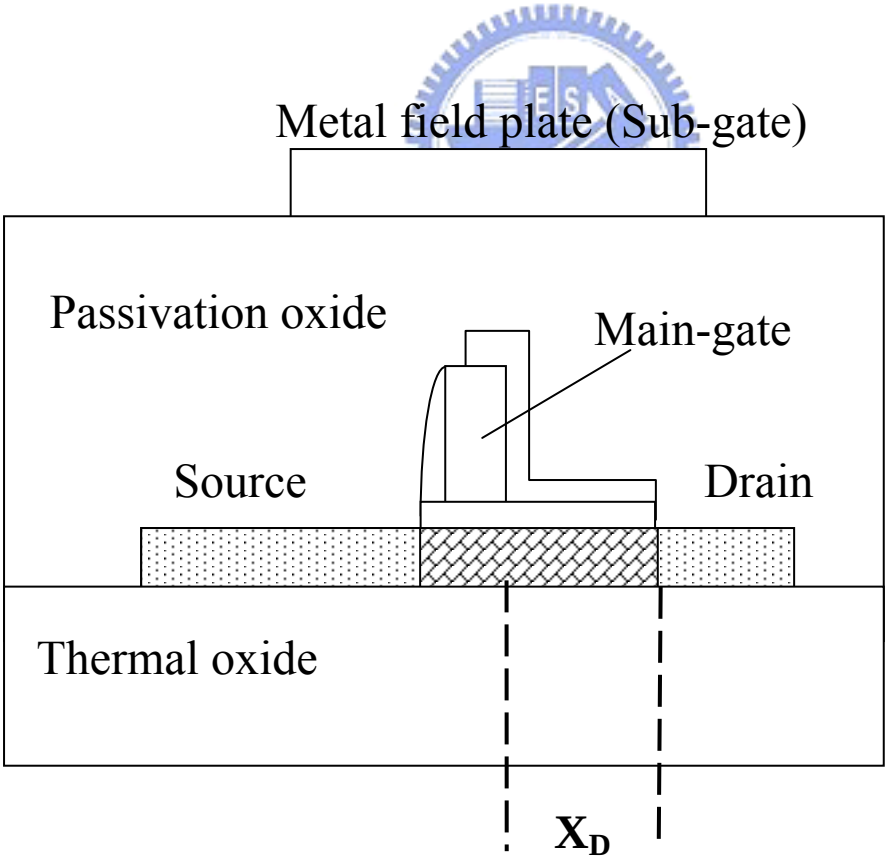
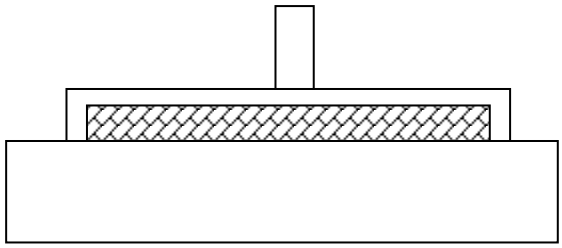
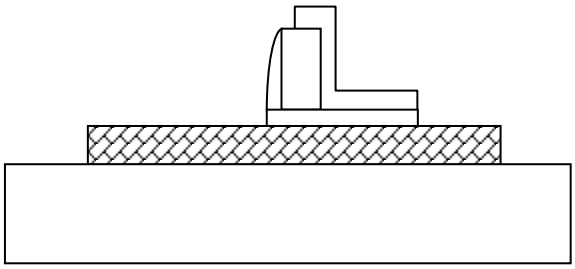


Fig. 2.3 (b) Non self-aligned Cross section of FID SBTFT.

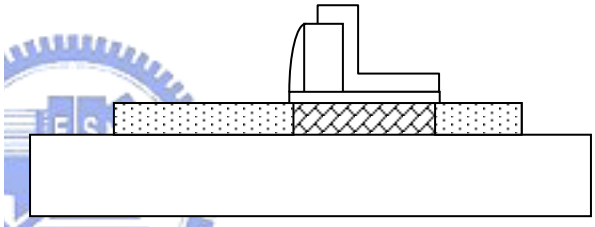
-Wet oxidation (200nm)
-LPCVD α-Si (50nm)
-ELA or SPC
-Active area patterning
-Gate oxide (100nm)
-Gate formation (n^+ poly-Si)



-LPTEOS (200nm)
-Oxide pattering



-Co salicide treatment



-Passivation (PETEOS 200nm)
-Metal pad and sub-gate

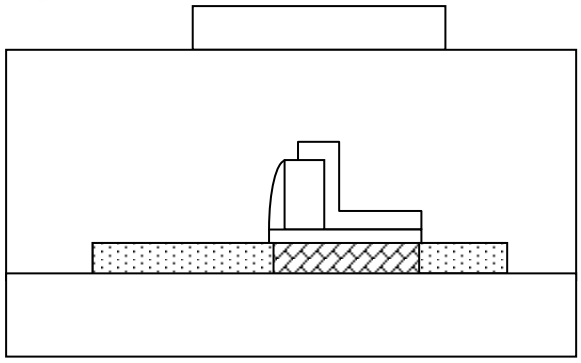


Fig. 2.4 The fabrication flow of FID SBTFT.

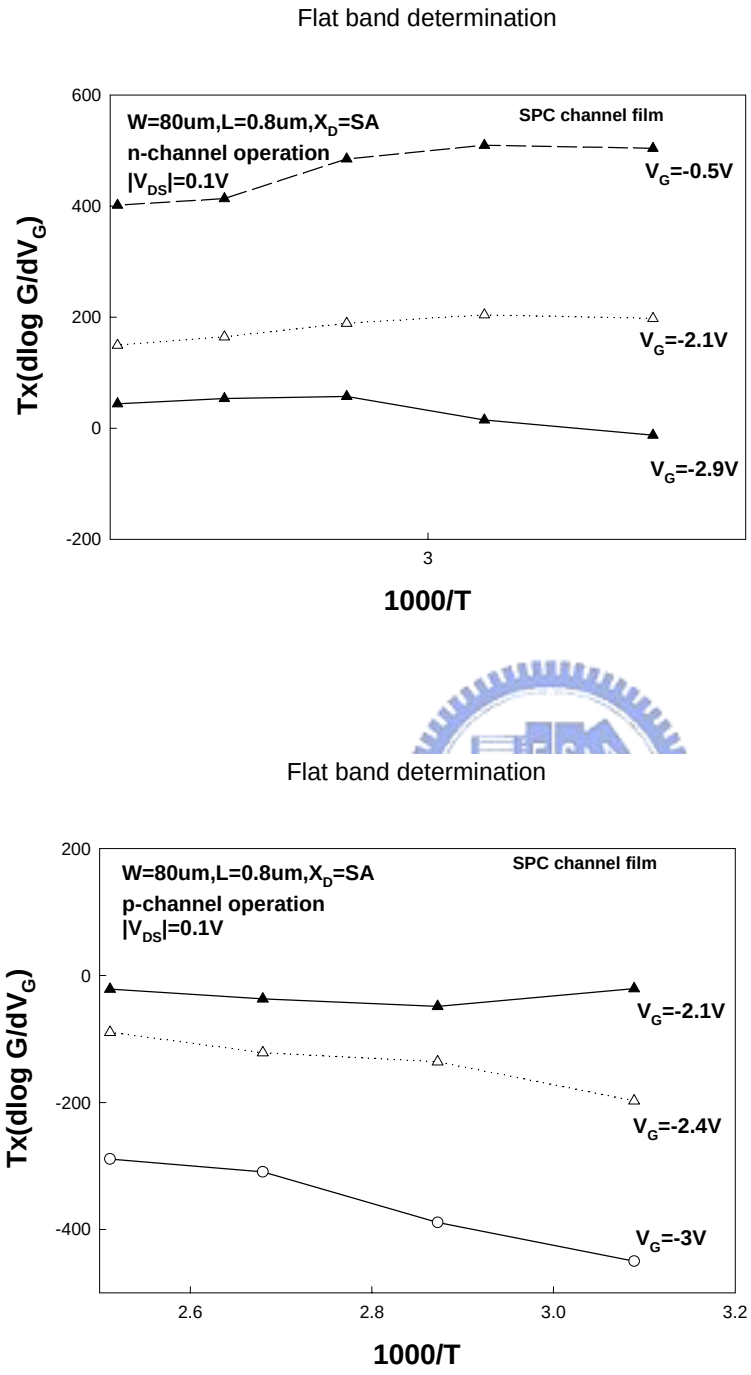


Fig.3.1 Flat-band voltage determination of FID SB-TFT using Tx($d$logG/dV$_G$) vs. 1/T plots: (a) n-channel operation; (b) p-channel operation.

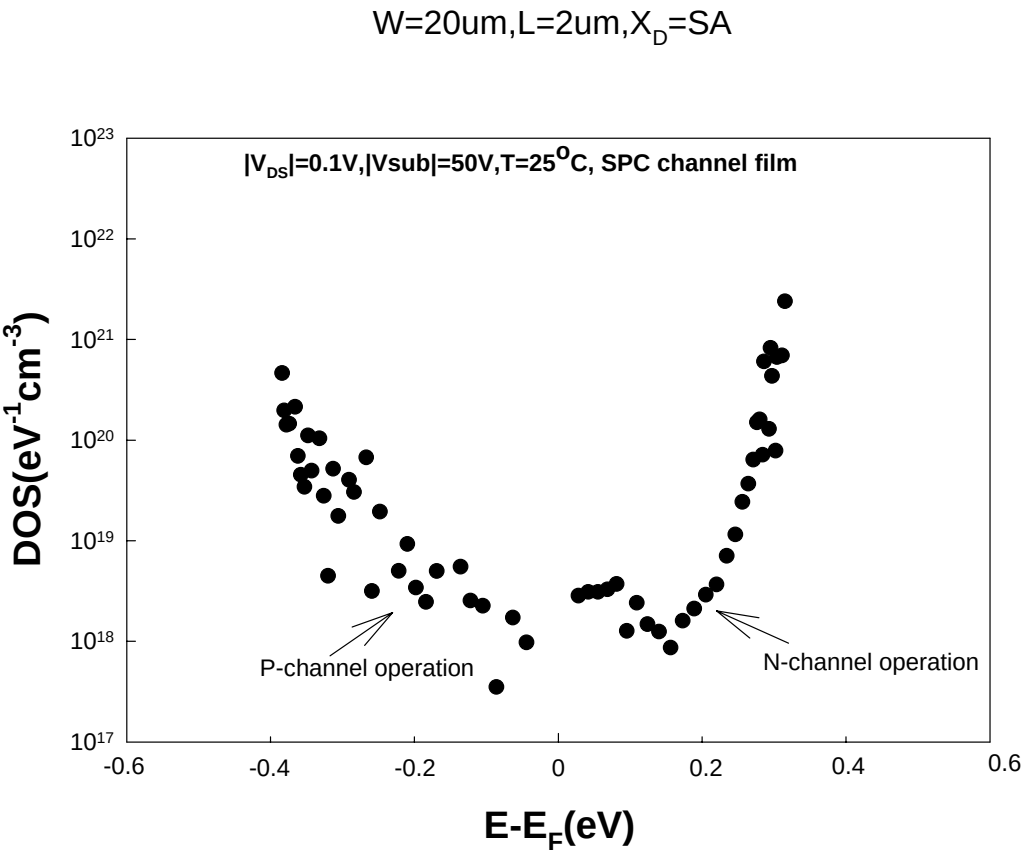


Fig.3.2 Full band-gap DOS distribution extracted using the FID SB-TFT.

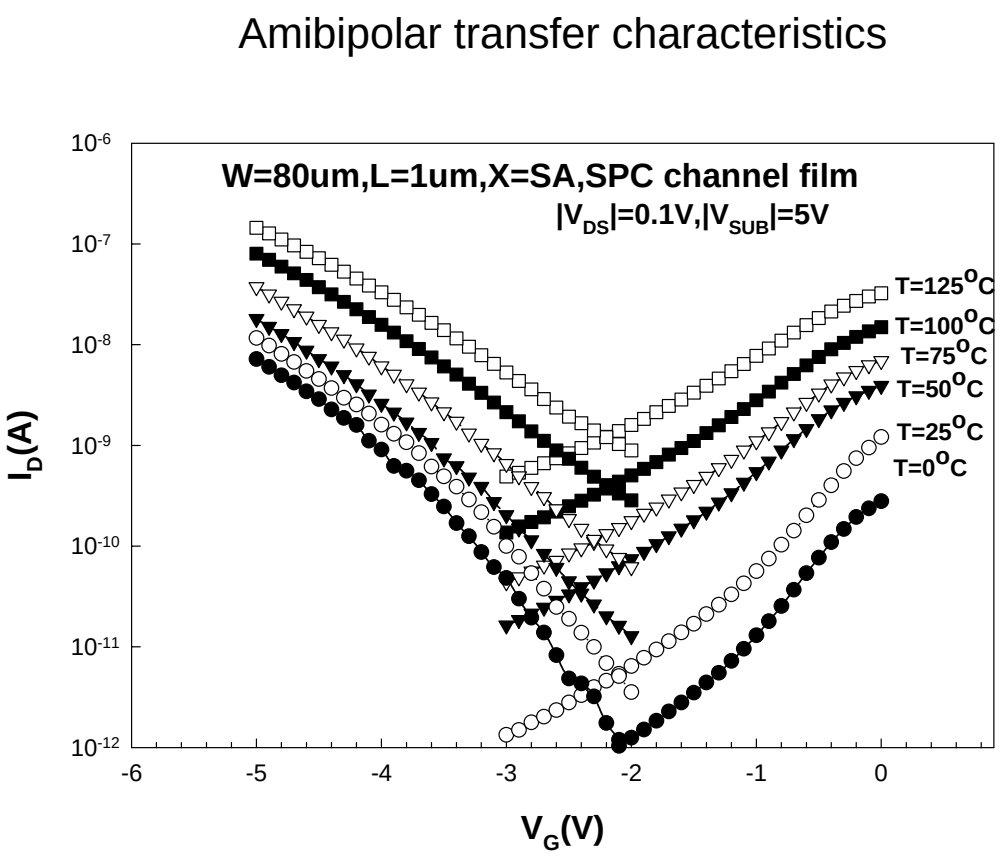


Fig.3.3 Drain current versus gate voltage characteristics.

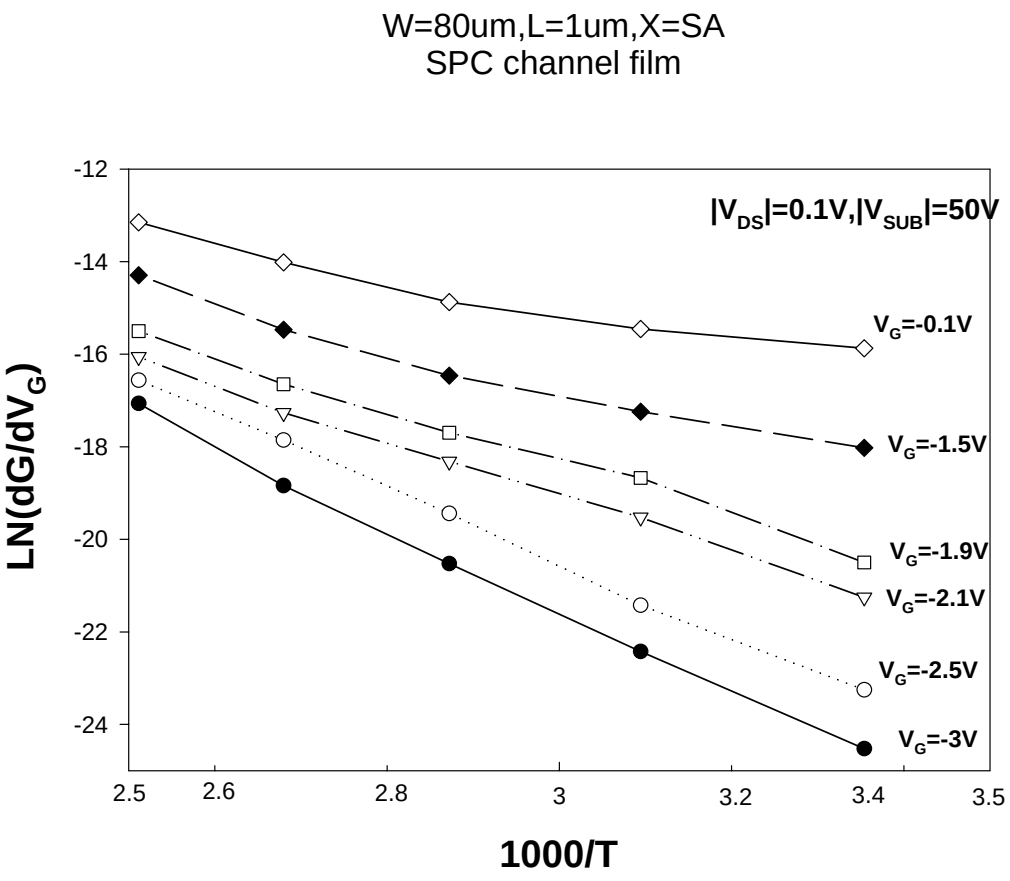


Fig.3.4 LN(dG/dV_G) versus 1000/T.

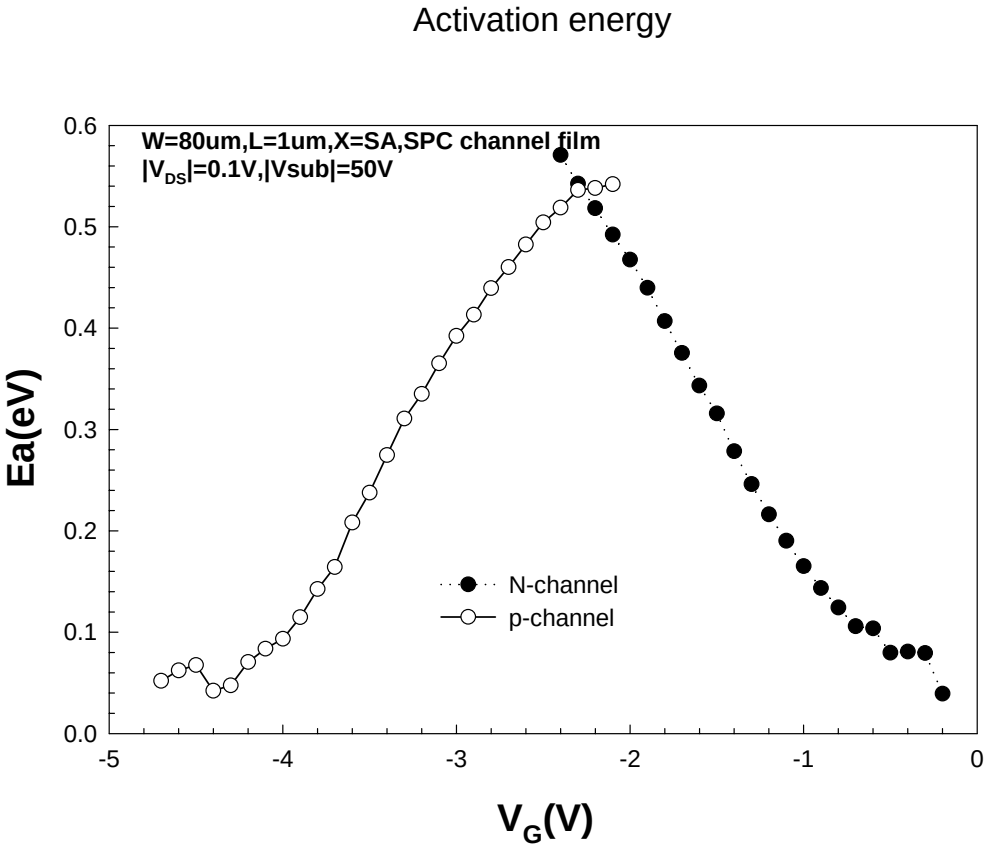


Fig.3.5 Activation energy versus gate voltage characteristics.

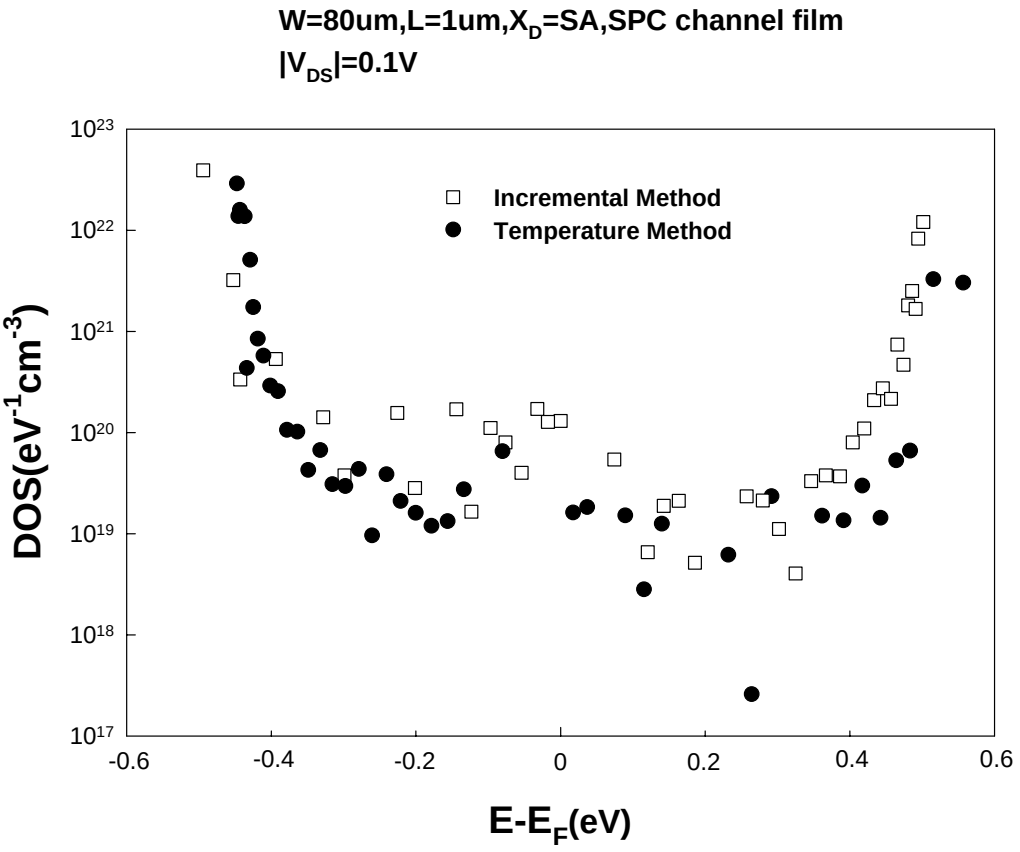


Fig.3.6 Full band-gap DOS deduced by the incremental method and the temperature method.

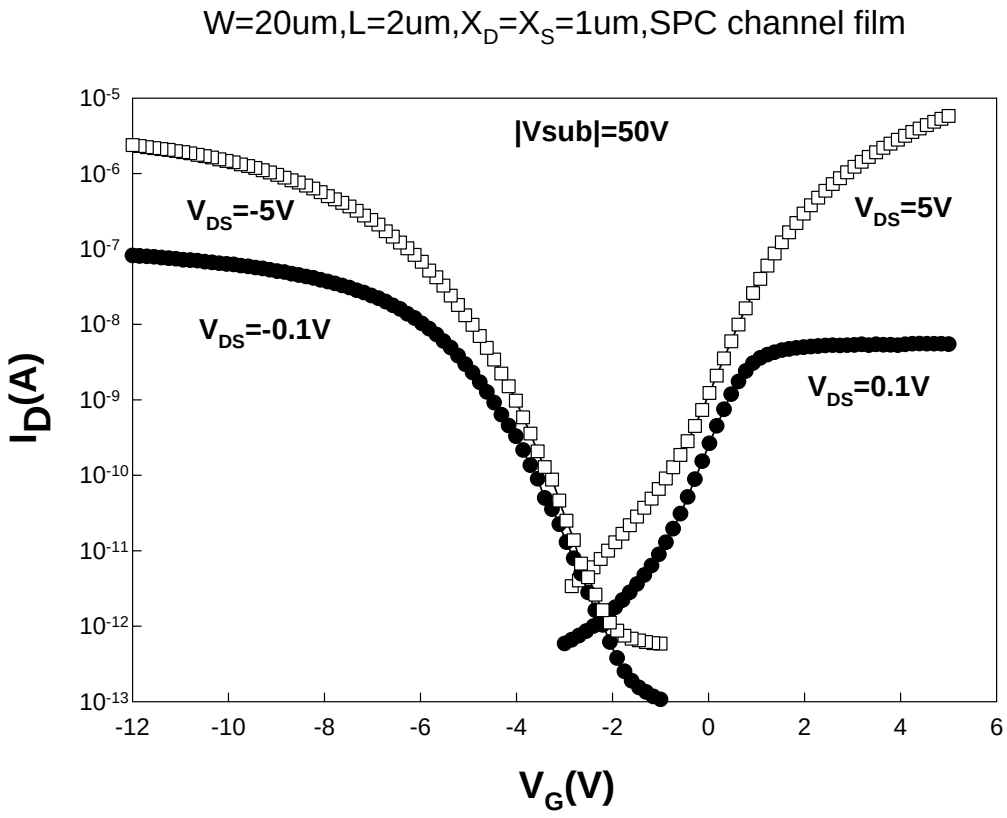


Fig.3.7 Ambipolar transfer characteristics in both low and high drain bias.

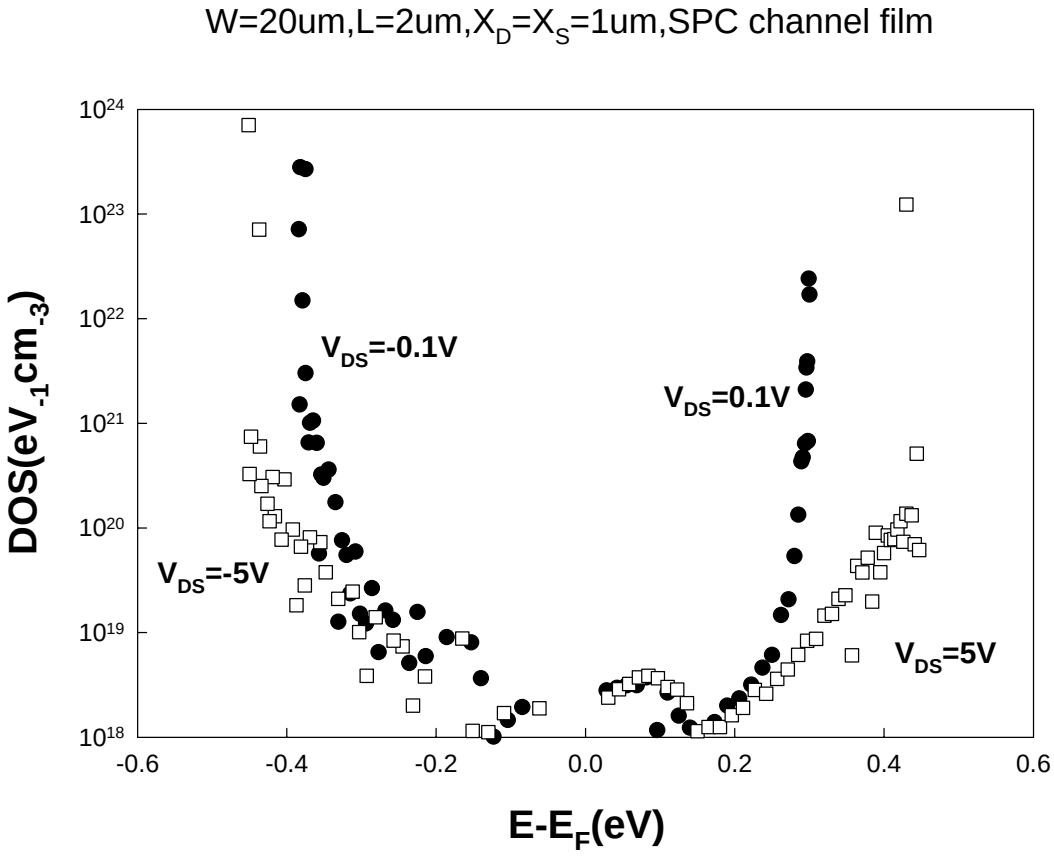
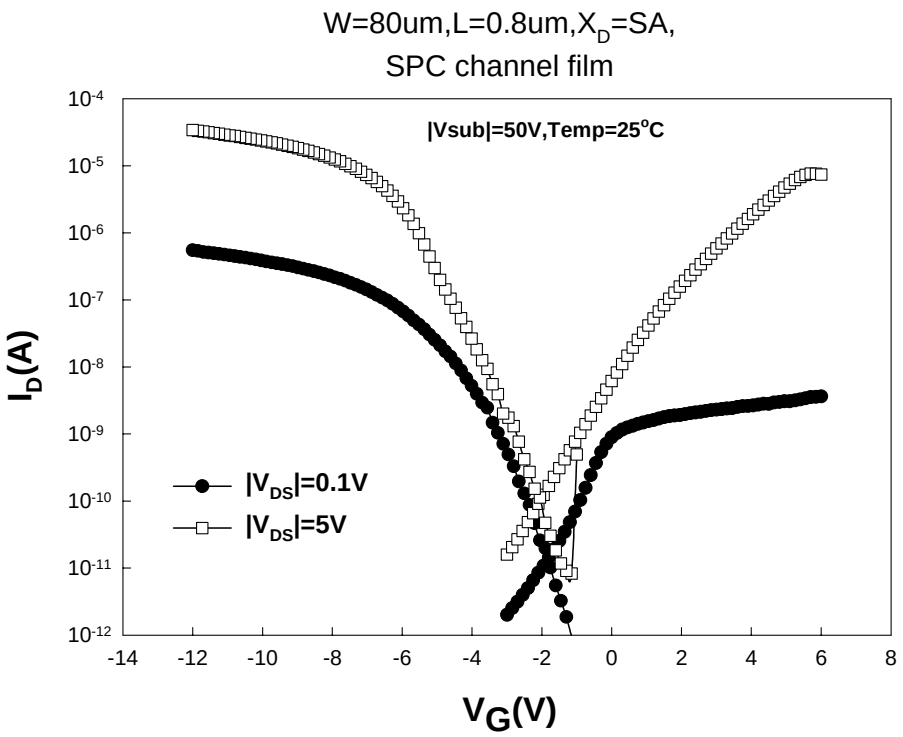
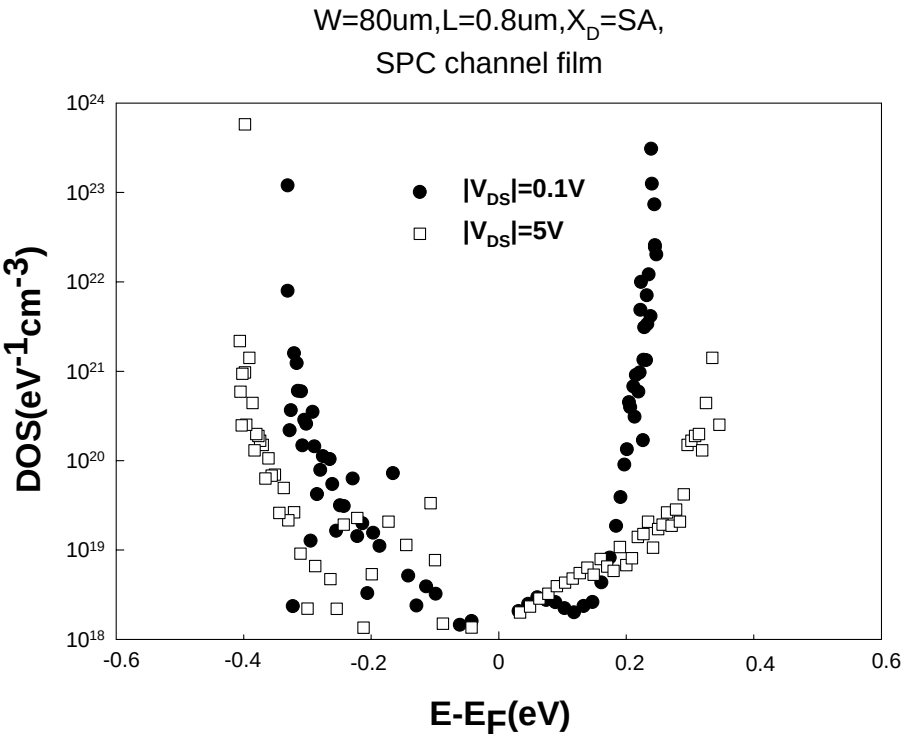


Fig.3.8 Full band-gap DOS extracted at $|V_{DS}|$ of 0.1 and 5 V.

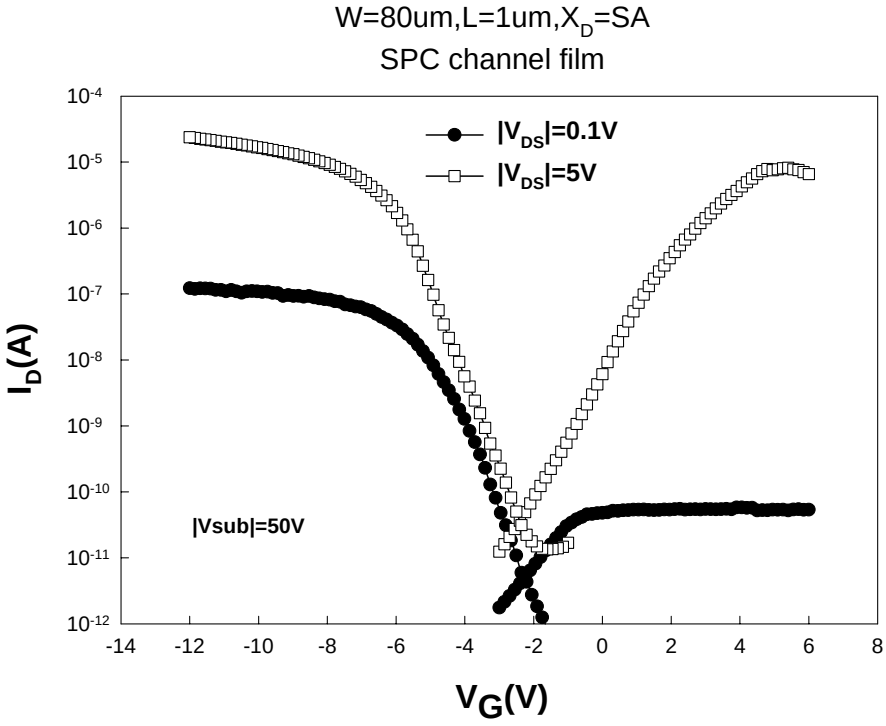


(a)

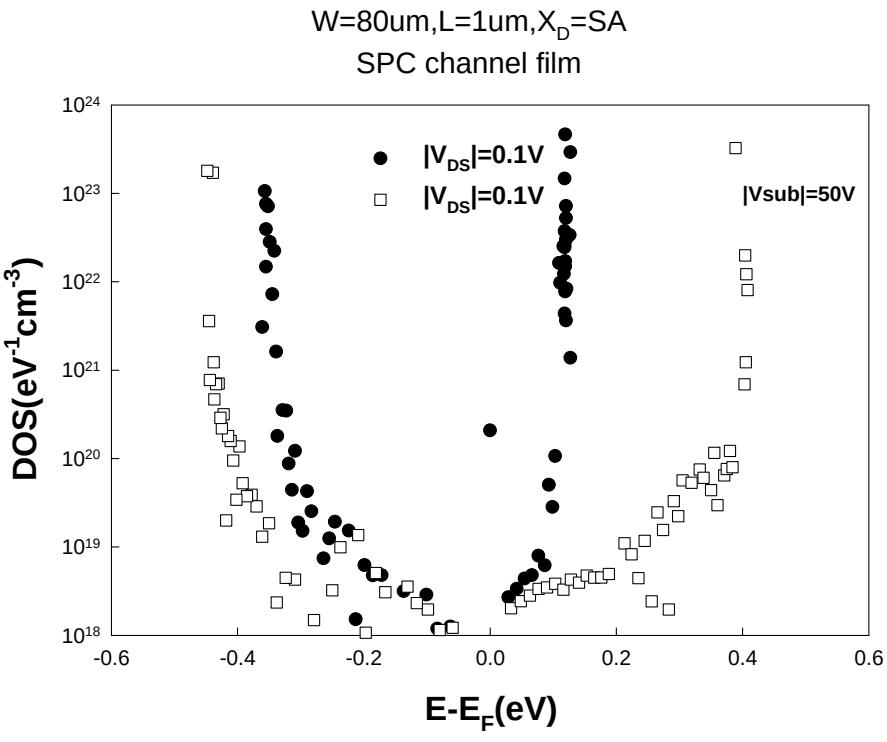


(b)

Fig.3.9 (a) Ambipolar transfer characteristics and (b) the extracted DOS results in a device with channel length of 0.8um.

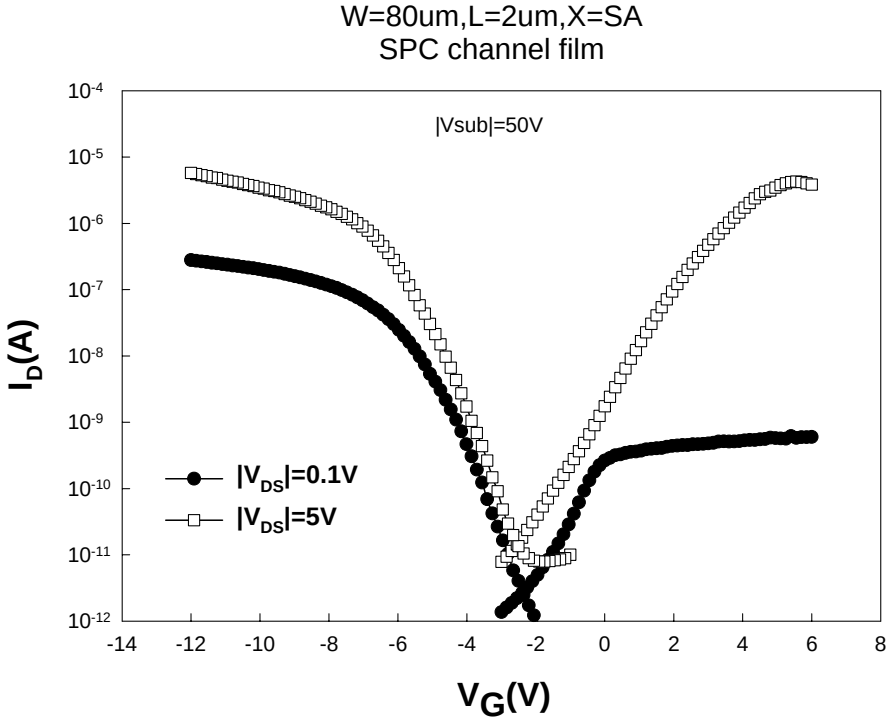


(a)

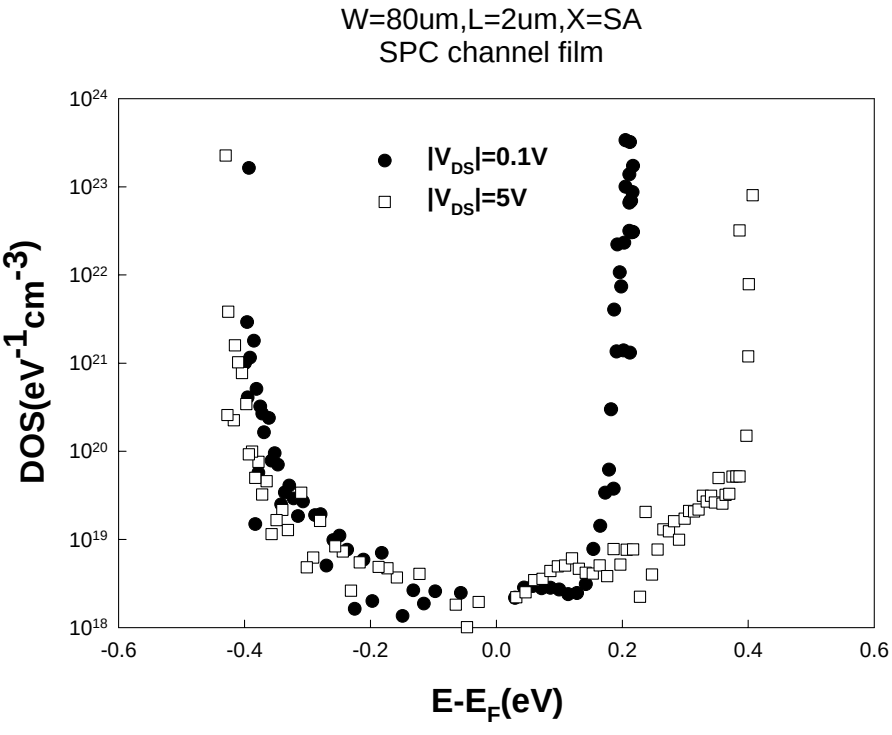


(b)

Fig.3.10 (a) Ambipolar transfer characteristics and (b) the extracted DOS results in a device with channel length of 1um.

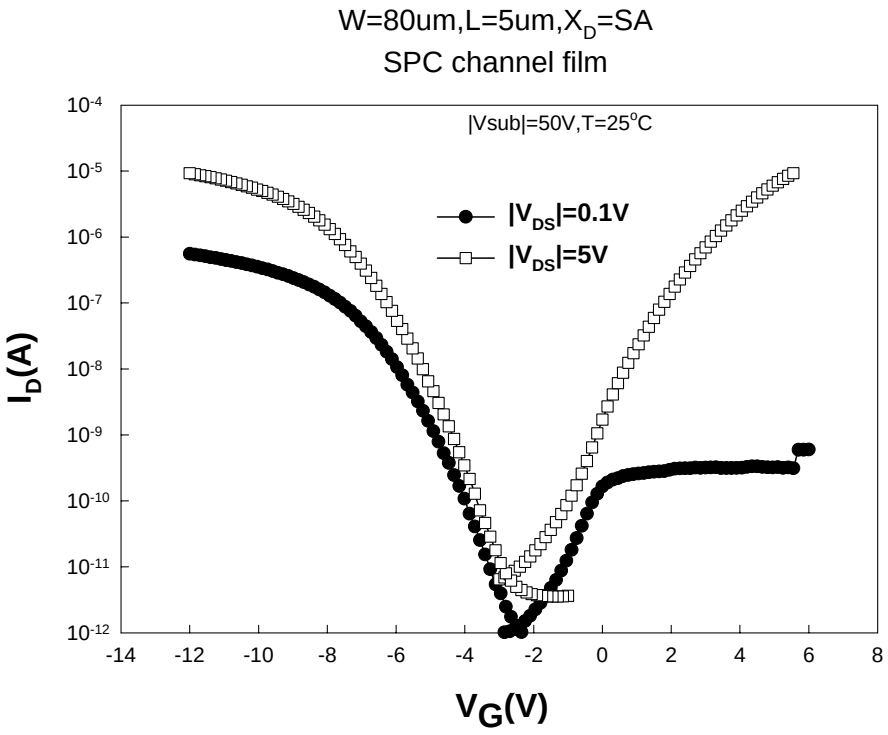


(a)

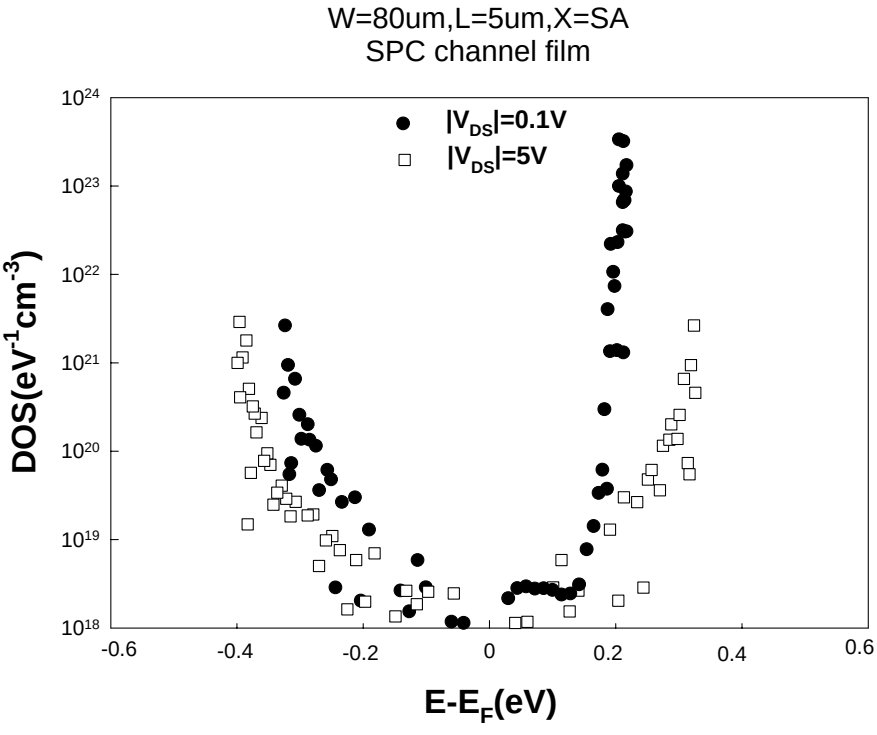


(b)

Fig.3.11 (a) Ambipolar transfer characteristics and (b) the extracted DOS results in a device with channel length of 2um.



(a)



(b)

Fig.3.12 (a) Ambipolar transfer characteristics and (b) the extracted DOS results in a device with channel length of 5um.

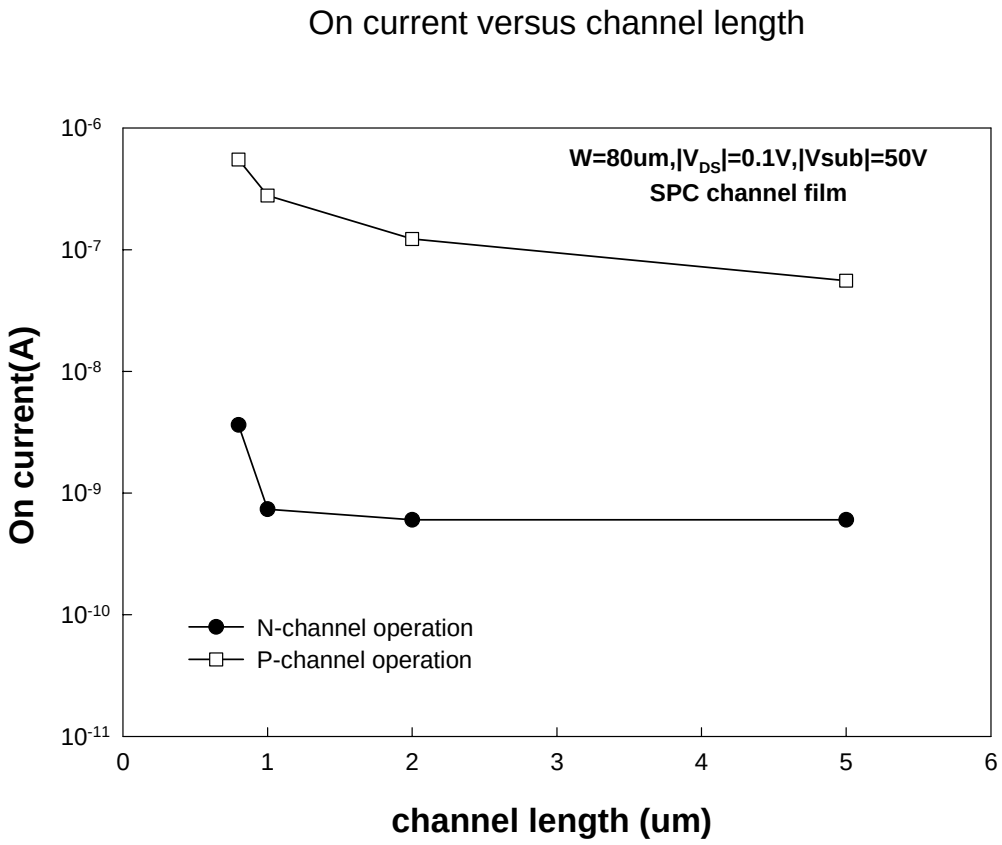
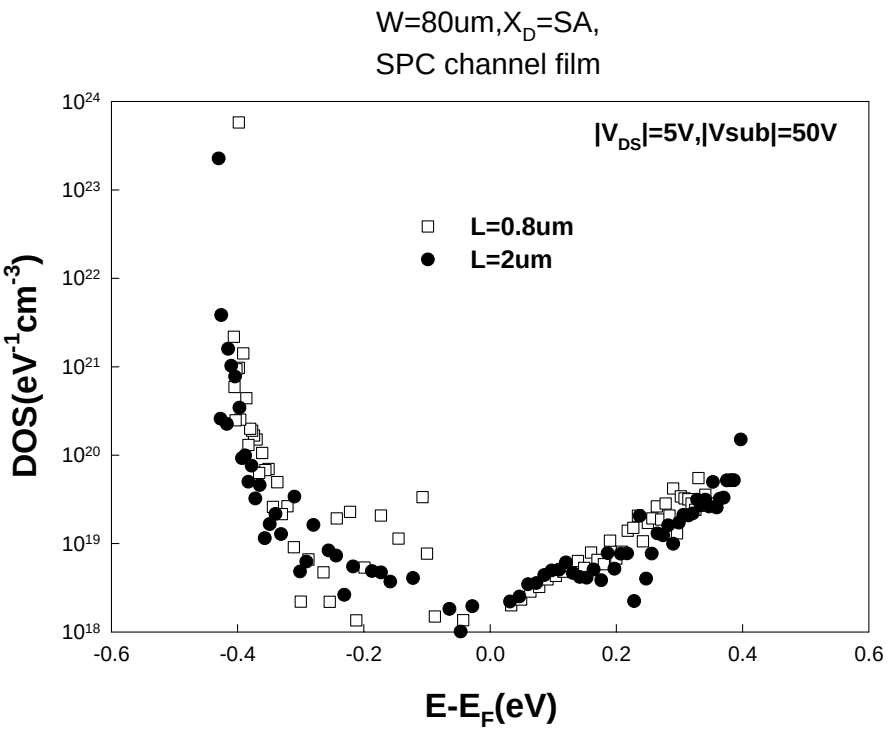
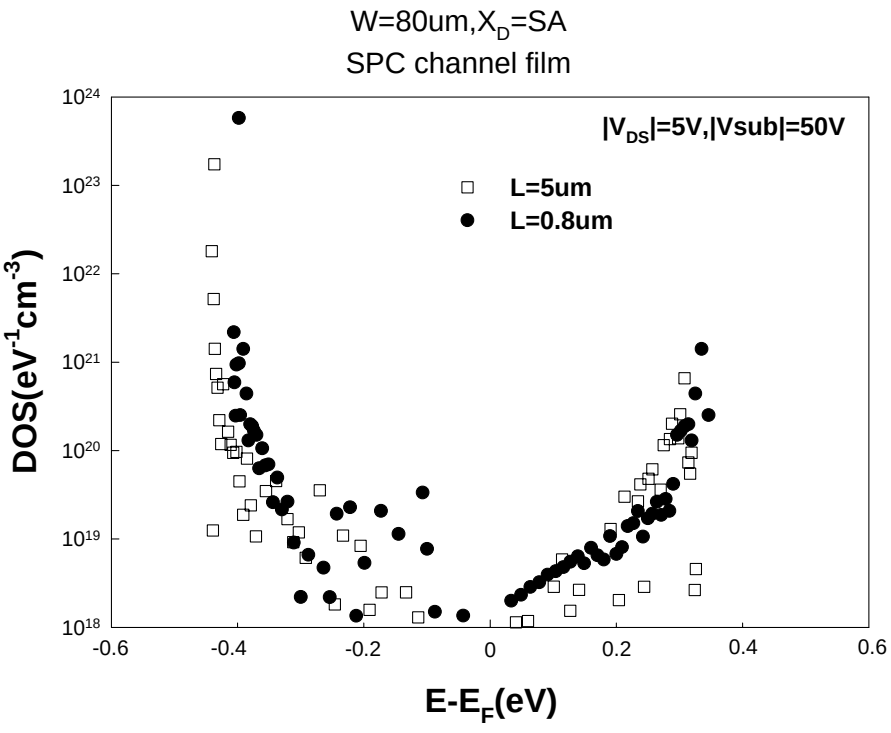


Fig.3.13 On current vs. channel length.

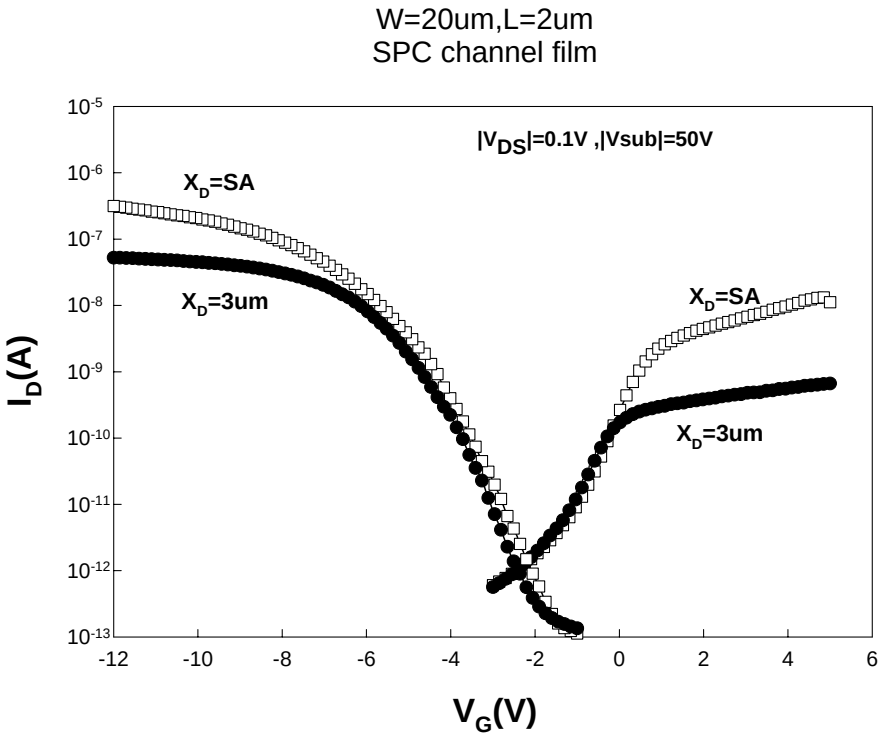


(a)

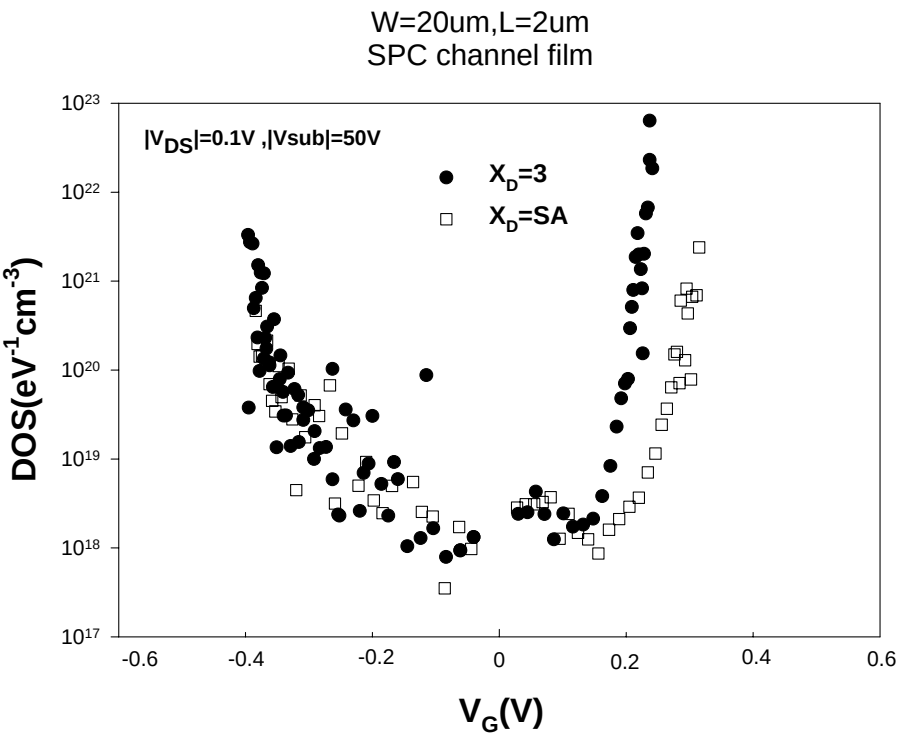


(b)

Fig.3.14 (a), (b) Comparison of DOS extracted in devices with various channel length.

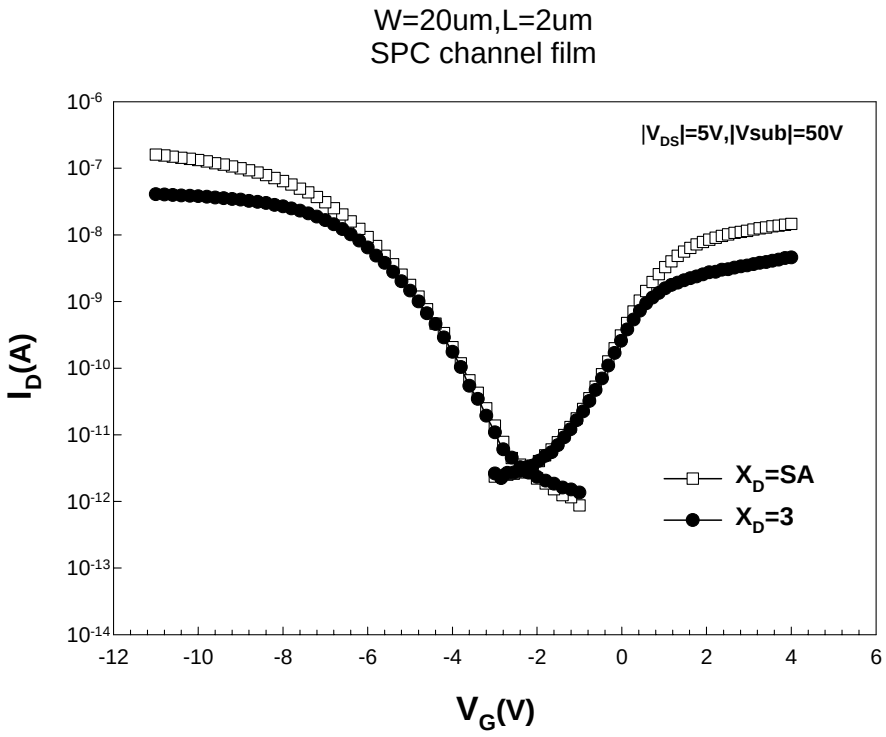


(a)

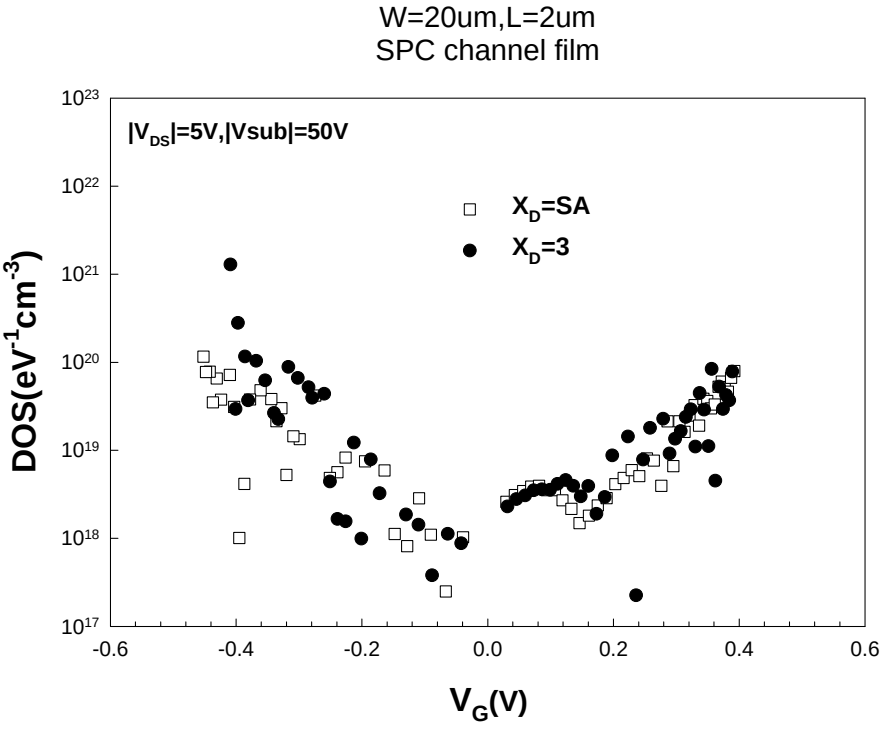


(b)

Fig.3.15 (a) Ambipolar transfer characteristics of deices with various drain-side offset length at $|V_{DS}|$ of 0.1 V. (b) Full band-gap DOS extracted deices with various drain-side offset length at $|V_{DS}|$ of 0.1 V.



(a)



(b)

Fig.3.16 (a) Ambipolar transfer characteristics of deices with various drain-side offset length at $|V_{DS}|$ of 5 V. (b) Full band-gap DOS extracted deices with various drain-side offset length at $|V_{DS}|$ of 5 V.

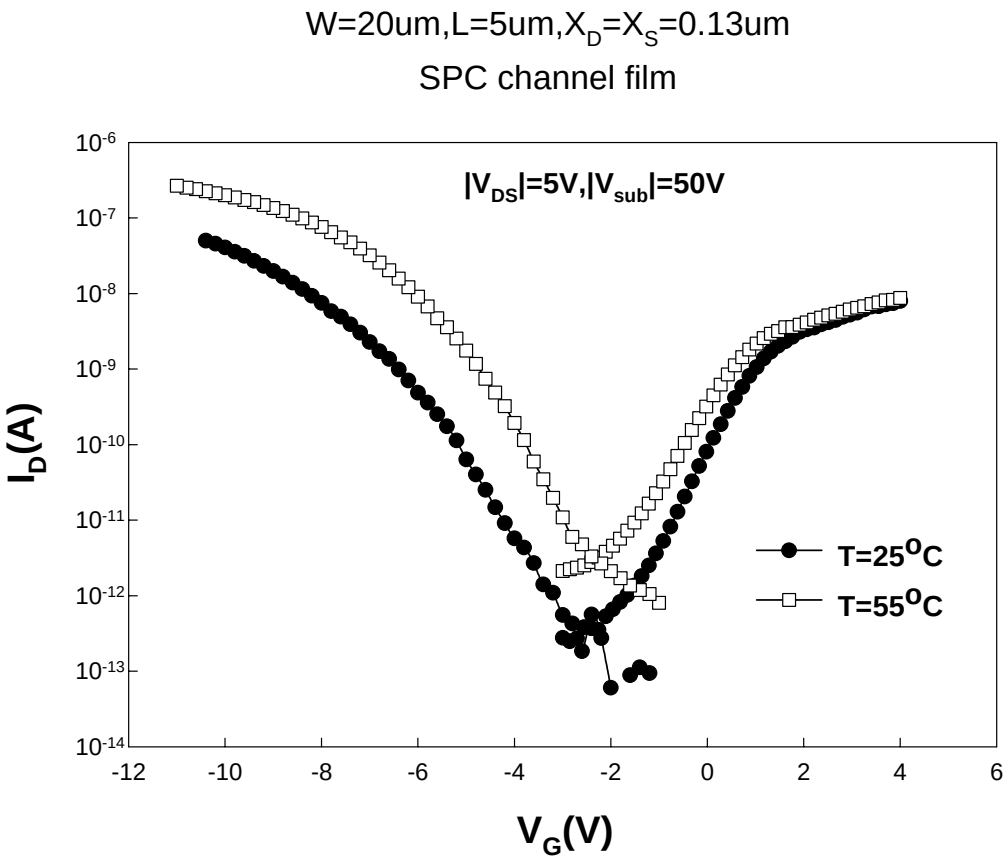


Fig.3.17 Ambipolar transfer characteristics measured at 25 and 55 ^{o}C.

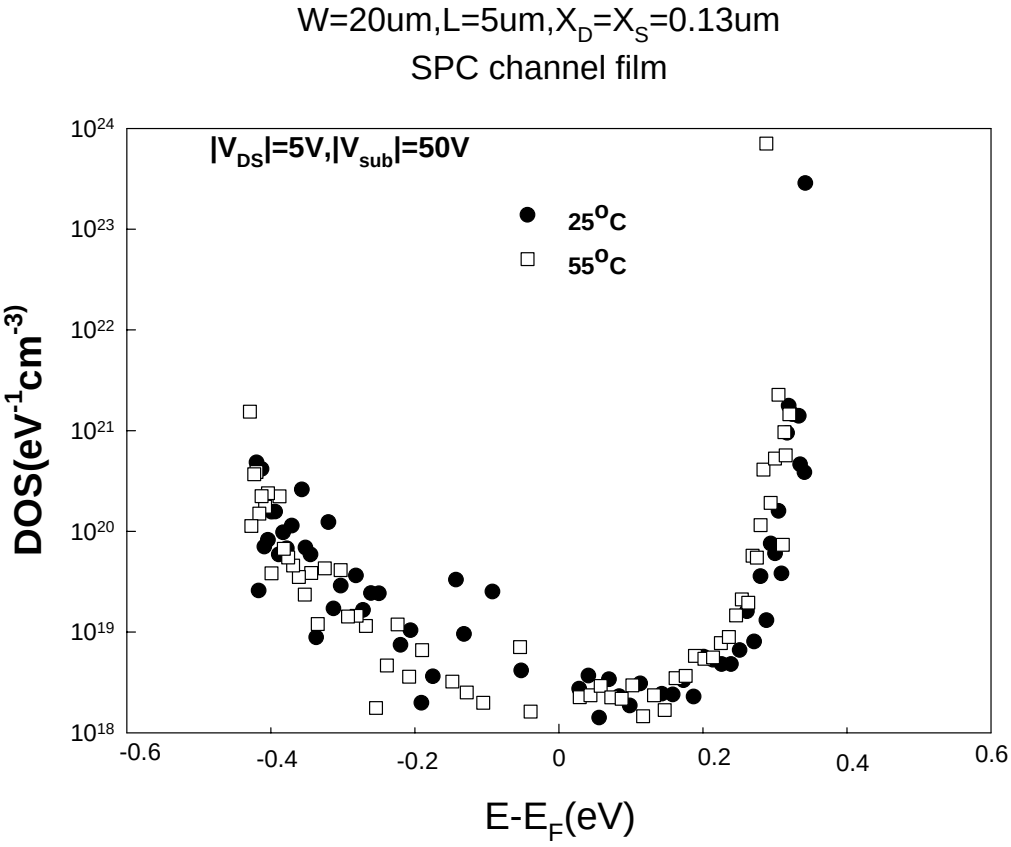


Fig.3.18 DOS extracted at 25 and 55 ^{o}C.

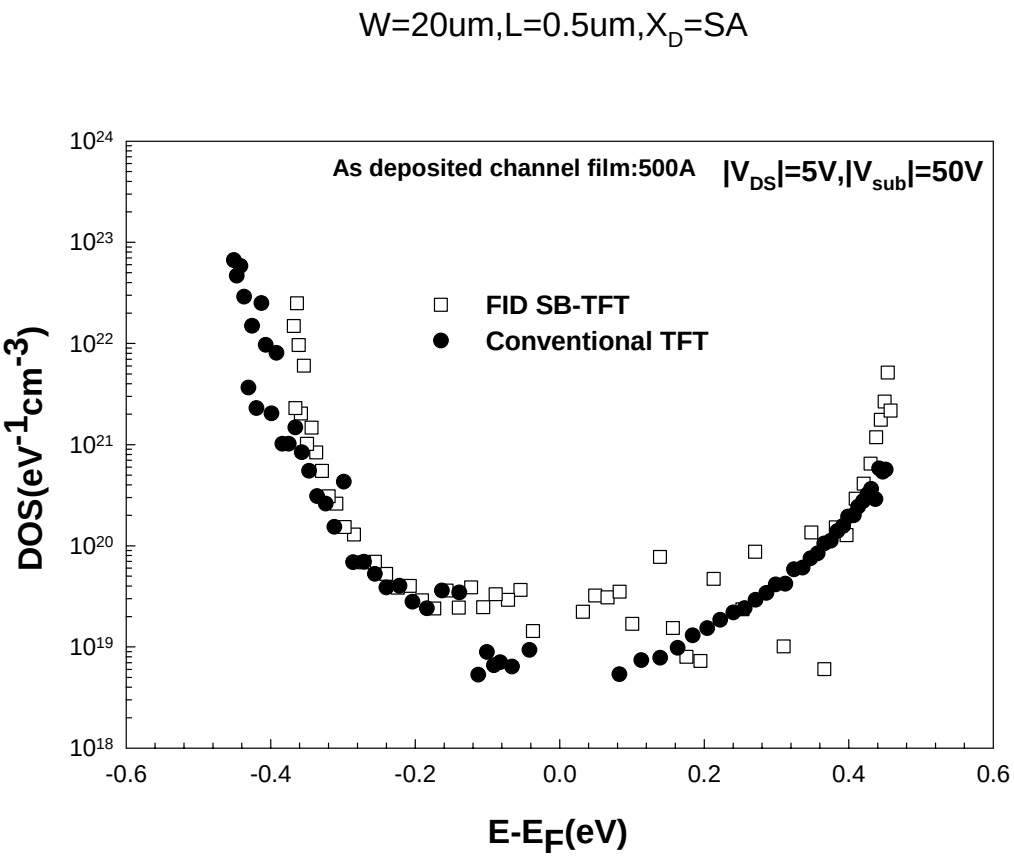


Fig.3.19 Comparison of DOS extracted from FID SB-TFT and Conventional TFTs.

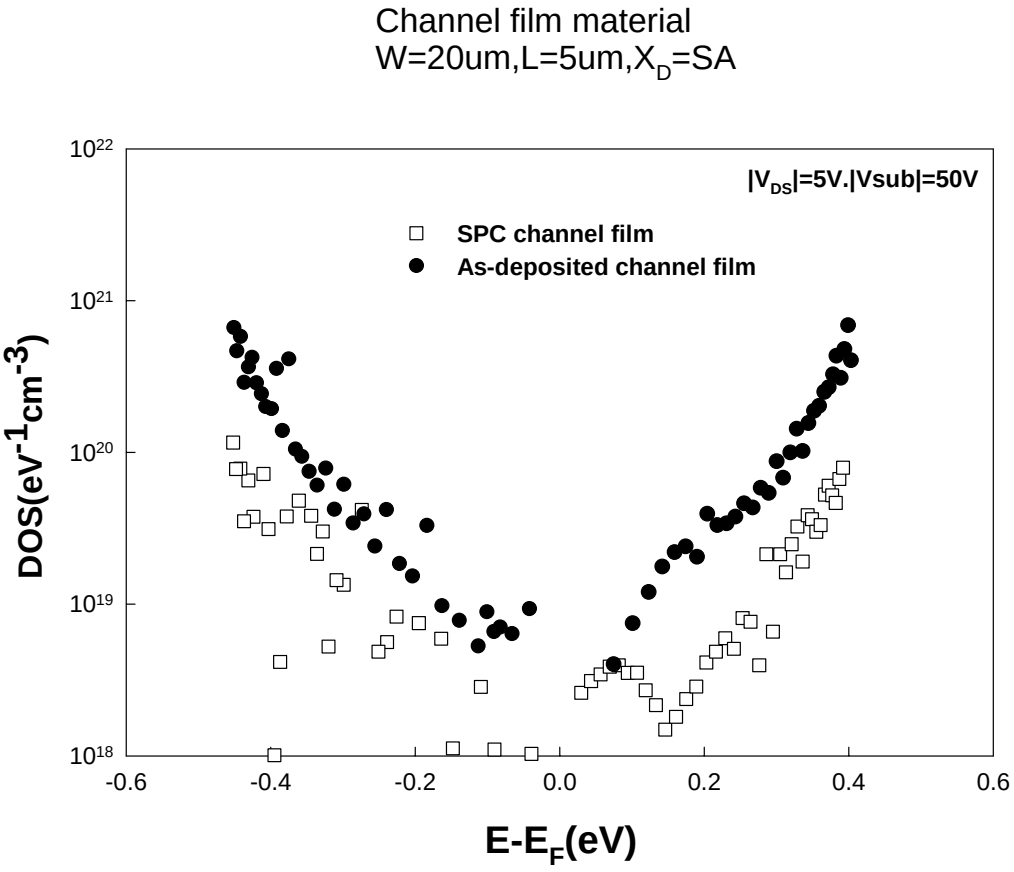
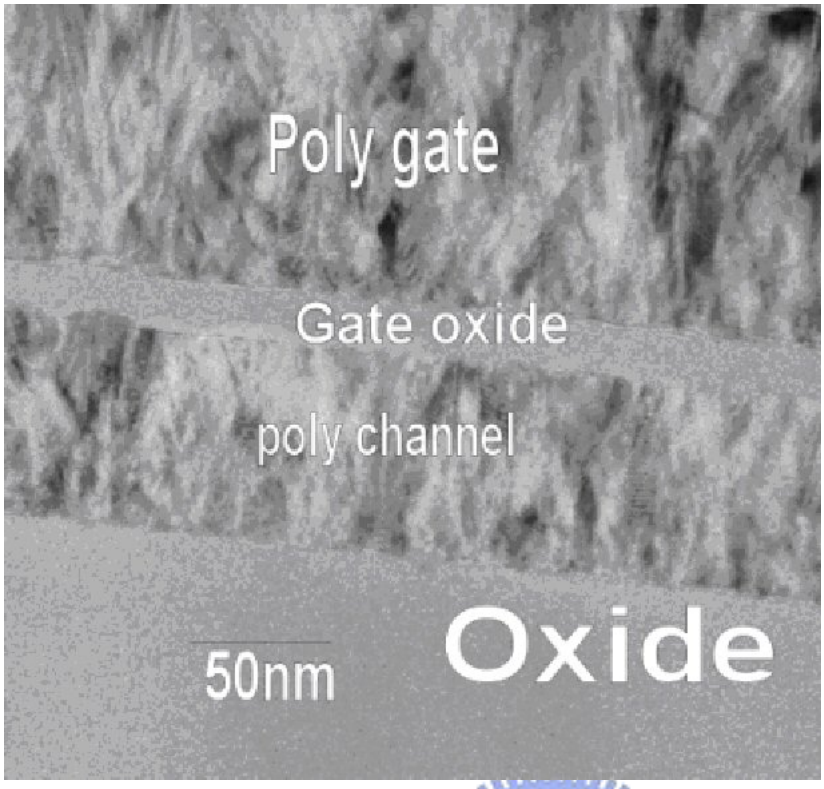
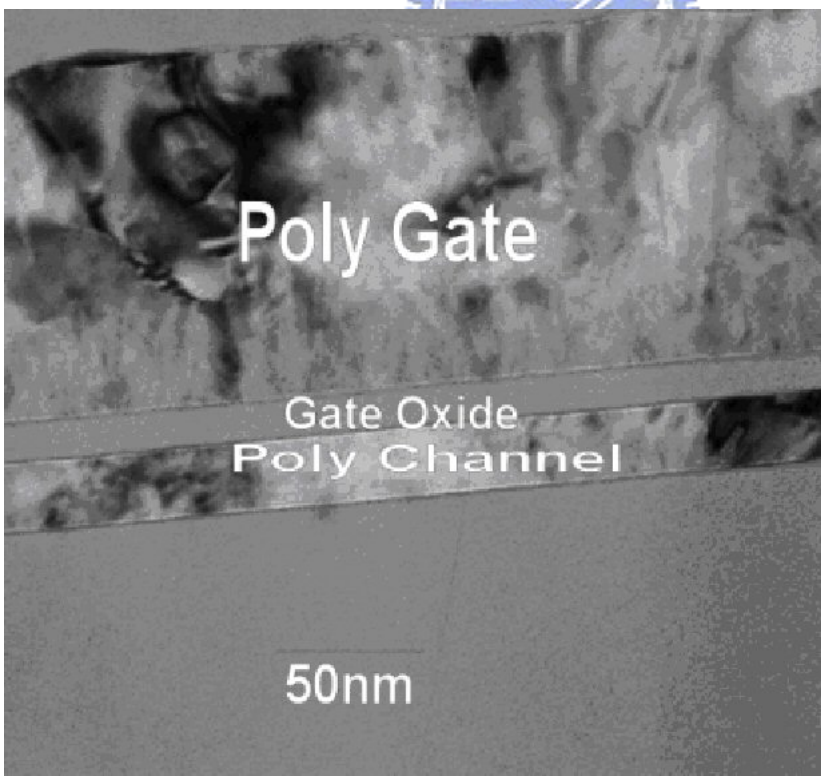


Fig.3.20 Full band-gap DOS of devices with SPC or as-deposited poly-Si channel.



(a) As-deposited channel film



(b) SPC channel film

Fig.3.21 TEM micrographs of device with (a) as-deposited poly-Si and (b) SPC channel film.

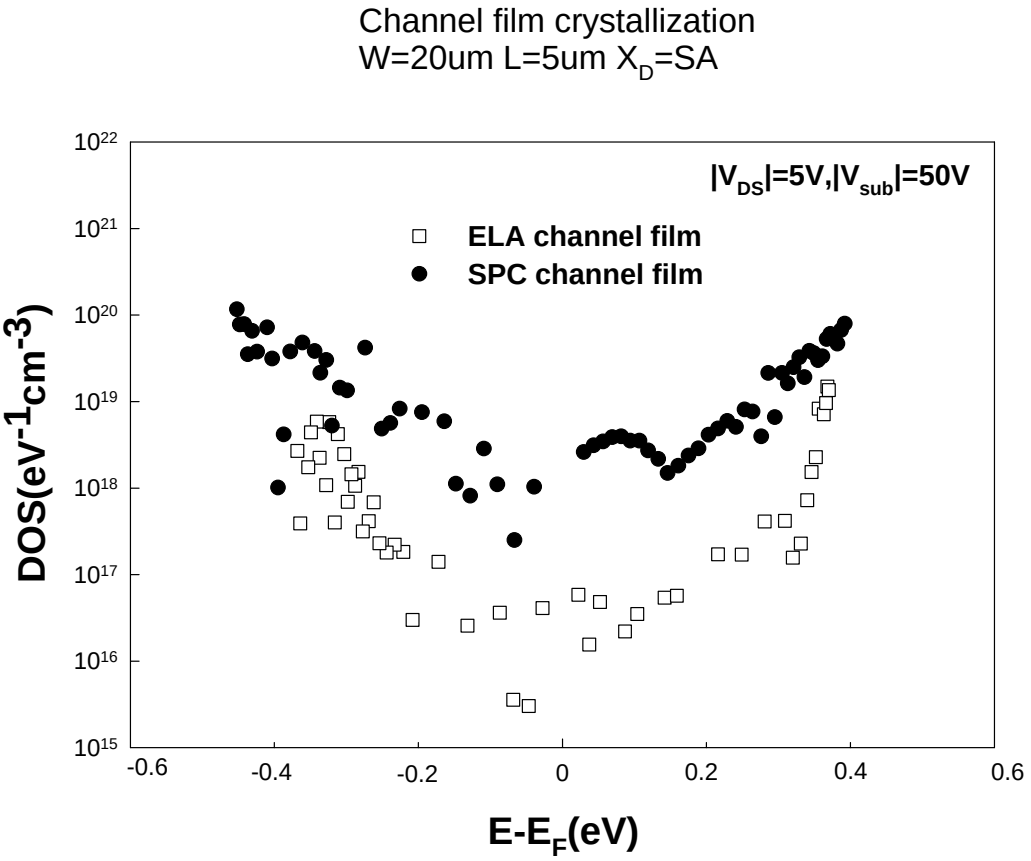


Fig.3.22 Full band-gap DOS of devices with SPC or ELA poly-Si channel.

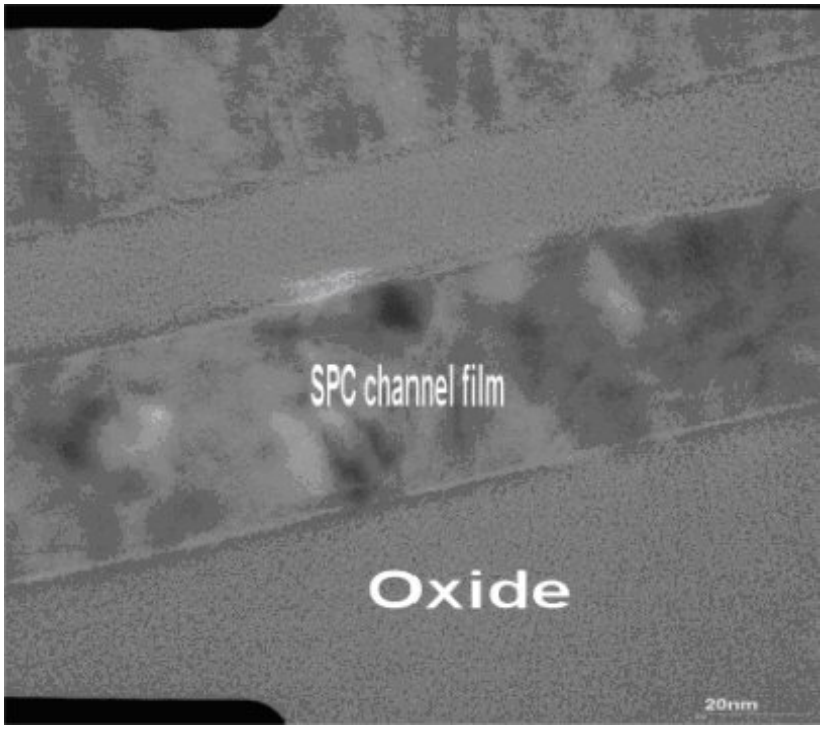
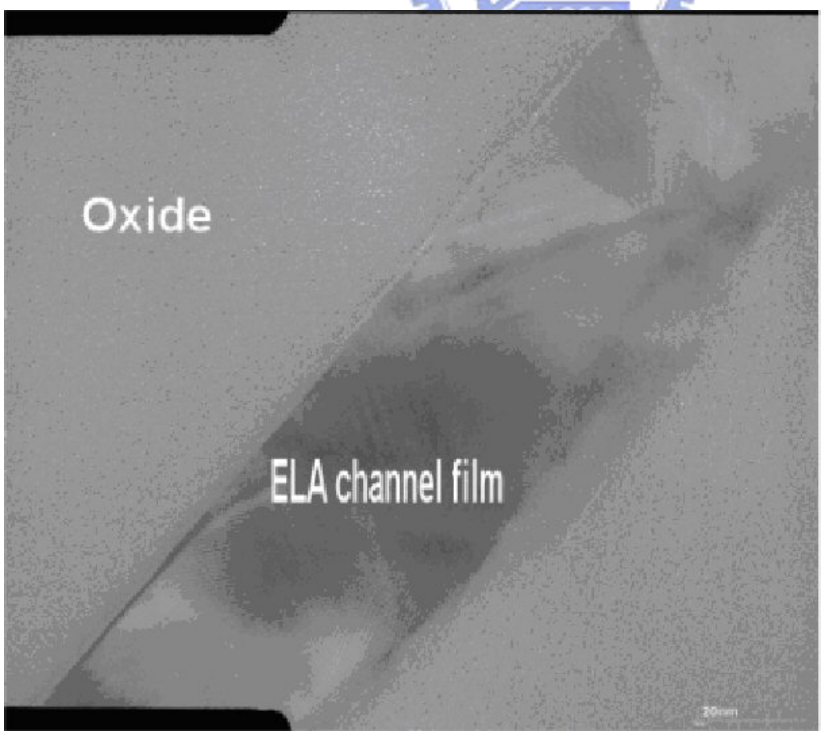


Fig.3.23 (a) TEM micrograph of SPC channel film.



(b)

Fig.3.23 (b) TEM micrographs of ELA channel film.

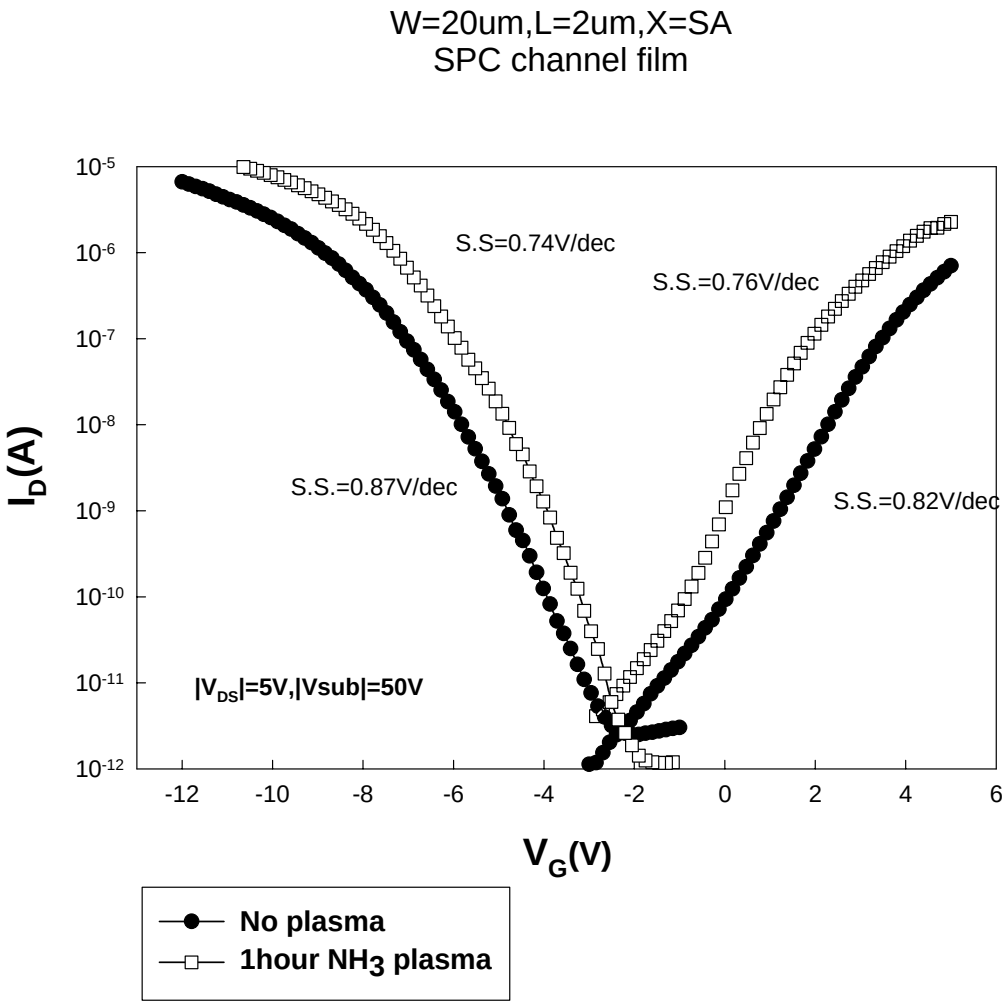


Fig.3.24 Ambipolar transfer characteristics of devices with and without plasma treatment.

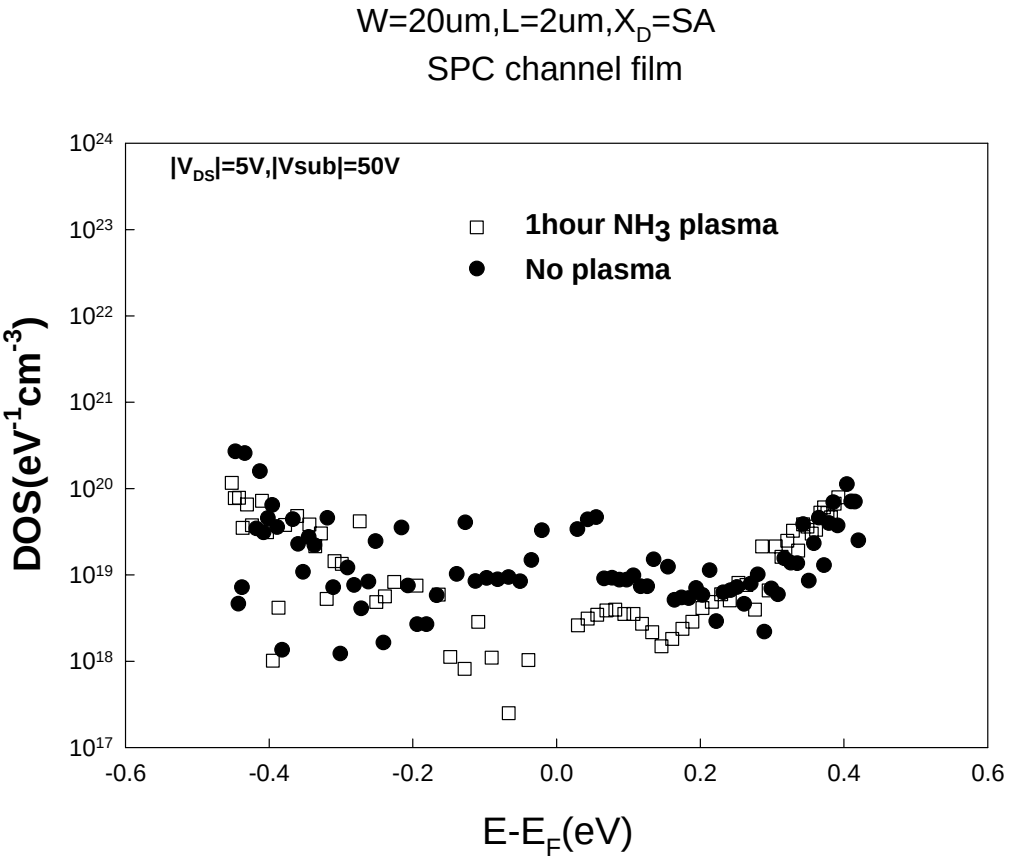


Fig.3.25 Full band-gap DOS before and after hydrogenation in devices with SPC channel.

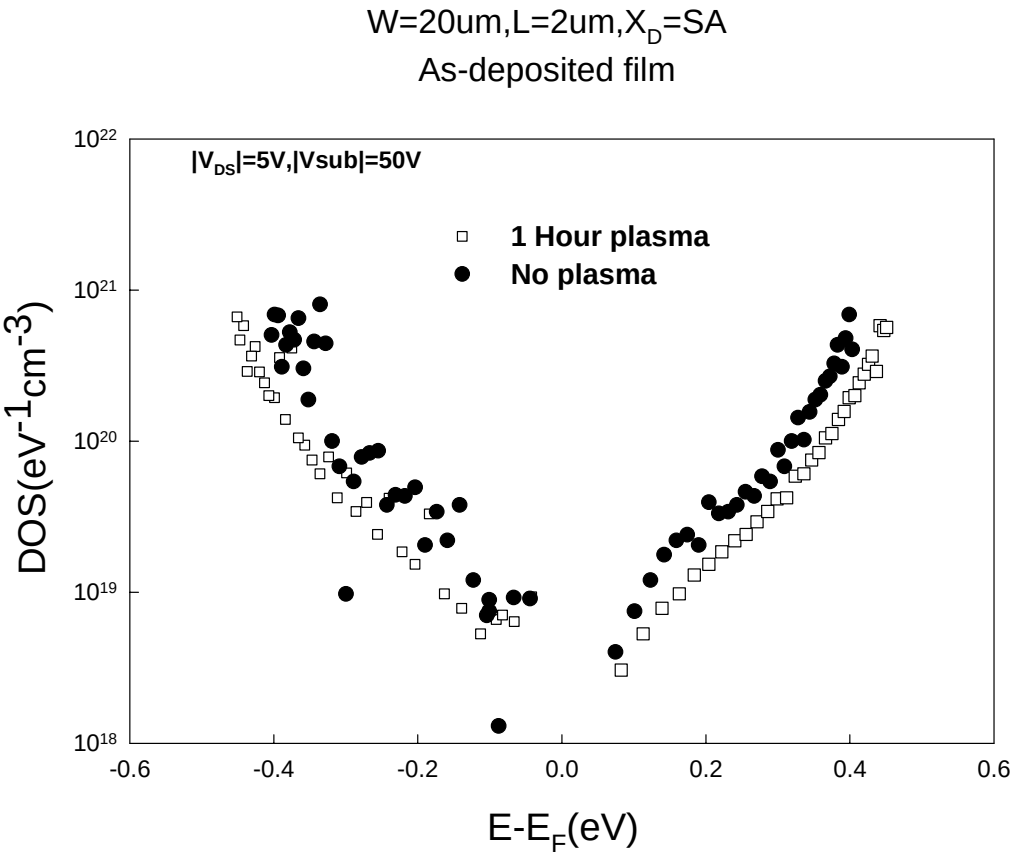


Fig.3.26 Full band-gap DOS before and after hydrogenation in devices with as-deposited poly-Si channel.

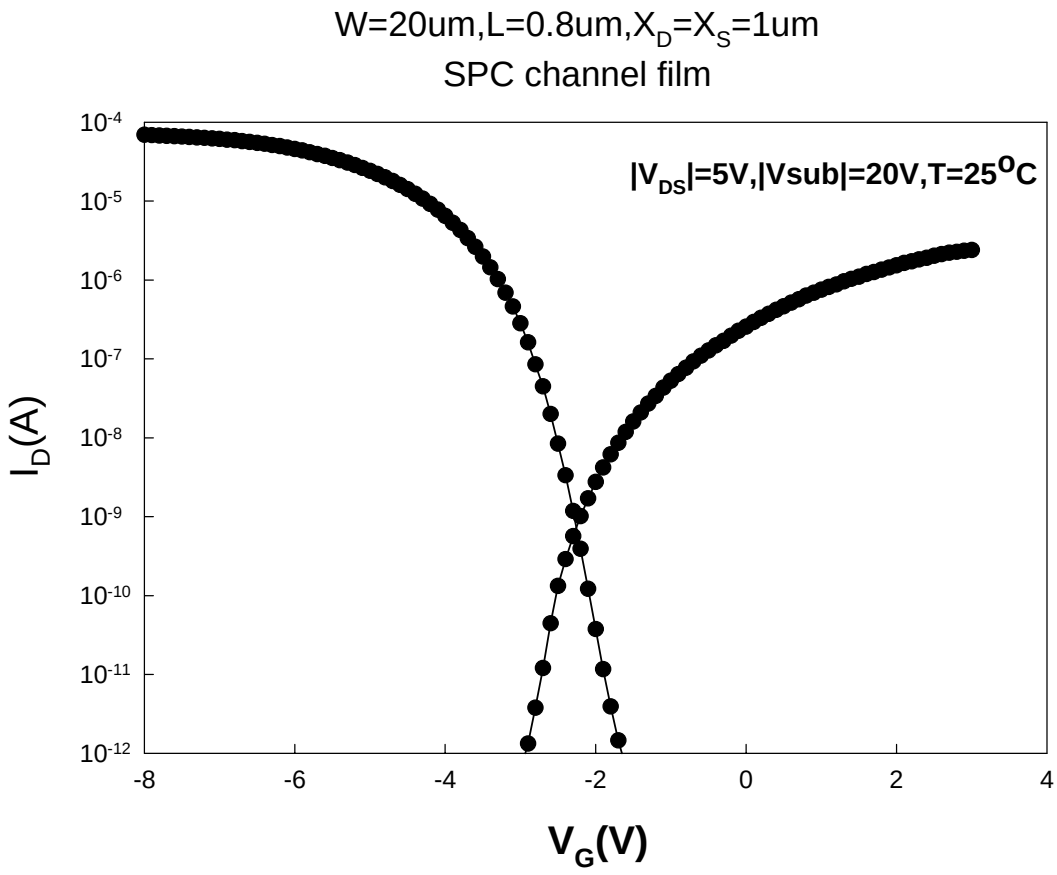


Fig.3.27 Ambipolar transfer characteristics of a device with PtSi S/D.

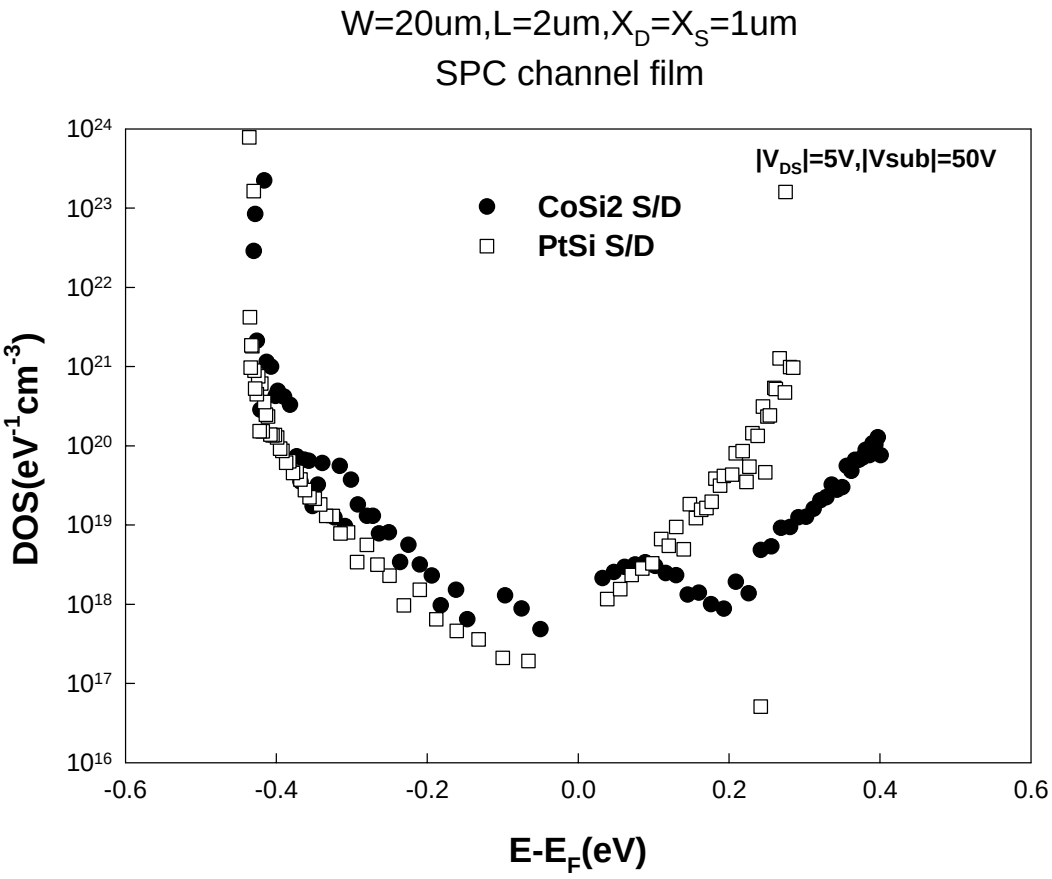
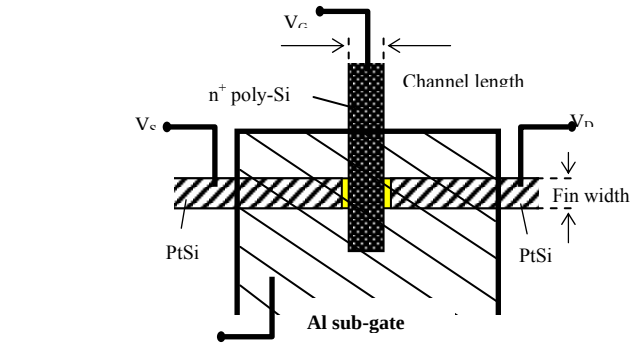
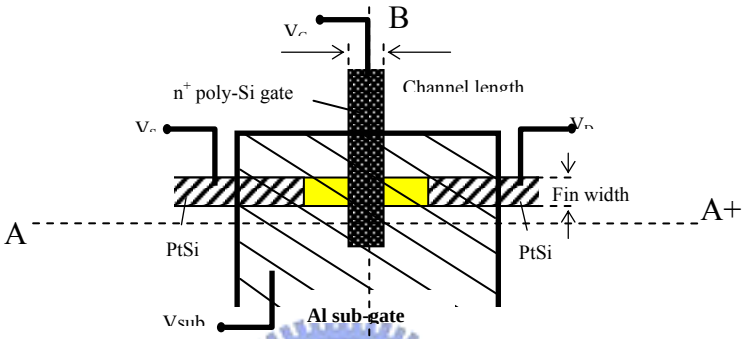


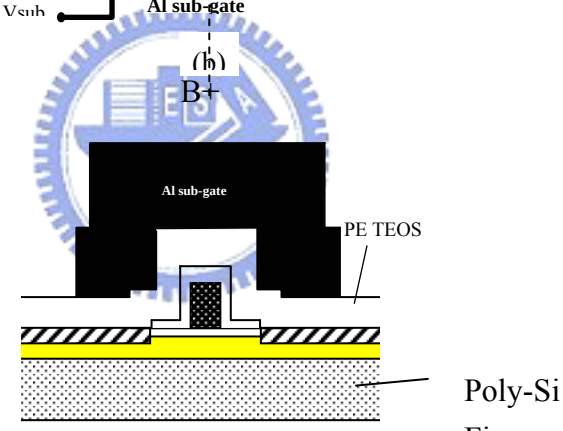
Fig.3.28 Full band-gap DOS of devices with $CoSi_2$ or PtSi S/D.



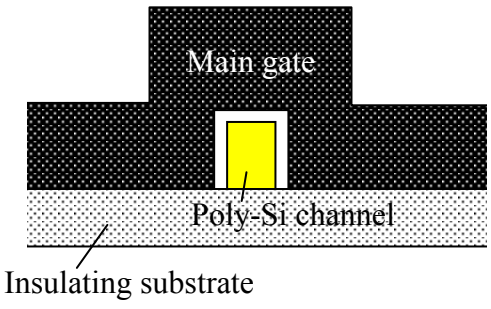
(a)



(b)



(c)



(d)

Fig.3.29 (a) Top view of poly-Si SB FinFET with self-aligned spacer; (b) Top view of poly-Si SB FinFET with offset region X_D and X_S. (c) Cross section view along A-A+ direction in (b); (d) Cross section view along B-B+ direction in (b).

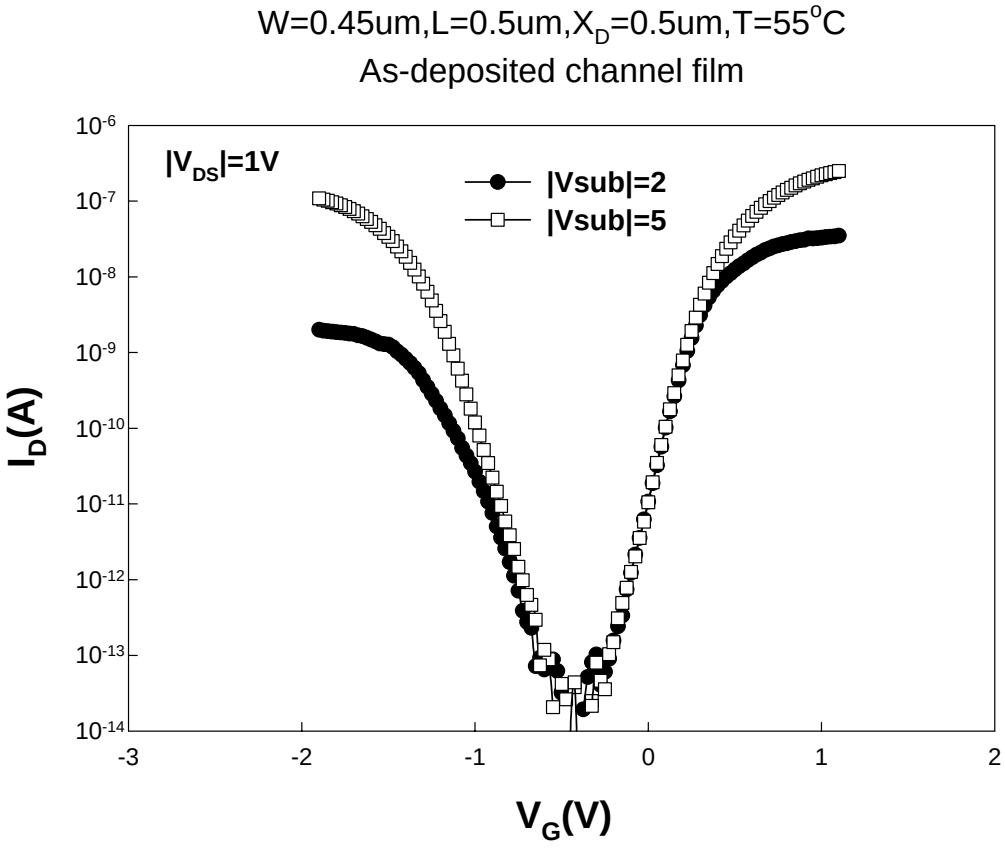
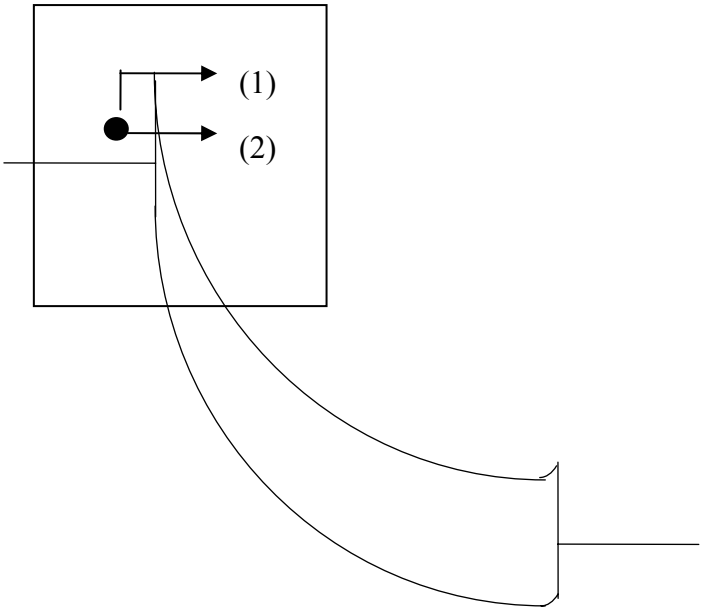


Fig.3.30 Ambipolar transfer characteristics of a SB poly-Si FinFET.



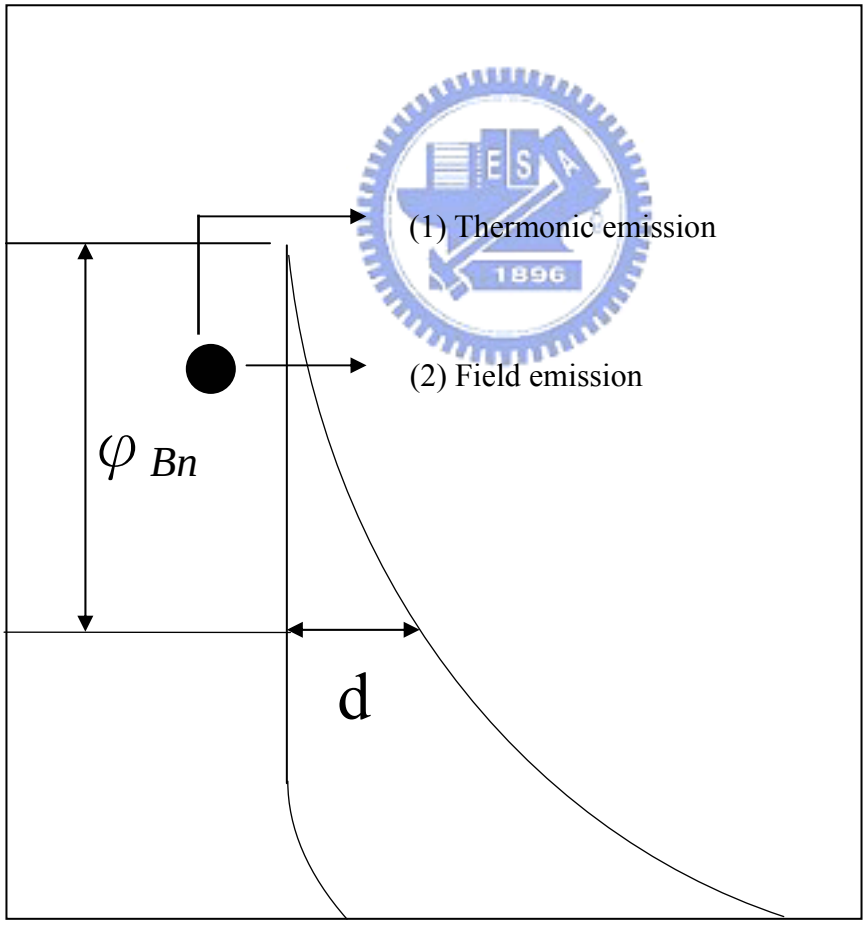


Fig 3.31 Higher sub-gate bias enhances the source-side field emission [14].

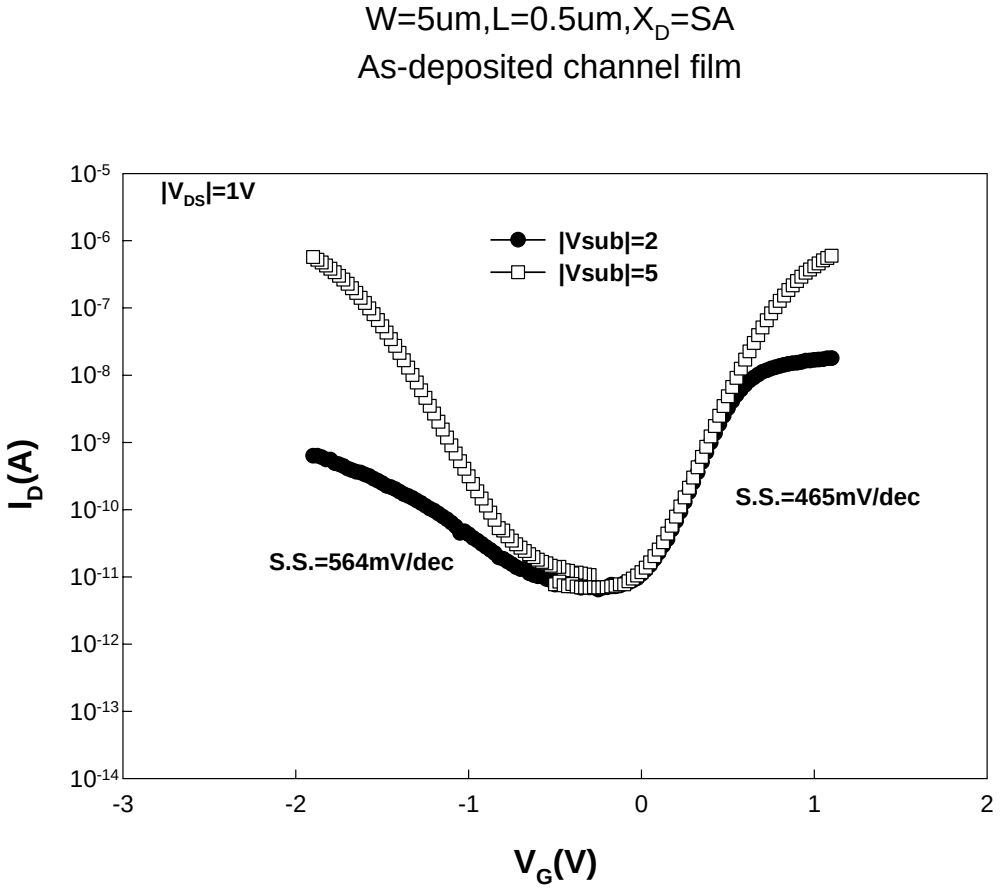


Fig.3.32 Ambipolar transfer characteristics of SB poly-Si TFT with planar structure.

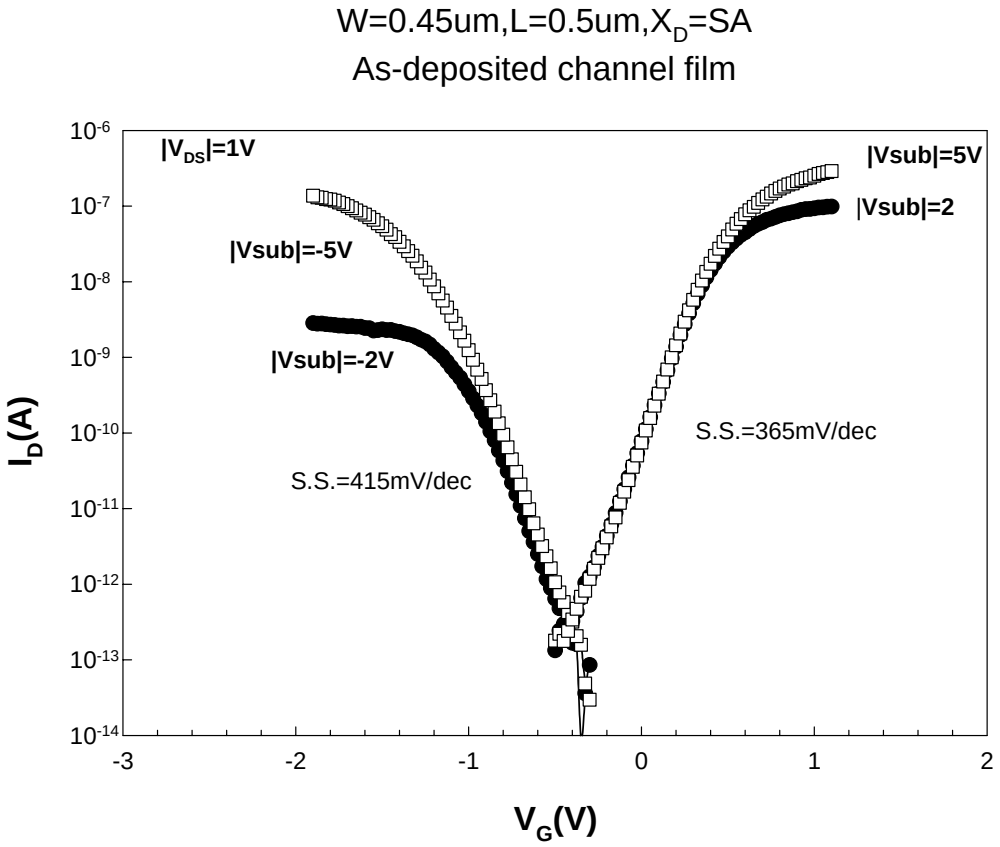
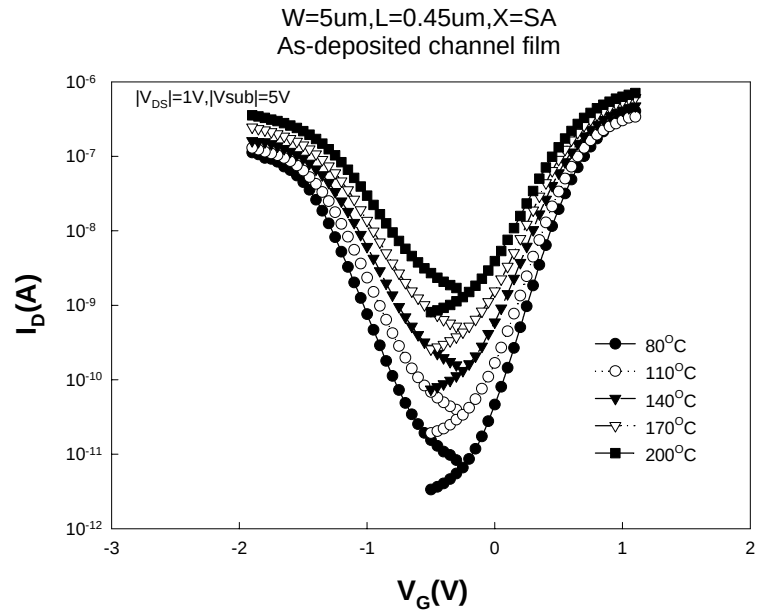
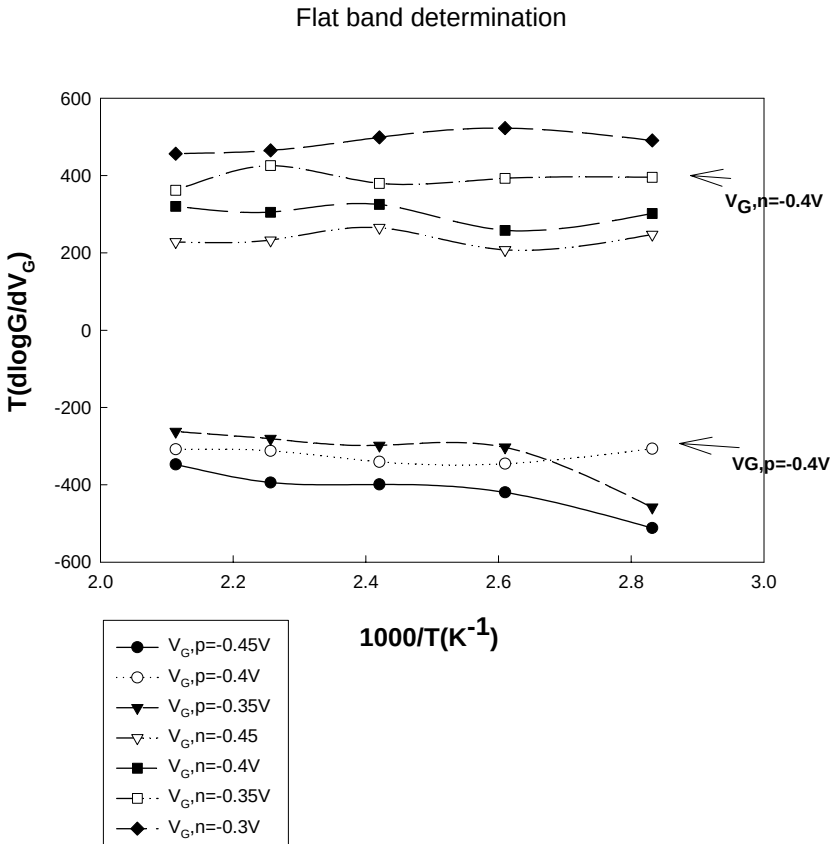


Fig.3.33 Ambipolar transfer characteristics of a SB poly-Si FinFET.



(a)



(b)

Fig.3.34 (a) Ambipolar transfer characteristics of a SB poly-Si FinFET measured at varying temperature, (b) Flat band voltage determination.

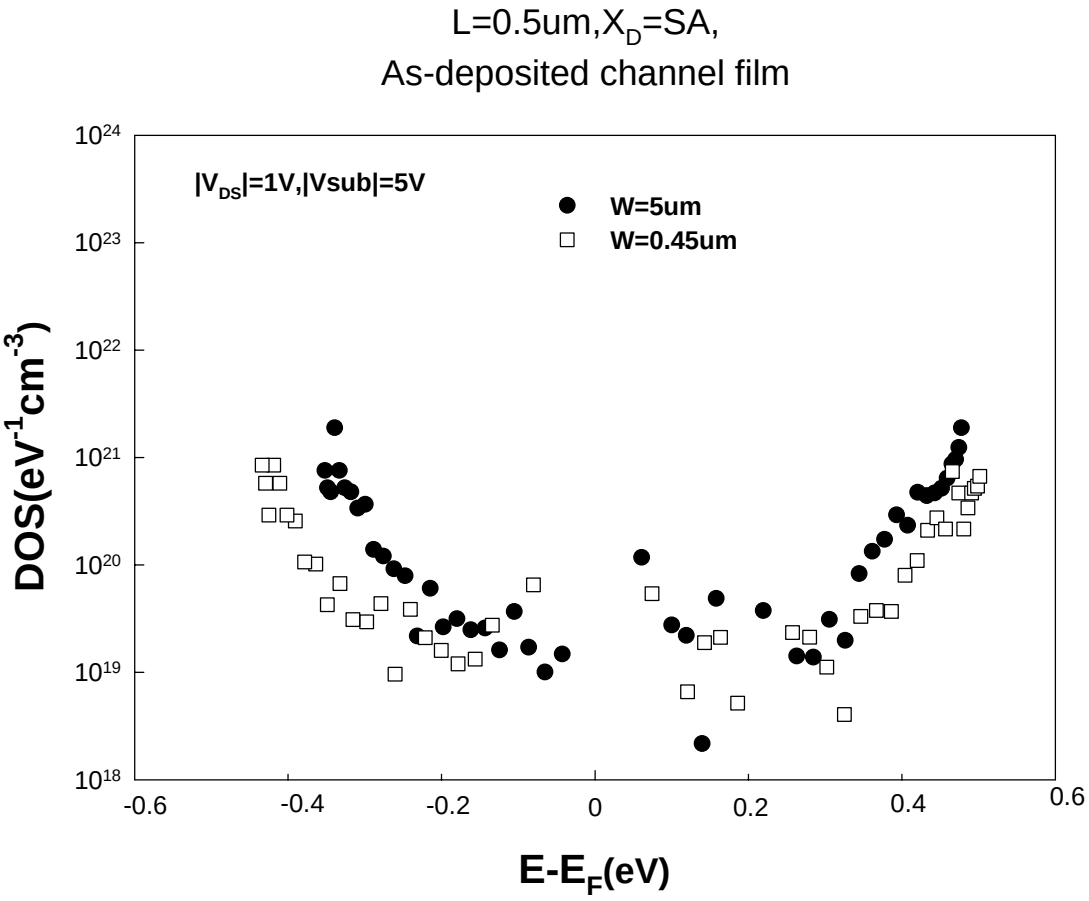


Fig.3.35 Full-band gap DOS of planar SB -TFT and SB FinFET.

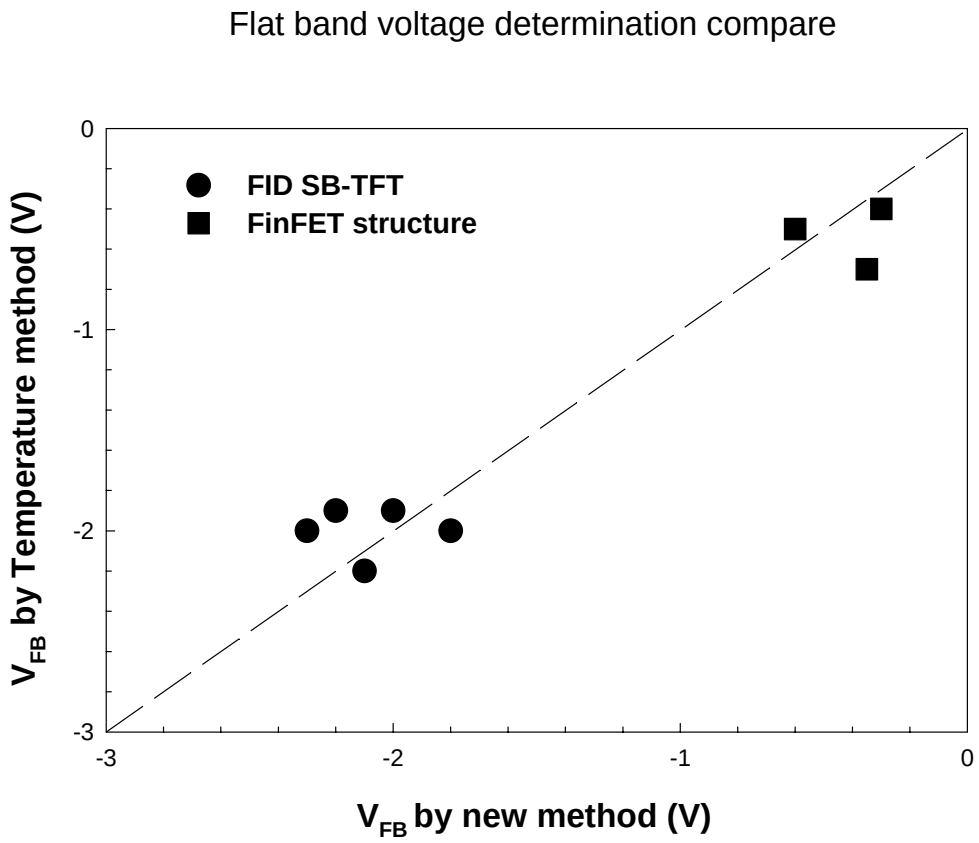


Fig.3.36 Comparison of flat-band voltage determined by conventional temperature method and our new method.

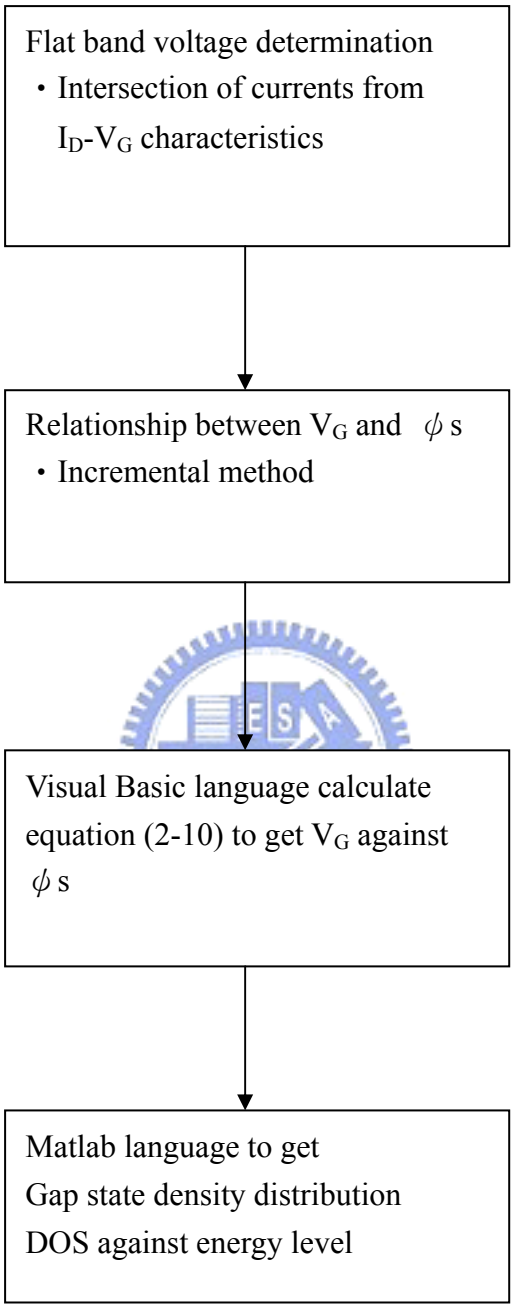


Fig.3.37 Modified Flow chart for determination of DOS density distribution.

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論文題目:一種分析薄膜電晶體內完整能帶隙態位密度分佈的新穎方法

A NOVEL METHOD TO ANALYZE FULL BAND-GAP DENSITY OF STATES DISTRIBUTION IN THIN FILM TRANSISTORS