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氮化矽記憶元件內電荷分佈
與可靠性分析

Localized Charge Distribution and Read Current Noise in Nitride Storage Flash Cells

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中華民國 九十三 年 六 月

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摘要

本篇論文主要著重於氮化矽記憶元件內儲存電荷分佈以及讀取電流不穩定等可靠性議題之討論。這些可靠性議題主要包括：寫入狀態電荷之橫向分佈（program charge lateral spread)、寫入動作干擾（program disturb effect)、以及讀取電流雜訊（read current noise)。而在此研究中，氮化矽記憶元件為一 n 型通道金氧半場效電晶體包含一 ONO 閘極結構。

由於雙位元操作，逆向讀取第二位元之臨界電壓時，可能受到第一位元儲存電荷的干擾，故控制儲存電荷分佈為一重要可靠性議題，我們以電荷幫浦方法 (charge pumping)得以一窺氮化矽層中儲存電荷之分佈情形。此外，建立一套微秒暫態量測電路（micro-second transient measurement circuit)，藉著此電路的輔助，我們將得以觀測短時間因寫入動作干擾所引發的可靠性議題，並研究因隨機雜訊所引發之讀取電流不穩定，此一不穩定現象會隨著寫入/抹除次數增加和閘極長度微縮而變差。且利用通道熱電子所寫入之不均勻電荷分佈亦會擴大其效應。憑藉在本篇論文中所提及之氧化層改進方法，此種負面現象將得以舒緩。

Localized Charge Distribution and Read Current Noise in Nitride Storage Flash Cells

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Abstract.

This thesis will focus on the discussion of localized trapped charge distribution in nitride film and read current instability issue in a SONOS type flash memory cell, which include program charge lateral spread, program disturb effect, and read current noise. In this study, the flash memory cell is made of a n-channel MOSFET with an oxide-nitride-oxide gate structure.

For two-bit storage, the control of programmed charge lateral distribution is particularly important since stored electrons at the first bit will affect the threshold voltage of the second bit in reverse read. We use a charge pumping method to explore the programmed charge distribution of each bit. In addition, a micro-second transient measurement circuit is set up to investigate the program disturb effect. Furthermore, program/erase cycling induced random

telegraph noise in read current noise is observed. The amplitude of current fluctuation increases with P/E cycle number and with decreasing gate length. Non-uniform charge storage by CHE programming can further enhance read current fluctuation. The improvement of bottom oxide reliability can significantly reduce this effect.

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成長，就是尋找自己的旅程。感謝曾經一同走過的許多學長，及參與研究的同學。首先感謝蔡慶威、吳俊威學長在研究生活中的鼓勵與指導；感謝小凱、小翎學長、及兆琪學姐，有你們的陪伴，在嚴肅的學問鑽研中增添輕鬆愉悅的氣氛。學識上的傾囊相授與人生經驗的交流，特別感謝陳旻政學長，由衷地。感謝志昌、建文、子強、信榮、政賢及文雄的陪伴，一起走過精彩的兩年。

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五十多頁的文字，承載七百多個日子滿滿的回憶。

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Chapter 1
Introduction

Currently, two major research thrusts in nonvolatile semiconductor memory are underway. One has data stored in a multi-layer gate structure in a field effect transistor and the other takes advantage of electrical polarization of ferroelectric material in a ferroelectric capacitor/transistor [1]. With respect to charge storage devices, there are two kinds of them. (a) Charge Trapping Devices: Charge is stored in traps at the interface of a multi-layer gate structure and/or in the bulk of insulator, such as the metal nitride oxide silicon (MNOS) structure [2], [3]. (b) Floating Gate Devices: Charge is stored in a thin conducting or semiconductor layer or conducting particles sandwiched between insulators [4], [5].

However, since its invention in 1967, the nitride-based nonvolatile memory structures, both MNOS and polysilicon oxide-nitride-oxide silicon (SONOS) [6]-[10], have received limited commercial acceptance due to their employment of ultra-thin dielectric (~20Å) and their non-ideal charge retention characteristics. In conventional SONOS cells, charges are stored uniformly in the nitride layer. This SONOS concept has recently evolved into a two-bit storage cell (NROM).

Recently, the new SONOS flash EEPROM cell has soon gained great attention for their smaller size per bit (2.5F^2/bit in Flash, where F is the feature size of the process) [11], [12], less fabrication complexity [13], no drain turn-on and better charge retentivity [14] This SONOS cell is made of a n-channel MOSFET with an oxide-nitride-oxide gate dielectric structure, as shown in Fig.1.1. The major difference between NROM and the conventional SONOS devices [15] is that the bottom oxide is about 60Å [11], which is much thicker than that of SONOS (~20 Å), where direct tunneling is involved for charge transport.

By taking advantage of localized charge storage in the nitride layer above the n^+

source and drain junctions, two-bit per cell operation can be achieved. Channel hot electron injection and band-to-band hot hole injection are utilized for programming and erasing, respectively. Table.1.1 shows the operation bias of program, erase, and read [16]. The I_d-V_{gs} of program state and erase state are shown in Fig.1.2 by using a reverse read method [17], which can be used to “read through” the first bit to obtain the information of the second bit. The sub-threshold swing deterioration in program state is due to a narrow charge trapping region, typically tens of nano-meter.

Because of a thicker bottom oxide and the non-uniformity of charge stored in the nitride layer, the reliability issues in the two-bit storage SONOS cell are quit different from that in the conventional SONOS cells. Charge loss characteristics and cycling endurance of these kind of cells have been discussed, and the models have been proposed [16], [18]-[22].

Following the introduction, the programmed charge lateral spread in the nitride layer will be discussed in chapter two. In chapter three, we will demonstrate a micro-second transient measurement circuit to investigate program disturb effect. Random telegraph noise induced read current fluctuation will be discussed in chapter four. Finally, we will make a conclusion of this thesis.

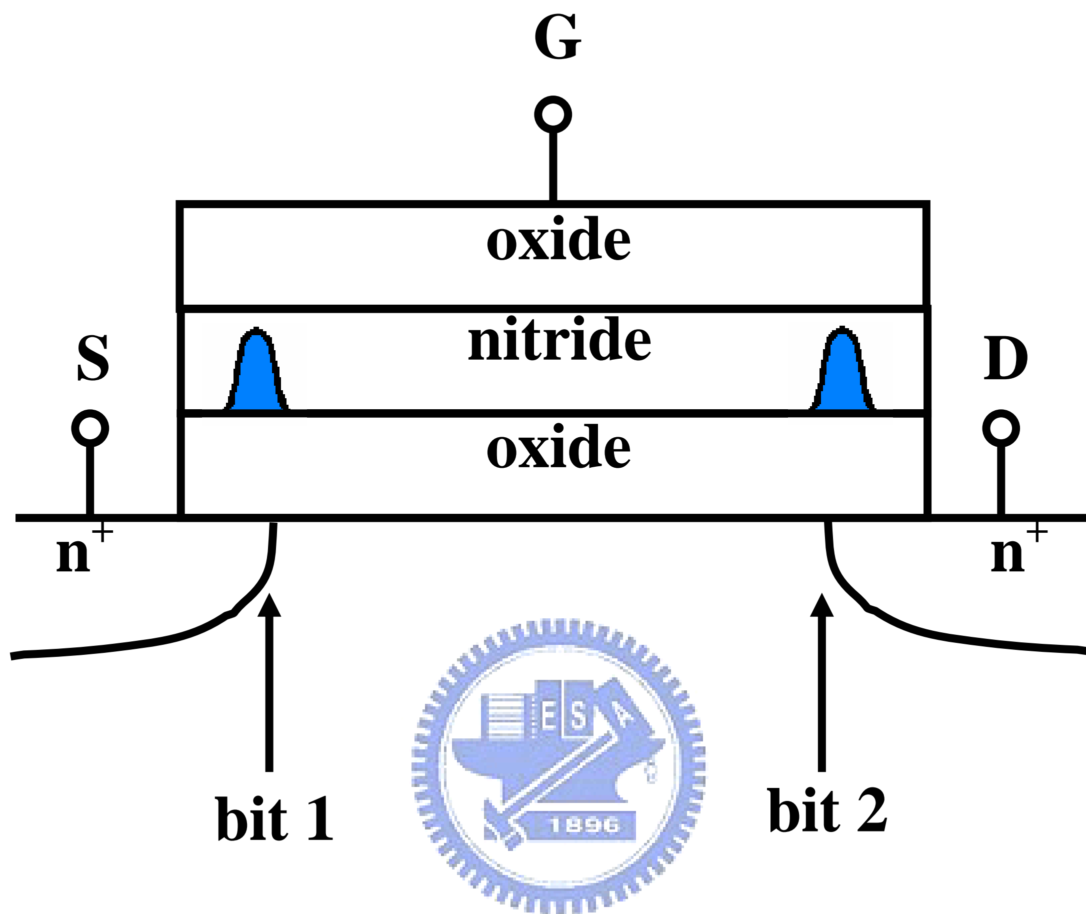


Fig. 1.1 Schematic representation of a SONOS cell and two-bit storage. The shaded area in the nitride layer represents stored charges.

Table.1.1 Suggested bias conditions for MXVAND cell operation.

		Program	Erase	Read
Bit 1	Vg	11V	-3V	2.5V
	Vd	5V	8V	0V
	Vs	0V	0V	>1.5V
Bit 2	Vg	11V	-3V	2.5V
	Vd	0V	0V	>1.5V
	Vs	5V	8V	0V

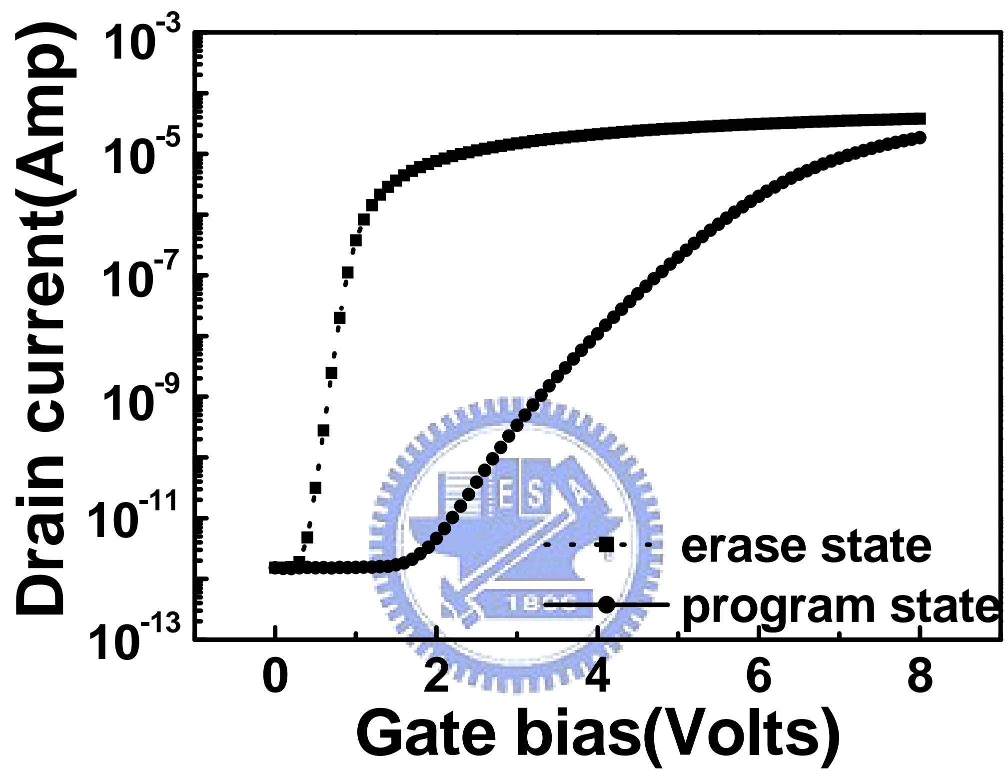


Fig. 1.2 Drain current versus gate bias in erase state and in program state.

Chapter 2
Programmed Charge Lateral Spread

2.1 Introduction

NROM flash cells have received much interest recently due to their smaller bit size, simpler fabrication process and absence of drain induced turn-on. By taking advantage of localized charge trapping in nitride above the source and the drain junctions, two-bit storage of a nitride cell can be achieved by utilizing hot electron program and band-to-band hot hole erase with a reverse read scheme.

For two-bit storage, the control of programmed charge lateral distribution is particularly important. This is because that in 2-bit operation, the stored electrons at the first bit will affect the threshold voltage of the second bit in reverse read and vice versa [23]. Furthermore, the lateral spread of programmed charge will cause a mismatch between programmed electron distribution and injected hole distribution in erase operation, thus resulting in the degradation of erase capability or ease speed [24].

In this work, we will use a modified charge pumping technique to explore the programmed electron distribution in the nitride layer. Moreover, we find that the programmed charge distribution spreads further into channel with program/erase cycle number. Finally, by using this profiling technique, the lateral spread of the first and secondly programmed bits can be characterized, and the cycling induced charge distribution broadening will be investigated.

2.2 Charge Pumping Measurement

The voltage waveforms in our charge pumping (CP) measurement are illustrated in Fig 2.1. We use trapezoidal gate pulses with a fixed V_{gh} and varying V_{gl}. The substrate current (called "charge pumping current (I_{cp})") versus V_{gl} is measured. The

fixed V_{gh} is sufficiently high to ensure that the entire channel is inverted [26]- [29]. By varying V_{gl}, only the part of channel where V_t is lower than V_{gh} can contribute to I_{cp} (Fig 2.2). When the entire channel contributes to the charge pumping current, I_{cp} reaches its maximum value. V_d is adjusted to modulate the drain (or source) depletion width while V_s is floating. The gate pulses have a frequency of 2.5 Mhz and 50% duty cycle. Rising and falling times are 2ns. The samples used in this work have a gate width of 0.35μm and a gate length of 0.5μm.

2.3 Programmed Charge Distribution

2.3.1 First bit Icp

Fig 2.3 shows I_{cp} versus V_{gl} with V_d=0V and source is floating in a fresh cell, in program state and in erase state, respectively. Only the first bit (drain side) is P/E cycled. The threshold voltage window (ΔV_t) is 2V. Here, V_t is defined as the gate voltage when the drain current is 1μA at a reverse read voltage of 1.6V. Note that I_{cp} in a fresh cell and in erase state are almost identical. The negative charge trapping is reflected by an I_{cp} bump in program state. The maximum I_{cp} ($I_{cp,max}$) bump is 195pA at V_{gl}=0V in Fig 2.3. The interface trap density (N_{it}) can be extracted by Eq. (2.1).

$$I_{cp,\max} = qfN_{it}WL_g \qquad (2.1)$$

where q is the elementary charge, f the gate pulse frequency, W the effective channel width, and L_g is the gate length. The program state I_{cp} bump increases with the V_t window because of more injected charges in the ONO layer (Fig 2.4).

The dependence of the program state I_{cp} bump on applied drain bias in charge pumping measurement is shown in Fig 2.5. When a low drain bias is applied, traps underneath the programmed charge are partly masked by the drain depletion region. At a sufficiently large V_d, for example 1.8V, the program state I_{cp} bump is completely suppressed. In contrast, when a V_s is applied in charge pumping measurement, the I_{cp}

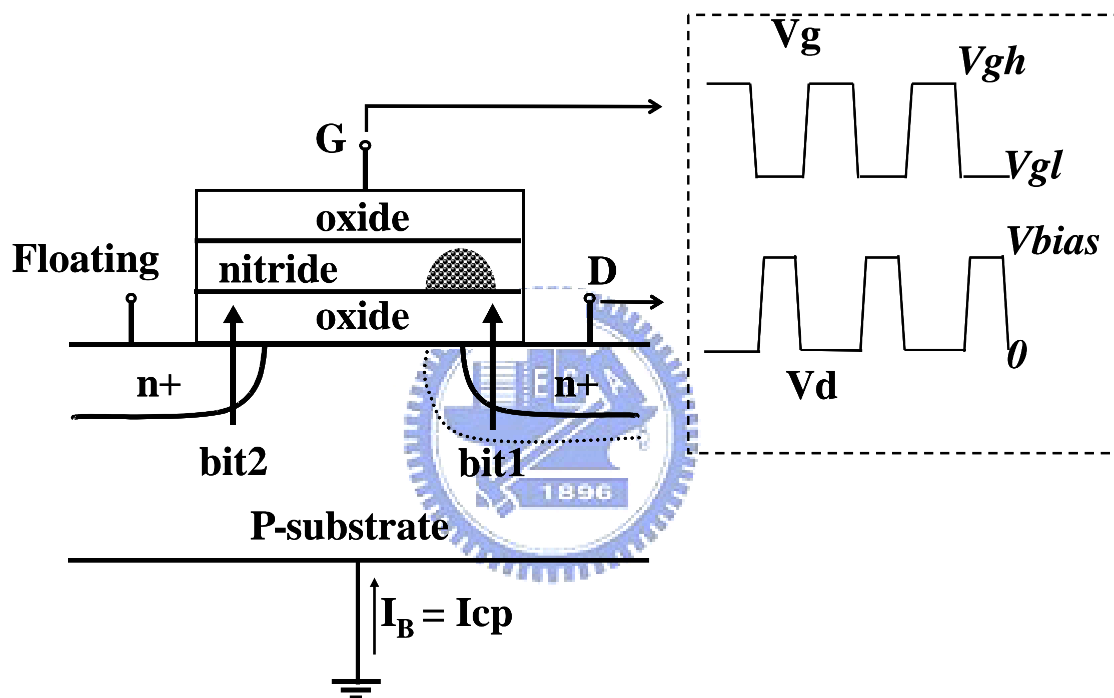


Fig. 2.1 Schematic diagram of a two-bit storage nitride cell and a CP measurement setup. The dashed line in the substrate represents depletion region caused by Vd. The thickness of the ONO gate stack is 9nm (top oxide), 6nm and 6nm, respectively.

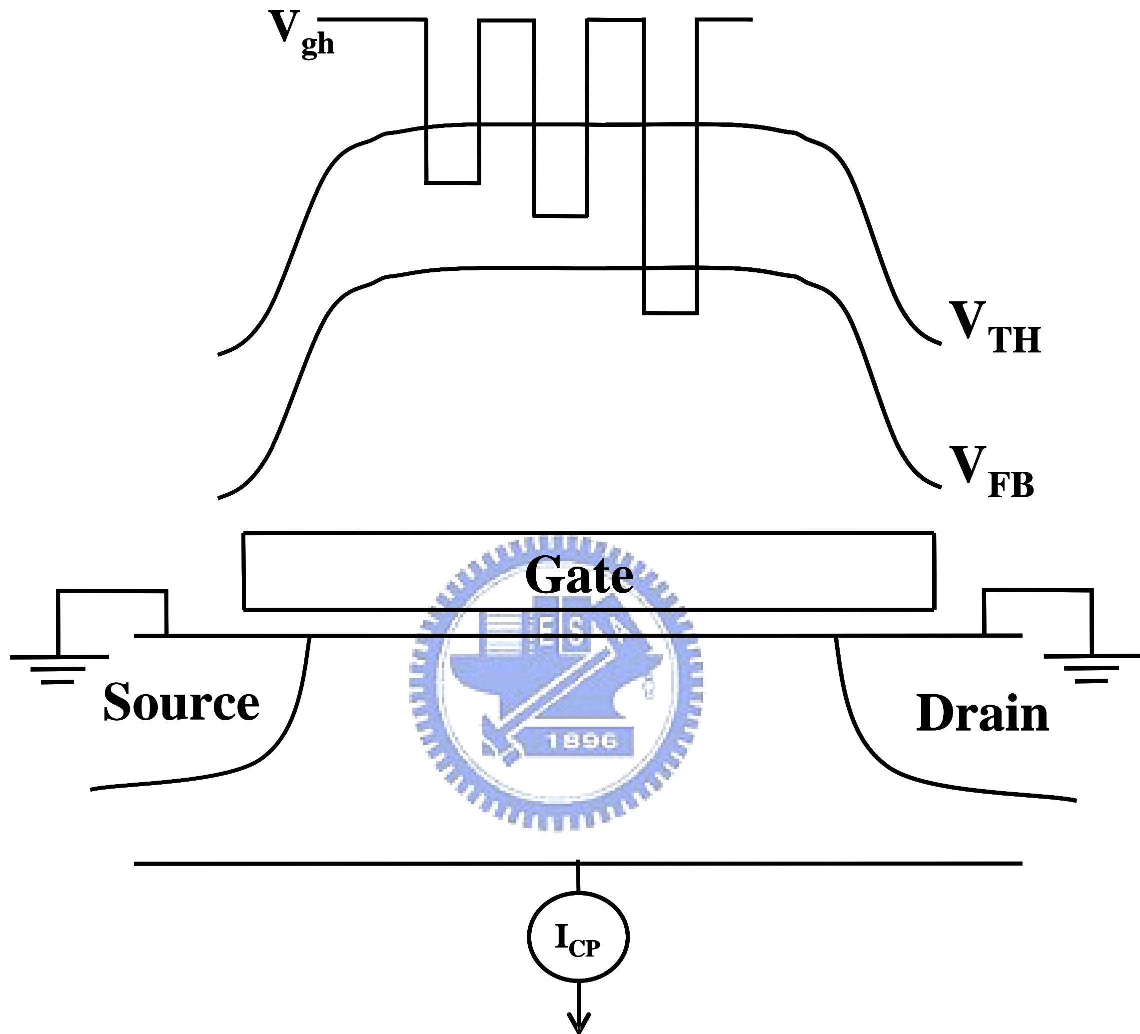


Fig. 2.2 Schematic illustration of Vgl varying in CP measurement. Vgh is above Vt and Vgl is varying. The part of channel undergoing accumulation-inversion-accumulation contributes to the Icp (bulk current)

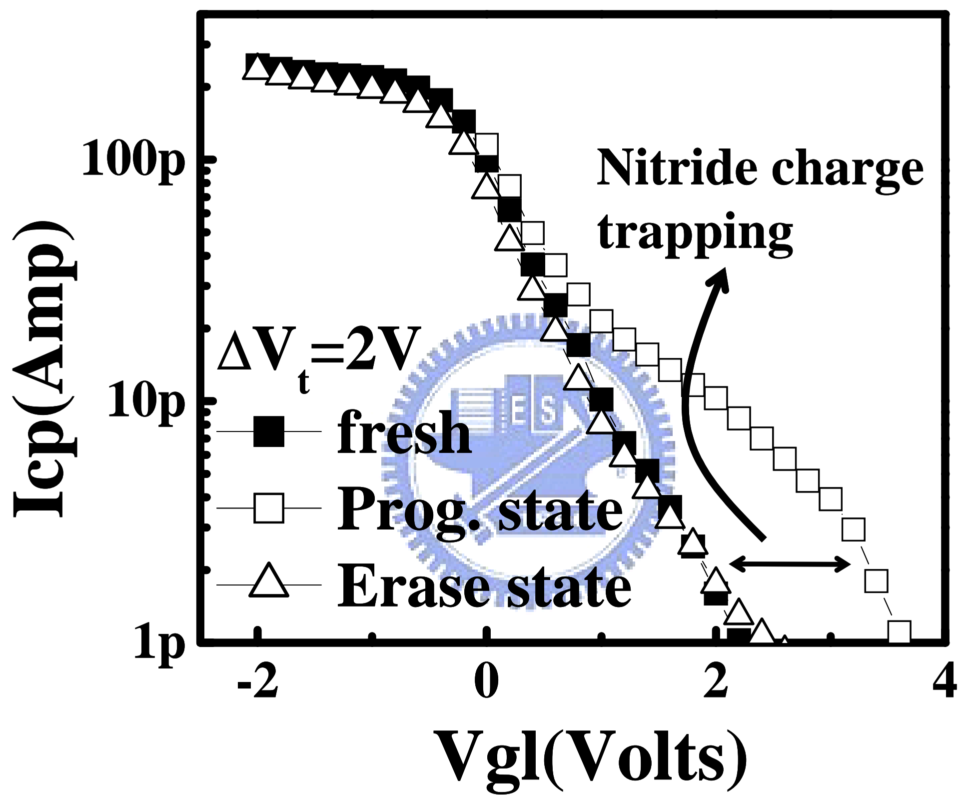


Fig. 2.3 Icp versus Vgl in a fresh cell, in program state, and in erase state, respectively. The Vt window (ΔVt) is 2V. Vd in CP measurement is 0V.

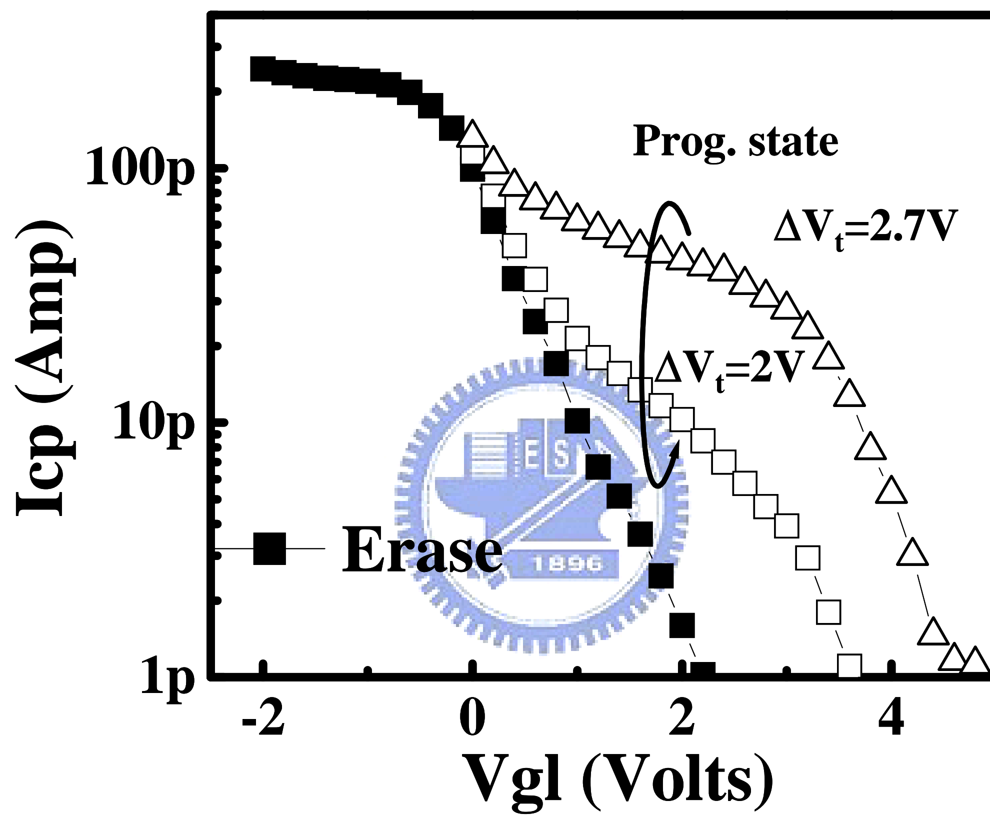


Fig. 2.4 The program-state Icp bump increase with Vt window due to more injected charges

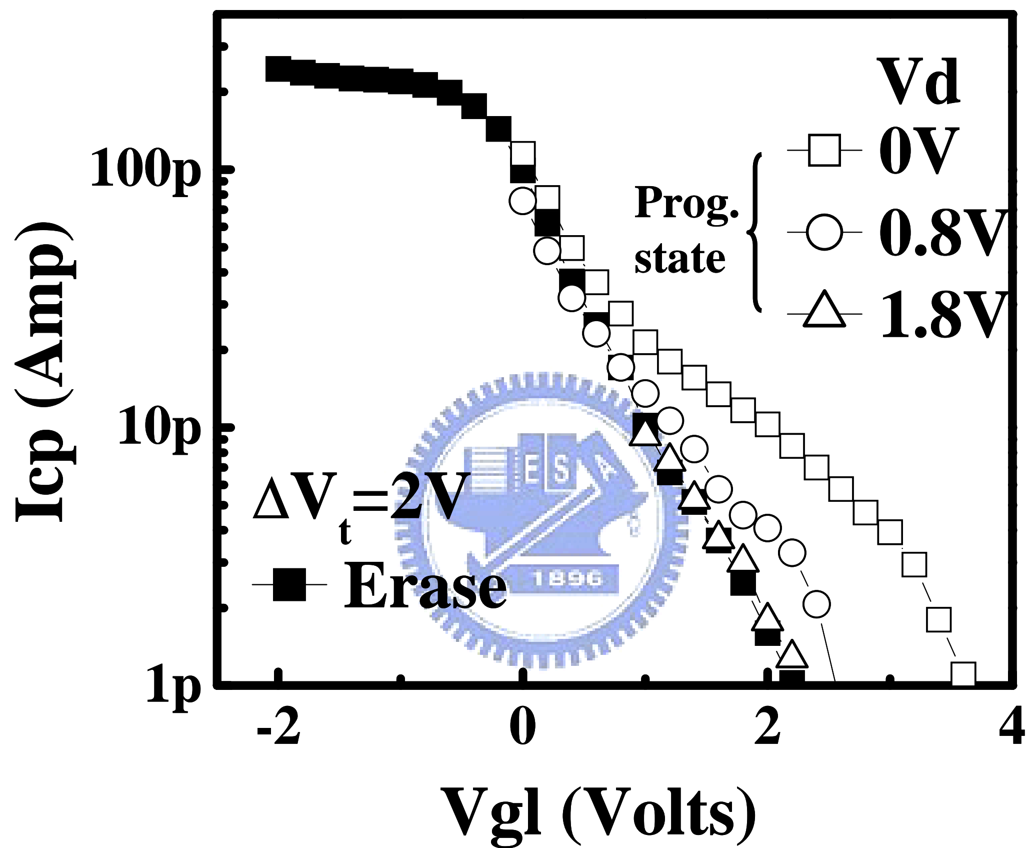


Fig 2.5 The decrease of the program state Icp bump with Vd in CP measurement. The V_t window is 2V.

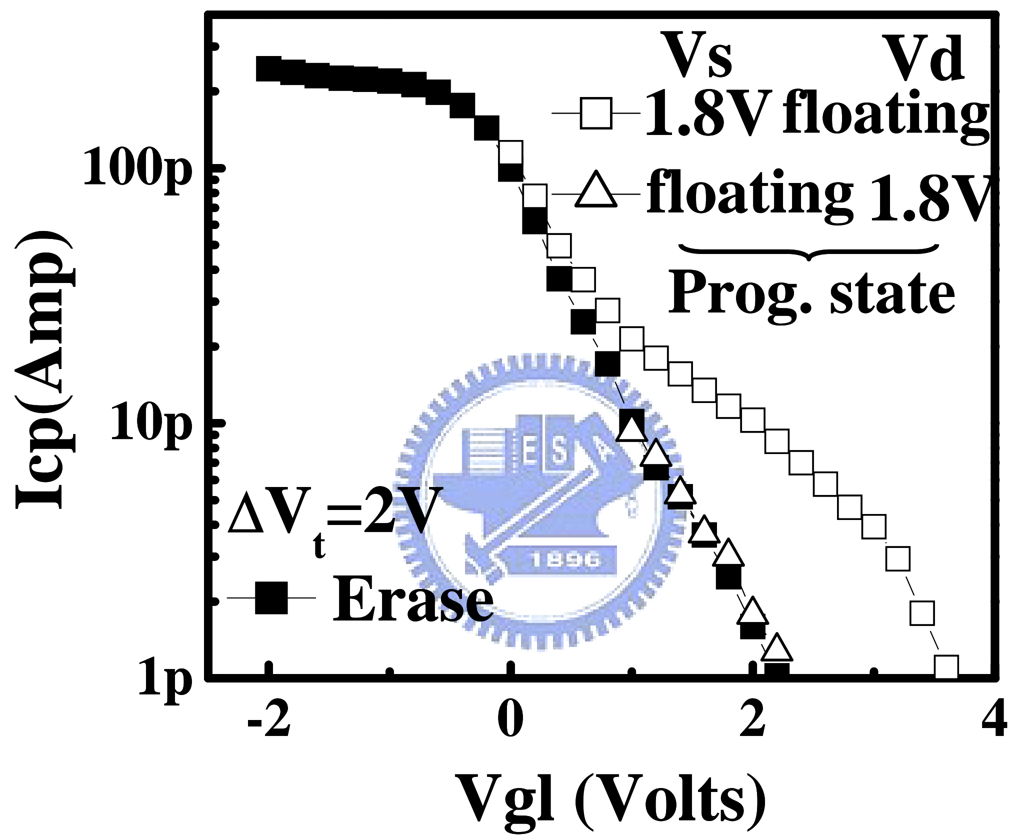


Fig 2.6 The program state Icp measured at Vd=1.8V & Vs floating and Vs=1.8V & Vd floating.

bump is not affected at all (Fig 2.6). The drain pulse is 180° phase-shifted with respect to Vg that the drain bias is applied only during the trapped electron emission cycle [29]. This indicates that the programmed charge is highly localized near the drain edge.

2.3.2 Two bit storage Icp

The Icp of four two-bit storage states, "11", "10", "01", and "00" is shown in Fig 2.7. "00" denotes both bits in program state and have the same threshold voltage window of 2V. "01"&"10" represents one bit in erase state and the other in program state. "00" means both bits in erase state. Fig 2.8 compares the Icp of the first programmed bit and the secondly programmed bit. The Icp of the secondly programmed bit is measured with the first bit erased. Notably, a cross-over in Fig 2.8 is observed. This cross-over suggests that the secondly programmed bit has a wider trapped charge distribution but a smaller peak density. By using a charge spatial profiling technique (Eq. 2.2 & 2.3) similar to [27], the nitride charge spatial distribution can be obtained;

$$Q_N(x) = \frac{C_{ONO}}{q}(V_{gl} - V_t) \qquad (2.2)$$

$$x = \frac{I_{cp}(V_{gl})}{I_{cp,\max}} L_g \qquad (2.3)$$

where $Q_N(x)$ is the nitride charge density, Lg is the gate length and Vt is the threshold voltage of a fresh device. Here Icp,max denotes the saturated CP current at Vgl=0. X=0 is at the drain or source junction edge. The extracted charge distribution of the first programmed bit and the secondly programmed bit is shown in Fig 2.9.

2.4 Simulation of the Channel Field Distribution

To estimate lateral spread of the secondly programmed bit, we perform a 2-D simulation [30] to calculate the channel field distribution. The drain side is programmed with a 2.5V threshold voltage window and the program bias condition is

V_g=11V and V_s=6.5V. The broader distribution of the secondly programmed bit (source side) is because a large channel field exists in the drain side during second bit programming (Fig 2.10). Such a large drain field arises from the stored electrons of the first programmed bit and will cause channel electrons to inject into the nitride earlier. It should be remarked that the above equation is derived from the 1D V_t model. For a narrow programmed charge distribution in a nitride flash cell, it only serves as a first-order approximation. Accurate profiling of a programmed charge distribution requires 2D device simulation by using MEDICI [30].

The programmed charge lateral extent can be also probed by varying V_d (or V_s) in CP measurement. The decrease of the program-state I_{cp} bump with V_d (or V_s) is shown in Fig 2.11. The secondly programmed bit needs a larger junction bias to "mask" the programmed charge. In other words, the second bit has a broader charge distribution

2.5 Cycling Dependence

The P/E cycling stress effect on programmed charge distribution is shown in Fig 2.12. In order to eliminate interface trap creation effect during P/E cycling, the I_{cp} bump is normalized to its value at V_d=0V. As cycling number increases, a large V_d in CP measurement is required to screen the programmed charge.

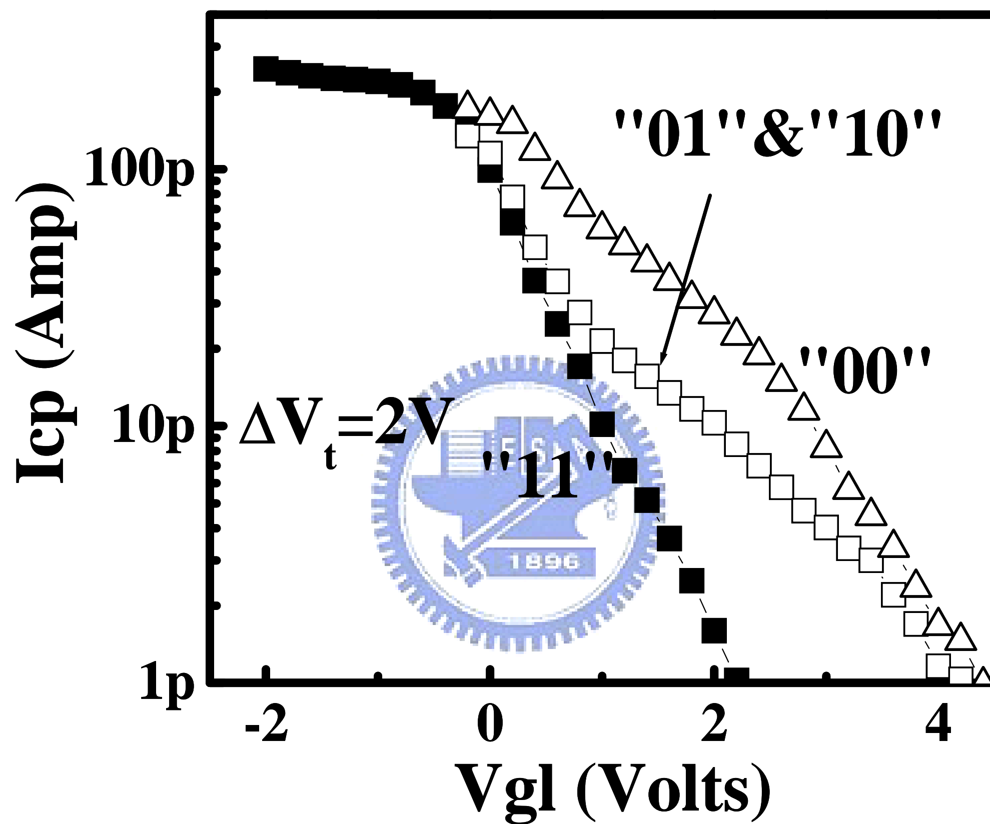


Fig. 2.7 The Icp of the four states of two-bit storage. “11” represents both bits in erase-state and “10” represents one bit in erase-state and one bit in program-state.

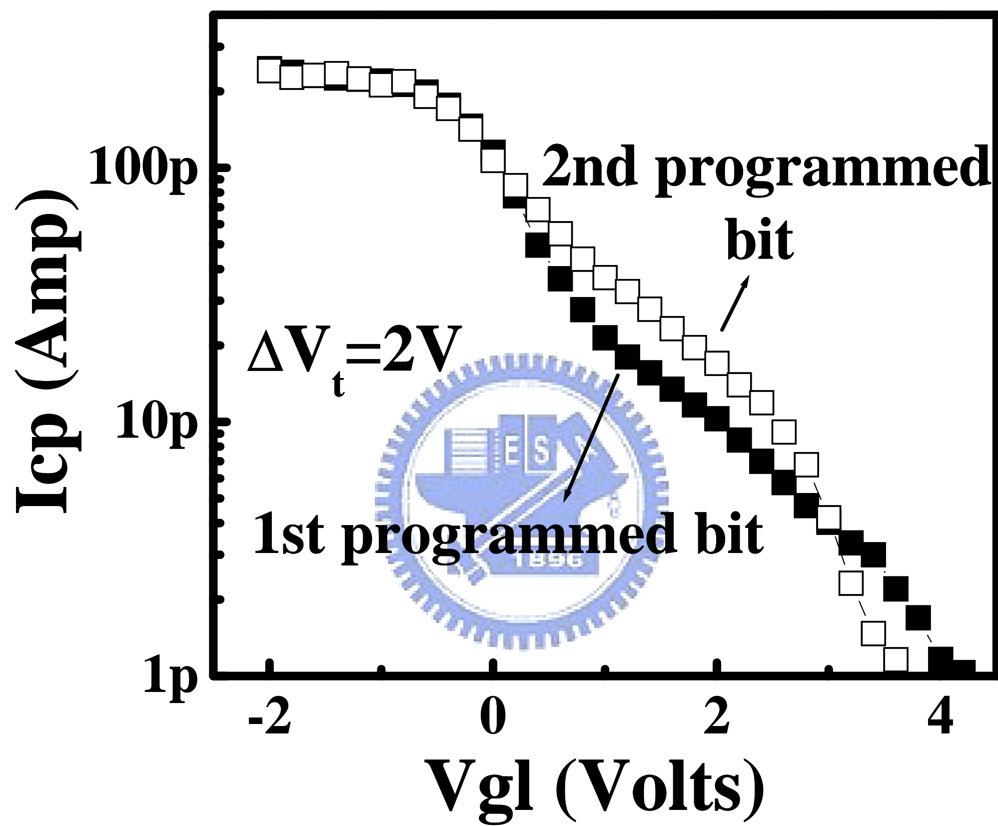


Fig. 2.8 Comparison of the Icp of the first programmed bit and the secondly programmed bit. The 2nd bit Icp is measured with the first bit erased

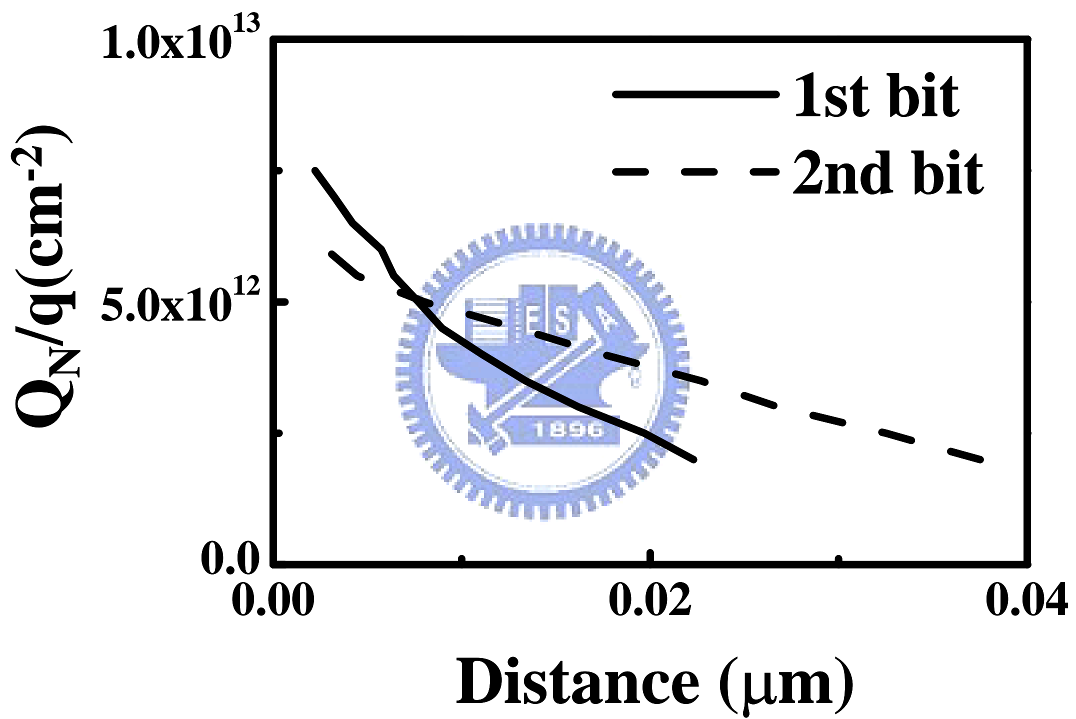


Fig. 2.9 Lateral profiling of the programmed charge distribution of the 1st programmed bit and the 2nd programmed bit. An uniform interface trap distribution along the channel is assumed. Icp,max is 195pA.

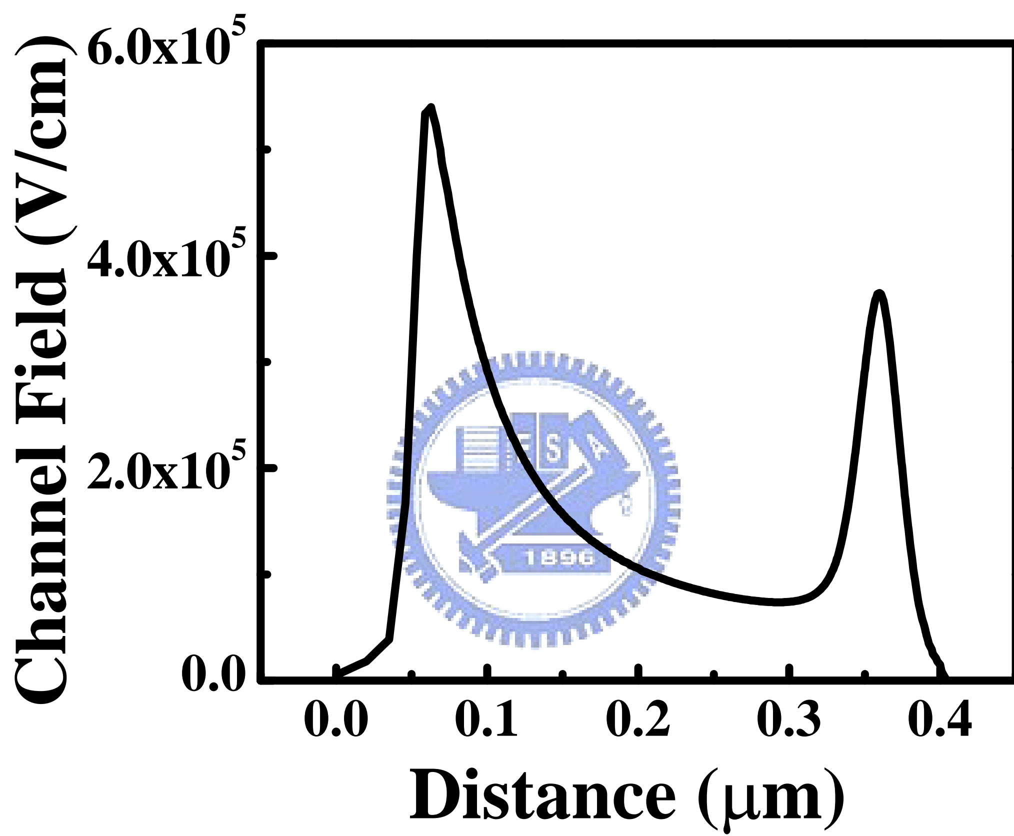


Fig. 2.10 Calculated channel field distribution in 2nd bit programming from 2D device simulation. x=0 is at the n+ source edge and x=0.4 is at the n+ drain edge. Vs=6.5V and Vg=11V in 2nd bit programming.

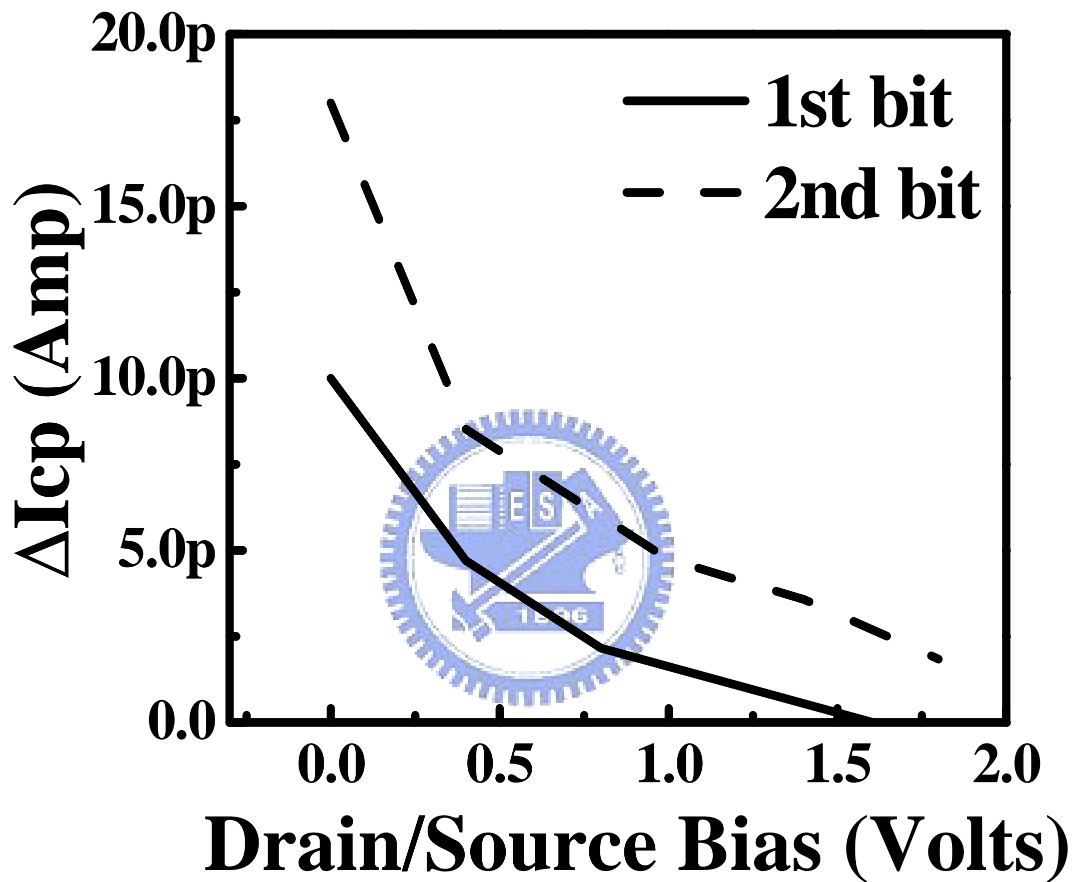


Fig. 2.11 The difference in Icp between program state and erase state as a function of drain bias for the 1st bit and source bias for the 2nd bit. ΔIcp is obtained from Fig. 2.8 at Vgl=1.6V.

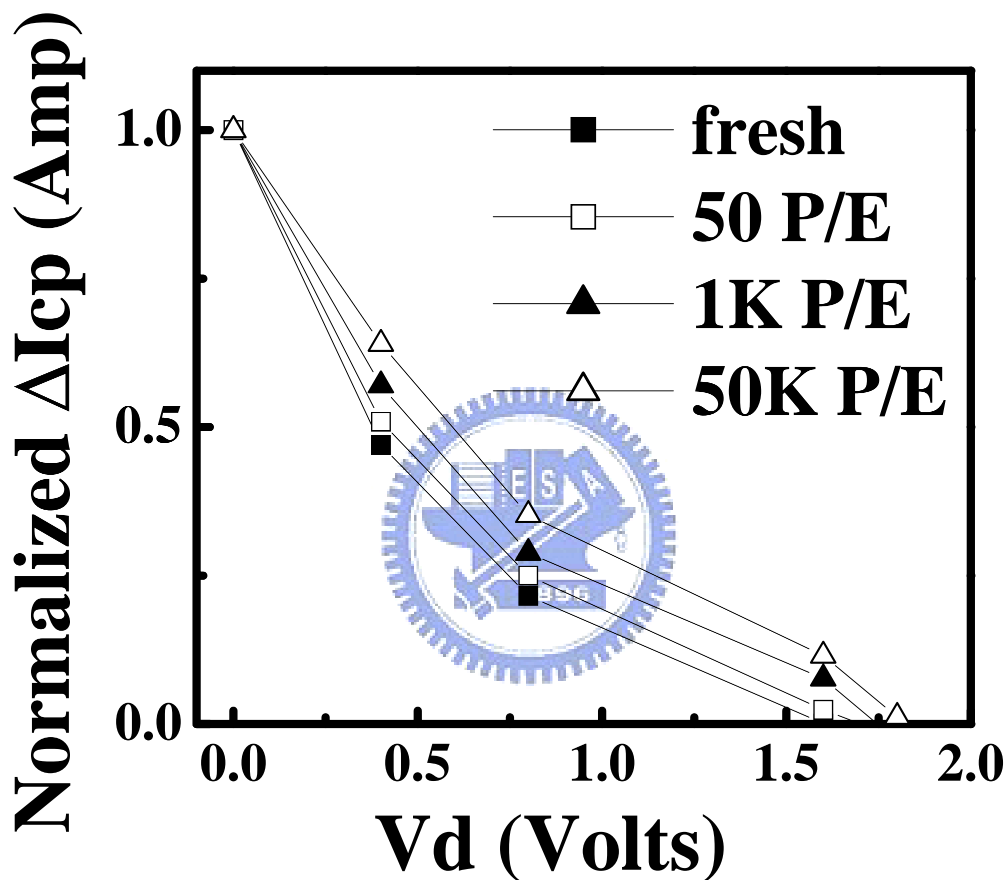


Fig. 2.12 The difference in Icp between program state and erase state as a function of Vd in CP measurement at various P/E cycle numbers. ΔIcp is measured at Vgl= 1.6V and is normalized to its value at Vd=0V to take into account interface trap creation in cycling.

Chapter 3

Program Disturb Induced Erase State Vt Shift

3.1 Introduction

Erase state threshold voltage instability in nitride-based localized trapping storage memory cells is investigated and reported in our previous study [16], [21]. The responsible mechanisms, room temperature Vt drift and read disturb, show that positive oxide charge plays a major role [31]. In this chapter, we will identify a gate disturb mechanism, causing erase state threshold voltage shift during program operation. A model of positive oxide charge assisted tunneling into a nitride layer is adopted to explain this mechanism [32].

A general representation of a 2-bit nitride storage flash memory array is shown in Fig. 3.1. The programming of cell P involves high voltage on the gate (word line) and drain (bit line). Un-addressed cells neighboring cell P (cell N) experiencing a high voltage (10~12V) on the word line suffer from gate stress induced program disturb [33]. The gate voltage stress time for one bit is thus proportional to the number of P/E cycles, thus causing reliability concerns during array structure programming. The programming time for a single bit is typically about a few micro seconds. In order to explore the program disturb, a micro-second transient measurement circuit was employed. Extra electrical anneal step reducing this disturb effect will be discussed [34].

3.2 Micro-second Transient Measurement

Fig.3.2(a) illustrates the circuit diagram of the micro-second measurement system. This circuit was composed of high speed analog switches and a low noise amplifier. Its output signal was displayed at an excellent resolution, high speed digital oscilloscope (Tektronix TDS5054). The operating biases and connections were shown

in Fig 3.2(b). Computer-controlled system monitors the threshold voltage shift immediately after stress. Fig. 3.3 shows the photography of our micro-second transient measurement circuit.

3.3 PCAT Model

Hole trap creation in the bottom oxide is generally believed to be the major cause of RT threshold voltage drift. Besides RT drift, the program disturb is also enhanced by positive oxide charges created during P/E cycling. The columbic potential caused by positive oxide trapped charge is incorporated in the electron tunneling barrier. When a positive Vg is applied at an cycling-stressed cell, the channel is inverted and a current component flowing from the gate to the source and the drain (Isd) arises due to positive oxide charge assisted electron tunneling (Fig. 3.4). If Vg is large, Isd becomes dominant and has a t^{-p} time dependence with p~0.7 [35]. The gate-disturb induced ΔVt should follow a power law time dependence with the power factor of n=0.2~0.3 (Eq. 3.1).

$$\Delta V_t \propto \int I_{sd}(t)dt = t^{1-p} \propto t^n \qquad \textit{with } n=0.2\sim0.3 \tag{3.1}$$

$$p = \sqrt{\frac{m_e \Phi_e}{m_h \Phi_h}} = 0.7\sim0.8$$

3.4 Program Disturb Behavior

3.4.1 Measurement setup

In order to measure the Vt shift caused by program disturb, the appropriate word-line (gate) and bit-line (source & drain) waveform patterns were designed, as shown in Fig.3.5. The patterns were generated by Agilent 8110A pulse generators. There are two phases in the pattern, P/E phase and M/D (measurement & disturb) phase. In the P/E phase, an appropriate bias was applied for program and erase. In the M/D phase, the disturb gate bias is the same as the program gate bias depending on

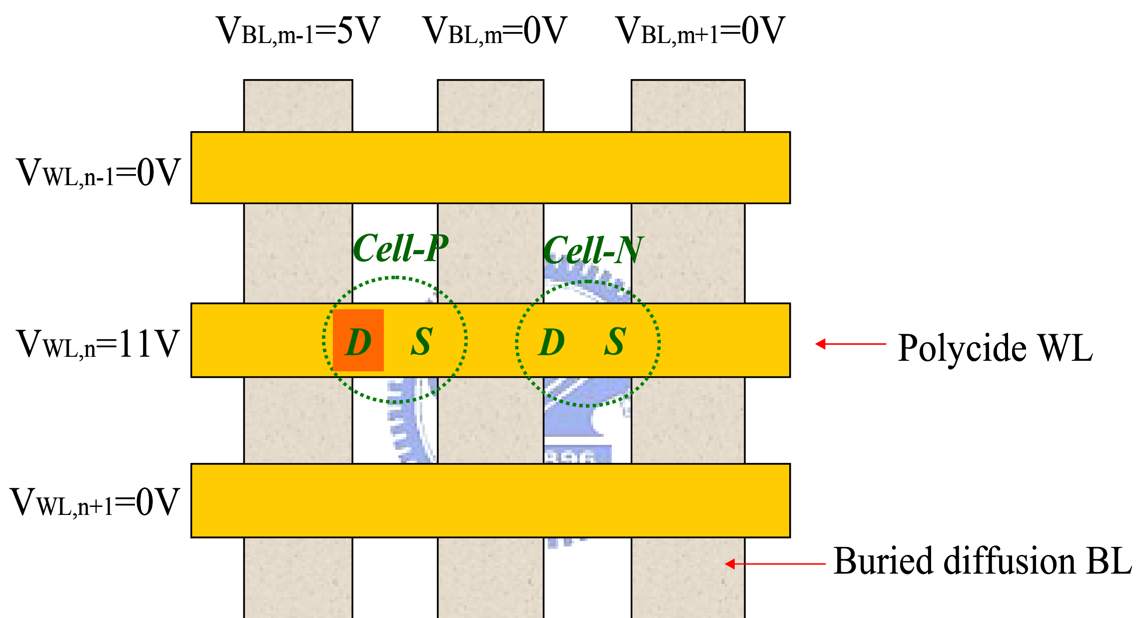
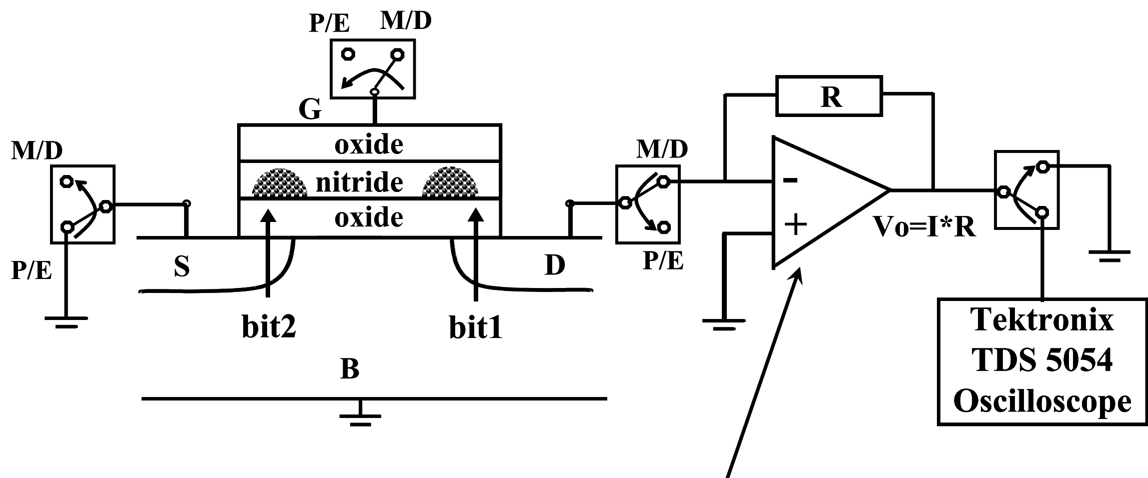


Fig. 3.1 Scheme of the virtual ground array and a technique to inhibit program disturb in adjacent cells. When programming D-bit of Cell P, program disturb occurs in Cell N sharing the same WL voltage (11V).



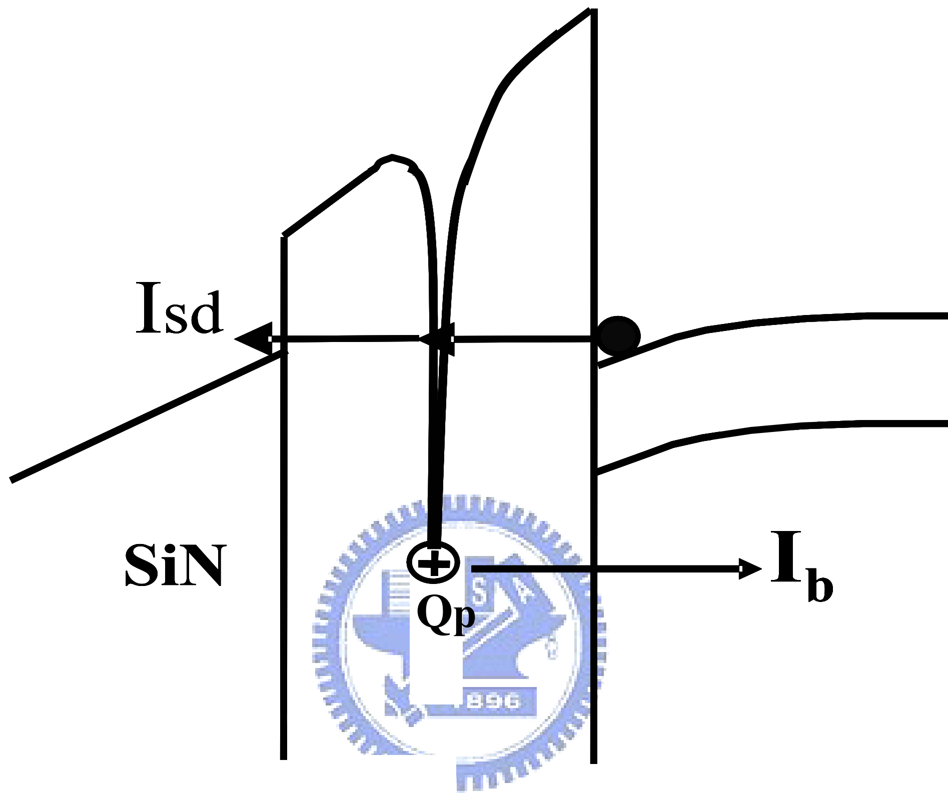
(a)

	V_G	V_D	Time	Vs	Is	OSC.
PGM	11	5	10μs	0	Bypass To GND	GND
ERS	-4	7	10ms	0		
Disturb	11	0	μs~s	0	Fed into OP	Vo
Meas.	2.5	Virtual Ground	μs~ms	1.6	Fed into OP	Vo

(b)

Fig. 3.2 Circuit diagram of the micro-second measurement system. The applied biases of P/E phase and M/D phase are shown in the table.

Fig. 3.3 Photograph of our micro-second transient measurement circuit.



$$\Delta V_t \propto \int I_{sd}(t)\,dt = t^{1-p} \approx t^n \text{ with n=0.2~0.3}$$

Fig. 3.4 Illustration of positive oxide charge assisted tunneling current (Isd). The time-dependence of Isd and corresponding Vt shift was given.

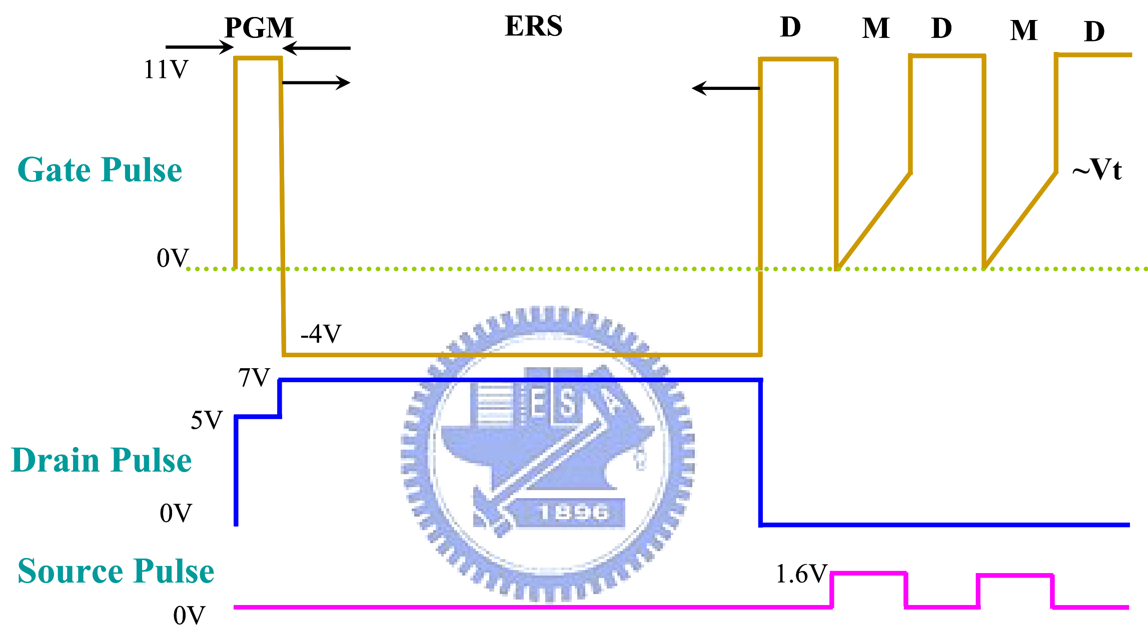


Fig. 3.5 The applied waveform patterns. The time interval of the measurement and disturb phase is 200µs.

operation conditions and Vd=Vs=0V. The measurement gate bias was applied near the threshold voltage and Vd=0.1V.

3.4.2 Program-disturb characteristics

The devices have a gate length of 0.35μm and a gate width of 0.5μm. Fig. 3.6 shows the disturb characteristics of a 10K P/E cycled cell in two different disturb conditions. The program disturb bias is Vg=11V. It is found that Vt shift (solid square) exhibits a power-law time dependence t^n, i.e., a linear plot in a log-log scale with n~0.3, which is consistent with the PCAT model [32]. The open square shows the read disturb effect measured by Agilent 4155C and exhibits the same time dependence. Fig. 3.7 shows the Vt shift versus the wait time after erase. Here, we see no Vt shift if we wait 100ms after erase and then have a 20ms disturb at Vg=11V.

3.4.3 Cycling Dependence

In a P/E stressed cell, the Vt shift induced by program disturb is found to be larger than that in a fresh cell. Fig.3.8 shows the threshold voltage shift versus P/E cycle number. The dependence of the Vt shift implies that the charge gain behavior in low Vt state is due to positive oxide charge detrapping. At low P/E stress, oxide trap creation is minimal and thus Vt shift is small.

3.4.5 Summary

Based on this work, we realize that erase state Vt drift measured by Agilent 4155C is underestimated since charge tunneling starts immediately after erase. From the above measurement results, micro-second time scale Vt shift can be probed. The Vt shift is much more severe in an array because of accumulated gate stress time during programming.

3.5 Modified Erase Scheme

Except for room-temperature drift and read disturb, our study showed that program disturb is also a reliability concern in the low Vt state. Some ways to prevent disturb such as isolated sector structure was proposed [36]. An alternative approach is

to use an appropriate voltage pulse to reduce this stress effect. After BTBT hot hole erase, an extra electrical anneal is reported to be effective [34]. As positive charges are accumulated during erase, subsequent anneal step will remove the cycling induced positive charges in the bottom oxide. An electrical pulse at Vg=10V and Vd=4V can significantly reduce program disturb effect (Fig. 3.9).

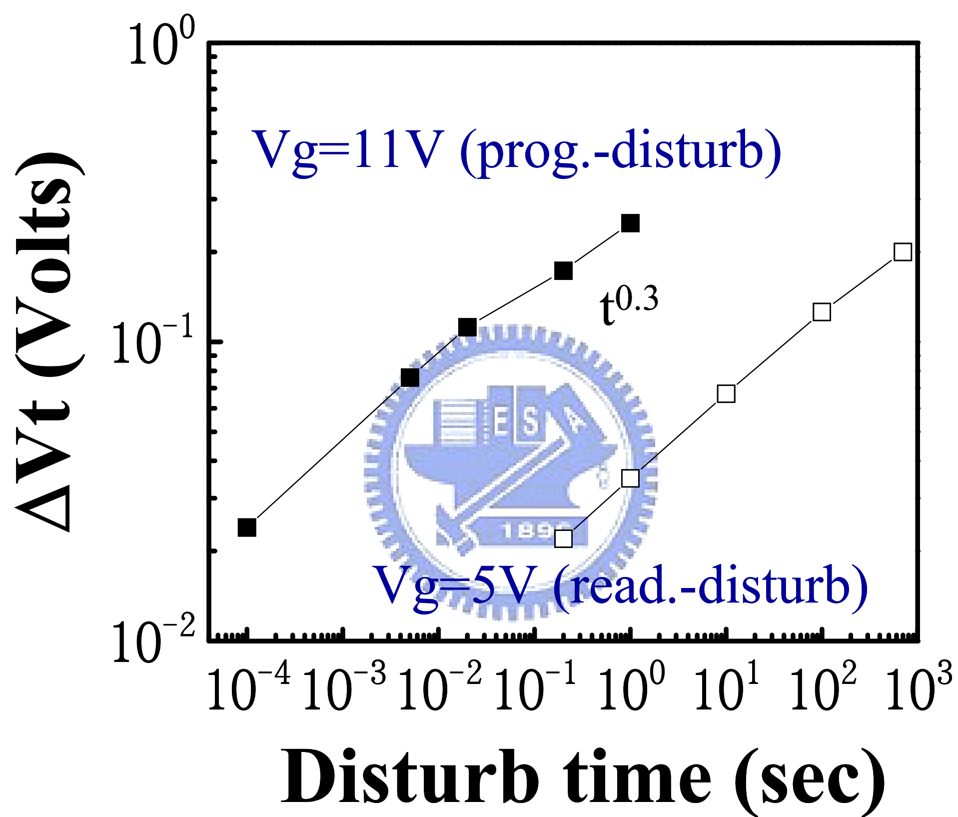


Fig. 3.6 Program and read disturb characteristics of a 10K P/E cell. Lg=0.5μm.

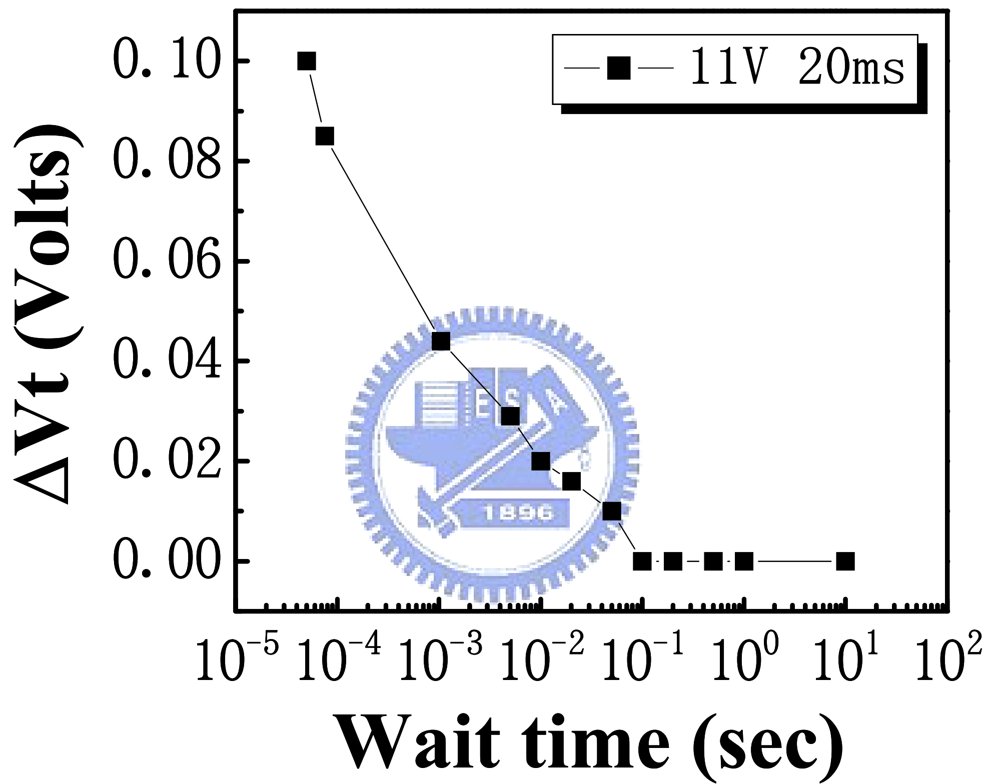


Fig. 3.7 Vt shift versus wait time after erase. Vg=Vd=Vs=Vb=0V during the wait time.

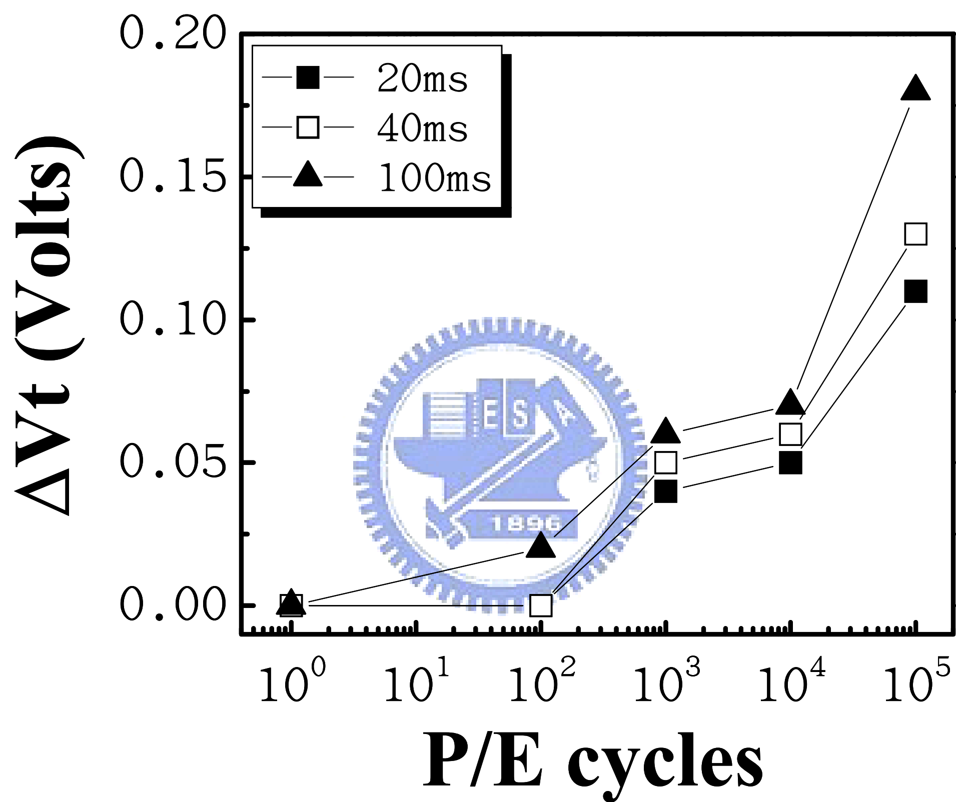


Fig. 3.8 Cycle number dependence of Vt shift. Note that no Vt shift observed in a fresh cell. After 10K P/E cycles, there is a 0.17V Vt shift after 100ms disturb.

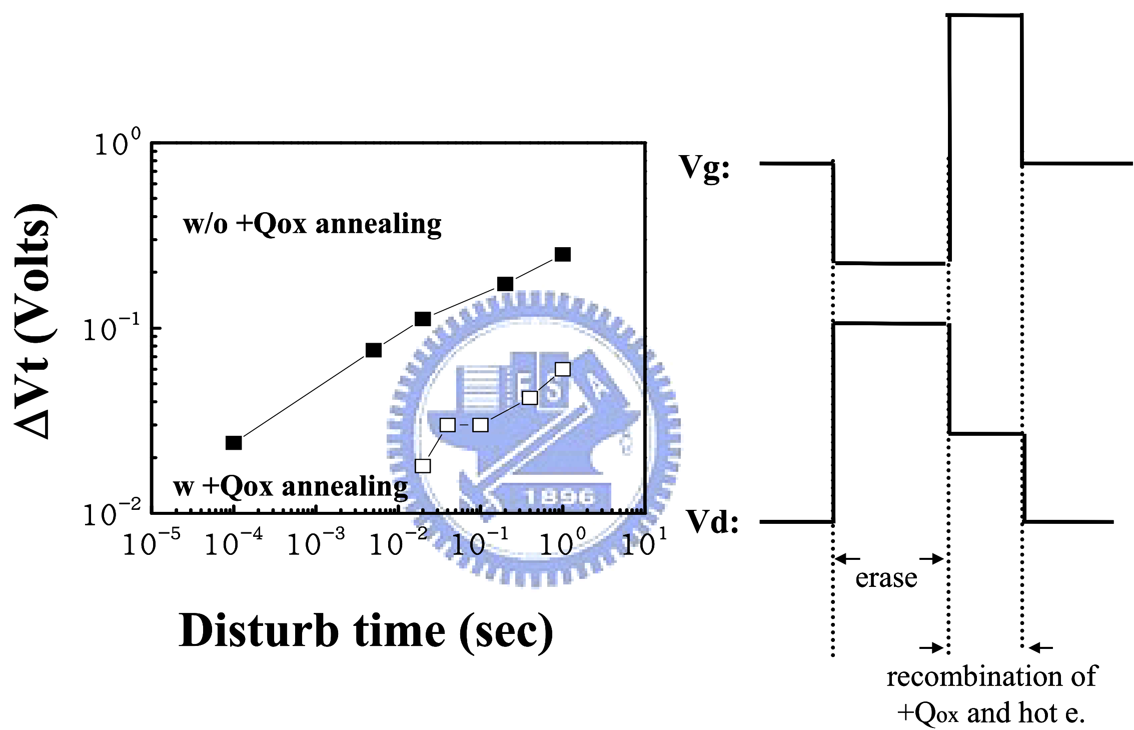


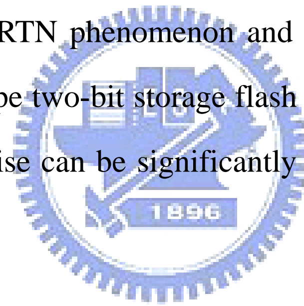
Fig. 3.9 Vt shift of conventional erase and modfiied erase with an electrical anneal step. The anneal voltage is Vg/Vd=10/4V.

Chapter 4
P/E Cycling Induced Read Current Noise

4.1 Introduction

In this chapter, we investigate P/E cycling induced random telegraph noise (RTN) in non-uniform charge storage nitride flash cells for the first time. The amplitude of RTN increases with P/E cycle number and with decreasing gate length. Non-uniform charge storage by channel hot electron programming can further enhance read current fluctuation. The large amplitude of read current fluctuation implies we must allow for more margins in cell operation and needs careful attention especially in Multi-level cell (MLC) application.

Therefore, to probe the RTN phenomenon and to find the solutions will be an important issue in SONOS type two-bit storage flash memory cells. According to our investigation, read current noise can be significantly reduced by the improvement of bottom oxide reliability.



4.2 Random Telegraph Noise Measurement

The charge transport through a MOSFET device characterized by discrete switching events of the drain current, has often been observed and attributed to the trapping/detrapping of conduction carriers by a single defect near Si/SiO_2 interface [37]-[39]. Different names exist for the phenomenon, like burst noise or Random Telegraph Noise (RTN). Micro-second Transient measurement system we mentioned at chapter 3 for measuring read current noise is shown in Fig. 4.1. This setup can monitor the drain current noise in fixed read bias. The sampling rate in our experiments is 10khz, which enables the observation of fast transitions of read current with time constant down to 0.1ms, which corresponds to 10^5 reading in each measurement of 10 seconds. The devices used in this work have a gate length of

0.35μm and a gate with from 0.5μm to 0.3μm.

4.3 P/E Cycling Stress

In a P/E cycled cell, the read current fluctuation induced by oxide trap is found to be larger than that in a fresh cell. Fig. 4.2 shows read current fluctuation at program state in a fresh cell, after 1k P/E cycles and after 100k P/E cycles. The cell biased in weak inversion and the read current is near 1μA. Apparent random telegraph noise patterns are observed in a 100k P/E cycled cell while it is undetected in a fresh cell. The RTN rises from the charging/discharging of single oxide trap or multiple oxide traps created by P/E cycling stress [40]. At a low cycle number the RTN exhibits two-level transitions (Fig. 4.2(b)) while at a large cycle number multi-level transitions (4-level) are occasionally observed (Fig. 4.2(c)). These multi-level transitions, superimposed by several independent two-level RTN waveforms, may exhibit a large ΔId and result in a read failure.

The dependence of noise amplitude on read current level is shown in Fig. 4.3. In this measurement, a NROM cell is programmed to different Vt and the reverse read bias is at |Vds|=1.5V and Vgs=4V. The cycle number is 100 that only two-level transitions are obtained. As shown in Fig. 4.3(a), ΔId is found to increase from 0.04μA in a high-Vt cell (1μA read current) to 0.18μA in a low-Vt cell (30μA read current).

4.4 Length Dependence & Non-uniform Vt Effect

The gate length effect on RTN is shown in Fig. 4.4. The read current level is about 1μA. The RTN amplitude with two-level transitions is shown in Fig. 4.4(a), a noticeable increases of ΔI_d with decreasing gate length [41]. A two-dimensional device simulation is performed to calculate the gate length dependence. A similar trend is obtained (Fig. 4.5). Moreover, RTN is found to be further enhanced by localized charge storage. Fig. 4.6 shows the current fluctuations by FN injection and

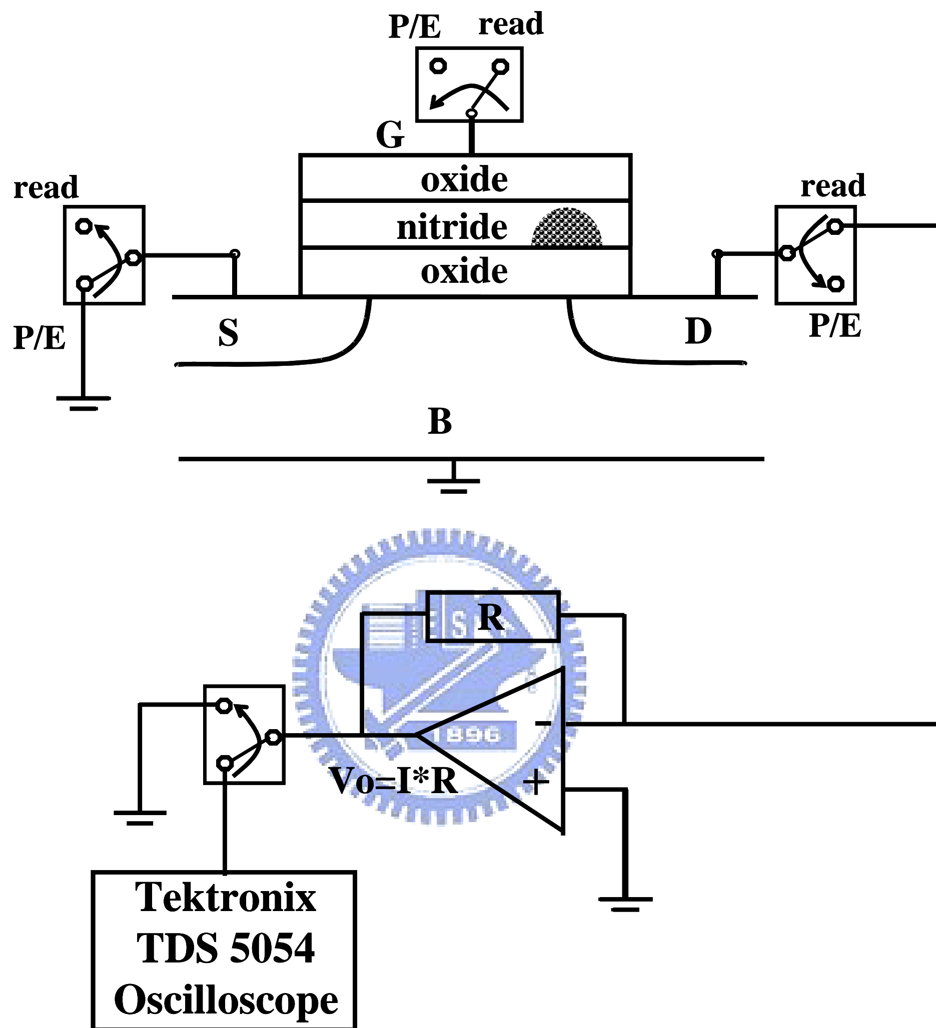


Fig. 4.1 Experimental setup for RTN measurement.

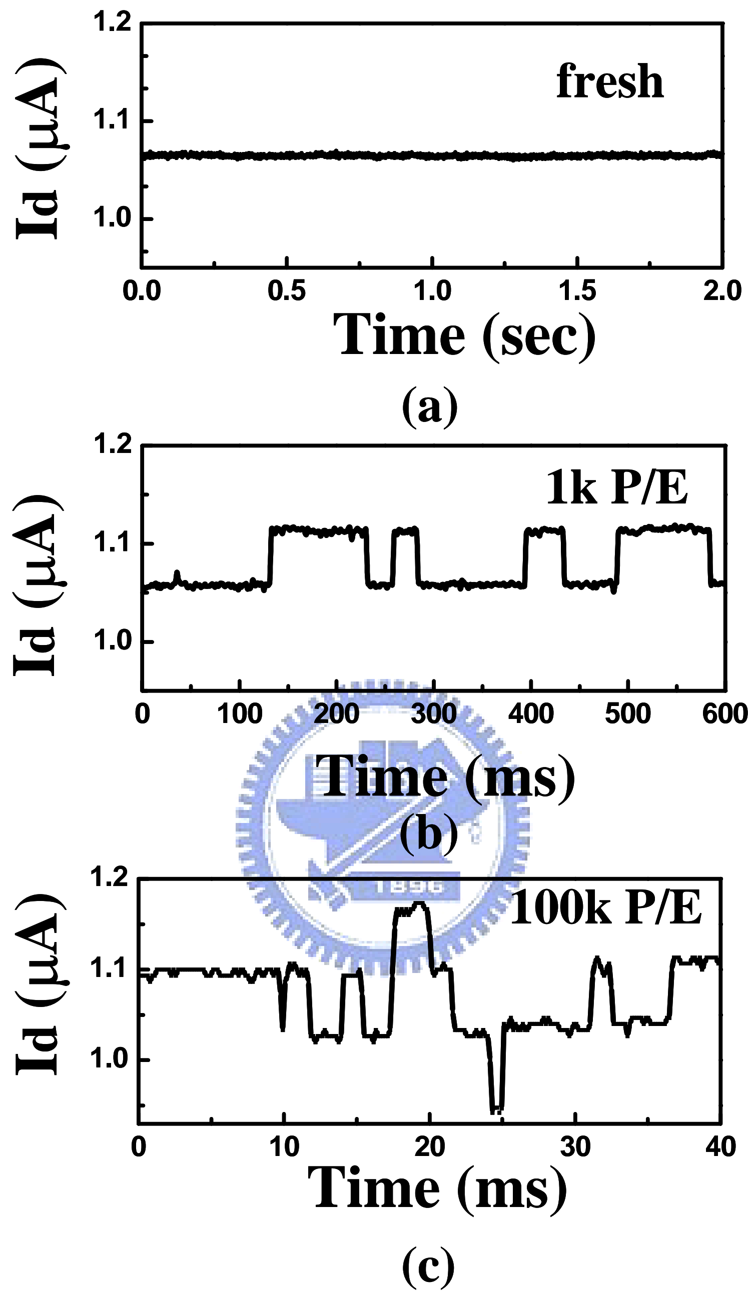
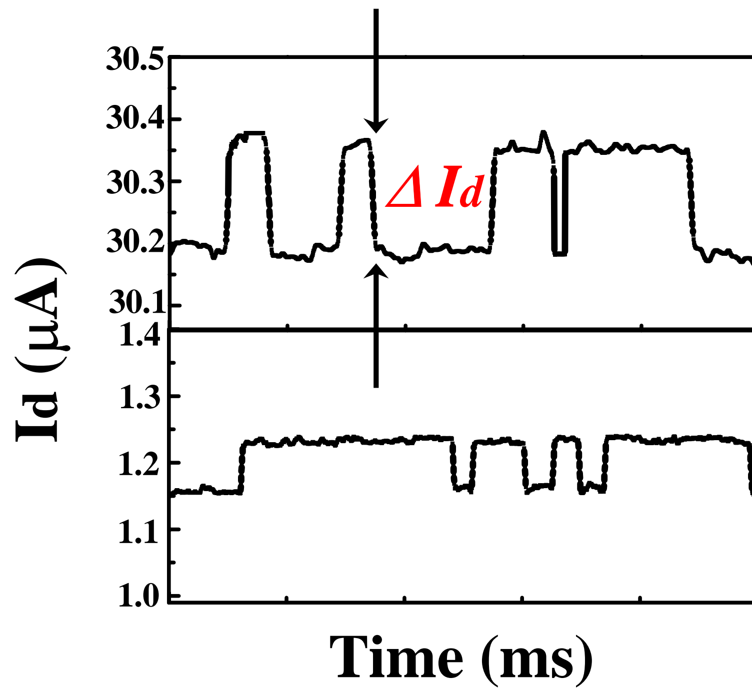


Fig. 4.2 Representative RTN traces in a NROM cell (W/L=0.35µm/0.3µm). (a) fresh, (b) 1k P/E cycles, (c) 100k P/E cycles.



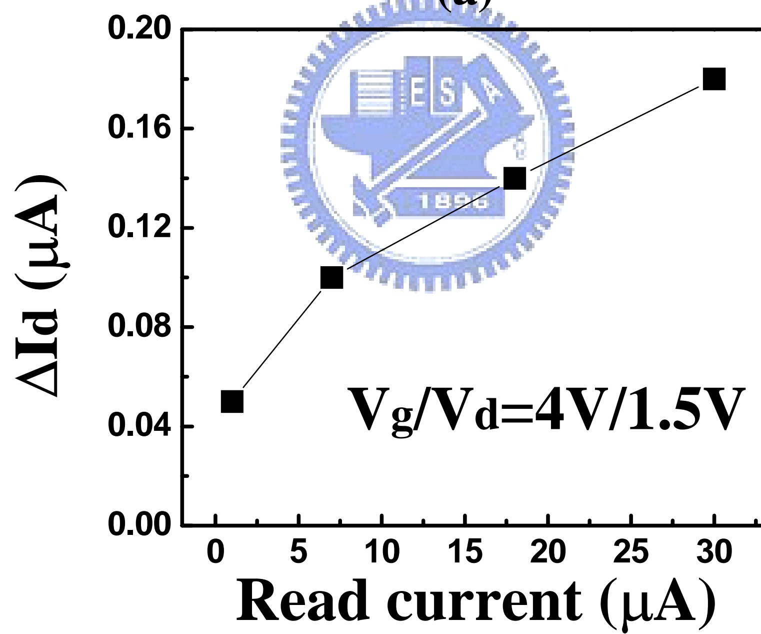
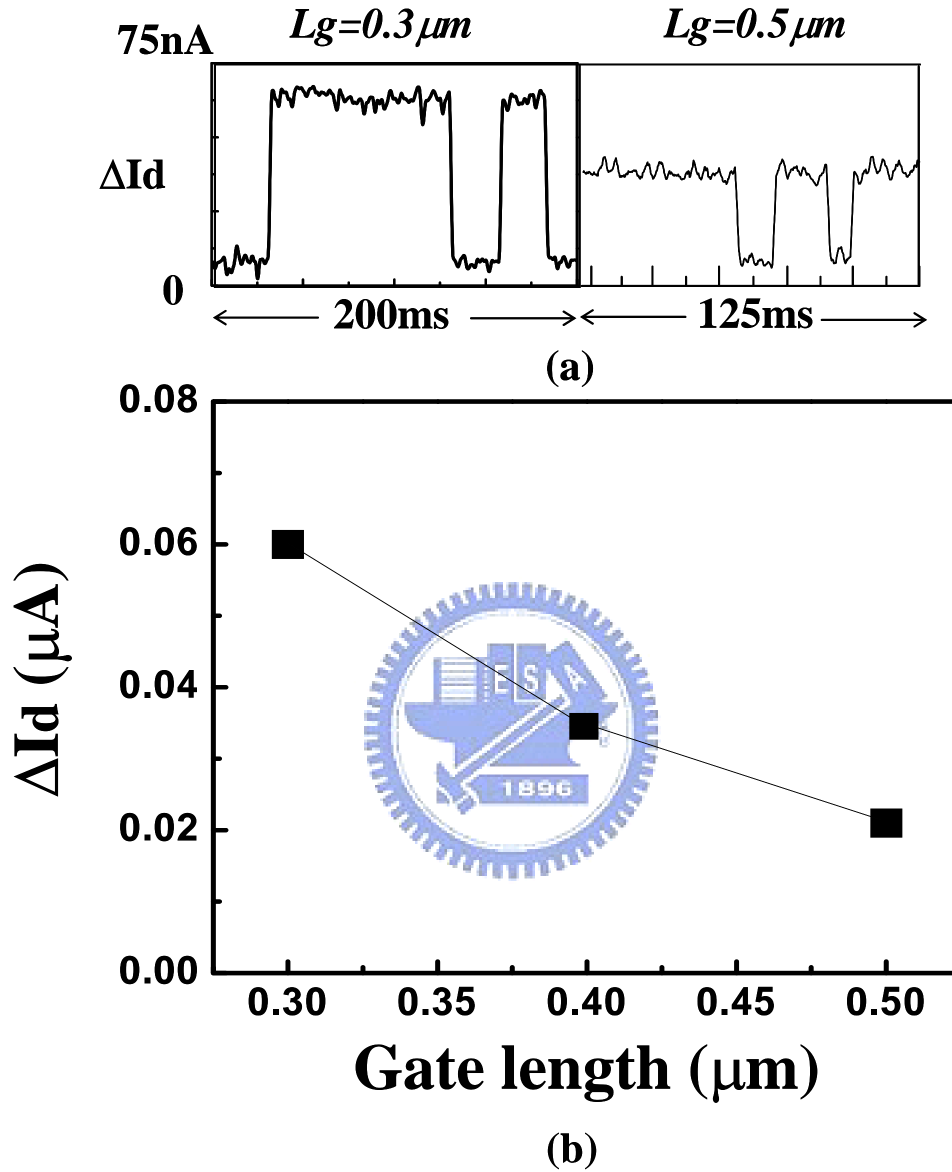


Fig. 4.3 Comparison of RTN amplitude in program-state and in erase-state (b) Dependence of ΔId (two-level transition) on read current. The P/E cycle number is 100 P/E. The reverse read bias is V_g=4V, V_s=1.5V and V_d=0V.



(b)

Fig. 4.4 (a) Comparison of RTN amplitude for L_g=0.3μm and 0.5μm.
(b) Dependence of ΔId (two-level transition) on gate length.
The read current level is about 1μA.

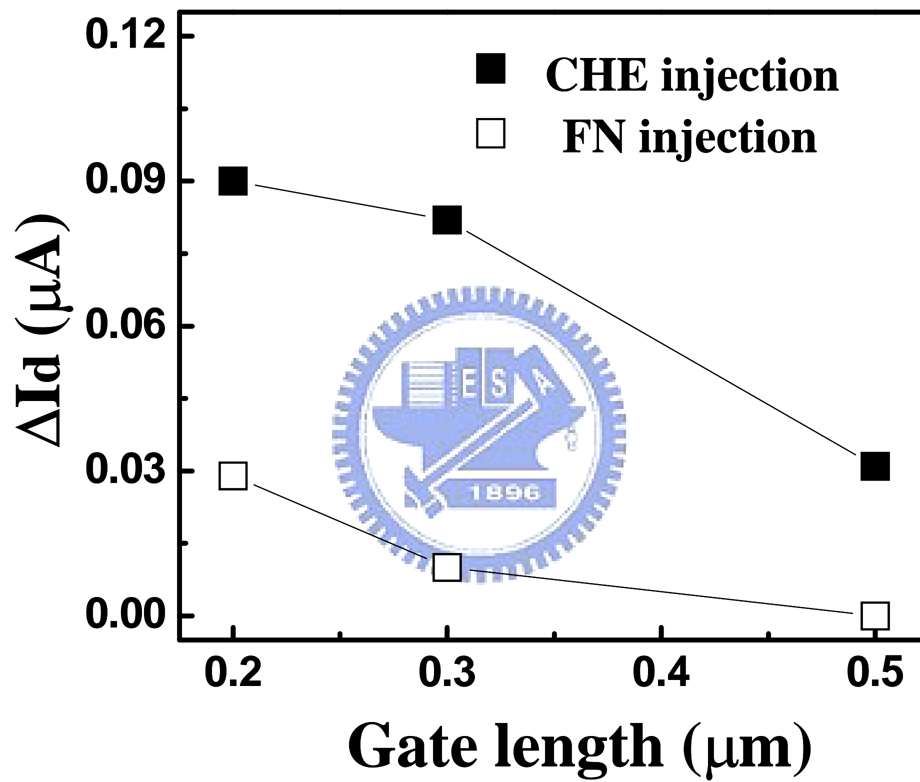


Fig. 4.5 Calculated gate length dependence of two-level RTN amplitude from 2D device simulation. For CHE injection, the trapped charge width is assumed to be 30nm. FN injection has uniform charge storage. The parameters in simulation are not calibrated.

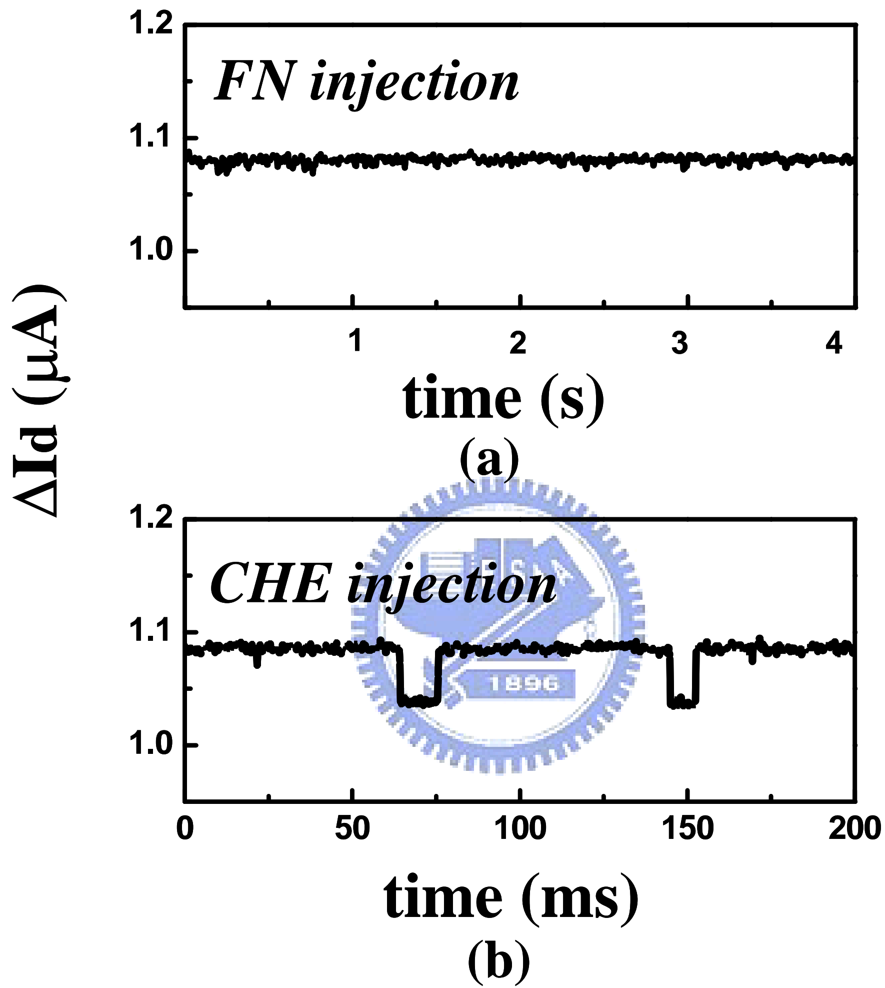


Fig. 4.6 Typical RTN traces for uniform FN injection (a) and channel hot electron injection (b). Both cells have the same P/E stress conditions.

CHE injection, respectively. The two cells experience the same cycling procedure but have different injection conditions in the last programming. In the uniform FN injection cell (Fig. 4.6(a)), RTN is very small or undetectable in a measurement span of 4 seconds. The simulated result in Fig 4.5 also shows that uniform injection yields smaller RTN. Our result here is consistent with earlier work in [42] that non-uniform channel Vt-distribution can increase 1/f noise. Fig 4.7 shows the maximum read current fluctuation and corresponding number of levels in read current in a 0.3μm cell. The read current is about 30μA. ***At 100k P/E cycles, 5-level transitions in read current is noticed and maximum ΔId is ~0.7μA in a sampling space of 10^5 reading.*** RTN with more levels and a large ΔId is still expected as more reading are taken [43].

4.5 Oxide Process Effect

To evaluate bottom oxide process effect on RTN, two different oxide process conditions with a 0.5μm gate length (device A and device B) are used. Device B is known to have better oxide endurance from a charge pumping measurement result (Fig. 4.8(a)) RTN traces in device A and B are shown in Fig. 4.8. Note that device B exhibits smaller amplitude in read current fluctuation. This is because device B has less oxide traps creation and thus the probability of multi-level RTN is much reduced.

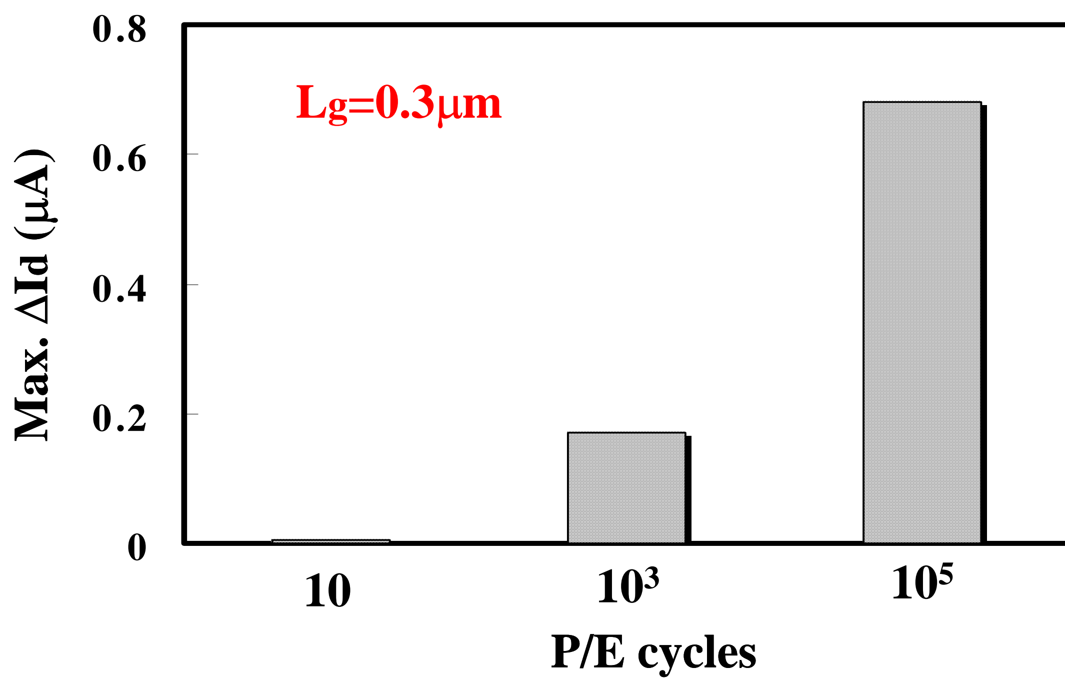


Fig. 4.7 Maximum ΔId observed at a read current of 30µA from multi-level RTN. The sampling size is 10^5 readings.

(a)

NROM	Process A	Process B
ΔIcp(10k)	70pA	40pA

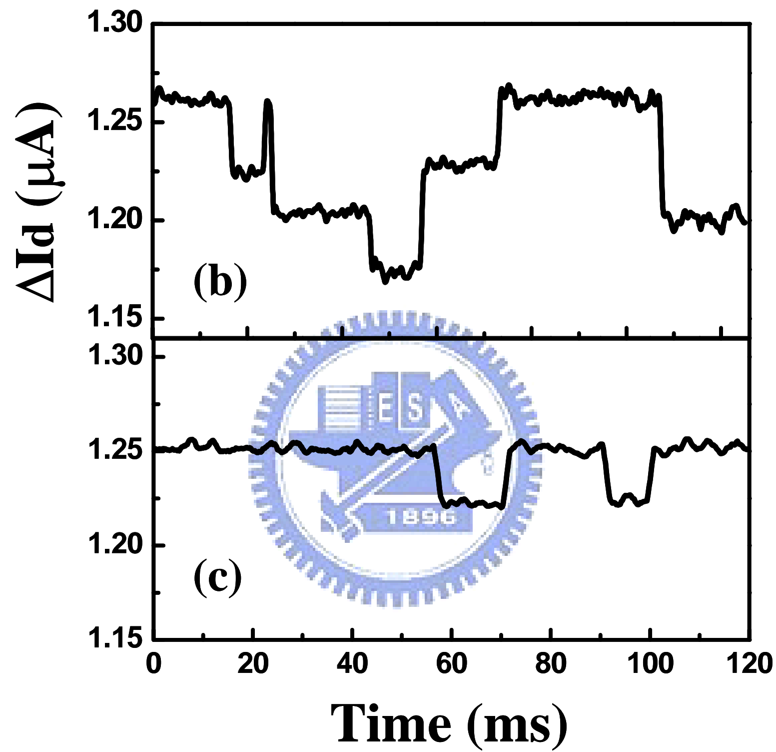


Fig. 4.8 (a) The increment of charge pumping current (I_{cp}) in device A and device B after 10k P/E cycles. (b) RTN traces in Device A after 10k P/E cycles (c) RTN traces in Device B after 10k P/E cycles.

Chapter 5
Conclusion

Programmed charge distribution in the ONO layer and the effects of read current noise in a localized trapping storage cell have been discussed in this thesis. The lateral distribution of programmed charge is investigated by using a charge pumping technique. The secondly programmed bit has a broader trapped charge distribution than the first programmed bit. The relationship between trapped charge and P/E cycle stress can be realized.

By using our micro-second transient measurement circuit, word-line disturb induced threshold voltage shift is investigated and is found to be a serious reliability issue in this cell. Oxide charge trapping/detrapping induced read current fluctuation is discussed. Read current noise is increased in localized charge storage cells due to non-uniform Vt distribution. As the cycle number increases, the read current instability caused by RTN will become more severe. The improvement of bottom oxide reliability can significantly reduce this effect.

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