Chapter 1

Introduction

1.1 Overview of Low Temperature Poly-Si (LTPS) TFTs

For the application of large-area displays, the silicon wafer is too expensive to serve as the substrate of semiconductor layer. In order to reduce costs, glass substrate seems to be the best choice. Therefore, the low temperature technology is essential to proceed.

In contrast with a-Si TFTs, the field effect mobility of poly-Si TFTs is superior for high current applications. That is why LTPS TFTs have been regarded as the most potential devices of pixel switch and peripheral driver circuit in the active matrix liquid crystal display (AM-LCD) and active matrix organic light emitting diode (AM-OLED) for recent years.

Although LTPS TFTs were popularly studied, there are several problems need solving. Various crystallization methods have been occurred to some people and implemented to improve device-to-device variations. For instance, the light-shield plate successfully produced the graded energy density of excimer laser and the phase-shift mask led to the phase-modulated excimer laser intensity both focus on the excimer laser crystallization system, and the bridge

structure as well as light absorption layer effectively reduced the solidification velocity of melted region and the double-pulse method prolonged the existent time of melted region all concentrate on the melted film itself. But among such many ingenious crystallization methods, there is no one immediately applicable to excimer laser crystallization equipment nowadays.

1.2 Crystallization Methods of Poly-Si Thin Films

Crystallization of poly-Si thin films from a-Si has been considered the most important process in the fabrication of LTPS TFTs because the crystallized poly-Si thin films will be made for active layers namely channels in the LTPS TFTs. Obviously the quality of crystallized poly-Si thin films greatly influences the performance of LTPS TFTs. And less defect density will lead to higher quality of crystallized poly-Si thin films as well as higher performance of LTPS TFTs. Most defects such as dangling bonds and strained bonds are generated in the grain boundaries. These defects act as trap states in the band gap and degrade the carrier mobility, leakage current, and reliability of LTPS TFTs [1.1]-[1.9]. For the sake of reducing the defects in the grain boundaries, many methods were proposed in the last decades. All these methods enlarge grain size to effectively diminish the number of grain boundaries. Then, we classify these methods into three categories, i.e. solid phase crystallization (SPC), laser crystallization, and metal-induced crystallization (MIC).

Solid phase crystallization is the first widely investigated method to enlarge grain size. Thin films deposited in the amorphous state and then crystallized into poly-Si by thermal annealing at 600°C for a long time (~20hours). Unfortunately, the long annealing time limits its application on large-scale glass substrate for mass production requirement.

Laser crystallization is a recently popular method since its high throughput compared with SPC. The laser process heated the a-Si thin films to the melting point and subsequently the melting liquids began to solidify from several nucleation sites. As a result of recrystallizing from melting point, the grain size of poly-Si thin films is quite large with fewer grain boundaries. Although laser crystallization heats the a-Si thin films to the melting point, the underneath substrate does not suffer from high temperature damage or destruction. Among all kinds of lasers, excimer laser seems to be the most promising since its strong absorption of UV light in silicon.

Compared with SPC, the addition of certain metals to a-Si thin films can effectively lower the temperature of SPC. Ni was found to induce lateral crystallization of a-Si. This metal-induced lateral crystallization (MILC) has been demonstrated to fabricate LTPS TFTs free of metal contamination [1.10]-[1.16].

1.3 Motivation

Due to the random nucleation sites, the conventional LTPS TFTs suffered from random distribution of grain boundary. The pulse-to-pulse variation of excimer laser led to device-to-device variation. And narrow process window of laser energy density is a critical issue. All of them resulted in poor uniformity of conventional LTPS TFTs. The large variation of field effect mobility and threshold voltage makes design difficult. The high current applications are also restricted by the performance of LTPS TFTs. So, novel crystallization method is essential to control the nucleation sites. Good uniformity combined with high performance of LTPS TFTs is necessary.

Chapter 2

Low Temperature Polycrystalline Silicon Thin Film Transistors Fabricated by Excimer Laser Crystallization

2.1 Crystallization Mechanism of Excimer-Laser-Irradiated a-Si Thin Films

Fig. 2-1 is the setup of excimer laser crystallization. Excimer laser crystallization (ELC) was performed by KrF excimer laser (λ=248nm) in a vacuum chamber pumped down to 10^{-4} torr at RT or with substrate heating to 400°C and the number of laser shots per area was 100, i.e. 99% overlap between laser beams.

In order to understand the crystallization mechanism of excimer laser, the following fig. 2-2, fig 2-3, and fig. 2-4 illustrate three distinct regimes observed from the excimer-laser-irradiated a-Si thin films. That is partially melted regime (low energy density regime), completely melted regime (high energy density regime), and near-completely melted regime (super lateral growth regime). In partially melted regime, the energy density is too low to completely melt the a-Si thin film. Therefore, the unmelted a-Si remains and explosive

crystallization are observed [2.1], [2.2]. And the vertical regrowth from the unmelted a-Si remains lead to small-grain poly-Si. But in completely melted regime, the energy density is unduly high, i.e. no unmelted a-Si remains. And homogeneous nucleation also leads to small-grain poly-Si. However, in near-completely melted regime, the energy density is controlled to almost completely melt the a-Si thin film. The discretely unmelted a-Si islands make super lateral growth possible. Consequently, the optimal condition namely large grain occurs in near-completely melted regime.

2.2 Conventional LTPS TFTs Fabricated by Excimer Laser Crystallization

Fig. 2-5 is the process flowchart of conventional ELC LTPS TFT. The experimental procedures are as follows [2.3], [2.4]. Firstly, an amorphous silicon (a-Si) thin film with thickness of 500Å or/and 1000Å was deposited by pyrolysis of pure silane (SiH_4) with low-pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafer with oxide thickness of 1μm. Then, excimer laser crystallization (ELC) was performed by KrF excimer laser (λ=248nm) in a vacuum chamber pumped down to 10^{-4} torr at RT or with substrate heating to 400°C and the number of laser shots per area was 100, i.e. 99% overlap between laser beams. After defining the device active region, a 1000Å TEOS gate oxide was deposited by PECVD at 385°C. A 2000Å a-Si thin film was then deposited by LPCVD at 550°C for gate electrode. Then, the a-Si

thin film and gate oxide were etched by TCP-RIE to form the gate electrode. A self-aligned phosphorous ion implantation with dose of $5\times10^{15}cm^{-2}$ was carried out to form source and drain regions. Next, a 3000Å TEOS passivation oxide was deposited with PECVD at 385°C following by thermal annealing at 600°C for 12hours to activate the implanted dopants. Finally, contact holes formation and metallization were carried out after dopants activation. Up to now, the conventional ELC LTPS TFT has been finished.

2.3 Device-to-Device Variations of Conventional LTPS TFTs

2.3.1 Dependence of Field Effect Mobility on Laser Energy Density

Fig. 2-6(a) and (b) exhibit the dependence of field effect mobility on laser energy density of 100nm conventional ELC LTPS TFTs for W/L=10μm/10μm at RT or with substrate heating to 400°C. The narrow process window of laser energy density was observed in both figures. And high field effect mobility accompanied with poor uniformity was also perceived. But the performance with substrate heating to 400°C seems to be better than those at RT.

Fig. 2-7(a) and (b) exhibit the dependence of field effect mobility on laser energy density of 50nm conventional ELC LTPS TFTs for W/L=10μm/10μm at RT or with substrate heating to 400°C. Similarly, the performance and uniformity with substrate heating to 400°C are better than those at RT. But

compared with 100nm, the field effect mobility of 50nm conventional ELC LTPS TFTs is relatively low. Therefore, the a-Si thin film with thickness of 100nm is more suitable for high current applications. That is why we always used 100nm a-Si thin films to fabricate novel devices in the chapters followed.

2.3.2 Dependence of Field Effect Mobility on Device Dimension

Fig. 2-8(a) and (b) exhibit the dependence of field effect mobility on device dimension of 100nm conventional ELC LTPS TFTs at RT or with substrate heating to 400°C. The device-to-device variations become serious when the device dimension shrinks to the grain size. But for large dimension devices, the non-uniformity is balanced off.

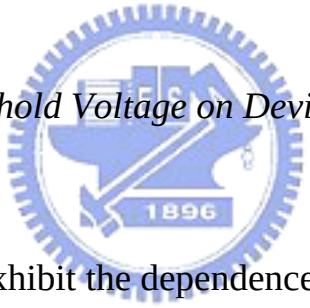
Fig. 2-9(a) and (b) exhibit the dependence of field effect mobility on device dimension of 50nm conventional ELC LTPS TFTs at RT or with substrate heating to 400°C. Also compared with 100nm, 50nm devices show better uniformity but worse performance. And the same as 100nm, the field effect mobility of large dimension devices is lower than small ones.

2.3.3 Dependence of Threshold Voltage on Laser Energy Density

Fig. 2-10(a) and (b) exhibit the dependence of threshold voltage on laser energy density of 100nm conventional ELC LTPS TFTs for W/L=10μm/10μm

at RT or with substrate heating to 400°C. To review fig. 2-6(a) and (b), the maximum variation of threshold voltage occurs in the vicinity where the field effect mobility is optimum, i.e. the corresponding laser energy density is just around the corner.

Fig. 2-11(a) and (b) exhibit the dependence of threshold voltage on laser energy density of 50nm conventional ELC LTPS TFTs for W/L=10μm/10μm at RT or with substrate heating to 400°C. Both 100nm and 50nm conventional ELC LTPS TFTs with substrate heating to 400°C demonstrate better uniformity than those merely at RT.



2.3.4 Dependence of Threshold Voltage on Device Dimension

Fig. 2-12(a) and (b) exhibit the dependence of threshold voltage on device dimension of 100nm conventional ELC LTPS TFTs at RT or with substrate heating to 400°C. It's like field effect mobility, threshold voltage also shows large variation in small dimension devices. Therefore, the uniformity of small dimension devices needs further improvement.

Fig. 2-13(a) and (b) exhibit the dependence of threshold voltage on device dimension of 50nm conventional ELC LTPS TFTs at RT or with substrate heating to 400°C. Threshold voltage differs from each distinct device dimension in both 100nm and 50nm conventional ELC LTPS TFTs.

2.4 Controlled Grain Growth without Pre-patterned a-Si Thin Films

2.4.1 Phase-modulated method

The phase-modulated method utilizes a phase-shift mask to make excimer laser generate interference, so as to modulate the trough of laser energy density to the level of near-completely melted regime. Then, the nucleation sites will be successfully arranged, and the large grain will crystallize from the artificial nucleation sites toward its right and left. Fig. 2-14 presents above-mentioned illustration.

Different step height of the phase-shift mask results in different interference phase. Fig. 2-15 shows the calculated intensity distribution as a function of the phase difference. In addition, the distance between phase-shift mask and the sample affects the intensity distribution as well as the length of lateral grain growth. Fig. 2-16 is the exhibition of the relationship between normalized intensity distributions and the distance from phase-shift mask to the sample. Fig. 2-17 is the 2-D controlled grain growth by means of phase-shift mask [2.5], [2.6].

2.4.2 Light-shield plate

Fig. 2-18 is the concept of large grain growth with graded excimer laser

energy density, and fig. 2-19 presents the graded laser energy density resulted from the light-shield plate [2.7]. Since laser energy density is graded, the lateral grain growth will be observed. Fig 2-20 is the 2-D controlled grain growth by means of light-shield plate [2.6].

2.5 Summary

In this chapter, whatever investigated is about the conventional ELC LTPS TFT, including the uniformity of field effect mobility and threshold voltage. All figures with substrate heating to 400°C presented high field effect mobility accompanied with good uniformity due to smaller solidification velocity. Although thickness of 100nm TFT is poor in uniformity, the performance of field effect mobility is better than 50nm one. Consequently, in the following chapters, excimer-laser-irradiated a-Si thin film of 100nm thickness with substrate heating to 400°C was adopted.

Chapter 3

Material Analysis of Polycrystalline Silicon Thin Films Fabricated by Excimer Laser Crystallization with Amorphous Silicon Spacer Structure

Many ELC methods have been reported to further improve the performance of conventional ELC LTPS TFTs [3.1]-[3.6]. Among all of the experimental procedures, the excimer laser crystallization is the most key one since the grain size of poly-Si thin film was determined in this step. Large grain size indicates high field effect mobility and few grain boundaries. Therefore, the novel method was proposed to enlarge the grain size and to diminish the grain boundaries [3.7].

3.1 Specimen Preparation for Material Analysis

Firstly, a 500Å or/and 1000Å silicon nitride (Si_3N_4) thin film was deposited by chemical reaction of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) with

low-pressure chemical vapor deposition (LPCVD) at 780°C on oxidized silicon wafer with oxide thickness of 1μm. Then, the silicon nitride layer in some regions was removed by reactive ion etching (RIE). A 1000Å amorphous silicon (a-Si) thin film was deposited by pyrolysis of pure silane (SiH_4) with LPCVD at 550°C. Subsequently, the upper a-Si layer was etched by transformer-coupled plasma reactive ion etching (TCP-RIE) to leave the a-Si spacer on the oxidized silicon wafer. After stripping off the remains of silicon nitride by heating phosphoric acid (H_3PO_4), another a-Si thin film with thickness of 1000Å was deposited also by LPCVD at 550°C. Excimer laser crystallization (ELC) was performed by KrF excimer laser (λ=248nm) in a vacuum chamber pumped down to 10^{-4} torr with substrate heating to 400°C and the number of laser shots per area was 20, i.e. 95% overlap between laser beams. Fig. 3-1 is the foregoing process flowchart.

3.2 Results and Discussion

3.2.1 SEM observation

Fig. 3-2 is the SEM of ELC poly-Si thin film with 50nm height a-Si spacer structure. The dotted lines indicate the a-Si spacer seeds namely nucleation sites during excimer laser irradiation. The left diagram is under optimal condition for 1μm grain length, and the right diagram is for 2μm grain length. Fig. 3-3 is the

SEM of ELC poly-Si thin film with 100nm height a-Si spacer structure. The right diagram is subjected to excimer laser of higher energy density than the left one. It is obviously that both of them are too high to be completely melted. Then, the small grains observed are the unmelted a-Si spacers.

3.2.2 AFM observation

In order to confirm that the a-Si spacer structure indeed formed, the AFM observation before and after excimer laser irradiation was carried out [3.8], [3.9]. Fig. 3-4 and fig. 3-5 exhibit the AFM of 50nm and 100nm height a-Si spacer structures before excimer laser irradiation. These diagrams distinctly described both existence of 50nm and 100nm height a-Si spacer structure. Fig. 3-6 and fig. 3-7 exhibit the AFM of ELC poly-Si thin film with 50nm and 100nm height a-Si spacer structures, respectively. It is obviously that 100nm height a-Si spacer is too thick. And the poly-Si thin film after excimer laser irradiation became rough.

3.3 Summary

The 100nm height a-Si spacer is observed partially melted after excimer laser irradiation. Therefore, for device fabrication, the relatively smooth surface of 50nm height a-Si spacer after excimer laser irradiation seems to be the better choice.

Chapter 4

Polycrystalline Silicon Thin Film Transistors Fabricated by Amorphous Silicon Spacer Structure with Pre-patterned Nitride Layer

According to the crystallization mechanism of excimer-laser-irradiated a-Si thin film, a novel crystallization method, i.e. a-Si spacer structure with pre-patterned nitride layer, was proposed to fabricate poly-Si TFTs. And the periodic grain growth on excimer-laser-irradiated a-Si thin film was achieved by this method [4.1].

4.1 Experimental Procedure

Firstly, a 500Å or/and 1000Å silicon nitride (Si_3N_4) thin film was deposited by chemical reaction of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) with low-pressure chemical vapor deposition (LPCVD) at 780°C on oxidized silicon wafer with oxide thickness of 1μm. Then, the silicon nitride layer in some

regions was removed by reactive ion etching (RIE). A 1000Å amorphous silicon (a-Si) thin film was deposited by pyrolysis of pure silane (SiH_4) with LPCVD at 550°C. Subsequently, the upper a-Si layer was etched by transformer-coupled plasma reactive ion etching (TCP-RIE) to leave the a-Si spacer on the oxidized silicon wafer. After stripping off the remains of silicon nitride by heating phosphoric acid (H_3PO_4), another a-Si thin film with thickness of 1000Å was deposited also by LPCVD at 550°C. Excimer laser crystallization (ELC) was performed by KrF excimer laser (λ=248nm) in a vacuum chamber pumped down to 10^{-4} torr with substrate heating to 400°C and the number of laser shots per area was 20, i.e. 95% overlap between laser beams. After defining the device active region, a 1000Å tetraethyl orthosilicate (TEOS) gate oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. A 2000Å a-Si thin film was then deposited by LPCVD at 550°C for gate electrode. The a-Si thin film and gate oxide were etched by TCP-RIE to form the gate electrode. A self-aligned phosphorous ion implantation with dose of $5\times10^{15}cm^{-2}$ was carried out to form source and drain regions. Next, a 3000Å TEOS passivation oxide was deposited with PECVD at 385°C following by thermal annealing at 600°C for 12hours to activate the implanted dopants. Finally, contact holes formation and metallization were carried out after dopants activation. For the sake of comparison, the conventional ELC poly-Si TFT with active region thickness of 1000Å was also fabricated.

Fig. 4-1 is the process flowchart of a-Si spacer structure with pre-patterned

nitride layer [4.2], and fig. 4-2 is the process flowchart of ELC poly-Si TFT with a-Si spacer structure.

4.2 Results and Discussion

Among these process procedures, the upper a-Si layer was etched by TCP-RIE to leave the a-Si spacer on the oxidized silicon wafer is the most key one. Because the upper a-Si layer should be precisely etched to leave the a-Si spacer behind only and other regions of a-Si should be all removed for a certainty. The etching rate of a-Si layer with TCP-RIE is the critical parameter.

Two kinds of thickness of Si_3N_4 thin films were used to modulate the a-Si spacer height. The a-Si spacer height is required to ensure that the a-Si thin film with a-Si spacer structure will become smooth after excimer laser irradiation. That is to say, the apparent residues of unmelted a-Si spacer must not exist in the crystallized poly-Si thin film. Although limitless raise of laser energy density can avoid the residues of unmelted a-Si spacer, too high laser energy density will lead to fine-grain and small-grain poly-Si thin film observed in completely melted regime. Therefore, the laser energy density and the a-Si spacer height must be adjusted to meet optimal condition.

4.2.1 Small dimension devices

Fig. 4-3(a) to 4-6(b) exhibit both the transfer and output characteristics of ELC poly-Si TFTs with 50nm height a-Si spacer structure for W/L=2μm/2μm, 3μm/3μm, 4μm/4μm, as well as 5μm/5μm and conventional counterparts, respectively. Among these transfer characteristics figures, the fig. 4-3(a) of W/L=2μm/2μm reveals optimum field effect mobility, and the output characteristics fig. 4-3(b) also reveals higher output current than others. But at the same time the decrease in field effect mobility one by one is observed when the device dimension expands. This phenomenon resulted from the maximum grain length limited by excimer laser crystallization. During excimer laser irradiation, the more vertical and lateral thermal gradient, the faster grain solidified [4.3]. Due to a large amount of heat transfer in the transition of crystallization, large solidification velocity of lateral grain growth will lead to reduction of the maximum grain length. Therefore, if we want to increase the maximum grain length, the sufficiently little solidification velocity is essential. The maximum grain length of lateral grain growth depends greatly on the thickness of a-Si thin film and the excimer laser energy density which both directly affect the solidification velocity of poly-Si [4.4]. In this thesis, the maximum grain length is between 2μm and 3μm. Besides, all output characteristics show higher current of ELC poly-Si TFT with 50nm height a-Si spacer structure than conventional counterparts. It is considered very competent for high current applications.

The electrical characteristics including threshold voltage, field effect mobility, sub-threshold swing, and on/off current ratio of ELC poly-Si TFT with 50nm height a-Si spacer structure for different device dimension and conventional counterparts were summarized in table 4-1. The field effect mobility of ELC poly-Si TFT with 50nm height a-Si spacer structure is indeed higher than conventional counterpart for each device dimension since a-Si spacer seed successfully contributed to periodic grain growth of poly-Si thin film.

Fig. 4-7 presents the dependence of field effect mobility on laser energy density of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=2μm/2μm and conventional counterpart. The conventional counterpart exists narrower process window of laser energy density than ELC poly-Si TFT with 50nm height a-Si spacer structure because of its random nucleation sites. In the conventional excimer laser crystallization, the corresponding laser energy density to near-completely melted regime is very critical. And because the thickness of a-Si thin film of conventional counterpart is uniform, the nucleation sites of conventional counterpart are obliged to distribute randomly. Besides, large variation of field effect mobility and narrow process window of laser energy density concurred because, in conventional devices, higher performance is followed by less uniformity. But the ELC poly-Si TFT with 50nm height a-Si spacer structure presents wide process window of laser energy density and uniform field effect mobility simultaneously. This is owing to the controlled

nucleation sites with a-Si spacer structure [4.5], [4.6].

Fig. 4-8(a) to 4-11(b) exhibit both the transfer and output characteristics of ELC poly-Si TFTs with 100nm height a-Si spacer structure for W/L=2μm/2μm, 3μm/3μm, 4μm/4μm, as well as 5μm/5μm and conventional counterparts, respectively. Like 50nm height a-Si spacer structure, the transfer characteristics fig. 4-8(a) of W/L=2μm/2μm reveals optimum field effect mobility. And the same as 50nm height a-Si spacer structure, the decrease in field effect mobility one by one is also observed when the device dimension expands due to the limited maximum grain length. The electrical characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for different device dimension and conventional counterparts were summarized in table 4-2. Table 4-3 compares the electrical characteristics of ELC poly-Si TFT with 50nm to 100nm height a-Si spacer structure for different device dimension. The poorer field effect mobility coincides with the material analysis in chapter 3 that the 100nm a-Si spacer seeds were partially melted after excimer laser irradiation. So, the 50nm height a-Si spacer structure is the better choice for ELC poly-Si TFT. But even though the 100nm height a-Si spacer structure will leave the unmelted a-Si seeds behind after excimer laser irradiation, nevertheless, its periodic grain growth of poly-Si thin film shows better performance than conventional counterpart.

4.2.2 Large dimension devices

The novel crystallization method, viz a-Si spacer structure with pre-patterned nitride layer, can be applied to not only small dimension devices but also large dimension ones. Fig. 4-12(a) is the diagram of periodic grain growth for large dimension devices applications. The dotted lines indicate the contrived nucleation sites, that is, the locations of a-Si spacer seeds before excimer laser irradiation. During excimer laser irradiation, the melted a-Si thin film crystallized from those contrived nucleation sites towards their both sides [4.7]. Fig. 4-12(b) represents the periodic grain growth for large dimension devices after gate electrode formation. It is perceived that only several perpendicular grain boundaries exist in the active region. This achievement is very applicable to large dimensions devices applications.

Fig. 4-13(a) to 4-16(b) exhibit both the transfer and output characteristics of ELC poly-Si TFTs with 50nm height and 2μm, 2.5μm, 3μm, as well as 4μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart, respectively. The field effect mobility and output current of ELC poly-Si TFTs with 50nm height and different distance a-Si spacer structure for W/L=10μm/10μm were all observed better than conventional counterparts because of periodic grain growth resulted from controlled nucleation sites. Furthermore, from the table 4-4, the electrical characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure and W/L=10μm/10μm for different a-Si spacer distance and conventional counterpart, the optimum field effect

mobility occurs when the a-Si spacer distance is 2.5μm which conforms to the above-mentioned maximum grain length limited by excimer laser crystallization.

Similarly, fig. 4-17(a) to 4-20(b) exhibit both the transfer and output characteristics of ELC poly-Si TFTs with 50nm height and 2μm, 2.5μm, 3μm, as well as 4μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart, respectively. Even when device dimension expanded to W/L=20μm/20μm, the field effect mobility and output current of ELC poly-Si TFTs with 50nm height and different distance a-Si spacer structure were also improved as for W/L=10μm/10μm due to effectively controlled nucleation sites. Table 4-5 the same summarized the electrical characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure and W/L=20μm/20μm for different a-Si spacer distance and conventional counterpart. The optimum field effect mobility also appears as for W/L=10μm/10μm when the a-Si spacer distance is 2.5μm.

To compare W/L=10μm/10μm with W/L=20μm/20μm, the larger dimension device suffers from more perpendicular grain boundaries which result in lower field effect mobility even though the grain length is subjected to the maximum.

4.3 Summary

In this chapter, the novel a-Si spacer structure with pre-patterned nitride layer was demonstrated. The optimal height of a-Si spacer seed is 50nm. Due to periodic grain growth resulted from controlled nucleation sites, the field effect mobility and output current of ELC poly-Si TFTs with 50nm height a-Si spacer structure for both small and large dimension devices were evidently improved. Despite partially melted a-Si spacer seeds of 100nm height, the field effect mobility and output current of ELC poly-Si TFTs with 100nm height a-Si spacer structure for small dimension devices were similarly improved. These are all attributed to the periodic arrangement of grain and grain boundary. Besides, the uniformity of field effect mobility and process window of laser energy density for small dimension device were also raised. In this thesis, the maximum grain length is 2.5μm [4.8], [4.9]. So, the optimum field effect mobility were observed for both W/L=10μm/10μm and 20μm/20μm when the a-Si spacer distance was 2.5μm.

Chapter 5

Low Temperature Polycrystalline Silicon Thin Film Transistors Fabricated by Amorphous Silicon Spacer Structure with Pre-patterned TEOS Oxide Layer

Although the a-Si spacer structure with pre-patterned nitride layer proposed in chapter 4 has been successfully used to fabricate high performance ELC poly-Si TFTs, another a-Si spacer structure was carried out to further improve the electrical characteristics of ELC poly-Si TFTs, namely a-Si spacer structure with pre-patterned TEOS oxide layer [5.1]. The a-Si spacer seed of the former a-Si spacer structure with pre-patterned nitride layer was below and encircled by another a-Si thin film deposition, which led to extended seed. According to the crystallization mechanism of excimer laser irradiation, we expect that the narrower seeds will result in precisely controlled nucleation sites and even better performance and uniformity of devices. Consequently, another a-Si spacer structure has been proposed to achieve this goal. Fig. 5-1 is the comparison of two a-Si spacer structures [5.2]. It's unlike the former structure, the a-Si spacer

seed of the latter one was over the initial deposition of a-Si thin film. It is obviously that the under illustration reveals narrower seeds than the upper one.

5.1 Experimental Procedure

Firstly, an amorphous silicon (a-Si) thin film with thickness of 1000Å was deposited by pyrolysis of pure silane (SiH_4) with low-pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafer with oxide thickness of 1μm. Then, a 500Å or/and 1000Å tetraethyl orthosilicate (TEOS) oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. The TEOS oxide layer in some regions was removed following by another 1000Å a-Si layer deposition with LPCVD at 550°C. Subsequently, the upper a-Si layer was etched by transformer-coupled plasma reactive ion etching (TCP-RIE) to leave the a-Si spacer on the initial a-Si thin film. After stripping off the remains of TEOS oxide by buffer oxide etchant (BOE), excimer laser crystallization (ELC) was performed by KrF excimer laser (λ=248nm) in a vacuum chamber pumped down to 10^{-4} torr with substrate heating to 400°C and the number of laser shots per area was 20, i.e. 95% overlap between laser beams [5.3]. After defining the device active region, a 1000Å TEOS gate oxide was deposited also by PECVD at 385°C. A 2000Å a-Si thin film was then deposited by LPCVD at 550°C for gate electrode. The a-Si thin film and gate oxide were etched by TCP-RIE to form the gate electrode. A self-aligned phosphorous ion

implantation with dose of $5\times10^{15}cm^{-2}$ was carried out to form source and drain regions. Next, a 3000Å TEOS passivation oxide was deposited with PECVD at 385°C following by thermal annealing at 600°C for 12hours to activate the implanted dopants. Finally, contact holes formation and metallization were carried out after dopants activation. For the sake of comparison, the conventional ELC LTPS TFTs with active region thickness of 1000Å were also fabricated.

Fig. 5-2 is the process flowchart of a-Si spacer structure with pre-patterned TEOS oxide layer, and fig. 5-3 is the process flowchart of ELC LTPS TFT with a-Si spacer structure.

5.2 Results and Discussion

The same as experimental procedure in chapter 4, there is the most key one among the foregoing process procedures, that is, the upper a-Si layer was etched by TCP-RIE to leave the a-Si spacer on the initial a-Si thin film. Because the material of etching stop layer is identical to the upper a-Si layer, the upper a-Si layer should be precisely etched to leave the a-Si spacer behind and not to damage the under a-Si thin film. The etching rate of a-Si layer with TCP-RIE is the critical parameter and the stability of TCP-RIE is the most essential element. In this chapter, we used end-point mode of TCP-RIE to automatically detect when the upper a-Si layer was almost completely etched. The end-point mode

operated by means of detecting the flow of gaseous products. The abruptly decreased flow of gaseous products indicated that the upper a-Si layer was almost completely etched.

Two kinds of thickness of TEOS oxide thin films were used to modulate the a-Si spacer height. The a-Si spacer height is required to ensure that the a-Si thin film with a-Si spacer structure will become smooth after excimer laser irradiation. That is to say, the apparent residues of unmelted a-Si spacer must not exist in the crystallized poly-Si thin film. Although limitless raise of laser energy density can avoid the residues of unmelted a-Si spacer, too high laser energy density will lead to fine-grain and small-grain poly-Si thin film observed in completely melted regime. Therefore, the laser energy density and the a-Si spacer height must be adjusted to meet optimal condition. This perspective is the same as a-Si spacer structure with pre-patterned nitride layer in chapter 4.

5.2.1 Small dimension devices

Fig. 5-4(a) to 5-7(b) exhibit both the transfer and output characteristics of ELC LTPS TFTs with 50nm height a-Si spacer structure for W/L=2μm/2μm, 3μm/3μm, 4μm/4μm, as well as 5μm/5μm and conventional counterparts, respectively. Among these transfer characteristics figures, the fig. 5-4(a) of W/L=2μm/2μm reveals optimum field effect mobility, and the output characteristics fig. 5-4(b) also reveals higher output current than others. But at

the same time the decrease in field effect mobility one by one is observed when the device dimension expands. This phenomenon resembled those in chapter 4 and also resulted from the maximum grain length limited by excimer laser crystallization [5.4]. During excimer laser irradiation, the more vertical and lateral thermal gradient, the faster grain solidified. Due to a large amount of heat transfer in the transition of crystallization, large solidification velocity of lateral grain growth will lead to reduction of the maximum grain length [5.5]. Therefore, if we want to increase the maximum grain length, the sufficiently little solidification velocity is essential [5.6]. The maximum grain length of lateral grain growth depends greatly on the thickness of a-Si thin film and the excimer laser energy density which both directly affect the solidification velocity of poly-Si. In this thesis, the maximum grain length is between 2μm and 3μm. Besides, all output characteristics show higher current of ELC LTPS TFT with 50nm height a-Si spacer structure than conventional counterparts. It is considered very competent for high current applications.

The electrical characteristics including threshold voltage, field effect mobility, sub-threshold swing, and on/off current ratio of ELC LTPS TFT with 50nm height a-Si spacer structure for different device dimension and conventional counterparts were summarized in table 5-1. The field effect mobility of ELC LTPS TFT with 50nm height a-Si spacer structure is indeed higher than conventional counterpart for each device dimension since a-Si spacer seeds successfully contributed to periodic grain growth of poly-Si thin

film. Additionally, electrical characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for different pre-patterned layer and device dimension were also summarized in table 5-2.

Fig. 5-8(a) and fig. 5-8(b) present the dependence of field effect mobility and threshold voltage on laser energy density of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=2μm/2μm and substrate heating to 400°C, respectively. It's unlike the conventional device, the ELC LTPS TFT with 50nm height a-Si spacer structure presents wide process window of laser energy density and uniform field effect mobility simultaneously. Furthermore, the field effect mobility is kept in high level within a wide range of laser energy density. These are all owing to the controlled nucleation sites with a-Si spacer structure [5.7]. Besides, the variations of threshold voltage were also decreased. The device-to-device variation has been a thorny problem toward the circuit designer for a long time.

5.2.2 Large dimension devices

The novel crystallization method, viz a-Si spacer structure with pre-patterned TEOS oxide layer, can be applied to not only small dimension devices but also large dimension ones. To review the mentioned in chapter 4, fig. 4-12(a) is the diagram of periodic grain growth for large dimension devices applications. The dotted lines indicate the contrived nucleation sites, that is, the

locations of a-Si spacer seeds before excimer laser irradiation. During excimer laser irradiation, the melted a-Si thin film crystallized from those contrived nucleation sites towards their both sides. Fig. 4-12(b) represents the periodic grain growth for large dimension devices after gate electrode formation. It is perceived that only several perpendicular grain boundaries exist in the active region. In this chapter, these results are observed again. This achievement is very applicable to large dimensions devices applications.

Fig. 5-9(a) to 5-12(b) exhibit both the transfer and output characteristics of ELC LTPS TFTs with 50nm height and 2μm, 2.5μm, 3μm, as well as 4μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart, respectively. The field effect mobility and output current of ELC LTPS TFTs with 50nm height and different distance a-Si spacer structure for W/L=10μm/10μm were all observed better than conventional counterparts because of periodic grain growth resulting from controlled nucleation sites. Furthermore, from the table 5-3, the electrical characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure and W/L=10μm/10μm for different a-Si spacer distance and conventional counterpart, the optimum field effect mobility occurs when the a-Si spacer distance is 2.5μm which conforms to the above-mentioned maximum grain length limited by excimer laser crystallization and the data summarized in table 4-4.

Similarly, fig. 5-13(a) to 5-16(b) exhibit both the transfer and output

characteristics of ELC LTPS TFTs with 50nm height and 2μm, 2.5μm, 3μm, as well as 4μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart, respectively. Even when device dimension expanded to W/L=20μm/20μm, the field effect mobility and output current of ELC LTPS TFTs with 50nm height and different distance a-Si spacer structure were also improved as for W/L=10μm/10μm due to effectively controlled nucleation sites. Table 5-4 the same summarized the electrical characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure and W/L=20μm/20μm for different a-Si spacer distance and conventional counterpart. The optimum field effect mobility also appears as for W/L=10μm/10μm when the a-Si spacer distance is 2.5μm.

To compare W/L=10μm/10μm with W/L=20μm/20μm, the larger dimension device suffers from more perpendicular grain boundaries which result in lower field effect mobility even though the grain length is subjected to the maximum. This result is the same as the a-Si spacer structure with pre-patterned nitride layer.

5.3 Summary

Instead of pre-patterned nitride layer in last chapter, the use of pre-patterned TEOS oxide layer is essential to construct the a-Si spacer seed over the initially deposited a-Si thin film. This is because no nitride layer with

low temperature of deposition is available. If the TEOS oxide deposited by PECVD at 385°C in fig. 5-2 is replaced by the nitride deposited by LPCVD at 780°C, the initial a-Si thin film will crystallize into poly-Si because of the thermal annealing of SPC before excimer laser irradiation. So, the choice of TEOS oxide is not due to the property of material but the temperature of deposition. It is especially important to fabricate ELC LTPS TFTs.

Periodic-grain-growth LTPS TFTs exhibit better performance and uniformity than conventional devices due to effective control of nucleation sites [5.8]. Even for small dimension devices, the good uniformity combined with high field effect mobility was observed. Moreover, the dependence of field effect mobility and threshold voltage on laser energy density became unobvious. Owing to uniform distribution of large grain size, the novel a-Si spacer structure can not only improve performance of small dimension devices but also apply to fabrication of large dimension ones.

According to the experimental results, the narrower a-Si spacer seeds indeed brought about precisely controlled nucleation sites and then higher performance of devices.

Chapter 6

Conclusion

Periodic-grain-growth (PGG) LTPS TFTs exhibit better performance and uniformity than conventional devices due to effective control of nucleation sites. Since uniform distribution of grain size, the novel PGG method with two kinds of a-Si spacer structures can not only improve performance of small dimension devices but also apply to fabrication of large dimension devices. According to the experimental results, the narrower a-Si spacer seeds will result in precisely controlled nucleation sites and then better performance and uniformity of devices. In the application of long channel devices, these novel structures also presented better performance than those others proposed. The improvement is very suitable to future system on panel (SOP) applications with AMLCD or AMOLED [6.1]-[6.10].

In this thesis, **NO NH_3 PLASMA TREATMENT IS EXECUTED.** Therefore, the field effect mobility and sub-threshold swing after passivation process will be further improved. But the reliability will become the critical issue.

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