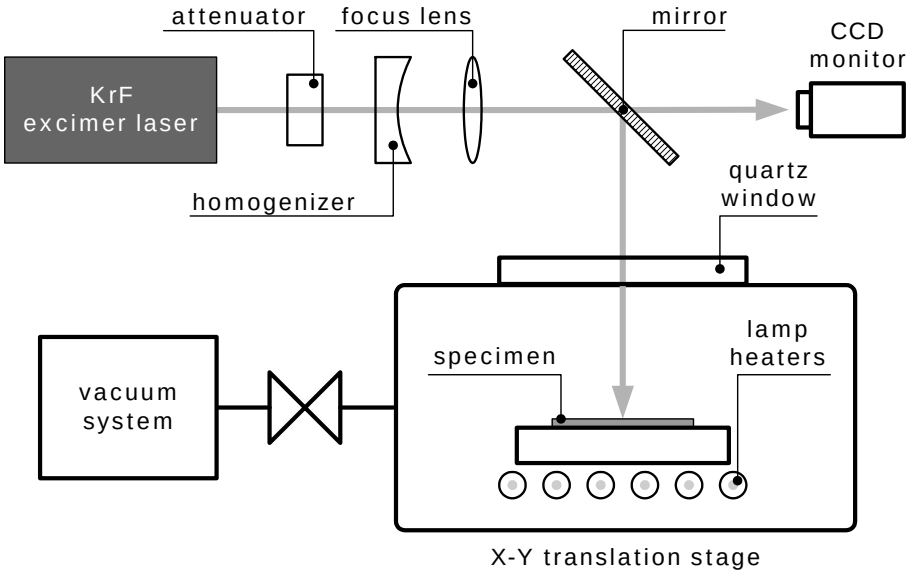


Fig. 2-1 The setup of excimer laser crystallization

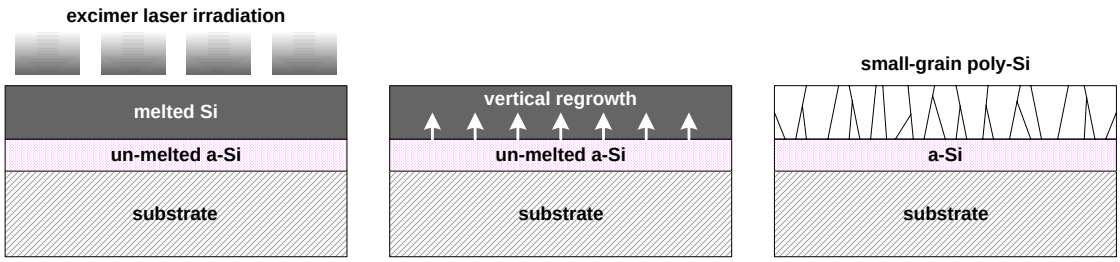


Fig. 2-2 Partially melted regime (low energy density regime)

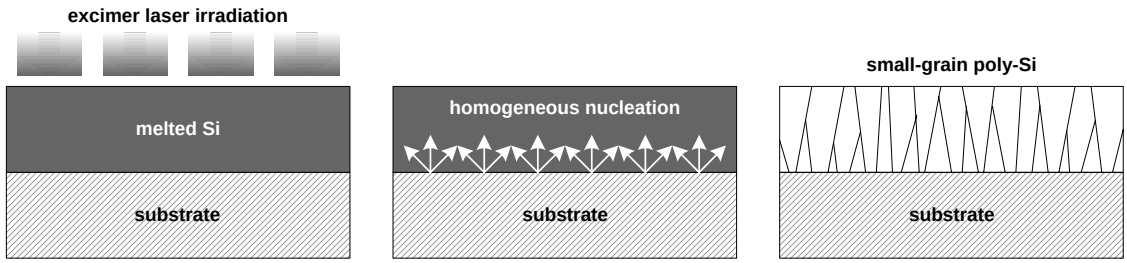


Fig. 2-3 Completely melted regime (high energy density regime)

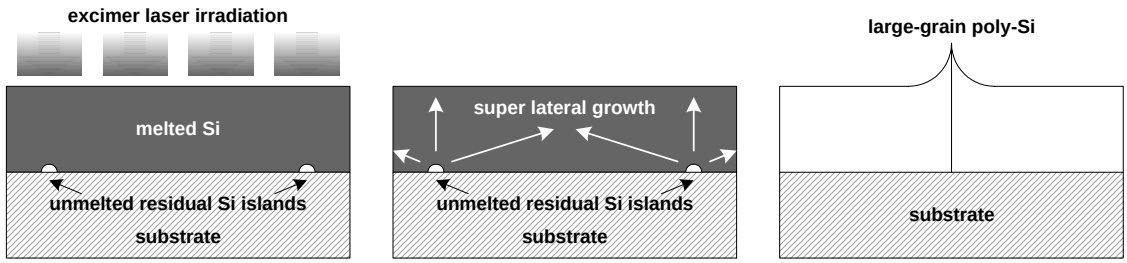


Fig. 2-4 Near-completely melted regime (super lateral growth regime)

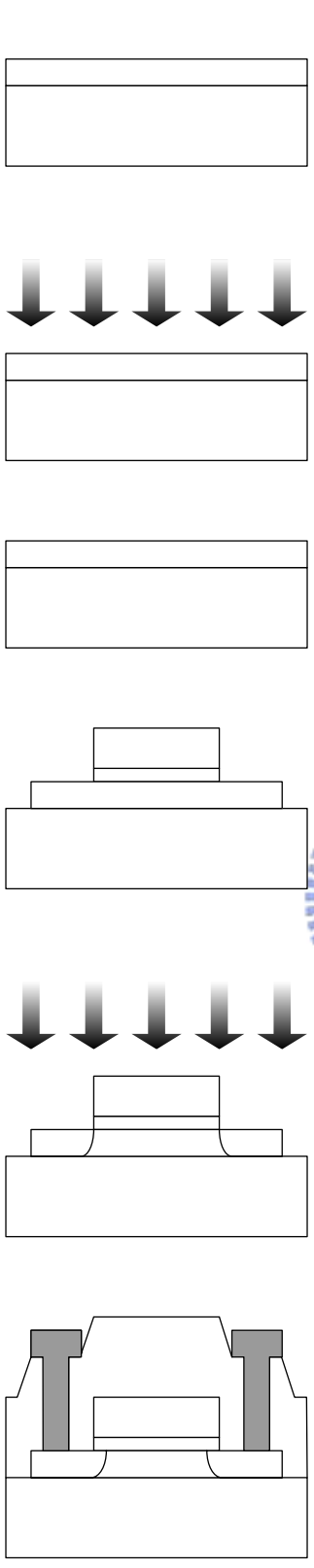


Fig. 2-5 Process flowchart of conventional ELC LTPS TFT

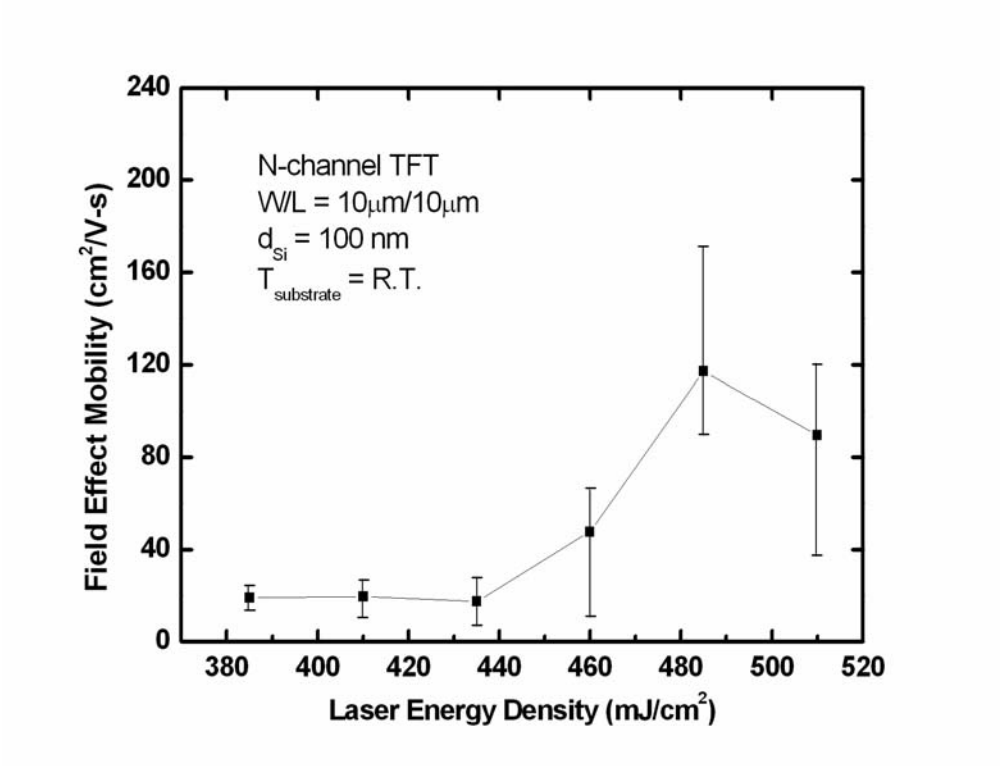


Fig. 2-6(a) Dependence of field effect mobility on laser energy density of 100nm conventional ELC LTPS TFTs for W/L=10μm/10μm at RT

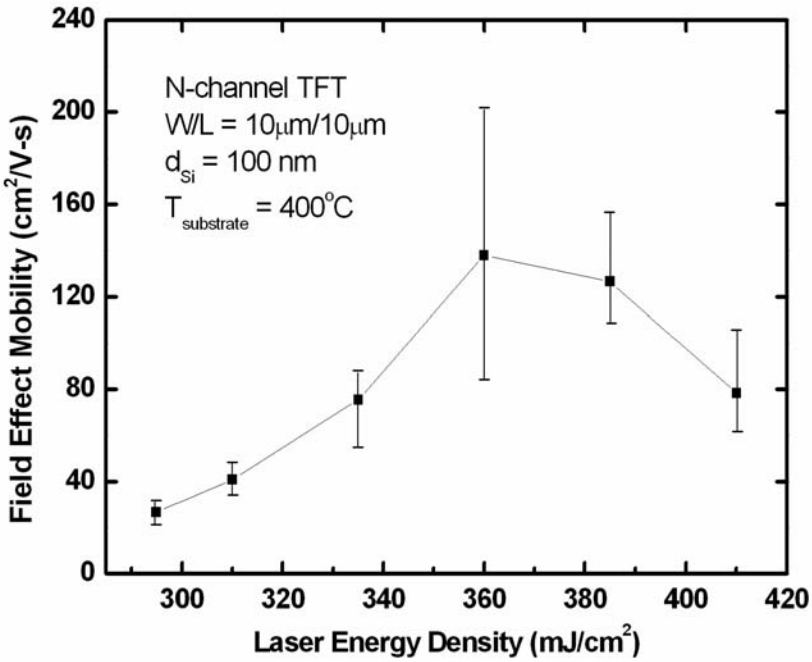


Fig. 2-6(b) Dependence of field effect mobility on laser energy density of 100nm conventional ELC LTPS TFTs for W/L=10μm/10μm with substrate heating to 400ºC

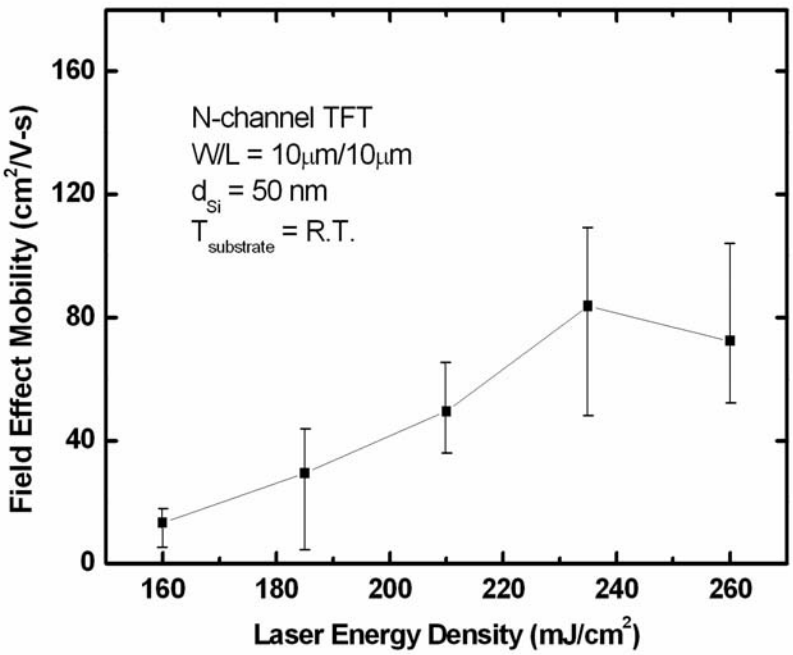


Fig. 2-7(a) Dependence of field effect mobility on laser energy density of 50nm conventional ELC LTPS TFTs for W/L=10μm/10μm at RT

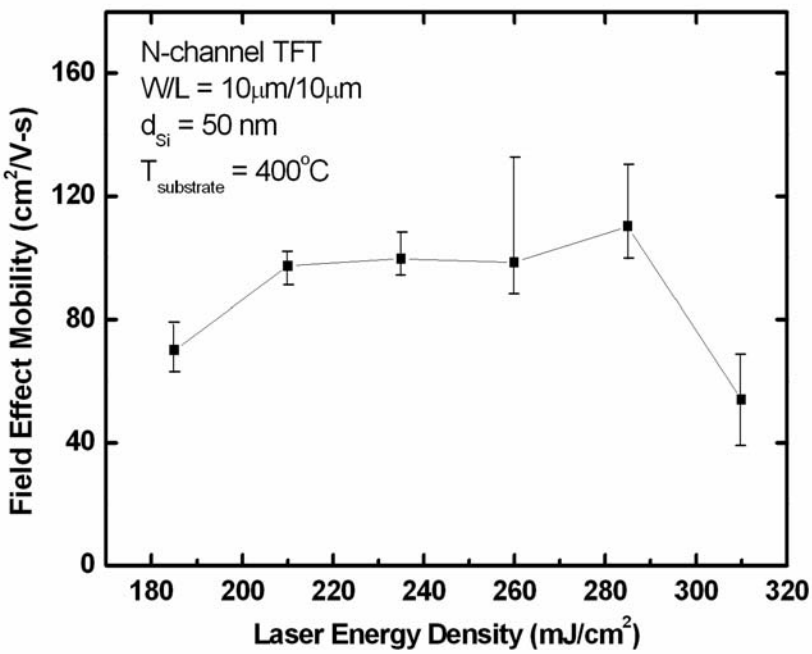


Fig. 2-7(b) Dependence of field effect mobility on laser energy density of 50nm conventional ELC LTPS TFTs for W/L=10μm/10μm with substrate heating to 400ºC

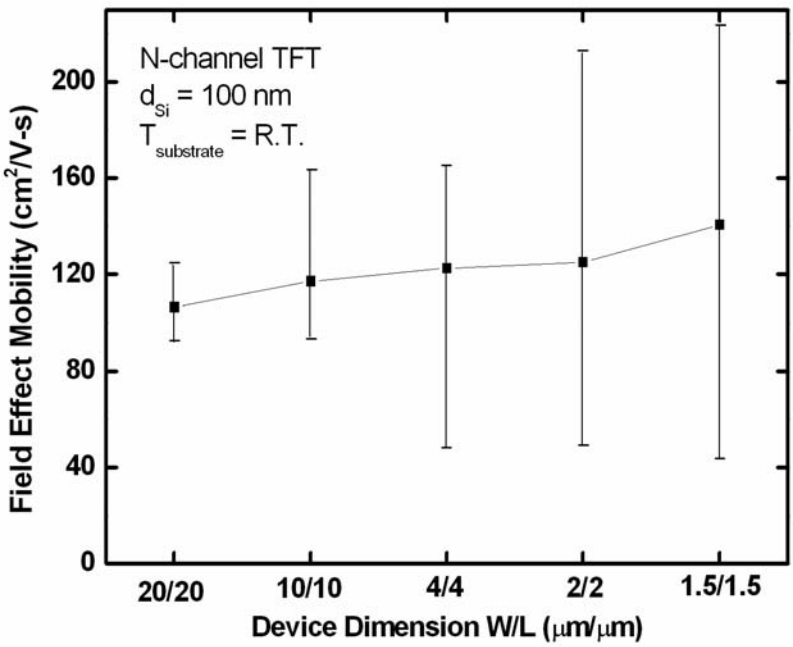


Fig. 2-8(a) Dependence of field effect mobility on device dimension of 100nm conventional ELC LTPS TFTs at RT

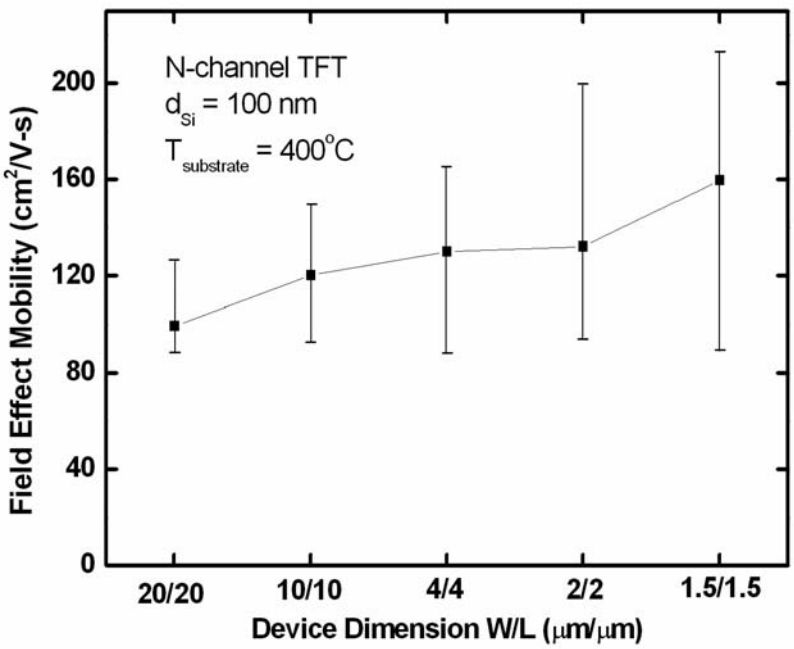


Fig. 2-8(b) Dependence of field effect mobility on device dimension of 100nm conventional ELC LTPS TFTs with substrate heating to 400ºC

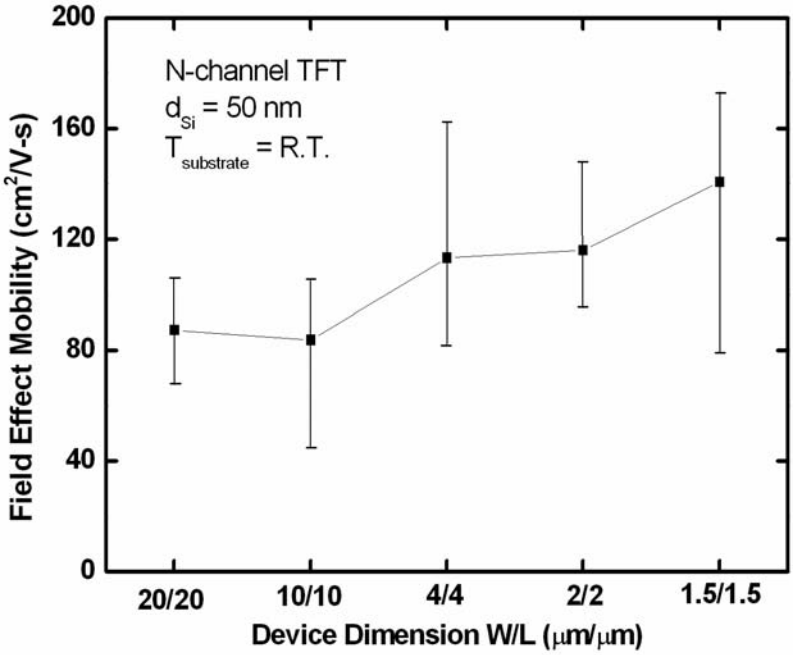


Fig. 2-9(a) Dependence of field effect mobility on device dimension of 50nm conventional ELC LTPS TFTs at RT

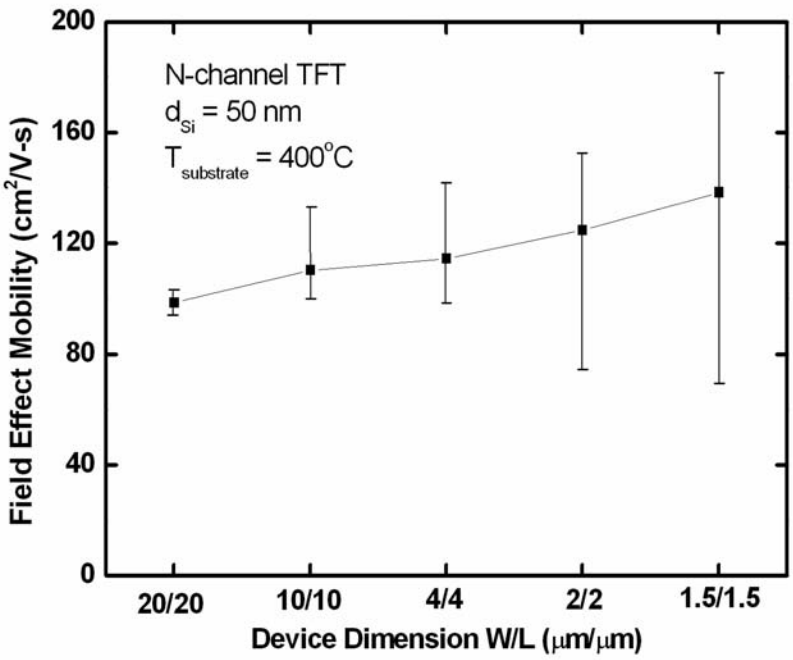


Fig. 2-9(b) Dependence of field effect mobility on device dimension of 50nm conventional ELC LTPS TFTs with substrate heating to 400ºC

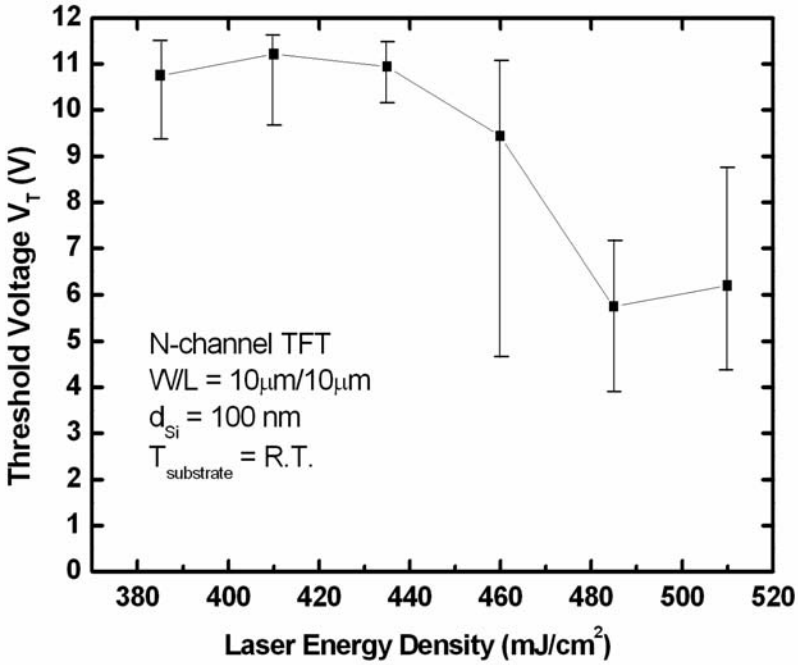


Fig. 2-10(a) Dependence of threshold voltage on laser energy density of 100nm conventional ELC LTPS TFTs for W/L=10μm/10μm at RT

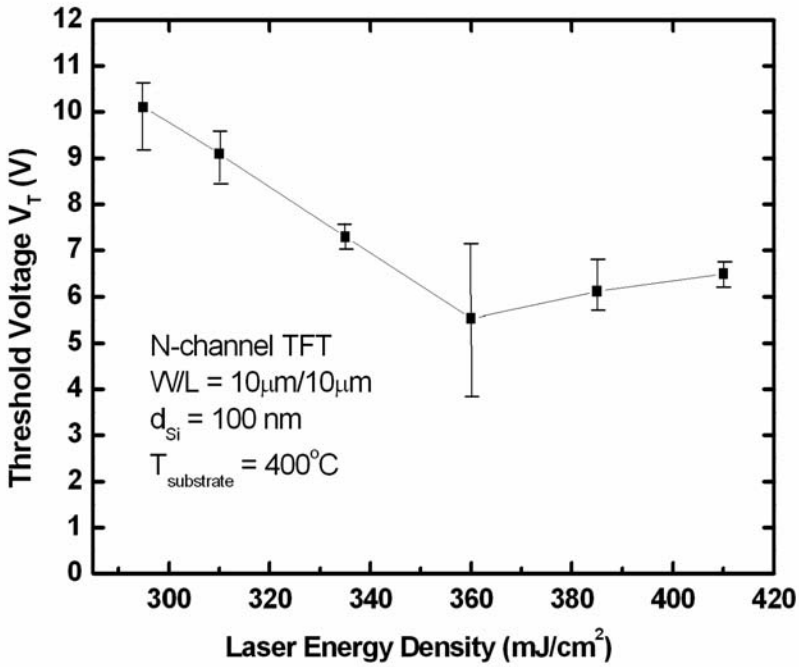


Fig. 2-10(b) Dependence of threshold voltage on laser energy density of 100nm conventional ELC LTPS TFTs for W/L=10μm/10μm with substrate heating to 400ºC

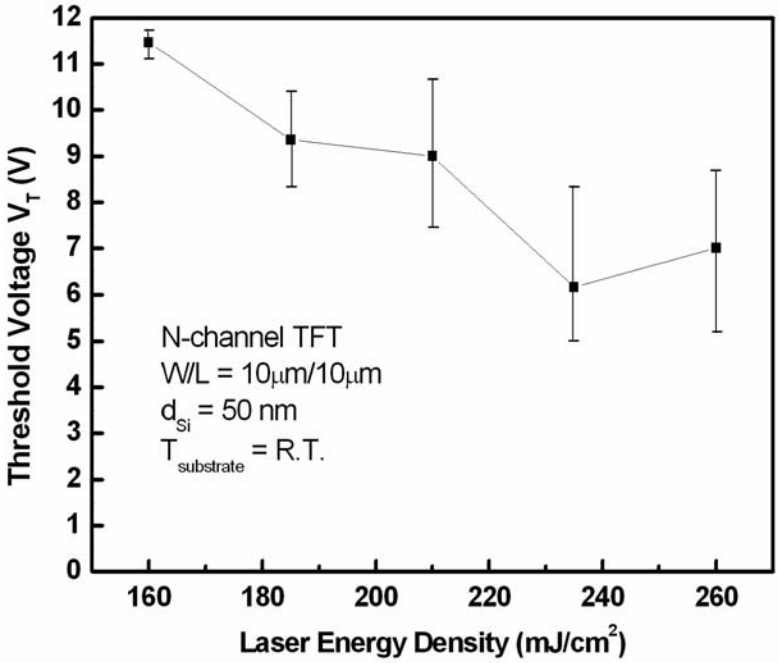


Fig. 2-11(a) Dependence of threshold voltage on laser energy density of 50nm conventional ELC LTPS TFTs for W/L=10μm/10μm at RT

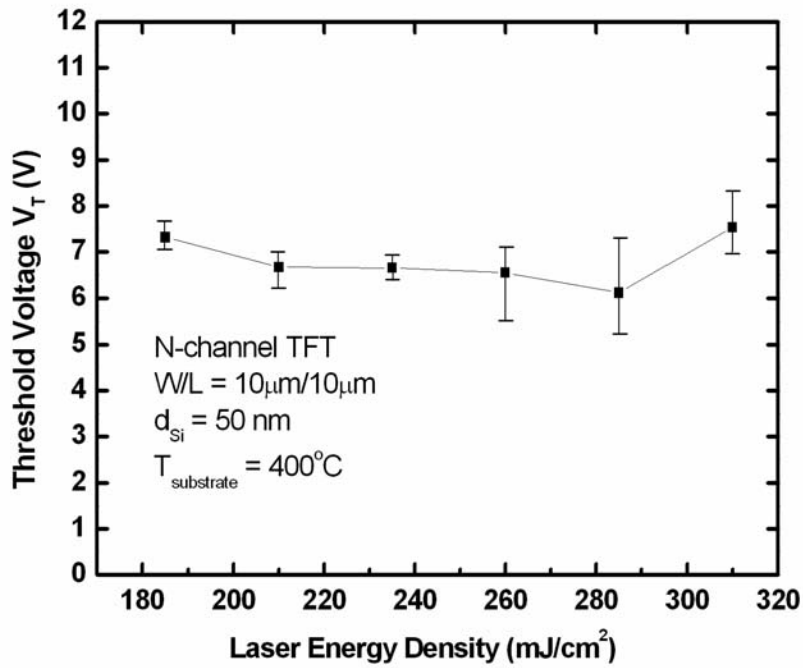


Fig. 2-11(b) Dependence of threshold voltage on laser energy density of 50nm conventional ELC LTPS TFTs for W/L=10μm/10μm with substrate heating to 400ºC

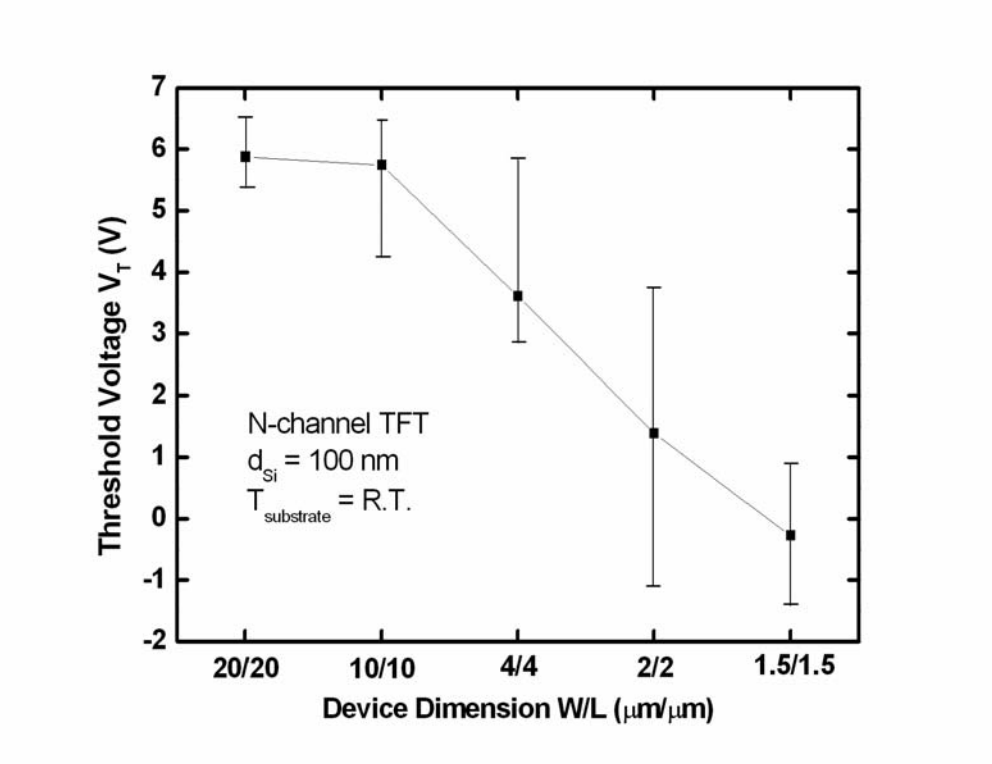


Fig. 2-12(a) Dependence of threshold voltage on device dimension of 100nm conventional ELC LTPS TFTs at RT

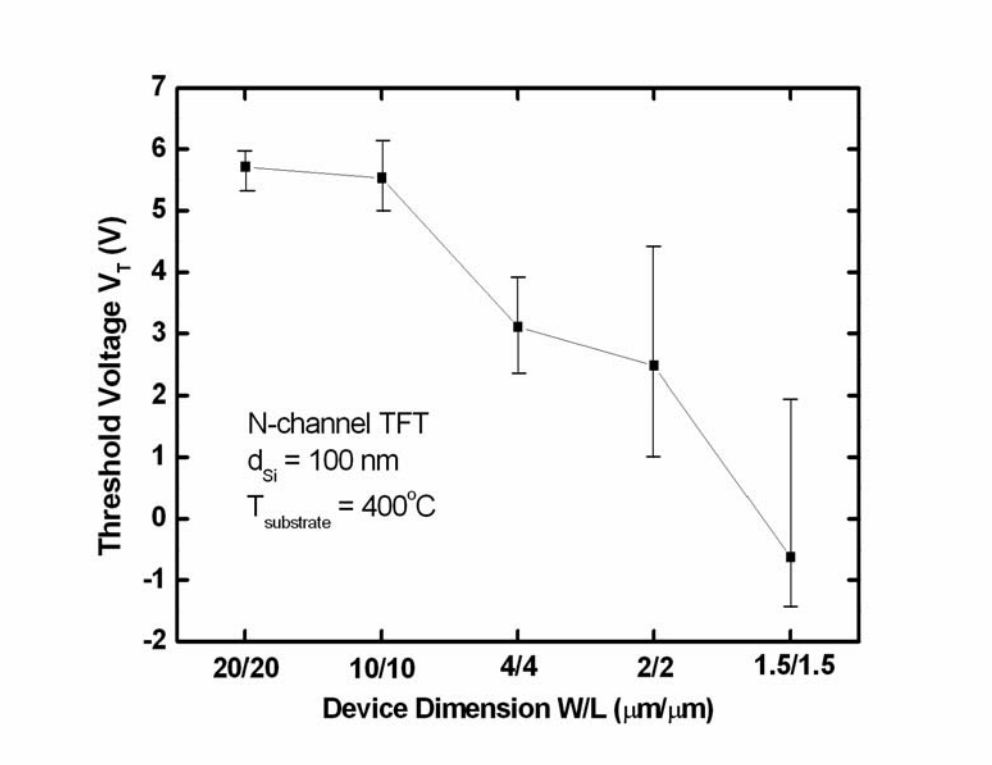


Fig. 2-12(b) Dependence of threshold voltage on device dimension of 100nm conventional ELC LTPS TFTs with substrate heating to 400ºC

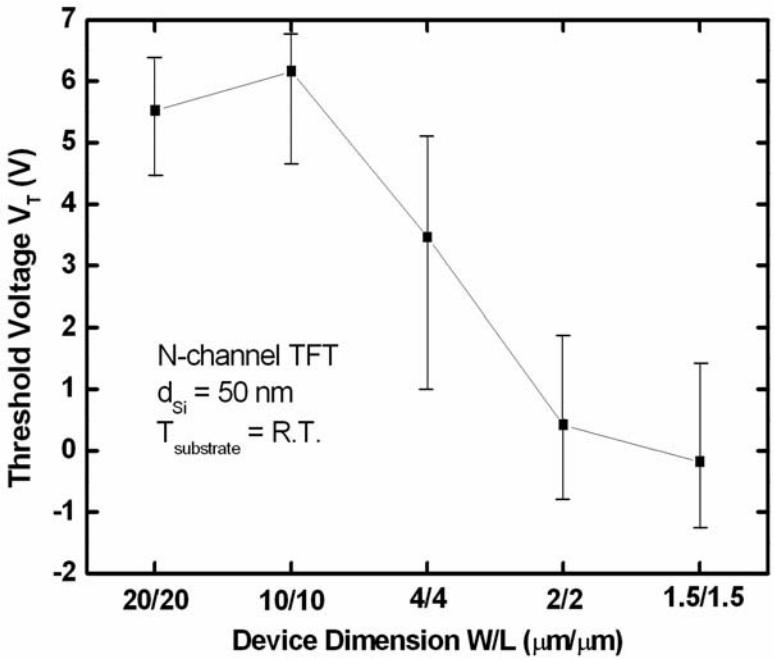


Fig. 2-13(a) Dependence of threshold voltage on device dimension of 50nm conventional ELC LTPS TFTs at RT

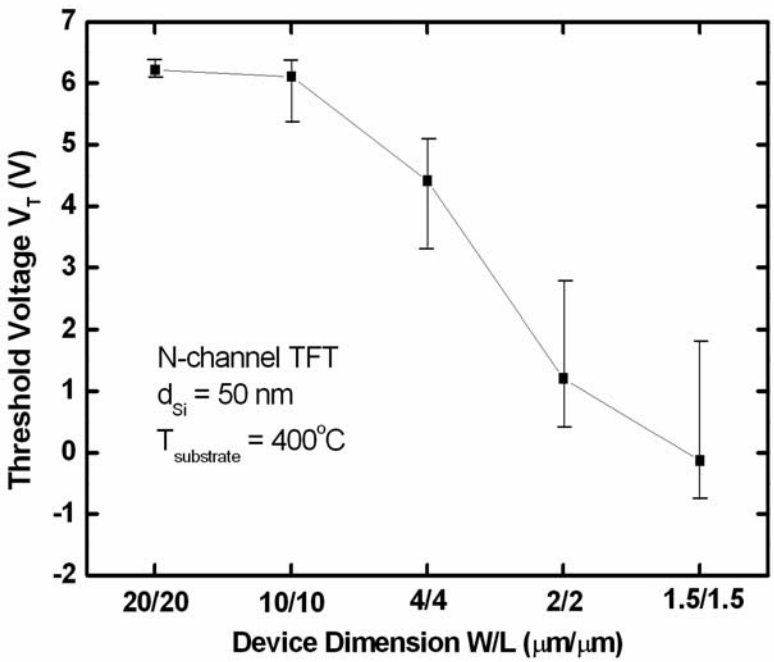


Fig. 2-13(b) Dependence of threshold voltage on device dimension of 50nm conventional ELC LTPS TFTs with substrate heating to 400ºC

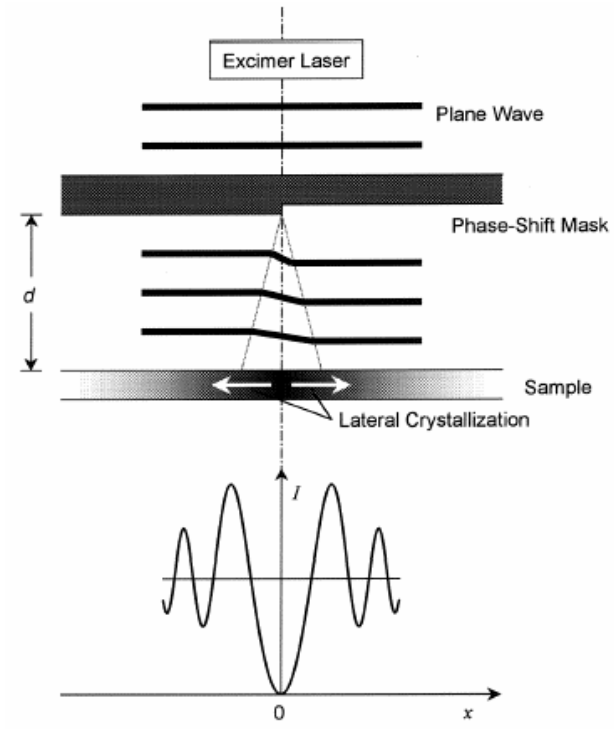


Fig. 2-14 The phase-modulated method

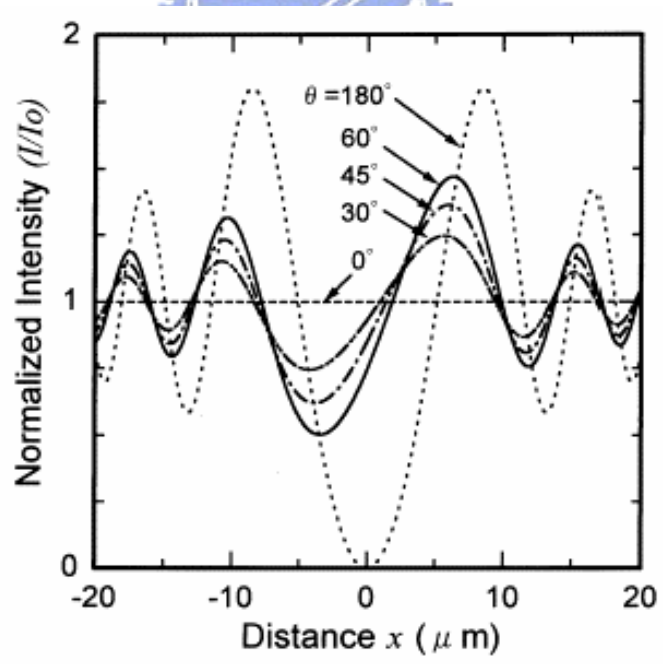


Fig. 2-15 The calculated intensity distribution as a function of the phase difference

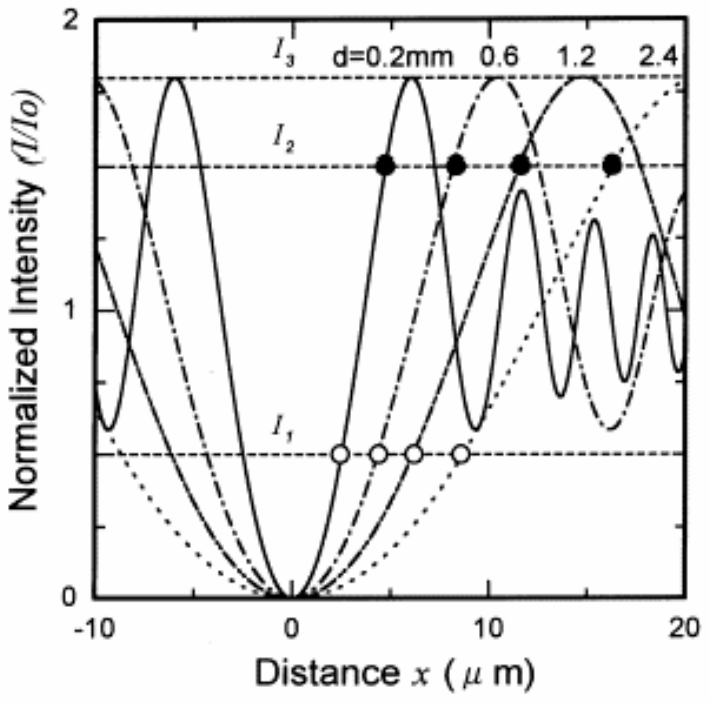


Fig. 2-16 The exhibition of the relationship between normalized intensity distributions and the distance from phase-shift mask to the sample

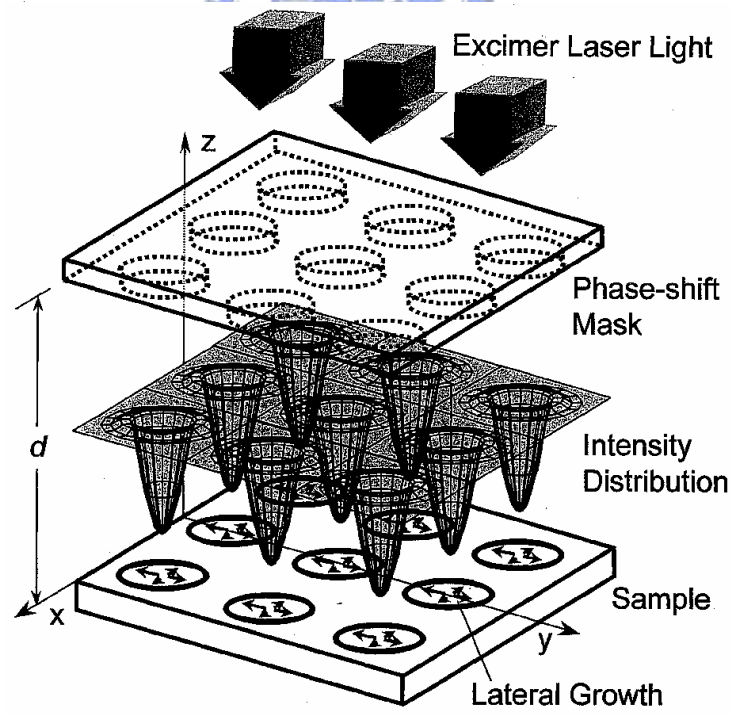


Fig. 2-17 The 2-D controlled grain growth by means of phase-shift mask

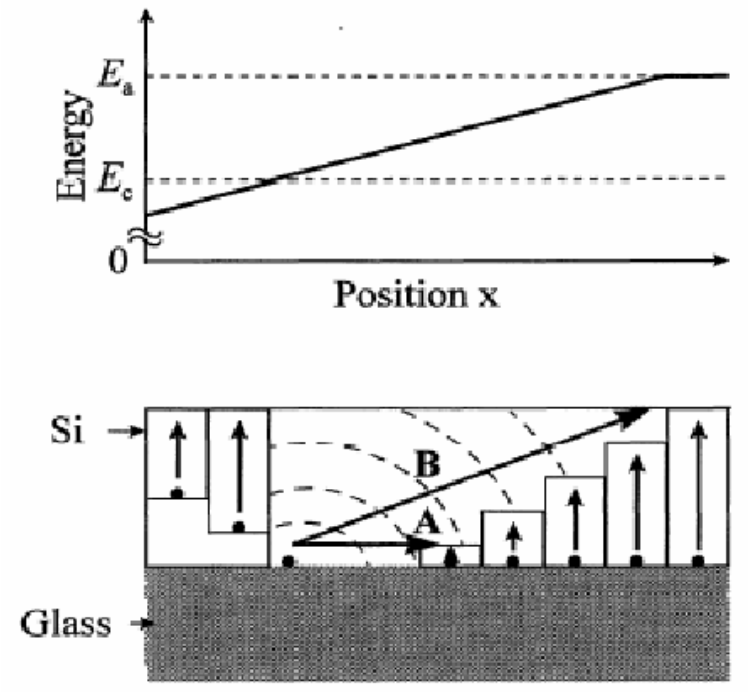


Fig. 2-18 The concept of large grain growth with graded excimer laser energy density

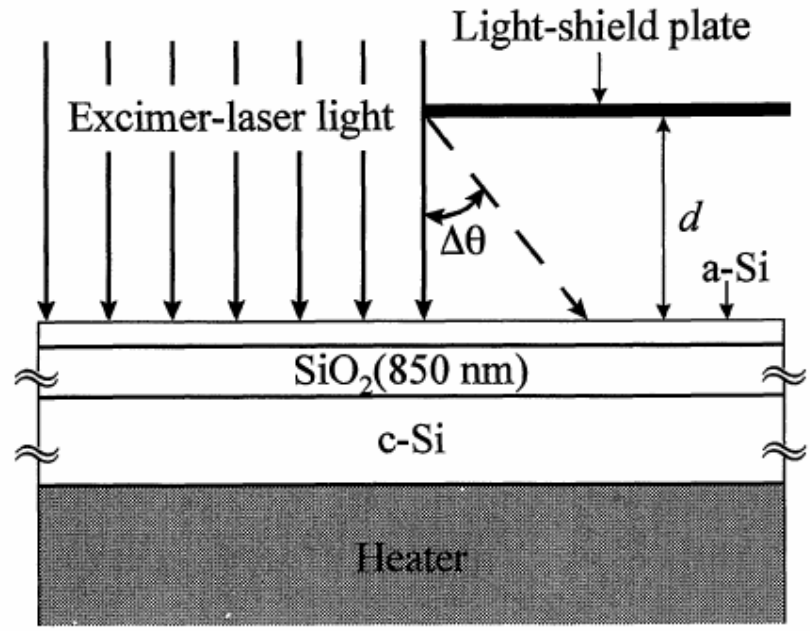


Fig. 2-19 The graded laser energy density resulted from the light-shield plate

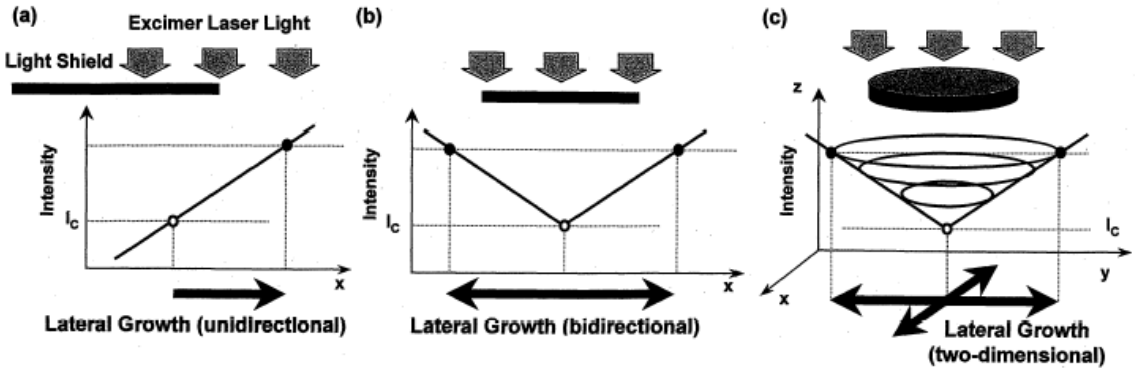
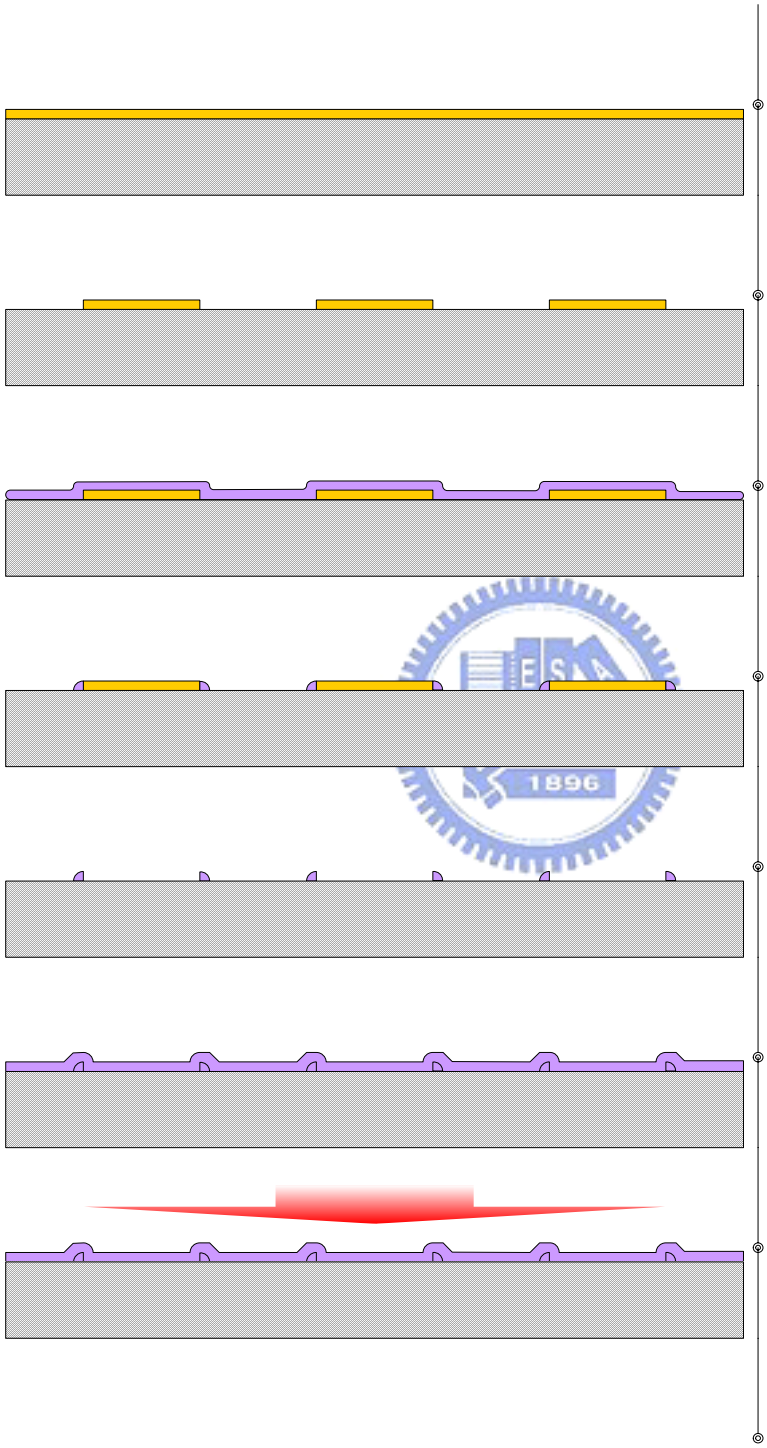


Fig. 2-20 The 2-D controlled grain growth by means of light-shield plate



Oxi

Fig. 3-1 Process flowchart of specimen preparation for material analysis

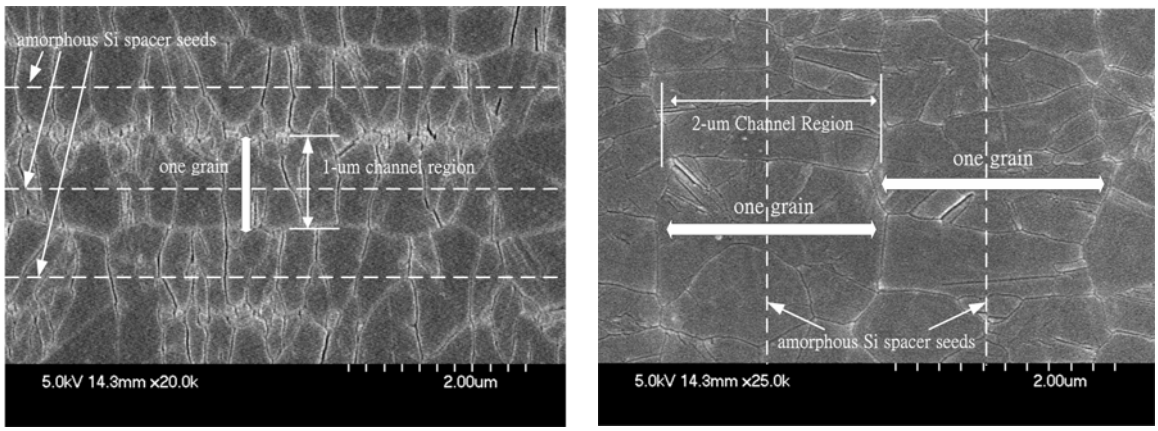


Fig. 3-2 SEM of ELC poly-Si thin film with 50nm height a-Si spacer structure

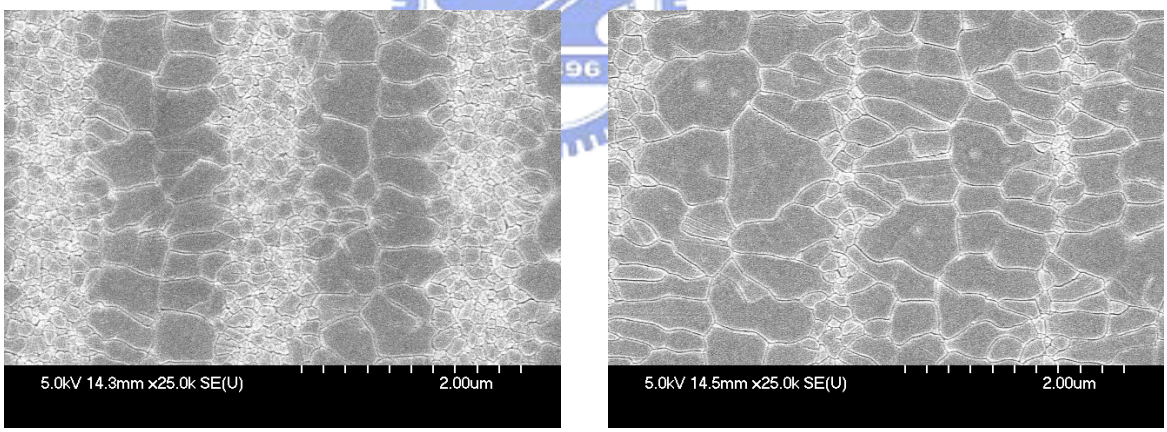


Fig. 3-3 SEM of ELC poly-Si thin film with 100nm height a-Si spacer structure

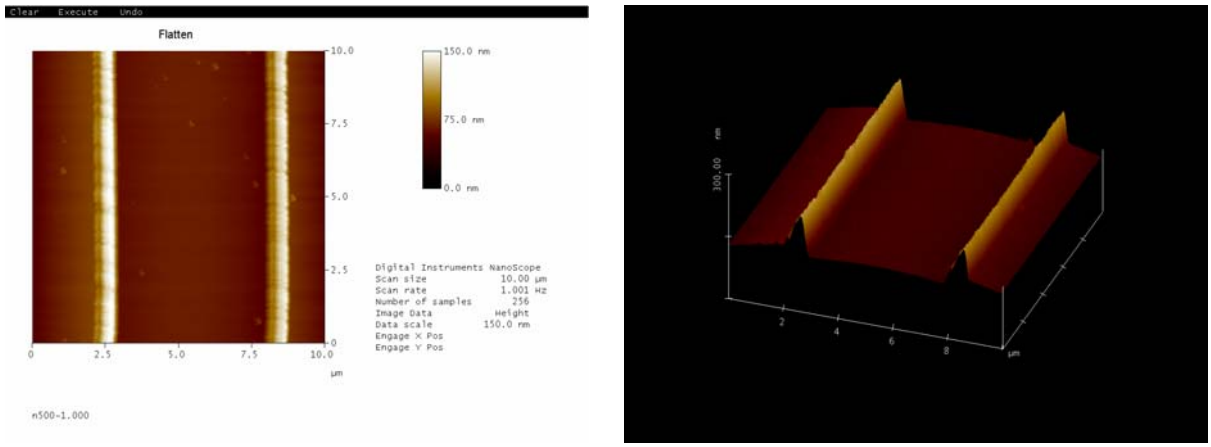


Fig. 3-4 AFM of 50nm height a-Si spacer structure

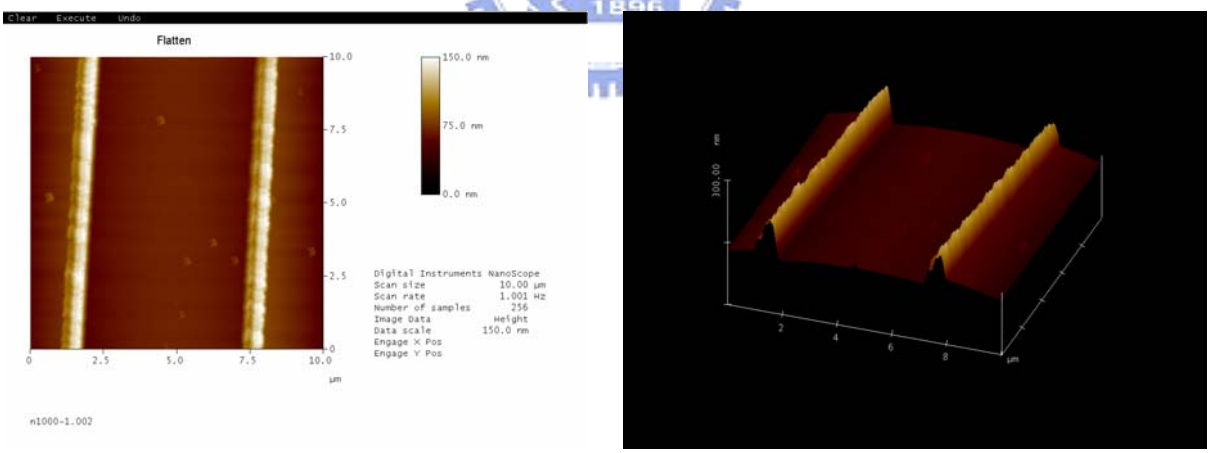


Fig. 3-5 AFM of 100nm height a-Si spacer structure

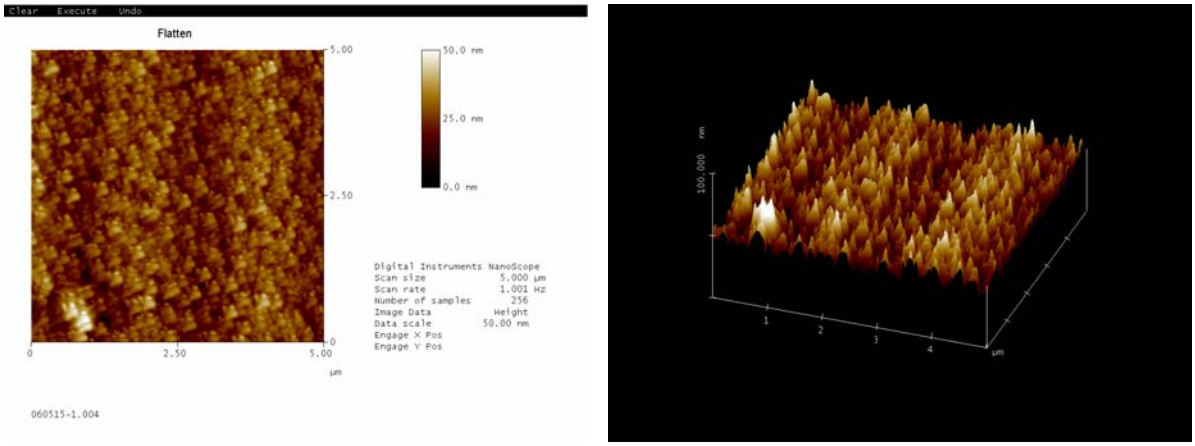


Fig. 3-6 AFM of ELC poly-Si thin film with 50nm height a-Si spacer structure

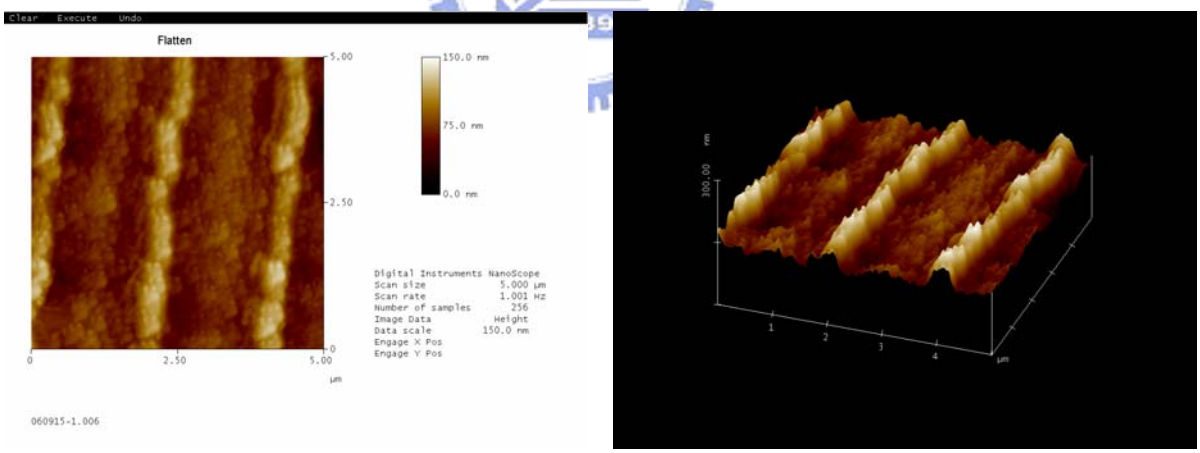


Fig. 3-7 AFM of ELC poly-Si thin film with 100nm height a-Si spacer structure

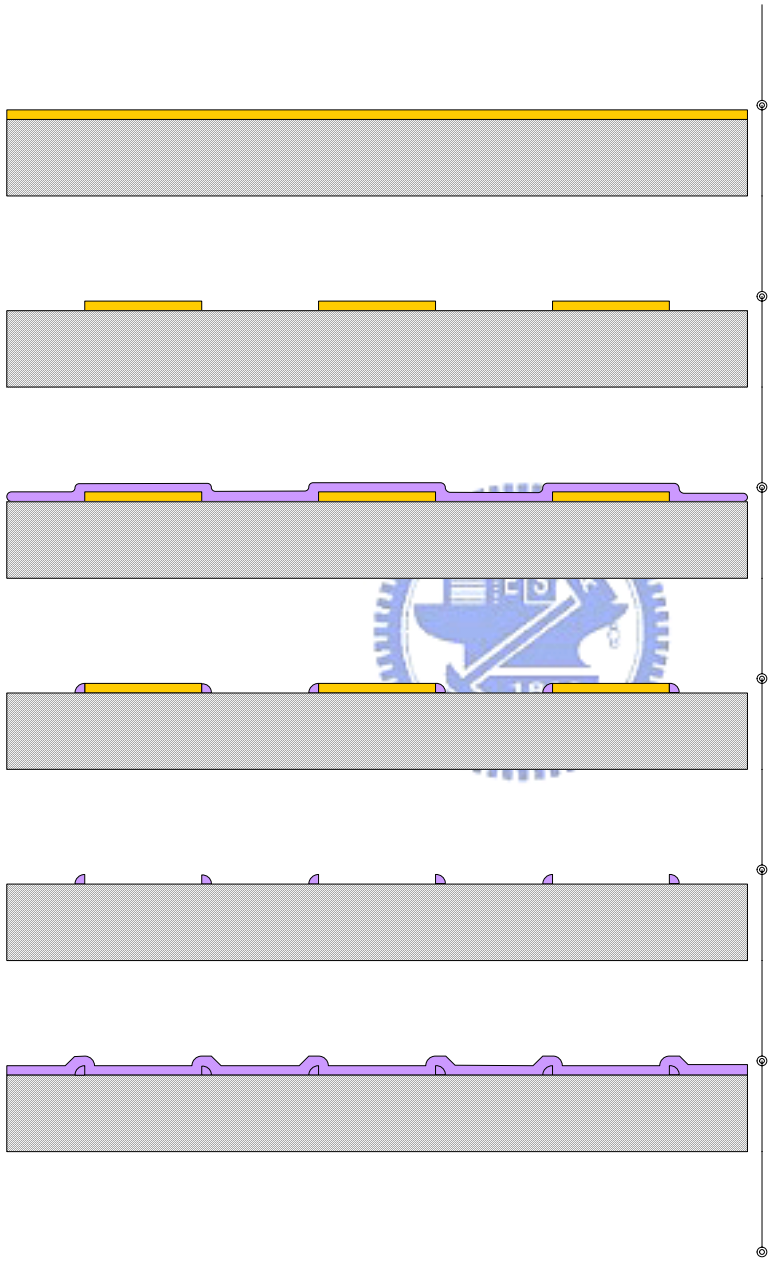


Fig. 4-1 Process flowchart of a-Si spacer structure with pre-patterned nitride layer

Ox

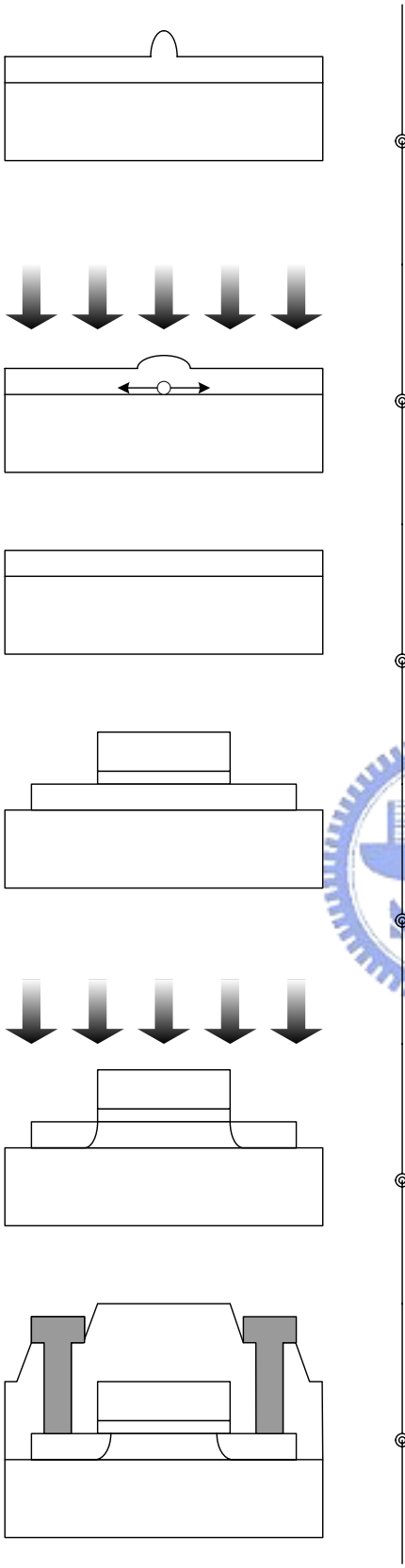


Fig. 4-2 Process flowchart of ELC poly-Si TFT with a-Si spacer structure

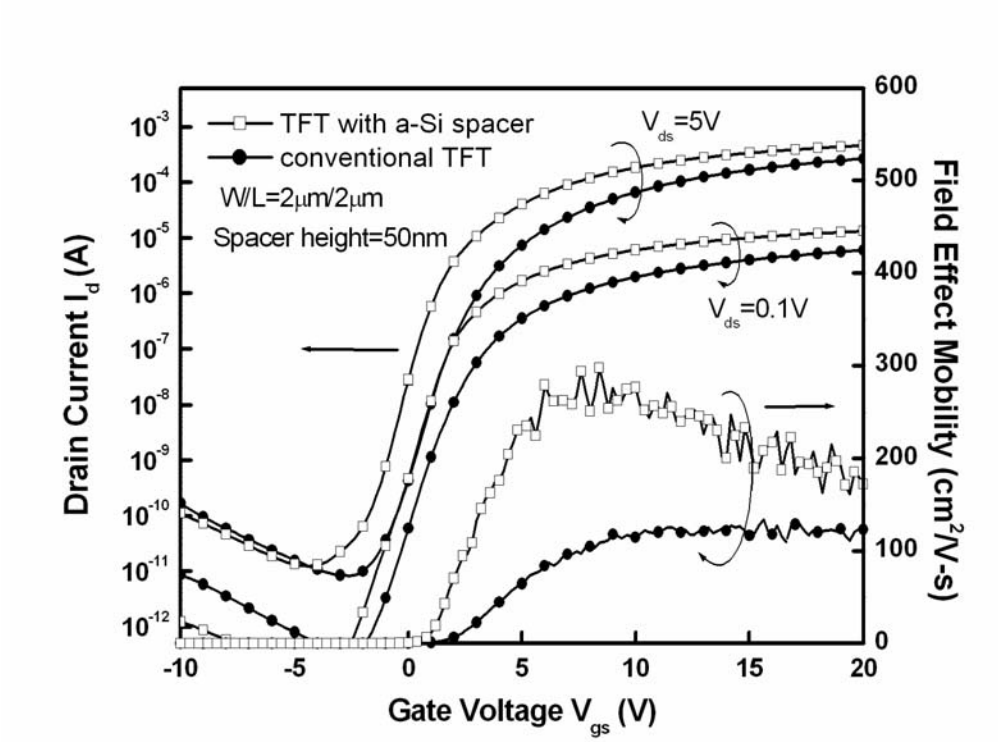


Fig. 4-3(a) Transfer characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=2μm/2μm and conventional counterpart

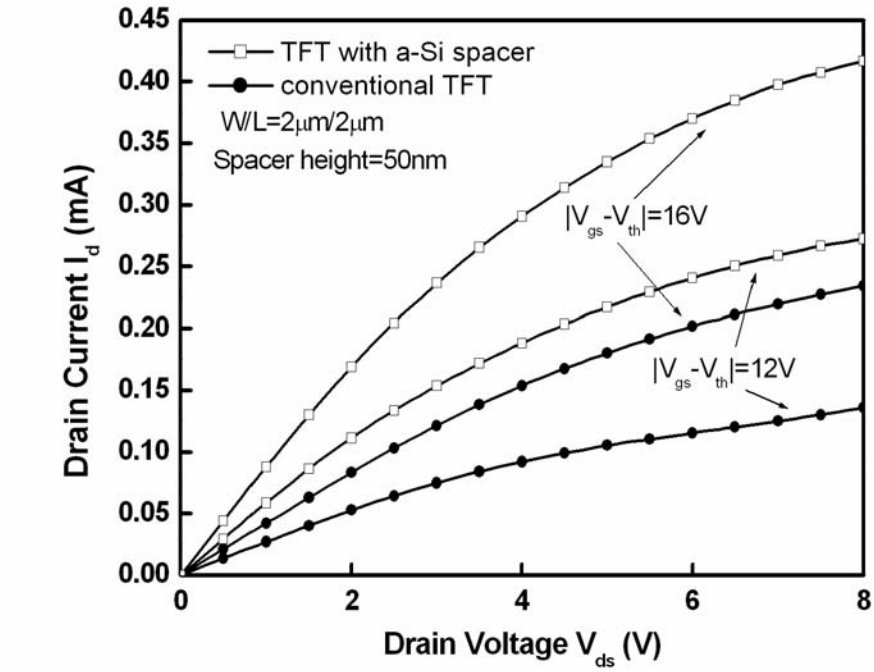


Fig. 4-3(b) Output characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=2μm/2μm and conventional counterpart

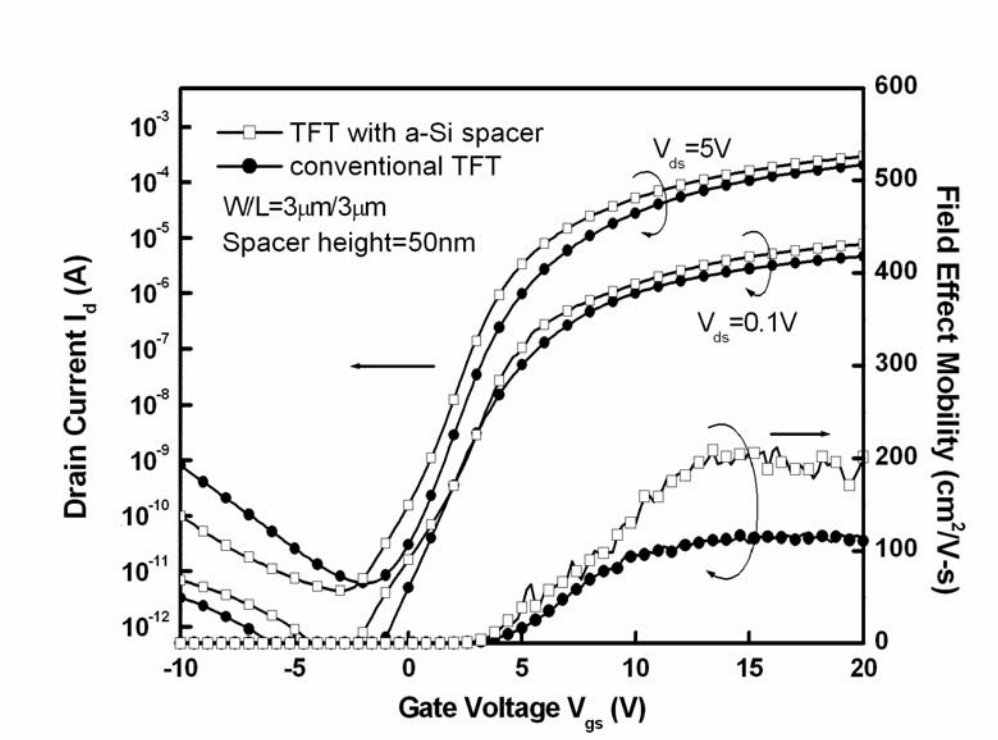


Fig. 4-4(a) Transfer characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=3μm/3μm and conventional counterpart

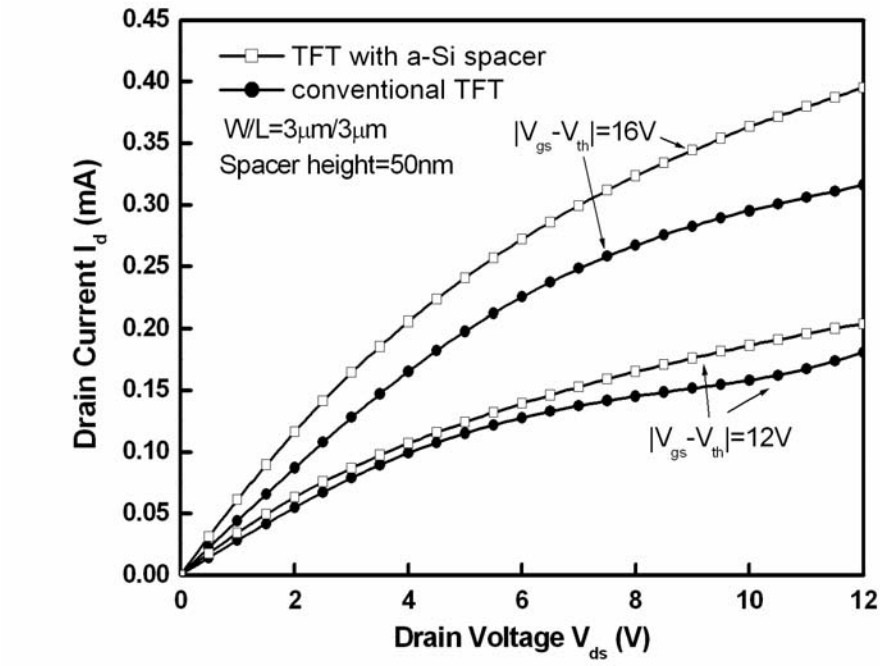


Fig. 4-4(b) Output characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=3μm/3μm and conventional counterpart

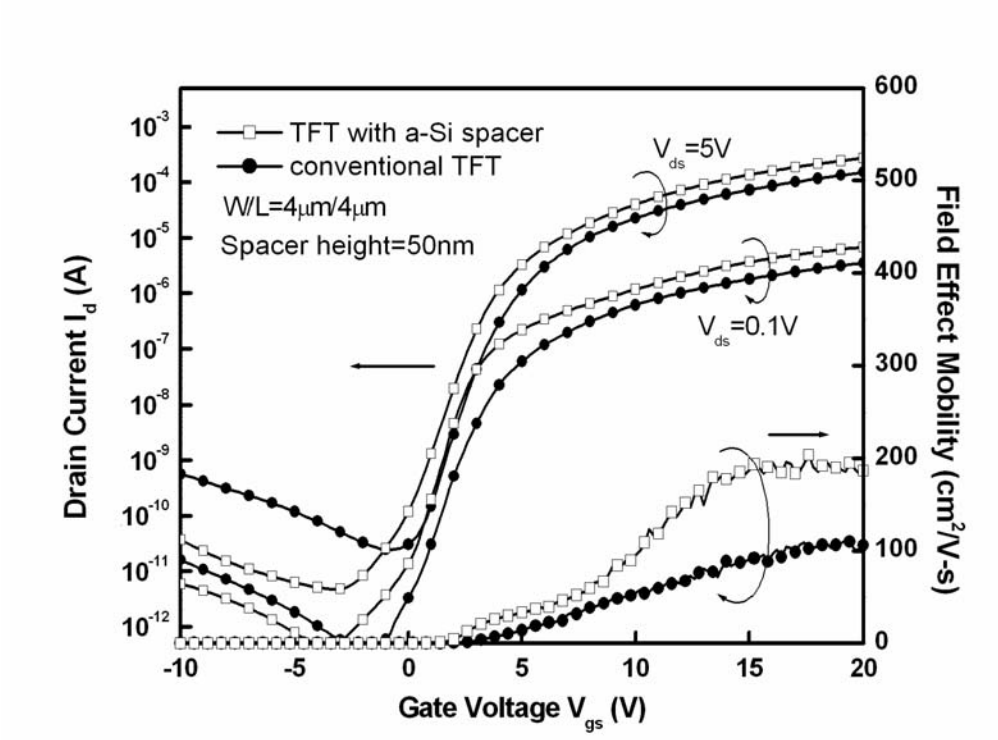


Fig. 4-5(a) Transfer characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=4μm/4μm and conventional counterpart

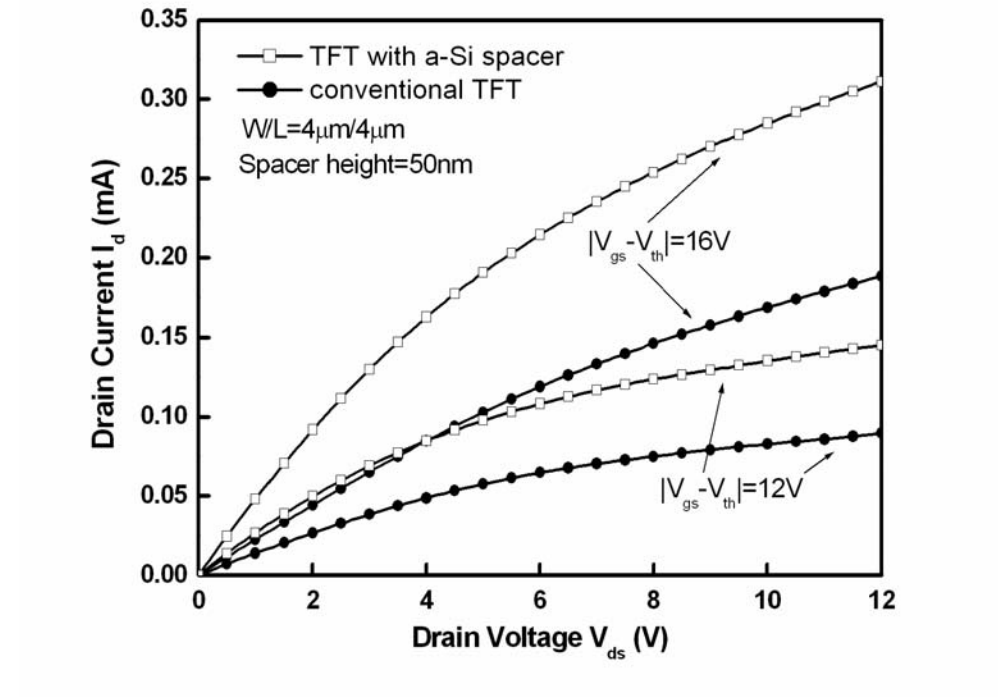


Fig. 4-5(b) Output characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=4μm/4μm and conventional counterpart

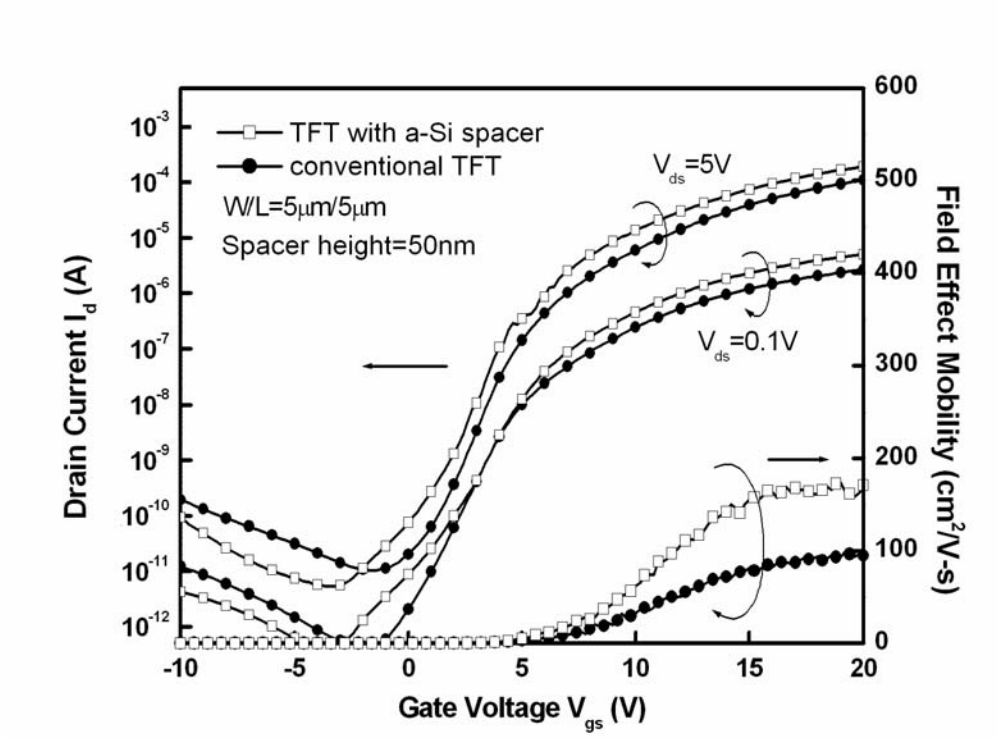


Fig. 4-6(a) Transfer characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=5μm/5μm and conventional counterpart

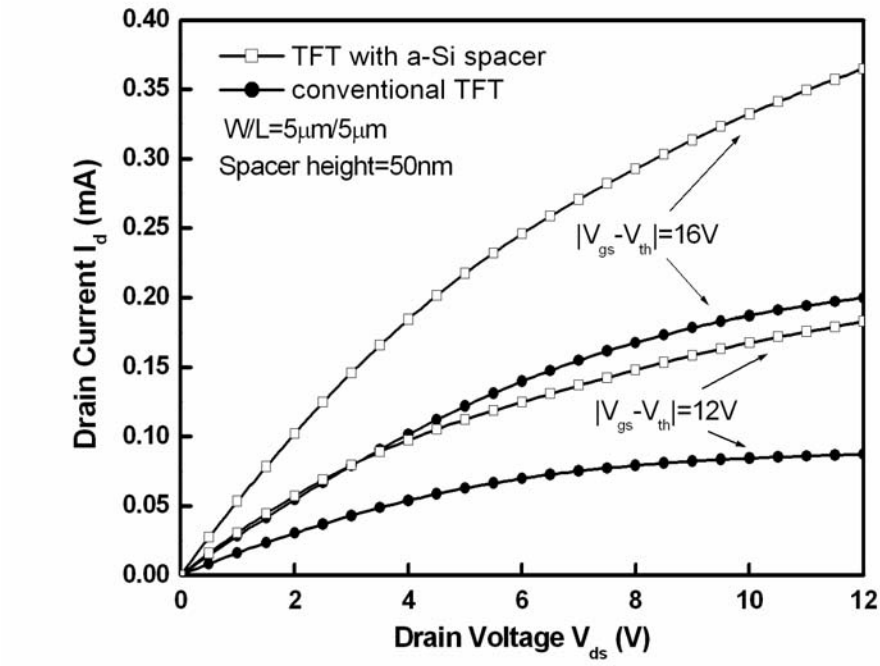


Fig. 4-6(b) Output characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=5μm/5μm and conventional counterpart

Table 4-1 Electrical characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for different device dimension and conventional counterpart

	V_{th} (V)	Mobility (cm^2/V-s)	Sub-threshold Swing (mV/dec)	On/Off current ratio
Conventional TFT (W=L=1.5um)	-0.652	155	1072	$1.68x10^6$
TFT with Si spacer (W=L=1.5um)	-0.438	**302**	807	$8.68x10^7$
Conventional TFT (W=L=2um)	1.94	128	738	$3.32x10^7$
TFT with Si spacer (W=L=2um)	0.976	**289**	672	$3.68x10^7$
Conventional TFT (W=L=3um)	3.72	116	1010	$3.41x10^7$
TFT with Si spacer (W=L=3um)	3.53	**206**	944	$6.81x10^7$
Conventional TFT (W=L=4um)	3.44	108	779	$6.23x10^6$
TFT with Si spacer (W=L=4um)	2.29	**198**	704	$5.73x10^7$
Conventional TFT (W=L=5um)	4.99	97	1170	$1.04x10^7$
TFT with Si spacer (W=L=5um)	4.84	**169**	1170	$3.6x10^7$

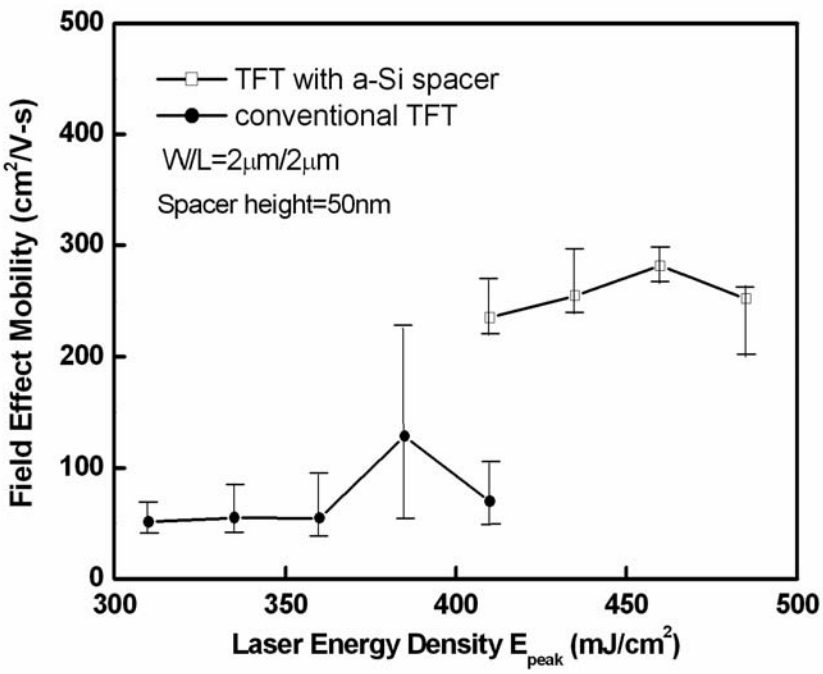


Fig. 4-7 Dependence of field effect mobility on laser energy density of ELC poly-Si TFT with 50nm height a-Si spacer structure for W/L=2μm/2μm and conventional counterpart

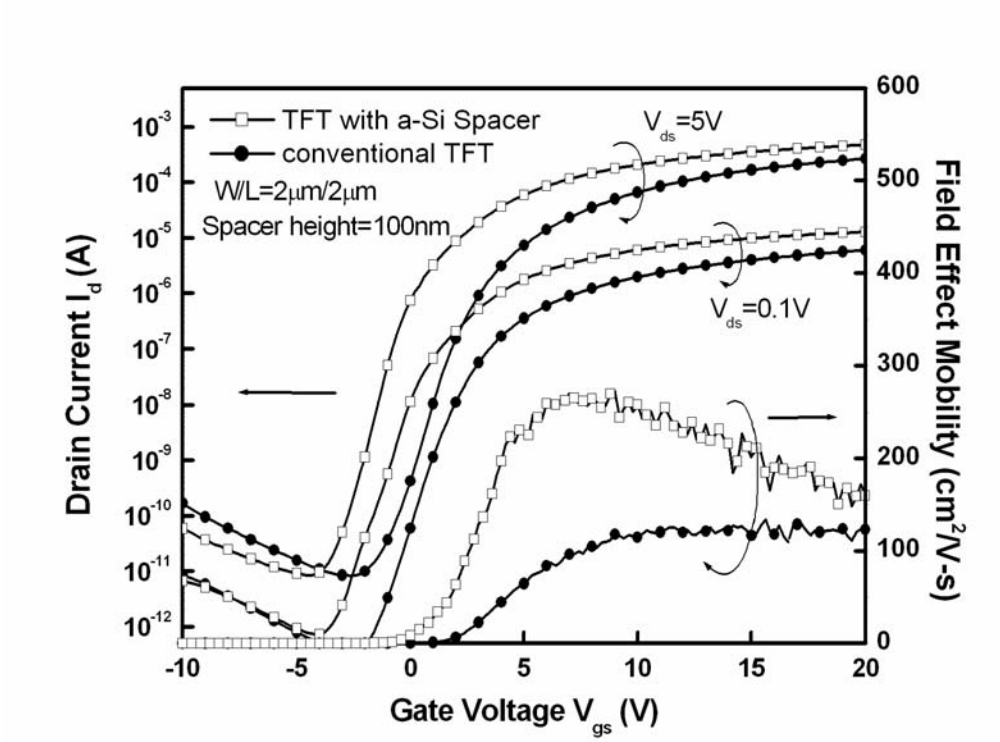


Fig. 4-8(a) Transfer characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for W/L=2μm/2μm and conventional counterpart

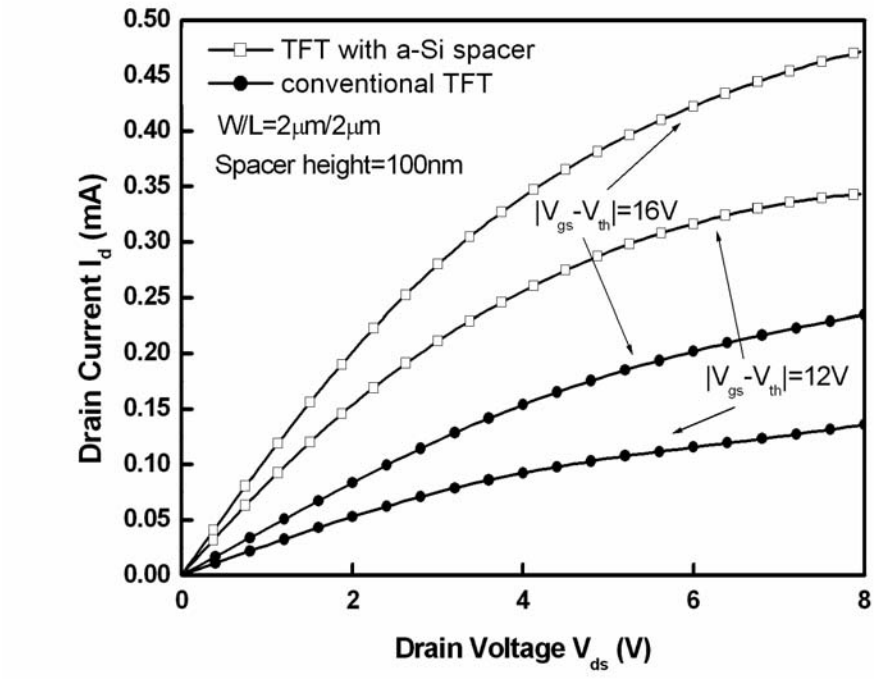


Fig. 4-8(b) Output characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for W/L=2μm/2μm and conventional counterpart

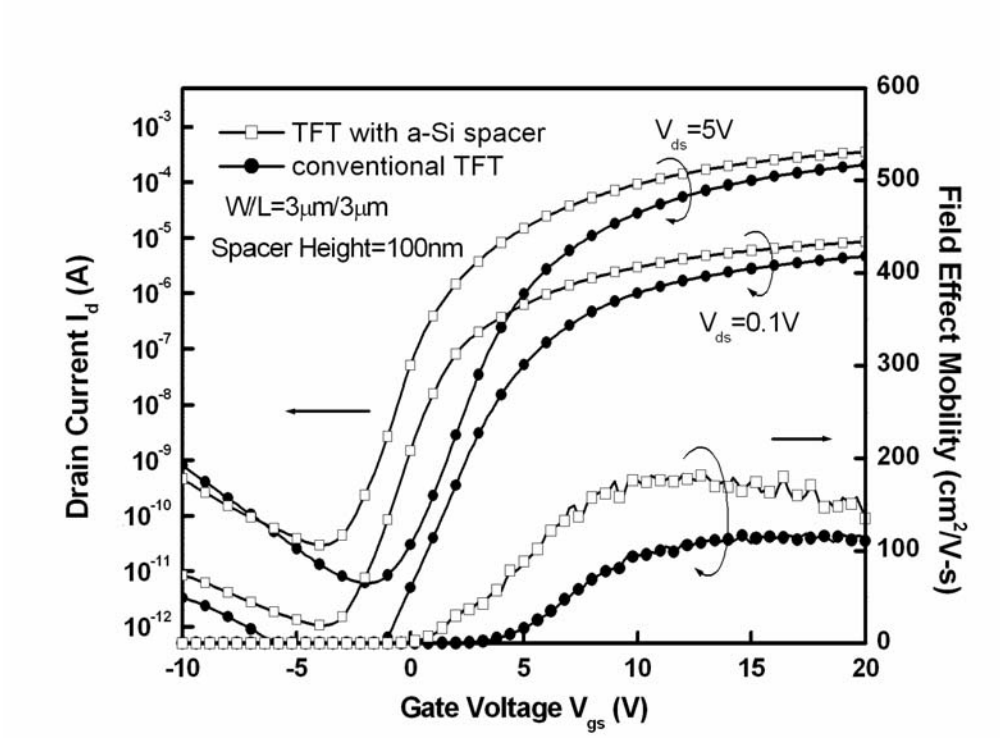


Fig. 4-9(a) Transfer characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for W/L=3μm/3μm and conventional counterpart

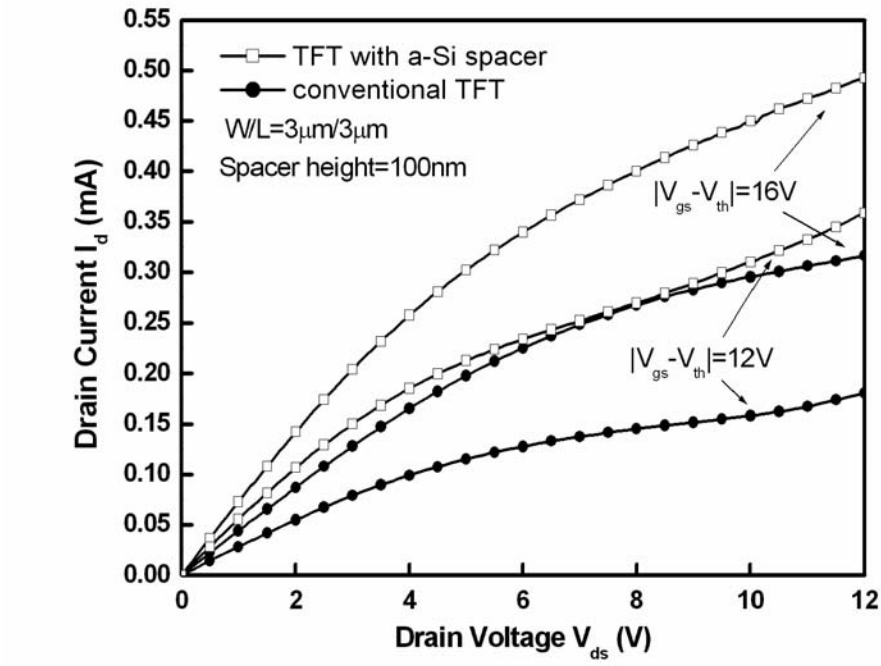


Fig. 4-9(b) Output characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for W/L=3μm/3μm and conventional counterpart

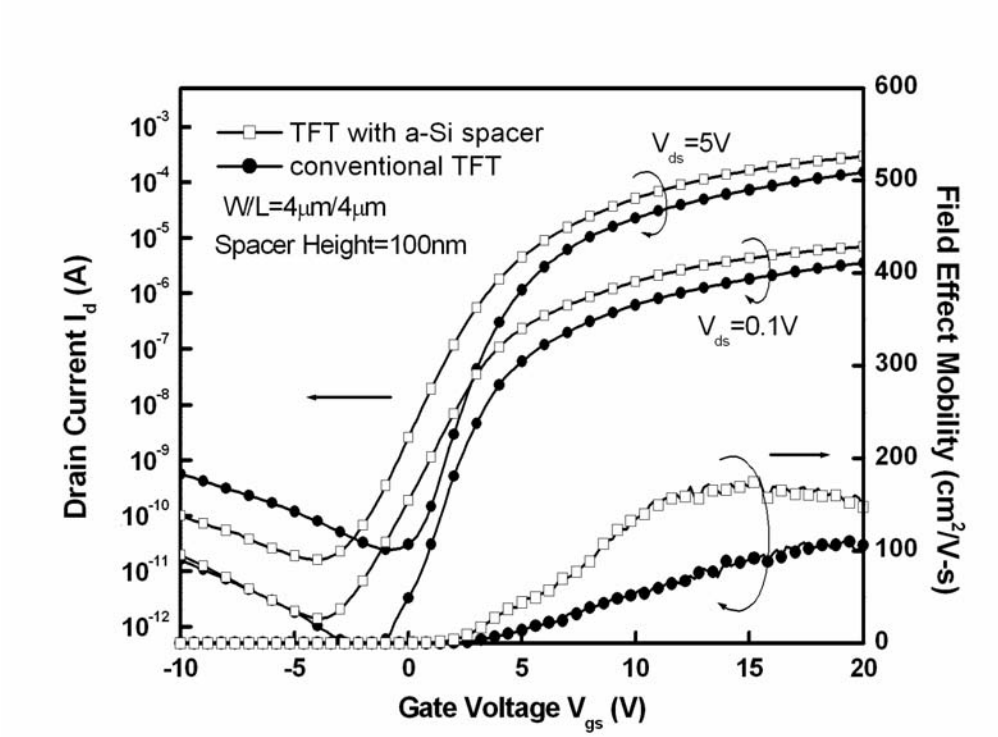


Fig. 4-10(a) Transfer characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for W/L=4μm/4μm and conventional counterpart

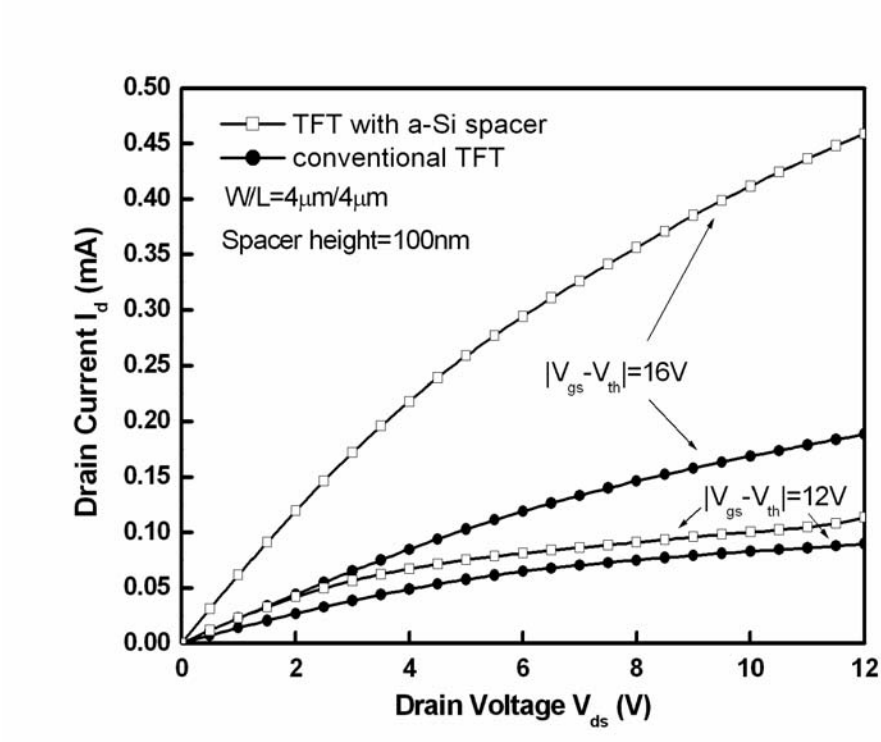


Fig. 4-10(b) Output characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for W/L=4μm/4μm and conventional counterpart

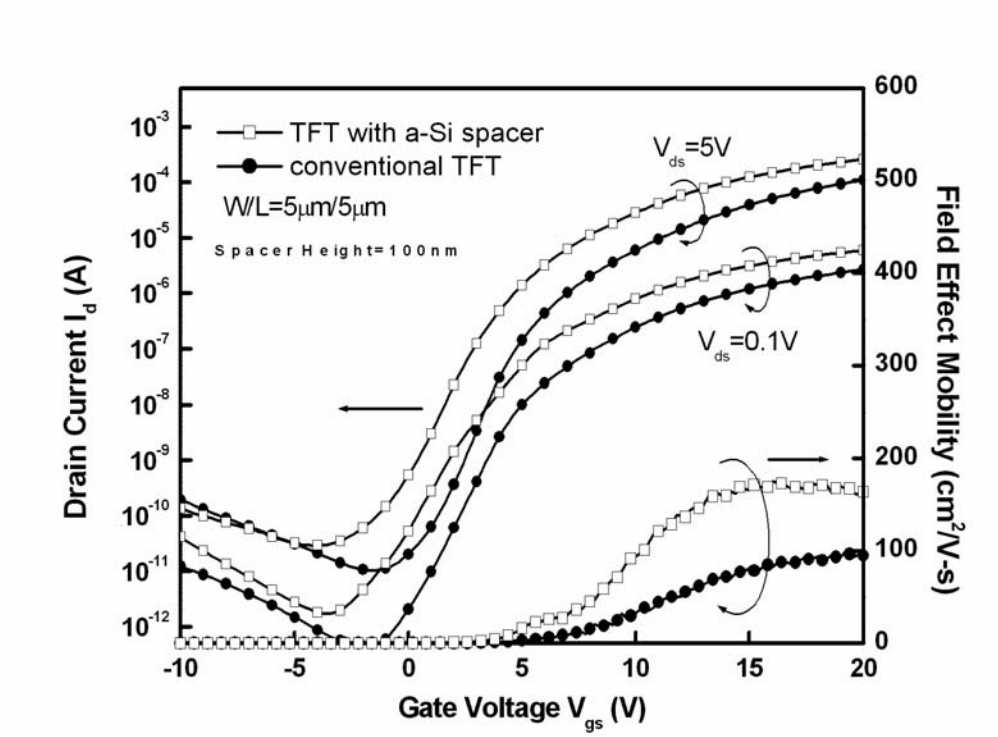


Fig. 4-11(a) Transfer characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for W/L=5μm/5μm and conventional counterpart

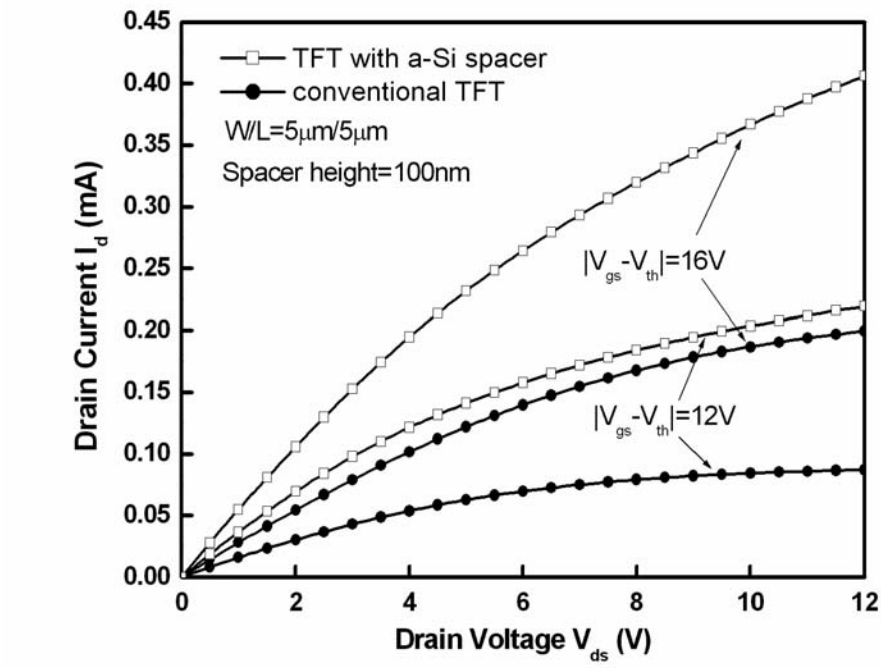


Fig. 4-11(b) Output characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for W/L=5μm/5μm and conventional counterpart

Table 4-2 Electrical characteristics of ELC poly-Si TFT with 100nm height a-Si spacer structure for different device dimension and conventional counterpart

	V_{th} (V)	Mobility (cm^2/V-s)	Sub-threshold Swing (mV/dec)	On/Off current ratio
Conventional TFT (W=L=1.5um)	-0.652	155	1072	$1.68x10^6$
TFT with Si spacer (W=L=1.5um)	-0.246	**258**	546	$2.25x10^7$
Conventional TFT (W=L=2um)	1.94	128	738	$3.32x10^7$
TFT with Si spacer (W=L=2um)	-0.051	**265**	713	$5.59x10^7$
Conventional TFT (W=L=3um)	3.72	116	1010	$3.41x10^7$
TFT with Si spacer (W=L=3um)	0.787	**189**	786	$1.20x10^7$
Conventional TFT (W=L=4um)	3.44	108	779	$6.23x10^6$
TFT with Si spacer (W=L=4um)	2.53	**174**	1247	$5.86x10^6$
Conventional TFT (W=L=5um)	4.99	97	1170	$1.04x10^7$
TFT with Si spacer (W=L=5um)	4.1	**170**	1442	$9.48x10^6$

Table 4-3 Electrical characteristics of ELC poly-Si TFT with 50nm and 100nm height a-Si spacer structure for different device dimension

	V_{th} (V)	Mobility (cm^2/V-s)	Sub-threshold Swing (mV/dec)	On/Off current ratio
Nitride = 500Å (W=L=1.5um)	-0.438	**302**	807	$8.68x10^7$
Nitride = 1000Å (W=L=1.5um)	-0.246	**258**	546	$2.25x10^7$
Nitride = 500Å (W=L=2um)	0.976	**289**	672	$3.68x10^7$
Nitride = 1000Å (W=L=2um)	-0.051	**265**	713	$5.59x10^7$
Nitride = 500Å (W=L=3um)	3.53	**206**	944	$6.81x10^7$
Nitride = 1000Å (W=L=3um)	0.787	**189**	786	$1.20x10^7$
Nitride = 500Å (W=L=4um)	2.29	**198**	704	$5.73x10^7$
Nitride = 1000Å (W=L=4um)	2.53	**174**	1247	$5.86x10^6$
Nitride = 500Å (W=L=5um)	4.84	**169**	1170	$3.60x10^7$
Nitride = 1000Å (W=L=5um)	4.1	**170**	1442	$9.48x10^6$

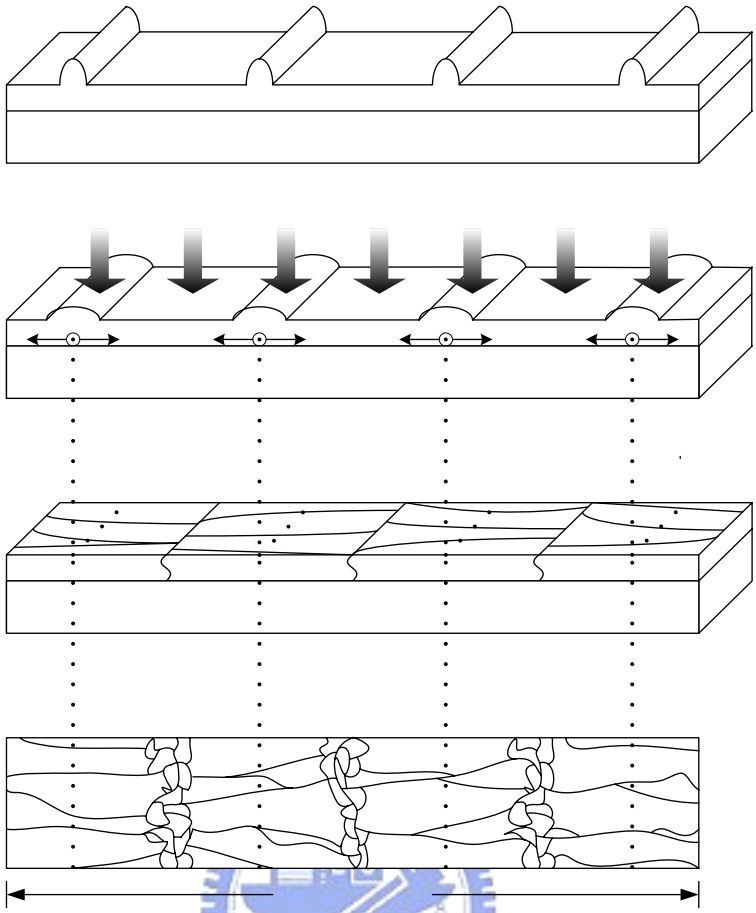


Fig. 4-12(a) The diagram of periodic grain growth for large dimension devices applications

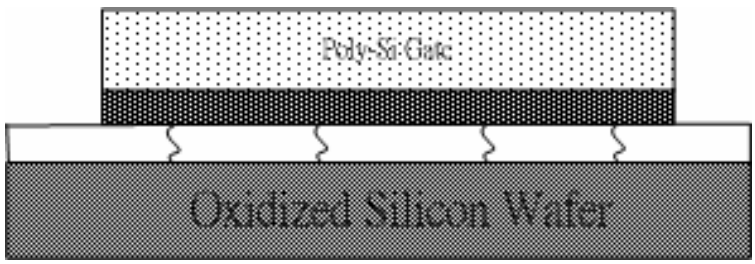


Fig. 4-12(b) The periodic grain growth for large dimension devices after gate electrode formation

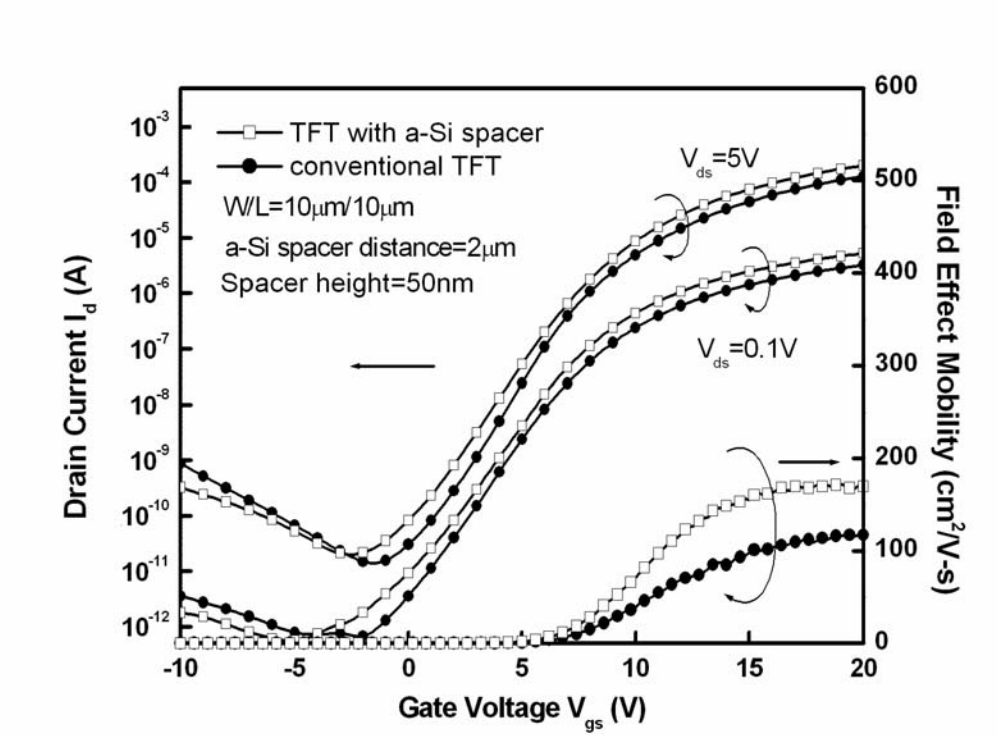


Fig. 4-13(a) Transfer characteristics of ELC poly-Si TFT with 50nm height and 2μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

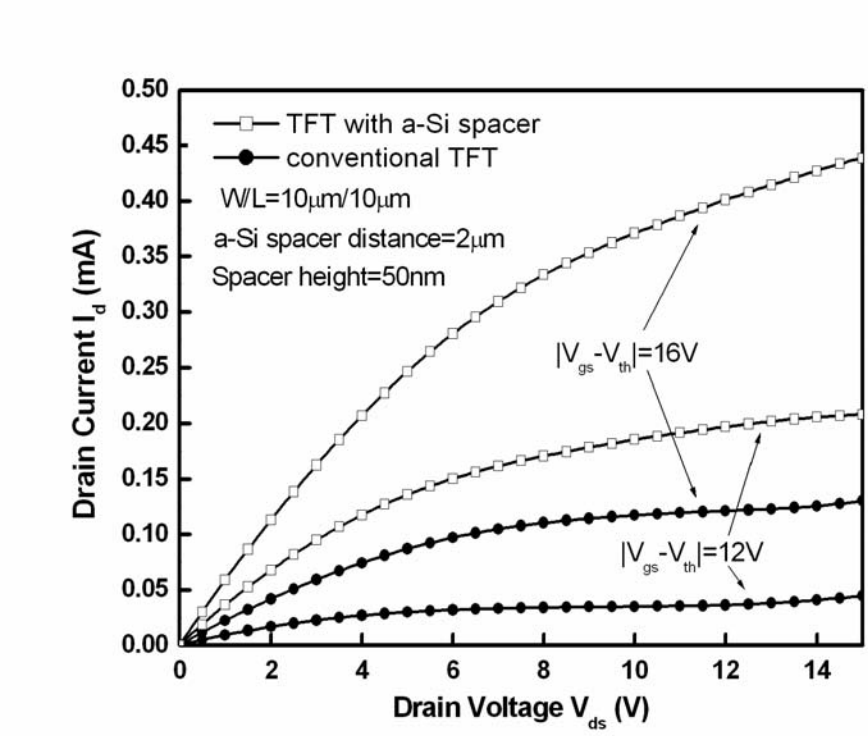


Fig. 4-13(b) Output characteristics of ELC poly-Si TFT with 50nm height and 2μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

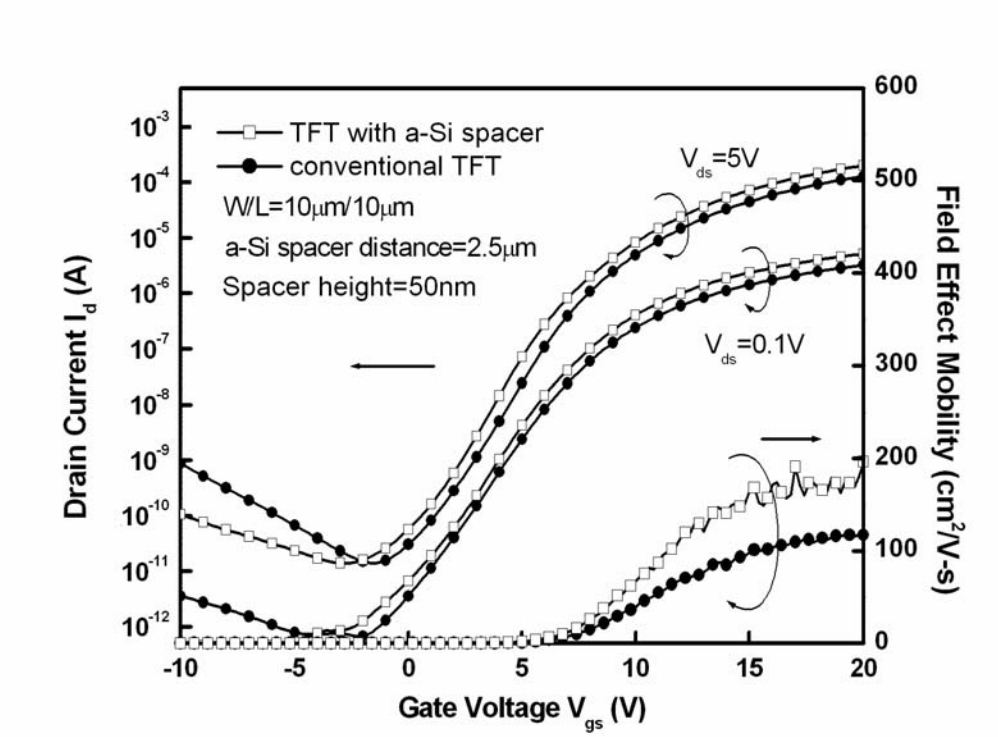


Fig. 4-14(a) Transfer characteristics of ELC poly-Si TFT with 50nm height and 2.5μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

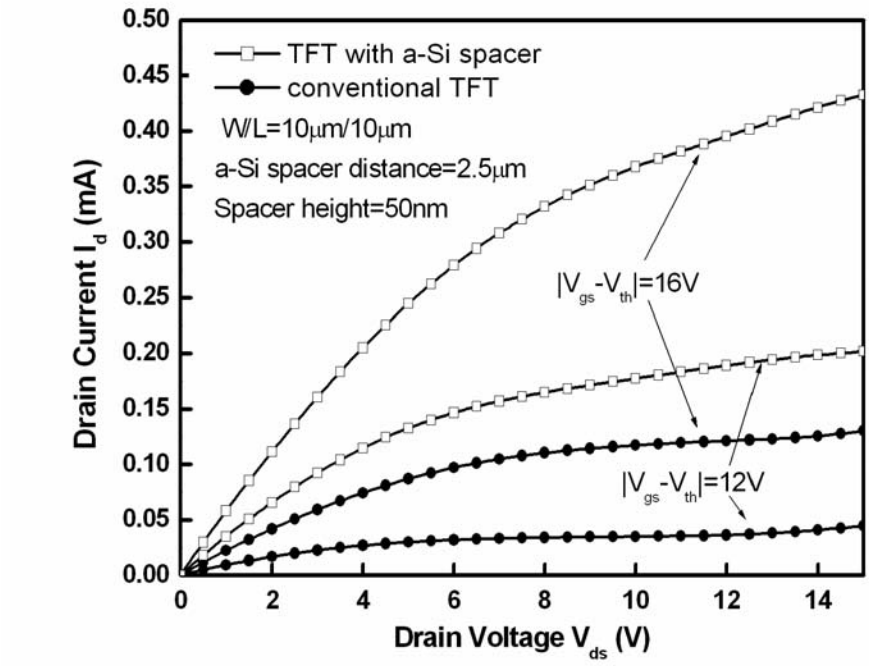


Fig. 4-14(b) Output characteristics of ELC poly-Si TFT with 50nm height and 2.5μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

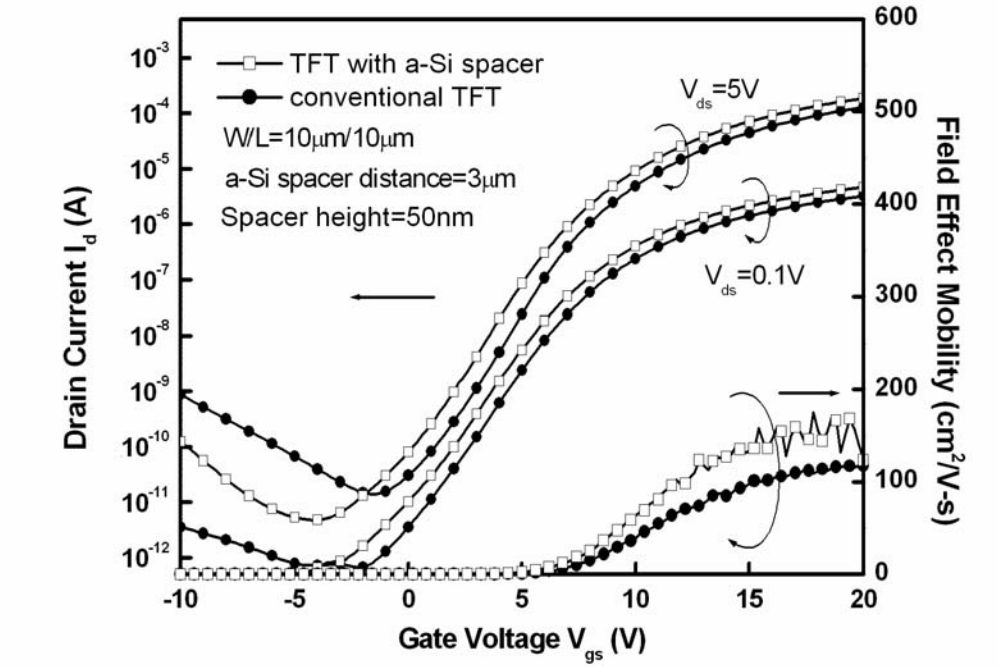


Fig. 4-15(a) Transfer characteristics of ELC poly-Si TFT with 50nm height and 3μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

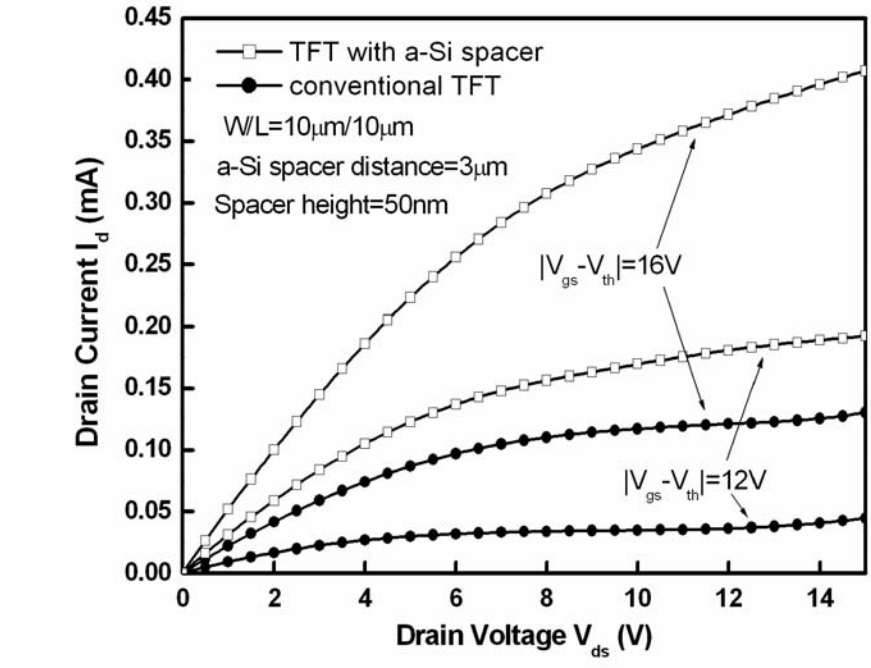


Fig. 4-15(b) Output characteristics of ELC poly-Si TFT with 50nm height and 3μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

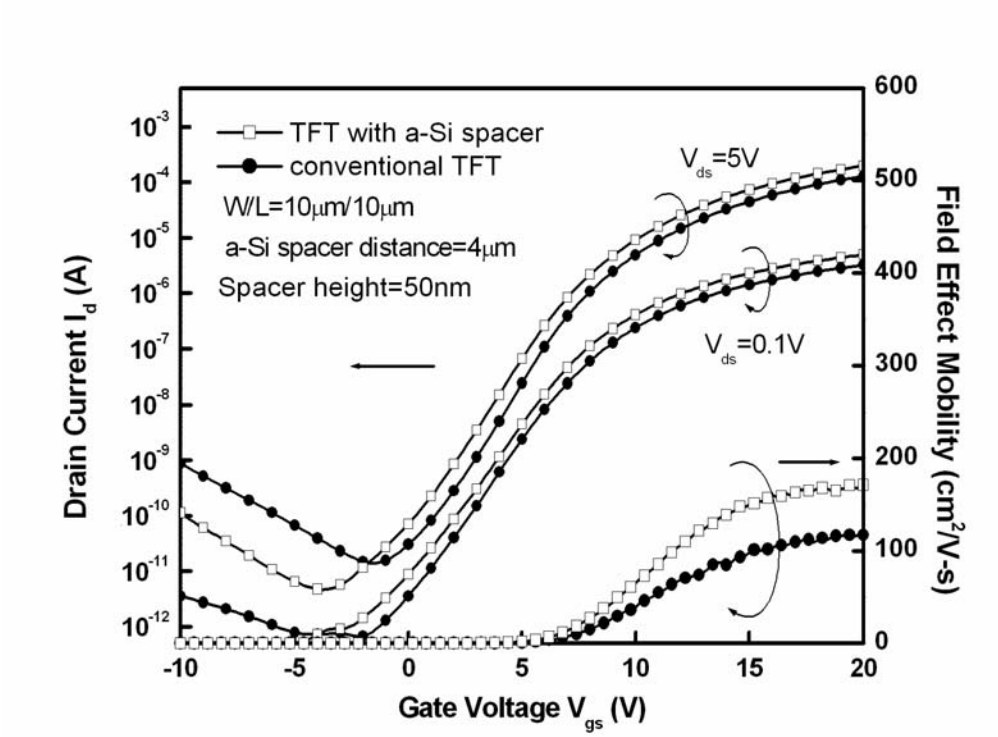


Fig. 4-16(a) Transfer characteristics of ELC poly-Si TFT with 50nm height and 4μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

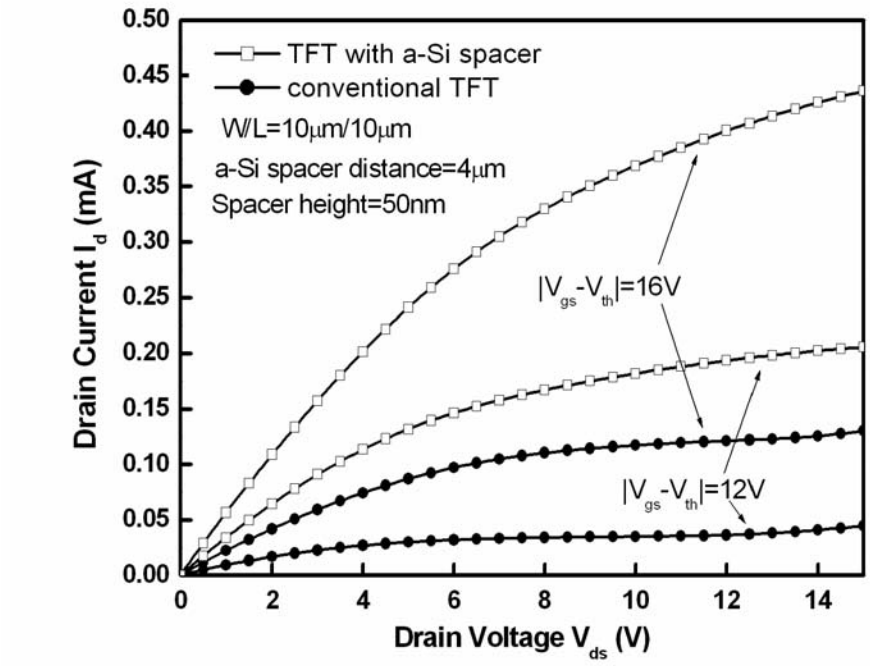


Fig. 4-16(b) Output characteristics of ELC poly-Si TFT with 50nm height and 4μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

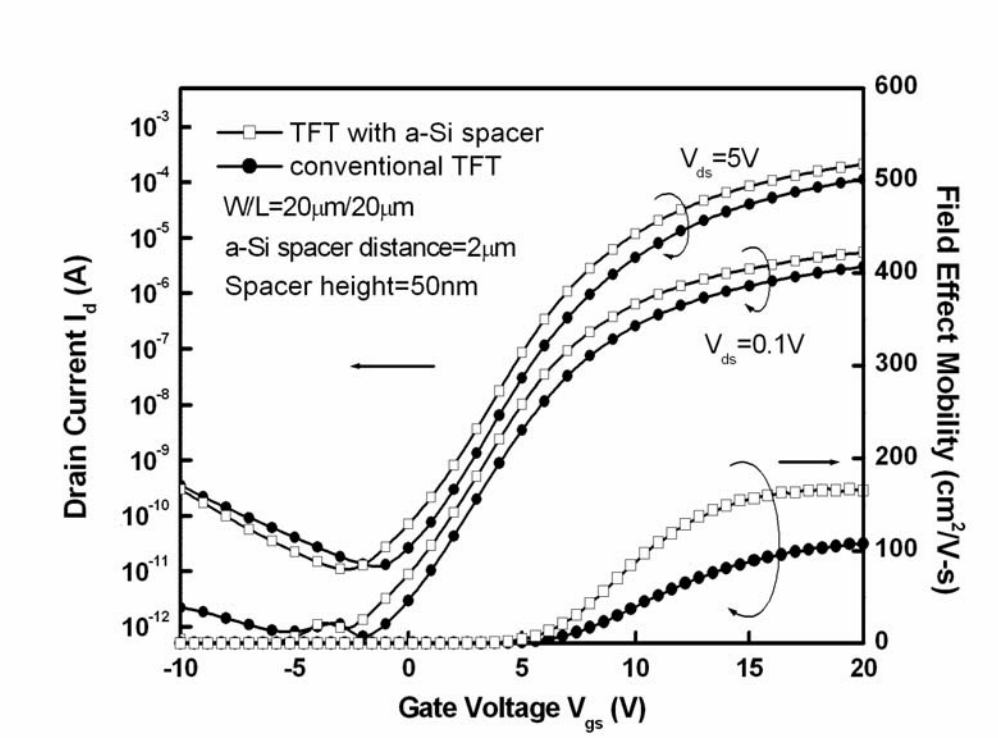


Fig. 4-17(a) Transfer characteristics of ELC poly-Si TFT with 50nm height and 2μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

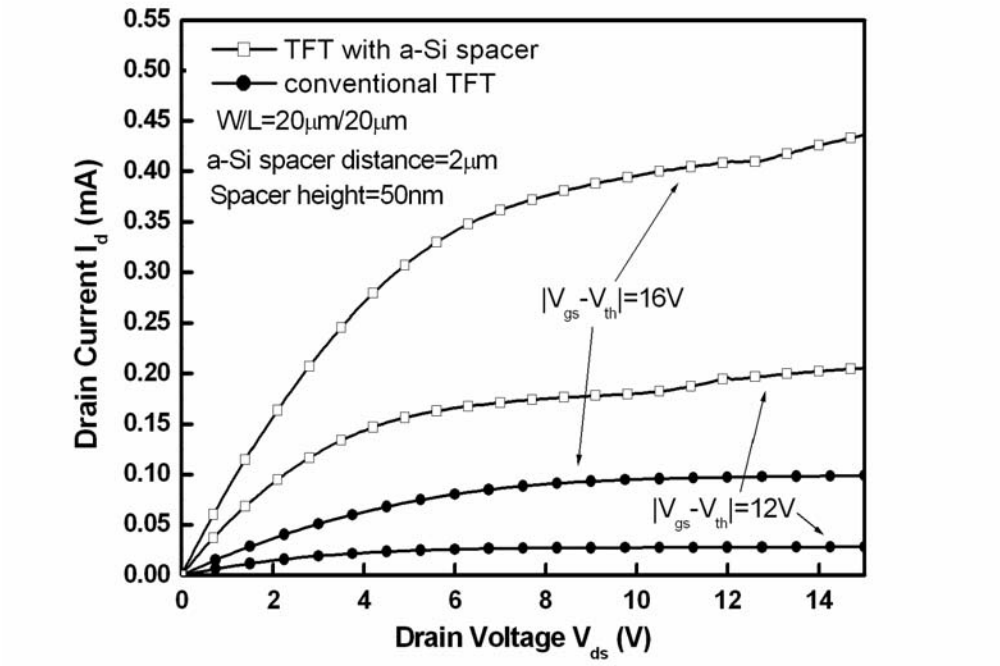


Fig. 4-17(b) Output characteristics of ELC poly-Si TFT with 50nm height and 2μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

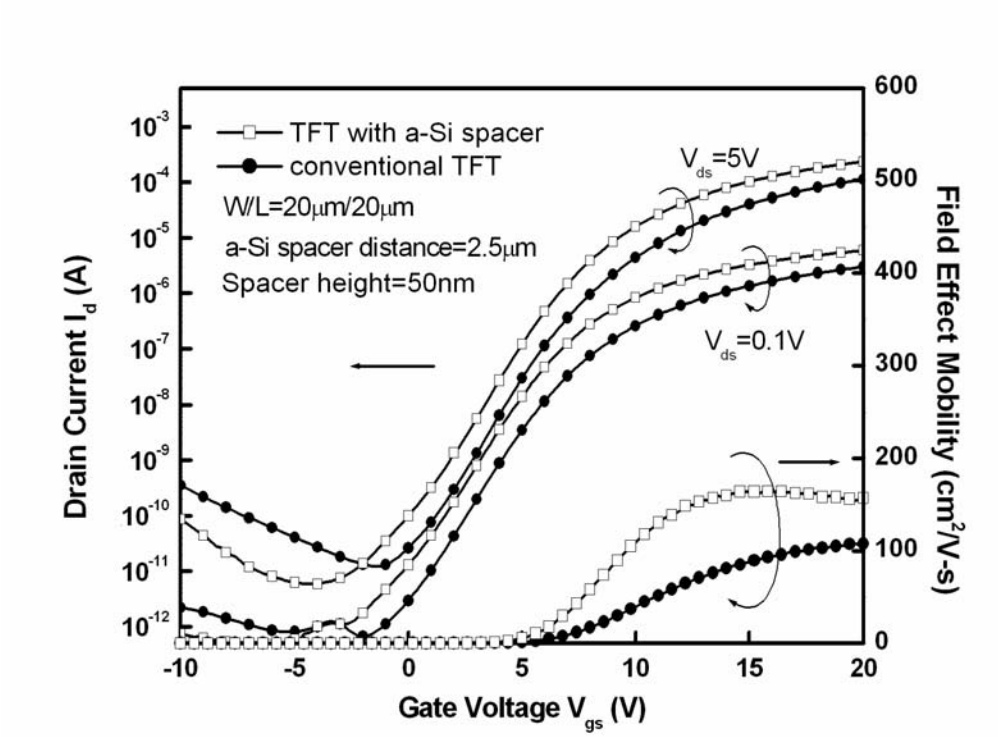


Fig. 4-18(a) Transfer characteristics of ELC poly-Si TFT with 50nm height and 2.5μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

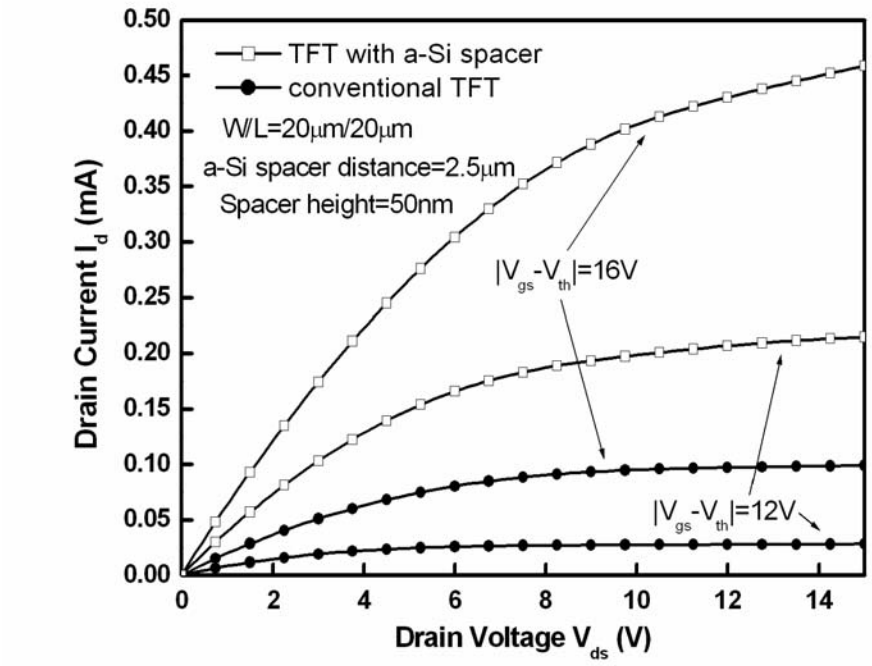


Fig. 4-18(b) Output characteristics of ELC poly-Si TFT with 50nm height and 2.5μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

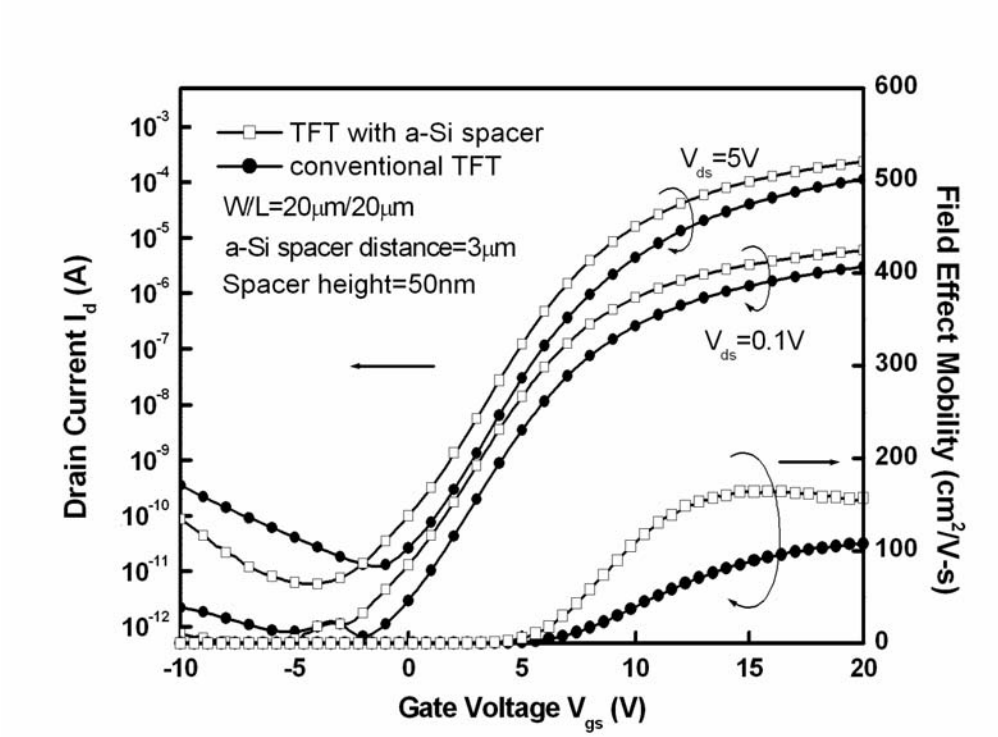


Fig. 4-19(a) Transfer characteristics of ELC poly-Si TFT with 50nm height and 3μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

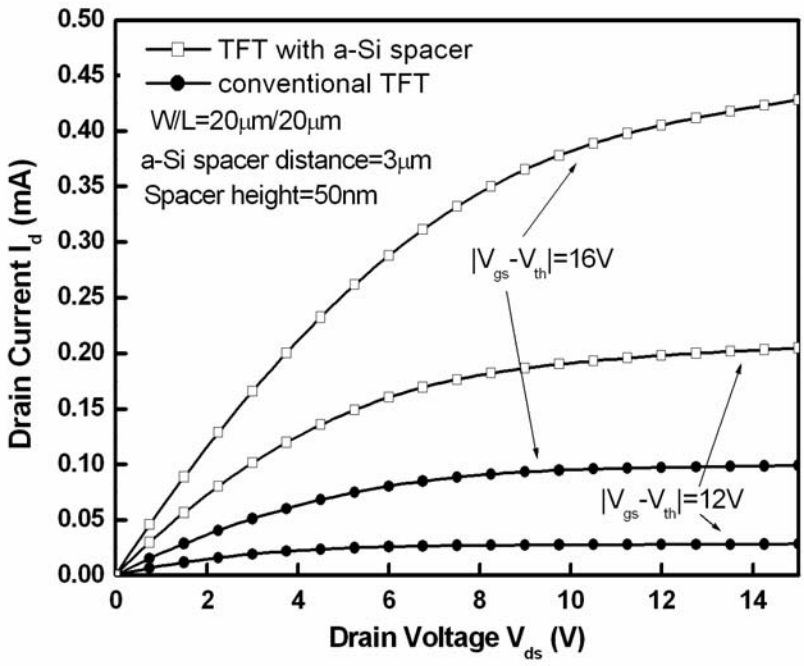


Fig. 4-19(b) Output characteristics of ELC poly-Si TFT with 50nm height and 3μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

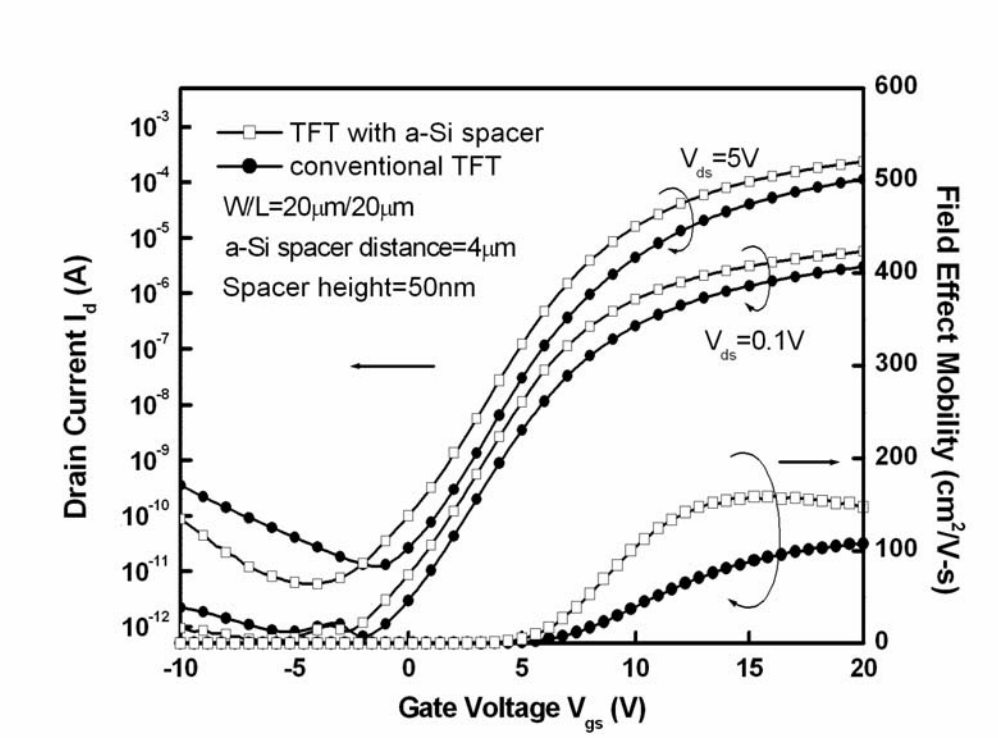


Fig. 4-20(a) Transfer characteristics of ELC poly-Si TFT with 50nm height and 4μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

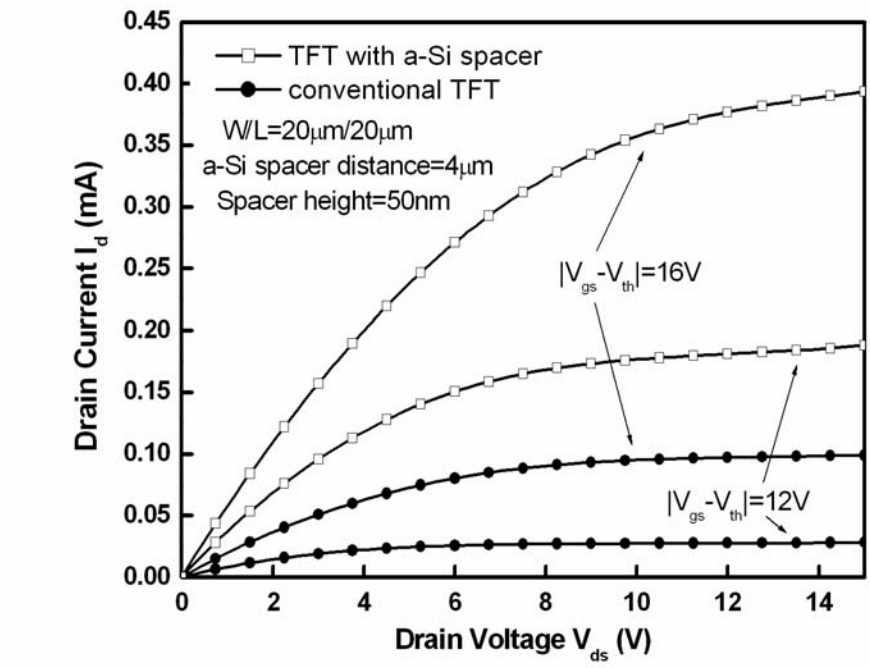


Fig. 4-20(b) Output characteristics of ELC poly-Si TFT with 50nm height and 4μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

Table 4-4 Electrical characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure and W/L=10μm/10μm for different a-Si spacer distance and conventional counterpart

	V_{th} (V)	Mobility (cm^2/V-s)	Sub-threshold Swing (V/dec)	On/Off current ratio
Conventional TFT	6.16	114	1.612	$9.27x10^6$
Spacer distance = 1um	5.88	**141**	1.68	$2.49x10^7$
Spacer distance = 1.5um	5.44	**147**	1.64	$2.39x10^7$
Spacer distance = 2um	5.66	**167**	1.71	$1.01x10^7$
Spacer distance = 2.5um	5.68	**191**	1.52	$1.43x10^7$
Spacer distance = 3um	5.49	**170**	1.61	$3.82x10^7$
Spacer distance = 4um	5.64	**167**	1.67	$4.27x10^7$

Table 4-5 Electrical characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure and W/L=20μm/20μm for different a-Si spacer distance and conventional counterpart

	V_{th} (V)	Mobility (cm^2/V-s)	Sub-threshold Swing (V/dec)	On/Off current ratio
Conventional TFT	5.97	105	1.53	$9.26x10^6$
Spacer distance = 1um	5.56	**130**	1.55	$1.10x10^7$
Spacer distance = 2um	4.99	**162**	1.49	$1.95x10^7$
Spacer distance = 2.5um	4.59	**176**	1.53	$1.41x10^7$
Spacer distance = 3um	4.75	**159**	1.47	$3.97x10^7$
Spacer distance = 4um	5.11	**151**	1.49	$2.73x10^7$

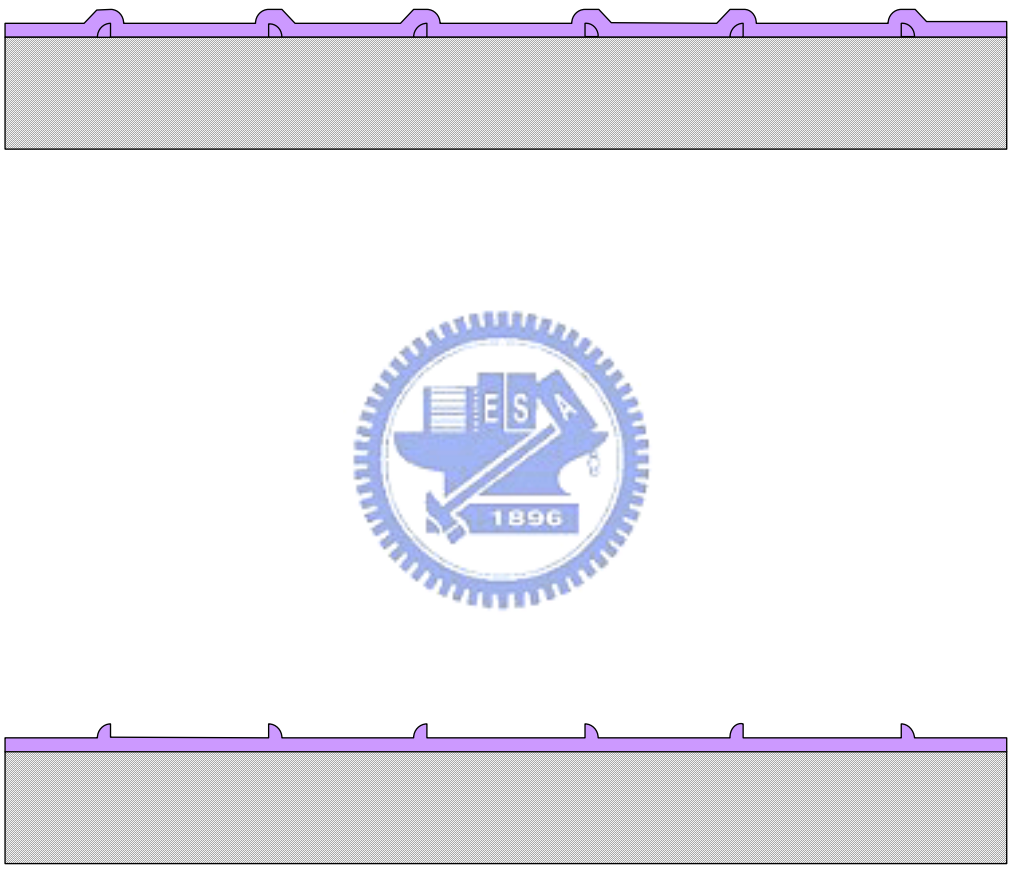


Fig. 5-1 The comparison of two a-Si spacer structures

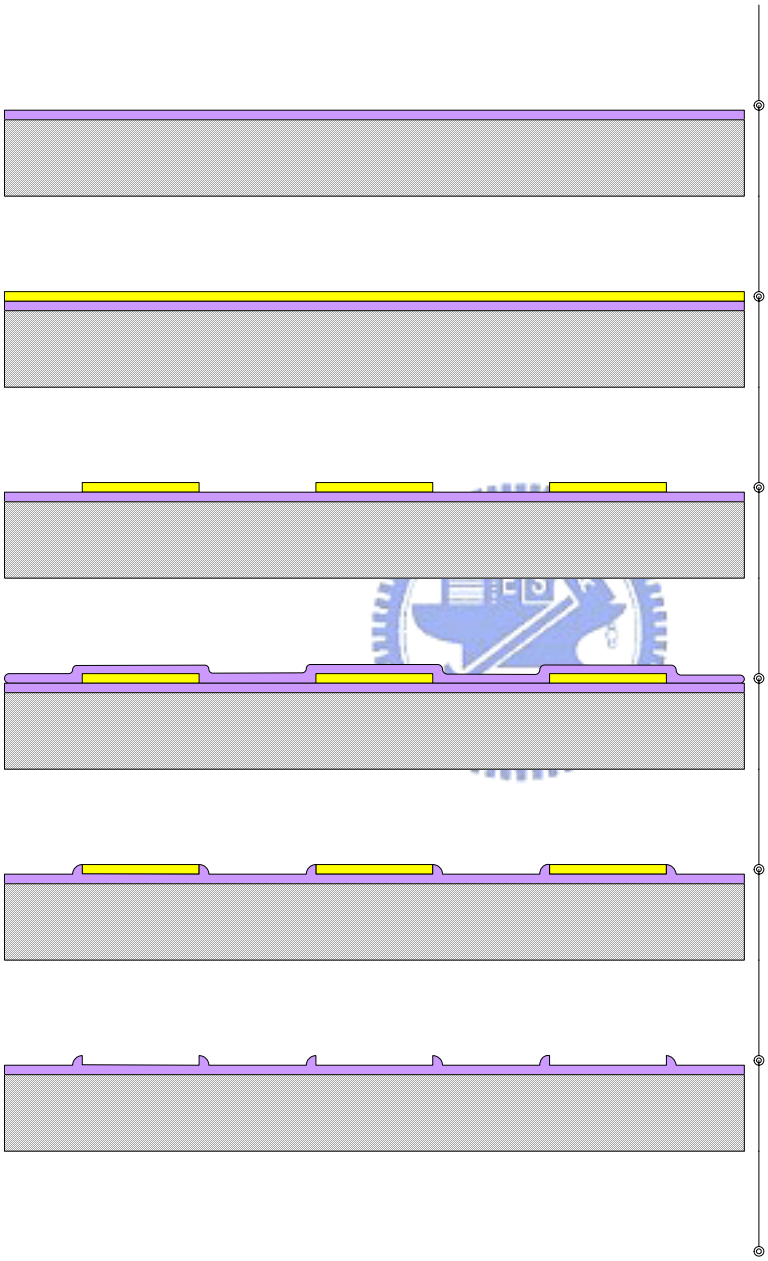


Fig. 5-2 Process flowchart of a-Si spacer structure with pre-patterned TEOS oxide layer

Ox

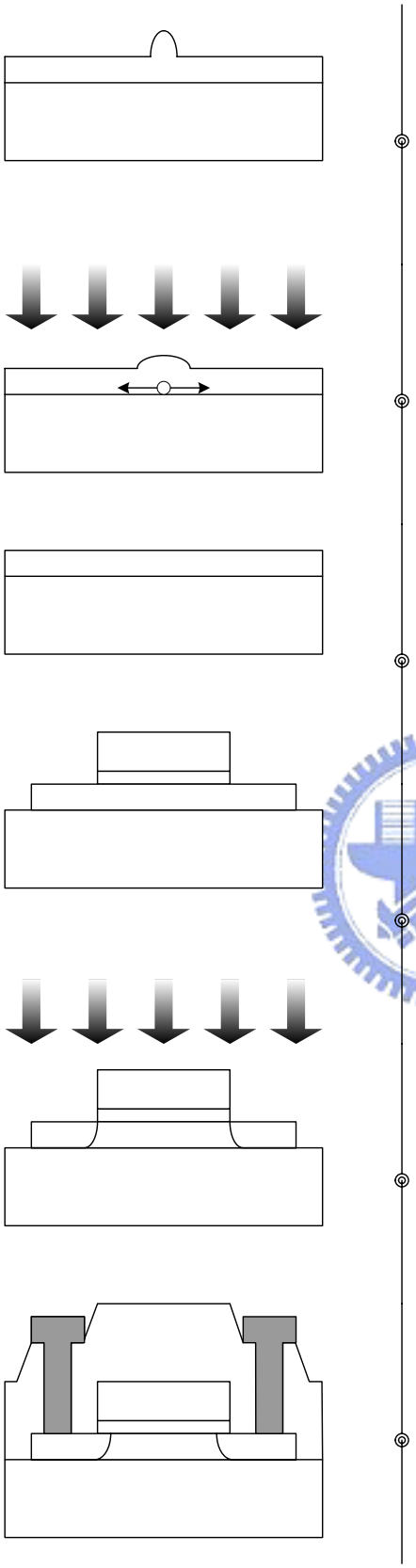


Fig. 5-3 Process flowchart of ELC LTPS TFT with a-Si spacer structure

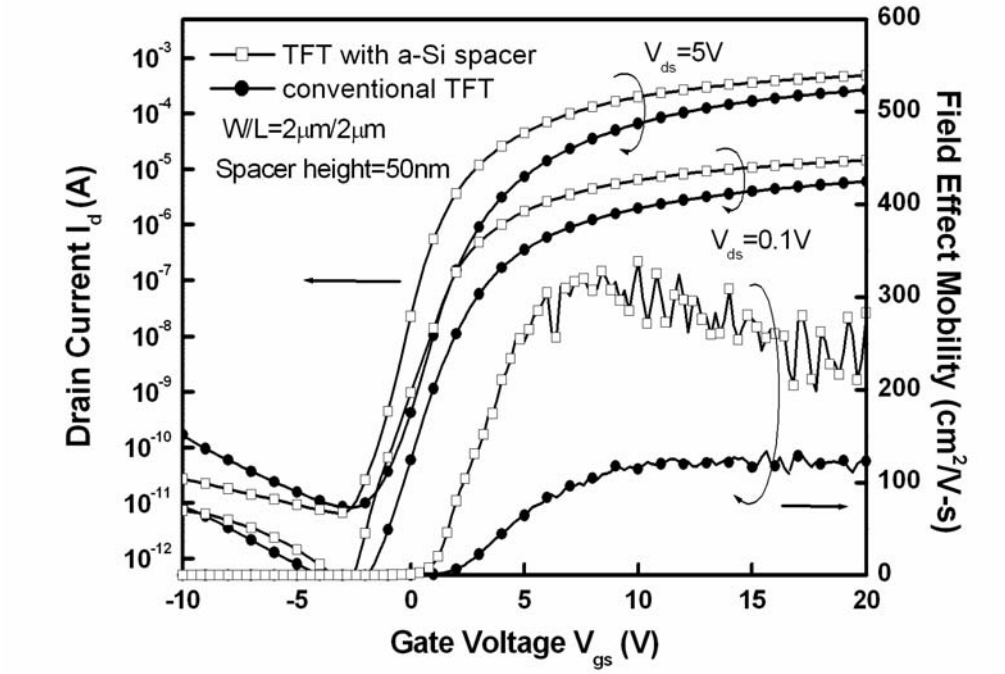


Fig. 5-4(a) Transfer characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=2μm/2μm and conventional counterpart

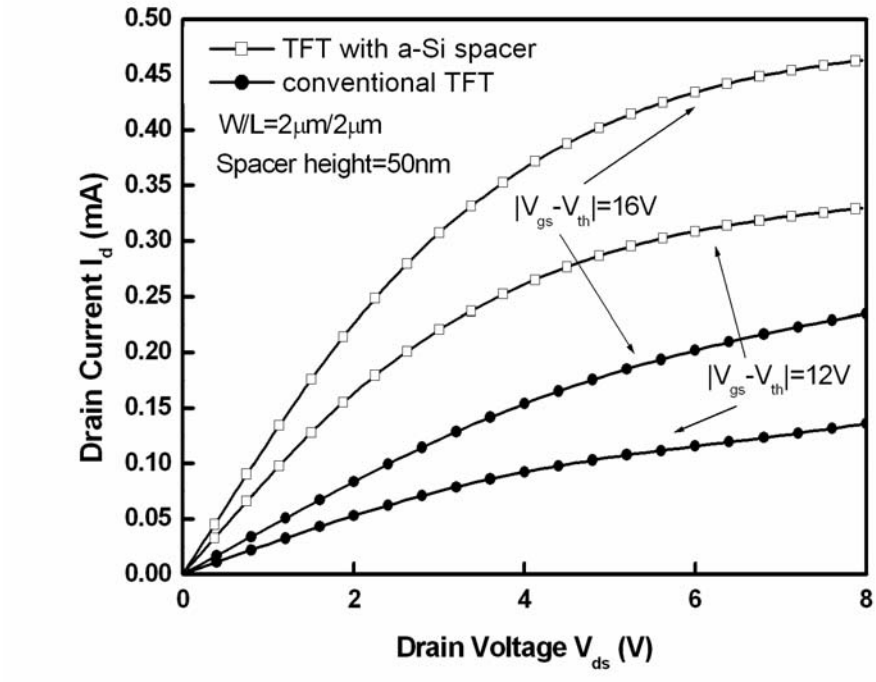


Fig. 5-4(b) Output characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=2μm/2μm and conventional counterpart

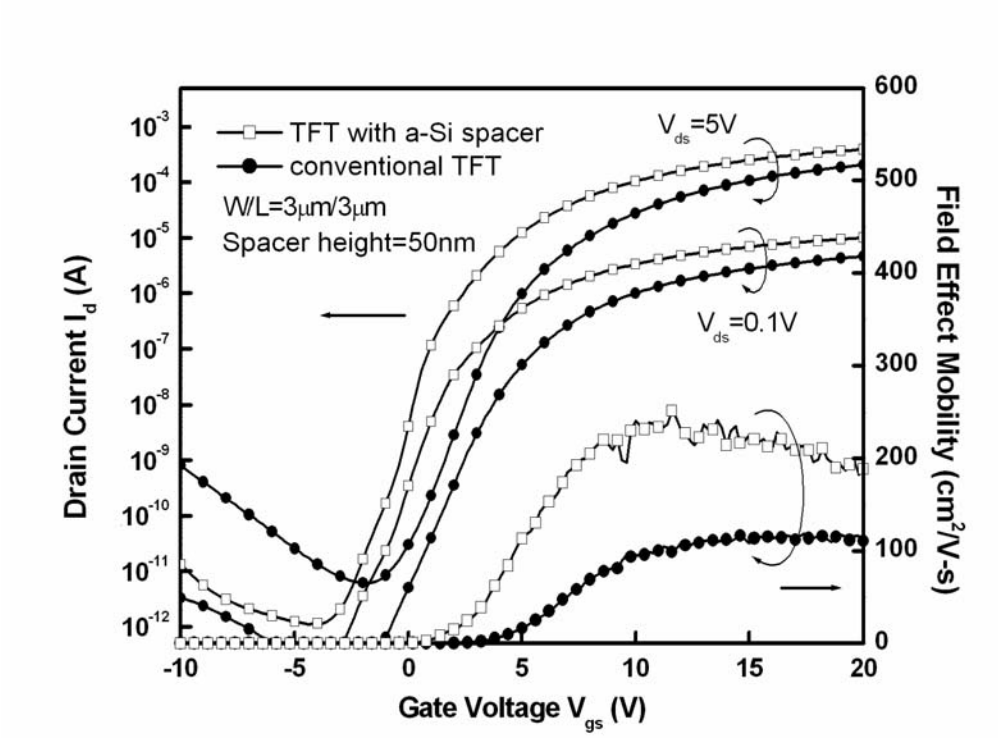


Fig. 5-5(a) Transfer characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=3μm/3μm and conventional counterpart

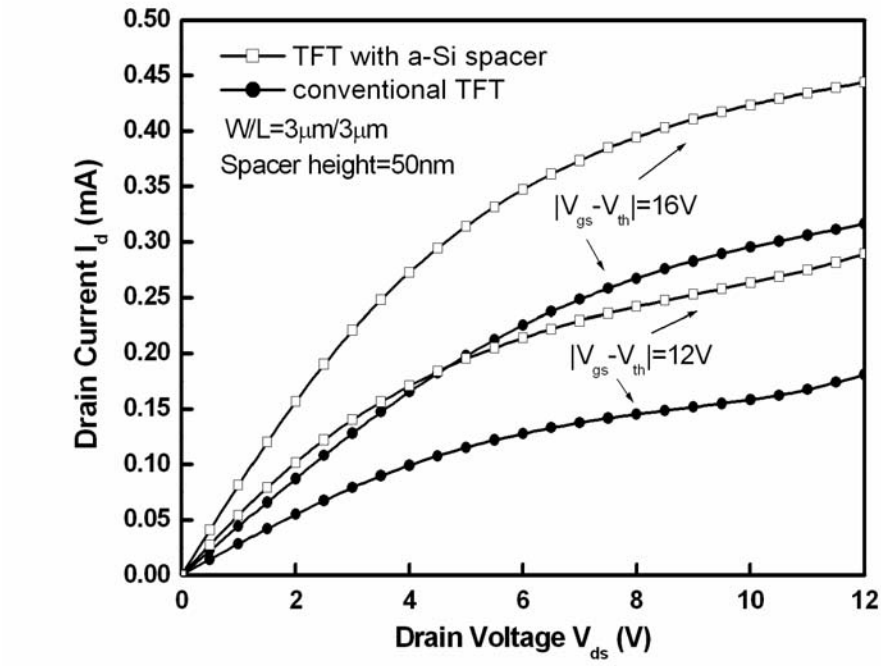


Fig. 5-5(b) Output characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=3μm/3μm and conventional counterpart

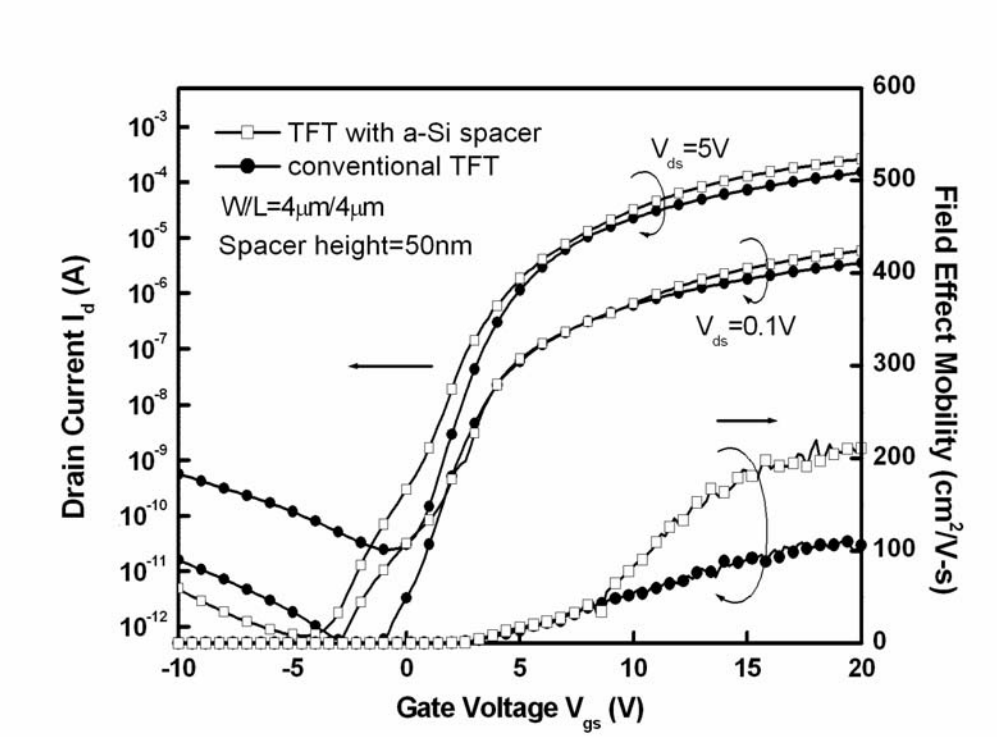


Fig. 5-6(a) Transfer characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=4μm/4μm and conventional counterpart

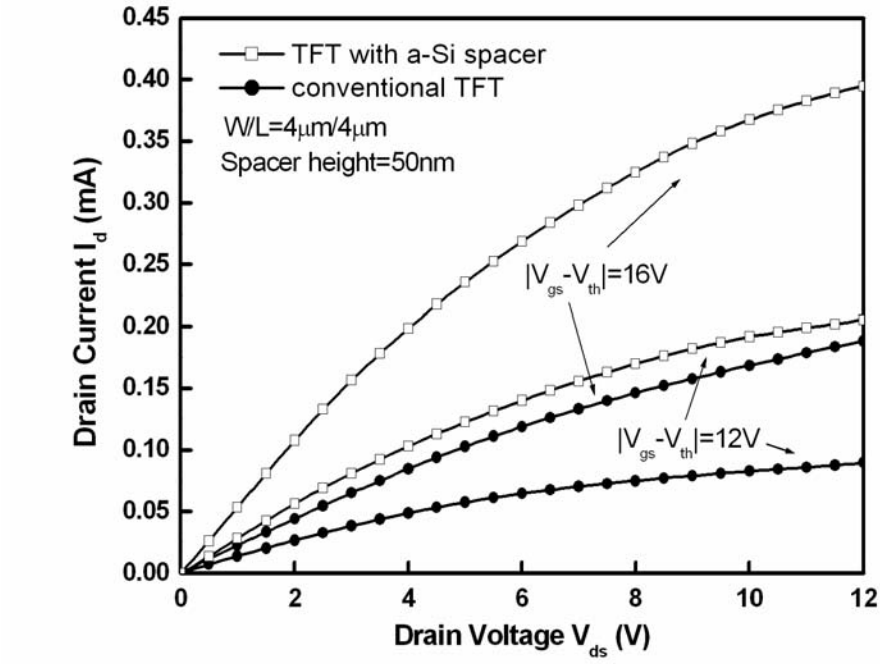


Fig. 5-6(b) Output characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=4μm/4μm and conventional counterpart

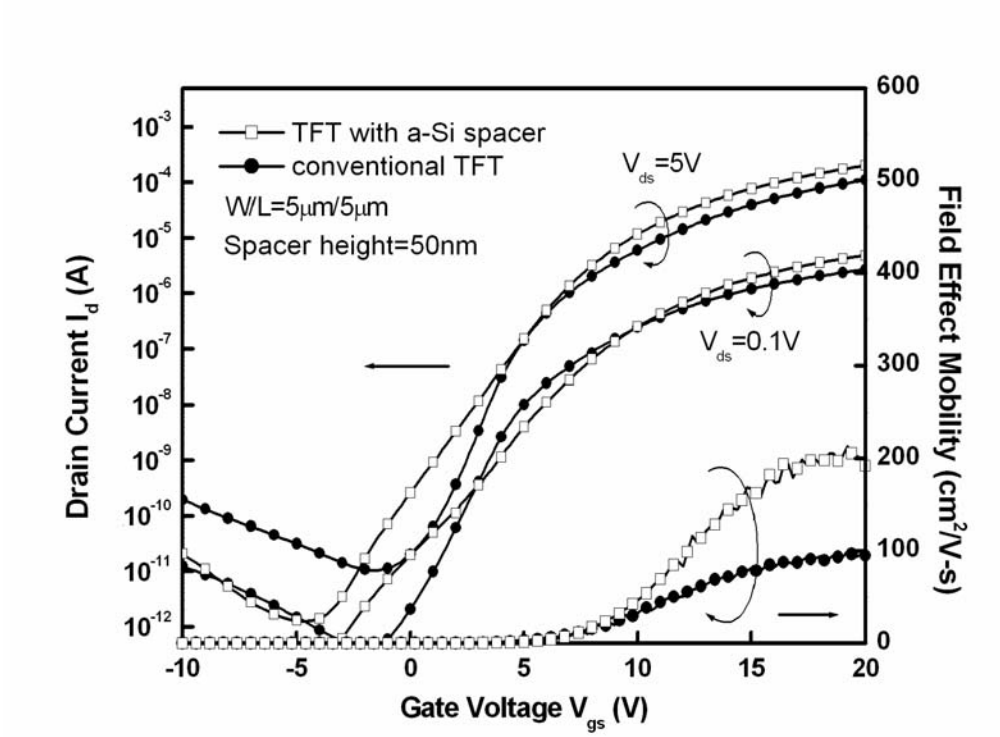


Fig. 5-7(a) Transfer characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=5μm/5μm and conventional counterpart

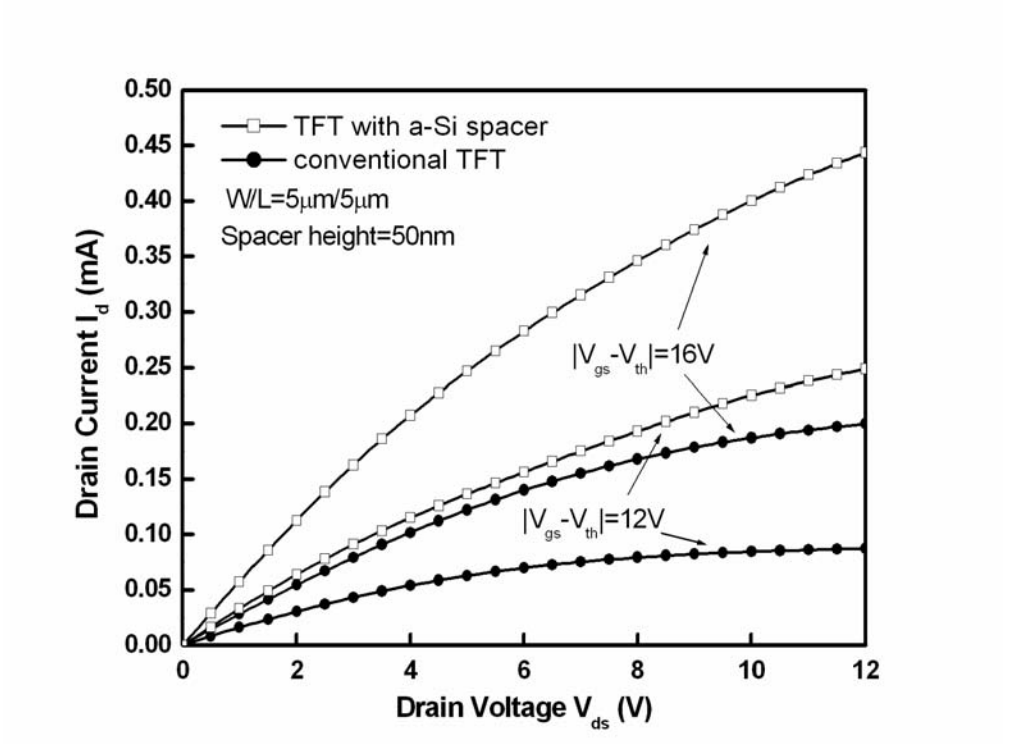


Fig. 5-7(b) Output characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=5μm/5μm and conventional counterpart

Table 5-1 Electrical characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure for different device dimension and conventional counterpart

	V_{th} (V)	Mobility (cm^2/V-s)	Sub-threshold Swing (mV/dec)	On/Off current ratio
Conventional TFT (W=L=2um)	1.94	128	738	$3.32x10^7$
TFT with Si spacer (W=L=2um)	-0.232	**367**	477	**$6.31x10^7$**
Conventional TFT (W=L=3um)	3.72	116	1010	$3.41x10^7$
TFT with Si spacer (W=L=3um)	1.324	**251**	743	**$3.52x10^8$**
Conventional TFT (W=L=4um)	3.44	108	779	$6.23x10^6$
TFT with Si spacer (W=L=4um)	3.491	**220**	785	**$3.89x10^8$**
Conventional TFT (W=L=5um)	4.99	97	1170	$1.04x10^7$
TFT with Si spacer (W=L=5um)	5.908	**213**	1691	**$1.6x10^8$**

Table 5-2 Electrical characteristics of ELC poly-Si TFT with 50nm height a-Si spacer structure for different pre-patterned layer and device dimension

	V_{th} (V)	Mobility (cm^2/V-s)	Sub-threshold Swing (mV/dec)	On/Off current ratio
TEOS oxide (W=L=2um)	-0.232	**367**	477	**$6.31x10^7$**
Nitride (W=L=2um)	0.976	**289**	672	$3.68x10^7$
TEOS oxide (W=L=3um)	1.324	**251**	743	**$3.52x10^8$**
Nitride (W=L=3um)	3.53	**206**	944	$6.81x10^7$
TEOS oxide (W=L=4um)	3.491	**220**	785	**$3.89x10^8$**
Nitride (W=L=4um)	2.29	**198**	704	$5.73x10^7$
TEOS oxide (W=L=5um)	5.908	**213**	1691	**$1.6x10^8$**
Nitride (W=L=5um)	4.84	**169**	1170	$3.6x10^7$

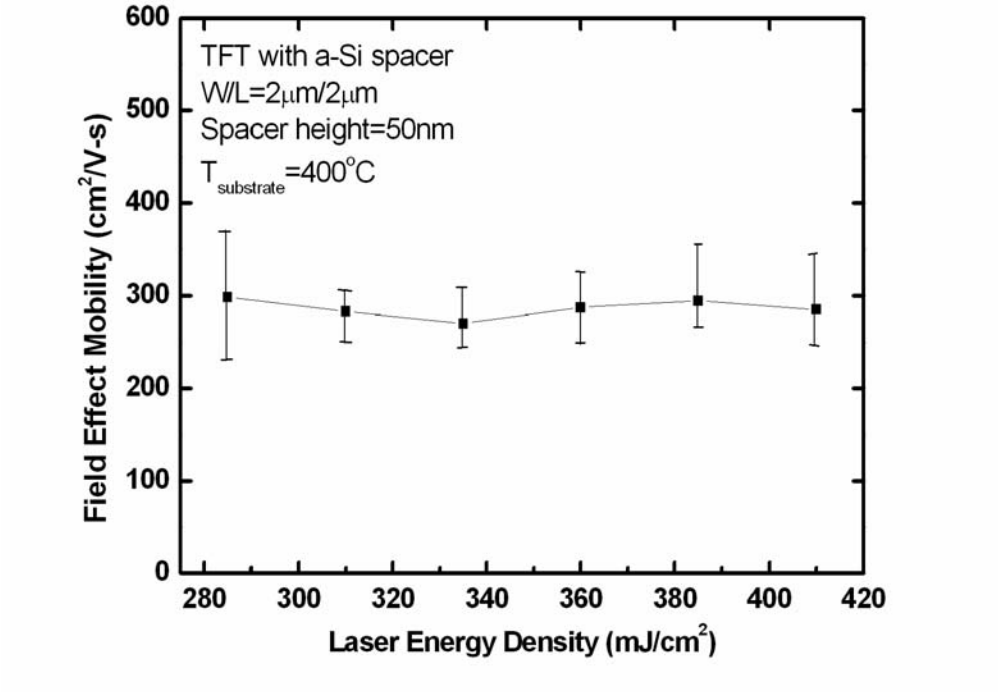


Fig. 5-8(a) Dependence of field effect mobility on laser energy density of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=2μm/2μm and substrate heating to 400ºC

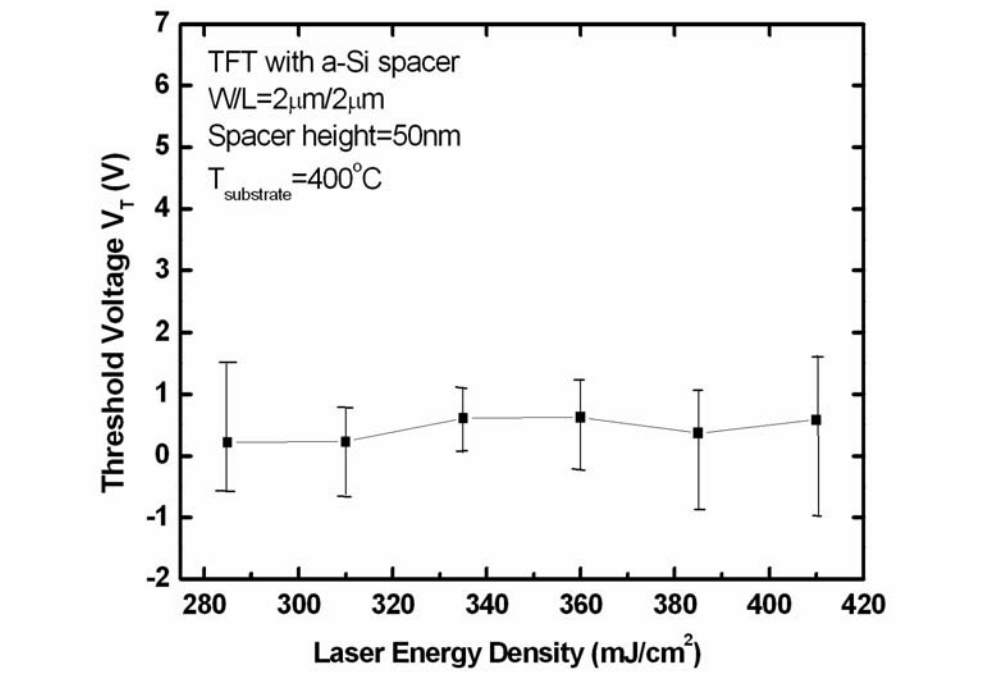


Fig. 5-8(b) Dependence of threshold voltage on laser energy density of ELC LTPS TFT with 50nm height a-Si spacer structure for W/L=2μm/2μm and substrate heating to 400ºC

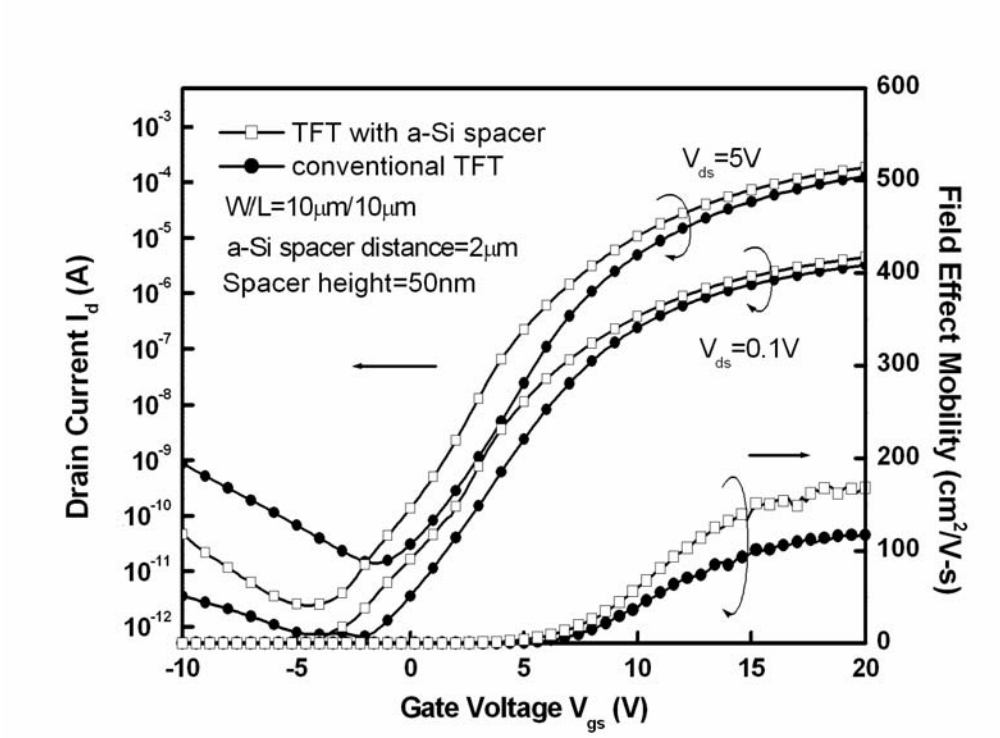


Fig. 5-9(a) Transfer characteristics of ELC LTPS TFT with 50nm height and 2μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

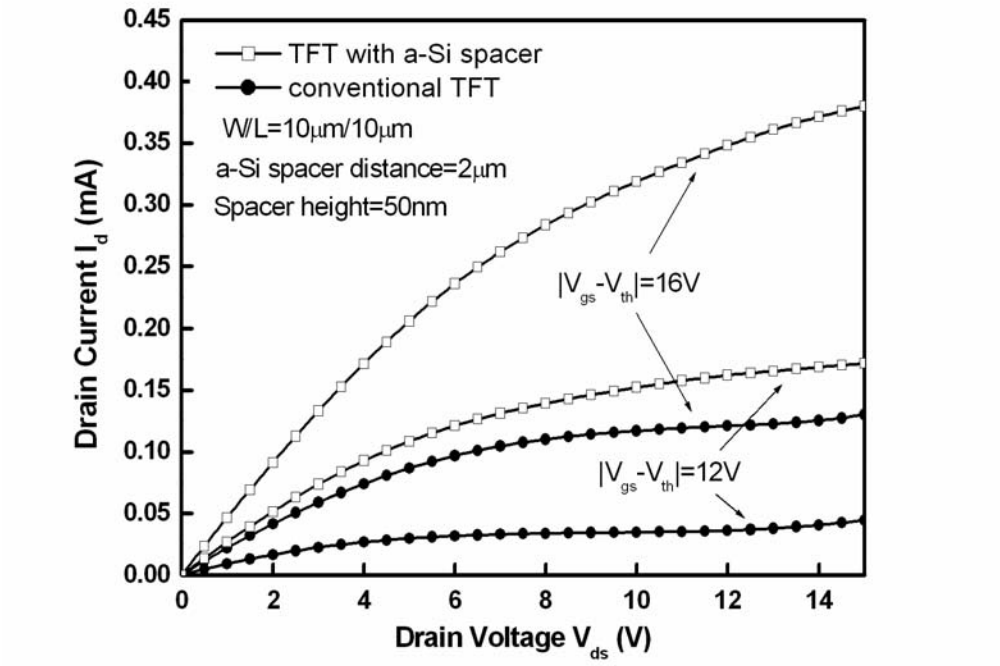


Fig. 5-9(b) Output characteristics of ELC LTPS TFT with 50nm height and 2μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

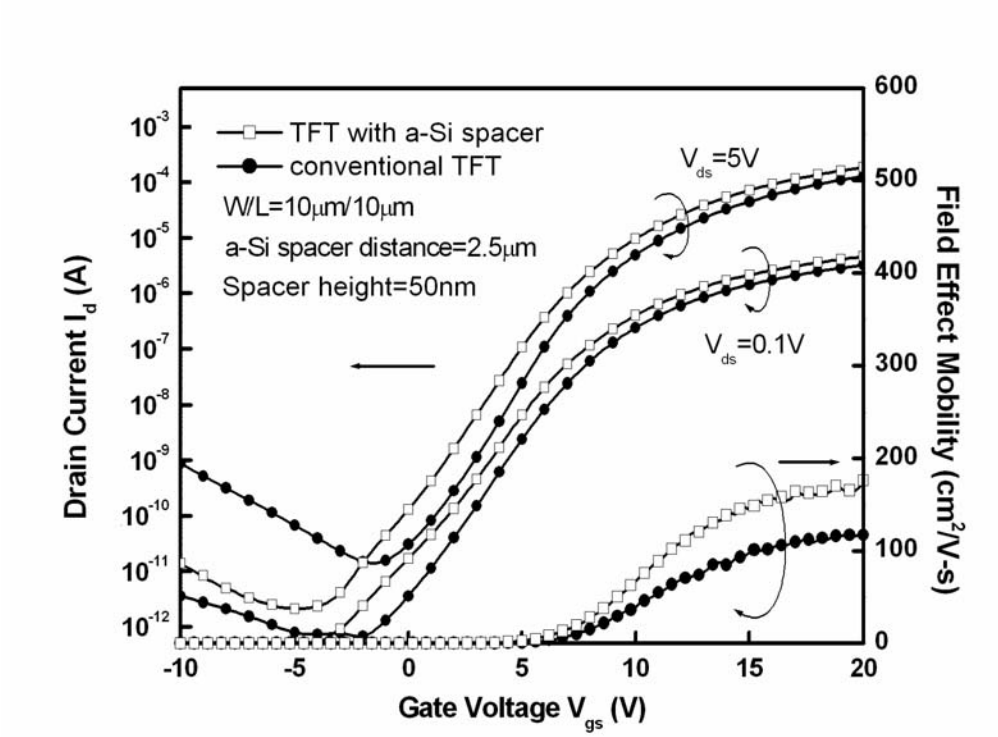


Fig. 5-10(a) Transfer characteristics of ELC LTPS TFT with 50nm height and 2.5μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

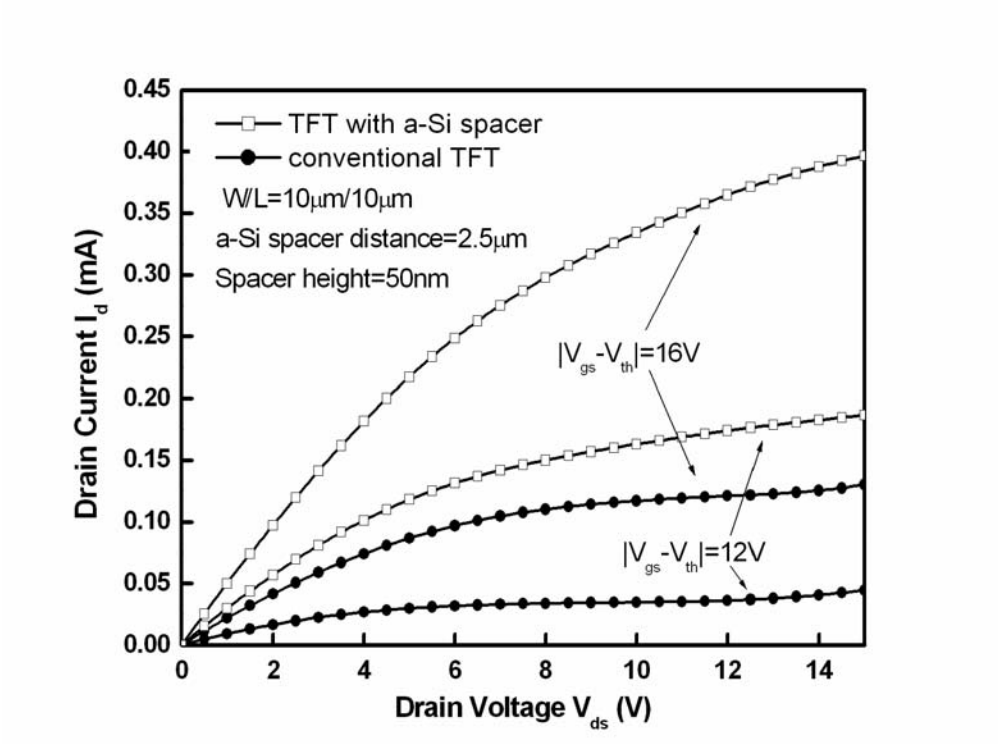


Fig. 5-10(b) Output characteristics of ELC LTPS TFT with 50nm height and 2.5μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

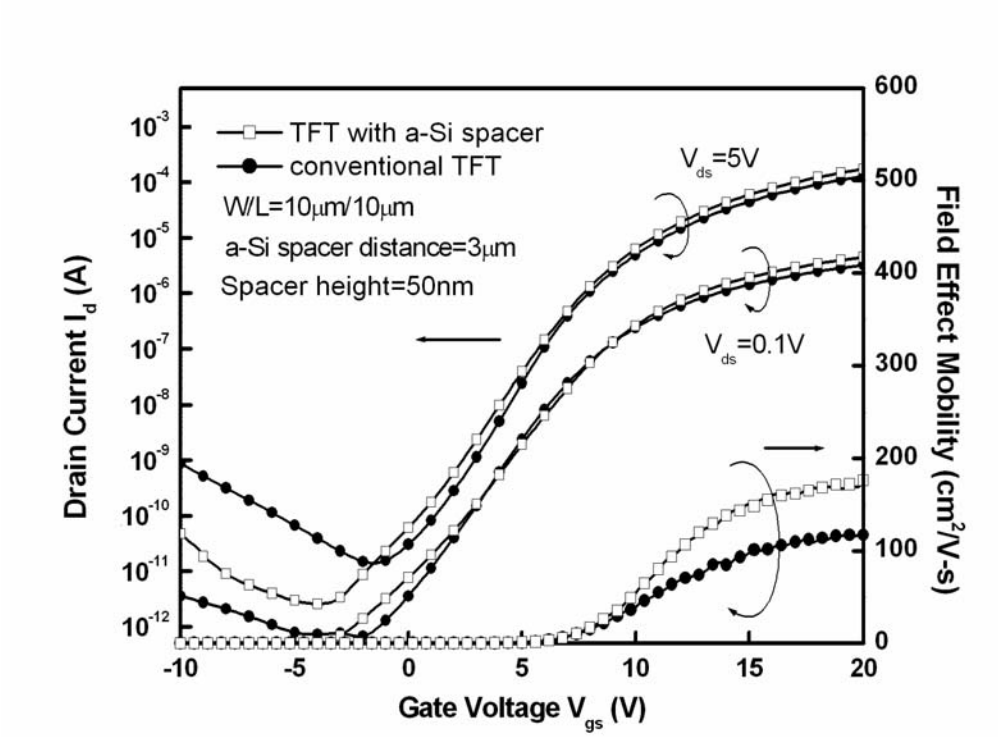


Fig. 5-11(a) Transfer characteristics of ELC LTPS TFT with 50nm height and 3μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

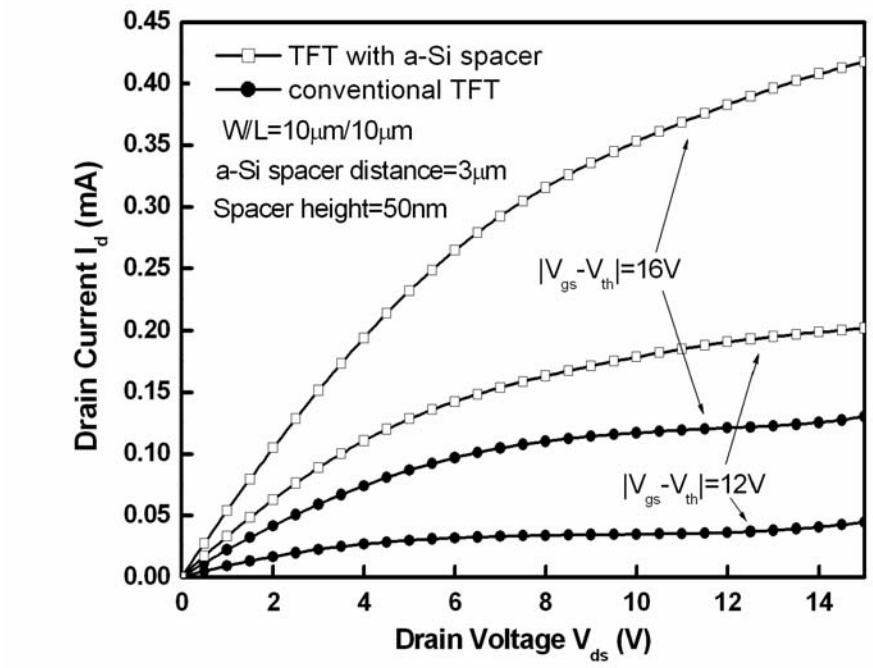


Fig. 5-11(b) Output characteristics of ELC LTPS TFT with 50nm height and 3μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

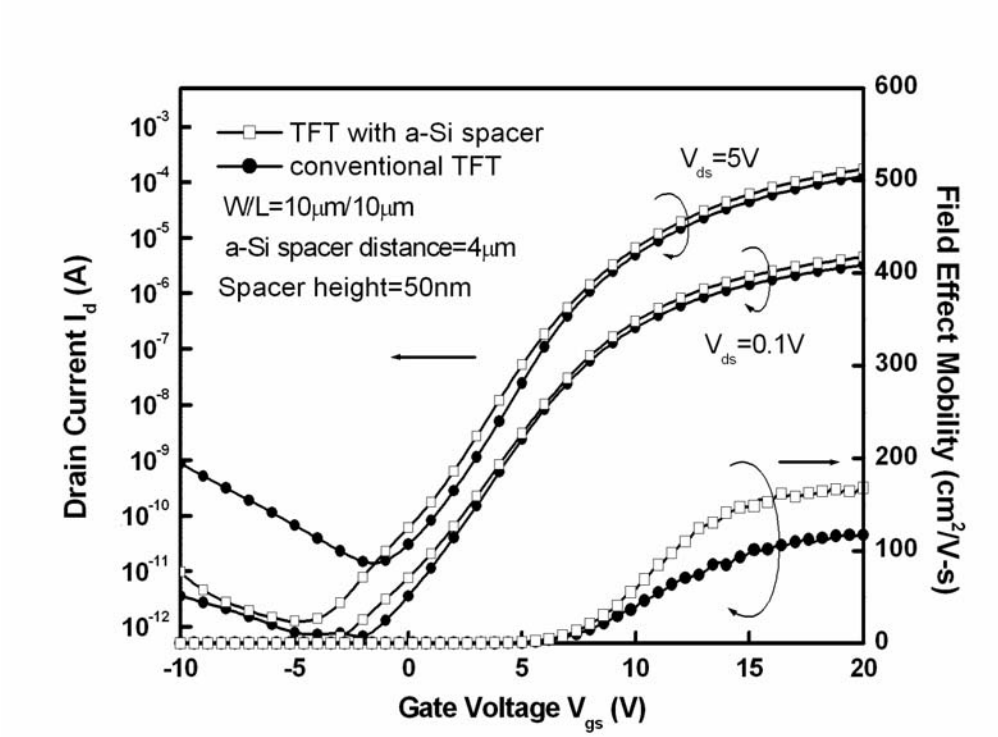


Fig. 5-12(a) Transfer characteristics of ELC LTPS TFT with 50nm height and 4μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

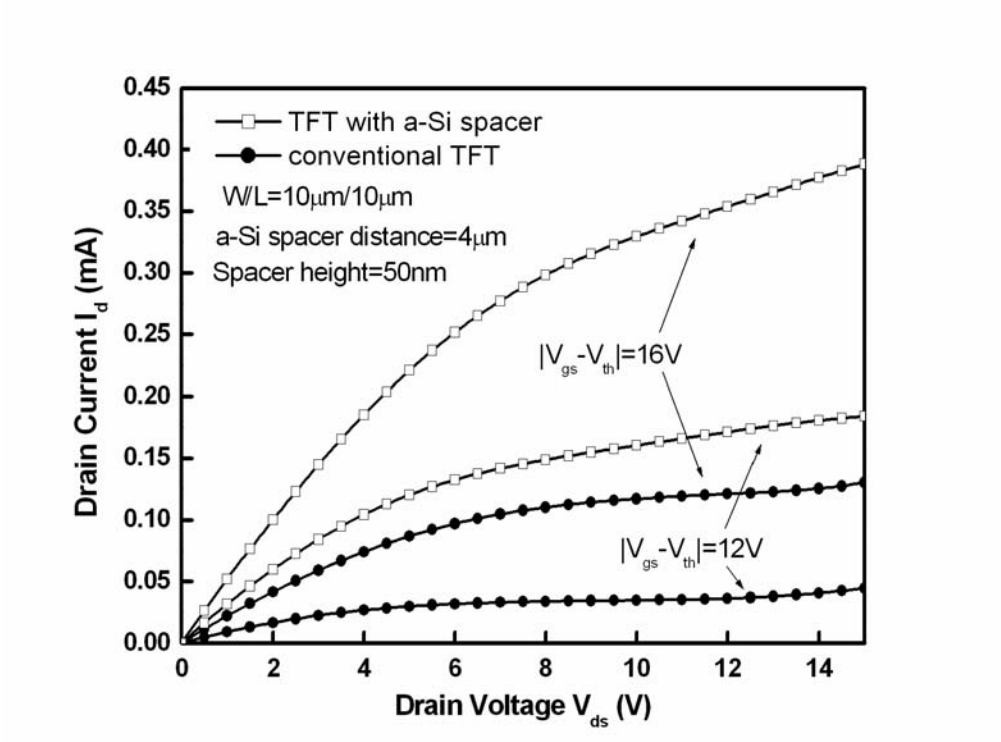


Fig. 5-12(b) Output characteristics of ELC LTPS TFT with 50nm height and 4μm distance a-Si spacer structure for W/L=10μm/10μm and conventional counterpart

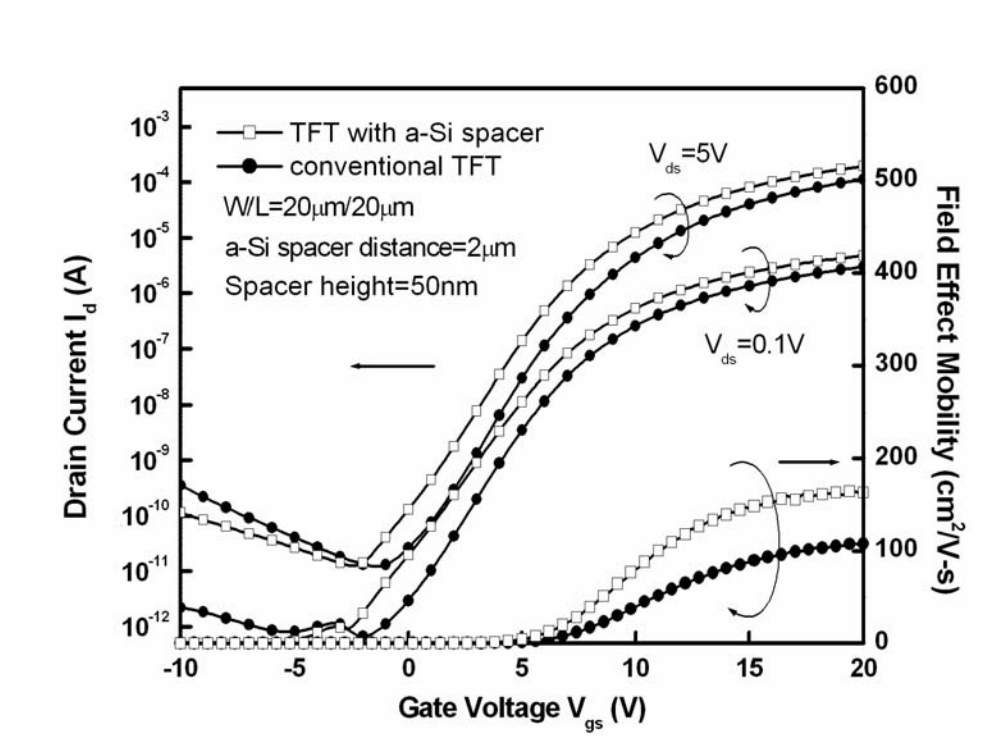


Fig. 5-13(a) Transfer characteristics of ELC LTPS TFT with 50nm height and 2μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

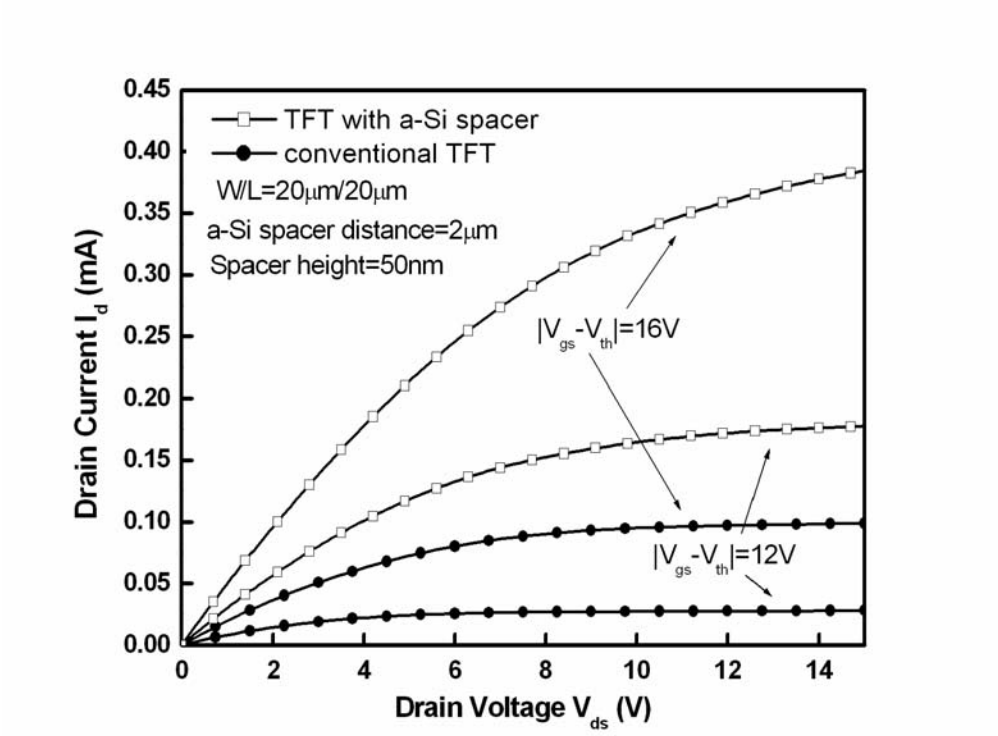


Fig. 5-13(b) Output characteristics of ELC LTPS TFT with 50nm height and 2μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

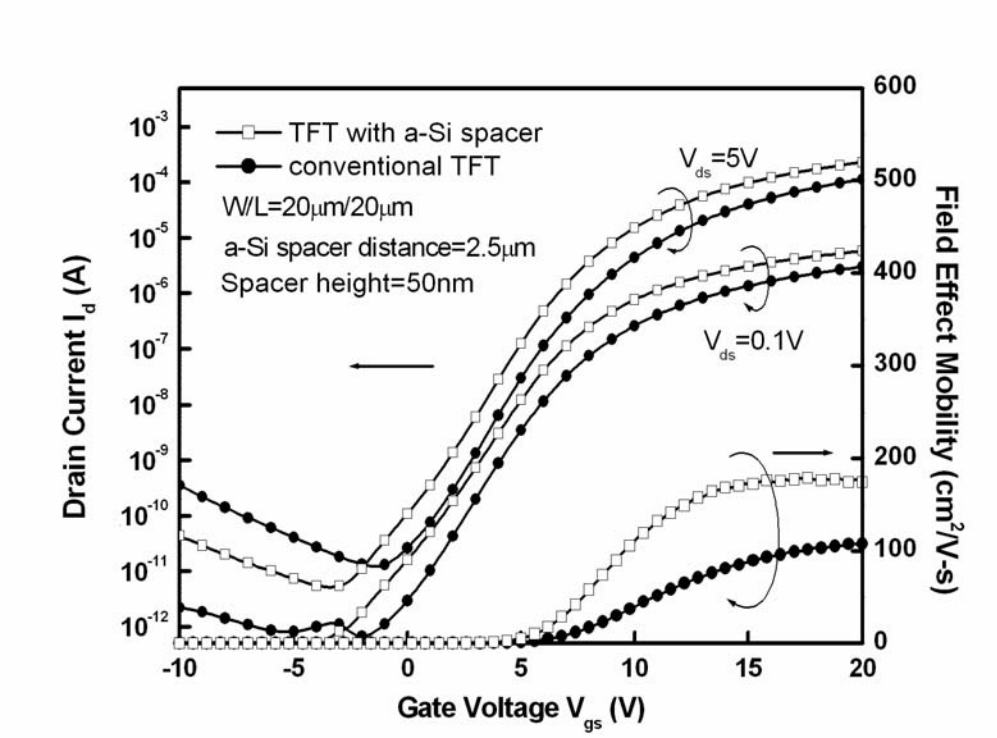


Fig. 5-14(a) Transfer characteristics of ELC LTPS TFT with 50nm height and 2.5μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

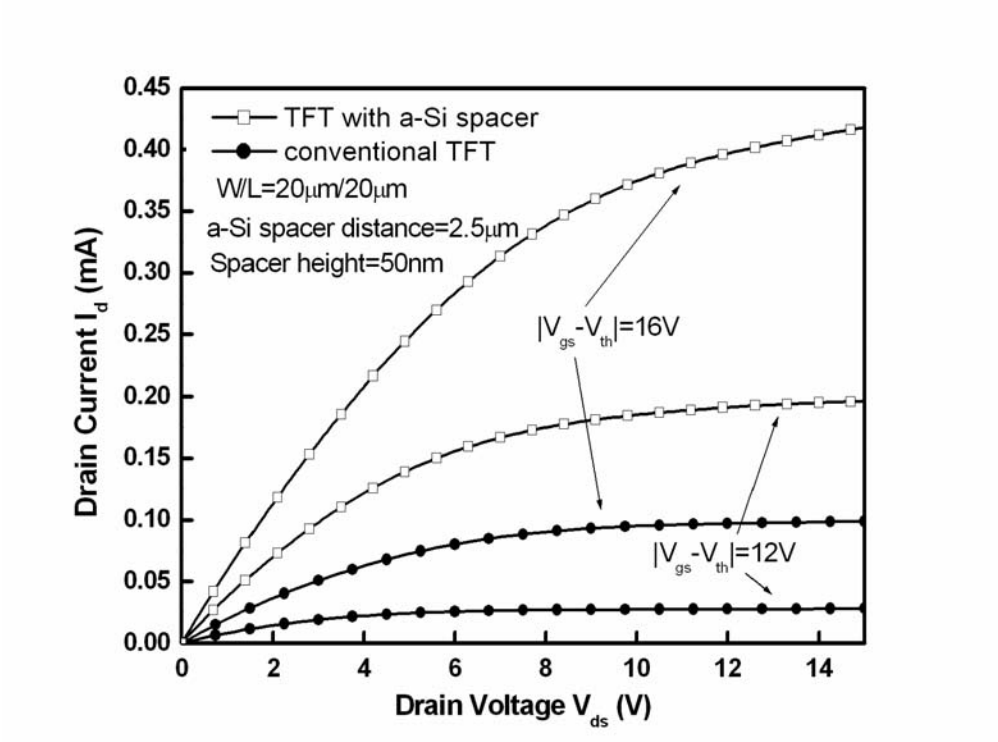


Fig. 5-14(b) Output characteristics of ELC LTPS TFT with 50nm height and 2.5μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

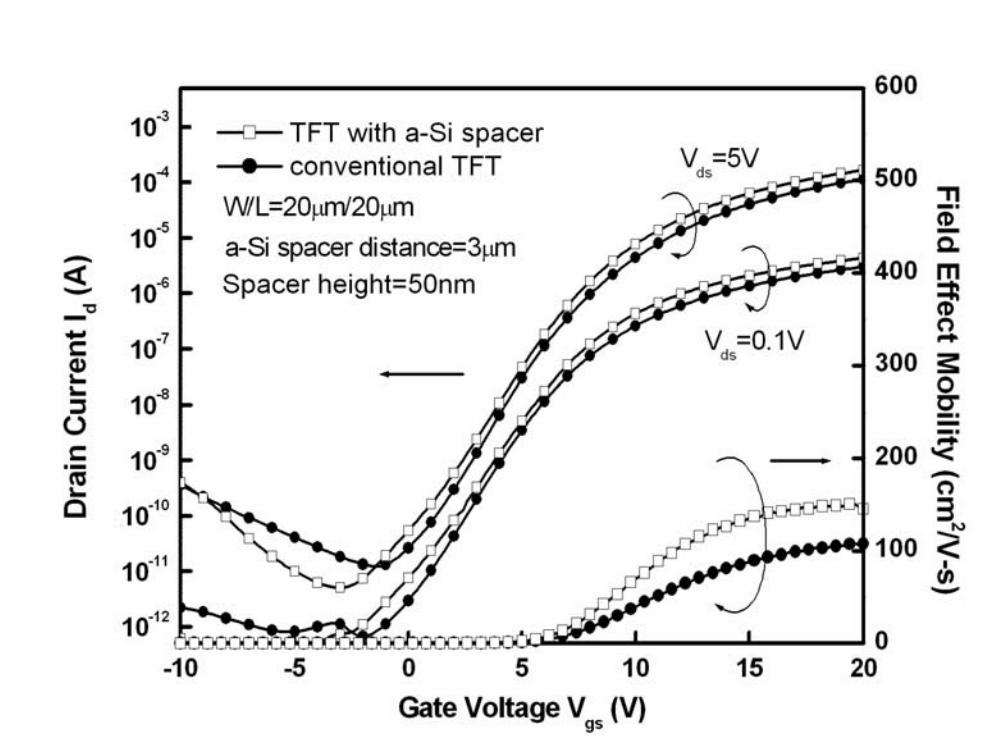


Fig. 5-15(a) Transfer characteristics of ELC LTPS TFT with 50nm height and 3μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

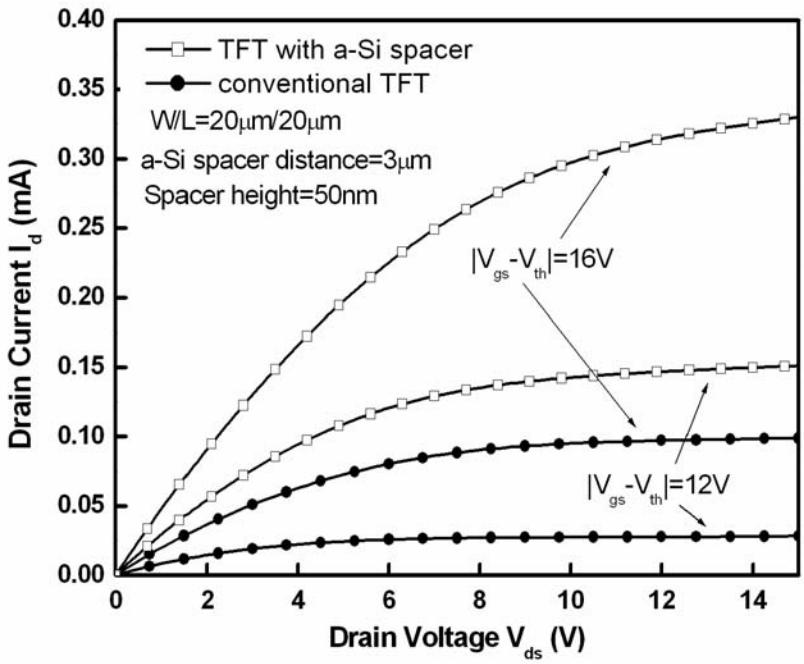


Fig. 5-15(b) Output characteristics of ELC LTPS TFT with 50nm height and 3μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

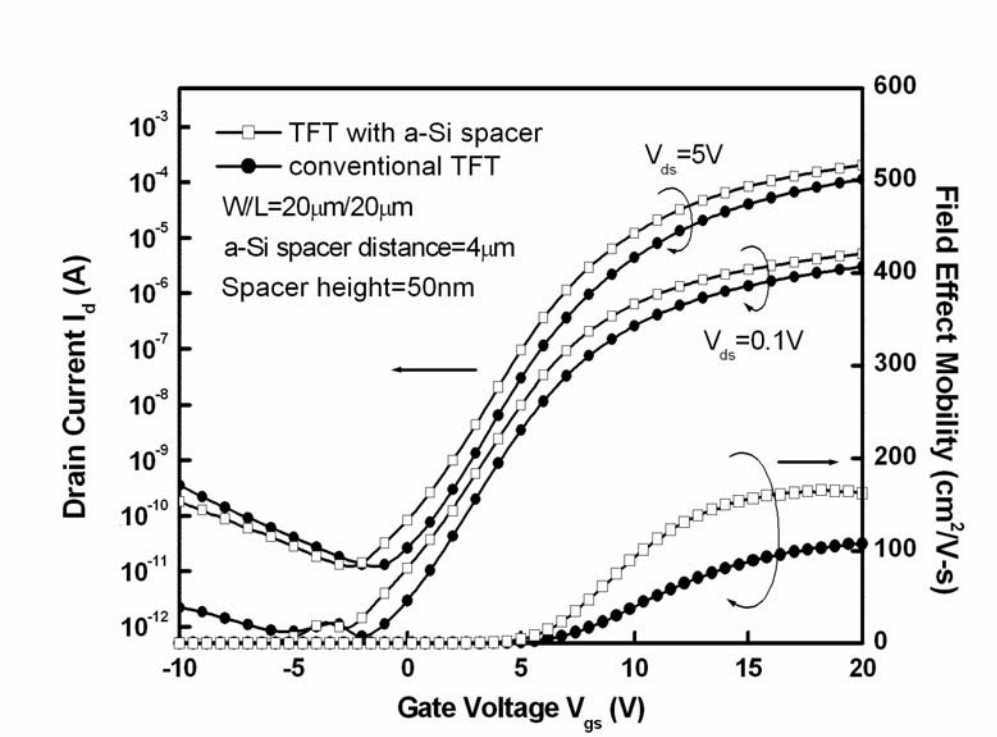


Fig. 5-16(a) Transfer characteristics of ELC LTPS TFT with 50nm height and 4μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

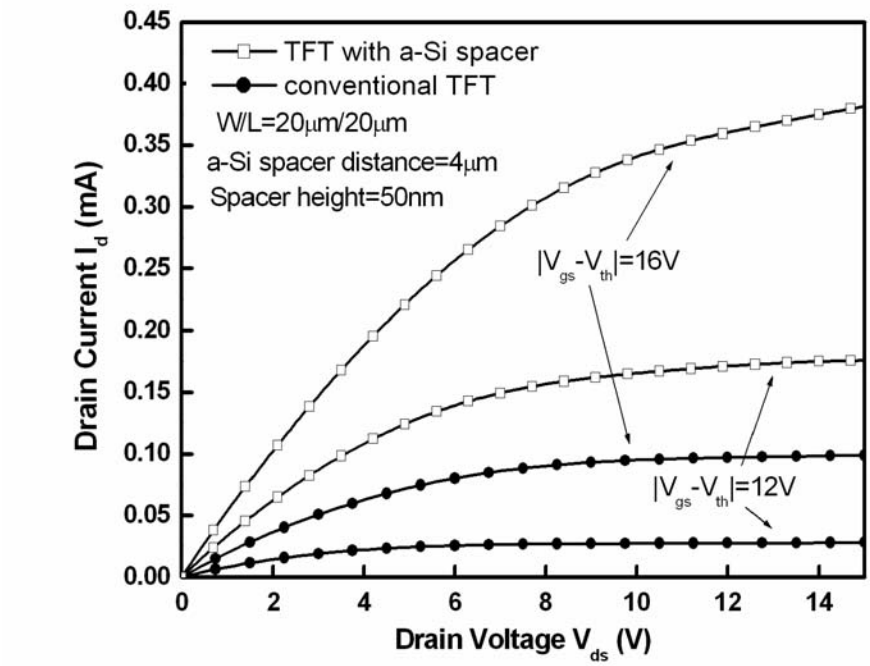


Fig. 5-16(b) Output characteristics of ELC LTPS TFT with 50nm height and 4μm distance a-Si spacer structure for W/L=20μm/20μm and conventional counterpart

Table 5-3 Electrical characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure and W/L=10μm/10μm for different a-Si spacer distance and conventional counterpart

	V_{th} (V)	Mobility (cm^2/V-s)	Sub-threshold Swing (V/dec)	On/Off current ratio
Conventional TFT	6.16	114	1.612	$9.27x10^6$
Spacer distance = 2um	4.883	**170**	1.274	**$7.76x10^7$**
Spacer distance = 2.5um	5.353	**176**	1.604	**$8.92x10^7$**
Spacer distance = 3um	6.403	**176**	1.806	**$6.81x10^7$**
Spacer distance = 4um	5.995	**168**	1.735	**$1.4x10^8$**

Table 5-4 Electrical characteristics of ELC LTPS TFT with 50nm height a-Si spacer structure and W/L=20μm/20μm for different a-Si spacer distance and conventional counterpart

	V_{th} (V)	Mobility (cm^2/V-s)	Sub-threshold Swing (V/dec)	On/Off current ratio
Conventional TFT	5.97	105	1.53	$9.26x10^6$
Spacer distance = 2um	4.902	**164**	1.72	$1.56x10^7$
Spacer distance = 2.5um	4.86	**179**	1.614	$4.44x10^7$
Spacer distance = 3um	5.542	**151**	1.377	$3.26x10^7$
Spacer distance = 4um	4.819	**166**	1.354	$2.51x10^7$