# Chapter 3

The Fabrication of the thin film transistor and the characteristic of electric

3.1 Introduction

A typical substrate temperature for a-Si: H TFT in glass substrate is about 300ºC; however, the substrate temperature of a-Si: H on plastic should be kept less than about 150ºC, because most plastic cannot withstand prolonged heating above this temperature.   Because of dimensional change of the plastic during heating, the substrate temperature should be kept as low as possible.   The actual upper limit depends on plastic material itself. [1] In this chapter, all of the thin film is deposited at 100ºC by the PECVD mwthod.
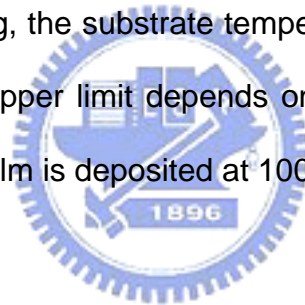
3.2 Low Temperature Deposition

3.2.1 Amorphous silicon

A good deal of experimental work has been performed on the deposition of a-Si: H at low temperatures.   One technique for deposition a-Si: H at low temperature is by reactive RF sputtering [2], where hydrogen is added to the Ar ambient in the sputtering chamber in order to deposit device-quality material that has a hydrogen content of 5-10 at %.   Films deposited at low temperature generally have high hydrogen content, but most of the hydrogen is bonded as Si-H2, and the film can be porous, leading to gas absorption from the air.

Further, the film may have a columnar structure and a significant density of defects [3]. The addition of He and/or hydrogen causes the growth rate to decrease and the hydrogen to bond as Si-H, improving the electronic properties.

Dilution of silane with hydrogen is widely used to enhance the electronic properties of a-Si: H and alloys over a wide temperature range. Hydrogen atoms produced in the plasma bring substantial energy to the growth surface. At 100ºC, the hydrogen content can be controlled to be the same as that in higher temperature films. Hydrogen removal can occur via hydrogen abstraction, either by hydrogen atoms or by silyl radicals impinging on the growth surface creating silicon dangling bonds.

Si-H$_x$ + H →   Si-H$_{x-1}$ + H$_2$

Si-H$_x$ + Si-H$_3$ →   Si-H$_{x-1}$ + Si-H$_4$

Hydrogen will also create dangling bonds by inserting into strained Si-Si bonds, eventually leading to etching

Si-Si-H$_x$ + H →   Si-H$_{x+1}$ + Si-

Thus it can be seen that using the hydrogen to dilute with SiH4 can improve the film quality, when the amorphous film is deposited at low temperature.   In order to improve it, we try different kind of the SiH4/H2 ratio to deposit the amorphous silicon.   First, we deposit a wet oxide layer on the

silicon wafer.   Then, we deposit the amorphous silicon with different SiH4/H2 ratio on the thermal oxide.   The aluminum film was deposited by the thermal coater on the amorphous layer.   The photoresist and wet etching were using to pattern the aluminum film to define the source and drain metal.   At last, the backside of the silicon wafer was coated with the aluminum to be served as the gate metal. The simple FET device is completed, Fig3-1.   It was using to study the performance of the amorphous silicon under different SiH4/H2 ratio.

We tried two kinds of SiH4/H2 ration, 1/10 and 1/49. When the SiH4/H2 ration is 1/10 (SiH4: 10sccm, H2: 100sccm, the deposit pressure 0.6mTorrs, the deposit temperature 100℃, and the deposit time is 30 minute).The transfer characteristics and the output characteristic are shown in Fig.3-2.   From the transfer characteristic of the device, we observe that the on/off ratio is 2 when the Vds is 30V and the testing device W/L is 300um/20um.   The output characteristic almost can't be observed, when the Vg are 0V and 40V, respectively.   Next, the SiH4/H2 ratio we utilized is 1/49 (SiH4: 10sccm, H2: 490sccm, the deposition pressure is 0.6mTorr, the deposit temperature is 100℃, and the deposit time is 30 minutes).   The transfer characteristics and the output characteristics are shown in Fig.3-3.   From the transfer characteristic of the device, we observe that the on/off ratio is 5 order   when the Vds is 30V and the testing device W/L is 300um/20um.   The output characteristic almost can be observed at the various Vg, such as 0V, 10V, 20V, 30V and 40V.   The comparison with the two different results, we find that the performance of the amorphous silicon is better by using the high hydrogen gas dilution.   It can prove the previously explanation.   So, we try to use the condition to deposit the amorphous film and apply to fabricate the thin film

transistor on the plastic substrate.

3.2.2 The gate dielectric

We deposited the SiON films to be the gate dielectric. The high flow N2 rate is involved to deposit the SiON film. The SiON film is deposited from the mixtures of SiH4, N2O and N2 using PECVD at a pressure of 0.6 mTorr. The layer is deposited at 100ºC and the SiH4, N2O and N2 flow were 10, 100 and 500 sccm, respectively. In order to study the performance of the film, it was deposited on the oxide to form an MIM structure (metal-insulator-metal). Fig. 3-4 shows the FTIR absorption spectra of the SiON layer. According to the diagram, we observed the N-H bonding which contributes to the defects in electrical conduction. Fig. 3-5 shows the I-V measurement of the SiON layer. We observed that the leakage current was about 1E-10. The result was still acceptable for a low temperature deposited film.

The introduction of high-k dielectric TiO2 to gate dielectric application can enhance the control ability of gate electrode, inducing channel formation readily. In other words, the device has the lower threshold voltage. Therefore, we also introduce the high-k dielectric Al_2O_3 and TiO2 to be the gate dielectric. First, the high-k film was also deposited on the silicon and fabricated to form a MIM structure. In order to realize the characteristics of the dielectric film, we performed the I-V and C-V measurements. Fig. 3-6~3-9 show the I-V and C-V measurements of the Al_2O_3 and TiO2, respectively. We observed that both the films have the same leaky magnitude, 1e-5. If we want to use the high-k dielectric to be the gate dielectric, we must deposit

another additional layer above it to prevent the leakage current.   As a consequence, we deposit a thin SiON layer after the deposition of high-k dielectric and form the multilayer as the gate dielectric.

3.3 The fabrication of the amorphous thin film transistor on plastic substrate

The cross-sectional of the TFT structure is shown in Fig.3-10.   All the deposition experiments were performed in the PECVD reactors and all layers were deposited at 100ºC.   The fabrication process is shown as follow:

- The different kinds of the hard coating were deposited on the plastic substrate.   The SiCN, SiN and SiON were deposited by the PECVD at 100ºC and the Al_2O_3 and TiO_2 were deposited by the Dual E-Gun Evaporation System.

- The 3000Å aluminum was deposited on the oxide/si and plastic at the same time by the Thermal Evaporation Coater.   Then, the aluminum film was patterned by the photo-lithography and wet etching to form the gate metal.

- The gate dielectric, amorphous silicon and n+ silicon were deposited by the PECVD at 100ºC, in situ.   After the deposition of these kinds of the film, we used several kinds of plasma treatment to improve the film quality.   For example, the H2 plasma treatment was used after deposited the amorphous silicon. And the NH3 plasma treatment was used after deposited the SiON layer.

- The 5000Å aluminum was deposited and was also patterned by using photolithography and wet etching to form the source/drain metal.

- Similarly, n+ silicon and the amorphous silicon were patterned by using the photolithography and wet etching to form the source/drain region and the active region respectively.

3.4 Measurement of Device Parameter

The current – voltage characteristic measurements of thin film transistor devices were performed by HP 4156C Precision Semiconductor Parameter analyzer.

3.5 Results and Discussion

We had already successfully fabricated the thin film transistor on the silicon substrate, glass and plastic substrate, respectively. It was shown in Fig. 3-11. Fig. 3-12 depicts the output (I_D-V_D) characteristics and the transfer (I_D-V_G) characteristics of the TFT which was fabricated on the silicon substrate with the channel width and channel length are 300 μm and 20 μm, respectively. The threshold voltage, on/off ration and mobility were 68.71V, 1E5 and 0.08 cm^2/V.s respectively. It was obviously observed that the threshold voltage was shifted. These phenomena are inferred to the films deposited at low temperature by the PECVD method. The films deposited at low temperature by the PECVD method were not good enough and the issues may become more seriously after stacking layer by layer. The roughness of the interface

will cause the mobility decrease.   And the gate dielectric may have numerous defects, these defect will also cause the device performance poor.

Fig. 3-12~15 depicts the output (I_D-V_D) characteristics and the transfer (I_D-V_G) characteristics of the TFT which was fabricated on the plastic substrate with different channel width and channel length.   Besides, the hard coating layers are SiCN and SiCN/SiN, respectively.   We obviously observed that characteristic was poorer by comparing with the Fig. 3-11.   The threshold voltage was also obviously shifted and the on/off ratio was 1E3.   We suggested that there were many reasons caused the characteristic poor. For example, the substrate was bended seriously after the sack of all the films and the bending will cause the cracking of the film due to the mismatch of stress between hardcoating and plastic substrate. The possible causes for poor electric characteristics may be that the active regions of TFT were not patterned completely.   In other words, all silicon active regions were connected, not isolated.   It was due to that the plastic was bended during the photolithography and wet etching; the bending will cause degradation of the film.   These results in that the film can't tolerate the wet etching process again and again.   Nevertheless, we still successfully fabricated the thin film transistor on the plastic substrate.

Fig. 3-16~17 depicts the output (I_D-V_D) characteristics and the transfer (I_D-V_G) characteristics of the TFTs which were fabricated on the plastic substrate with TiO2 hard coating and with different channel width and channel length.   It was obviously observed that the performance was better by comparing with Fig. 3-12~15.   The mobility can reach about 7E-3 cm^2/V.s and

the on/off ratio was 1E4. The TiO2 can compensate the stress from stack films, beneficial to microlithography process; thereby, superior electrical characteristics were obtained in my work.

In order to use the high-k dielectric to be the gate dielectric, we deposited a thin SiON layer on the high-k dielectric to prevent the leakage from the high-k film.   Although we deposited the thin SiON layer, the electric characteristic still can't be measured.   Nevertheless, we still can fabricate the thin film transistor on plastic substrate. The complete diagram was shown in Fig. 3-18.

3.6 Conclusion

Experimental results have shown that the adhesion between the SiCN and plastic substrate can be improved significantly, increasing feasibility of fabricating TFT on the plastic substrate. Furthermore, the usage of double-layer SiCN/SiN hardcoating will not modify the adhesion to the plastic in comparison with single SiCN coating.   The TiO2 hard coating can compensate the stress from stack films, and beneficial to microlithography process; thereby, superior electrical characteristics are obtained in our work. Besides, we can fabricate the thin film transistor at low temperature by using the high H_2 dilute.   By using the hard coating and low temperature method, the thin film transistor have the output characteristic and transfer characteristic, and the mobility can reach about 0.08 cm^2/V.s on the Si substrate and 0.0007 cm^2/V.s on the plastic substrate.