國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

適用於 CMOS 製程之高慢波係數共平面帶線

及其在濾波器之應用

High Slow-Wave-Factor Coplanar Stripline

in CMOS Technology and Its Application to Filter Design

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摘要

本文提出一種適用於標準CMOS製程的新式傳輸線結構—高慢波係數共平面帶線，並將其運用在濾波器之設計。

本設計藉由同時增加傳輸線單位長度電感值及單位長度電容值，可在不改變傳輸線特性阻抗下，大幅降低訊號傳輸之相位速度，亦即大幅降低波長，可縮短70%以上傳輸線長度，亦即減少佔用晶片面積。此外，波長的縮短，亦使得單位波長之損耗大幅降，而使得本設計之傳輸線可用來實現小面積、高品質之電路。

此新式傳輸線為一週期性結構，藉由調整週期結構單元，可改變傳輸線截止頻率，故傳輸線本身即可用來設計低通濾波器。此外，本文利用此新式傳輸線設計一40GHz電容耦合共振帶通濾波器，特點在小面積、小基板損耗、及適用於標準CMOS製程，其佔用面積僅有 72*400um^2，最小介入損耗(Insertion Loss)為1.4dB，和目前所發表之濾波器比較面積大幅縮小，品質亦顯著提升，更因不需任何後製程而節省了製造成本。

High Slow-Wave-Factor Coplanar Stripline in CMOS Technology and Its Application to Filter Design

Student: Hung-Ta Tso Advisor: Prof. Chien-Nan Kuo

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ABSTRACT

This thesis presents a novel transmission line— high slow-wave-factor coplanar stripline (HS-CPS) and exploits the new structure to filter applications.

In the HS-CPS structure, the distributive inductance and the distributive capacitance per unit length are enhanced simultaneously and consequently the slow-wave characteristic can be increased significantly, while the characteristic impedance can be remained the same. The wavelength reduction of above 70% in the HS-CPS indicates the above 70% occupied area can be saved as compared with the conventional coplanar stripline. In addition, the total attenuation decreases as the length is reduced.

The HS-CPS consists of several identical cells, and the cell length determines the cutoff frequency. Therefore, a lowpass filter can be realized simply utilizing the HS-CPS itself. For further application, a 40GHz capacitive coupled one-resonator bandpass filter has been designed and fabricated utilizing the HS-CPS. This bandpass filter features in small size, low substrate loss, and suiting for standard CMOS

technology. The occupied area and minimum insertion loss are 72*400um^2 and 1.4dB respectively. As compared with the other presented on-chip filters, it is extremely a cheap, miniature, and high-performance solution.

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首先我要感謝我的指導教授郭建男博士二年前願意收留一個非本科系畢業的學生，並在這二年間耐心的給與指導和鼓勵，老師豐富的學識及治學嚴謹的態度使我獲益良多。

感謝一起建立實驗室的同學們將一間堆滿雜物積滿灰塵的「倉庫」變了做研究的新樂園，專搞笑的可愛鳥逸、整天打電玩的泰國貓、還有只會開帳號的洪英瑞，以及後來才加入任勞任怨的小馬，使得實驗室不用再請工友，只愛辣妹的王柏之為我們單調的研究生活加入多采多姿的聯誼活動，比我還老的馬修讓我降低年紀的壓力。還要感謝可愛的學弟妹，我的專屬小弟岡田、書卷娃娃、傻傻傻強、和實驗室之花仰鵑，大家一起上課、一起做研究、一起出遊、使得實驗室就像一個大家庭。還要感謝傅昶綜學長餓著肚子幫我量測，還量得超準讓我有畢業的機會。

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卓宏達

九十三年一月

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CHAPTER 1

Introduction

1.1 Motivation

As the expanding market of the portable communication, a low cost, high integration, and high performance semiconductors technology is an urgent demand for RF and Microwave circuits design. Fortunately, scaling of Silicon-based CMOS technology offers an opportunity of a highly integrated single-chip solution and the advance of nano-CMOS technology makes it possible to apply for high-frequency applications [1].

Since many passive components are implemented with transmission lines such as resonant tanks, impedance matching networks, signal splitters, balun transformers and filters, a low-loss, compact-size, and easy-fabricated transmission line, or interconnect, in CMOS technology is needed for monolithic components. Unfortunately, typical epi-substrate with a low-resistivity bulk silicon, which is used to improve yield and suppress latch-up, causes significant high frequency losses, and the occupied areas of those components are still extremely large for on-chip implementation.

Therefore, many post-processes have been proposed to minimize Si-substrate loss but those methods increase the cost of fabrication. To reduce the occupied areas of those passive components, several slow-wave structures have been presented. To further shrink the sizes of the passive components and overcome the severe high frequency losses, a novel transmission─ high slow-wave-factor coplanar stripline (HS-CPS) is presented in this thesis. It features in low substrate loss, compact size, and easy fabrication (without any post-processes).

While the high performance transmission line is available, the high performance passive components mentioned previously can be realized. Accordingly, this thesis make efforts in the miniature bandpass filter design since the bandpass filter is an essential components in RF and microwave circuits.

1.2 Thesis Organization

Chapter 2 reviews the basic transmission theory and introduces the 0.18um CMOS process and several popular transmission line structures suited to monolithic integration including microstrip, stripline, coplanar waveguide (CPW), and coplanar stripline (CPS).

Chapter 3 presents the novel HS-CPS structure and the comparison with several previous slow-wave transmission lines. Simulated results of the HS-CPS show that the high slow-wave characteristic and low substrate loss are possible for the novel structure. Moreover, further investigation of the cutoff frequency of the HS-CPS is done and it shows the potential for lowpass filter applications.

Chapter 4 introduces the 40GHz miniature bandpass filters formed with the novel HS-CPS structure. Moreover, the occupied area and the minimum insertion loss are compared with the previous on-chip bandpass filters. Finally, the measured method and results are displayed.

Chapter 5 makes a summary of the thesis and provides some future works about the applications of the HS-CPS circuit.

CHAPTER 2

Monolithic Transmission Lines

In this Chapter, some concepts of transmission lines are reviewed in section 2.1. They are basic but essential to design a high performance monolithic transmission line. Section 2.2 gives some information of the commercial 0.18um CMOS process used in this thesis and shows several popular monolithic transmission lines.

2.1 Transmission Line Theory

Transmission line theory differs from circuit theory in one essential feature—electrical wavelength. While circuit analysis assumes the physical dimensions of a network are very much smaller than the electrical wavelength, transmission lines are usually a considerable fraction of a wavelength and may even be many wavelengths long. They can't be described by lumped parameters and must be described by circuit parameters which are distributed throughout its length.

2.1.1 Equivalent Circuit

As shown in Fig 2.1, a transmission line is usually described by the equivalent circuit with four parameters:

R= series resistance per unit length, for both conductors, in Ω/m

L= series inductance per unit length, for both conductors, in H/m

G= shunt conductance per unit length, in S/m

C= shunt capacitance per unit length, in F/m

The series inductance L represents the total self-inductor of the two conductors, and the shunt capacitance C is due to the close proximity of the two conductors. The series resistance R represents the resistance due to the finite conductivity of the conductors, and the shunt conductance G is due to dielectric loss in the material between the conductors.

2.1.2 Wave Propagation

From the circuit of Fig. 2.1, Kirchhoff's voltage law and current law can be applied to give

$$v(z,t) - R\Delta z i(z,t) - L\Delta z \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0 \tag{2.1a}$$

and

$$i(z,t) - G\Delta z v(z+\Delta z,t) - c\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} - i(z+\Delta z,t) = 0 \tag{2.1b}$$

respectively. In the limit as $\Delta z \to 0$, the following general transmission-line equations can be given:

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t} \tag{2.2a}$$

$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t} \quad . \tag{2.2b}$$

For the sinusoidal steady-state condition, with cosine-based phasors, (2.2a, b) become time-harmonic transmission-line equations:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.3a}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2.3b}$$

The coupled time-harmonic transmission-line equations, (2.3 a, b) can be combined to

solve for $V(z)$ and $I(z)$:

$$\frac{d^2V(z)}{dz^2} = \gamma^2 V(z) \tag{2.4a}$$

$$\frac{d^2I(z)}{dz^2} = \gamma^2 I(z) \tag{2.4b}$$

where $\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$ (2.5)

is the propagation constant whose real and imaginary parts, α and β, are the attenuation constant and phase constant of the line, respectively.

The solutions of (2.4a, b) are

$$V(z) = V_o^+ e^{-\gamma z} + V_0^- e^{rz} \tag{2.6a}$$

$$I(z) = I_o^+ e^{-\gamma z} + I_0^- e^{rz} \tag{2.6b}$$

where the $e^{-\gamma z}$ term represents wave propagation in the $+z$ direction, and the $e^{\gamma z}$ term represents wave propagation in the $-z$ direction. Applying (2.3a) to the voltage of (2.6a) gives the current on the line:

$$I(z) = \frac{\gamma}{R + j\omega L}[V_o^+ e^{-\gamma z} - V_0^- e^{rz}]$$

Comparison with (2.6b) shows the characteristic impedance, Z_0, can be defined as

$$Z_0 = \frac{V_o^+}{I_o^+} = \frac{-V_o^-}{I_o^-} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.7}$$

In the lossless line ($R = G = 0$), the characteristic impedance of (2.7) reduces to

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.8}$$

Propagation constant and phase velocity can be given as

$$\gamma = \alpha + j\beta = j\omega\sqrt{LC} \qquad (\alpha = 0, \beta = \omega\sqrt{LC})$$

$$v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}}$$

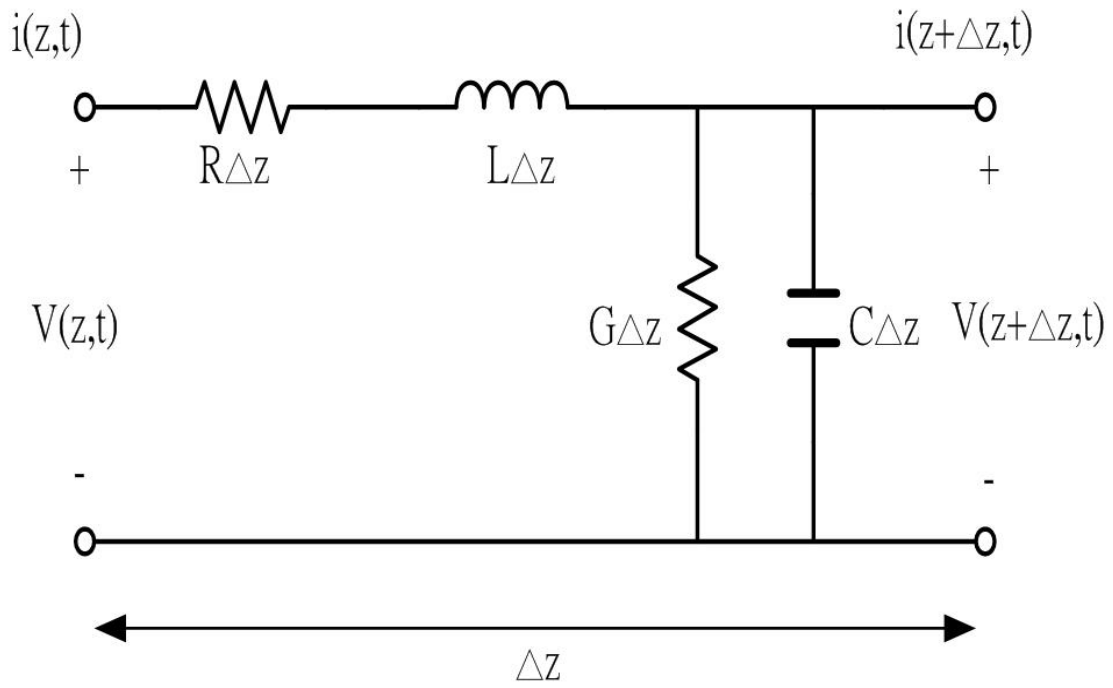


Fig. 2.1 Equivalent circuit of an incremental length of transmission line.

2.2 Monolithic Transmission Lines

With the operating frequencies rising to several tens of gigahertz, the monolithic transmission line becomes an attractive topic. A variety of monolithic transmission lines have been presented and investigated in a few decades [2]. Accordingly, the accurate modeling of transmission lines helps designers predict the performance of high frequency circuits and furthermore allow them to invent a useful component.

Before the investigation of monolithic transmission lines, it is necessary to review the back end of 0.18um CMOS process.

2.2.1 0.18um CMOS Process

As depicted in Fig. 2.2 for a 0.18um generation, the process provides a polysilicon layer for the gates of MOS and six metal layers (M1~M6) for interconnect. Each of the first five metal layers has a thickness of about 0.5um. The thicker top metal layer (M6) with lower sheet resistance can be used to form the spiral inductors. The metals are separated by dielectrics of the dielectric constant, ε_r, of about 4. A special metal layer (CTM) between the M6 and M5 is only used for Metal-Insulator-Metal (MIM) capacitor of unit capacitance of about 1fF/um^2. The Si-substrate resistivity is about 10 Ω-cm.

2.2.2 Microstrip, Stripline, Coplanar Waveguide, and Coplanar Stripline.

Microstrip, stripline, CPW, and CPS are four popular monolithic transmission lines. In this section, both of them are reviewed and the performance limitations in 0.18um CMOS process are mentioned.

The geometry and the field lines of the microstrip line is shown in Fig. 2.3. It is composed of a conductor of width W and an infinite conductor plane, separated by a dielectric sheet with dielectric constant, ε_r. Because the dielectric does not fill the air region above the strip, the microstrip line cannot support a pure TEM wave. However, the fields are quasi-TEM wave. In other words, the fields are essentially the same as those of the static case. Therefore, good approximations can be obtained from static solutions.

Unfortunately, the presence of the Si-substrate in the CMOS process complicates the behavior and analysis of microstrip line. Illustrated in Fig 2.4(a), the

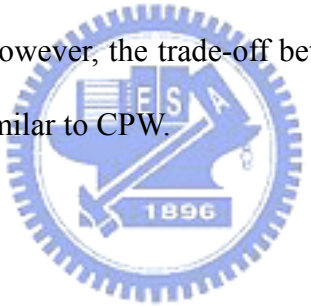
properties of microstrip line on Si-SiO_2 system**,** named metal-insulator-semiconductor (MIS) microstrip line, were investigated a few decades ago [3], it exhibits three types of fundamental modes and the condition for the appearance of each mode. The wavelength depends on the operating frequency, substrate resistivity and the dielectric constant. In the slow-wave mode, signal propagates very slowly or the slow-wave factor is very high. Unfortunately signal attenuation in this mode is very high as well. In the dielectric mode, wave velocity and wavelength are simply inversely proportional to the square root of the effective relative dielectric permittivity of the transmission line. On the standard CMOS process Si-substrate, a slow-wave mode propagates at low frequencies. As frequency is increased, a quasi-TEM mode propagates. It is a pity that both of them suffer from severe attenuation due to the low resistivity of the Si-substrate.

Microstrip also can be formed by the top metal (M6) and the first metal (M1) layers, as illustrated in Fig. 2.4(b). The first metal layer prevents the energy from penetrating into the Si-substrate and eliminates the severe attenuation results from substrate loss. However, because the thickness of the dielectric between M6 and M1 is only about 6 um, the capacitance per unit length of the line is large resulting in low characteristic impedance. It can be overcome by shrinking the width of the strip but the series resistance will increase.

Another structure is the stripline configuration, depicted in Fig.2.5. It is similar to the coaxial transmission line. The signal line is realized in an intermediate metal layer and shielded by reference ground planes in M1 and M6 and vertical walls in stacked vias. Since the reference ground is around the signal strip with smaller distance than the microstrip, the capacitance per unit length of the stripline is larger indicating lower characteristic impedance compared with the microstrip line.

The physical realization of a monolithic coplanar waveguide (CPW) is indicated in Fig. 2.6. It consists of a center signal strip and two wide reference ground planes both in M6. Since the space between the signal strip and reference ground planes is adjustable, the capacitance per unit length can be smaller than the microstrip and stripline by increasing the space. In other words, the characteristic impedance of the CPW can be enlarged. Unfortunately, as seen in Fig.2.6, the more the space increase, the more E-field couples to the Si-substrate and then the more signal energy dissipates in the lossy substrate [1].

Another coplanar transmission line is coplanar stripline (CPS), which consists of two identical strips in M6 as shown in Fig. 2.7. Comparing with CPW structure, it is suitable for differential circuit design due to its balance configuration and saves a great deal of occupied area. However, the trade-off between characteristic impedance and substrate loss in CPS is similar to CPW.



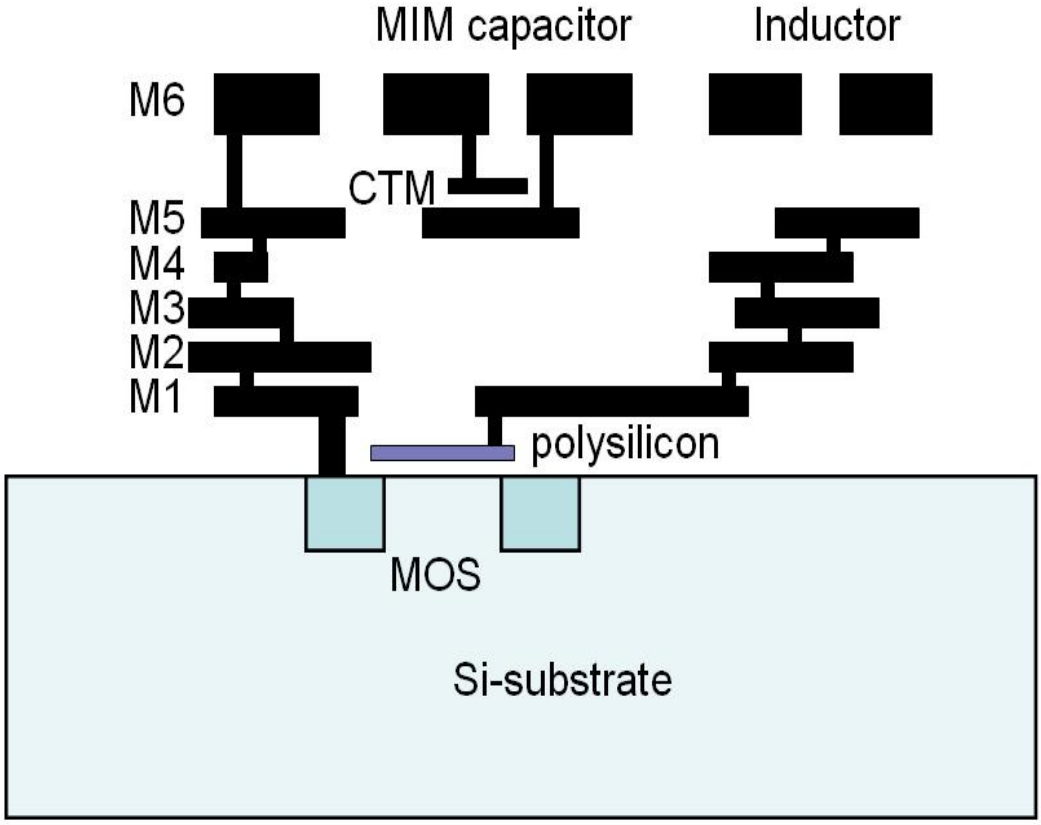


Fig. 2.2 The cross-section of the 0.18um CMOS process.

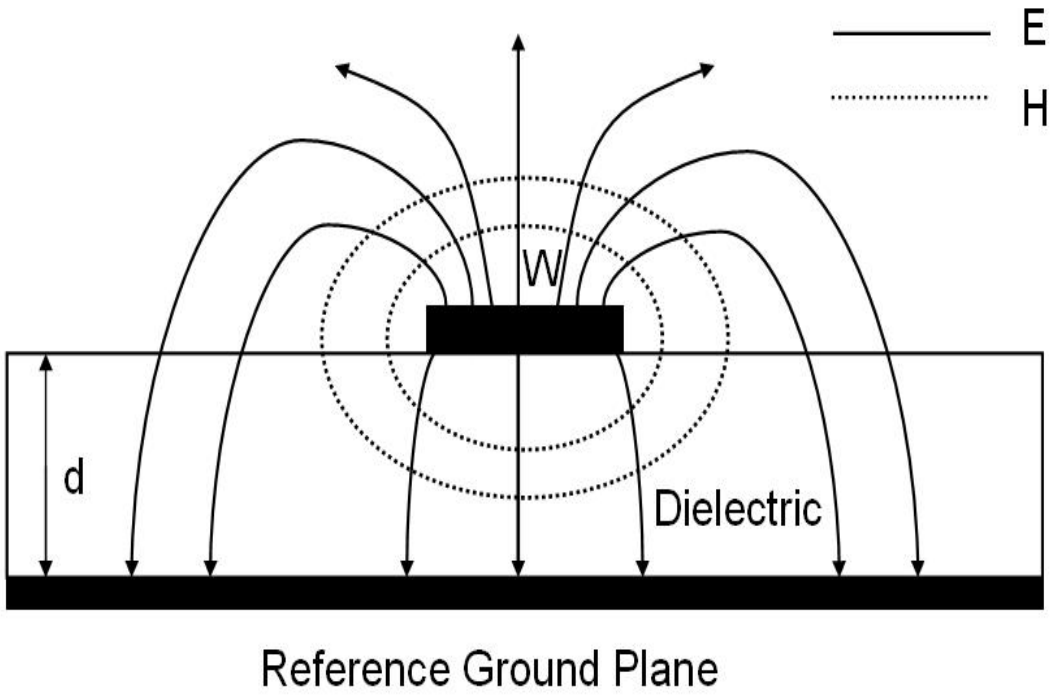
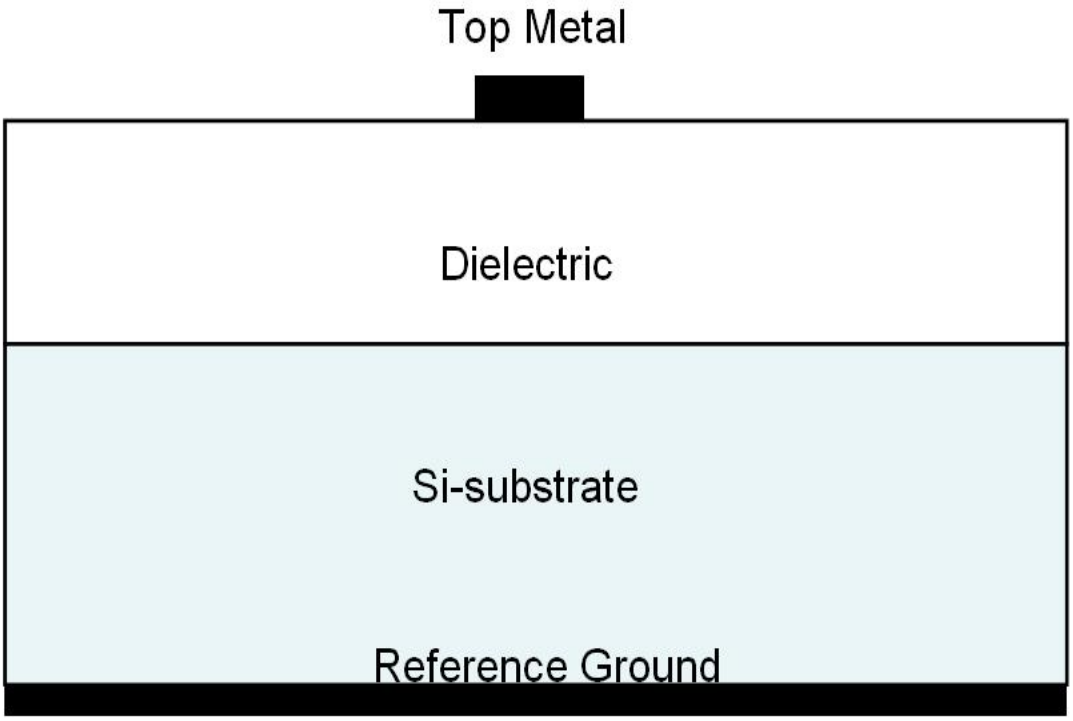
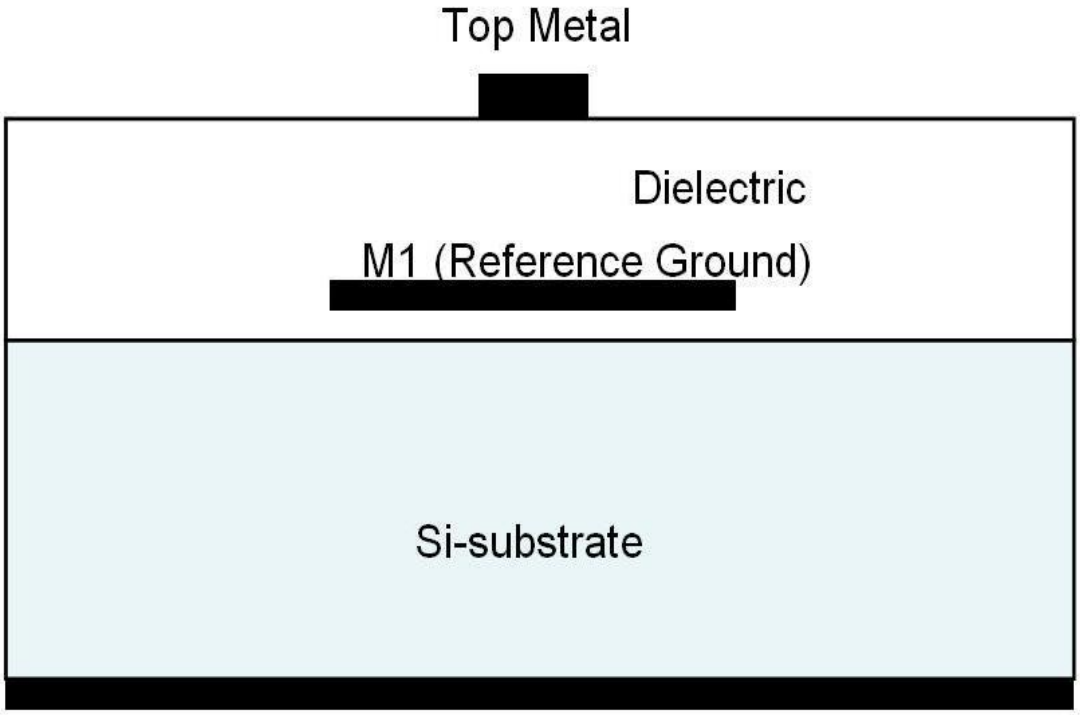


Fig. 2.3 Geometry and field lines of the microstrip



(a)



(b)

Fig. 2.4 Geometry of (a) the MIS microstrip line and (b) the microstrip line with M1 ground shield.

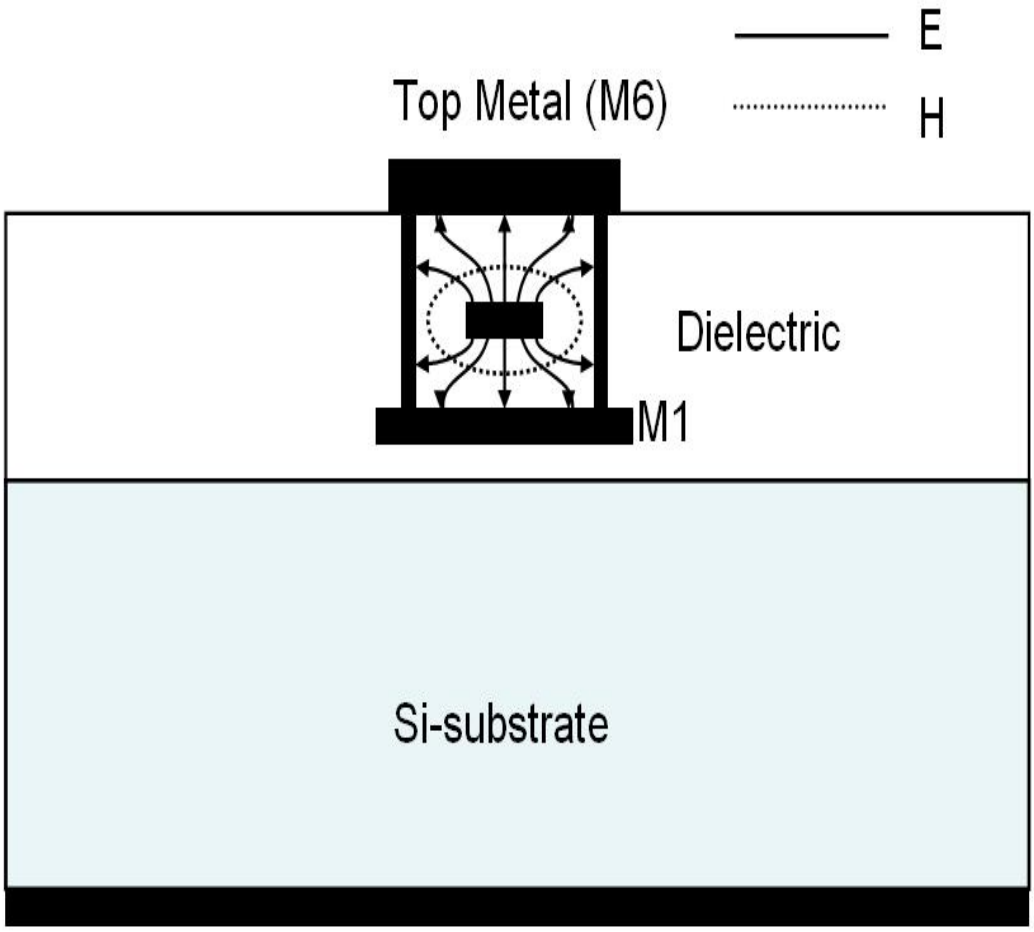
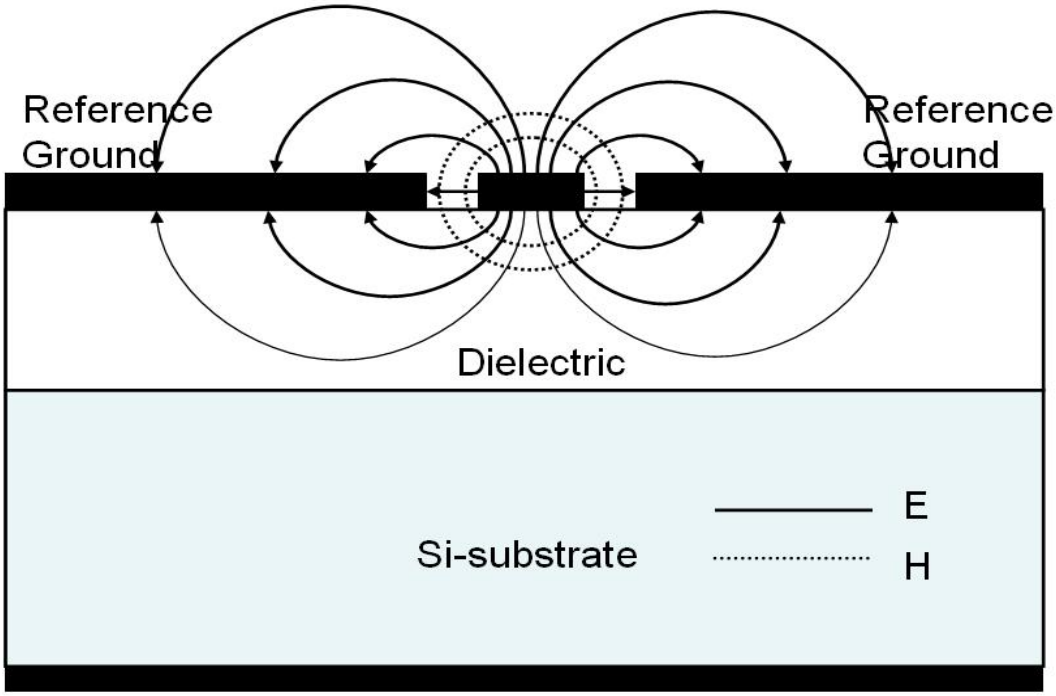
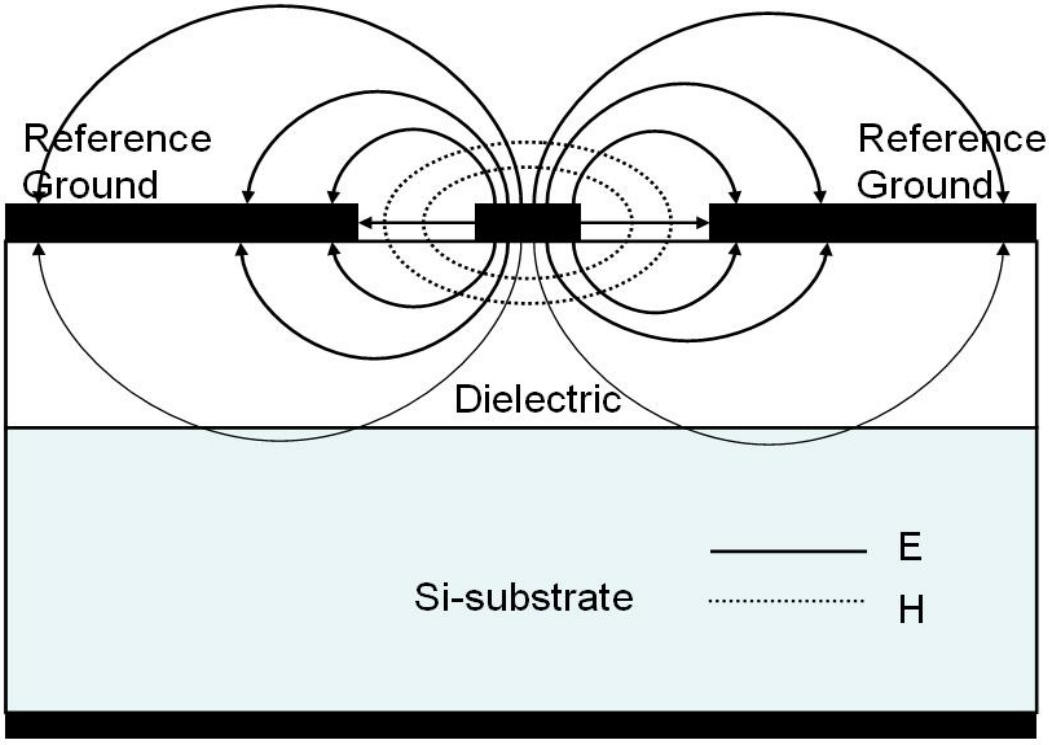


Fig. 2.5 Geometry and field lines of the monolithic stripline



(a)



(b)

Fig. 2.6 Geometry and field lines of the (a) small space and (b) large space monolithic CPW

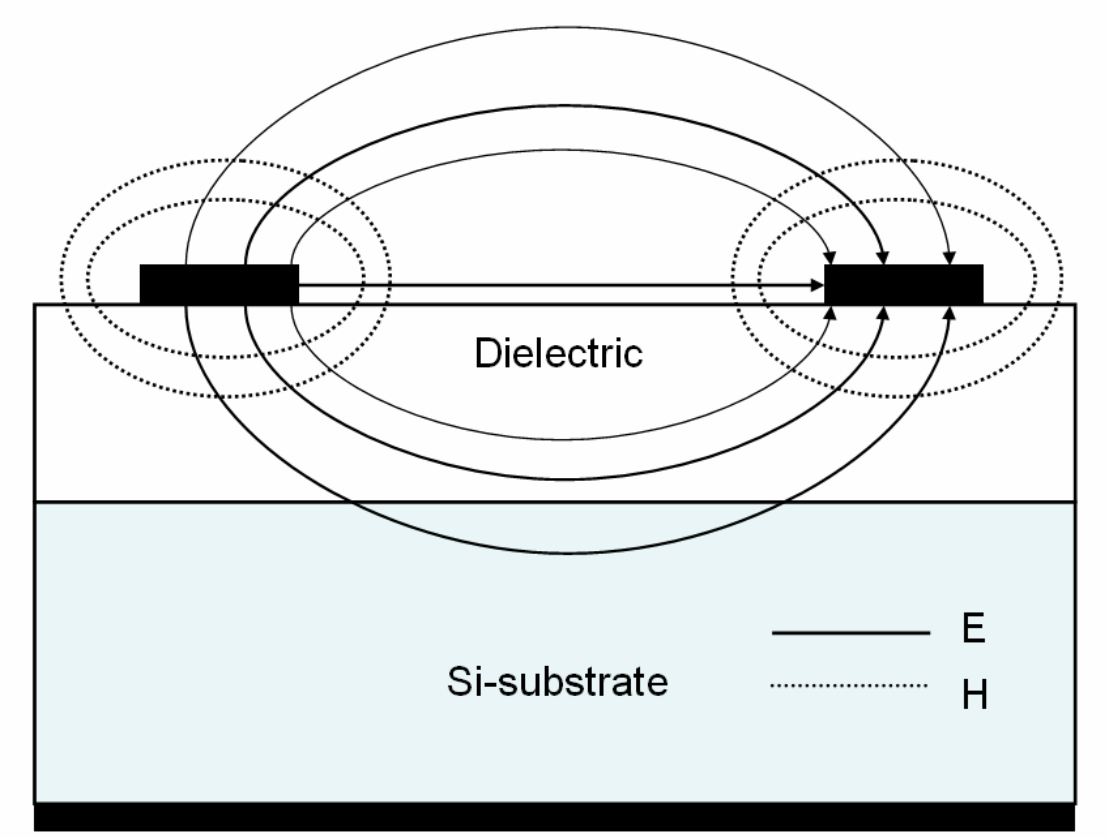
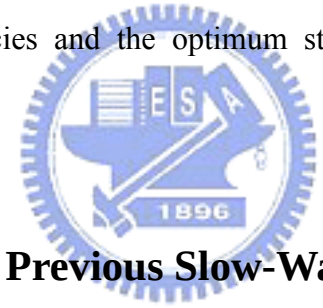


Fig. 2.7 Geometry and field lines of the monolithic CPS

CHAPTER 3

High Slow-Wave-Factor Coplanar Stripline (HS-CPS)

In this chapter, an on-chip interconnect of HS-CPS on the standard 0.18um CMOS process Silicon-based low-resistivity substrate is realized using the structure of coplanar striplines. With MIM capacitors distributed along the striplines, signal propagation reaches a high slow-wave factor, which is demonstrated to be 3.5 times larger than that of conventional coplanar striplines over a wide frequency range. The occupied area can be therefore greatly reduced. It is further found that the transmission loss is minimized, mainly due to metal loss rather than substrate loss. Finally, the cut-off frequencies and the optimum strip width of the HS-CPS are investigated.



3.1 Introduction and Previous Slow-Wave Transmission Lines

Scaling of Silicon-based CMOS technology offers an opportunity of a highly integrated single-chip solution. The advance of CMOS technology makes it possible to apply for high-frequency applications. On-chip passive components, such as filters and resonators, however, still require further effort to minimize the size for cost concern. To do so, it needs to reduce the effective wavelength of signal propagation in a standard CMOS structure.

An on-chip interconnects, or transmission lines, can be simply implemented by a top conductor over dielectric, silicon substrate and ground plane, namely a metal-insulator-semiconductor (MIS) microstrip line [3].The wavelength depends on

the operating frequency, substrate resistivity and the dielectric constant. Three fundamental propagation modes exist in such a structure. In the slow-wave mode, signal propagates very slowly or the slow-wave factor is very high. Unfortunately signal attenuation in this mode is very high as well. In the dielectric mode, wave velocity and wavelength are simply inversely proportional to the square root of the effective relative dielectric permittivity of the transmission line. To compromise signal attenuation and to decrease the wavelength, periodic ground plane microstrip [4] and electric-magnetic-electric (EME) microstrip line [5] were developed for enhancement of the slow-wave characteristic. Typically microstrip structures yield to high signal attenuation due to significant portion of energy propagating in the lossy substrate. As the operating frequency moves to higher, the attenuation becomes higher.

This issue of substrate loss can be alleviated by the configuration of uniplanar transmission lines, such as coplanar waveguide (CPW) and coplanar stripline (CPS) [6] structures, which are also easy for solid-state device integration. For hybrid-circuit implementation, miniature periodic-structure CPW [7] has been proposed for filter applications in less area. On-chip implementation can actually make use of multi-layer configuration. As such, a slow-wave CPW (S-CPW) structure was presented, consisting of CPW top conductors and a second layer of floating metal strips [8]. This S-CPW design overcomes many of the limitations of existing design that the on-chip wavelength of MIS and CPW structures is about one-half of the free-space wavelength for Silicon-based processes. Slow-wave performance of these structures is summarized in Table 3.1.

In this Chapter, a novel high-slow-wave-factor coplanar stripline (HS-CPS) is presented. As compared to CPW lines, the CPS structure, as shown in Fig.3.1 (a), is a better choice for balanced circuit design. It is also simple for implementation of open-

or short-ended stubs. The HS-CPS features in small size, low substrate loss, and easy fabrication (by standard process). To the best knowledge of the author, the slow-wave factor achieves to a value much higher than those in previous work, and the attenuation is small enough for practical applications.

Table 3.1 Summary of slow-wave performance.

	structure	slow-wave factor	attenuation (dB/ λ)	Configuration width
[3]	MIS microstrip (on-chip)	15 (0.03-4GHz)	15 (at 4G)	160um
[4]	periodic ground plane microstrip	3-7 (0.5-8.5GHz)	----	25mil
[5]	(EME) microstrip	2.5-3 (0.5-7GHz)	0.48 (at5GHz)	4.268mm
[7]	periodic-structure CPW	3.5-4.1 (0.5-8.5GHz)	----	55mil+ground width*2
[8]	S-CPW (on-chip)	4.5-4.7 (1-40GHz)	1 (at20GHz)	420um
This work	**HS-CPS (on-chip)**	**7.1-7.5 (1-30GHz)**	**1.61 (at20GHz)**	**72um**

3.2 Design Principles and Considerations

3.2.1 Enhancement of Slow-Wave Propagation

From the transmission-line theory, the propagation constant and phase velocity of a lossless transmission line are given as $\beta = \omega\sqrt{LC}$ and $v_p = 1/\sqrt{LC}$, respectively, where L and C are the inductance and capacitance per unit length along the transmission line. Thus, increasing the values of L and C can reduce the phase velocity and therefore effectively enhance slow-wave propagation.

Consider an on-chip CPS as shown in Fig.3.1 (a), realized by two top conductors as a differential signal path on the same metal layer. Similar to those approaches in [7], there are several modifications to the CPS structure to enhance the slow-wave characteristic. The effective inductance can be enlarged by increasing the space and decreasing the widths of the two strips, while the effective capacitance can be increased by branching out the strips. Larger space between two conductors essentially corresponds to larger magnetic flux in the current loop formed by the two conductors. A narrower width results in higher line impedance or a more inductive transmission line. Branching strips produce higher capacitive coupling between the two conductors.

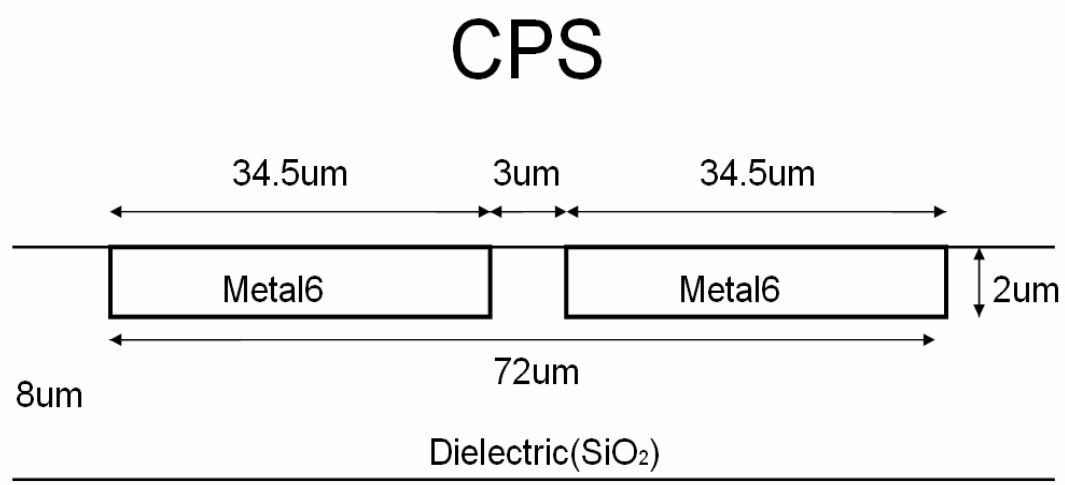
In the proposed HS-CPS structure, capacitive coupling is further enhanced by MIM capacitors available in standard processes. The capacitance of a MIM capacitor can be adjusted quite arbitrarily and the value is much larger than that per unit length in a conventional CPS line, and that of capacitive coupling in branching strips. Thus, MIM capacitors, placed underneath the branches, enable much more capacitive coupling. Moreover, these MIM capacitors introduce no extra area since they are located in a different layer from the top conductors. The new structure is depicted in

Fig. 3.1 (b) and (c), where all the aforementioned improvements are realized in a cell unit, which is placed periodically along the line. The inductance and capacitance per unit length are consequently increased.

3.2.2 Losses in HS-CPS

In the HS-CPS configuration, the issue of substrate loss is insignificant. As can be seen from simulations, signal energy is strongly confined near the region of MIM capacitors. Only a fraction of energy leaks into the substrate. Newer generations of nano-CMOS technology will help improve this issue as the thickness of the dielectric layer becomes thicker and the top conductor layer is more distant from the substrate.

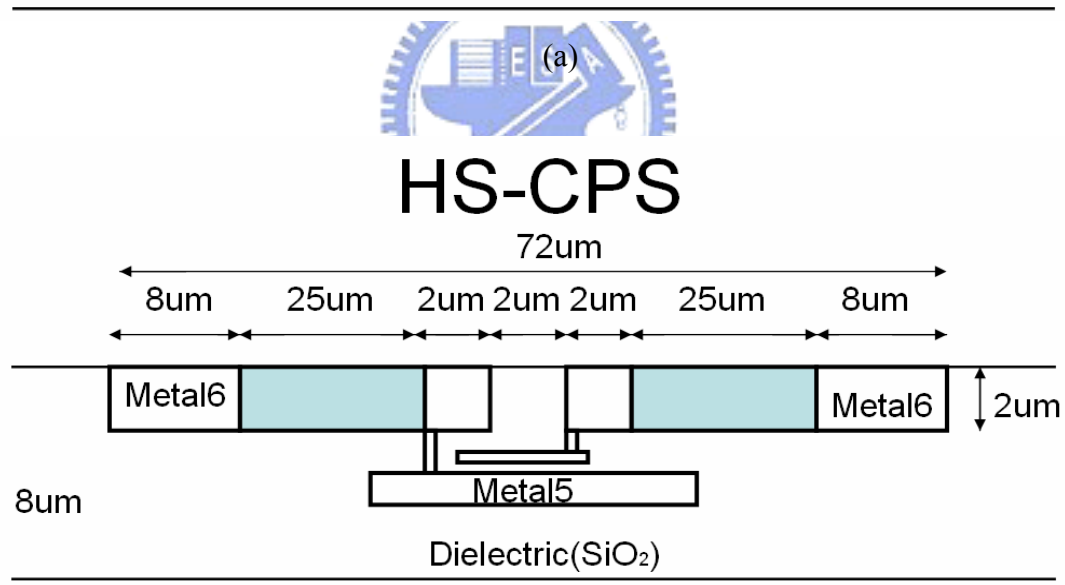
On the other hand, signal attenuation mainly arises from the resistivity due to non-ideal top conductors and the discontinuity due to placement of MIM capacitors. The impact of the discontinuity can be minimized by using small value of numerous MIM capacitors placed closely and uniformly along the transmission line. As to the former issue of metal loss, it is a trade-off between substrate loss and the effective line resistance. Theoretically wider strips produce less resistivity. Nevertheless it is limited by the skin effect and the factor that more energy coupling into the substrate occurs. A narrow width is preferred for the reason of a higher inductance per unit length, but the effective resistance per unit length may also become larger. As a result, the conductor width needs to be optimized. The trade-off will be relaxed in newer generations of nano-CMOS technology as the top conductor becomes thicker and higher conductivity of metal can be used.



450um

Substrate(Si)

(a)



450um

Substrate(Si)

(b)

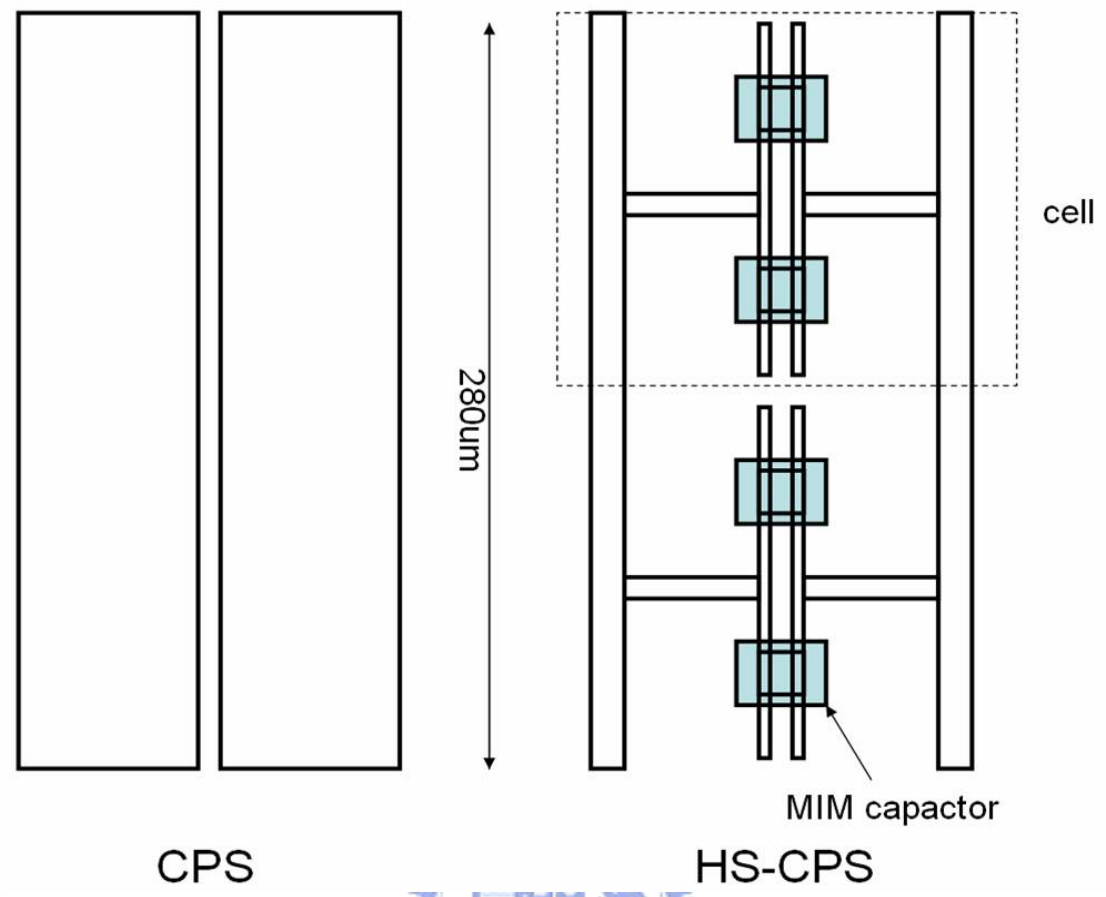


Fig. 3.1. On-chip CPS transmission lines. Cross-sectional view of (a) the conventional CPS and (b) HS-CPS, and (c) Top view of the conventional CPS and HS-CPS

3.3 Simulation Results

The 3-D EM simulation software of Ansoft HFSS is used to extract the S-parameters in all the configurations, and then other electrical parameters can be obtained.

3.3.1 Simulation Results

Three configurations are under consideration, the CPS, the HS-CPS, and the

HS-CPS with perfect conductors. The CPS and HS-CPS are both designed for characteristic impedance Z_o of about 50Ω. In the simulations, the length of a transmission line is chosen as 280um.

A 0.18um CMOS process is assumed. The top conductor is with a thickness of about 2um and the conductivity σ of about 2.8e7 S/m. The bottom layer of MIM capacitors is labeled as "Metal5". The thickness of SiO_2 layer is about 8um. The dimensions of each configuration are depicted in Fig. 3.1 (a), (b) and (c). The CPS line consists of two 34.5um–wide strips separated by 3um gap. The strip width in the HS-CPS line is chosen as 8um. Four MIM capacitors, each of 16fF, are uniformly distributed in two cells, as illustrated in Fig. 3.1(c). The total widths of the entire configuration for the CPS and the HS-CPS are the same as 72um. In the simulation case for the HS-CPS with perfect conductors, all the metal is set as ideal.

The characteristic impedances of all configurations are plotted in Fig. 3.2. From the phase information of S-parameters, the effective relative dielectric constant ε_{eff} is calculated and plotted in Fig. 3.3 (a). The slow-wave factor, defined as $\sqrt{\varepsilon_{eff}}$ based on $v_p = c / \sqrt{\varepsilon_{eff}}$, is shown in Fig. 3.3 (b). The HS-CPS reaches a high slow-wave factor of 7.1 at 20 GHz, which is 3.5 times larger than that of the conventional CPS, indicating great wavelength reduction. Thus, an on-chip $\lambda/4$ CPS line at 20 GHz reduces in size from 1.88 to 0.53 mm when using the HS-CPS configuration.

Fig. 3.4 (a), (b) show the attenuation per mm and per wavelength of all configurations respectively. Using the HS-CPS, the attenuation at 20GHz is improved from 5.51 to 1.61 dB/λ. The improvement is for the reason that total attenuation in a transmission line decreases as the effective wavelength is greatly reduced. In the

HS-CPS line, metal loss dominates the total loss. It can be verified by the case with perfect conductors. The attenuation of the HS-CPS with perfect conductor drops down to be less than 1dB per wavelength, as shown in Fig. 3.4(b). The results indicate that signal attenuation due to substrate loss and discontinuity of MIM capacitors is insignificant. Fig. 3.5 (a), (b) show the electric field distribution of CPS and HS-CPS respectively. Due to the relative large capacitance of MIM capacitors, the electric field in HS-CPS is mostly confined near the region of MIM capacitors, while it can be seen that more energy couples into Si-substrate in CPS. Performance of the HS-CPS is summarized and compared to previous work in Table 3.1.

3.3.2 Investigation of Cut-off Frequency

In order to investigate the cut-off frequencies of the HS-CPS structures, two two-cells HS-CPS structures of 190um and 380um unit cell length respectively, and a three-cells HS-CPS structure of 190um unit cell length, as illustrated in Fig.3.6 (a), (b), (c) are simulated. Each of them has the same cross-sectional view as shown in Fig.3.1(b), and the same MIM capacitors, each of 21.16fF, per unit length. The S-parameters and slow-wave factors are shown in Fig.3.7. Similar to [7], The cut-off frequency for the unit cell length, l, can be estimated as:

$$f_c = \frac{c_0}{4 \times l \times S.F.} \tag{3.1}$$

where the c_0 is the velocity of light in vacuum and the $S.F.$ is the slow-wave factor of the HS-CPS structure. Comparing the two-cells HS-CPS of 190um cell length with the three-cells one, it is obviously that sharper rolloff can be accomplished simply by inserting more cells, while the cut-off frequency can be determined by the cell length. Therefore, a lowpass filter can be design.

3.3.3 Optimization for Attenuation per Wavelength

The strip width of the HS-CPS can be further reduced and the capacitance of MIM capacitors can be increased for higher inductance and capacitance per unit length along the HS-CPS. Therefore, the slow-wave factor can reach a much higher value. However, as the strip width shrinks, the series resistance of the HS-CPS goes up resulting in severer attenuation per unit length. In other words, the trade-off is between slow-wave factor and attenuation per unit length.

In order to find the optimal strip width, another two HS-CPS structures of different strip widths, 3um and 13um, depicted in Fig. 3.8(a), (b), are investigated. For the same characteristic impedances, 50Ω, MIM capacitors of different capacitance, 30.25fF and 12.25fF, are used in the two HS-CPS structures respectively.

Through the simulator, Ansoft HFSS, slow-wave factors, attenuations per mm, and attenuations per wavelength of the three 50Ω HS-CPS of different strip widths, 3um, 8um, 13 um, are given in Fig.3.9 (a), (b), and (c). As shown in Fig.3.9 (a), (b), although the slow-wave-factor of the HS-CPS of 3um strip width can reach the highest value about 9, unfortunately, the aggravation of attenuation per mm is the severest simultaneously due to the highest series resistance of the narrowest strip width. The HS-CPS of 13um strip width has the least attenuation per mm, however, the slow-wave factor is the lowest. Since the trade-off is between slow-wave factor and attenuation per unit length, the attenuation per wavelength is a fair criterion for optimal strip width. According to the attenuations per wavelength, as demonstrated in Fig.3.9 (c), both the structures of 13um strip width and 8um strip width are better choices than that of 3um strip width. Since the attenuation per wavelength of the HS-CPS of 8um strip width is almost the same as that of 13um strip width, the 8um

strip width is a better choice than the 13um strip width because of the much higher slow-wave factor. The design flowchart of the HS-CPS is shown in Fig.3.10.

3.3.4 The Effect of the Arrangement of MIM Capacitors

In order to find the effect of the arrangement of MIM capacitors, the performances of two HS-CPS lines of eight 3.25x3.25um^2 MIM capacitors and of two 6.5x6.5um^2 MIM capacitors respectively, shown in Fig.3.11, are compared with the aforementioned HS-CPS of four 4.6x4.6um^2 MIM capacitors. In other words, each HS-CPS has the same total MIM capacitance about 84.5fF but has different arrangement of it.

Simulation results of the slow-wave factor, attenuation per mm, and attenuation per wavelength of the three HS-CPS lines are depicted in Fig.3.12, Fig.3.13, and Fig.3.14. According to above simulation results, there is no significant difference between the three HS-CPS lines. In other words, the effect of the arrangement of the MIM capacitors doesn't matter in this case. A little divergence of the slow-wave factor of the HS-CPS of eight 3.25x3.25um^2 MIM capacitors should result from the fringing capacitance of the MIM capacitance. Under the cases of the same capacitance, the more small MIM capacitors are used, the more fringing capacitance are introduced and results in larger slow-wave factor than expected.

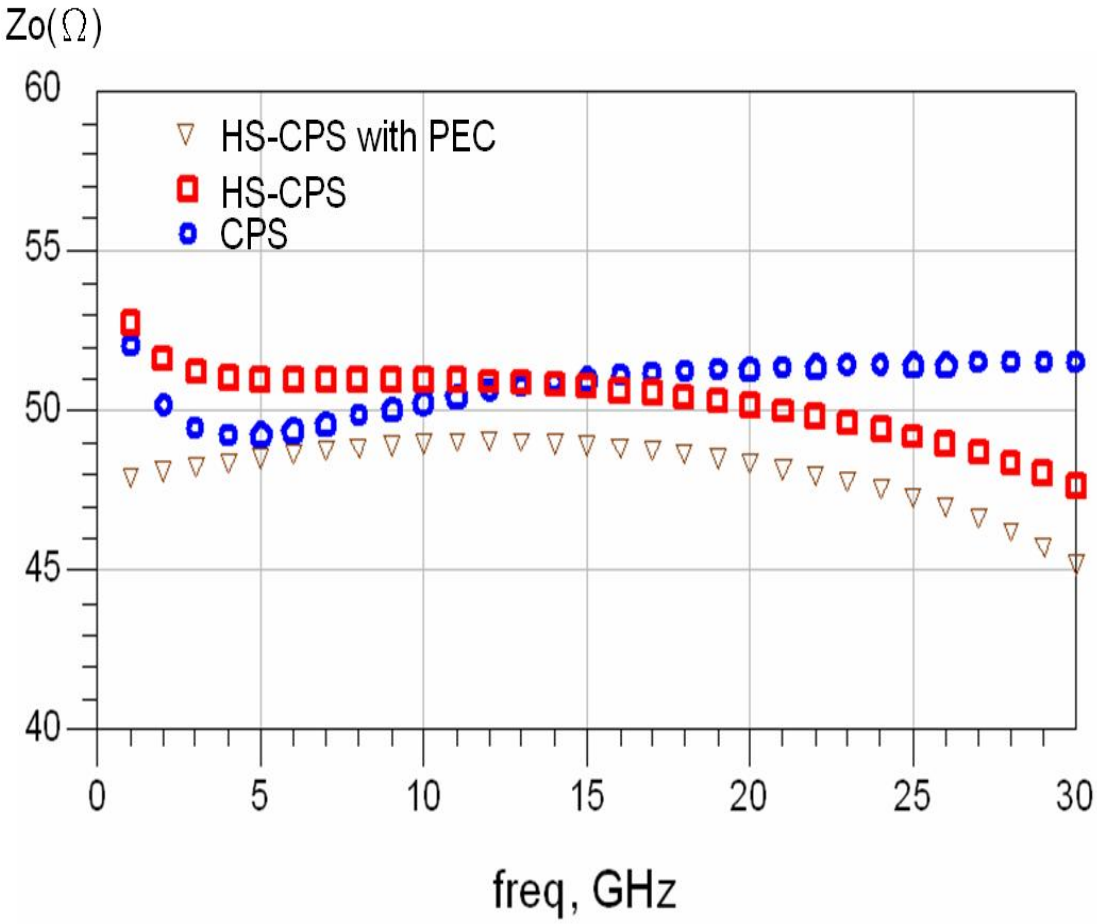
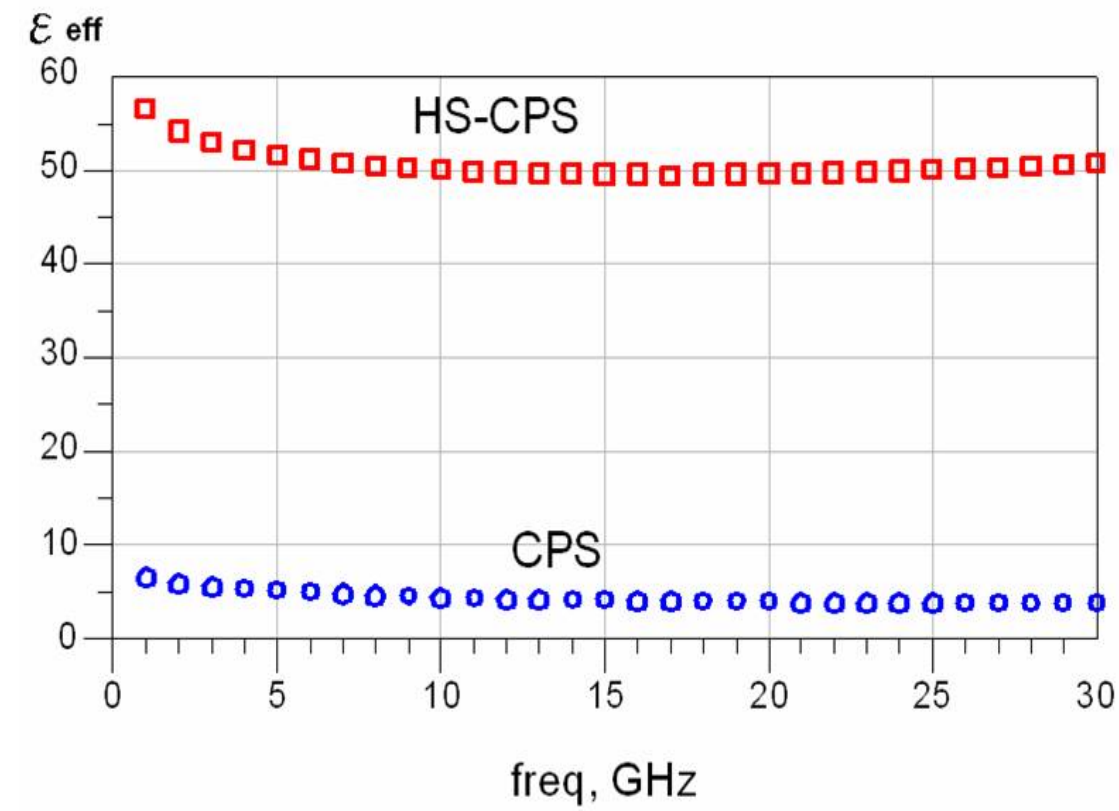
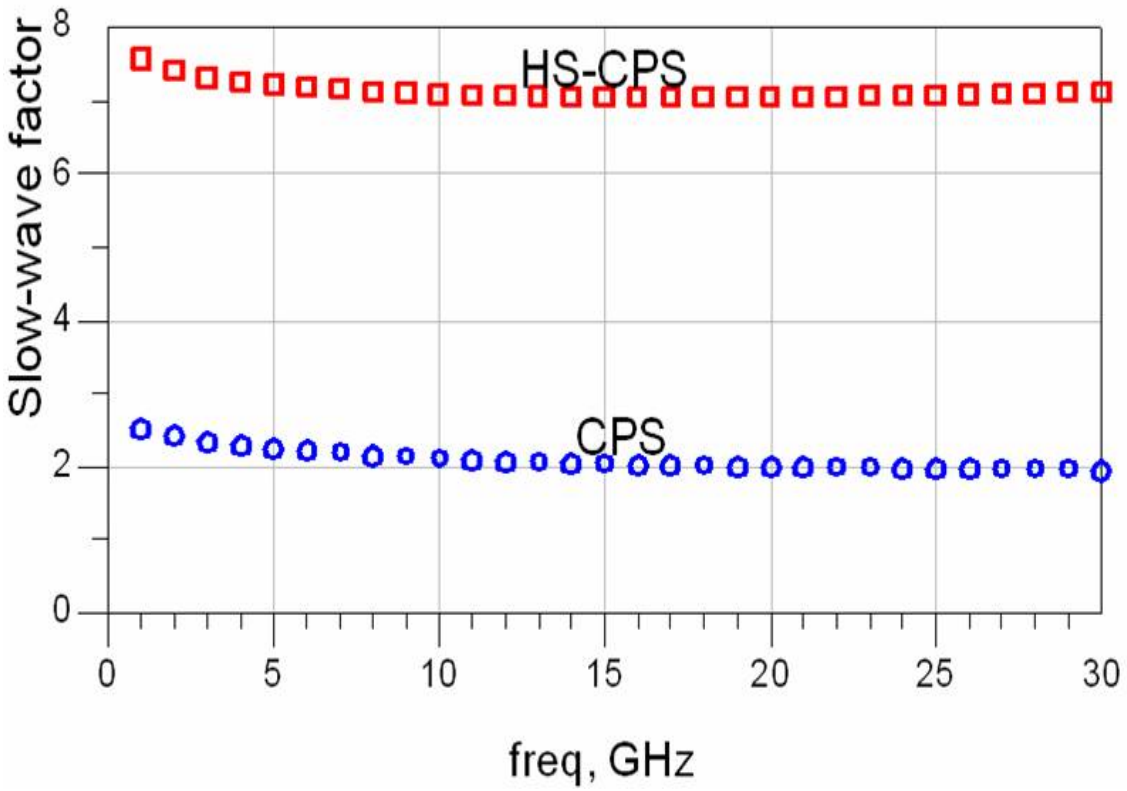


Fig. 3.2 Characteristic impedance (Z_0) of CPS and HS-CPS.

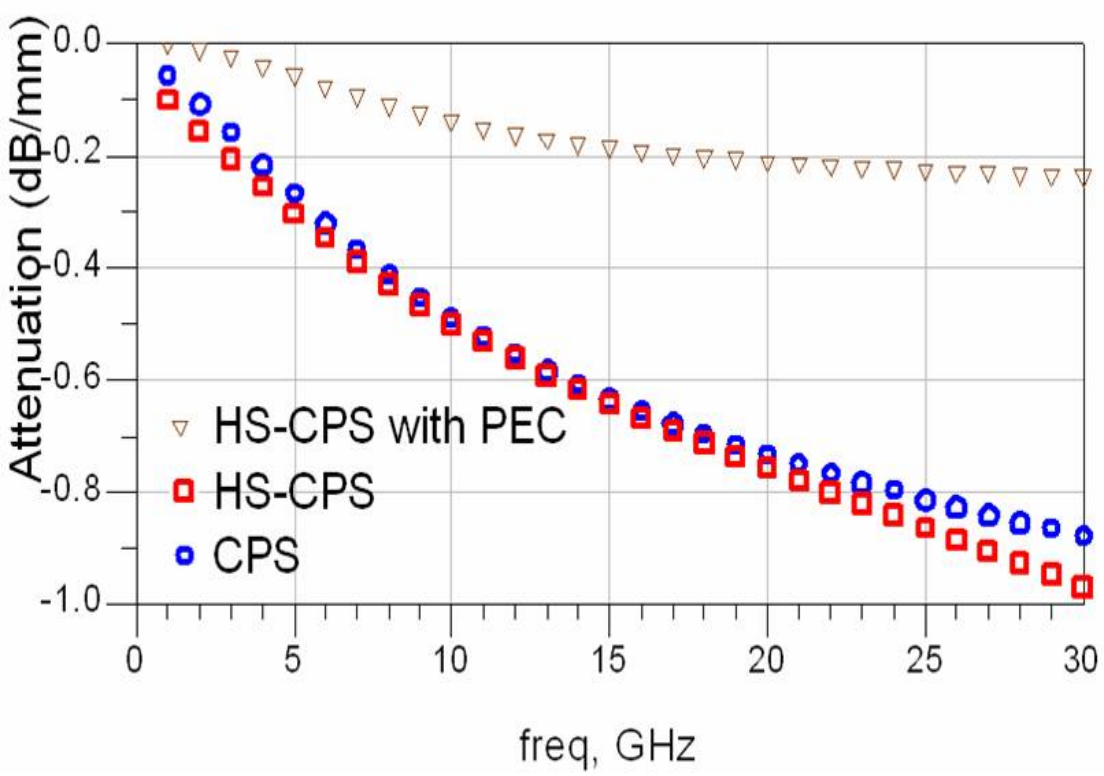


(a)

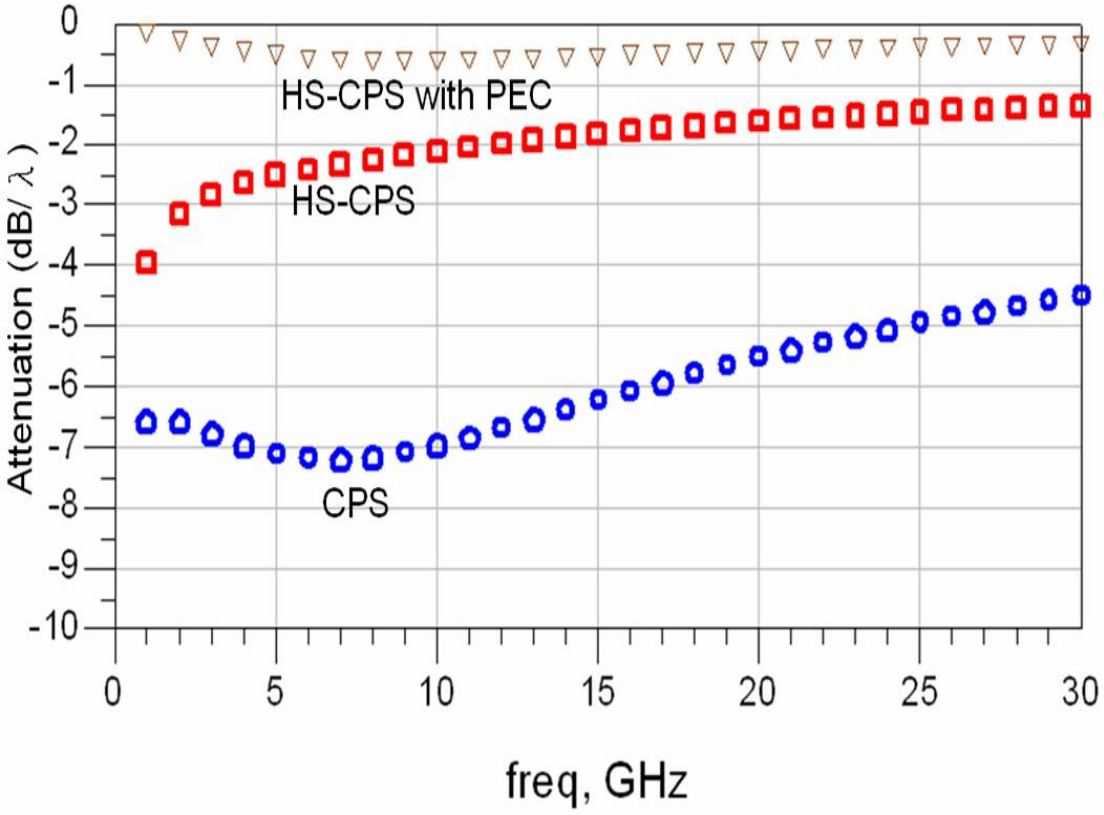


(b)

Fig. 3.3 (a) Effective relative dielectric constants. (b) Slow-wave factors of CPS and HS-CPS

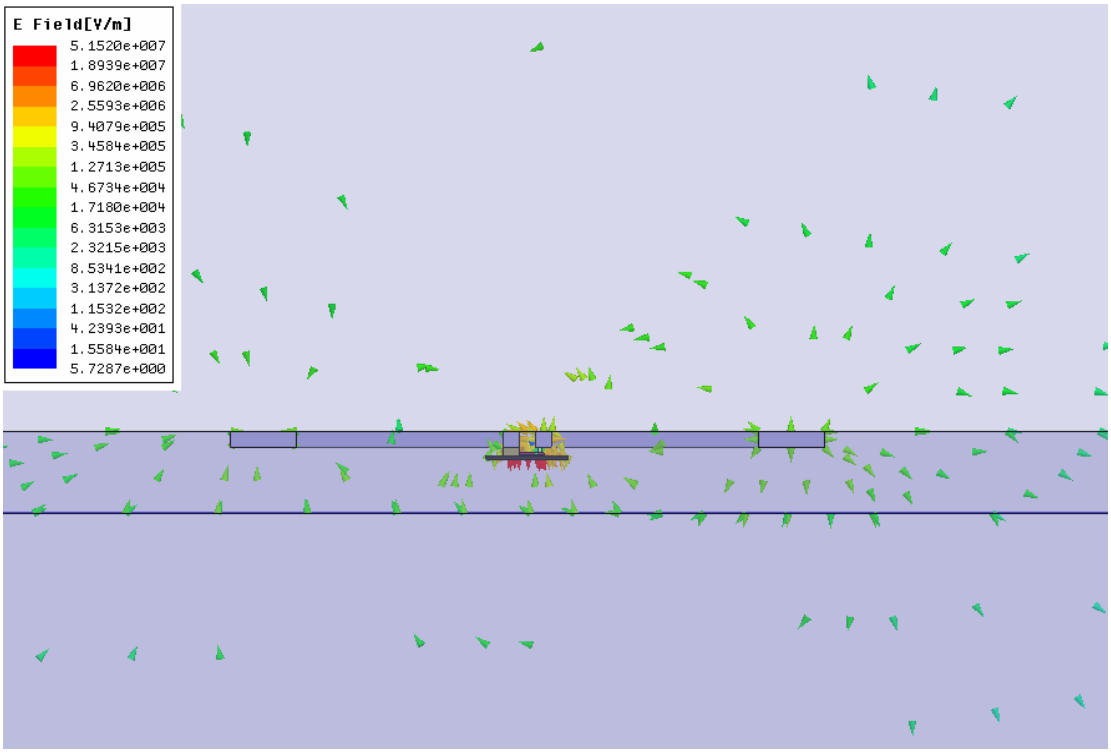


(a)

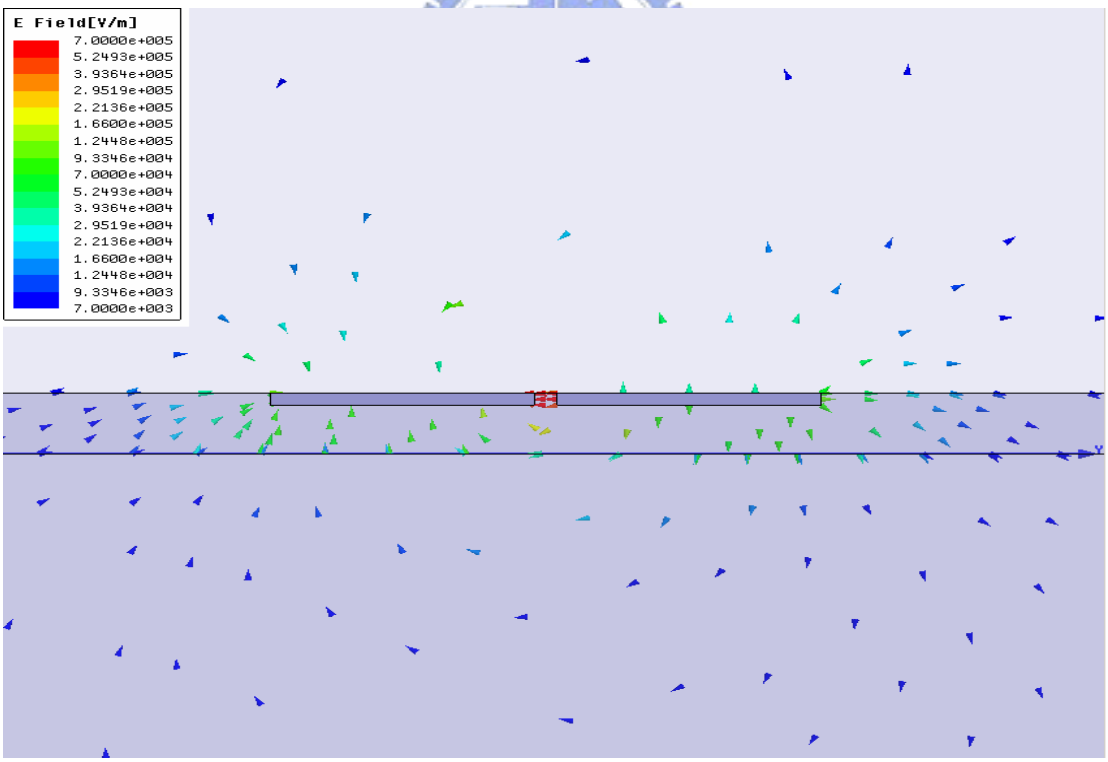


(b)

Fig. 3.4 Attenuation (a) per mm and (b) per wavelength of CPS, HS-CPS, and HS-CPS with perfect conductivity



(a)



(b)

Fig. 3.5 Electric field (a) in CPS couples to Si-substrate (b) in HS-CPS is mostly concentrated in the MIM capacitor

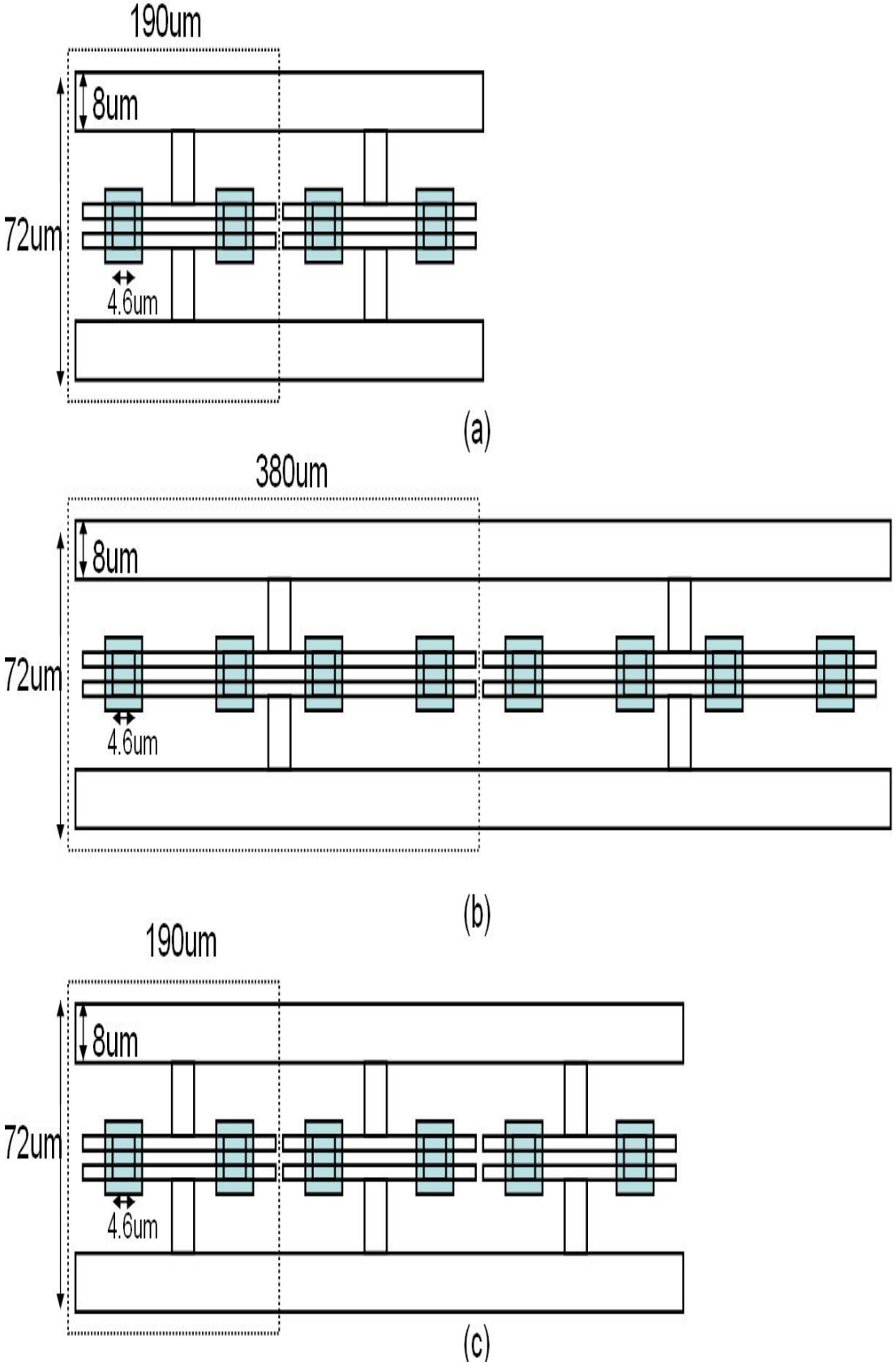
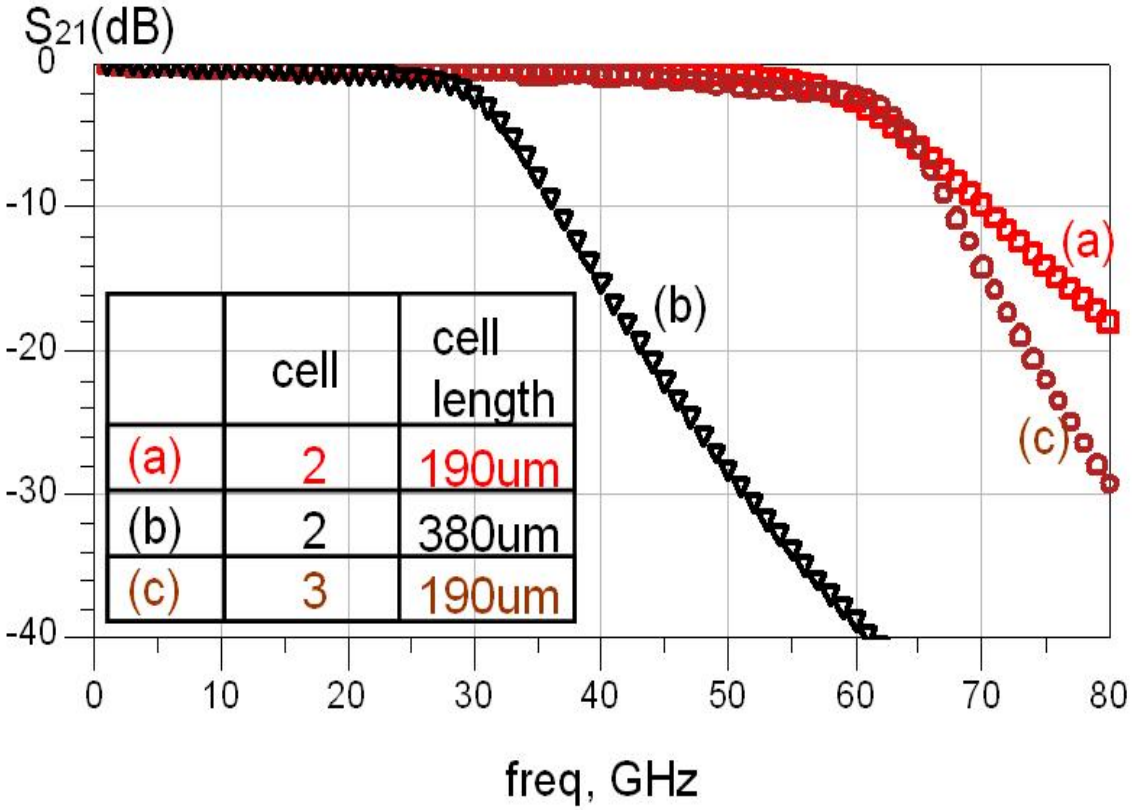
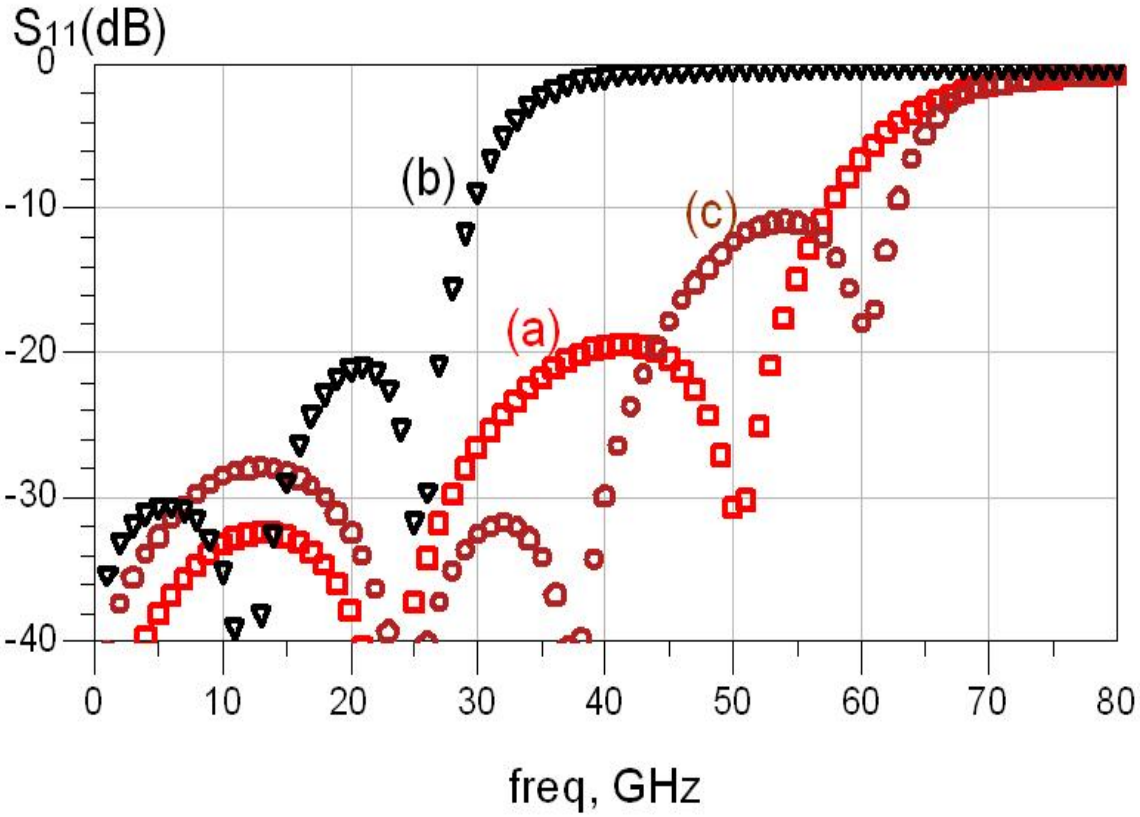


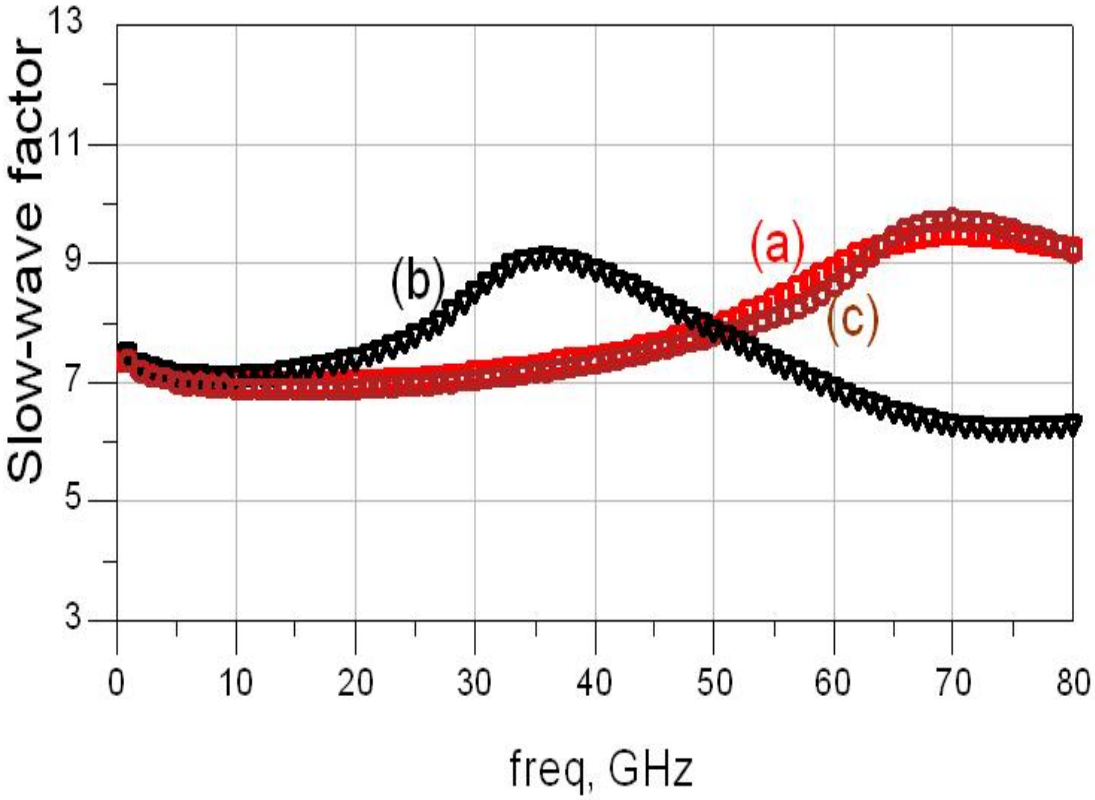
Fig. 3.6 Two-cells HS-CPS of (a) 190um cell length and (b) 380um cell length. (c) Three-cells HS-CPS of 190um cell length.


S21(dB)
0
-10
-20
-30
-40
0
10
20
30
40
50
60
70
80
freq, GHz
(a)
(b)
(c)
cell
cell length
(a) 2 190um
(b) 2 380um
(c) 3 190um

(a)


S11(dB)
0
-10
-20
-30
-40
0
10
20
30
40
50
60
70
80
freq, GHz
(b)
(c)
(a)

(b)



(c)

Fig. 3.7 (a) S_{21}, (b) S_{11}, and (c) slow-waver factors of the HS-CPS structures with different cell length or the number of cells.

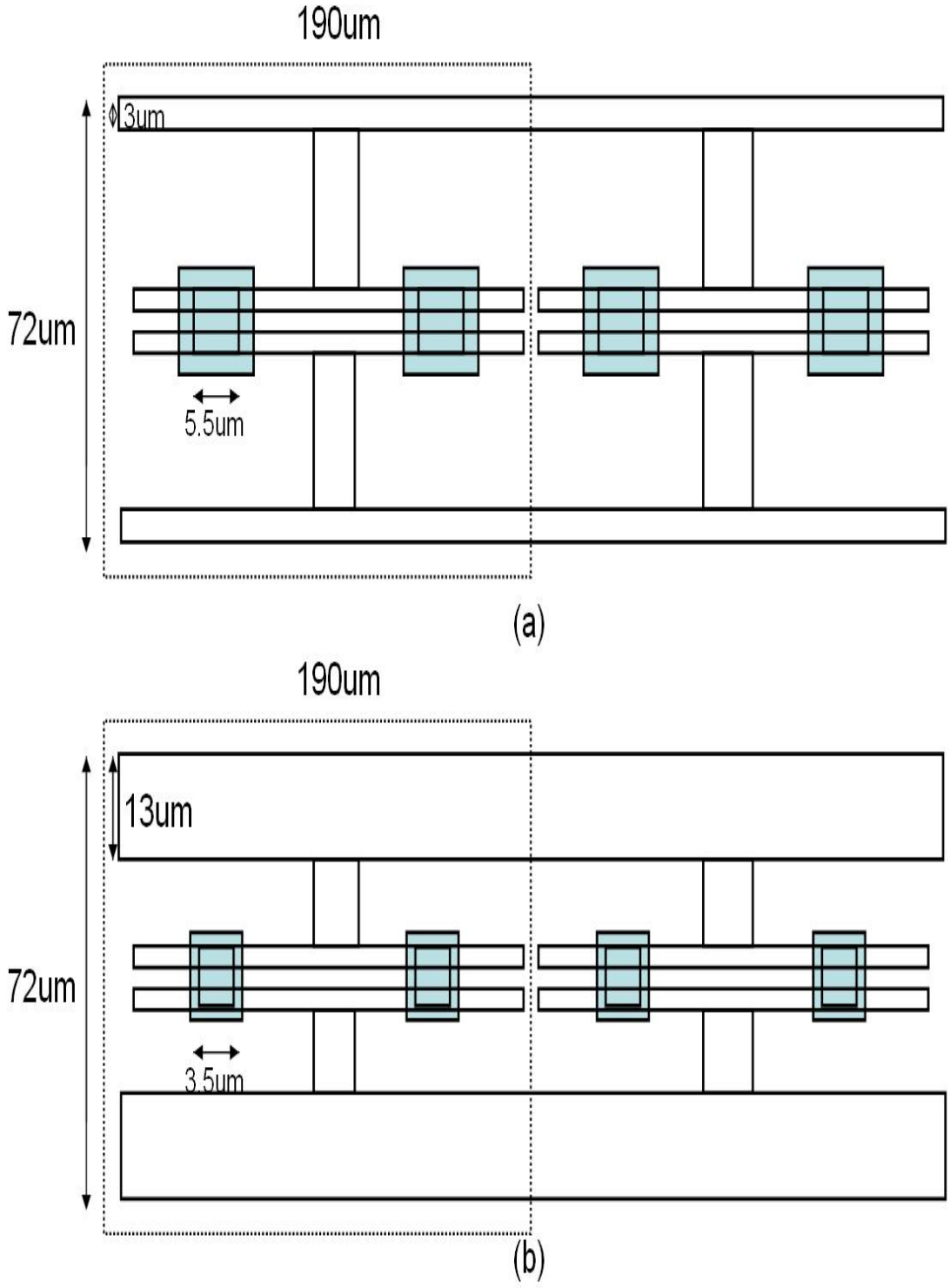
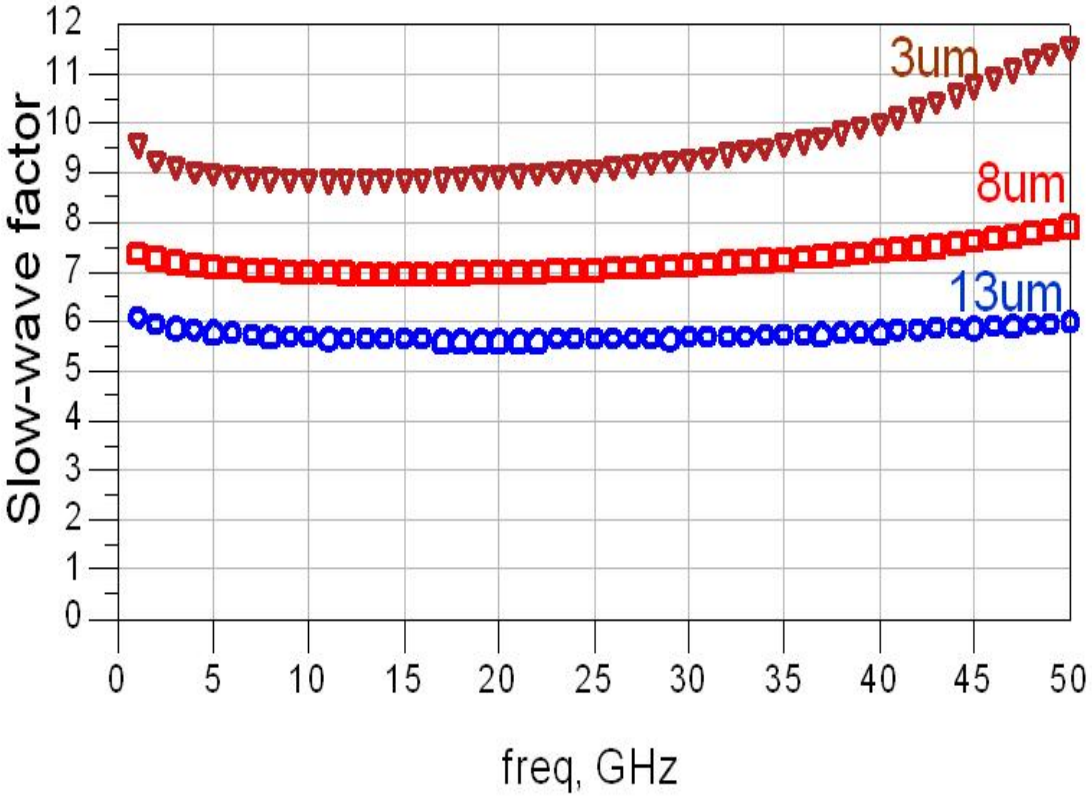
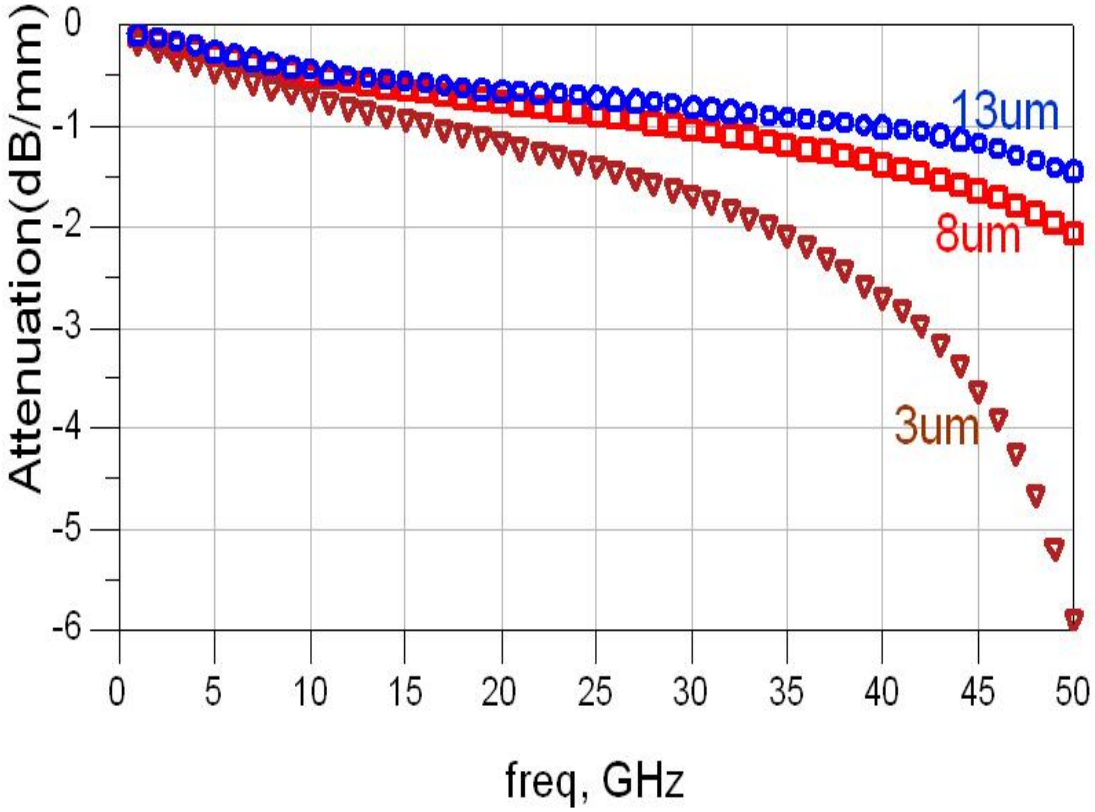


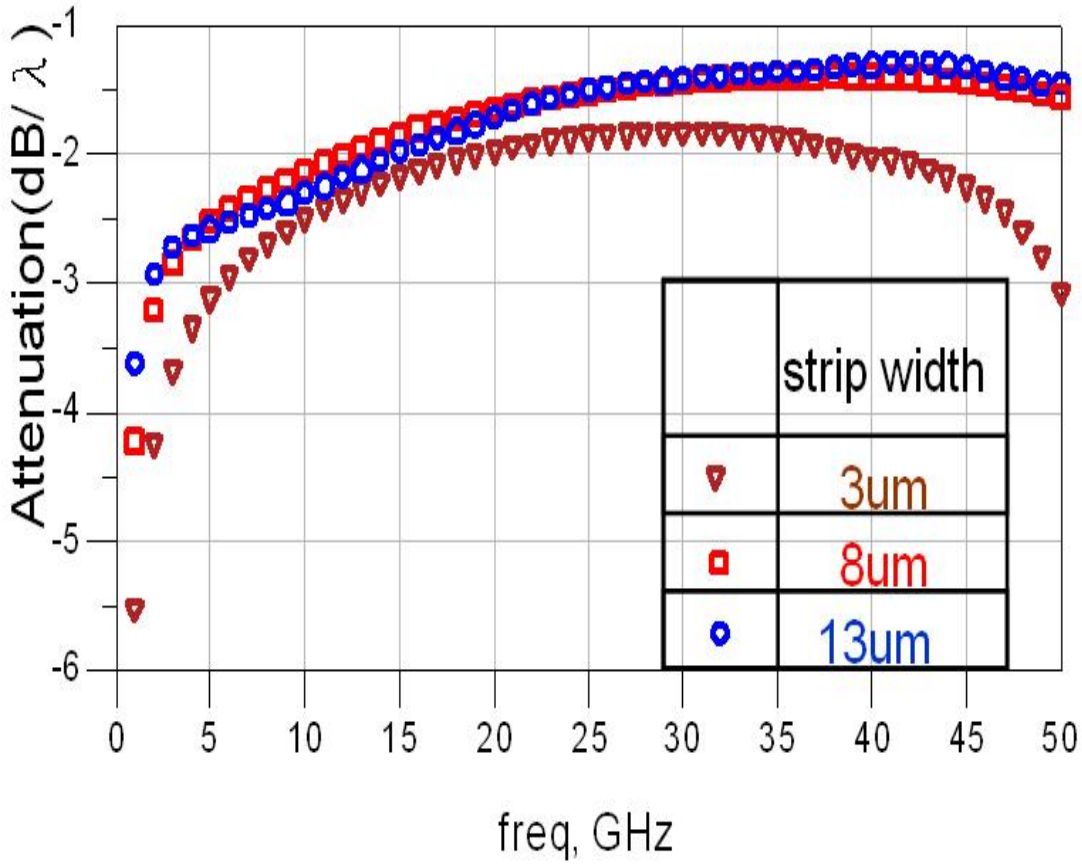
Fig. 3.8 Two-cells HS-CPS of (a) 3um strip width and (b) 13um strip width.


Slow-wave factor
freq, GHz
3um
8um
13um

(a)


Attenuation(dB/mm)
freq, GHz
13um
8um
3um

(b)



(c)

Fig. 3.9 (a)Slow-wave factor, (b) attenuation per mm (dB), and (c) attenuation per wavelength (dB) of the HS-CPS structures with different strip width.

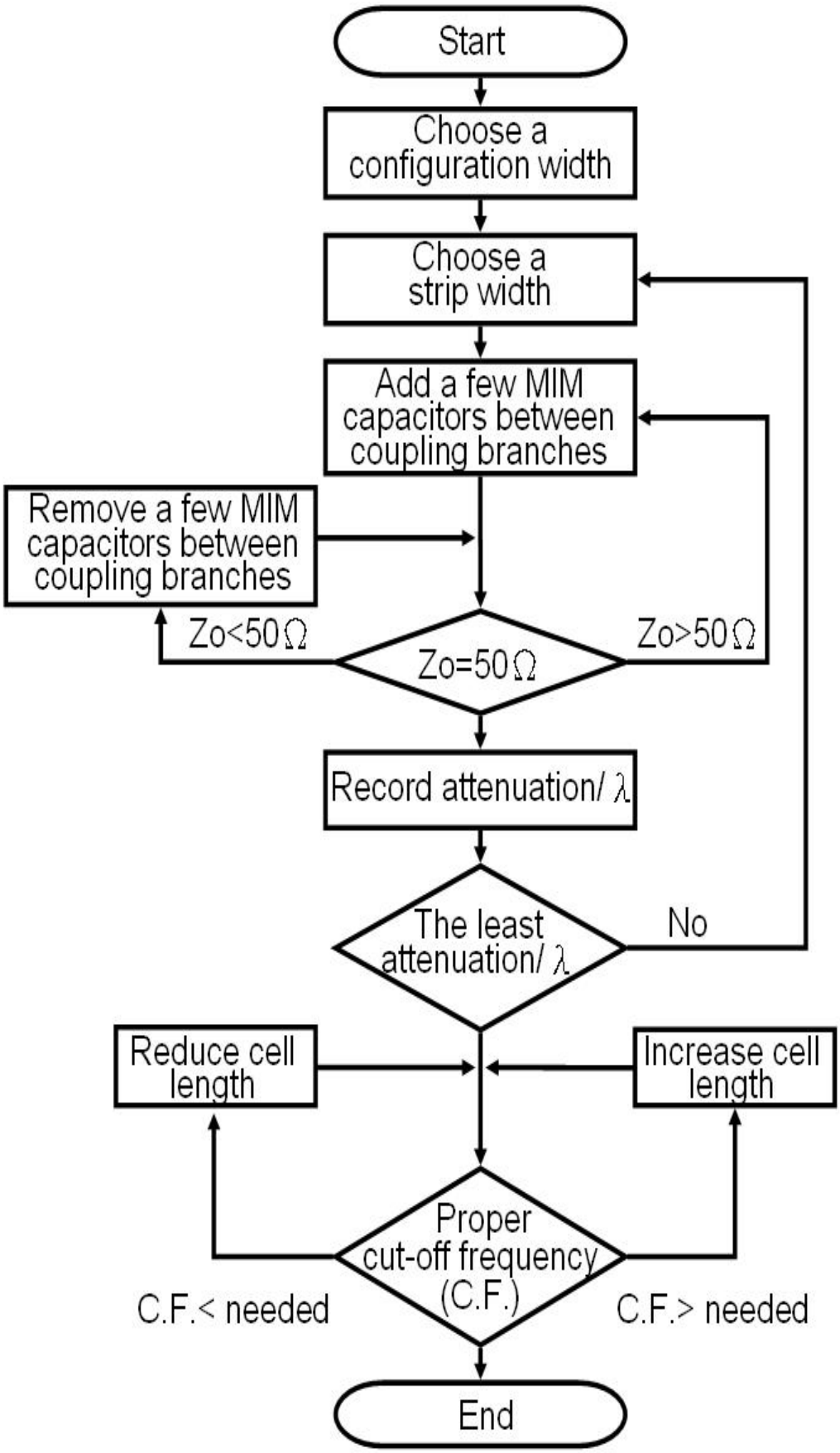


Fig. 3.10 The design flowchart of the HS-CPS.

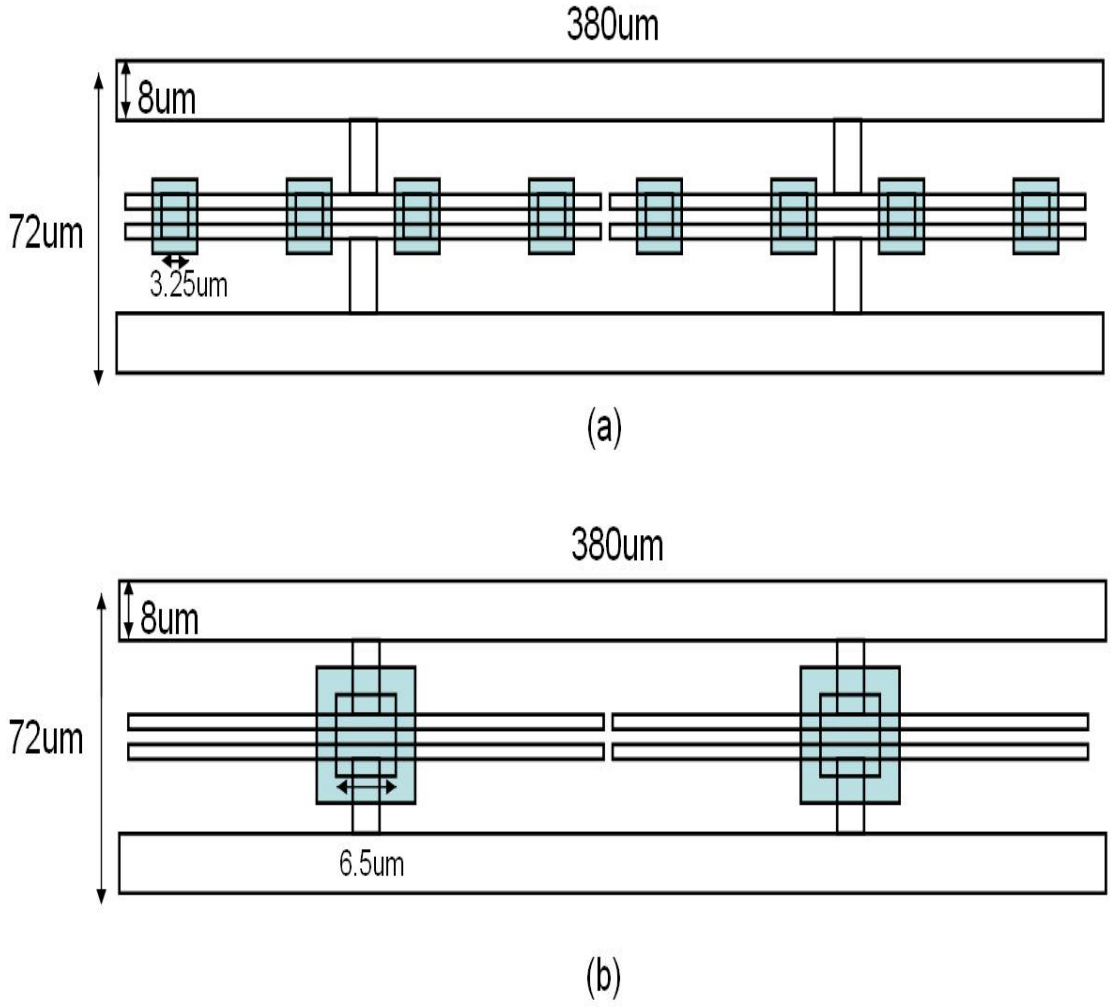


Fig.3.11 The HS-CPS lines of (a) eight 3.25X3.25um^2 MIM capacitors and (b) two 6.5X6.5um^2 MIM capacitors.

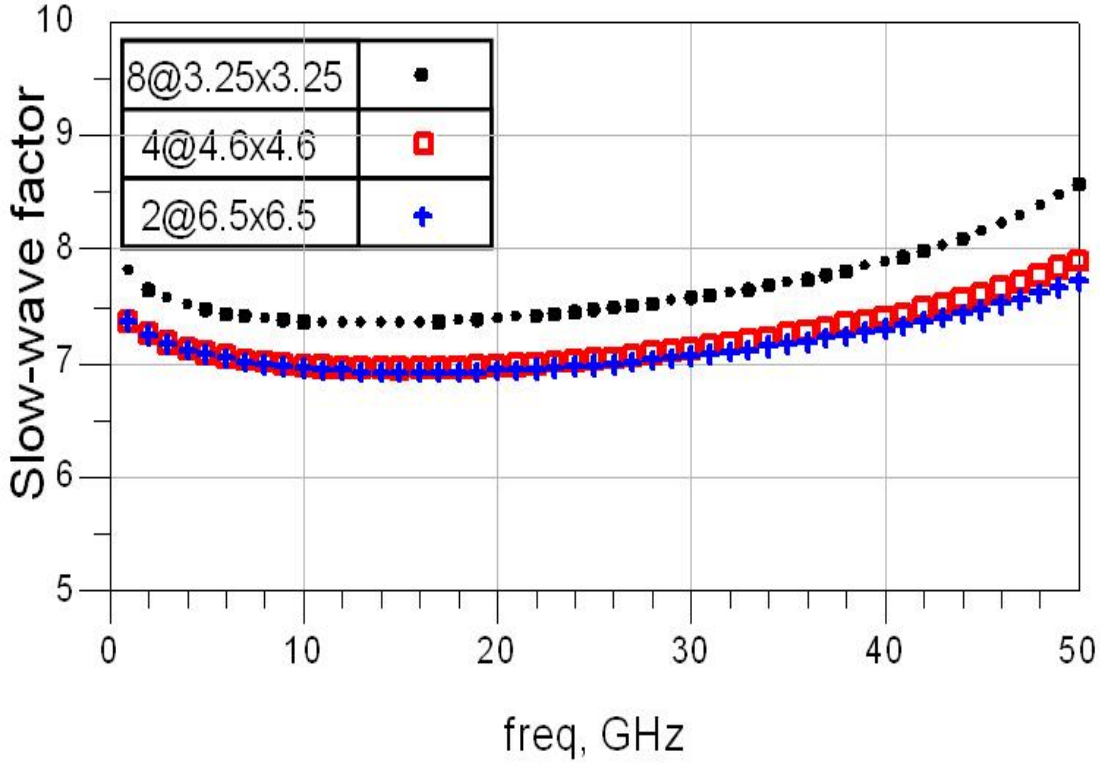


Fig.3.12 The slow-wave factors of the HS-CPS lines of different arrangements of MIM capacitors.

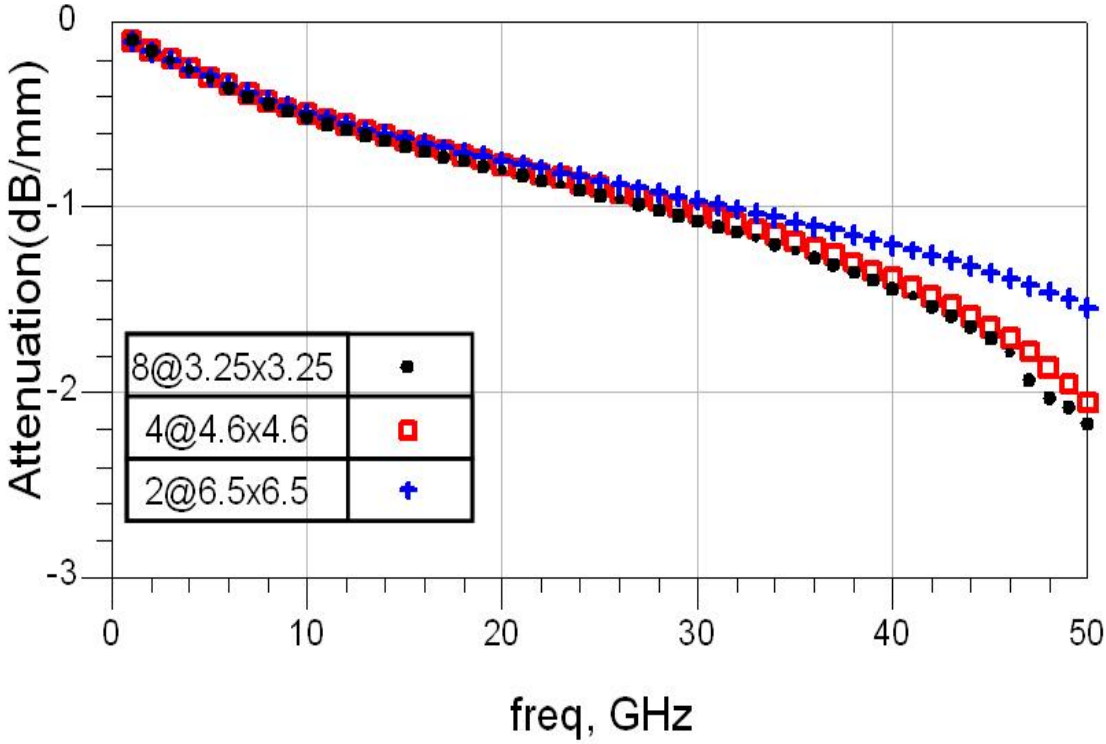


Fig.3.13 The attenuations per mm of the HS-CPS lines of different arrangements of MIM capacitors.

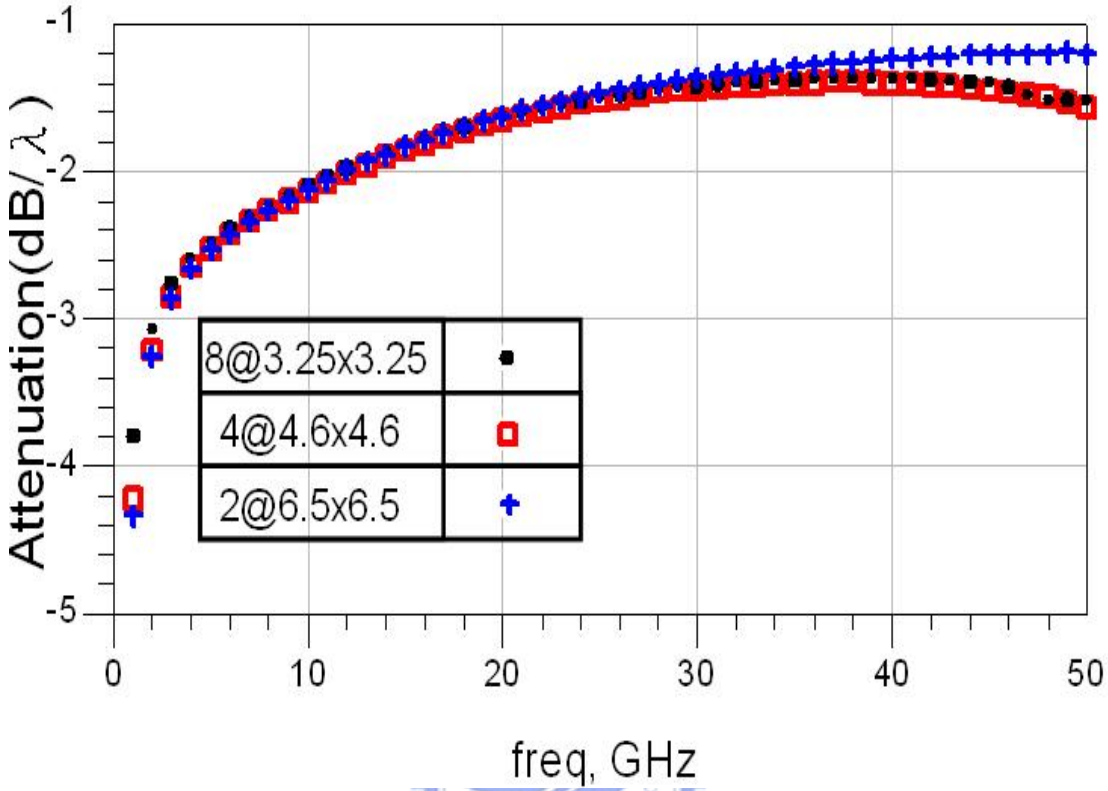


Fig.3.14 The attenuations per wavelength of the HS-CPS lines of different arrangements of MIM capacitors.

3.4 Conclusion

A new type of slow-wave periodic CPS using MIM capacitors has been proposed. It is suitable to be applied in the standard CMOS process without any additional post-process. The slow-wave factor is 3.5 times larger than that of conventional CPS and the substrate loss is also minimized significantly. The new structure therefore has the potential to improve the performance and miniaturize the size of any component consisting of transmissions.

CHAPTER 4

40GHz Miniature Bandpass Filter

An on-chip high performance 40GHz miniature bandpass filter is presented. Implemented in a standard CMOS process without any extra post processing, the filter features in small size ($72*400um^2$) and low insertion loss (1.4dB) by using the HS-CPS

4.1 Introduction and Previous Works

As far as the cost and the level of integration is concerned, silicon-based CMOS technology has become a good candidate as the solution of a highly integrated single-chip system, which incorporates digital, analog and RF circuitry [9]. While CMOS devices have been successfully applied to RF integrated circuit design, the on-chip filter, an essential component in RF or microwave circuits, however, still suffer from the high insertion loss due to the lossy substrate as well as the large occupied area in a standard CMOS process. Consequently an external off-chip filtering circuit is typically employed in a high performance system. Extensive research has been conducted in the area of on-chip filter design.

It can be found that much effort has been directed to high resistivity substrates in order to minimize the effect of substrate loss, including methods by directly using high resistivity Si wafers [10], by using thick polyimide layer on the top of lossy Si substrate [11], by microelectromechanical system (MEMS) technology [12], or by proton implantation process [13]. Nevertheless, it is of great interest to design filters on a standard CMOS substrate without extra post processing.

Several structures have been proposed for size reduction by enhancement of slow-wave characteristics, such as periodic ground plane microstrip [4], and slow-wave CPW (S-CPW) [8]. Besides, a bandpass filter of compact size has been implemented by an electric-magnetic-electric (EME) microstrip line [5] and miniature lowpass filters have been realized by periodic-structure CPW [7]. For on-chip implementation, it is necessary to further reduce the effective wavelength of signal propagation since filtering is generally related to the wavelength. That is, it is essential to design the filtering structure appropriately in a manner to enhance the slow wave characteristic.

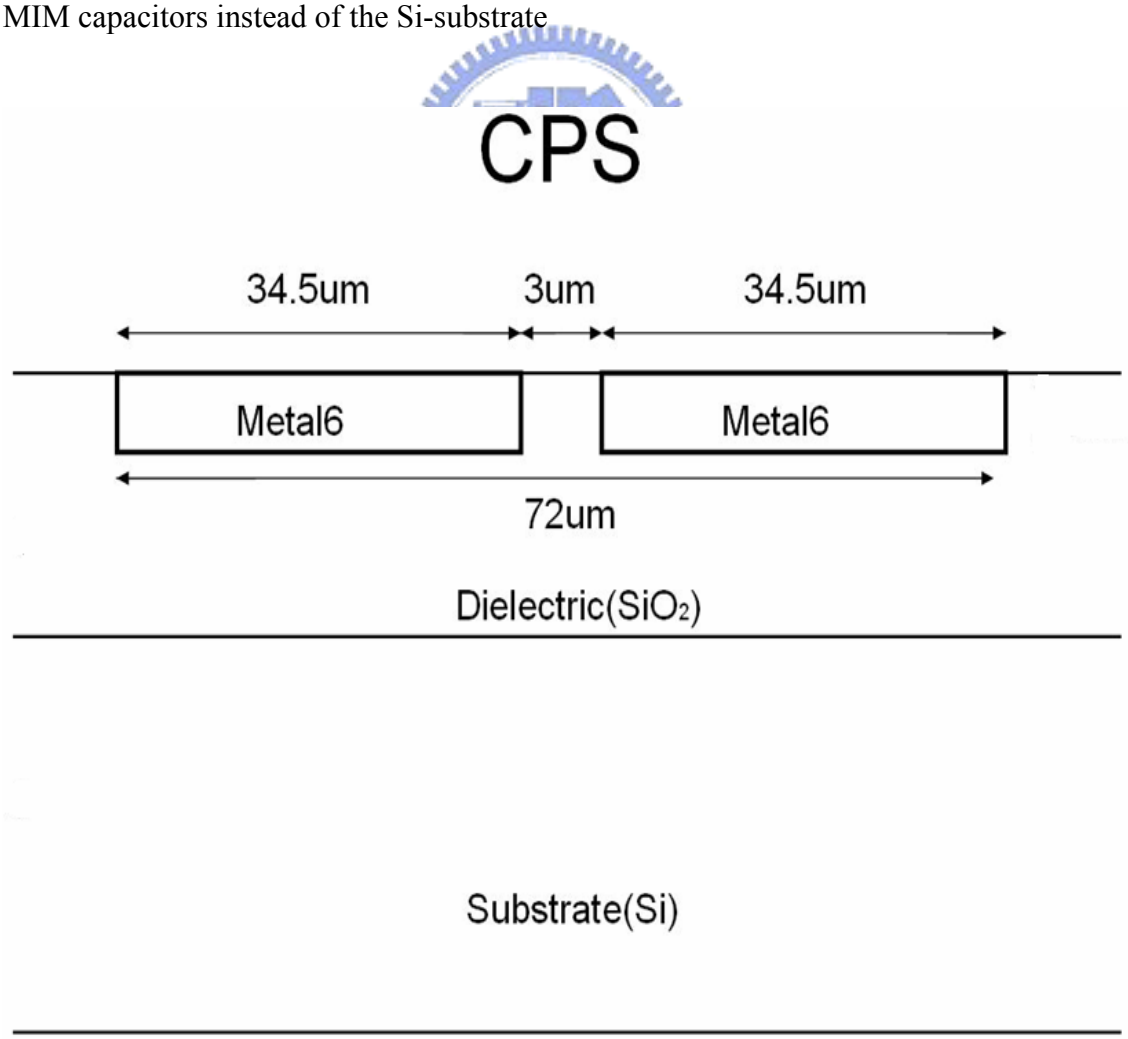
In this paper, an on-chip miniature bandpass filter is designed at the frequency of 40GHz and realized by the novel HS-CPS structure. It features in small size, low substrate loss, and easy fabrication (by standard 0.18um CMOS process). The slow-wave factor of the HS-CPS achieves to a value higher than those in previous work, and the attenuation is small enough for practical applications. Therefore, the two critical limitations, large size and severe substrate loss, of the on-chip filters can be relaxed

4.2 Design Consideration for Size Reduction

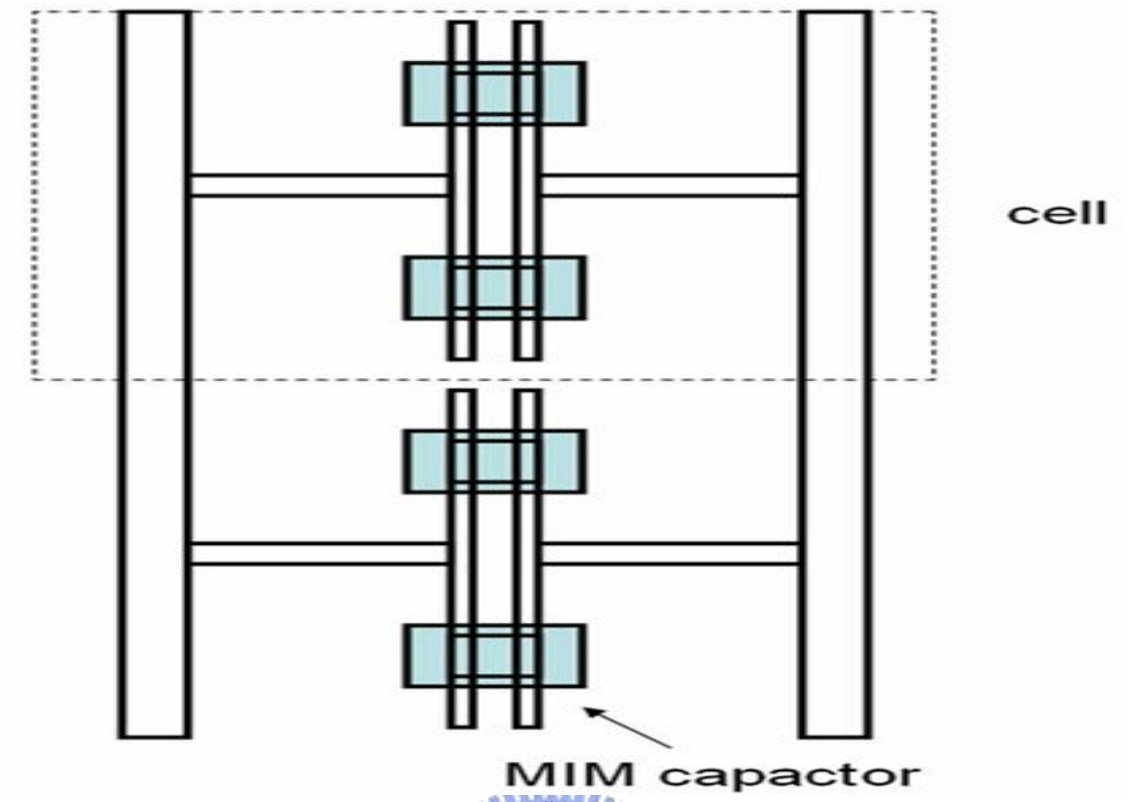
To reduce the size of a filter, it is critical to apply a transmission line, or an interconnect, with high slow-wave characteristic. The conventional CPS line is shown in Fig. 4.1(a). The slow-wave characteristic is enhanced in two folds by using a narrow strip width and large spacing between strip lines, and by adding capacitive coupling branches, as the HS-CPS structure shown in Fig. 4.1 (b). The cross-sectional view is illustrated in Fig. 4.1 (c).

The result of a narrow strip width and wide spacing is large magnetic flux in the

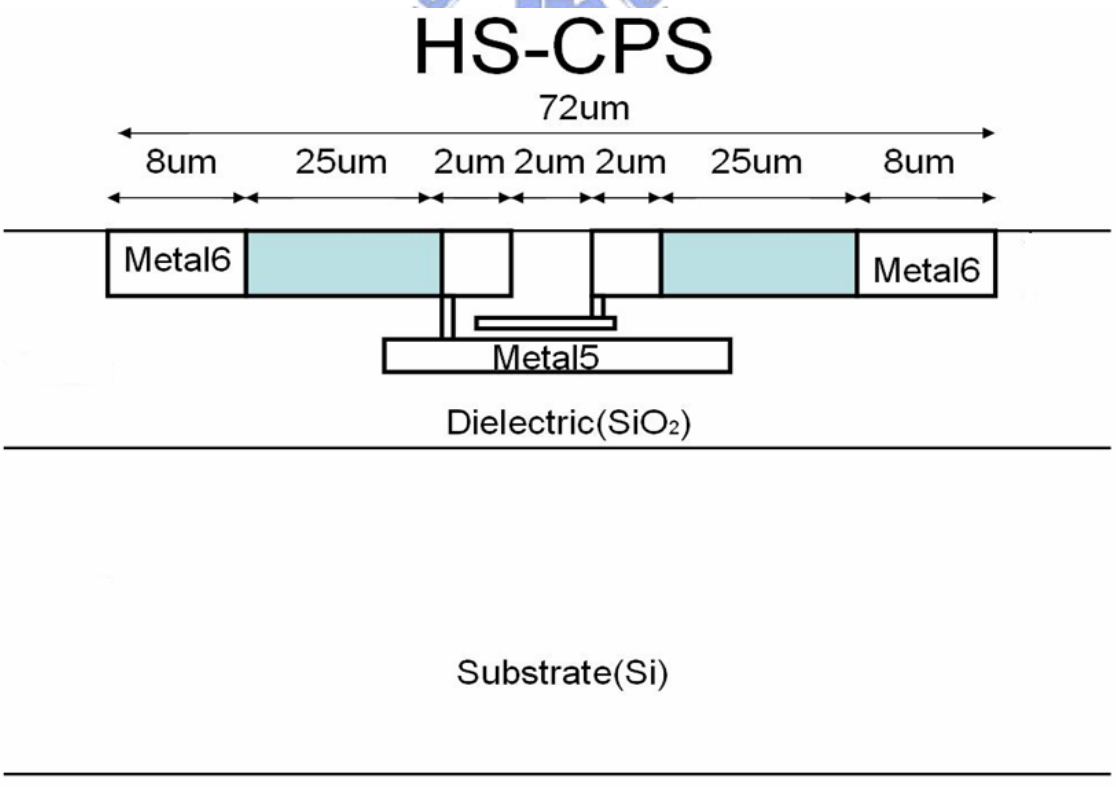
current loop formed by the two strips. Consequently the distributive inductance per unit length of the CPS line increases. Furthermore, each coupling cell contains two MIM capacitors such that the capacitive coupling between strip lines increases and essentially the distributive capacitance per unit length of the CPS transmission line is enlarged. As a result, the slow-wave characteristic is enhanced as the phase velocity decreases, $v_p = 1/\sqrt{LC}$, where L and C are distributive inductance and capacitance per unit length, while the characteristic impedance can be remained the same. The advantage of the structure lies in the flexibility to choose a large value of MIM capacitors available in multi-layer on-chip configuration. Also, it minimizes signal attenuation due to substrate loss because most signal energy is near the area of MIM capacitors instead of the Si-substrate



(a)



(b)



(c)

Fig. 4.1 (a) Cross-sectional view of the conventional CPS. (b) Top view and (c) cross-sectional view of the HS-CPS.

4.3 Filter Design and Simulation Results

The bandpass filter is implemented in TSMC 0.18um CMOS technology and analyzed by 3D EM simulation software of Ansoft HFSS. The passband is designed to be centered at 40GHz with 30% fractional bandwidth. A Chebyshev-type capacitive coupled single-stage resonator is employed for the design [14].

Fig. 4.2(a) and (b) show the transmission line model and the design of the filter. The characteristic impedance of the transmission line is chosen as 50Ω, implemented by using a HS-CPS line with the dimensions as shown in Fig. 4.1 (c). The slow-wave factor is plotted in Fig.4.3 (a), reaching to 7.5 at 40 GHz, which is 3.9 times larger than that of the conventional 50-Ohm CPS line shown in Fig. 4.1(a), indicating great size reduction. In Fig. 4.3 (b), the attenuation at 40GHz is improved from 4 to 1.4 dB/ λ for the reason that the total attenuation decreases as the effective wavelength is reduced. To further explore the mechanism that causes signal attenuation in such a structure, all conductor of the HS-CPS is replaced with perfect electric conductor. It is found that attenuation decreases to much less than 1dB per wavelength as shown in Fig. 4.3(b), demonstrating attenuation is mainly due to conductor loss rather than Si-substrate loss.

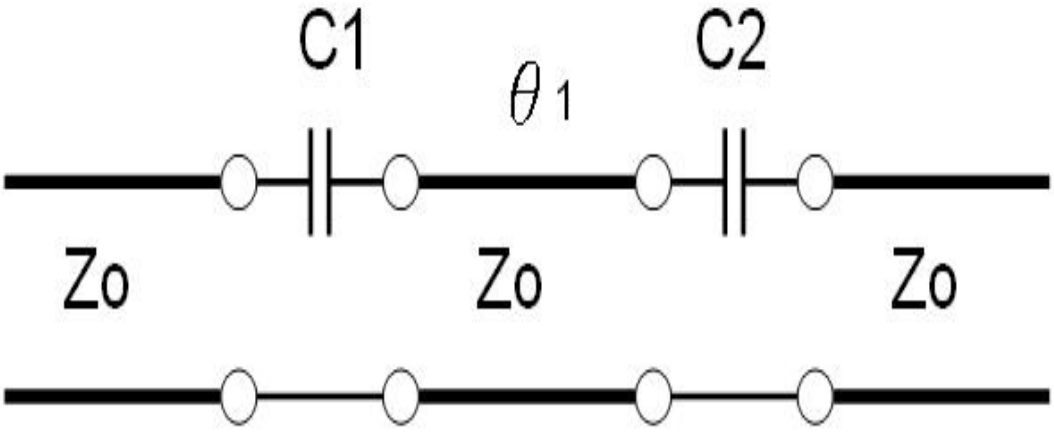
According to one-stage 3dB Chebyshev filter coefficient, g1=1.9953, the electrical length, θ_1, is 128° (at 40GHz), which corresponds to a length of 360 um in the HS-CPS structure but 1400 um in the conventional CPS line. It stands for a length reduction of 74%. The values of C_1 and C_2 in the transmission line model of the bandpass filter are required to be as of 50fF, which leads to a value of 100fF for the MIM capacitor C.

In Fig. 4.4, it shows the simulation results of this miniature bandpass filter. The center frequency is 39.5GHz with an insertion loss of 1.1dB, and the 3-dB frequencies

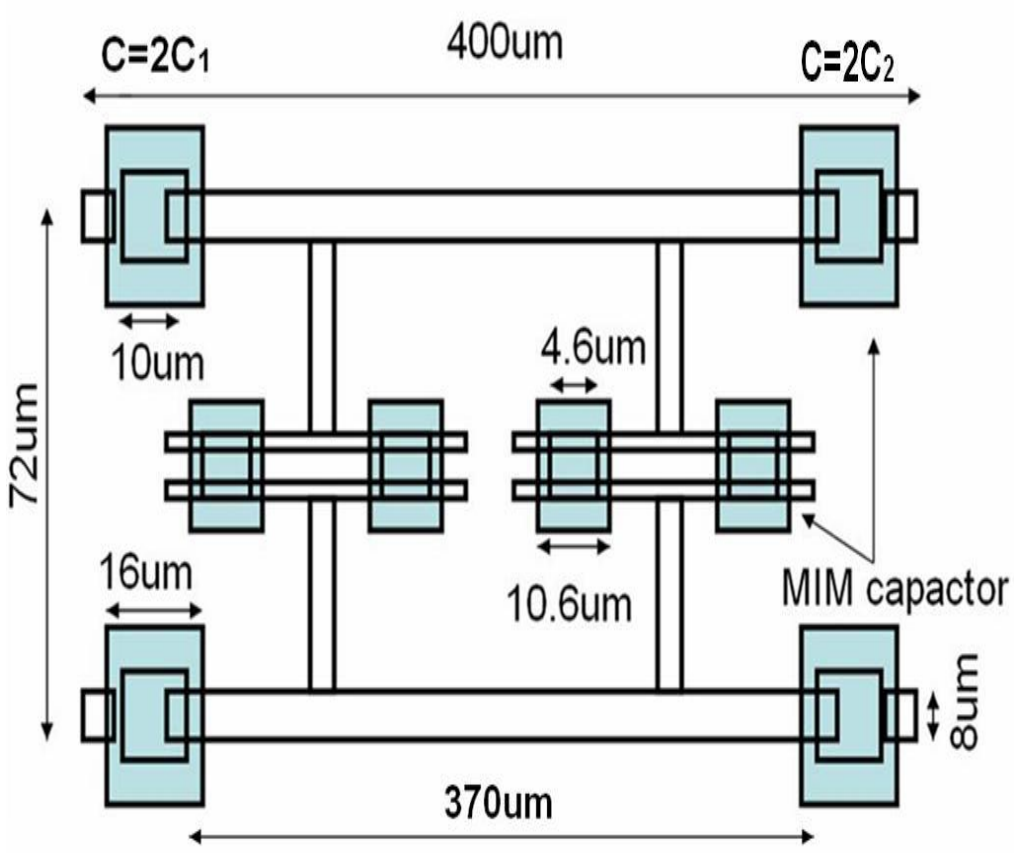
are 32.5GHz and 50.5GHz. The S-parameters of the theoretical design and the 40GHz CPW bandpass filter on proton-implanted Si-substrate [13], depicted in Fig. 4.5, are also plotted in the same figure. The comparison in Table 4.1 shows that the insertion loss of this design is smaller than that of the proton-implanted filter and that of the filter with thick Polyimide layer [11] and the occupied area are reduced significantly.

Another advantage of this bandpass filter is the spurious response rejection. As the bandpass filter is investigated in higher frequencies, shown in Fig.4.6, it is obvious that there is no passband near the second harmonic (80GHz). It is due to the cut-off frequency of the HS-CPS used in the bandpass filter is less than 80GHz, and therefore, it works as a lowpass filter rejecting the signal of higher frequency than its cut-off frequency.

In order to investigate the substrate loss and metal loss of this filter, all metals used in the filter are replaced with perfect conductor. It means the metal loss is eliminated and the remaining loss is substrate loss. The simulation results in Fig. 4.7 show the substrate loss is insignificant. It also can be verified by replacing the lossy substrate of 0.18um CMOS technology with lossless substrate (σ=0 S/m). The simulation results are also shown in the same figure. As the lossy substrate of 0.18um CMOS technology is replaced with lossless substrate, the insertion loss is improved slightly indicating the slight effect of the lossy substrate in this novel structure.

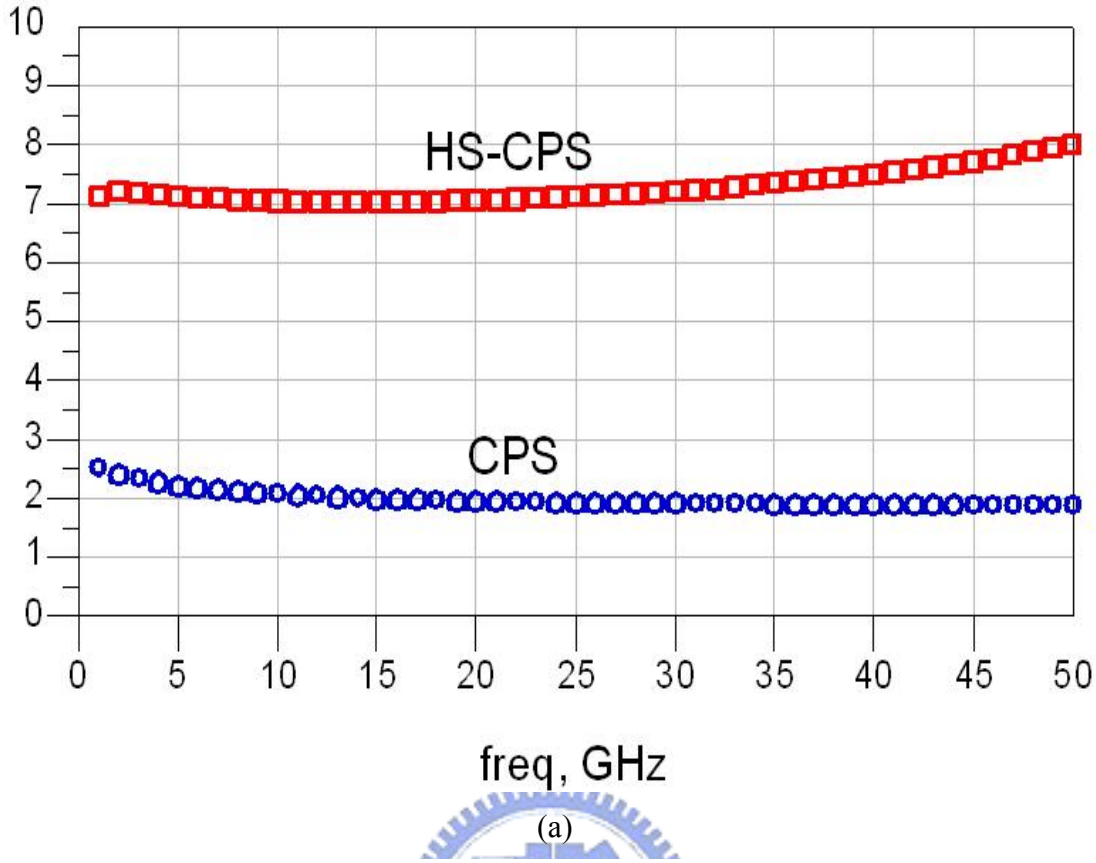


(a)

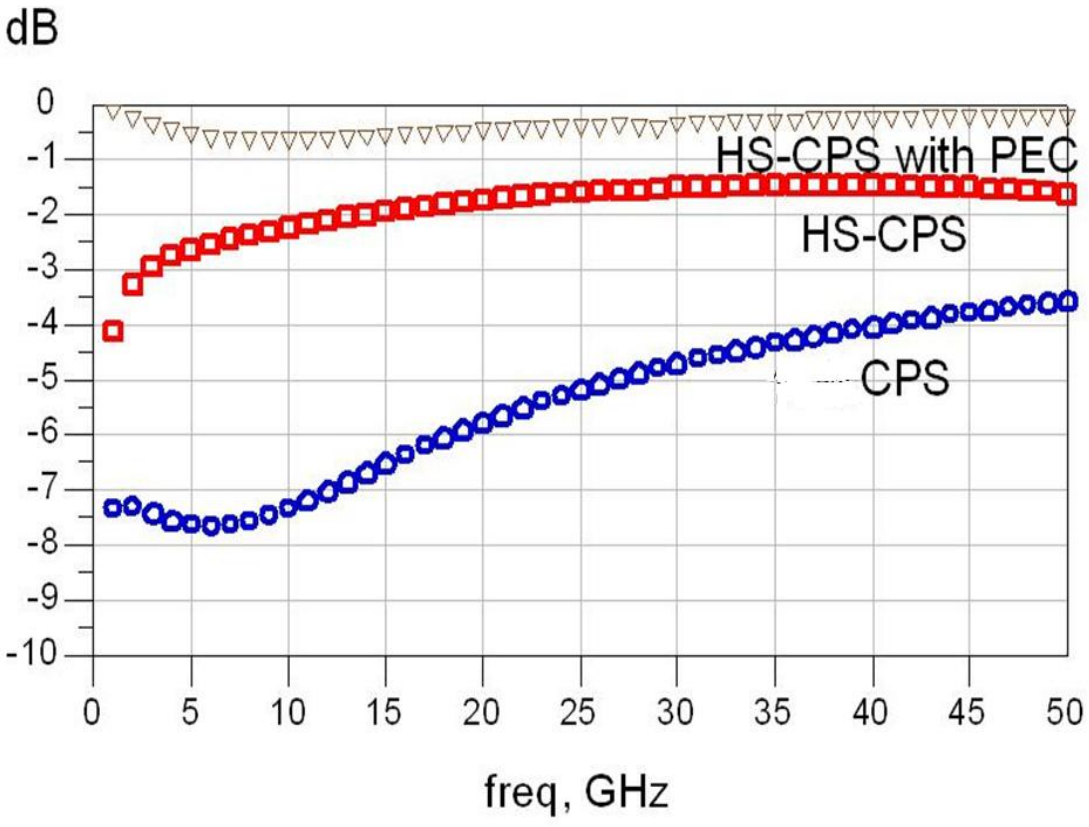


(b)

Fig. 4.2 (a) Transmission line model of capacitive coupled one-resonator bandpass filter and (b) dimensions.



(a)



(b)

Fig. 4.3 (a) Slow-wave factors and (b) attenuation per wavelength of conventional CPS and HS-CPS

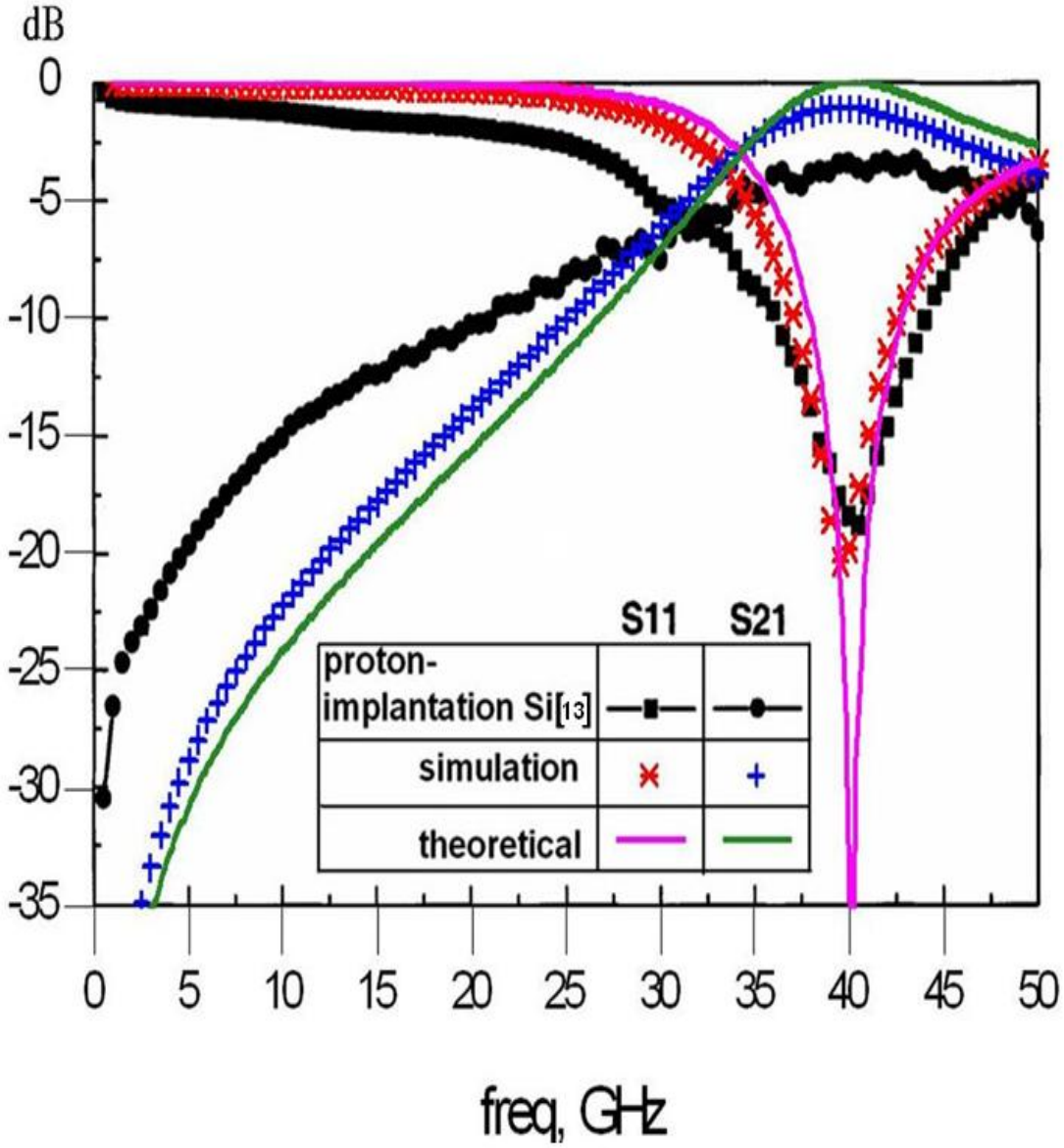


Fig. 4.4 S-parameters of the HS-CPS miniature bandpass filter, theoretical bandpass filter, and the CPW bandpass filter on proton-implanted Si-substrate.

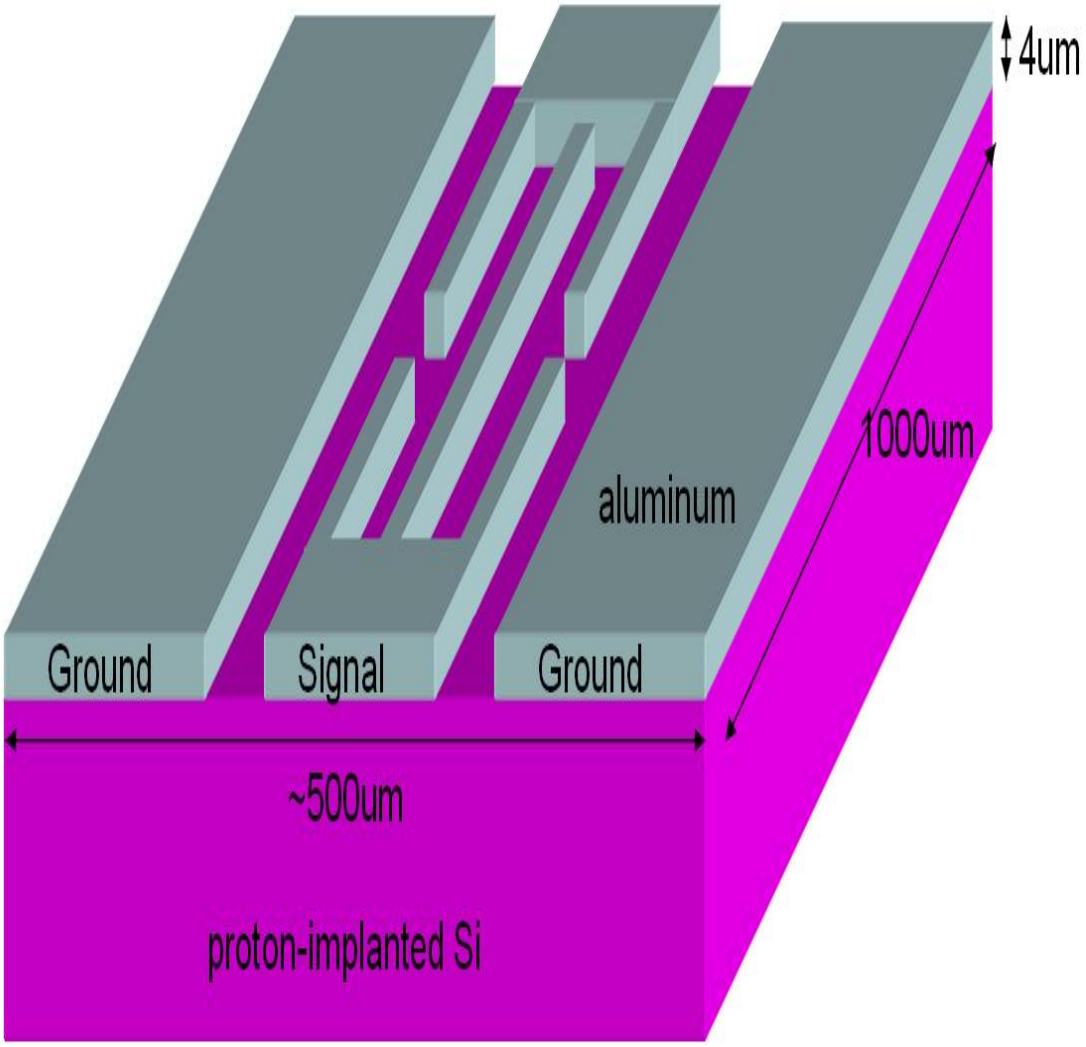


Fig. 4.5 The CPW bandpass filter on proton-implanted Si-substrate.

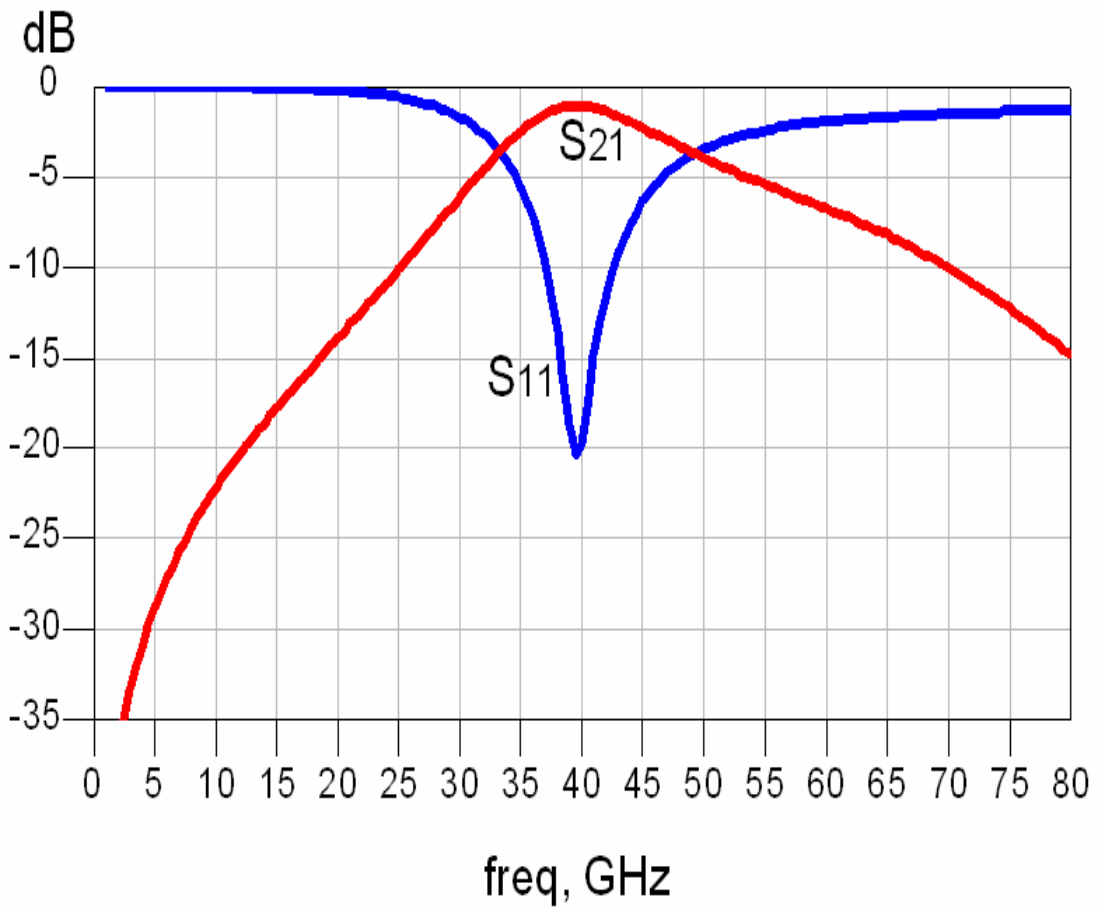


Fig.4.6 The spurious response rejection of the bandpass filter.

Table 4.1 Size and min. insertion loss (IL) of on-chip bandpass filters.

Structure	Configuration Length	Configuration Width	Min. IL
thick Polyimide layer filter[11]	3400um*	215um	2.76dB
proton-implanted filter [13]	1000um	~ 500um	3.4dB
This work	**400um**	**72um**	**1.1dB****

* Center frequency is at 30GHz
**Measured Min. insertion loss is 1.4dB

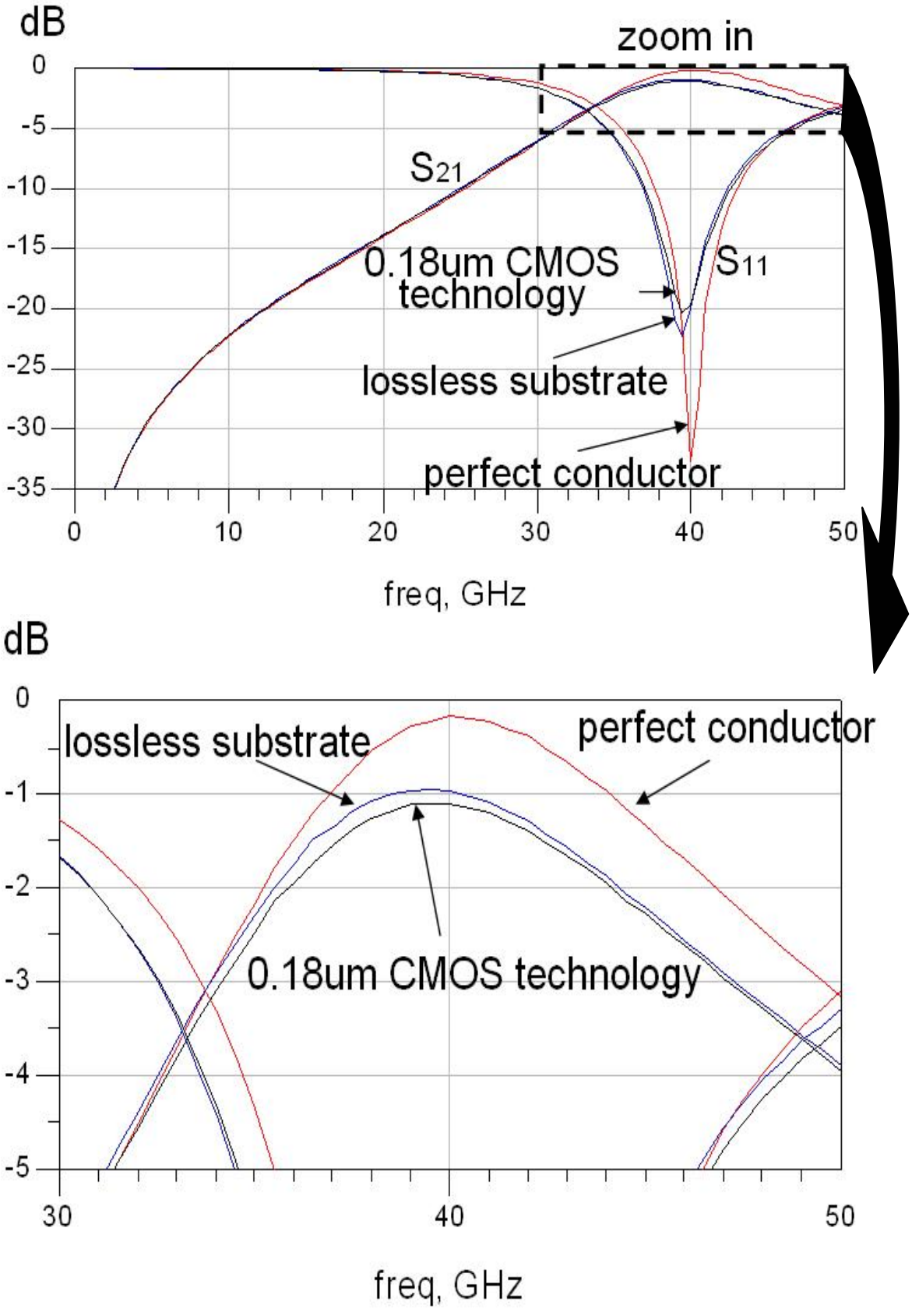


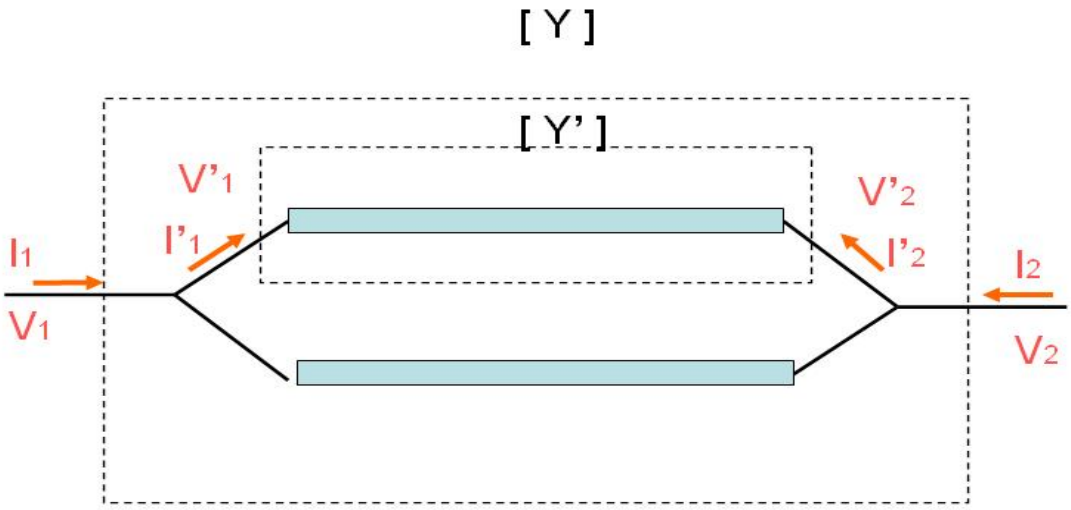
Fig. 4.7 S-parameters of the HS-CPS miniatures bandpass filters with perfect conductor, lossless substrate, and 0.18um CMOS technology.

4.4 Measurement Considerations and Results

Two issues of measurements of this filter will be discussed in this section, one is the measurement of the CPS-like structure with Ground-Signal-Ground (GSG) probes and the other is the de-embedding method used in this measurement.

4.4.1 Measurement with GSG probe

The S-parameters was measured on wafer with two-port GSG probes from 10MHz to 50GHz by Agilent E8364B. While this CPS-like filter is measured with GSG probes directly, there will be an obvious discontinuity of electric field at the GSG pads. It is likely to cause the inaccurate measurement. In order to measure this CPS-like structure accurately by GSG probes, another identical filter is put aside the under-test filter symmetrically as shown in Fig. 4.8. It means that the results of the shunt circuit of the two identical filters will be measured. After the Y-parameters of the shunt structure, $[Y]$, is measured, the Y-parameters of the single filter, $[Y']$, can be got from the following equation (4.1).



$$[Y'] = \frac{1}{2}[Y] \tag{4.1}$$

4.4.2 De-Embedding Method

For accurate measurement of the filter, the parasitics of the pads and interconnects should be removed. Therefore, the open/short/thru de-embedding (OSTD) [15] is used in this measurement. The parasitics (z_i , y_p , z_l) and the device under test (DUT) are illustrated in Fig. 4.9 (a). After the impedances of the open ($Z_{in,o}$), short ($Z_{in,s}$), and thru ($Z_{in.thru}$) pads, depicted in Fig. 4.9 (a), (b), are measured. The three parasitics can be extracted through the following equations.

$$z_i = z_{in,s} \tag{4.2}$$

$$y_p = \frac{1}{z_{in,o} - z_{in,s}} \tag{4.3}$$

$$z_l = \frac{1}{2}\left(\frac{1}{\frac{1}{z_{in,thru} - z_{in,s}} - y_p} - \frac{1}{y_p + \frac{1}{z_{in,s}} + 50} \right) \tag{4.4}$$

and then the ABCD matrix of DUT, $\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{DUT}$,can be derived:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Total} = \begin{bmatrix} 1 & z_i \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ y_p & 1 \end{bmatrix} \begin{bmatrix} 1 & z_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{DUT} \begin{bmatrix} 1 & z_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ y_p & 1 \end{bmatrix} \begin{bmatrix} 1 & z_i \\ 0 & 1 \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{DUT} = \begin{bmatrix} 1 & z_l \\ 0 & 1 \end{bmatrix}^{-1} \begin{bmatrix} 1 & 0 \\ y_p & 1 \end{bmatrix}^{-1} \begin{bmatrix} 1 & z_i \\ 0 & 1 \end{bmatrix}^{-1} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Total} \begin{bmatrix} 1 & z_i \\ 0 & 1 \end{bmatrix}^{-1} \begin{bmatrix} 1 & 0 \\ y_p & 1 \end{bmatrix}^{-1} \begin{bmatrix} 1 & z_l \\ 0 & 1 \end{bmatrix}^{-1}$$

Therefore, the Y-parameters of the DUT, $[Y]_{DUT}$, can be obtained from:

$$[Y]_{DUT} = \begin{bmatrix} \frac{D}{B} & \frac{BC - AD}{B} \\ -\frac{1}{B} & \frac{A}{B} \end{bmatrix} \tag{4.5}$$

Finally, the Y-parameters of the single filter, $[Y']$, is given through (4.1) and then the S-parameters of the single filter can be derived.

$$[S]=\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

$$=\frac{1}{(y'_{11}+\frac{1}{50})(y'_{22}+\frac{1}{50})-y'_{12}y'_{21}}\begin{bmatrix} (\frac{1}{50}-y'_{11})(\frac{1}{50}+y'_{22})+y'_{12}y'_{21} & -2y'_{12}\frac{1}{50} \\ -2y'_{21}\frac{1}{50} & (\frac{1}{50}+y'_{11})(\frac{1}{50}-y'_{22})+y'_{12}y'_{21} \end{bmatrix}$$

4.4.3 Measurement Results

Fig.4.10 shows the measured S-parameters for the miniature bandpass filter. Good agreement with the simulation is observed. The center frequency is 39 GHz and the minimum insertion loss is 1.4dB.The measured group delay is shown in Fig.4.11.

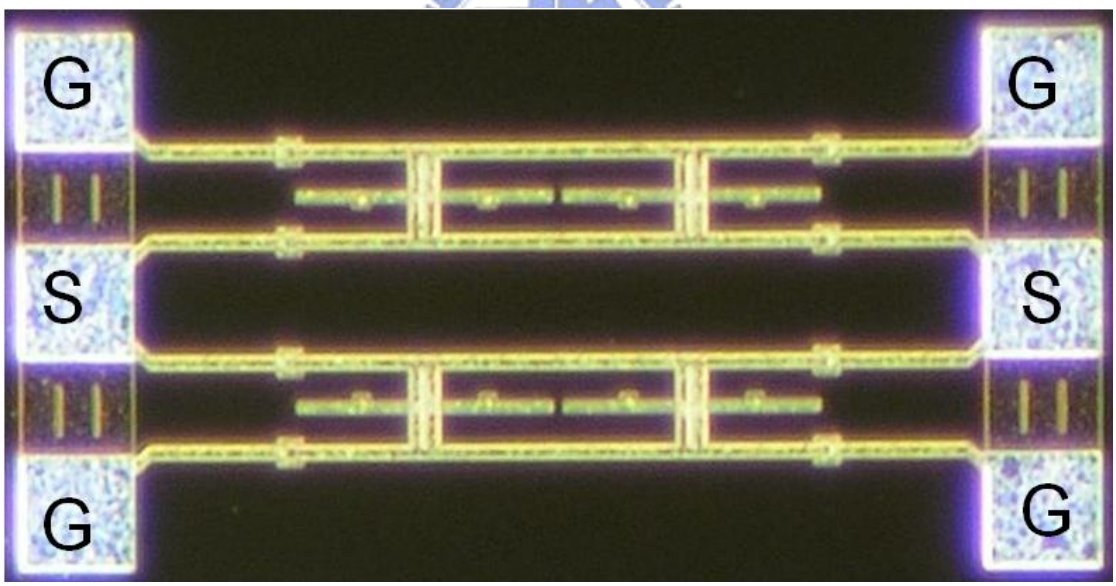
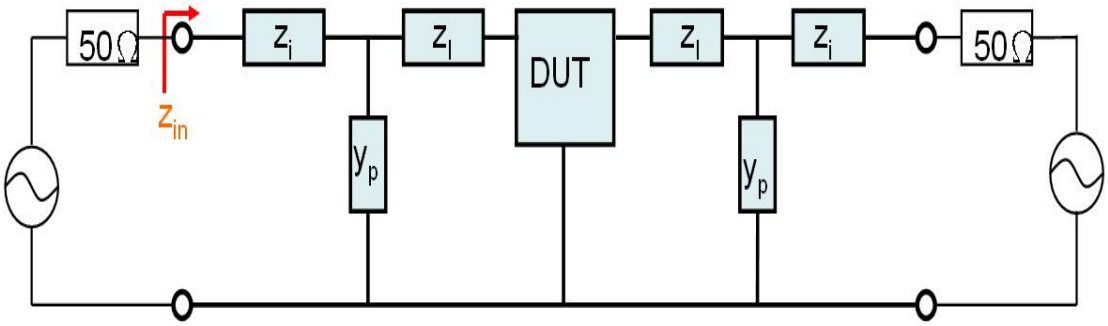


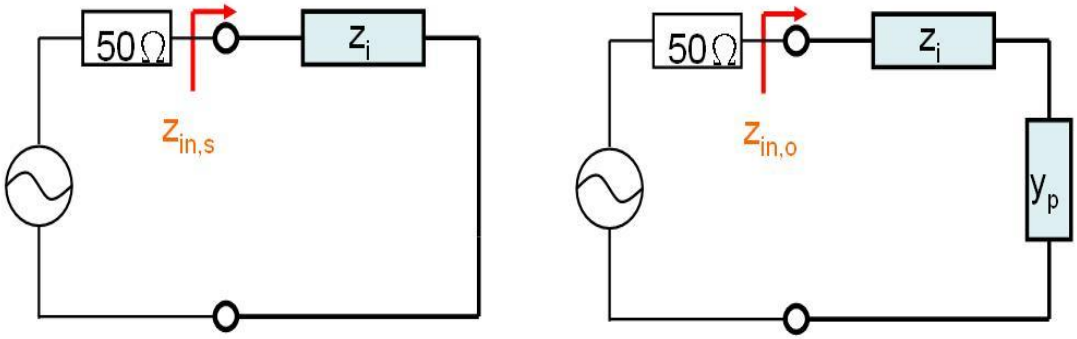
Fig. 4.8 Die photo of the two shunt miniature filters

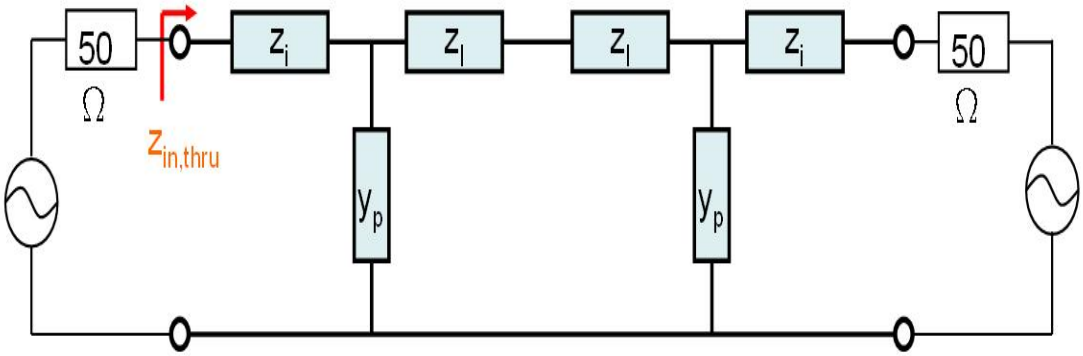
$$\begin{bmatrix} 1 & z_i \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ y_p & 1 \end{bmatrix} \begin{bmatrix} 1 & z_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{DUT} \begin{bmatrix} 1 & z_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ y_p & 1 \end{bmatrix} \begin{bmatrix} 1 & z_i \\ 0 & 1 \end{bmatrix}$$



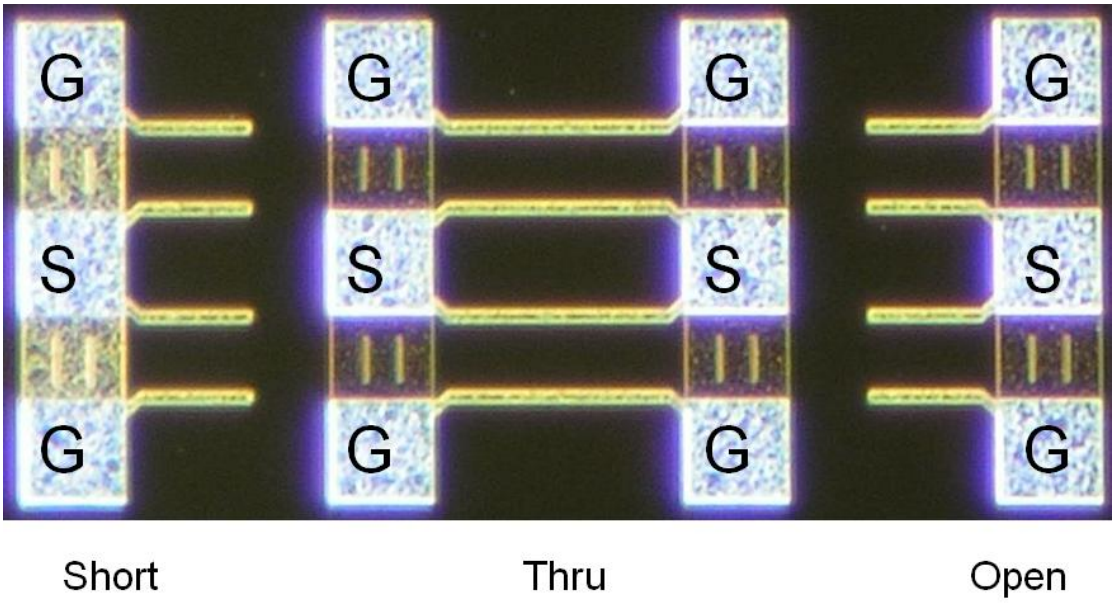
$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Total} = \begin{bmatrix} 1 & z_i \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ y_p & 1 \end{bmatrix} \begin{bmatrix} 1 & z_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{DUT} \begin{bmatrix} 1 & z_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ y_p & 1 \end{bmatrix} \begin{bmatrix} 1 & z_i \\ 0 & 1 \end{bmatrix}$$

(a)





(b)



(c)

Fig. 4.9 (a) Device under test and the parasitics of pads and interconnects.

(b)Parasitics and (c) photo of the short, open, and thru pads.

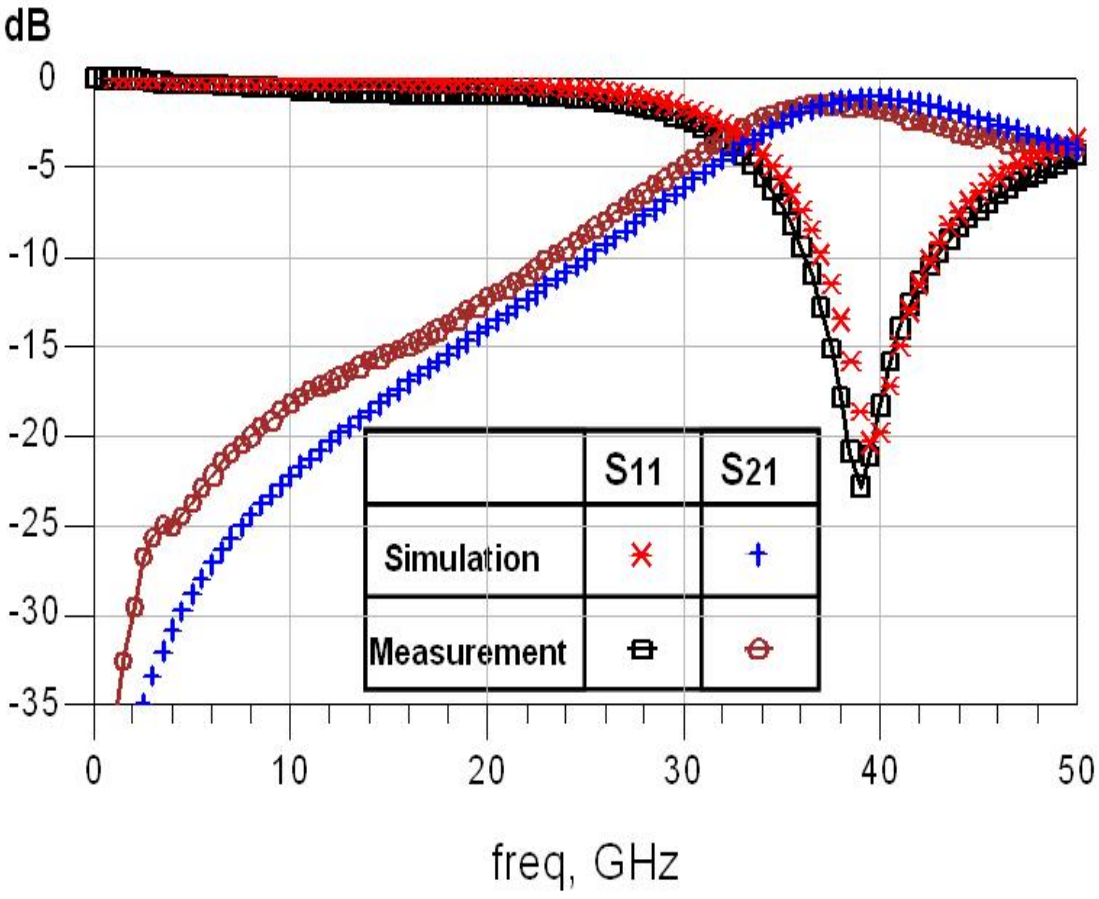


Fig. 4.10 Measured S-parameters of the miniature bandpass filter.

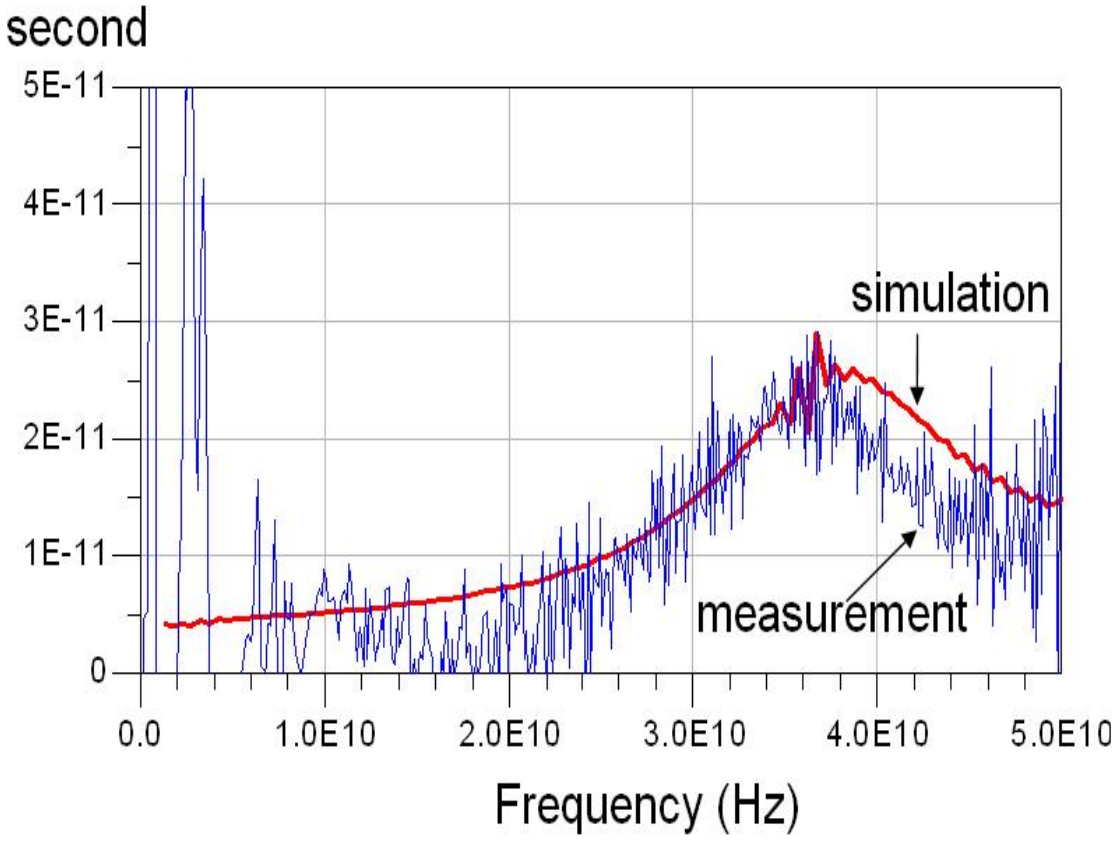


Fig. 4.11 Group delay of the miniature bandpass filter.

4.5 Conclusion

A high performance miniature on-chip bandpass filter is implemented in a standard CMOS process without extra post processing. The size is greatly reduced with good performance as compared with previous works. It shows a great potential for high-frequency applications of low-cost highly integrated single-chip circuits.

CHAPTER 5

Summary and Future Works

5.1 Summary

In this thesis ,a novel monolithic transmission— HS-CPS is presented. The slow-wave factor can achieves to a value (7.1~7.5) higher than those in previous works, and the attenuation (1.61dB/ λ at 20GHz) is small enough for practical applications. The high slow-wave factor means the compact occupied area and small attenuation indicates the high quality. Furthermore, it is suitable to be applied in the standard CMOS process without any additional post-process resulting in low cost.

A 40GHz miniature bandpass filter is designed using the novel HS-CPS. Taking the advantages of the HS-CPS, it features in mush smaller size (72*400um^2) and lower insertion loss (1.4dB) and easier fabrication (standard CMOS process) comparing with previous works. It shows a great potential for high-frequency applications of low-cost highly integrated single-chip circuits.

5.2 Future Works

Further development on nano-CMOS technology will leverage up the advantage of this HS-CPS line since higher conductivity metal is used and the lossy substrate is further from the top metal. The new structure therefore has the potential to further improve the performance and miniaturize the size of any component consisting of transmissions.

Several useful attributes of transmission lines as circuit elements such as small inductors, controlled-impedance interconnects, and electrostatic discharge protection

have been summarized and some examples of transmission lines circuit applications such as distributed amplifiers, distributed oscillators, and rotary traveling-wave oscillators are provided [2]. Obvious, it is an interesting topic to investigate how to improve the performances or reduce the occupied area of those circuits by the novel HS-CPS structure.

REFERENCES

[1] Bendik Kleveland, Carlos H. Diaz, Dieter Vook , Liam Madden, Thomas H .Lee, and S. Simon Wong, "Exploiting CMOS reverse interconnect scaling in multigigahertz amplifier and oscillator design," *IEEE J. of Solid-State Circuits.*, vol. 36, pp. 1480-1488, Oct. 2001.

[2] Behzad Razavi, "The role of monolithic transmission lines in high-speed integrated circuits," in *Proc. CICC*, May 2002, pp. 367-374.

[3] Hideki Hasegawa, Mieko Furukawa, and Hisayoshi Yanai, "Properties of microstrip line on Si-SiO_2 system," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, pp. 869-881, Nov. 1971.

[4] Fei-Ran Yang, Yongxi Qian, Roberto Coccioli, and Tatsuo Itoh, "A novel low-loss slow-wave microstrip structure," *IEEE Microwave Guided Wave Let.*, vol. 8, pp. 372-374, Nov. 1998.

[5] Ching-Kuo Wu, Hsien-Shun Wu, and Ching-Kuang Cliver Tzuang, "Electric–magnetic–electric slow-wave microstrip line and bandpass filter of compressed size," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 1996-2004, May 2002.

[6] Michael Y. Frankel, Robert H. Voelker, and James N. Hilfiker, "Coplanar transmission lines on thin substrates for high-speed low-loss propagation," *IEEE Trans. Microwave Theory and Tech.,* vol. 42, pp. 396-402, March 1994.

[7] James Sor, Yongxi Qian, and Tatsuo Itoh, "Miniature low-loss CPW periodic structures for filter applications," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 2336-2341, Dec 2001.

[8] Tak Shun D. Cheung, et al., "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *ISSCC Dig. Tech. papers*, pp. 396 – 397, Feb. 2003.

[9] Behzad Razavi, "CMOS technology characterization for analog and RF design," *IEEE J. Solid-State Circuits*, vol. 34, pp. 268-276, March 1999.

[10] H. S. Gamble et al., "Low-loss CPW lines on surface stabilized high-resistivity Silicon," *IEEE Microwave Guided Wave Lett.*, vol. 9, pp. 395-397, Oct. 1999.

[11] John Papapolymerou, and George E. Ponchak, "Microwave filters on a low resistivity Si substrate with a Polyimide interface layer for wireless circuits," in *IEEE RFIC Symposium.*, pp. 128-128, June 2001.

[12] Katherine Juliet Herrick, Thomas A. Schwarz, and Linda P. B. Katehi, "Si-micromachined coplanar waveguides for use in high-frequency circuits," *IEEE*

Trans. Microwave Theory Tech., vol. 46, pp. 762–768, June 1998.

[13] K. T. Chan, C. Y. Chen, Albert Chin, J. C. Hsieh, J. Liu, T. S. Duh, and W. J. Lin, "40-GHz coplanar waveguide bandpass filters on Silicon substrate," *IEEE Microwave and Wireless Components Letters*, vol. 12, pp. 429-431, Nov. 2002.

[14] D. M. Pozar, *Microwave Engineering 2nd*, published by Johnson Wiley & Sons, Inc, 1998.

[15] Troels Emil Kolding, "On-wafer calibration techniques for giga-hertz CMOS measurements," in *Proc. ICMTS*, March 1999, pp. 105-110.

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[1]. Hung-Ta Tso and Chien-Nan Kuo, “On-chip interconnect of high slow-wave-factor CPS structure in nano-CMOS technology,” in *Proc. of ISNCGS*, Feb. 2004.

[2]. Hung-Ta Tso and Chien-Nan Kuo, “40GHz miniature bandpass filter design in standard CMOS process,” in *Proc. of IEEE Topical Meeting on Silicon Monolithic IC in RF Systems*, 2004.