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電子工程學系電子研究所

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高電壓橫向擴散金氧半電晶體中

暫態熱載子效應與元件模型之探討

Investigation of Transient Hot Carrier Stress and Device Modeling Issues in High-Voltage Lateral Diffused Metal-Oxide-Semiconductor Field Effect Transistors

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摘要

隨著電源管理日趨重要，橫向擴散金氧半導體場效電晶體(LDMOS)於高電壓整合型電路中的使用也日趨廣泛。在高功率的操作下，熱載子引發的可靠性問題及元件模型的建立仍然是最大挑戰。

本篇論文將針對 LDMOS 的可靠度與元件模型的建立做一系列探討。首先，吾人提出一個具有特殊接觸電極的 LDMOS 結構，藉以量測 LDMOS 中通道(channel)部分的內部電壓(internal voltage)、電流、與低頻雜訊。兩個利用此種特殊結構的例子將在第二章中被討論；一個是對自我加熱效應(self-heating effect)的研究，另一個是對通道電流與 LDMOS 電流的特性分析。在自我加熱效應的研究中，吾人提出一個以內部電壓為觀察指標的研究方式，觀察到自我加熱效應所引發的暫態電壓改變將呈現兩段式變化。我們的研究也顯示出，內部電壓量測法將比傳統電流量測法更有效率，並能更清楚得到所需要的熱時間常數。在另一個例子中，此特殊結構將用來研究通道與 LDMOS 間的特性。電流與低頻雜訊在通道中與在 LDMOS 中的特性將被研究。我們的研究顯示，在低閘極偏壓下，汲極電流與汲極低頻雜訊主要是由 LDMOS 中的通道所決定，這也暗示了一個新的元件模型建立方法與熱載子(hot carrier)特性分析方法。

在第三章中，針對熱載子效應所導致的氧化層傷害，吾人提出一個新式三段式電荷幫浦(three-region charge pumping)的量測方法加以研究。利用此方法，我得以確認不同傷害模式下的氧化層損傷位置，並可以進一步知道所產生的損傷缺陷特性。我們的研究結果顯示，在最大閘極電流(max. I_G stress)模式下，將導致最大的汲極電流與次臨限區斜率(subthreshold slope)的退化，退化的原因為通道區的表面缺陷(interface trap)產生與鳥嘴區(bird's beak region)的負電荷量(negative oxide charge)累積，其產生的速度將可從三段式電荷量測幫浦中個別萃取。同時，我們也將利用二維元件模擬與低頻雜訊量測方法進一步確認實驗結果。

經由前面章節的了解，在第四章中，吾人將利用特殊結構研究自我加熱效應所引發的暫態熱載子效應(transient hot carrier effect)。同時，利用二維元件模擬驗證實驗結果，並用來分析交流頻率與元件退化間的關聯性。吾人研究結果發現，熱載子效應在交流偏壓下的電流退化，將比直流偏壓下的電流變化更為嚴重，其原因在於自我加熱效應的消失將造成熱載子的增加。

最後，吾人發展出一個雙組合元件模型(a two-component device model)，用來描述 LDMOS 的電流特性，並將模擬自我加熱效應所引發的內部電壓改變。此 LDMOS 模型將使用一種新的模型建立方法，以低閘極/高閘極電流分別建立通道區與淡摻雜區(drift region)的模型。並利用內部電壓控制有/無自我加熱效應下的汲極電流。經由比較後發現，我們的模型在所有的操作電壓下均可以準確的預測汲極電流，這範圍包含次臨限區(subthreshold)到臨限區以上(super-threshold)、有自我加熱情形及無自我加熱情形都可準確描述。

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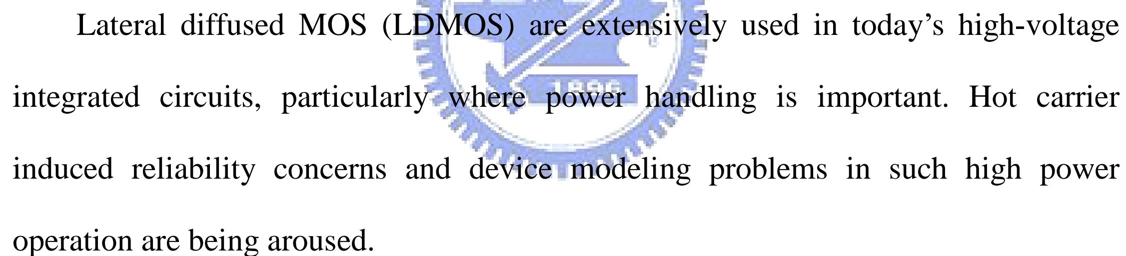
Abstract



Lateral diffused MOS (LDMOS) are extensively used in today's high-voltage integrated circuits, particularly where power handling is important. Hot carrier induced reliability concerns and device modeling problems in such high power operation are being aroused.

The objective of this dissertation is to investigate both reliability and device modeling issues in LDMOS transistors. First of all, a novel LDMOS structure incorporating an additional metal contact in the drift region is fabricated, which allows us to probe internal voltages, currents, and flicker noise in the channel-part of a LDMOS. Two examples of making use of this structure are presented in Chapter 2; one is a study for self-heating effect and the other is a characterization between channel and LDMOS currents. In the self-heating study, an internal voltage method to characterize self-heating effect is proposed. We find that a self-heating induced internal voltage transient exhibits two stages. The time constants of self-heating are

measured. Our study shows that the internal voltage method is more sensitive to self-heating than a conventional drain current method in a LDMOS. In the other example, the metal contact structure is used to investigate the channel and the LDMOS characteristics. Current and flicker noise in the channel and in the LDMOS are measured. Our experiments show that both drain current and drain flicker noise at low-V_G regime are major determined by the channel-part of a LDMOS, which imply a new extraction method for device modeling and a characterization technique for hot carrier effects.

In Chapter 3, hot carrier stress induced oxide degradation in n-LDMOS is investigated by using a novel three-region charge pumping technique. This technique allows us to locate oxide damage area in various stress modes and gain insight into trap creation properties. Our characterization shows that a max. I_G stress causes a largest drain current and subthreshold slope degradation because of both interface trap (N_{it}) generation in the channel region and negative bulk oxide charge (Q_{ox}) creation in the bird's beak region. The density of N_{it} and Q_{ox} can be separately extracted from the proposed charge pumping method. A numerical device simulation and drain flicker noise are performed to confirm our result.

Based on the understanding of Chapter 3, self-heating induced transient hot carrier effects are investigated in Chapter 4 by using the metal-contact structure introduced in Chapter 2. The AC stress-frequency dependence of device degradation is characterized and evaluated by a two-dimensional numerical simulation. Our result shows that drain current degradation in AC stress is more serious than in DC stress because of the reduction of self-heating effect.

Finally, a two-component device model including self-heating induced internal voltage transient in a LDMOS is developed. A new modeling method for the channel/drift regions is proposed by fitting a low-V_G/high-V_G drain current. Our

modeling method uses an internal voltage to control drain current in self-heating and in non-self-heating conditions. A comparison with dc measurements shows that our model provides an accurate description in all regimes of operation, ranging from subthreshold to super-threshold, for both self-heating and non-self-heating conditions.

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Contents

Chinese Abstract i

English Abstract iii

Acknowledgement vi

Contents vii

Figure Captions x

Table Captions xvi

List of Symbols xvii

Chapter 1 **Introduction** 1

1.1 Backgrounds 1

1.2 Organization of the Dissertation 3

Chapter 2 **A Novel Metal Contact Structure for Self-Heating Effect and Device Characterization** 8

2.1 Introduction 8

2.2 An Internal Voltage Method to Characterize Self-Heating 9

2.2.1 Internal Voltage Transient 10

2.2.2 Comparison of V_I Method and Conventional I_D Method 11

2.3 Comparison of Channel and LDMOS Characteristics 11

2.3.1 I-V Characteristics 12

2.3.2 Flicker Noise Characteristics 12

2.4 Summary 14

Chapter 3	**Physics and Characterization of Various Hot-Carrier Degradation Modes in LDMOS by Using a Three-Region Charge-Pumping Technique**	25
	3.1 Introduction	25
	3.2 Three-region Charge Pumping Measurement	27
	3.3 Flicker Noise Measurement	28
	3.4 Various DC Hot Carrier Stress Modes	29
	3.3.1 Maximum I_B Stress Mode	29
	3.3.2 V_G ~ (1/2) V_D Stress Mode	30
	3.3.3 Maximum I_G Stress Mode	31
	3.5 Summary	32
Chapter 4	**Impact of Self-Heating Effect on Hot Carrier Degradation in High-Voltage LDMOS**	55
	4.1 Introduction	55
	4.2 Self-Heating Characterization	56
	4.3 Degradation Characteristics in AC/DC Stress	57
	4.4 Summary	58
Chapter 5	**A Two-Component LDMOS Model including Self-Heating Effect**	74
	5.1 Introduction	74
	5.2 Model Description	75
	5.3 A New Modeling Method	76
	5.3.1 MOS Model	76

5.3.2 V_I Controller Model 77

5.3.3 Self-Heating Model 78

5.4 Results and Discussions 78

5.5 Summary 79

Chapter 6 Conclusion and Future Work 94

6.1 Conclusion 94

6.2 Future Work 95

Appendix A List of MOS Parameters 97

Appendix B SPICE Model Implementation Example 101

Appendix C Derivation of V_{Isat} 104

References 105

Vita 114

Publication Lists 115

Figure Captions

Chapter 1

Fig. 1.1 Applications of power devices in relation to their voltage and current ratings, from [1.1]. 5

Fig. 1.2 Applications of power semiconductor devices provided as a function of system operating frequency and power handling capability, from [1.1]. 6

Fig. 1.3 The organization of the dissertation. 7

Chapter 2

Fig. 2.1 Top view of a novel metal contact structure. Three different regions are indicated by L_{ch} (channel region), L_{acc} (accumulation region), and L_{FOX} (field-oxide region). A contact (V_I) is placed in the accumulation region. 15

Fig. 2.2 Cross-section of the metal contact structure to characterize self-heating effect. The cross-section is plotted from the line (A-A') in Fig. 2.1. The metal contact (V_I) is arranged in the bird's beak region with an n^+ implant. 16

Fig. 2.3 Measured internal voltage (V_I) transient due to self-heating. V_D is 40V. The gate voltage is switched from 15V to 40V at t=0μs. Two-stage transient is noticed. 17

Fig. 2.4 Simulated temperature distribution along the device at V_D=40V and V_G=40V. 18

Fig. 2.5 (a) Internal voltage versus drain voltage with and without self-heating effect. The full squares (w/ SHE) are obtained by Agilent 4156 while the open squares (w/o SHE) are obtained from the measurement setup in Fig. 2.2. (b) Drain current versus drain voltage measured by Agilent 4156 (full squares) and by an external resistor method (open squares). 19

Fig. 2.6 Drain current versus internal voltage in a LDMOS. The reduction of V_I and 20

I_D due to self-heating is denoted by ΔV_I and ΔI_D, respectively.

Fig. 2.7 I_D-V_D in LDMOS and in the proposed new structure. (a) At lower V_G (V_G<10V). (b) At higher V_G (V_G>10V). 21

Fig. 2.8 I-V Measurement setup for device characterization. The V_I is measured by forcing a zero current in SMU 3. V_G/V_D are given by Agilent 4156. 22

Fig. 2.9 Comparison of metal-contact structure (I_D-V_D) characteristics and channel part of metal-contact structure (I_D-V_I) characteristics. (a) At lower V_G. (b) At higher V_G. 23

Fig. 2.10 Noise power spectrum density versus current flow in LDMOS, channel part of the LDMOS, and drift-region part of the LDMOS. (a) V_G=2V, (b) V_G=9V, and (c) V_G=18V. 24

Chapter 3

Fig. 3.1 (a) Cross-section of a n-LDMOS and flat-band (solid line) and threshold (dash line) voltage distributions. The device is divided into three parts, i.e., 1) L_{chan} (channel region), 2) L_{acc} (accumulation region), and 3) L_{fox} (field oxide region). (b) Illustration of a charge pumping measurement waveform. V_{gh}=12V is fixed and V_{gl} varies from +3.6V to -40V. 34

Fig. 3.2 Typical CP current in a n-LDMOS. The three stages of the CP current correspond to the three regions of the device. The flat-band voltage of each region is indicated in the figure. The frequency in charge pumping measurement is fixed at 200 kHz. 35

Fig. 3.3 Power spectrum density (S_I) at a lower V_G (V_G=2V) and at a higher V_G (V_G=18V). Solid and empty symbols represent the measurement results in LDMOS and in channel region, respectively. 36

Fig. 3.4 Gate current versus gate voltage in a LDMOS. Stress modes A (maximum 37

I_B), B (V_G~1/2V_D), and C (maximum I_G) are indicated.

Fig. 3.5 (a) Charge pumping current versus V_{gl} before and after 1400 sec. mode A stress. (b) Two-dimensional device simulation of impact ionization generation (IIG) distribution in stress mode A. 38

Fig. 3.6 Comparison of normalized low flicker noise before and after mode A stress. (a) At a lower V_G (V_G=2V) and (b) at a higher V_G (V_G=18V). 39

Fig. 3.7 (a) Charge pumping current versus V_{gl} before and after 1400 sec. mode B stress. The shift of the flat-band voltage in stage 2 implies the generation of negative oxide charge in the accumulation region. (b) Two-dimensional device simulation of impact ionization generation (IIG) in stress mode B. 40

Fig. 3.8 The charge pumping results in stress mode B for different stress times. 41

Fig. 3.9 Region (II) oxide-trapped charge growth rate in stress mode B. 42

Fig. 3.10 Linear drain current degradation (I_{dlin}) rate measured at V_G/V_D=40V/0.1V in stress mode B. 43

Fig. 3.11 Comparison of normalized low flicker noise before and after mode B stress. (a) At a lower V_G (V_G=2V) and (b) at a higher V_G (V_G=18V). The increase of (S_{id}/I_d^2) at a higher V_G is attributed to the creation of negative oxide charge in the accumulation region. 44

Fig. 3.12 (a) Charge pumping current before and after 1000 sec. mode C stress. Upward shift in stage 1 I_{cp} indicates interface trap generation in the channel and rightward shift in stage 2 I_{cp} implies oxide charge creation in the 45

accumulation region. (b) Two-dimensional device simulation of impact ionization generation (IIG) distribution in stress mode C. Two IIG regions are found; One is in the channel region and the other is in the accumulation region.

Fig. 3.13 Comparison of normalized flicker noise before and after mode C stress. (a) At a lower V_G (V_G=2V) and (b) at a higher V_G (V_G=18V). The increase of (Sid/Id^2) at a lower V_G and at a higher V_G are attributed to the creation of N_{it} in the channel and Q_{ox} in the drift region, respectively. 46

Fig. 3.14 Subthreshold characteristics before and after mode C stress. The swing degradation is attributed to interface trap generation in the channel region. 47

Fig. 3.15 The linear drain current versus V_G before and after mode C stress. 48

Fig. 3.16 Simulated drain current versus gate voltage without and with oxide charges. (a) The oxide charge is placed in the channel and (b) the oxide charge is placed in the bird's beak region. 49

Fig. 3.17 Region (I) interface trap growth rate in stress mode C. 50

Fig. 3.18 Region (II) oxide charge growth rate in stress mode C. 51

Fig. 3.19 I_{dlin} degradation versus stress time in stress mode C. The degradation is mainly caused by negative oxide creation in the drift region. 52

Fig. 3.20 Impact ionization generation rate in (a) Max. I_B stress mode, (b) V_G~1/2V_D stress mode, and (c) Max. I_G stress mode. 54

Chapter 4

Fig. 4.1 Fast transient measurement setup for drain current and internal voltage (V_I) characterization. The resistance (10Ω) is small than the total resistance (~40V/10mA ~4kΩ). A gate pulse and constant V_D are used. 60

Fig. 4.2 (a) Normalized drain current (I_D/W) versus drain voltage in small and large gate width devices in DC measurement (Agilent 4156). (b) The I_D/W from a DC and a fast transient measurement for the large width device. 61

Fig. 4.3 Internal voltage versus gate voltage measured by Agilent 4156 and by a transient measurement setup. 62

Fig. 4.4 Substrate current and gate current versus gate voltage in a LDMOS. Two hot carrier stress modes are shown, maximum I_B stress and maximum I_G stress. 63

Fig. 4.5 Linear drain current degradation (V_G/V_D= 40V/0.1V) in two hot carrier stress modes. DC and AC stresses have the same cumulative stress time. AC stress has a frequency of 20kHz and a duty cycle of 10%. 64

Fig. 4.6 (a) I_{dlin} degradation versus stress frequency with a duty cycle of 10%. A corner frequency (*f1*) is around 20kHz. (b) I_{dlin} degradation versus duty cycle for a frequency of 20 kHZ. 65

Fig. 4.7 I_{dlin} degradation versus pulse duration (=duty cycle/frequency) in AC stress. The corner time is around 5μs. 66

Fig. 4.8 The internal voltage (V_I) transient in a pulsed gate and DC drain voltage 67

(V_D=40V) condition. The waveforms of V_I and V_G are plotted. The onset time for SHE is ~5μs.

Fig. 4.9 Three-region charge pumping measurement results after maximum I_G AC and DC stress. A V_{gL} shift is in the accumulation region and a I_{cp} increase is in the channel region. 68

Fig. 4.10 Substrate current and gate current versus gate voltage for different temperatures. 69

Fig. 4.11 Simulation of a temperature distribution with SHE. The ambient temperature is 300K. X axis is the direction from source to drain. Y axis represents the depth. (a) V_G/V_D=10V/40V. (b) V_G/V_D=40V/40V. 70

Fig. 4.12 Internal voltage change (V_I(non-SHE)-V_I(SHE)) versus gate voltage from measurement and from simulation. 71

Fig. 4.13 Two-dimensional device simulation of impact ionization generation (IIG) rate at V_G/V_D=40V/40V. (a) SHE is included and (b) SHE is not included. 72

Fig. 4.14 I_{dlin} degradation rate after AC and DC stress in maximum I_G stress condition. The AC stress frequency is 20 kHz and the duty cycle is 10%. 73

Chapter 5

Fig. 5.1 (a) An equivalent circuit of the LDMOS model. An internal voltage (V_I) between two circuit elements is illustrated. The MOS element represents the channel region while the V_I controller accounts for the drift region. (b) 80

Illustration of different operating regions controlled by each component.

Fig. 5.2 Illustration of input/output process of the LDMOS model. The V_I is controlled by V_G and V_D. The I_D is determined by V_I and V_G. 81

Fig. 5.3 Illustration of the V_I controller. An internal voltage transient due to self-heating (SH) is taken into account. The V_I at $t=0^+$ is expressed as a function of V_G and V_D (listed in Equation 1). The ΔV_I transient is described by a RC network in Fig. 5.9. 82

Fig. 5.4 A new modeling method for the MOS element and the V_I controller. Five extraction steps are indicated, including (1, 2) MOS model, (3) V_I simulation step, (4) V_I controller model, and (5) LDMOS macro-model. 83

Fig. 5.5 A V_I simulation method in step 3. Each measured I_D can extract a simulated V_I. Typical V_I simulation is shown in the inset under self-heating (w. SH) and non-self-heating (w/o SH) conditions. The MOS model is obtained from step 1 and 2. This method is performed by a HSPICE simulator. 84

Fig. 5.6 A comparison of a fitting result during the extraction step of the MOS model. The I_D-V_G is measured from a LDMOS. The I_{ch}-V_G is obtained from the MOS model performed by a HSPICE simulator. 85

Fig. 5.7 A comparison of fitting results during the extraction step of the MOS model. (a) At lower V_G. (b) At higher V_G. The I_D-V_D is measured from a LDMOS. The I_{ch}-V_I is obtained from the MOS model. A match between LDMOS and MOS model means no voltage drop in the drift region and thus $V_I=V_D$. A 86

mismatch at V_G=40V indicates a voltage drop in the drift region and thus V_I is much smaller than V_D as current flow is the same.

Fig. 5.8 A comparison of V_I controller model in a non-SH condition. Symbol is the V_I obtained from the V_I simulation method. Line represents a simulation result of the V_I controller model. (a) V_I-V_D. (b) V_I-V_G. 87

Fig. 5.9 A RC network to describe self-heating induced internal voltage transient ($\Delta V_I(t)$). Three components are used, including a current source, a resistor R, and a capacitor C. 88

Fig. 5.10 I_D transient and a corresponding V_I simulation performed by the V_I simulation method. β indicates a difference of V_I transient due to self-heating. τ_C represents a time constant of V_I transient. 89

Fig. 5.11 A comparison of V_I transient at V_G/V_D=40V/40V. Line represents the V_I obtained from the V_I simulation method. Dash represents the V_I obtained from the V_I controller model. A fitting result of $\Delta V_I(t)$ is also indicated. 90

Fig. 5.12 A comparison of I_D transient between measurement and our macro-model. 91

Fig. 5.13 A comparison of I_D-V_D between measurement and our macro-model. (a) At lower V_G. (b) At higher V_G. The I_D in SH and non-SH conditions are extracted from I_D transient as $t=0^+$ and t=30μs. 92

Fig. 5.14 A comparison of I_D-V_G between measurement and our macro-model. (a) In the linear region (V_D=0.1V). (b) In the saturation region (V_D=40V). 93

Table Captions

Chapter 3

Table 3.1 Summary of major oxide and device performance degradations in various stress modes. 53

List of Symbols

C	Capacitance
f	Frequency
G_m	Trans-conductance
I_G	Gate current
I_B	Substrate current
I_D	Drain current
I_{ch}	Channel current
I_{cp}	Charge-pumping current
L_{ch}	Channel length
L_{acc}	Accumulation region length
L_{fox}	Field oxide region length
N_{it}	Interface trap
Q_{ox}	Bulk oxide charge
q	Electronic charge
R	Resistor
S_{Id}	Drain current noise power spectrum density
τ_{on}	Onset time of a self-heating effect
τ_s	Saturation time of a self-heating effect
τ_C	Corner time constant of self-heating effect
V_G	Gate voltage
V_D	Drain voltage
V_{gh}	High-level voltage of voltage waveform
V_{gl}	Low-level voltage of voltage waveform
V_{FB}	Flat-band voltage
V_I	Internal voltage of LDMOS
$V_{I,eff}$	Effective internal voltage
V_{TH}	Threshold voltage
W	Channel width
ΔN_{it}	Change in interface trap
ΔI_{cp}	Change in charge-pumping current
ΔQ_{ox}	Change in bulk oxide charge
ΔV_{FB}	Change in flat-band voltage
ΔV_I	Change in internal voltage
β	Change of V_I due to self-heating effect
μ_0	Mobility
v_{sat}	Saturation velocity

Chapter 1

Introduction

1.1 Backgrounds

The increasing applications of high-voltage integrated circuits force the continuous evolution of modern power semiconductor devices. The first applications of power integrated circuits, about 40 years ago, were in voltage regulators and audio amplifiers [1.1]. A monolithic integrated circuit that combines power and signal circuitry on a chip is developed to reduce electronic products size, weight, and cost. Nowadays, power devices are presented in various applications. Fig. 1.1 shows applications for power semiconductor, where the boxes indicate the device voltage and current ratings required from system [1.2]. The power devices at relatively lower voltages (<100V) and current levels (<10A) are usually integrated with control circuits [1.3]. At higher power levels, such as in traction and high voltage DC transmission systems, the systems are implemented using discrete components [1.3].

From operating frequency point of view, power thyristors, bipolar power transistors, and power MOSFET play different roles in the development of power devices. A comparison of operating frequency for different applications is illustrated in Fig. 1.2. The power devices used in the applications are indicated in the figure. Power thyristors are designed for blocking voltage above 6000V and have relatively slow switching speed [1.3]. These devices are suitable for systems with low operating frequency. Two examples of such applications are high voltage direct current (HVDC) power transmission networks and high power motor drives used in steel mills [1.2]. For relatively lower blocking voltage and higher operating frequency, bipolar power transistors become more attractive. The blocking voltage of these devices has been

extended to 500V ~ 1200V with operating frequency of ~50kHz [1.3]. As system operating frequency is much higher, power MOSFET transistor provides a better solution and simplicity control. These devices are operated at frequency above 100 kHz and the blocking voltages are less than 200V [1.4].

In addition, an integrated bipolar, CMOS, and power DMOS (BCD) technology has been developed in the mid eighties. This technology allows the integration of a wide variety of high-voltage device structures [1.5]. Among the candidates of high-voltage devices, lateral diffused MOS (LDMOS) transistors are attractive because the advantage of process compatible to CMOS technology. The LDMOS has been widely used in today's high-voltage and high-current output circuits [1.6], from a standard 12-V automotive battery [1.7] to 100-V plasma display panel drivers [1.8].

Several issues in LDMOS transistors are presented, including (a) hot carrier degradation induced reliability constraint [1.9] [1.6], (b) high power induced temperature rising or self-heating effect [1.10] [1.11], and (c) device modeling [1.12]. Since an LDMOS processes an intrinsic channel region and a lightly doped drift region, its hot carrier degradation mechanisms are different from a traditional MOSFET. The lightly-doped drift region was reported to be the major limitation for hot carrier degradation because of a specific double-hump substrate current behavior [1.9]. Besides, an increasing voltage/current in a LDMOS tends to raise device operating temperature and result in self-heating effect (SHE). Anghel et al. found that the degree of SHE in a LDMOS is determined by the applied pulse frequency and duty cycle [1.10]. Roux et al. [1.13] reported that this frequency-dependence SHE results in erroneous lifetime prediction and a correction is required in SOI technology. Similarly, SHE is also significant in a LDMOS. The correlation between SHE and hot carrier degradation in a LDMOS should be considered.

SHE is also important to the device modeling because of a non-uniform

temperature distribution in a LDMOS [1.14]. Larger voltage drop across the lightly-doped drift region causes a higher temperature rising in this area [1.15]. A temperature difference between the channel and drift regions leads to an internal voltage change in a LDMOS [1.15]. This SHE induced internal voltage change, however, cannot be described by a conventional SHE model [1.10] [1.16]. Thus, a new SHE model, which considers both the non-uniform temperature distribution and SHE induced internal voltage change, is necessary.

1.2 Organization of the Dissertation

The organization of this dissertation is schematically illustrated in Fig. 1.3. A novel LDMOS structure incorporating a metal contact in the bird's beak region is fabricated and will be described in detail in Chapter 2. With the use of the metal contact structure, internal voltages during the device operation are retrieved. A comparison of I-V characteristics between LDMOS and channel-part of LDMOS is discussed in Chapter 2. In addition, an internal voltage transient due to self-heating effect is also investigated in Chapter 2 and modeled in Chapter 5.

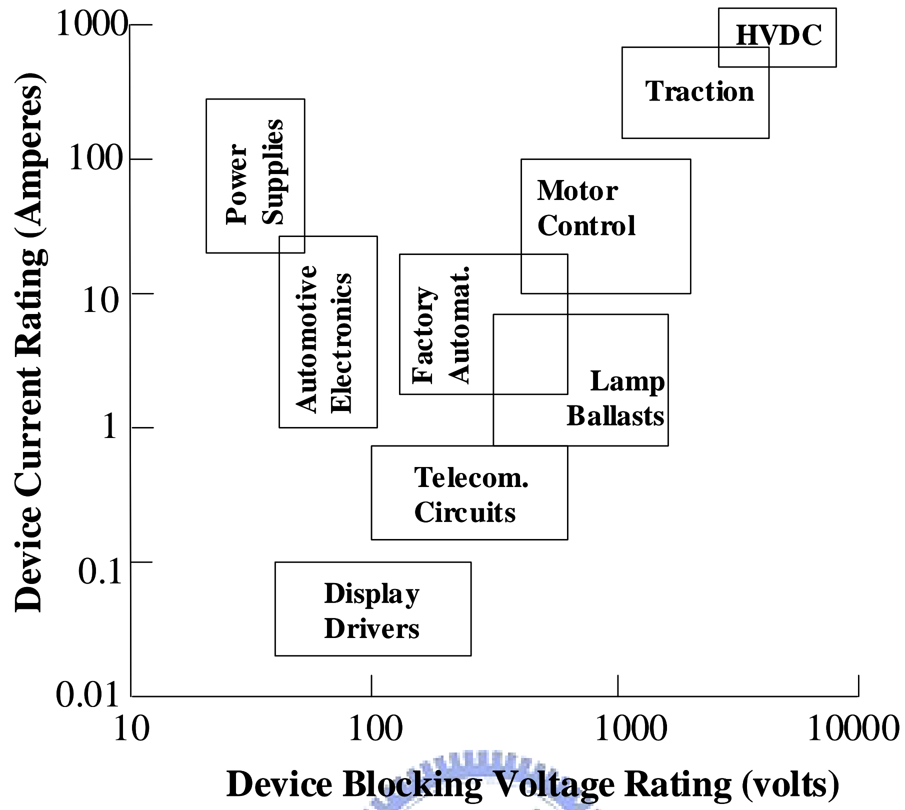
In Chapter 3, degradation of lateral diffused MOS transistors in various DC hot-carrier stress modes is investigated. A novel three-region charge-pumping technique is proposed to characterize interface trap (N_{it}) and bulk oxide charge (Q_{ox}) creation in the channel and in the drift regions separately. The growth rates of N_{it} and Q_{ox} are extracted from the proposed method. A two-dimensional numerical device simulation is performed to gain insight into device degradation characteristics in different stress conditions. The impact of oxide trap property and location on device electrical characteristics is analyzed from measurement and simulation.

In Chapter 4, self-heating induced transient hot carrier effects in high-voltage n-LDMOS are investigated. A novel LDMOS structure incorporating a metal contact

in the bird's beak region is utilized, which allows us to probe an internal voltage transient in hot carrier stress. The AC stress-frequency dependence of device degradation is characterized and evaluated by a two-dimensional numerical simulation.

In Chapter 5, an internal-voltage-based LDMOS SPICE model including self-heating effect is proposed. Our model combines a low-voltage MOS element with a high-voltage controller. The MOS parameters are extracted from the LDMOS I-V data in the low-V_G region and in the linear portion of the high-V_G region. A new SHE model, describing an internal-voltage transient rather than a temperature rise, is developed. Modeling results of self-heating and non-self-heating drain currents at various V_G and V_D are also compared.

Conclusions are finally made in Chapter 6.



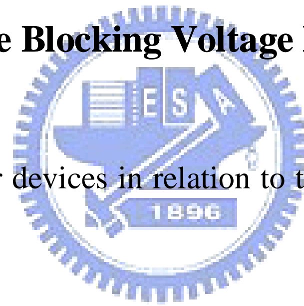


Fig.1.1 Applications of power devices in relation to their voltage and current ratings, from [1.1].

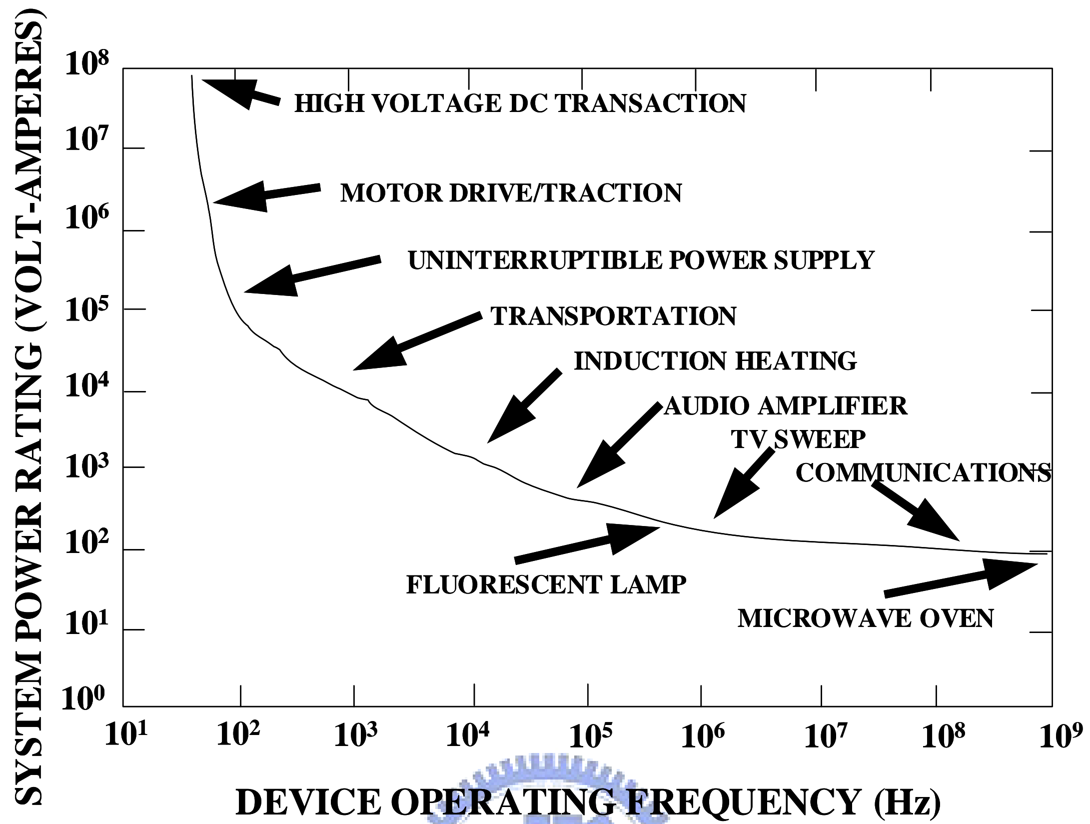


Fig. 1.2 Applications of power semiconductor devices provided as a function of system operating frequency and power handling capability, from [1.1].

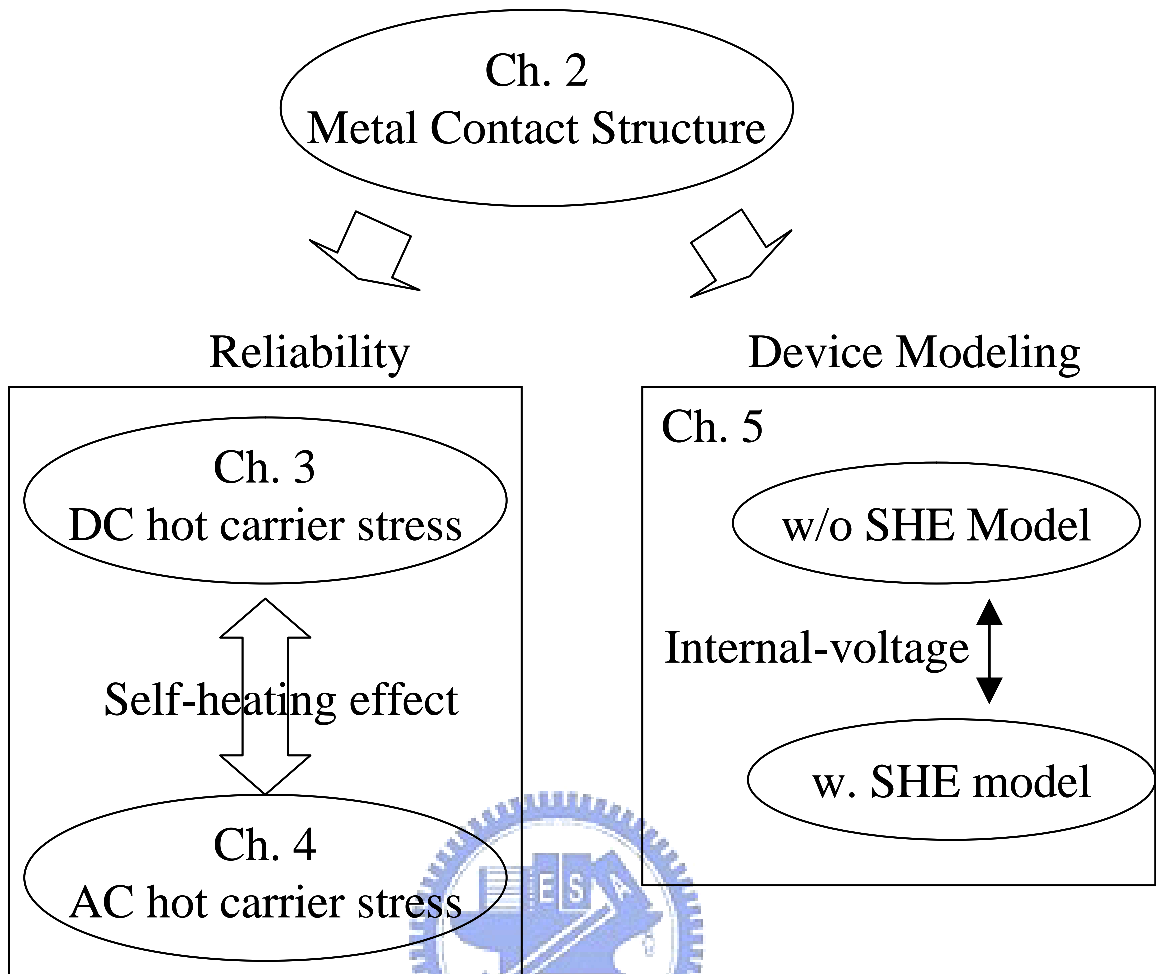


Fig. 1.3 The organization of this dissertation.

Chapter 2

A Novel Metal-Contact Structure for Self-Heating Effect and Device Characterization

2.1 Introduction

Integration of logic and power devices on the same chip has attracted much attention in recent years [2.1] [2.2]. Many applications, such as power management and RF-applications, require a high voltage/high current operation in the power devices. Among the candidates of high-voltage devices, lateral diffused MOS (LDMOS) transistors are attractive because they can be easily integrated with standard low-voltage CMOS process. A lightly doped area with the use of RESURF (reduced surface field) principle [2.3] is generally adopted in the LDMOS, which can support a high drain-to-source breakdown voltage [2.4] and reduce the device dimension. However, continuous increase in power density with the lightly doped area scaling is now seriously challenged in the progression of CMOS and LDMOS technology [2.5] [2.6]. As power consumption increases, hot carrier degradation [2.7] and self-heating effect [2.8] become two most formidable limitations in the LDMOS. The enhanced self-heating effect may cause a snapback breakdown and result in a thermal runaway in the LDMOS [2.5]. In addition, Roux [2.9] reported that self-heating effect may also result in erroneous lifetime prediction in hot carrier stress condition. The correlation between hot carrier degradation and self-heating effect becomes important to the study of the LDMOS.

To characterize these physical phenomena, we proposed a novel metal contact LDMOS structure to get insight into the device I-V characteristics and self-heating effect. Fig. 2.1 shows the top view of a metal contact LDMOS structure. The device

was processed in a 0.18μm CMOS technology with a gate oxide thickness of 100nm and a field-oxide thickness of 500nm. A small metal contact (V_I), as compared to the device width, is placed in the drift region. Parts of the N-Well and field-oxide regions are controlled by the poly-gate because of the use of RESURF (reduced surface field) principle [2.3]. An internal voltage change in a normal LDMOS operation will be measured from the V_I. Since the complexity of the LDMOS behavior is mostly occurred in the lightly doped drift region, the fabrication of the V_I allows us to distinguish the I-V characteristics in the channel and drift regions. In this way, the channel region can be regarded as an intrinsic MOS and the drift region can be considered as a resistance. Thus, the physical effects that take place in the LDMOS can be easily understood and explained in the studies.

2.2 An Internal Voltage Method To Characterize Self-Heating

Self-heating effect (SHE) has been observed in laterally diffused metal-oxide-semiconductor (LDMOS) transistors [2.10] [2.11], particularly when the device is operated in high-voltage/high-current circuits. This effect results in an increase of device local temperature and thus a reduction of the drain current. To characterize SHE, a conventional drain current (I_D) method [2.11] [2.12] [2.13] [2.14] is usually adopted. In an I_D method, a short voltage pulse is applied to the gate and the drain current transient resulting from self-heating is extracted from a voltage drop across an external resistor [2.11] [2.13] [2.14]. In the I_D measurement, the bias at the drain must be continually adjusted to compensate for the voltage drop across the external resistor [2.15], added to determine the drain current. The adjustment of the drain voltage, however, may lead to an ambiguous thermal time constant and result in a questionable SHE study and SPICE modeling. In addition, the drain current in the saturation region is rather insensitive to the change of a local temperature, which

makes an accurate self-heating measurement more difficult in a LDMOS. Here, we propose a more effective characterization method for SHE.

In our method, we measure a self-heating induced internal voltage (V_I) change rather than a drain current change. In this way, a series external resistor at the drain is not necessary. To the purpose, we fabricated a special LDMOS device. Fig. 2.2 shows the cross-section of the LDMOS structure, which incorporates a metal contact in the bird's beak region, thus allowing us to probe an internal voltage directly. The contact area is sufficiently small that the device electrical characteristics are not affected. The device used in this work was processed with a gate width of 20μm and a channel length of 3μm. The operational voltages are V_G =40V and V_D =40V.

2.2.1 Internal Voltage Transient

The measurement result of an internal voltage transient due to self-heating is shown in Fig. 2.3. A gate voltage pulse with a low-level voltage of 15V and a high-level voltage of 40V is applied. The low-level voltage of 15V is chosen to prevent V_I contact breakdown. The V_I transient exhibits two stages in Fig. 2.3. Two time-constants, τ_{on} and τ_s, are noted. In the initial stage ($t<\tau_{on}$), V_I remains nearly unchanged and τ_{on} (=~7μs) represents an onset time of a self-heating effect. In the second stage ($t>\tau_{on}$), V_I decreases with pulse time until a dynamic balance between heat generation and dissipation is reached. The saturation time of SHE is denoted by τ_s (=~32μs) in Fig. 2.3. The decrease of the V_I can be explained in the following. Fig. 2.4 shows the simulated temperature distribution along the device due to self-heating at V_G =40V and V_D =40V. In the simulation, a thermal electrode is placed at the bottom of the device and is assumed to be isothermal at 300°K. Homogeneous Neumann boundary conditions are used at all boundaries not contacted by the thermal electrode. A larger temperature rise in the drift region than in the channel region is

obtained because of a larger voltage drop in the drift region and thus higher power consumption. As a result, the decrease of V_I can be realized due to larger mobility degradation in the drift region. A decrease of V_I from 16.5V to 13V due to self-heating effect is observed.

2.2.2 Comparison of V_I Method and Conventional I_D Method

For comparison, self-heating induced V_I reduction and I_D reduction are shown in Fig. 2.5 (a) and (b), respectively. The open squares represent the result without SHE while the full squares are obtained in DC measurement (i.e., including SHE). The self-heating effect is more significant as V_D increases. In addition, a lager reduction in V_I than in I_D is obtained. For instance, at V_D=40V, self-heating induced ΔV_I is about 23% while the ΔI_D is only 8%, showing that the V_I method is more sensitive to self-heating than the conventional I_D method. The reason for the difference in the V_I method and the I_D method is shown in Fig. 2.6 by plotting the relation between measured I_D and V_I. Since the device is operated in the saturation region, I_D is weakly dependent on V_I. A large change in V_I only yields a small change in I_D.

2.3 Comparison of LDMOS/MOS Characteristics

One of the purposes of measuring V_I, as we have mentioned in section 2.1, is to compare the device characteristics in the channel region (intrinsic MOS) and in the LDMOS. The V_I is designed with dimensions much smaller than the device width, and thus no significant influence is expected on the I-V characteristics. Fig. 2.7 plots a comparison of the I_D-V_D characteristics between the LDMOS and the metal contact LDMOS (new structure). A good matching of the I_D-V_D characteristics shows no significant difference between the LDMOS and the metal contact structure, which assures no process variation in the following measurements.

2.3.1 I-V Characteristics

To compare the I-V characteristics in the intrinsic MOS and in the LDMOS, a measurement setup is illustrated in Fig. 2.8. A current mode (I Mode) is used in SMU3 for the purpose of probing a voltage drop in the channel region. A comparison of the LDMOS (I_D-V_D) and the intrinsic MOS (I_D-V_I) is shown in Fig. 2.9. As V_G is low (Fig. 2.9(a)), the I-V of the intrinsic MOS and the LDMOS in linear region and saturation regions are nearly the same. This feature implies that V_I is close to V_D and the LDMOS performance is dominated by the intrinsic MOS at low V_G. A similar comparison of the characteristics of the intrinsic MOS and the LDMOS in the high-V_G region is presented in Fig. 2.9(b). At small V_D, the drain current of the intrinsic MOS and the LDMOS are very close, indicting that the intrinsic MOS still dominates the LDMOS characteristics in the linear region. However, a significant current difference is observed in the saturation region, implying a large voltage drop in the drift region. Thus, the saturation characteristics of the device are controlled by both the intrinsic MOS and the drift region. In addition, Fig. 2.9 also implies two saturation mechanisms in the LDMOS; one is a classic saturation mechanism that takes place in the intrinsic MOS [2.8], and the other is a quasi-saturation mechanism which is determined by the saturation of the drift region [2.6].

The characterization also leads to a possible LDMOS modeling technique: We may use an intrinsic MOS model to control the low-V_G LDMOS characteristics and another component to model the device I-V in the high V_G region. This new modeling technique will be discussed in chapter 5.

2.3.2 Flicker Noise Characteristics

The use of the LDMOS in high power switches did not really require

low-frequency noise performance, but with the introduction of the applications, such as high-voltage digital cells and operational amplifiers, the flicker noise behavior has become important [2.16]. In this section, we used the V_I to characterize the flicker noise in the channel and drift regions. All noise measurements are biased at low V_G (V_G <18V) in the linear region to assure that number fluctuation mechanism dominates the noise behavior. In order to have a reasonable comparison, we adjusted the applied voltage drop in the channel region and in the drift region, which allow us to obtain the same order of the current flow. The flicker noise measurement system includes an Agilent 4156 semiconductor parameter analyzer, a BTA 9603 FET noise analyzer, and a SR780 network signal analyzer. All measurement is controlled automatically through GPIB by using a computer program named Cadence-NoisePro.

Fig. 2.10 shows a flicker noise measurement at different applied V_G. Each data point represents an average of 3 to 5 devices. As V_G is low (Fig. 2.10(a)), the S_{id} of drift region is small, which is attributed to thermal noise. In addition, the S_{id} of LDMOS at low V_G is nearly the same as the S_{id} of MOS, implying that the flicker noise of LDMOS at low V_G is major determined by the channel-part of the LDMOS. Compared to the I-V characteristics of Fig. 2.9(a), the I_D-V_I is close to the I_D-V_D at low V_G and thus the channel region dominates the LDMOS behavior at low V_G regime. At a large V_G (Fig. 2.10(b)(c)), the S_{id} of LDMOS appears to be controlled by both the channel region and the drift region. This feature is in agreement with the comparison of I-V characteristics in Fig. 2.9(b).

The measurement result of the flicker noise behavior also implies a new characterization method for hot carrier stress. By comparing the pre-stress and post-stress flicker noise at different V_G, we can identify the locations of oxide damage area in the device and corresponding trap properties. This approach will be utilized and discussed in the chapter 3

2.4 Summary

A novel metal-contact LDMOS structure is fabricated to investigate self-heating effect and LDMOS/MOS characteristics. A new technique for self-heating characterization has been proposed. This approach can probe a self-heating induced V_I change directly without adding an external resistor. The two-stage behavior of a V_I transient is noticed for the first time and explained. This method provides a higher resolution than a conventional I_D method. The characteristics of the channel part of the LDMOS, including the I-V characteristics and the flicker noise behaviors, are measured and compared to the LDMOS. Our measurement result shows that the drain current at low V_G regime is major determined by the channel-part of the LDMOS, whereas the drain current at high V_G regime is affected by both the channel region and the drift region. Similarly, the flicker noise behaviors at low V_G regime and at high V_G regime are controlled by the channel region and by both the channel region and the drift region, respectively.

Based on the comparison of the I-V characteristics, a new modeling methodology for LDMOS SPICE model is proposed. A two-component LDMOS model using the new methodology will be developed in chapter 5. In addition, we also proposed a noise characterization method to identify oxide damage area in various hot carrier stress modes. This method will be performed and discussed in chapter 3.

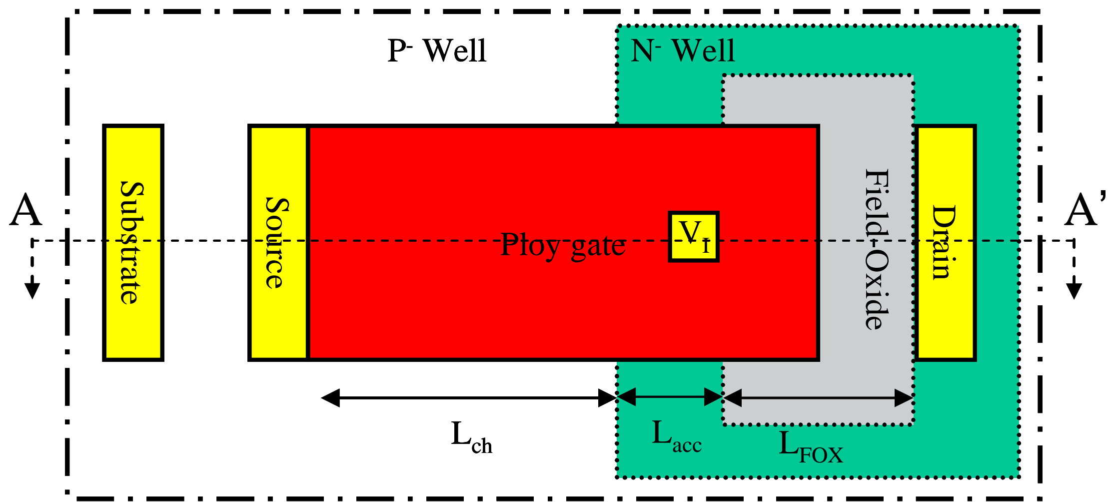


Fig. 2.1 Top view of a novel metal contact structure. Three different regions are indicated by L_{ch} (channel region), L_{acc} (accumulation region), and L_{FOX} (field-oxide region). A contact (V_I) is placed in the accumulation region.

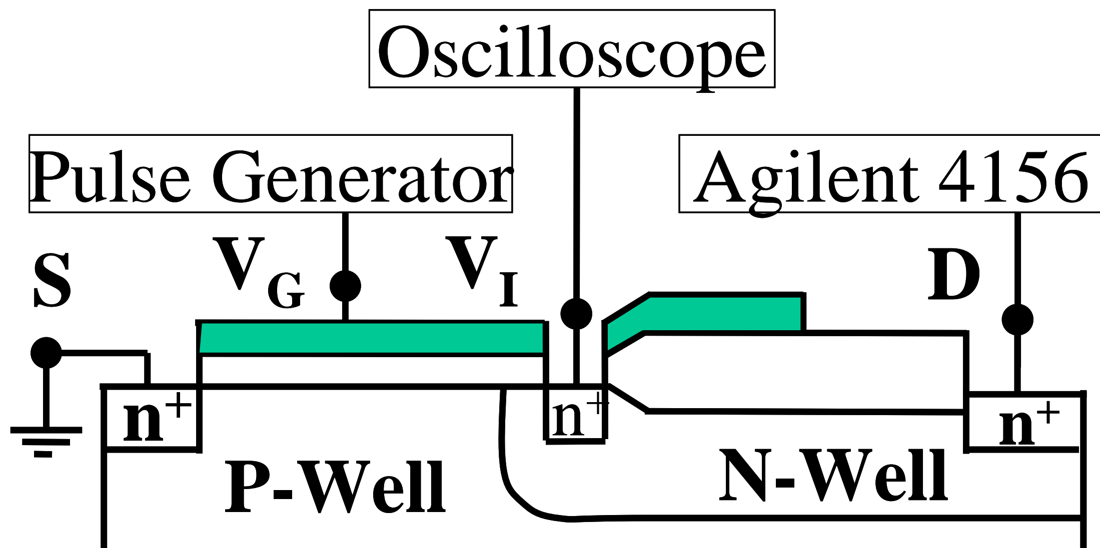
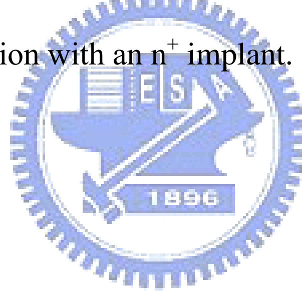


Fig. 2.2 Cross-section of the metal contact structure to characterize self-heating effect. The cross-section is plotted from the line (A-A') in Fig. 2.1. The metal contact (V_I) is arranged in the bird's beak region with an n^+ implant.



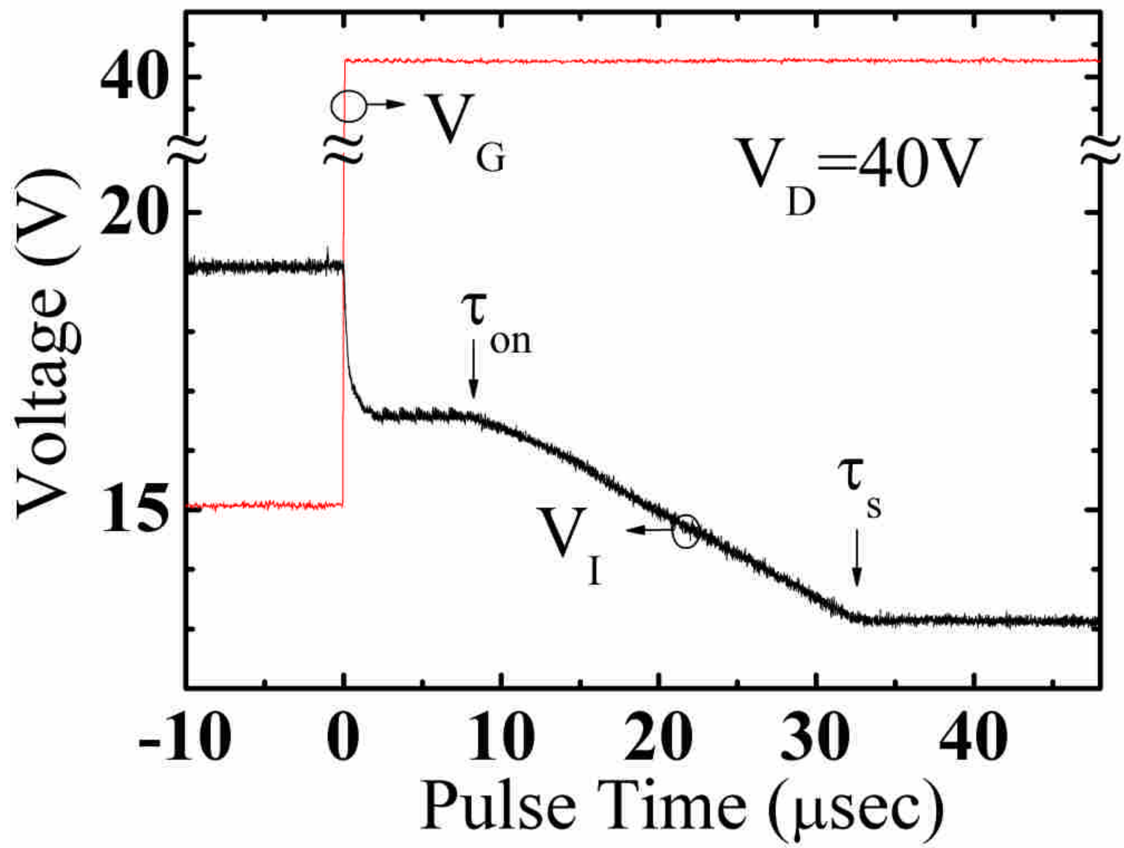


Fig. 2.3 Measured internal voltage (V_I) transient due to self-heating. V_D is 40V. The gate voltage is switched from 15V to 40V at t=0μs. Two-stage transient is noticed.

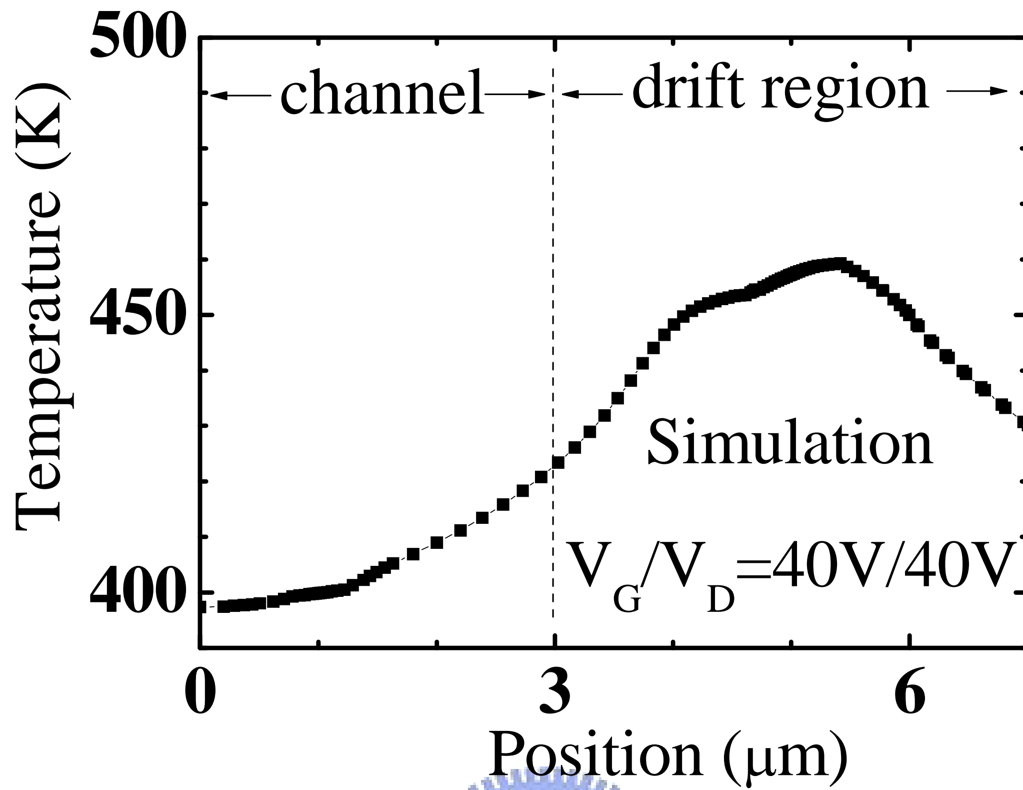


Fig. 2.4 Simulated temperature distribution along the device at V_D=40V and V_G=40V.

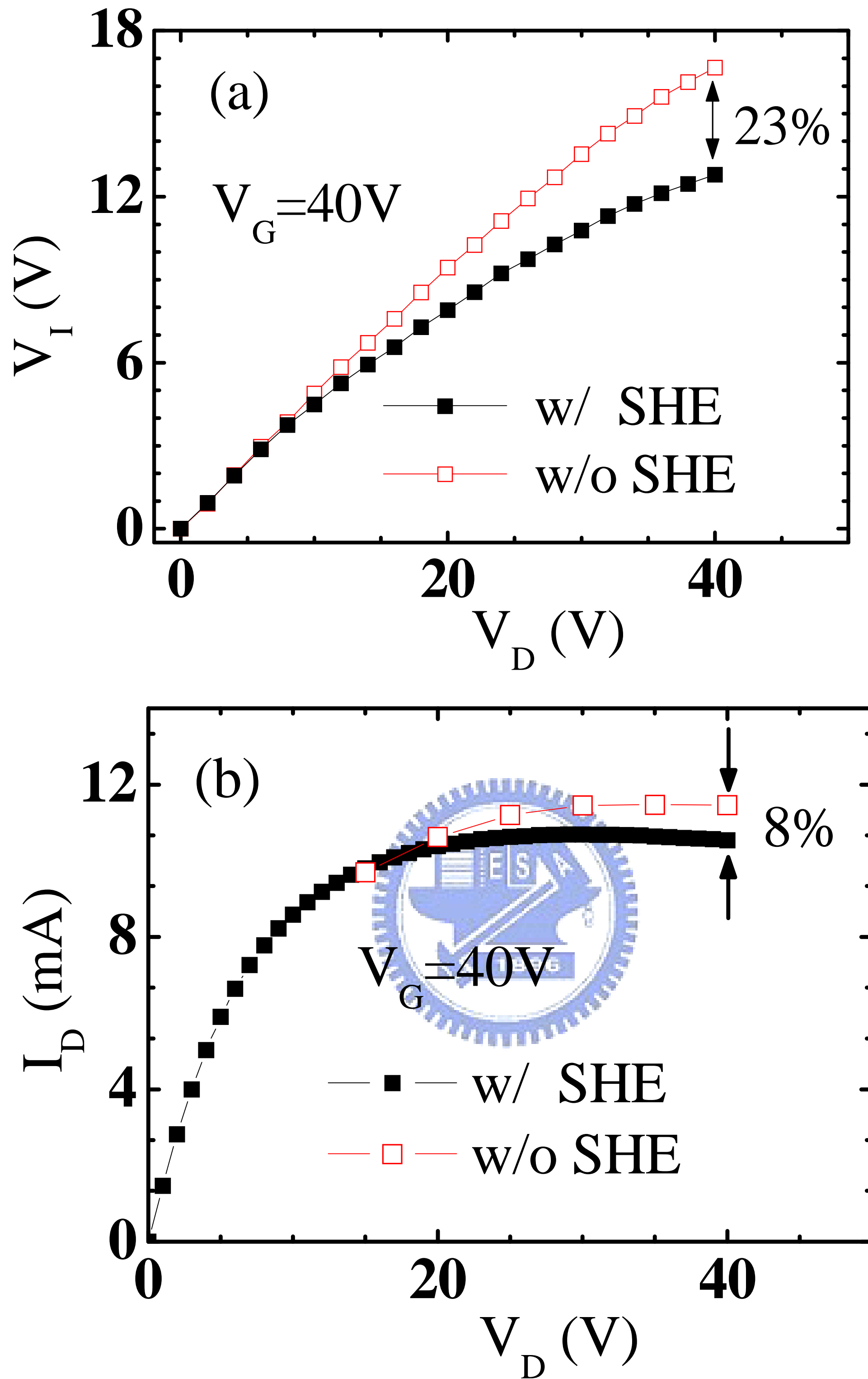


Fig. 2.5 (a) Internal voltage versus drain voltage with and without self-heating effect. The full squares (w/ SHE) are obtained by Agilent 4156 while the open squares (w/o SHE) are obtained from the measurement setup in Fig. 2.2. (b) Drain current versus drain voltage measured by Agilent 4156 (full squares) and by an external resistor method (open squares).

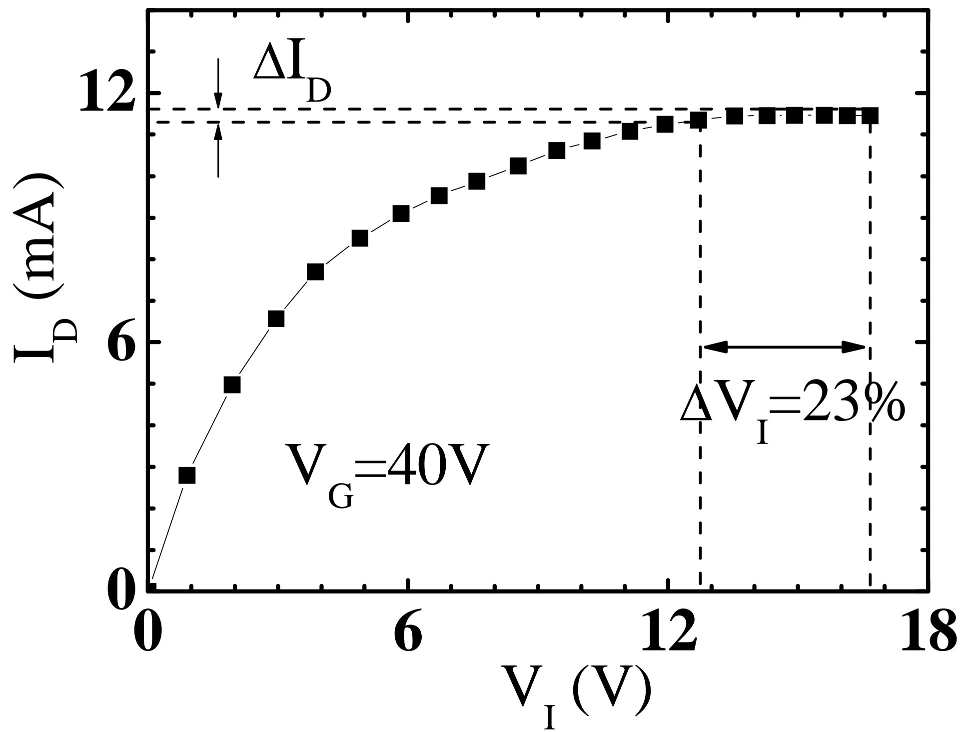
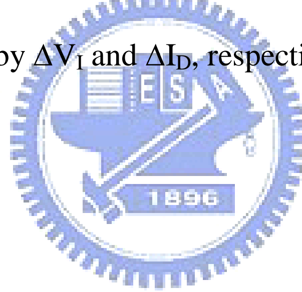


Fig. 2.6 Drain current versus internal voltage in a LDMOS. The reduction of V_I and I_D due to self-heating is denoted by ΔV_I and ΔI_D, respectively.



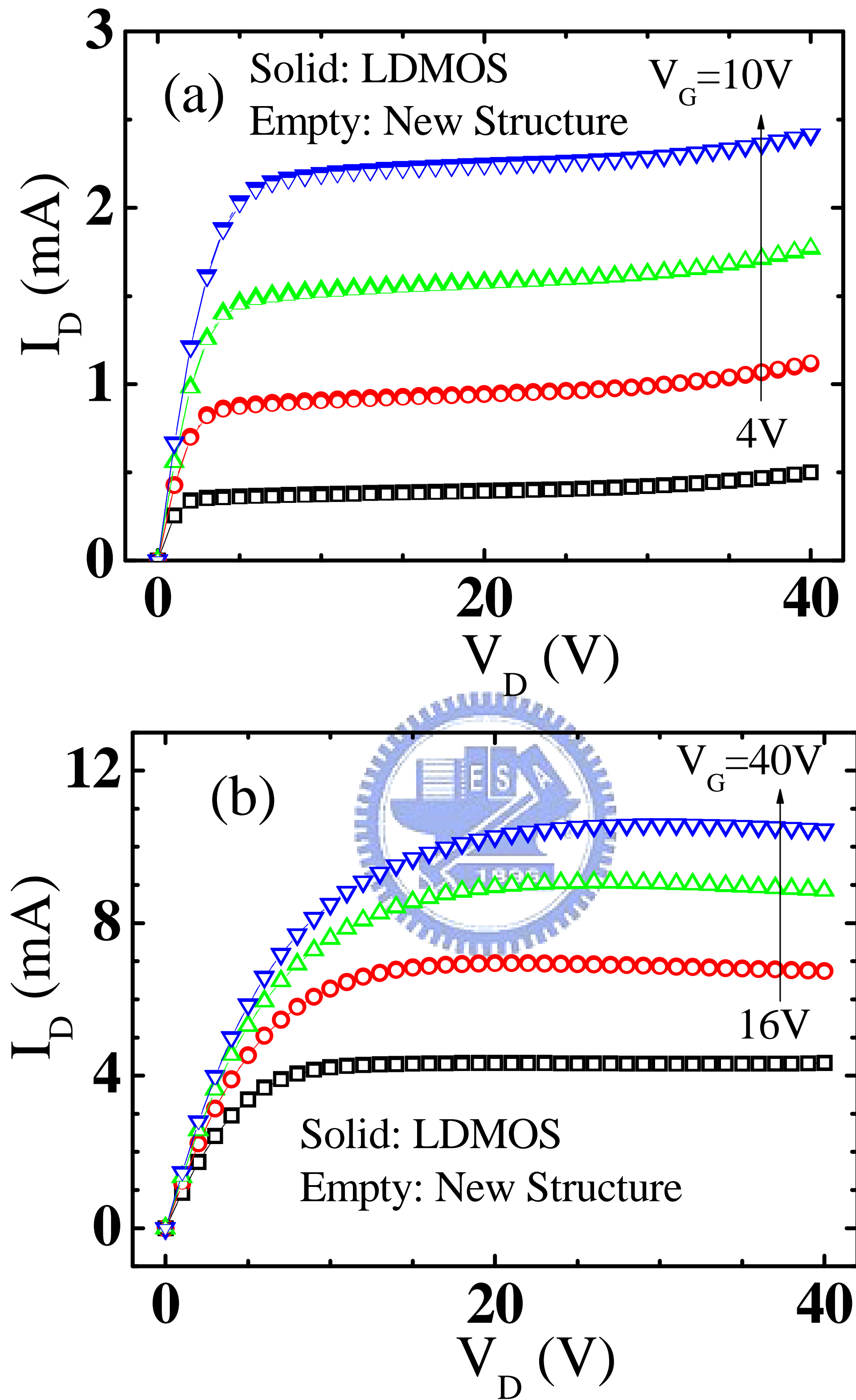


Fig. 2.7 I_D-V_D in LDMOS and in the proposed new structure. (a) At lower V_G (V_G<10V). (b) At higher V_G (V_G>10V).

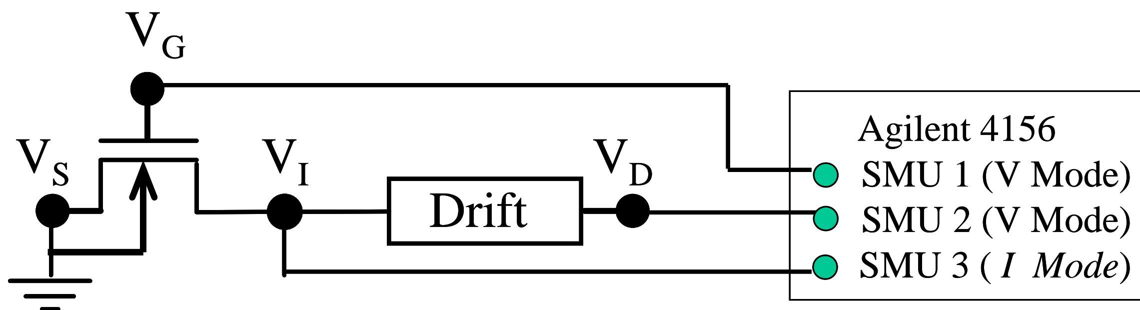
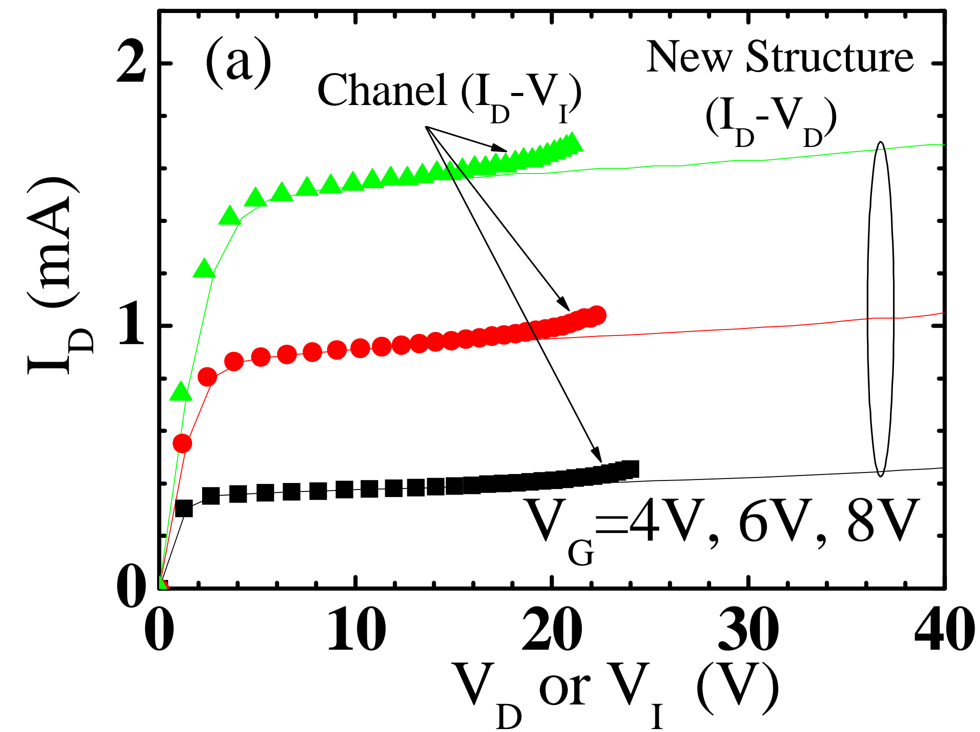


Fig. 2.8 I-V Measurement setup for device characterization. The V_I is measured by forcing a zero current in SMU 3. V_G/V_D are given by Agilent 4156.



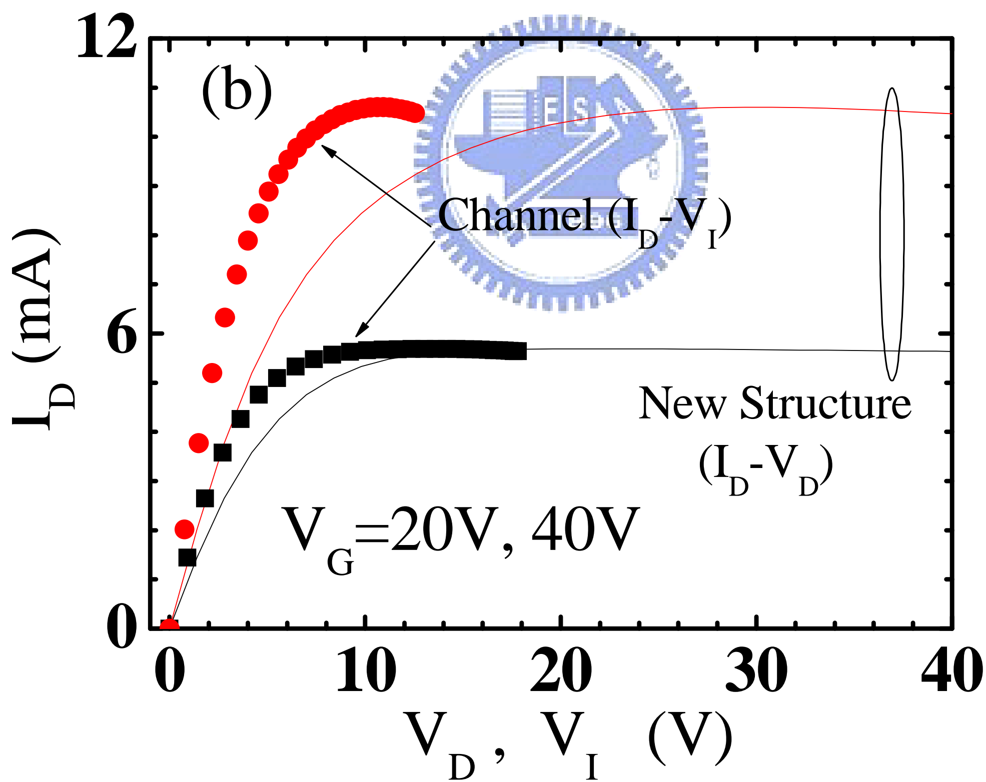


Fig 2.9 Comparison of metal-contact structure (I_D-V_D) characteristics and channel part of metal-contact structure (I_D-V_I) characteristics. (a) At lower V_G. (b) At higher V_G.

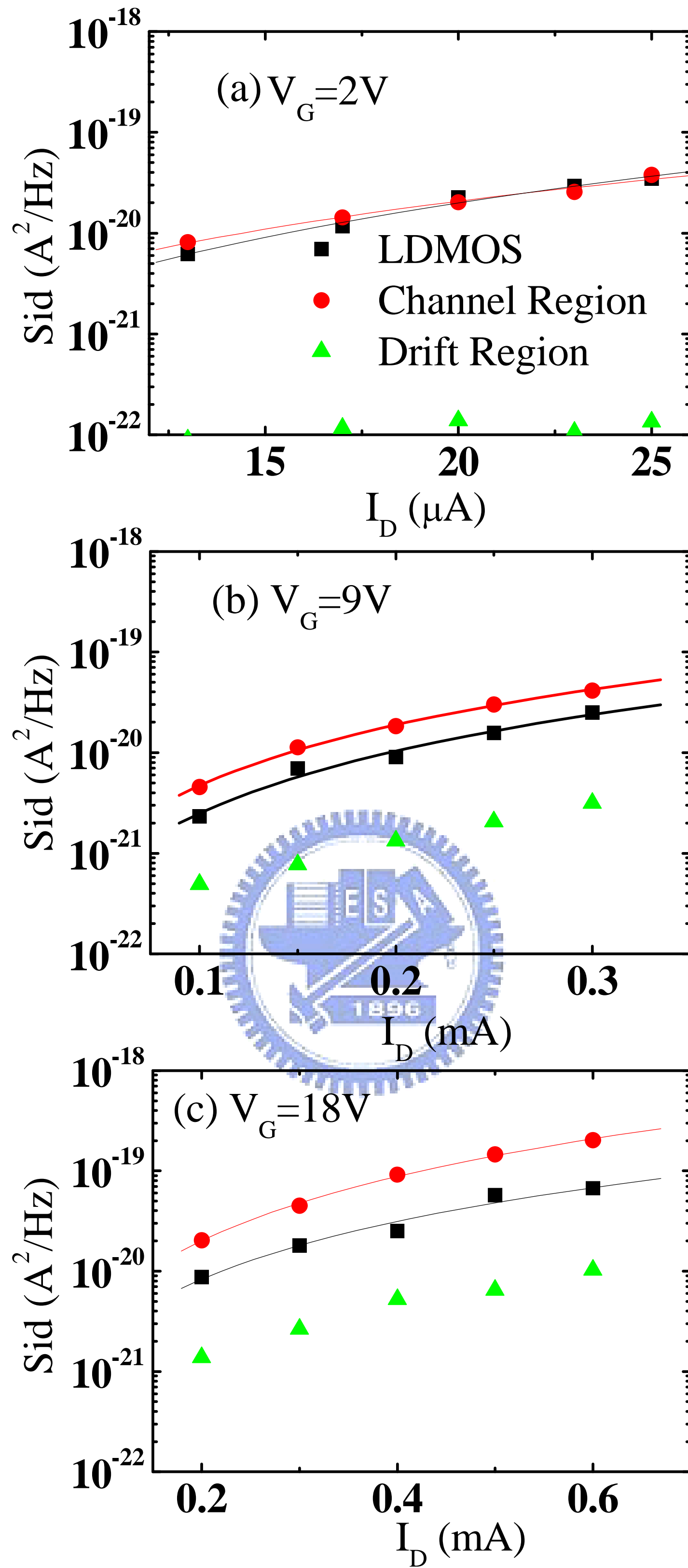


Fig. 2.10 Noise power spectrum density versus current flow in LDMOS, channel part of the LDMOS, and drift-region part of the LDMOS. (a) V_G=2V, (b) V_G=9V, and (c) V_G=18V.

Chapter 3

Physics and Characterization of Various Hot-Carrier Degradation Modes in LDMOS by Using a Three- Region Charge-Pumping Technique

3.1 Introduction

In recent years, multi-function power integrated chips are strongly demanded for the market of portable devices, automotive applications, and display drivers [3.1]. The integrated bipolar, CMOS, and DMOS (BCD) process has been developed to realize complex single power ICs [3.2] [3.3]. Among the candidates of high-voltage devices, lateral DMOS (LDMOS) transistors are attractive because they can be easily integrated with standard low-voltage CMOS process [3.1]-[3.4]. Nowadays, the LDMOS has been widely adopted in today's high-voltage and high-current output circuits [3.4], from a standard 12V automotive battery [3.5] to 100V plasma display panel drivers [3.6].

One of the major reliability issues in a LDMOS is hot carrier injection and trapping in the oxide [3.7]. Since an LDMOS possesses an intrinsic channel region and a lightly doped drift region, its hot carrier degradation mechanisms are different from a traditional MOSFET. The degradation mechanisms in LDMOS are closely dependent on device dimensions, process parameters, and operation voltages. Various hot carrier stress modes have been reported for an LDMOS in literature. Different

stress conditions result in oxide damage of different types (N_{it} and Q_{ox}) and locations (channel or drift region). Peter Moens reported that maximum I_B stress results in the worst hot carrier degradation for a gate oxide thickness from 7nm [3.7] to 17nm [3.8]. His studies showed that gate oxide damage occurs in the channel and in the accumulation regions. The device characteristics degradation is attributed to interface trap generation [3.7] [3.8]. N. Hefyene [3.9] and J.F. Chen [3.10] claimed that maximum I_G stress has more serious degradation and, again, interface trap generation is the cause of degradation. Since LDMOS degradation is closely dependent on trap type and location, the profiling of trap spatial distribution and trap behavior is important to the understanding of the impact of various hot carrier stress modes.

In this chapter, we demonstrate a novel three-region charge pumping (CP) technique to probe hot carrier stress induced oxide damage in a LDMOS [3.11]. Each region of the CP current corresponds to a different part of the device. By comparing the pre-stress and post-stress charge pumping currents in each region, we are able to identify the locations of oxide damage in the device and corresponding trap properties. To further recognize the damage locations, the dependence of low frequency noise on various hot carrier stress modes will be analyzed. Based on the study of device characterization in chapter 2, low-V_G and high-V_G flicker noise are performed to represent the channel and drift region damages respectively. A two-dimensional device simulation is simulated to identify an impact ionization generation (IIG) region in the device. The dependence of device degradation characteristic on trap position is

also studied.

3.2 Three-Region Charge Pumping Measurement

The n-LDMOS used in this work was processed in a 0.18μm CMOS technology with a gate oxide thickness of 100nm and a field oxide thickness of 500nm. The operation voltages are V_G=40V and V_D=40V. Fig. 3.1(a) shows the device cross-section. The device is divided into three regions. Region (I) is the channel region. Regions (II) and (III) are the accumulation region and the field oxide region. The length of each region is denoted by L_{chan}(=3μm), L_{acc}, and L_{fox}, respectively. The gate width is 20μm and the threshold voltage is 1.5V.

The device flat-band voltage (V_{FB}, solid line) and threshold voltage (V_T, dash line) distributions of the three regions are illustrated in Fig. 3.1(a). In the channel region, the flat-band voltage is lower than the threshold voltage. However, in the drift region, the flat-band voltage is higher than the threshold voltage because of the n-type substrate. A lower V_{FB2} than V_{FB1} is attributed to the different type of substrate doping. Moreover, a higher V_{FB2} than V_{FB3} is due to a thinner oxide thickness in the accumulation region than in the field-oxide region.

The gate voltage waveform in CP measurement is illustrated in Fig. 3.1(b) with a fixed V_{gh}=12V and a variable V_{gl}. For the 100nm thick gate oxide, we can switch V_{gl} from +3.6V to -40V without a significant gate oxide tunneling current. In this V_{gl} range, all the three regions of the device can be probed. The measurement frequency in this work is 200 kHz. Typical CP measurement result is shown in Fig. 3.2. The

charge pumping current (I_{cp}) exhibits three stages, corresponding to the three regions of a n-LDMOS respectively. It should be noticed that each stage has their corresponding threshold and flat-band voltages. By measuring the change of I_{cp} and V_{FB} after stress in each stage, we are able to separate N_{it} and Q_{ox} in each region of the device [3.11], for example, ΔN_{it}(channel)=ΔI_{cp}(stage 1)/$qfWL_{chan}$, ΔQ_{ox}(acc.)=ΔV_{FB} (stage 2)·C/q and so on.

3.3 Flicker Noise Measurement

Flicker noise was observed in vacuum tubes by Johnson in 1920 and interpreted by Walter Schottky in 1926. Two major models to explain the mechanisms of flicker noise in CMOS device are McWhoter's [3.12] charge trapping model and Hooge's empirical relation [3.13]. According to the carrier number fluctuation theory [3.12], flicker noise is explained by the fluctuation of channel free carrier where the random capture and emission by the oxide traps near Si-SiO_2 interface. In Hooge's hypothesis, the flicker noise is regarded as a consequence of bulk mobility fluctuation, which is caused by phonon population through phonon scattering. However, either theory couldn't verify the noise generation mechanism independently and completely, especially in high-voltage LDMOS.

The purpose of the flicker noise measurement in LDMOS is to find out the oxide damage location for various kinds of hot carrier stress modes. Fig. 3.3 compared a normalized flicker noise in a LDMOS and in a channel-part of LDMOS. The flicker noise in channel region is measured from a metal contact LDMOS, as discussed in chapter 2. In Fig. 3.3, the normalized flicker noise at low-V_G in the LDMOS is almost the same as in the channel, suggesting that the flicker noise at low-V_G is determined

by the channel region. At a higher V_G, however, the normalized flicker noise in the LDMOS becomes lower than in the channel region because the drift region takes effect to the LDMOS. These features are similar to the device I-V characteristics in Fig. 2.3 in chapter 2 and can be used to investigate the locations of oxide damage after hot carrier stress.

3.4 Various DC Hot Carrier Stress Modes

To study the dependence of damage types and locations on hot carrier stress voltages, three hot carrier stress modes, i.e., 1) mode A (maximum I_B); 2) mode B (V_G~1/2V_D); and 3) mode C (maximum I_G), are investigated. The I_G-V_G of a n-LDMOS is shown in Fig. 3.4. The maximum I_B (mode A) stress is applied at V_G/V_D=8V/50V and the maximum I_G (mode C) stress is at V_G/V_D=50V/50V. The bias conditions of the three stress modes are also indicated in Fig. 3.4. For each stress mode, the three-region CP method is performed to investigate trap type (N_{it} or Q_{ox}) and growth characteristics. The low-V_G and high-V_G flicker noise are measured to identify the damage region. Subthreshold slope and linear drain current (I_{dlin}, @V_G=40V, V_D=0.1V) are used to monitor device degradation.

3.4.1 Maximum I_B Stress Mode

Fig. 3.5(a) shows the I_{cp} in a fresh device and after 1400 sec. max. I_B stress. The post-stress I_{cp} in the first stage is nearly the same as the pre-stress one, indicating that region (I) oxide is not damaged by the stress. The post-stress I_{cp} in stage 2, however, exhibits an upward shift while the flat-band voltage keeps the same (no rightward shift in the I_{cp}). This feature suggests N_{it} generation in region (II) but no Q_{ox} creation. Numerical device simulation also shows the maximum IIG rate in region (II) (Fig. 3.5(b)). Although interface trap generation is observed from the I_{cp}, the subthreshold

swing of the device is not degraded because the generated N_{it} is distributed in region (II) rather than in the channel region.

Since maximum I_B stress results only N_{it} in region (II), the channel region is not damaged and thus the normalized flicker noise at low-V_G (Fig. 3.6(a)) exhibits no significant change after stress. The damage in region (II) can be further identified by the normalized flicker noise at high-V_G (Fig. 3.6(b)). The generated N_{it} in region (II) results in a large increase of flicker noise at high-V_G but no significant I_{dlin} degradation is observed.

3.4.2 V_G～(1/2) V_D Stress Mode

The I_{cp} results before and after mode B stress (@V_G/V_D =30V/50V) are shown in Fig. 3.7(a). N_{it} generation in stress mode B is relatively small and can be realized due to a smaller substrate current (and a smaller IIG region in Fig. 3.7(b)), as compared to stress mode A. Unlike stress mode A, a distinct flat-band voltage shift in region (II) is noticed, which is manifested by a rightward shift of the I_{cp} in stage 2. An arrow is drawn in Fig. 3.7(a) to indicate the flat-band voltage shift (ΔV_{FB2}). The rightward shift of the slope is caused by negative Q_{ox} creation in region (II). Fig. 3.8 shows the evolution of the I_{cp} with stress time. As stress time increases, the flat-band voltage of the region (II) continuously shifts to the right. The Q_{ox2} generation rate (Fig. 3.9) can be extracted from the ΔV_{FB2} versus stress time by using the equation in section 3.2. Because of negative Q_{ox} creation, the resistance beneath the bird’s beak increases. At a large V_g, region (I) resistance is relatively small and the resistance in the bird’s beak region occupies a larger part of the total resistance. Thus, I_{dlin} degradation is observable at a higher measurement V_G =40V (Fig. 3.10). Consequently, the normalized flicker noise at low-V_G (Fig. 3.11(a)) exhibits no change and the high-V_G flicker noise (Fig. 3.11(b)) increases after stress. Numerical simulation for the

dependence of I_{dlin} degradation on trap location will be given later.

3.4.3 Maximum I_G Stress Mode

Fig. 3.12(a) shows the I_{cp} result before and after max. I_G stress for 1000 seconds. Two different stress induced oxide degradation mechanisms are noticed; One is N_{it} generation in region (I) and the other is negative Q_{ox} creation in region (II). These two trap creation processes are reflected by an upward shift of the first stage I_{cp} denoted by ΔI_{cp1} and by a rightward shift of the second stage I_{cp} (ΔV_{FB2} in Fig. 9(a)). In contrast to stress mode A, two-dimensional device simulation reveals that the IIG region in max. I_G stress splits into two parts (Fig. 3.12(b)); One is in the channel (region (I)) and the other is underneath the bird's beak. These two degradation mechanisms are also observed in the flicker noise measurement (Fig. 3.13). The N_{it} generation in the channel region results an increase of the normalized flicker noise at low-V_G (fig. 3.13(a)) and the oxide damage in drift region worsens the normalized flicker noise at high-V_G (Fig.3.13(b)). The N_{it} generation in region (I) results in a significant subthreshold swing degradation (Fig. 3.14) in stress mode C. In addition, Q_{ox2} creation accounts for a serious I_{dlin} degradation (Fig. 3.15) in mode C. Fig. 3.15 shows that the I_{dlin} degradation is more apparent at a larger V_G. To explain the V_G dependence, a two-dimensional device simulation is performed. We calculate the I_{dlin} versus V_G by placing the same amount of fixed oxide charge ($Q_{ox}/q=10^{19}/cm^3$) in the channel (Fig. 3.16(a)) and in the bird's beak region (Fig. 3.16(b)). Fig. 3.16(a) shows a larger I_{dlin} degradation at a low V_G while Fig. 3.16(b) shows a larger I_{dlin}

degradation at a high V_G. The trend in Fig. 3.16(b) agrees with our measured result (Fig. 3.15) and thus we can conclude that the created Q_{ox} is in region (II).

The N_{it1} and Q_{ox2} growth rate in stress mode C are shown in Fig. 3.17 and Fig. 3.18, respectively. The growth rate obeys a power-law time dependence and the power factor is around 0.25, which is in agreement with [3.14]. Comparing to mode A and B, the larger Q_{ox2} growth rate in mode C is attributed to a larger stress gate current (or a higher stress gate voltage). The I_{dlin} degradation rate is shown in Fig. 3.19. Stress mode C has the worst I_{dlin} degradation. Due to oxide charge creation in region (II), region (II) resistance increases and the current flow in region (II) is pushed deeper. Consequently, the electron mobility exhibits a saturated effect and thus I_{dlin} degradation has a tendency to saturate in Fig. 3.19. This mobility saturation model is also described in [3.15] [3.16] for MOSFET and [3.8] for LDMOS structure. The LDMOS degradation behavior and trap properties in the three stress modes are summarized in Table 3.1. A comparison of impact ionization generation rate distribution in the three various stress modes is shown in Fig. 3.20.

3.5 Summary

A novel three-region CP technique has been developed to characterize hot carrier stress induced oxide degradation in each region of a n-LDMOS. The trap location and property in various stress modes are identified and their impact on device characteristics has been analyzed. A correlation between device degradation and charge pumping and device simulation results has been established. The dependence of low frequency noise on various hot carrier stress modes has been characterized.

Our study reveals that the device subthreshold swing degradation is mainly affected by interface traps in the channel region while the linear drain current degradation is dictated by oxide trapped charge in the drift region. A correlation between the trap locations and the flicker noise at different applied gate voltage is noticed in the study. An increase of low-V_G flicker noise accounts for the damage in the channel region and the damage in the drift region causes an increase of high-V_G flicker noise. Our study also shows that maximum I_B stress only results in an increase of flicker noise at high-V_G and no significant I_{dlin} degradation is observed. In addition, maximum I_G stress results in the worst I_{dlin} degradation in a LDMOS, which is attributed to both N_{it} generation in the channel region and Q_{ox} generation in the bird's beak region.

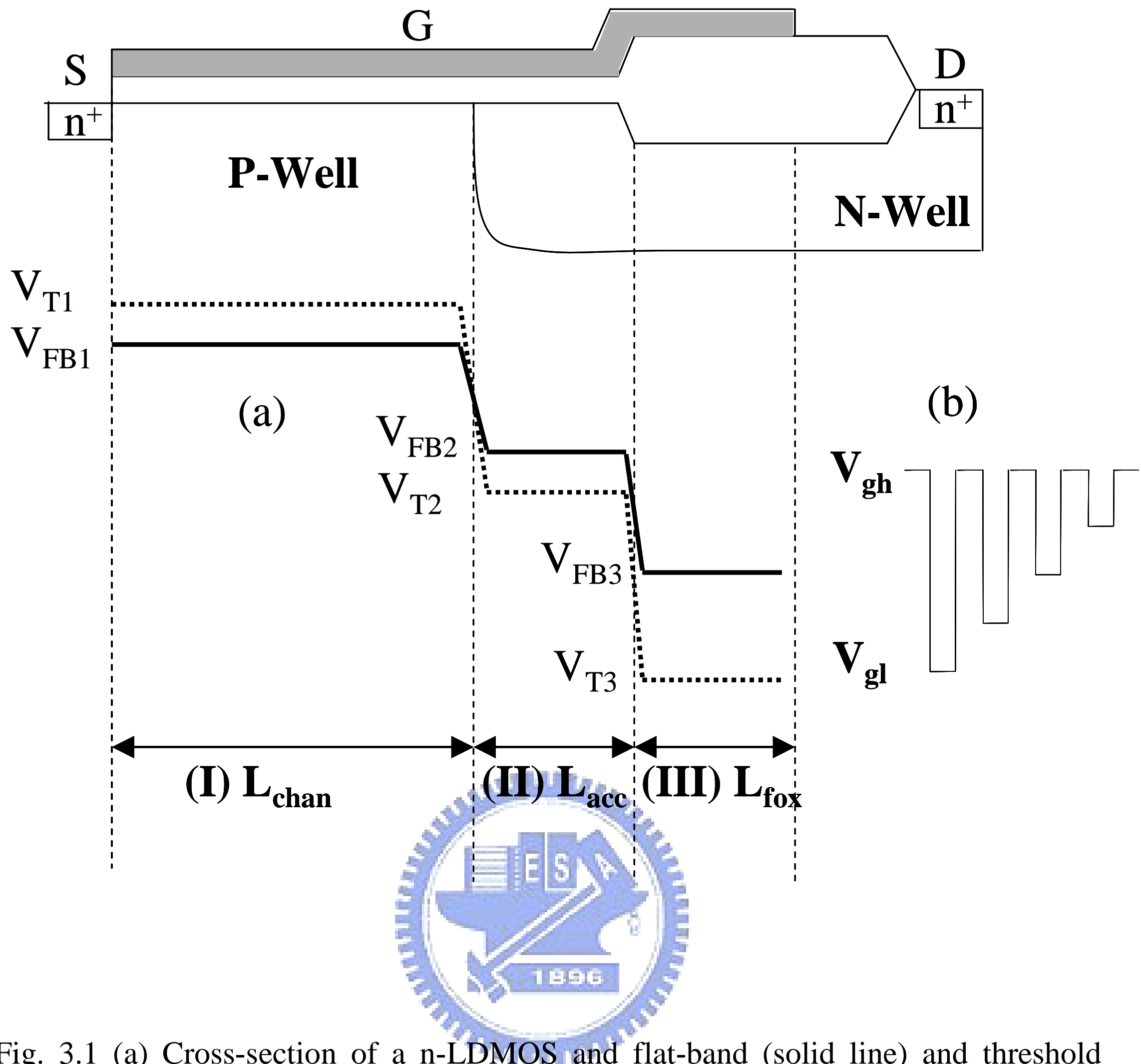


Fig. 3.1 (a) Cross-section of a n-LDMOS and flat-band (solid line) and threshold (dash line) voltage distributions. The device is divided into three parts, L_{chan} (channel region), L_{acc} (accumulation region), and L_{fox} (field oxide region). (b) Illustration of a charge pumping measurement waveform. The V_{gh}=12V is fixed and V_{gl} varies from +3.6V to -40V.

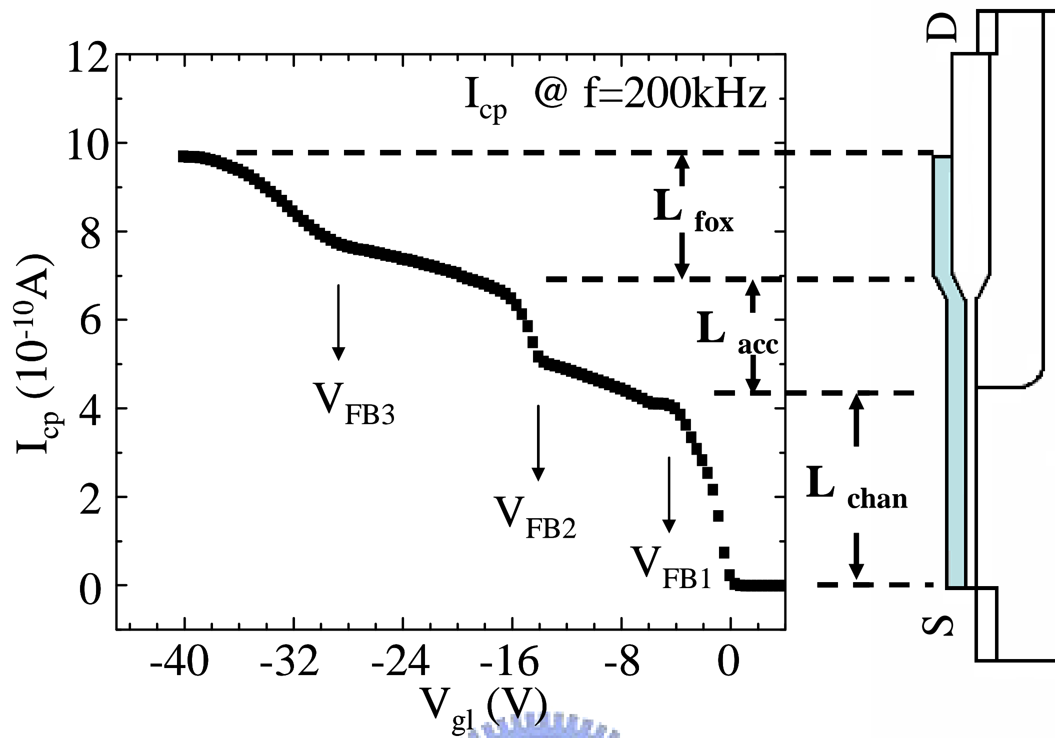


Fig. 3.2 Typical CP current in a n-LDMOS. The three stages of the CP current correspond to the three regions of the device. The flat-band voltage of each region is indicated in the figure. The frequency in charge pumping measurement is fixed at 200 kHz.

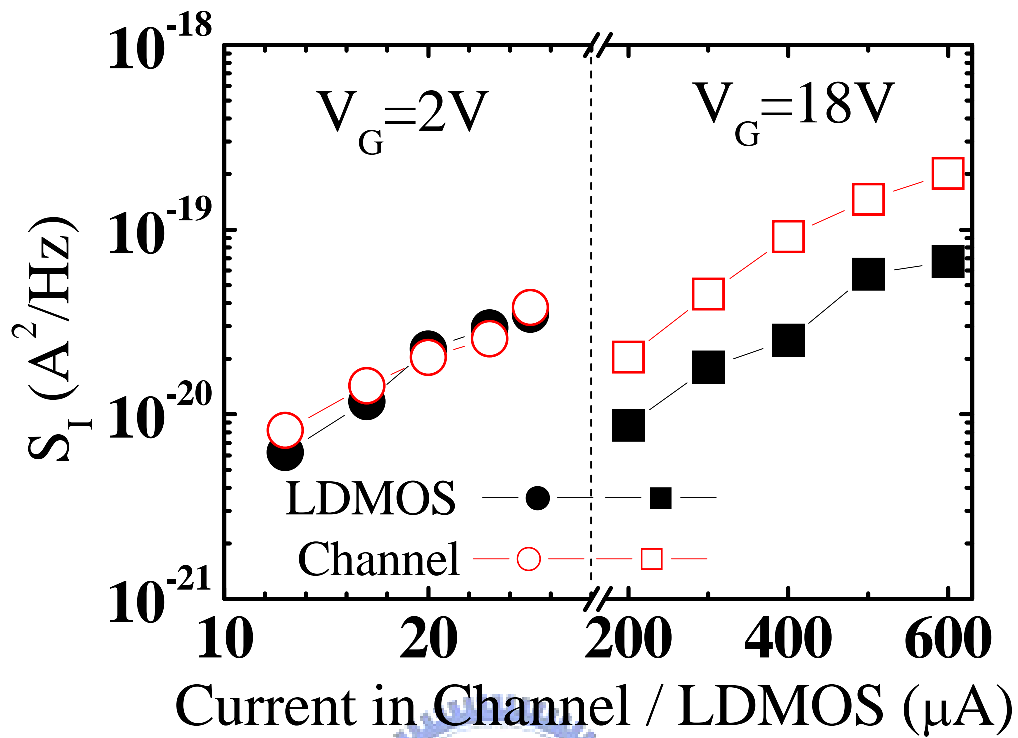
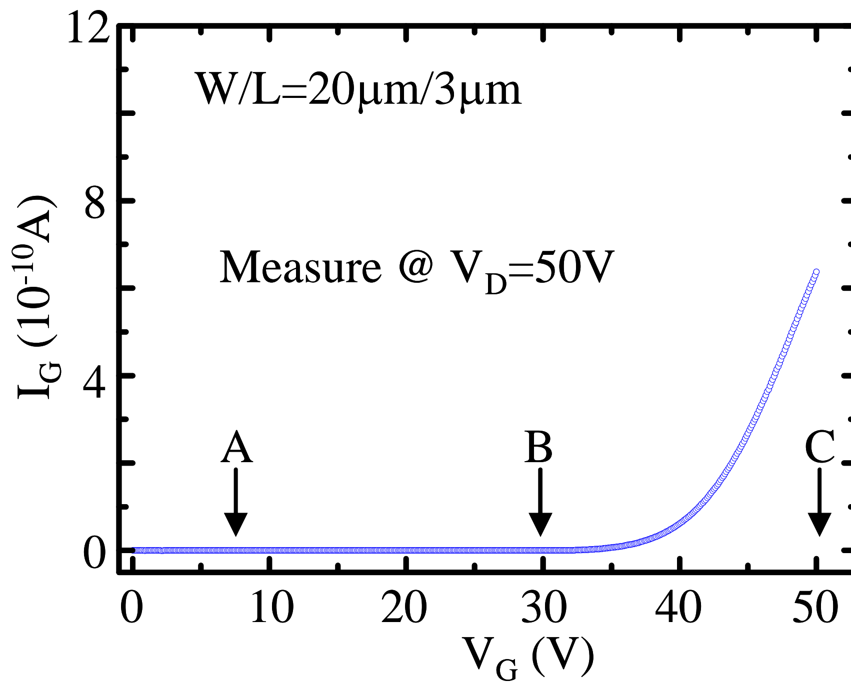


Fig. 3.3 Power spectrum density (S_I) at a lower VG (VG=2V) and at a higher VG (VG=18V). Solid and empty symbols represent the measurement results in LDMOS and in channel region respectively.



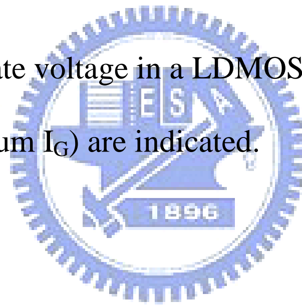
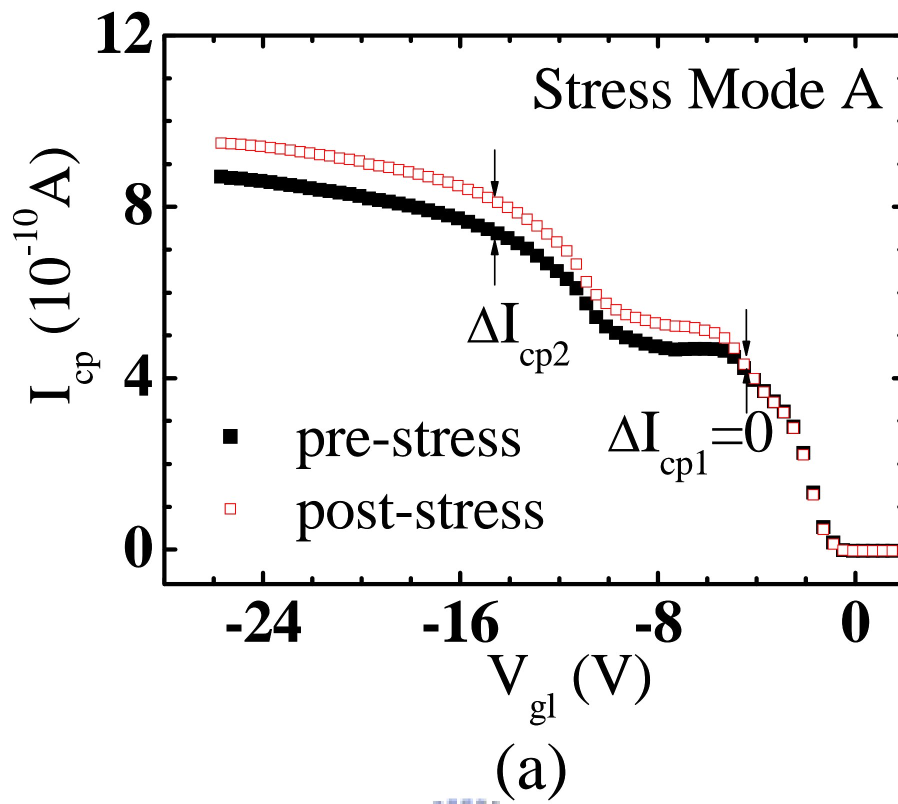
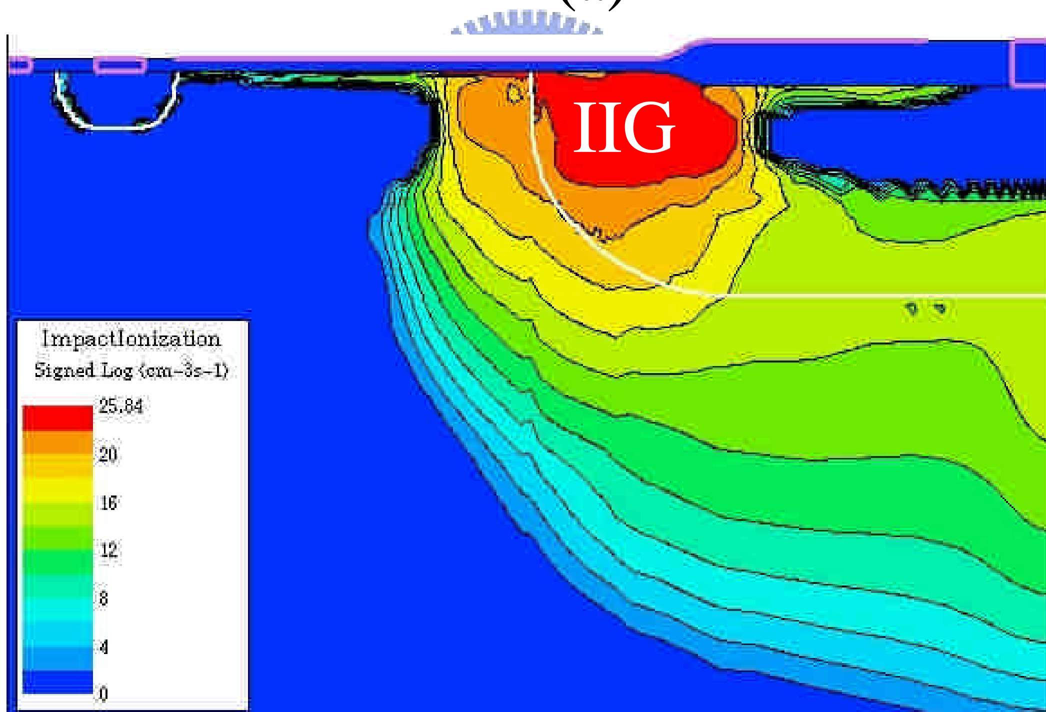


Fig. 3.4 Gate current versus gate voltage in a LDMOS. Stress modes A (maximum I_B), B (V_G~1/2V_D), and C (maximum I_G) are indicated.

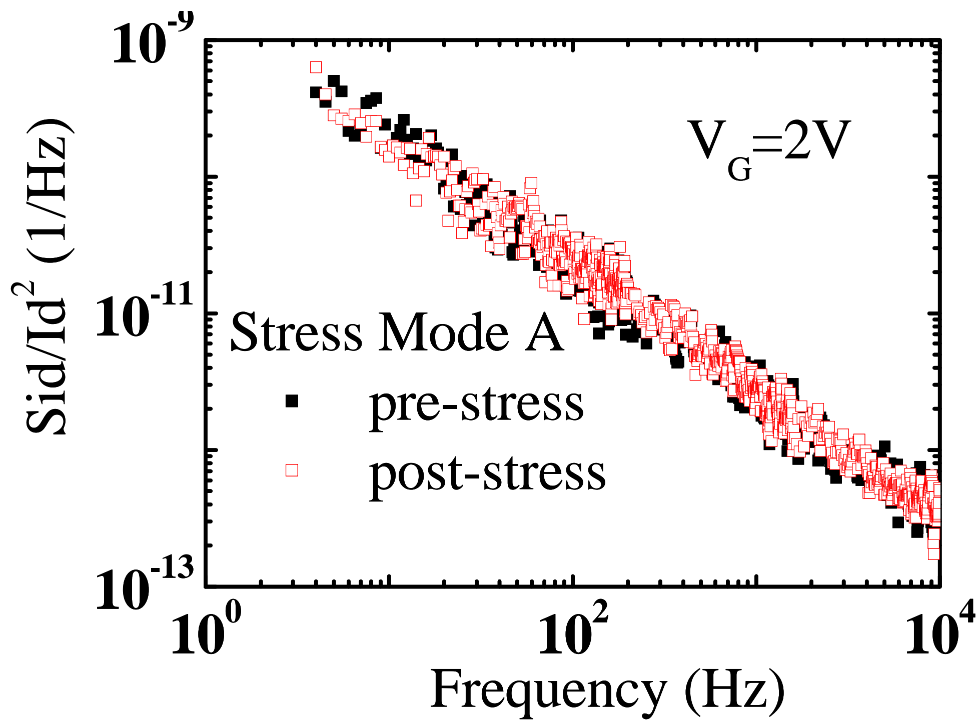


(a)

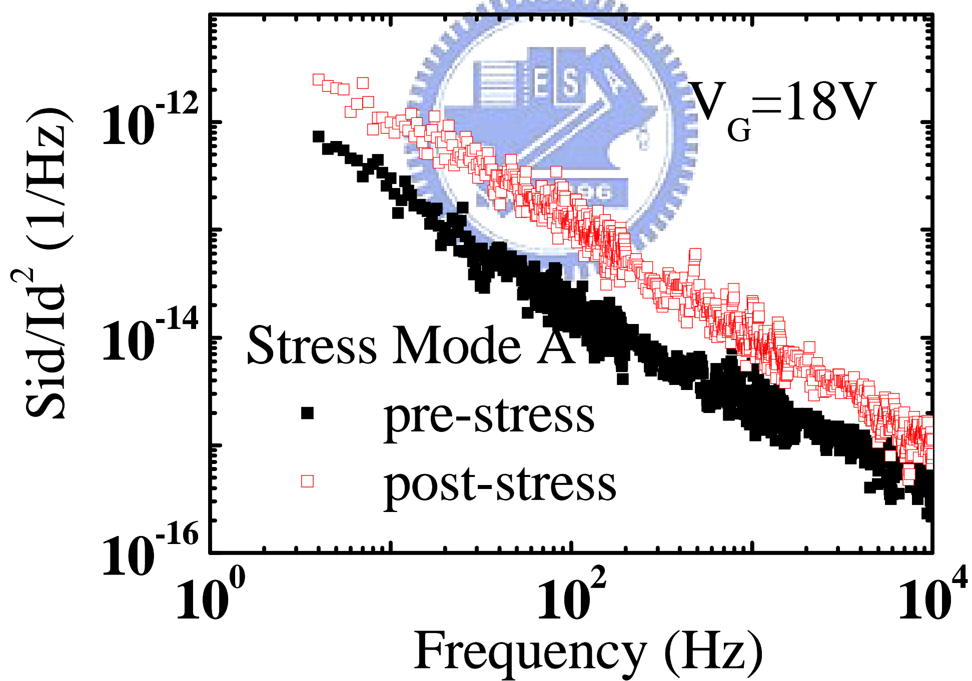


(b)

Fig. 3.5 (a) Charge pumping current versus V_{gl} before and after 1400 sec. mode A stress. (b) Two-dimensional device simulation of impact ionization generation (IIG) distribution in stress mode A.

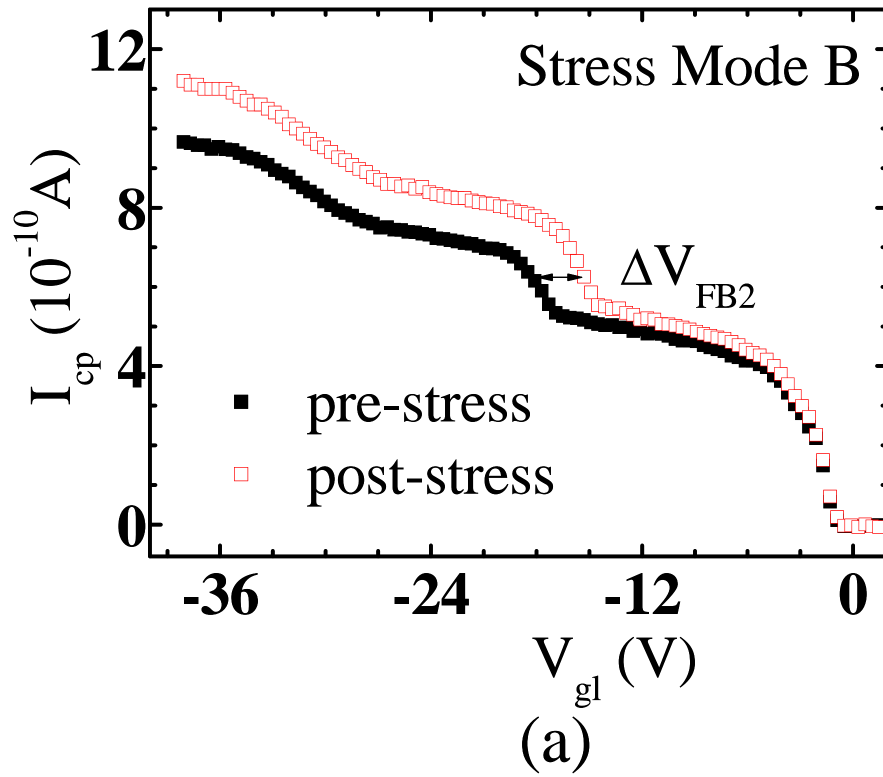


(a)

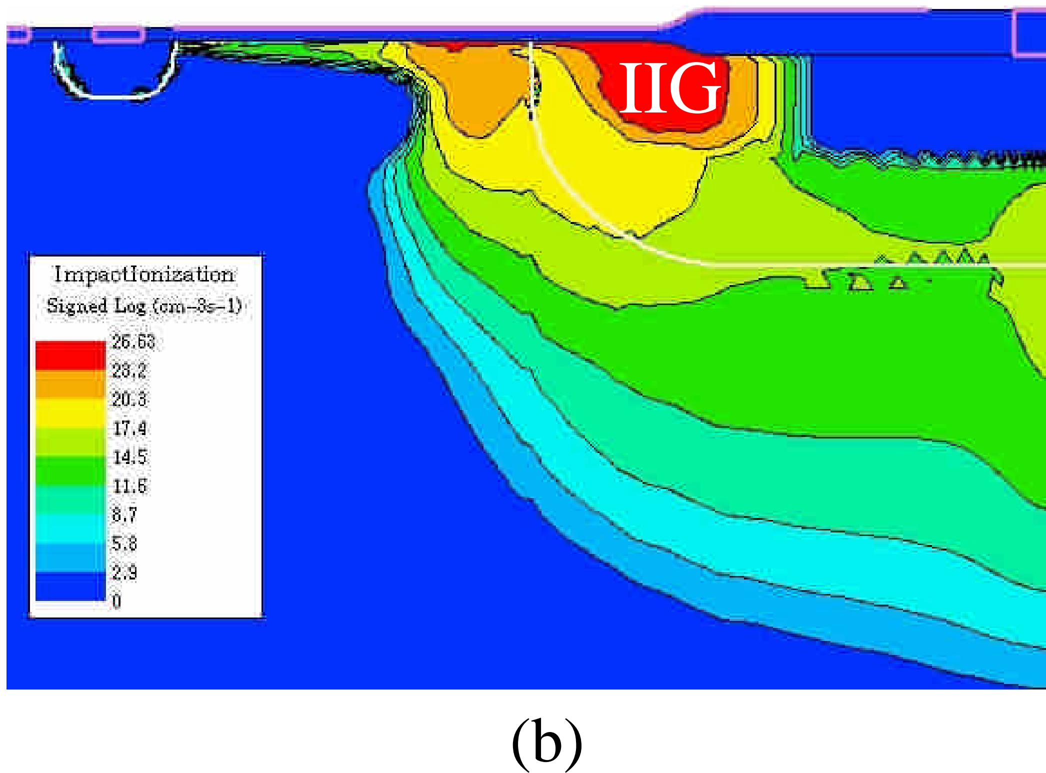


(b)

Fig. 3.6 Comparison of normalized flicker noise before and after mode A stress. (a) At a lower V_G (V_G=2V) and (b) at a higher V_G (V_G=18V).



(a)



(b)

Fig. 3.7 (a) Charge pumping current versus V_{gl} before and after 1400 sec. mode B stress. The shift of the flat-band voltage in stage 2 implies the generation of negative oxide charge in the accumulation region. (b) Two-dimensional device simulation of impact ionization generation (IIG) in stress mode B.

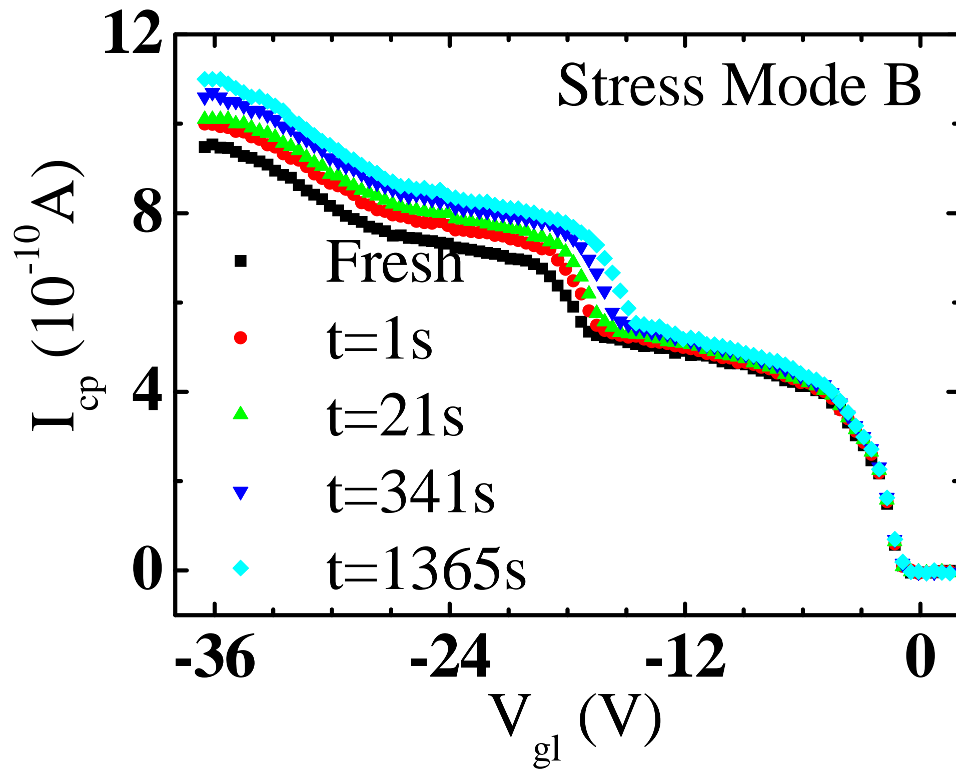


Fig. 3.8 The charge pumping results in stress mode B for different stress times.

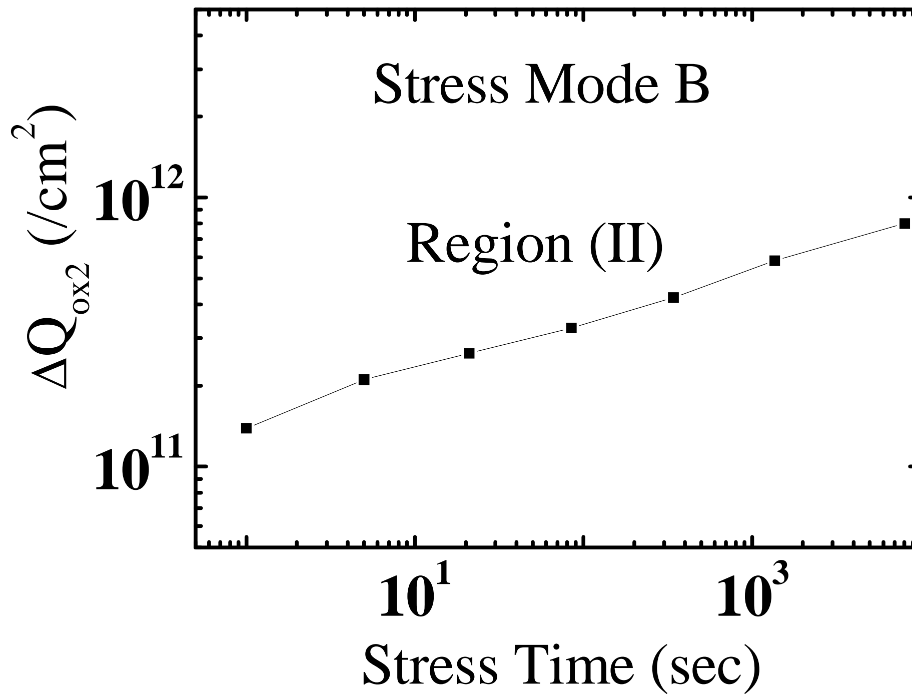


Fig. 3.9 Region (II) oxide-trapped charge growth rate in stress mode B.

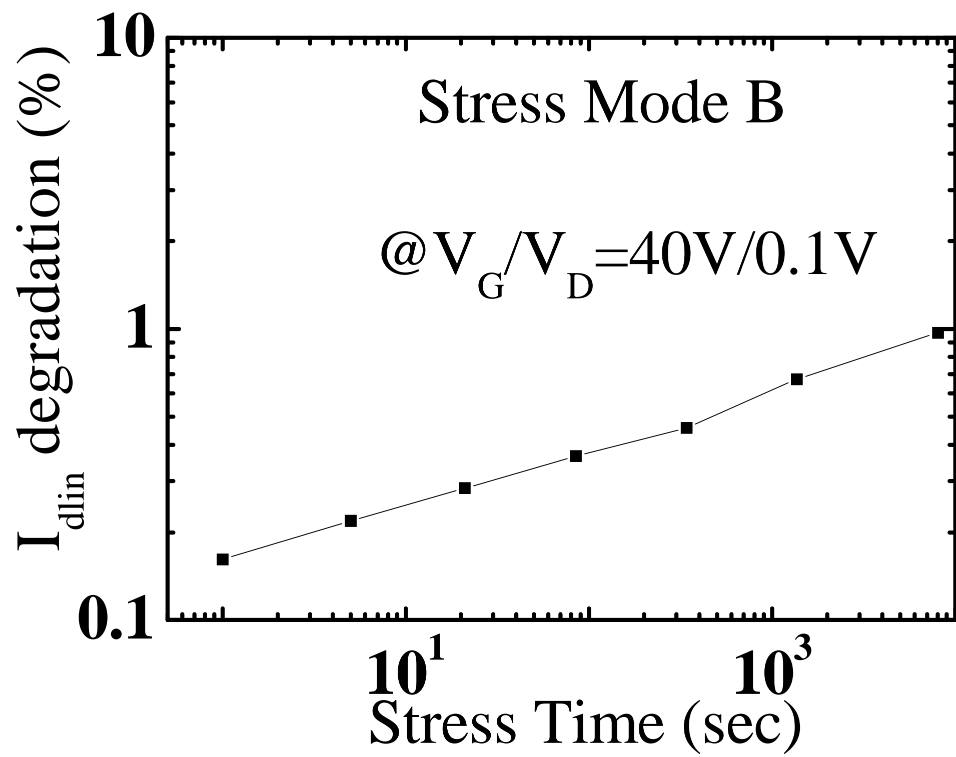
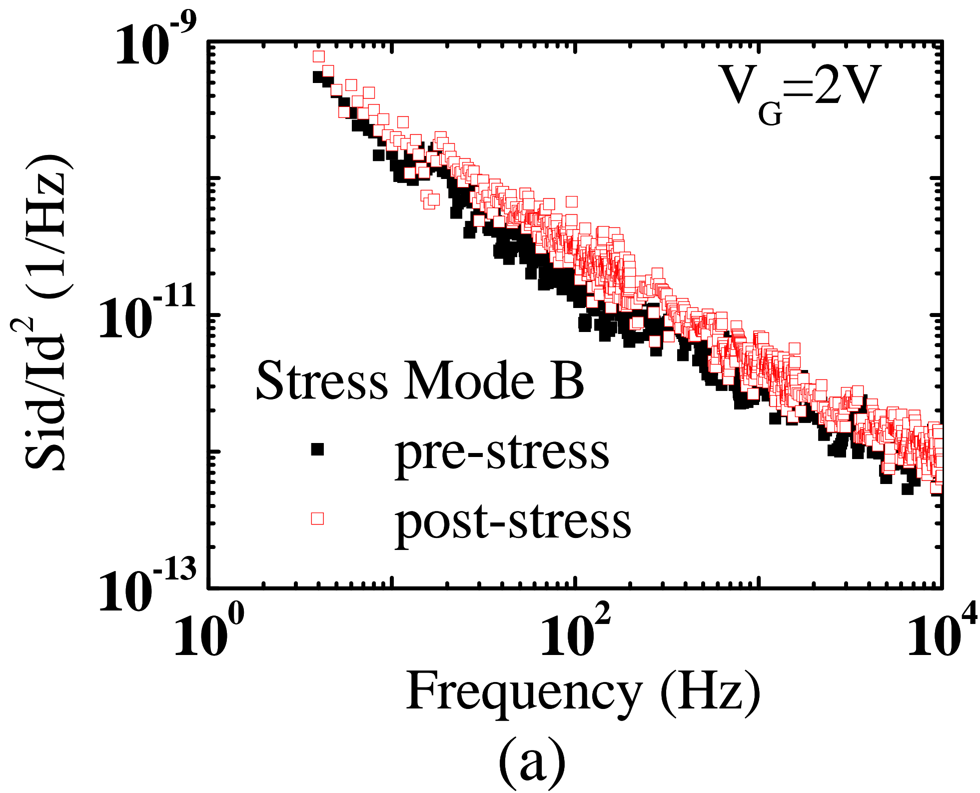
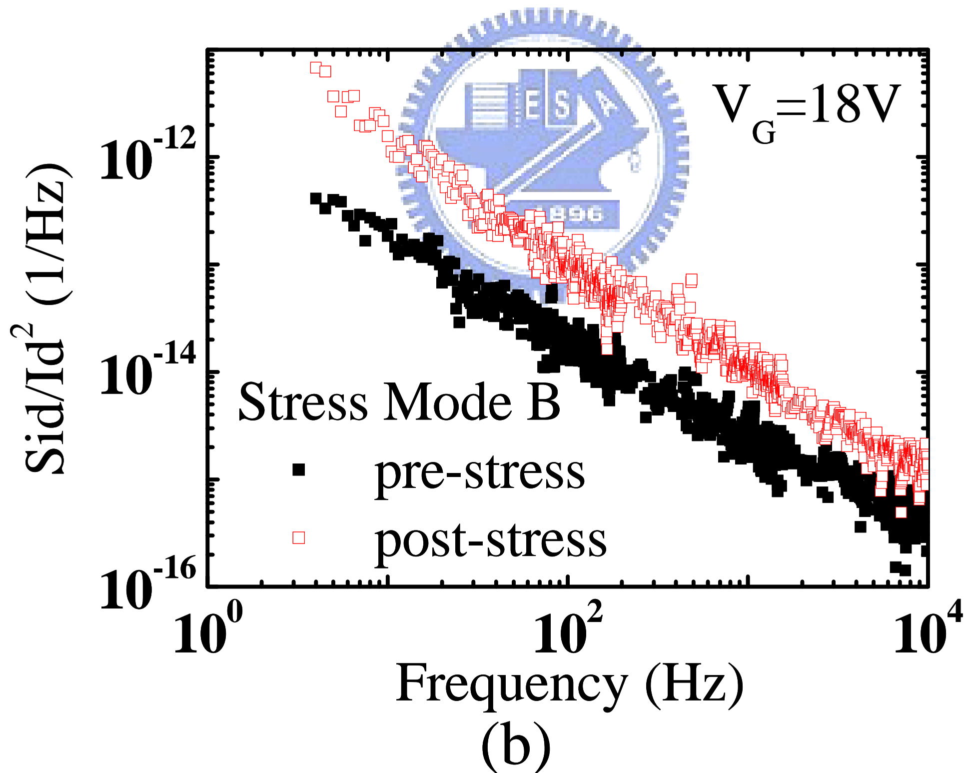


Fig. 3.10 Linear drain current degradation (I_{dlin}) rate measured at V_G/V_D=40V/0.1V in stress mode B.

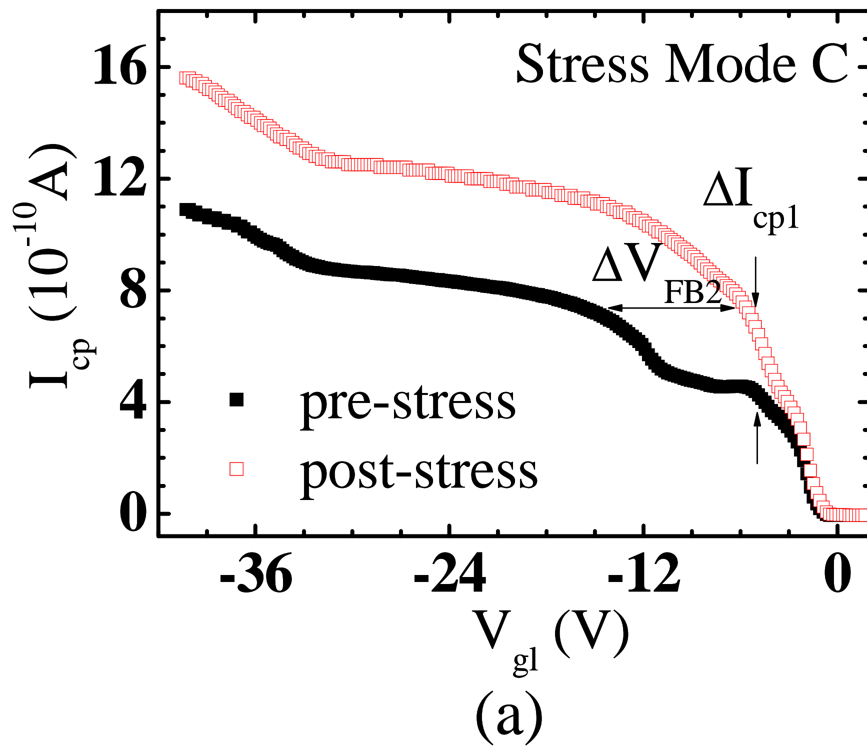


(a)

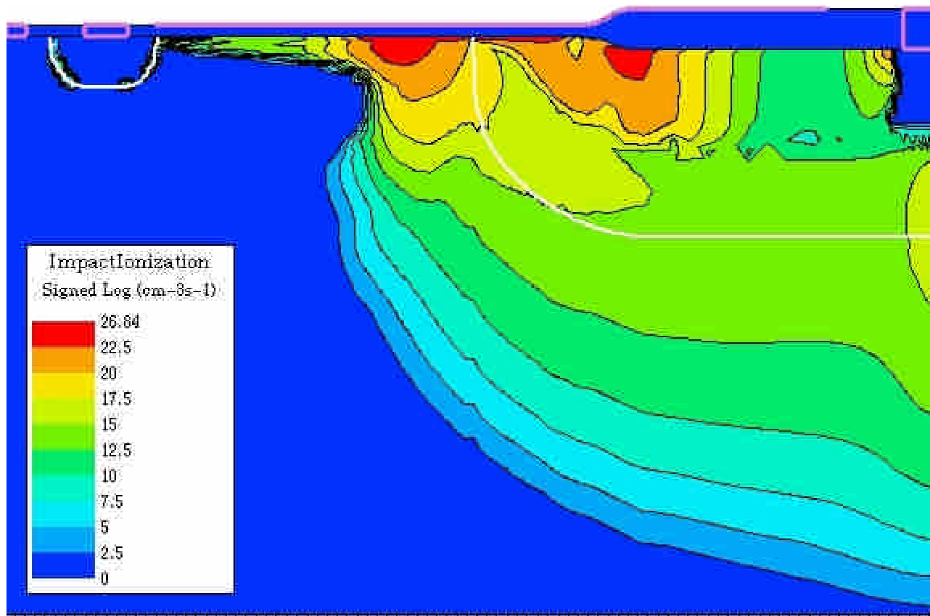


(b)

Fig. 3.11 Comparison of normalized flicker noise before and after mode B stress. (a) At a lower V_G (V_G=2V) and (b) at a higher V_G (V_G=18V). The increase of (Sid/Id^2) at a higher V_G is attributed to negative oxide charge creation in the accumulation region.

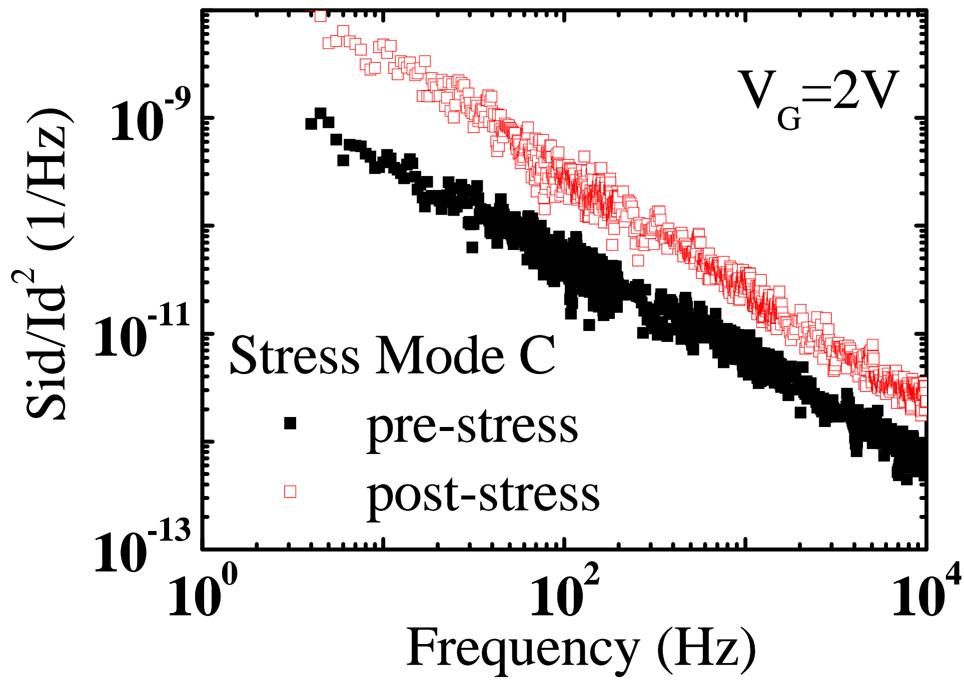


(a)

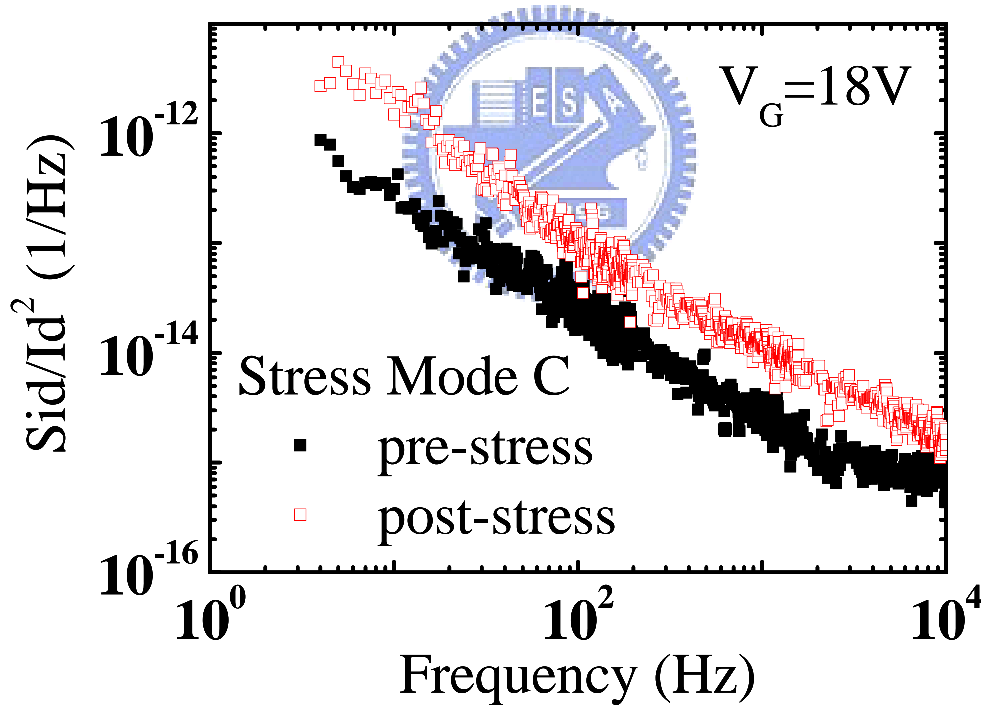


(b)

Fig. 3.12 (a) Charge pumping current before and after 1000 sec. mode C stress. Upward shift in stage 1 I_{cp} indicates interface trap generation in the channel and rightward shift in stage 2 I_{cp} implies oxide charge creation in the accumulation region. (b) Two-dimensional device simulation of impact ionization generation (IIG) distribution in stress mode C. Two IIG regions are found; One is in the channel region and the other is in the accumulation region.



(a)



(b)

Fig. 3.13 Comparison of normalized flicker noise before and after mode C stress. (a) At a lower V_G (V_G=2V) and (b) at a higher V_G (V_G=18V). The increase of (Sid/Id^2) at a lower V_G and at a higher V_G are attributed to the creation of N_{it} in the channel and Q_{ox} in the drift region, respectively.

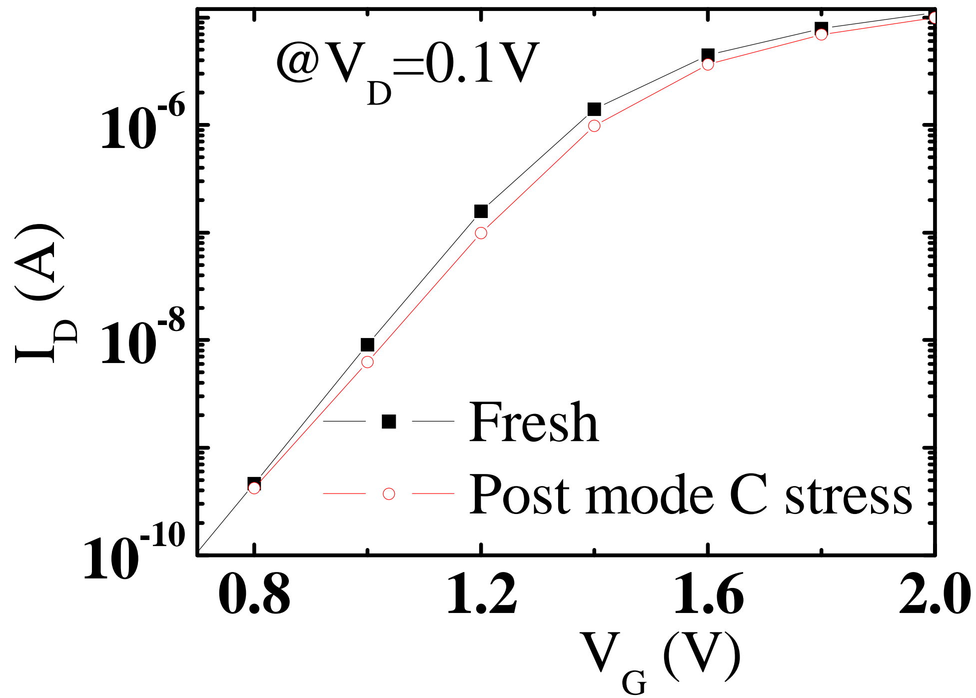
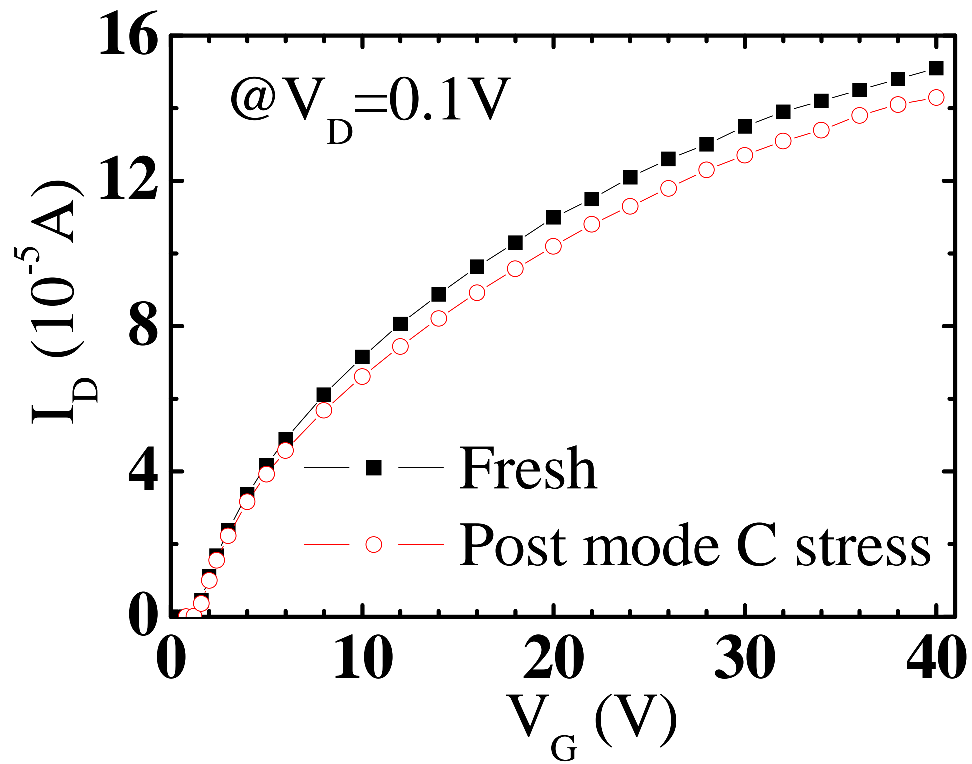


Fig. 3.14 Subthreshold characteristics before and after mode C stress. The swing degradation is attributed to interface trap generation in the channel region.



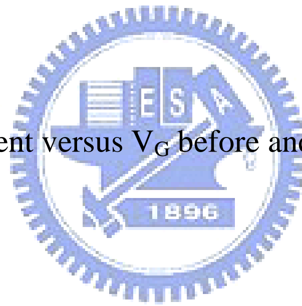
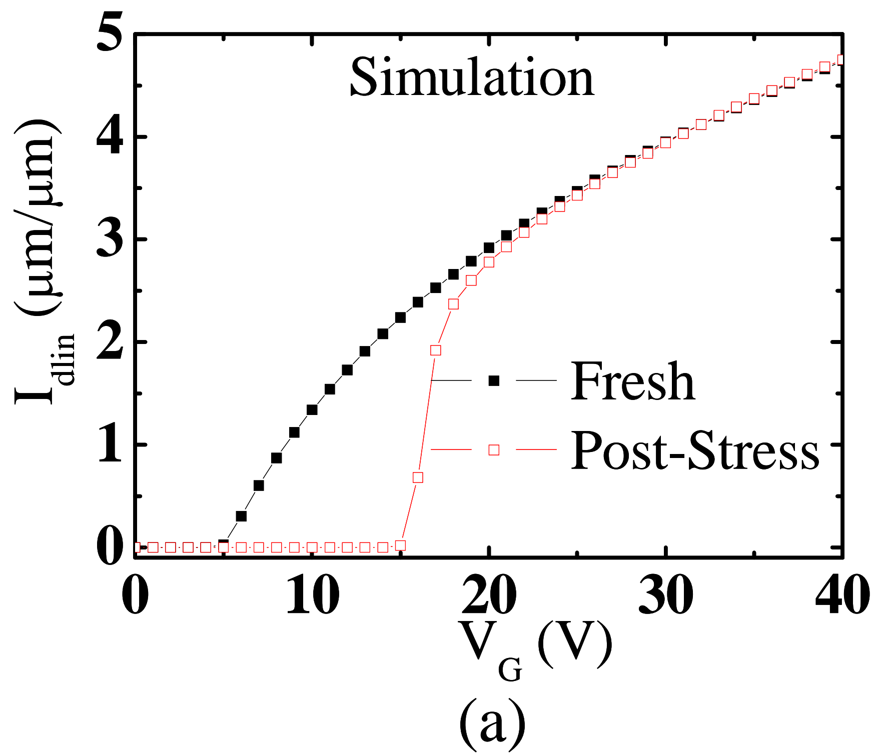
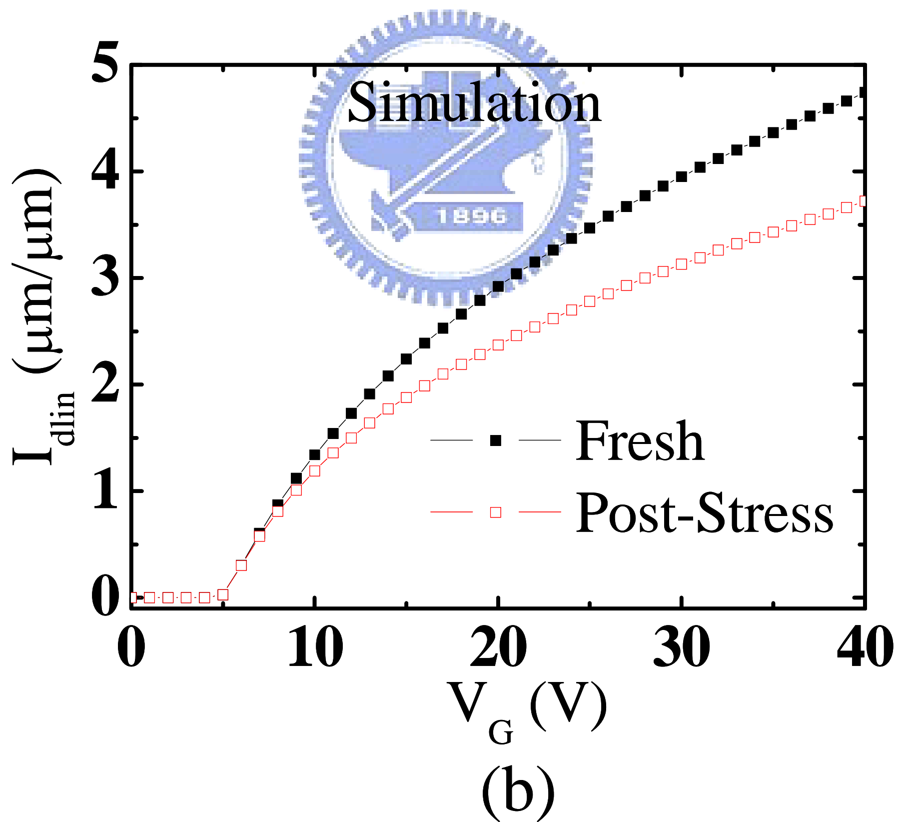


Fig. 3.15 The linear drain current versus V_G before and after mode C stress.



(a)



(b)

Fig. 3.16 Simulated drain current versus gate voltage without and with oxide charges. (a) The oxide charge is placed in the channel and (b) the oxide charge is placed in the bird's beak region.

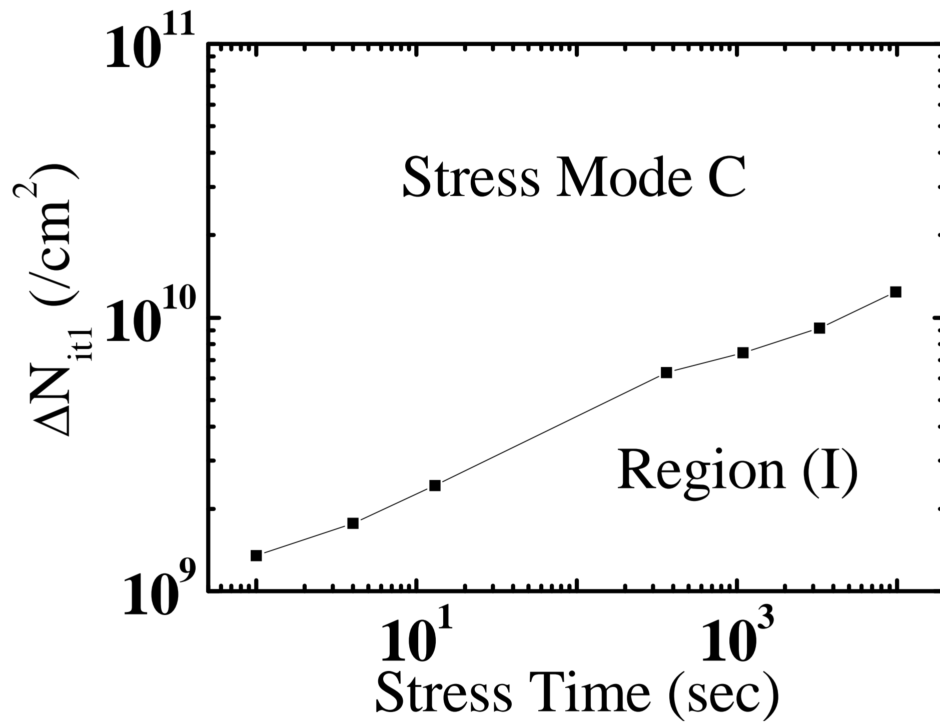


Fig. 3.17 Region (I) interface trap growth rate in stress mode C.

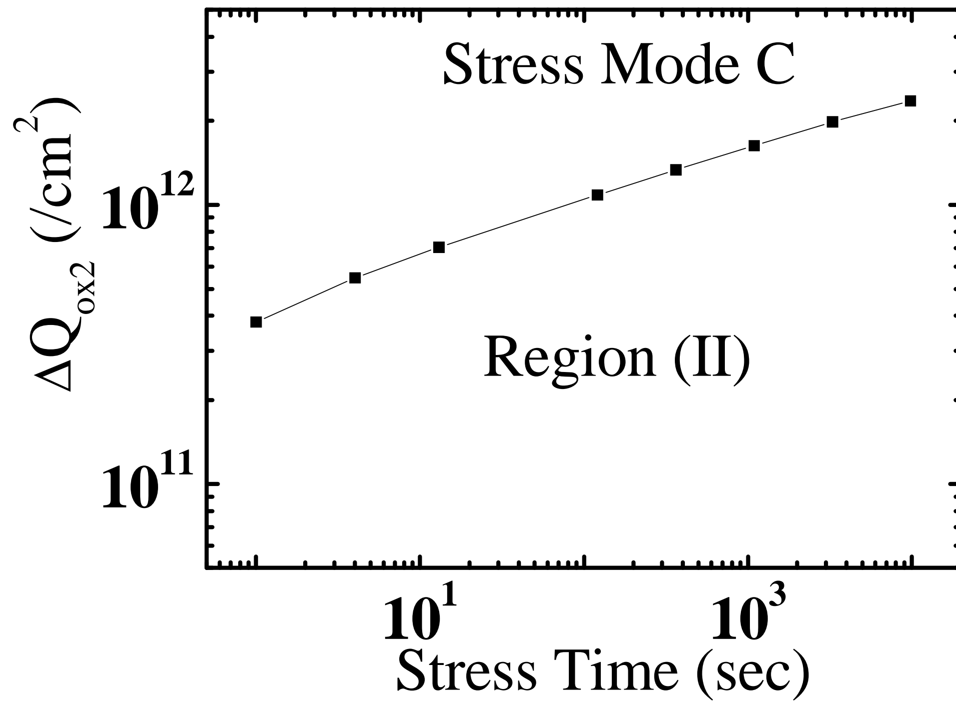


Fig. 3.18 Region (II) oxide charge growth rate in stress mode C.

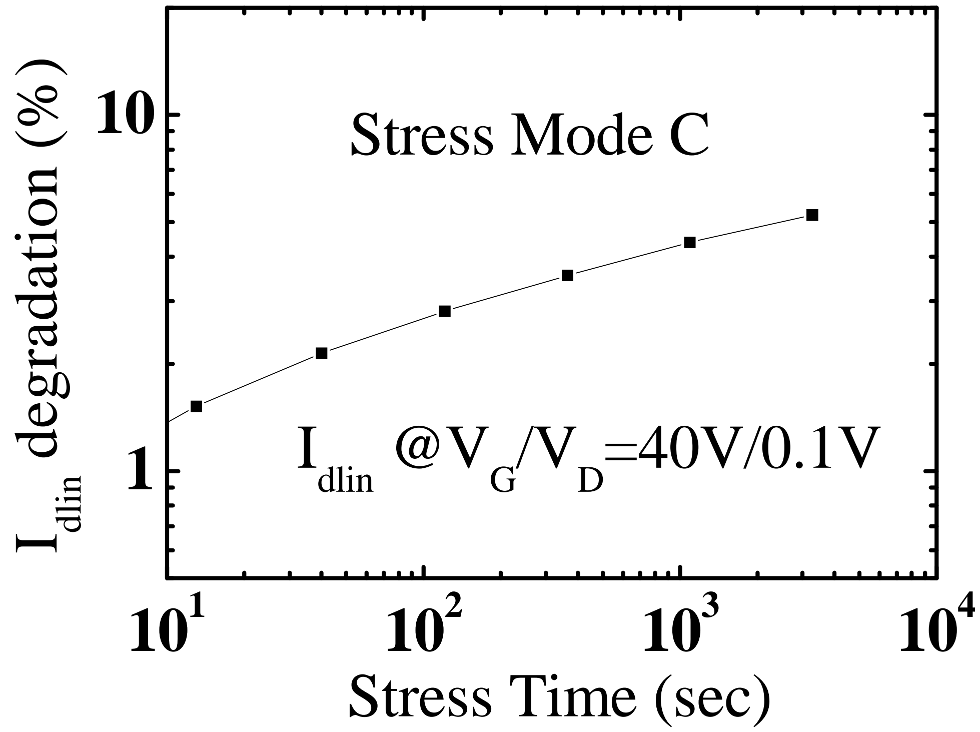


Fig. 3.19 I_{dlin} degradation versus stress time in stress mode C. The degradation is mainly caused by negative oxide creation in the drift region.

Table 3.1 Summary of major oxide and device performance degradations in various stress modes.

Stress Mode	A (Max. I_B)	B	C (Max. I_G)	
Trap Location	Drift Region	Drift Region	Channel Region	Drift Region
Trap Property	N_{it}	Q_{ox}	N_{it}	Q_{ox}
Device Degradation	Flicker Noise Degradation	I_{dlin}	Subthreshold Swing	I_{dlin}

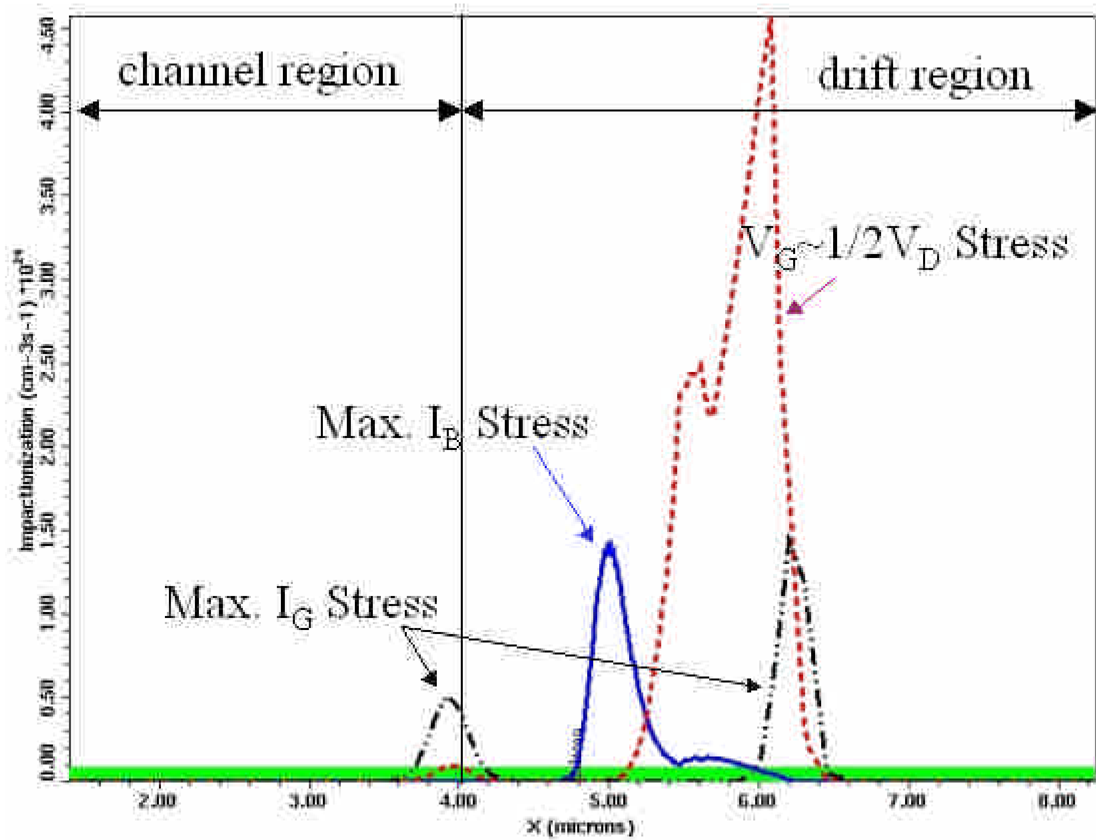


Fig. 3.20 Impact ionization generation rate in (a) Max. I_B stress mode, (b) V_G~1/2V_D stress mode, and (c) Max. I_G stress mode.

Chapter 4

Impact of Self-Heating Effect on Hot Carrier Degradation

4.1 Introduction

Hot carrier induced degradation in lateral diffused MOS (LDMOS) has continuously been one of the major reliability concerns, particular when the operating voltages is high. The degradations of the LDMOS under DC stress conditions have been investigated in many studies [4.1] [4.2] [4.3] [4.4]. However, in most applications, the LDMOS transistors are operated dynamically and subjected to AC stress rather than DC stress [4.5]. In addition, in a high-voltage/high-current operation, self-heating effect (SHE) is significant in the LDMOS. The influence of SHE on AC and DC stress modes are different. To explore the correlation between SHE and hot carrier degradation becomes important to the understanding of the LDMOS reliability constrain.

In this chapter, we will study SHE on hot carrier degradation in DC and AC stress modes. To this purpose, we fabricate a special LDMOS structure, which incorporates a metal contact in the bird's beak region. Thus, we can probe an internal voltage (V_I) transient due to SHE directly. The device cross section is shown in Fig. 2.2 of chapter 2. A top view of the device is illustrated in Fig. 2.1 of chapter2. Three regions of a LDMOS are indicated in the figure, including a channel region (L_{ch}), an accumulation region (L_{acc}) and a field-oxide region (L_{fox}). The contact is arranged in the accumulation region that the internal voltage V_I can be used as a monitor for hot carrier effects in the channel. The contact area is small enough that the device electrical characteristics are not affected.

The device was processed in a 0.18μm CMOS technology with a gate oxide

thickness of 100nm and a channel length of 3μm. The operation voltages are V_G=40V and V_D=40V. To eliminate SHE in measurement, a fast transient measurement setup including a digital oscilloscope is built, as shown in Fig. 4.1. The internal-voltage and drain-current transient in the LDMOS are measured by the V_I contact and a small resistance respectively. Linear drain current (I_{dlin}@V_G/V_D=40V/0.1V) is measured to monitor device degradation under AC/DC stress. A three-region charge pumping technique [4.4] [4.6] is used to locate hot carrier damage area in the device and to identify the type of generated oxide traps. Two-dimensional numerical device simulation is performed to calculate a device temperature distribution and corresponding hot carrier effects.

4.2 Self-Heating Characterization

Fig. 4.2(a) shows a normalized drain current (I_D/W) versus V_D in small and large gate width devices in DC (Agilent 4156) measurement. The I_D/W in a linear region is nearly the same, indicating no process variations in these two devices. However, the larger width device exhibits a smaller I_D/W in the saturation region because of larger power consumption and thus a larger SHE. The reduction of the saturation current is attributed to self-heating induced mobility degradation [4.7] [4.8]. Fig. 4.2(b) compares the I_D/W from a DC and from a fast transient measurement for the large width device. A larger I_D/W is noticed in the transient measurement because of the elimination of SHE. In addition, SHE is manifested in the internal voltage measurement results by Agilent 4156 and by the fast transient setup (Fig. 4.3). The larger V_I in a non-SHE condition is attributed to a higher mobility in accumulation region, thus resulting in a smaller drift region resistance. A larger internal voltage in non-SHE condition implies a stronger hot carrier stress in the channel region.

4.3 Degradation Characteristics in AC/DC Stress

Two stress modes (maximum I_B, and maximum I_G) are chosen in the study of hot carrier degradation in n-LDMOS. The I_G-V_G and I_B-V_G of a n-LDMOS are shown in Fig. 4.4. The maximum I_B stress is applied at V_G / V_D = 8V / 50V, while the maximum I_G stress is applied at V_G / V_D = 50V / 50V. The bias conditions of the two stress modes are also indicated in Fig. 4.4. It should be noticed that the I_B in figure 4.4 reveals a double-hump behavior [4.9] because of a series connection with a lightly-doped drift region. Fig. 4.5 shows AC and DC stress induced I_{dlin} degradations in the above two stress modes. Maximum I_B stress shows a slight difference in I_{dlin} degradation between AC and DC stresses, implying that SHE is not important at a lower stress V_G. However, in maximum I_G stress, AC stress shows much more I_{dlin} degradation than DC stress. Moreover, strong stress-frequency (Fig. 4.6(a)) and duty cycle (Fig. 4.6(b)) dependence is observed. In Fig. 4.6(a), the I_{dlin} degradation increases with frequency and then becomes saturated. A corner frequency is found to be f_1 = 20 kHZ at a duty cycle = 10%. In Fig. 4.7, we plot I_{dlin} degradation versus pulse duration, i.e., duty cycle / frequency, in AC stress. A corner time of ~5μs is obtained, suggesting that SHE becomes important as pulse duration is longer than ~5μs.

Fig. 4.8 shows a V_I transient in a pulsed gate and DC drain voltage condition (V_D=40V). A gate voltage pulse with a low-level voltage of 15V and a high-level voltage of 40V is applied. The low-level voltage of 15V is chosen to prevent V_I contact breakdown. The V_I decreases with time due to SHE and the onset time of SHE is extracted to be around 5μs. This result is consistent with the findings from AC stress induced degradation (Fig. 4.7) and from the literature which has a time constant of 4.8μs [4.10] in SOI technology.

A charge pumping measurement (I_{cp}) result is shown in Fig. 4.9. A distinguished

three-stage feature in I_{cp}-V_{gL} is observed, corresponding to the three regions of a LDMOS respectively. By comparing the pre-stress and post-stress I_{cp} in each stage, we are able to separate interface trap (N_{it}) and fixed oxide charge (Q_{ox}) creation in each region of the device. The result in Fig. 4.9 reveals that AC stress generates more N_{it} in the channel region and more Q_{ox} in the accumulation region. The larger trap generation rate in AC stress results from a smaller temperature rise and thus a larger stress gate current (Fig. 4.10). For the 100nm thick gate oxide, the stress gate current is major determined by the hot carrier injection rather than by channel electron tunneling. Thus, Fig. 4.10 shows a larger stress gate current at a lower temperature. The self-heating induced temperature change in a LDMOS is simulated by a two-dimensional numerical device simulation (Fig. 4.11). In the simulation, a thermal electrode is placed at the bottom of the device and is assumed to be isothermal at 300°K. Homogeneous Neumann boundary conditions are used at all boundaries not contacted by the thermal electrode. In Fig. 4.11, the drift region shows a higher temperature change than channel region, implying a larger mobility degradation and thus a higher drift region resistance. By compared Fig. 4.11 (a) and (b), we observe that the SHE is stronger at a higher V_G. To further support the V_I measurement result in Fig. 4.3, the V_I change due to SHE is plotted in Fig. 4.12. The ΔV_I is extracted underneath the gate oxide of ~20Å. The simulation also reveals a higher V_I in a non-SHE condition. Good agreement between measurement and simulation is obtained in Fig. 4.12. Because of a larger V_I in the non-SHE condition, the simulated impact ionization rate is stronger in the non-SHE condition (Fig. 4.13). This feature also confirms our charge-pumping results in Fig. 4.9 and concludes a more serious I_{dlin} degradation rate in AC stress (Fig. 4.14).

4.4 Summary

Transient self-heating effect in AC hot carrier stress in LDMOS has been studied by measuring an internal voltage. The self-heating time extracted from the internal voltage transient is around 5μs. A correlation between the AC stress pulse duration and the self-heating time is established. The AC stress at maximum I_G yields the worst hot carrier degradation because of the elimination of self-heating effect.

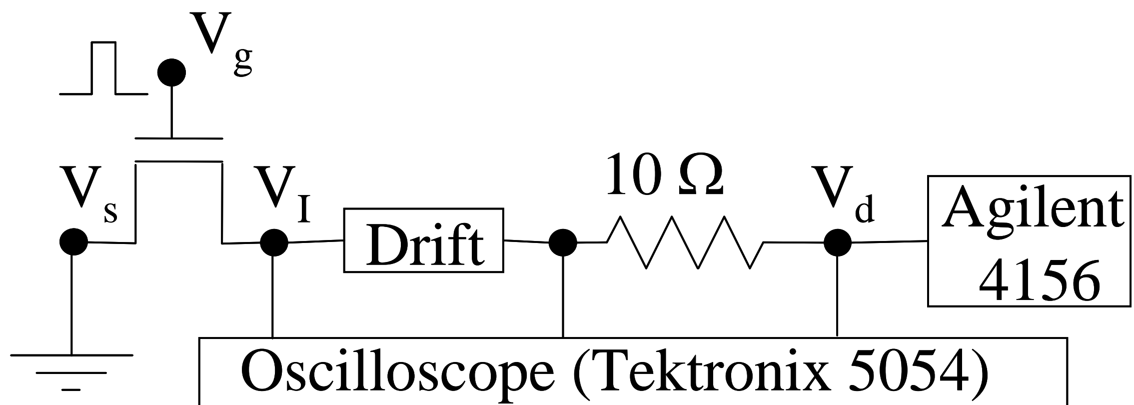
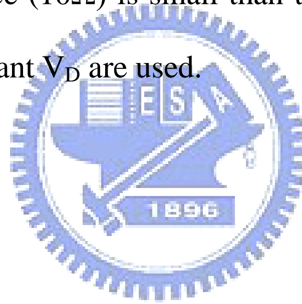
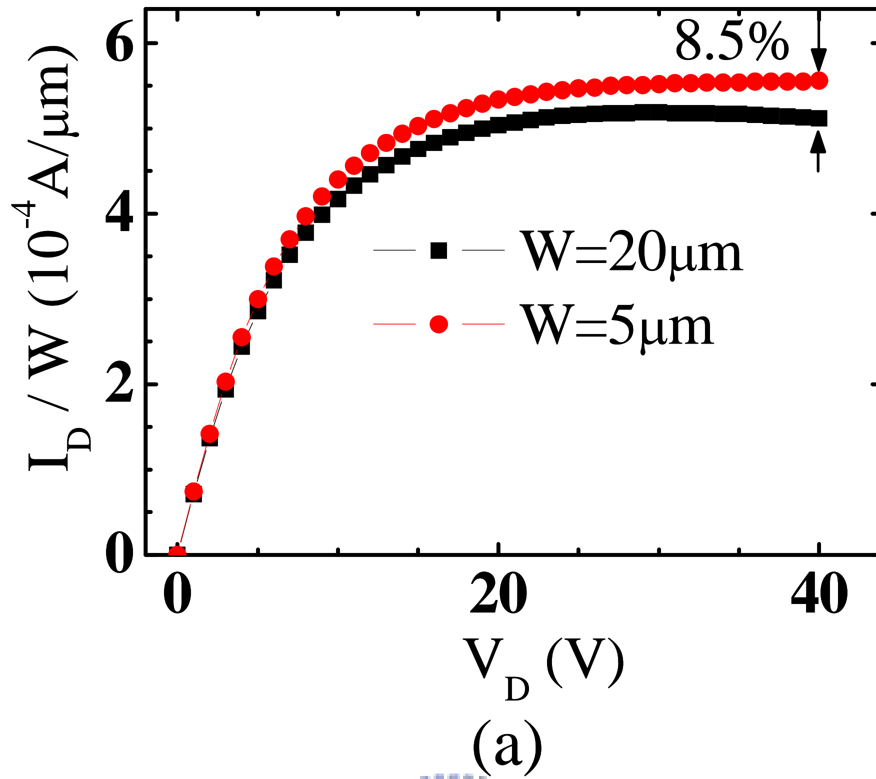
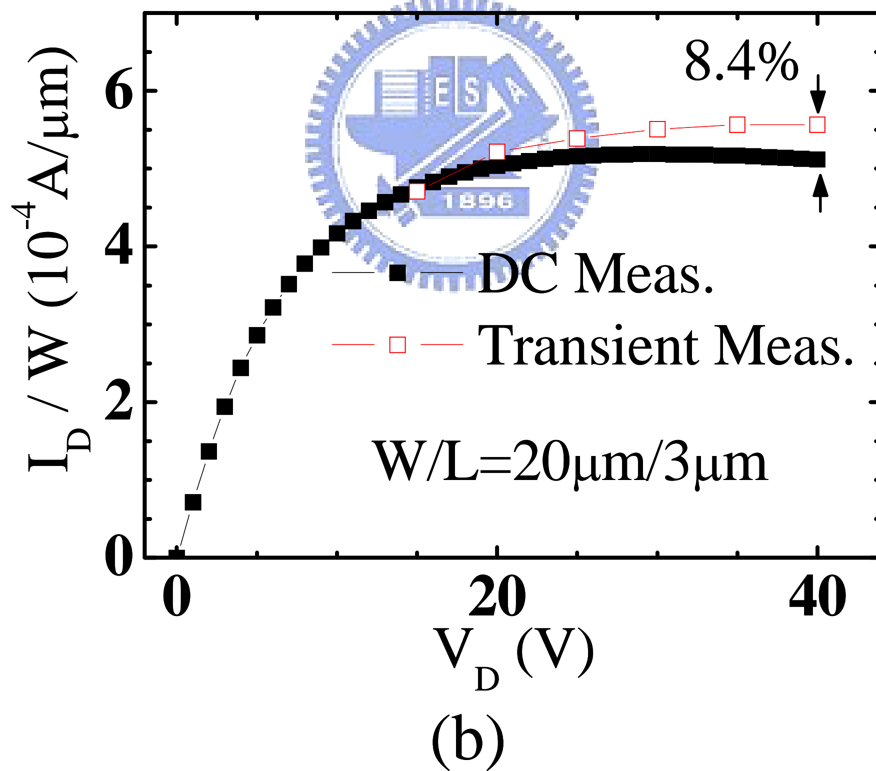


Fig. 4.1 Fast transient measurement setup for drain current and internal voltage (V_I) characterization. The resistance (10Ω) is small than the total resistance (~40V/10mA ~4kΩ). A gate pulse and constant V_D are used.



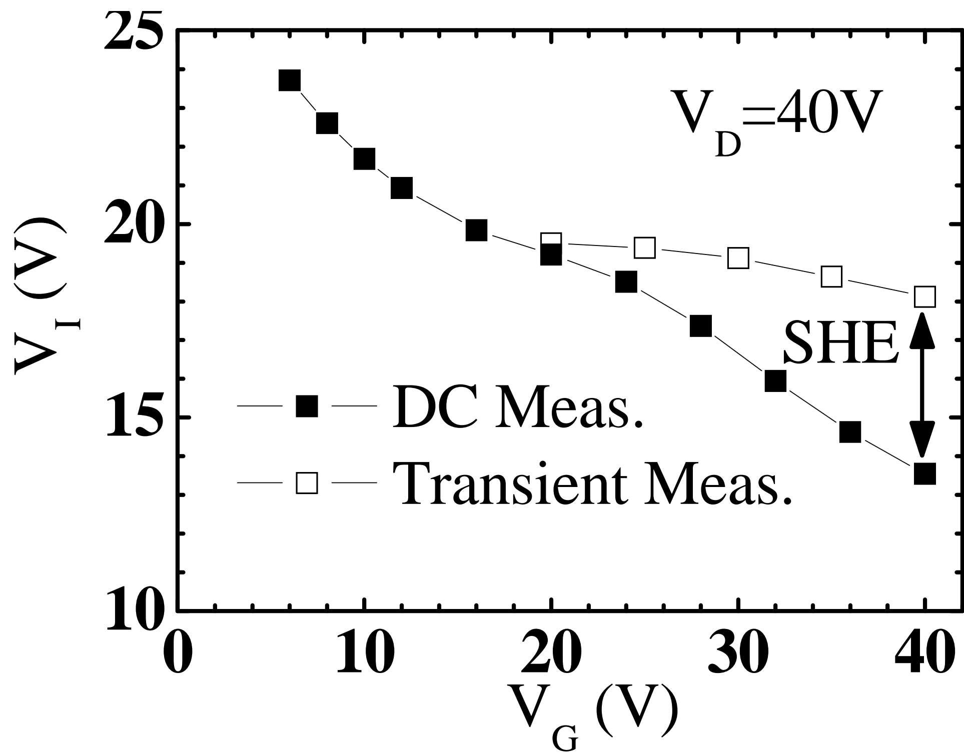


(a)



(b)

Fig. 4.2 (a) Normalized drain current (I_D/W) versus drain voltage in small and large gate width devices in DC measurement (Agilent 4156). (b) The I_D/W from a DC and a fast transient measurement for the large width device.



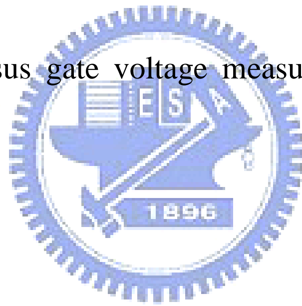


Fig. 4.3 Internal voltage versus gate voltage measured by Agilent 4156 and by a transient measurement setup.

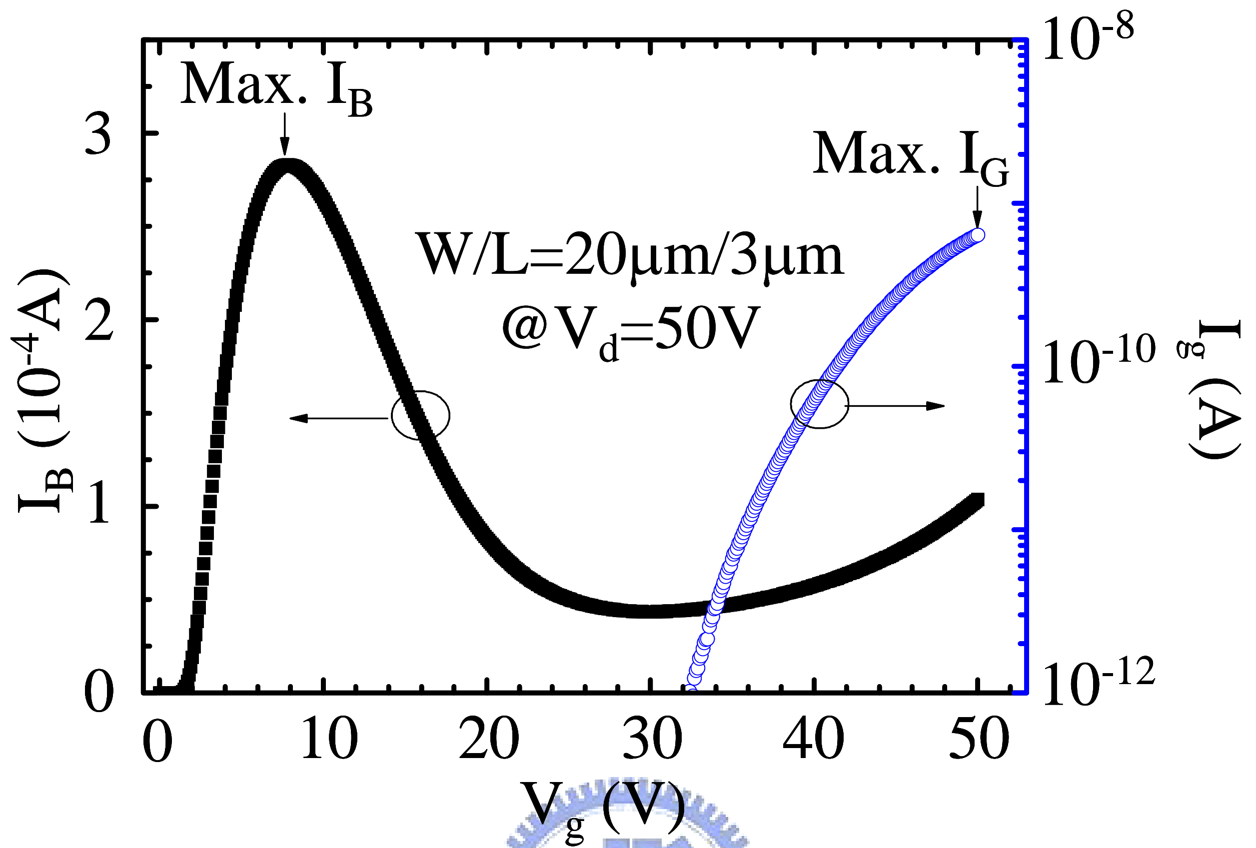


Fig. 4.4 Substrate current and gate current versus gate voltage in a LDMOS. Two hot carrier stress modes are shown, maximum I_B stress and maximum I_G stress.

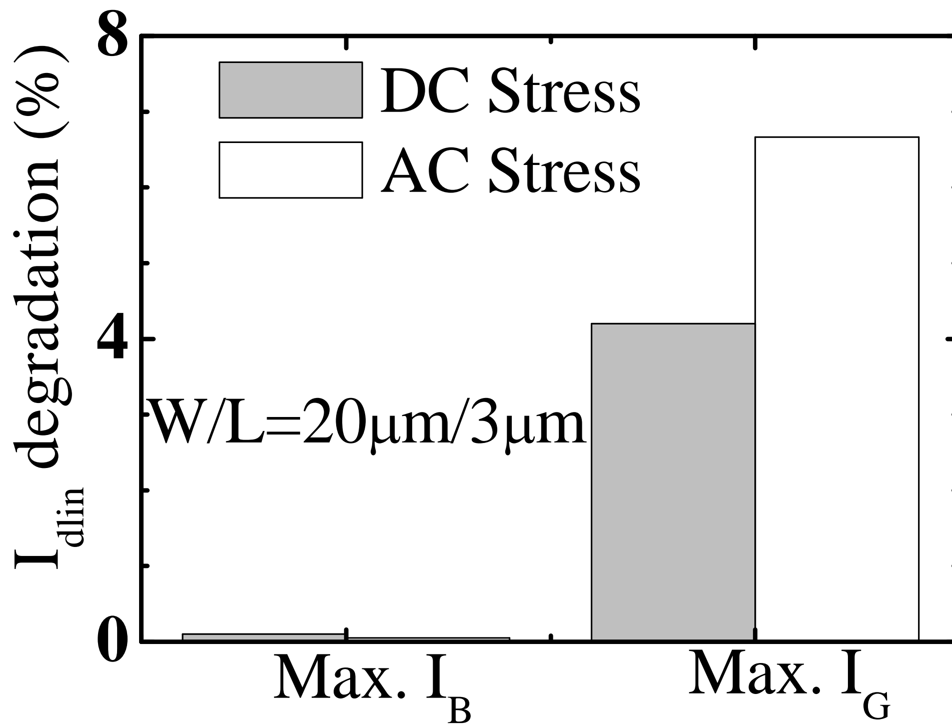
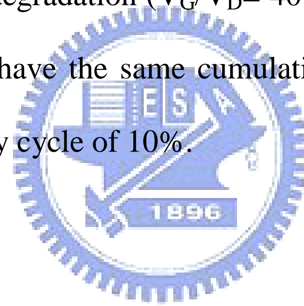
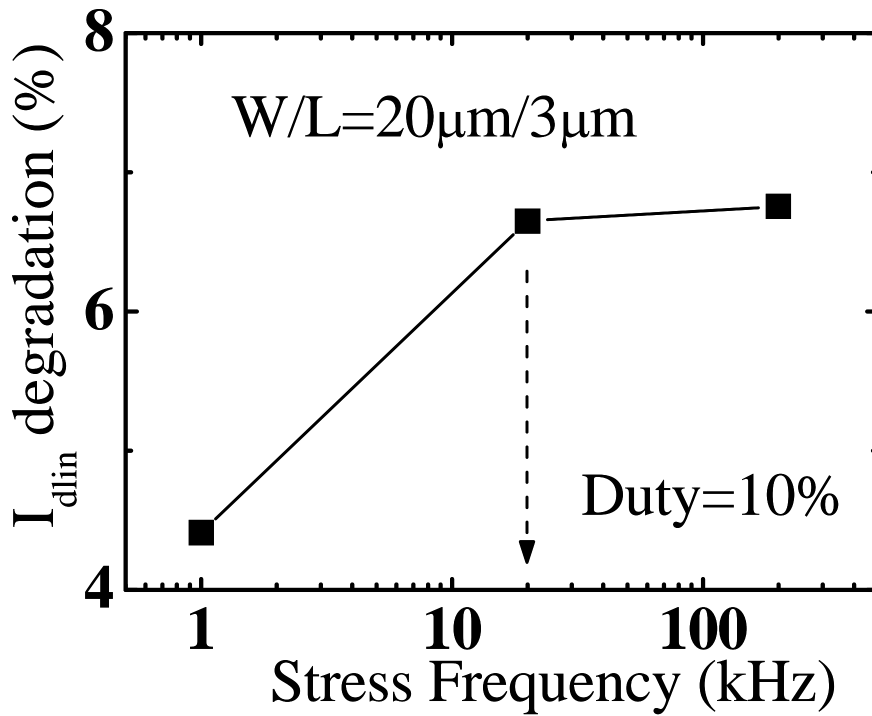


Fig. 4.5 Linear drain current degradation (V_G/V_D= 40V/0.1V) in two hot carrier stress modes. DC and AC stresses have the same cumulative stress time. AC stress has a frequency of 20kHz and a duty cycle of 10%.





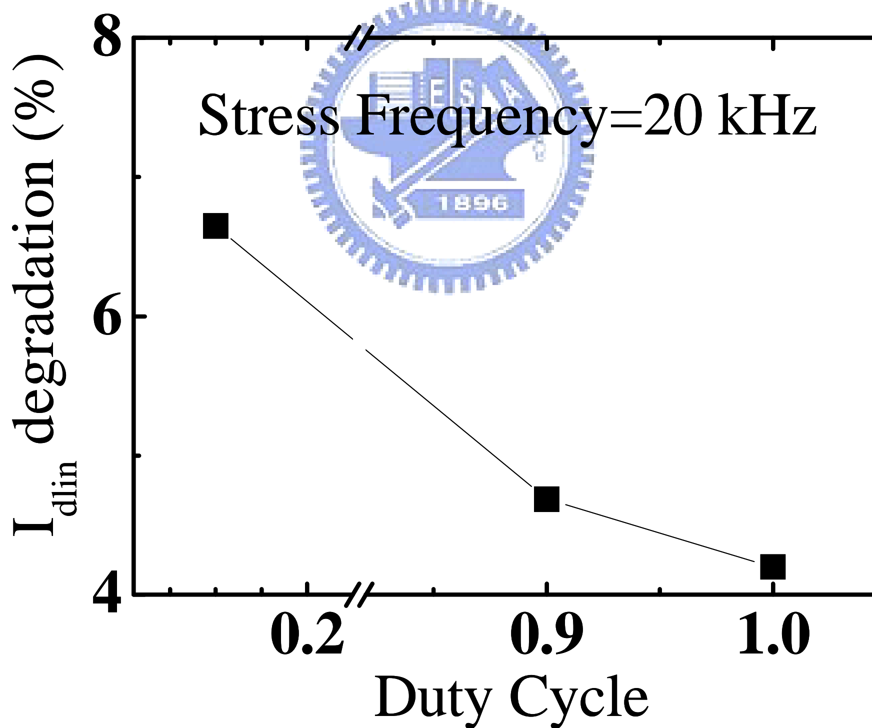
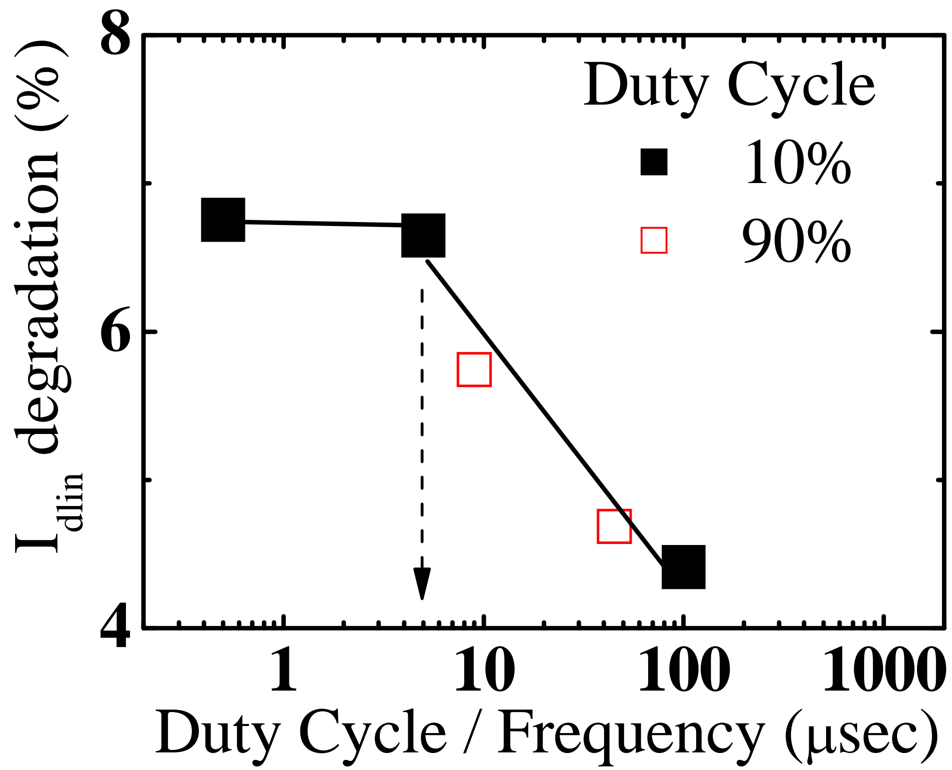


Fig. 4.6 (a) I_{dlin} degradation versus stress frequency with a duty cycle of 10%. A corner frequency (*f1*) is around 20kHz. (b) I_{dlin} degradation versus duty cycle for a frequency of 20 kHZ.



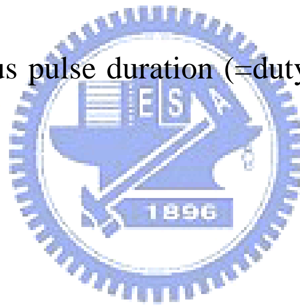


Fig. 4.7 I_{dlin} degradation versus pulse duration (=duty cycle/frequency) in AC stress. The corner time is around 5μs.

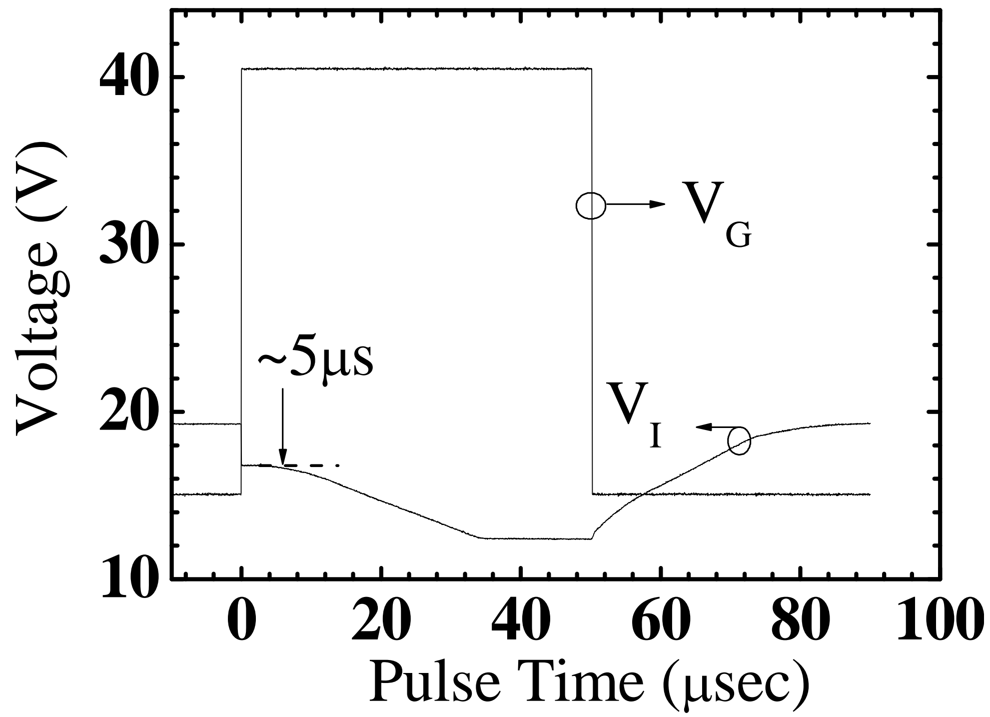


Fig. 4.8 The internal voltage (V_I) transient in a pulsed gate and DC drain voltage (VD=40V) condition. The waveforms of V_I and V_G are plotted. The onset time for SHE is ~5μs.

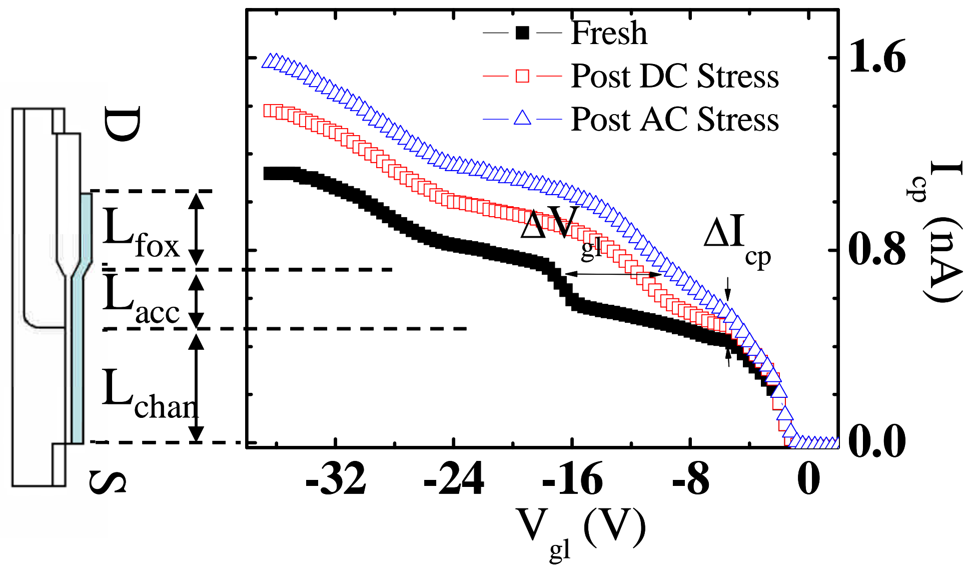
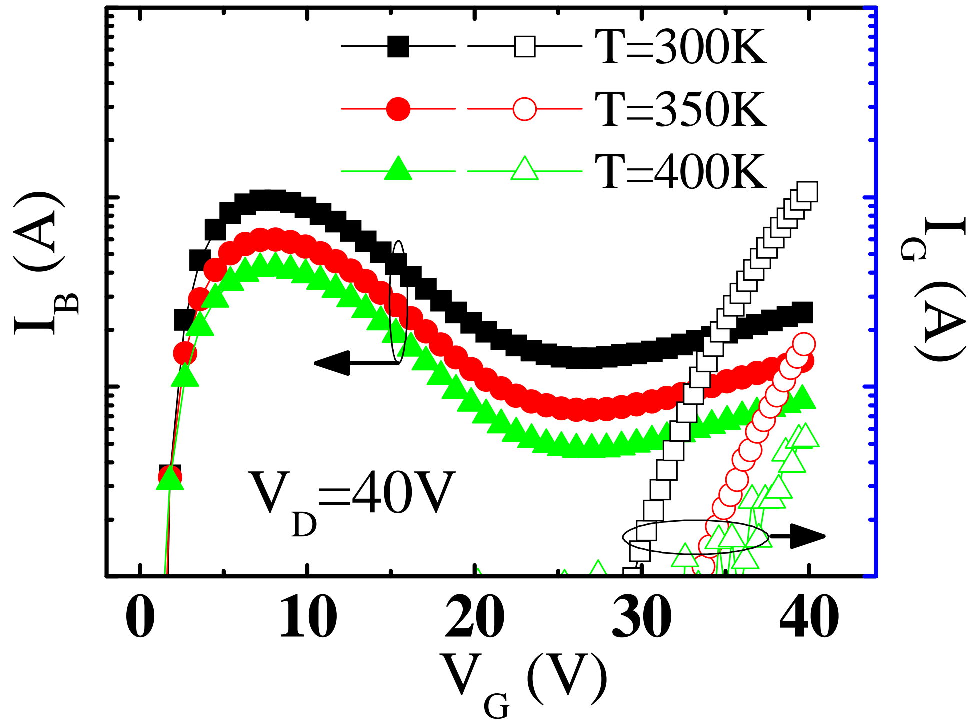


Fig. 4.9 Three-region charge pumping measurement results after maximum I_G AC and DC stress. A V_{gL} shift is in the accumulation region and a I_{cp} increase is in the channel region.



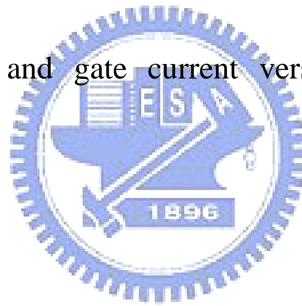
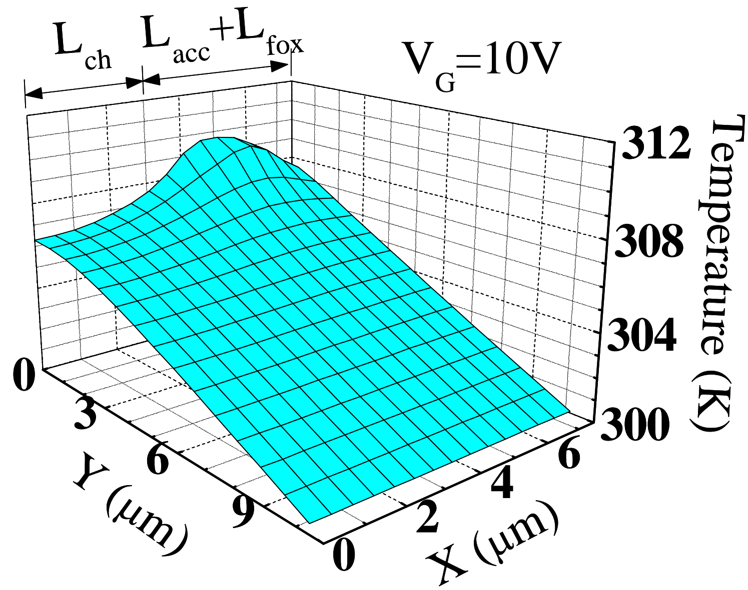
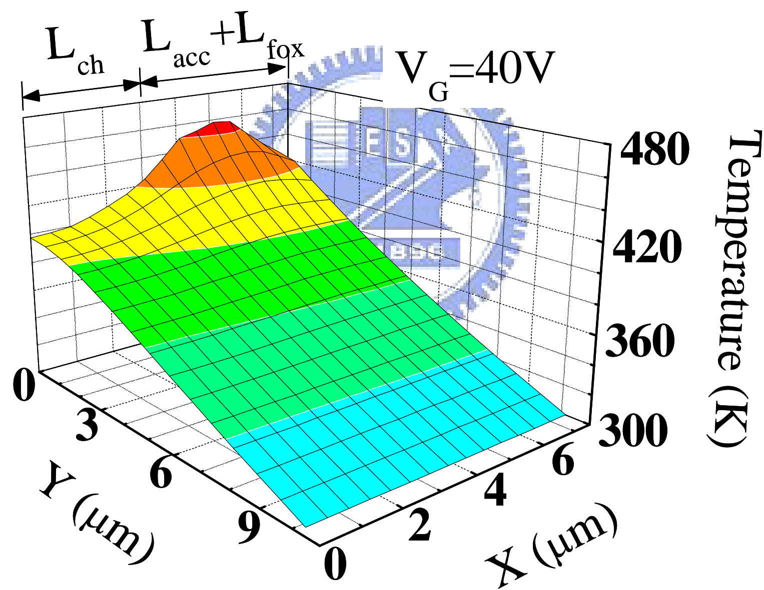


Fig. 4.10 Substrate current and gate current versus gate voltage for different temperatures.



(a)



(b)

Fig. 4.11 Simulation of a temperature distribution with SHE. The ambient temperature is 300K. X axis is the direction from source to drain. Y axis represents the depth. (a) V_G/V_D=10V/40V. (b) V_G/V_D=40V/40V.

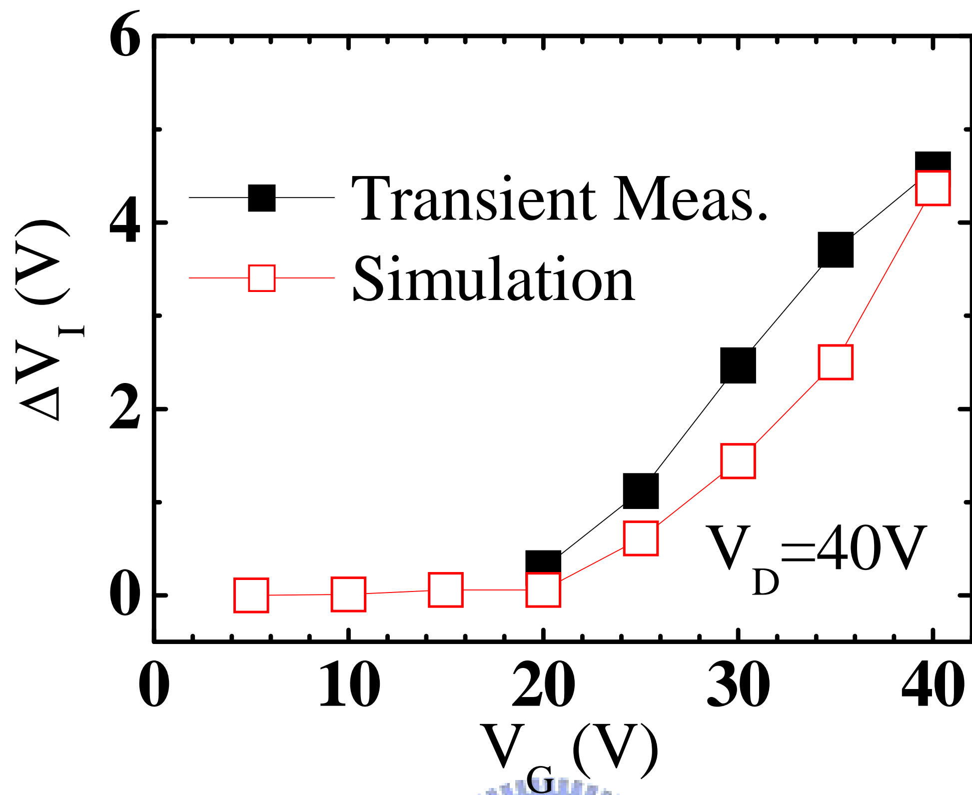
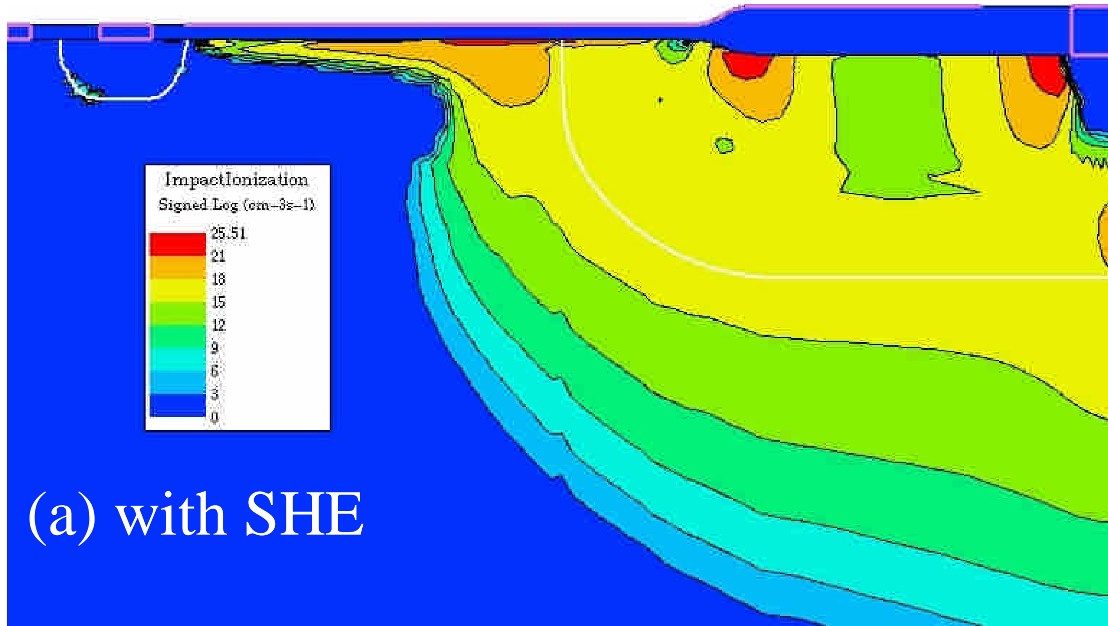


Fig.4.12 Internal voltage change (V_I(non-SHE) - V_I(SHE)) versus gate voltage from measurement and from simulation.

ESA



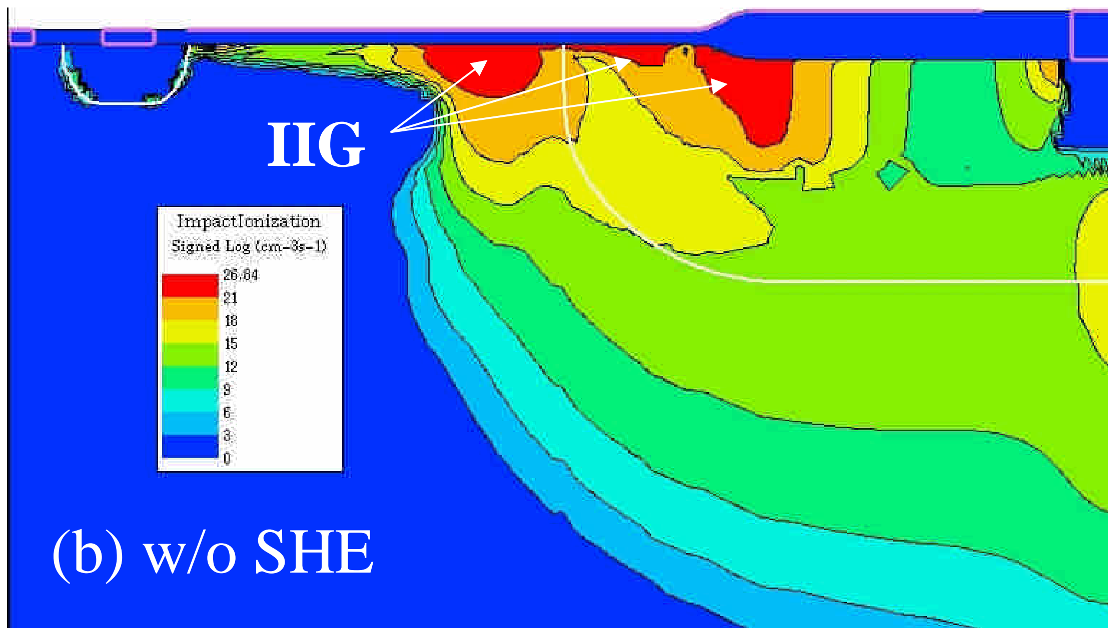
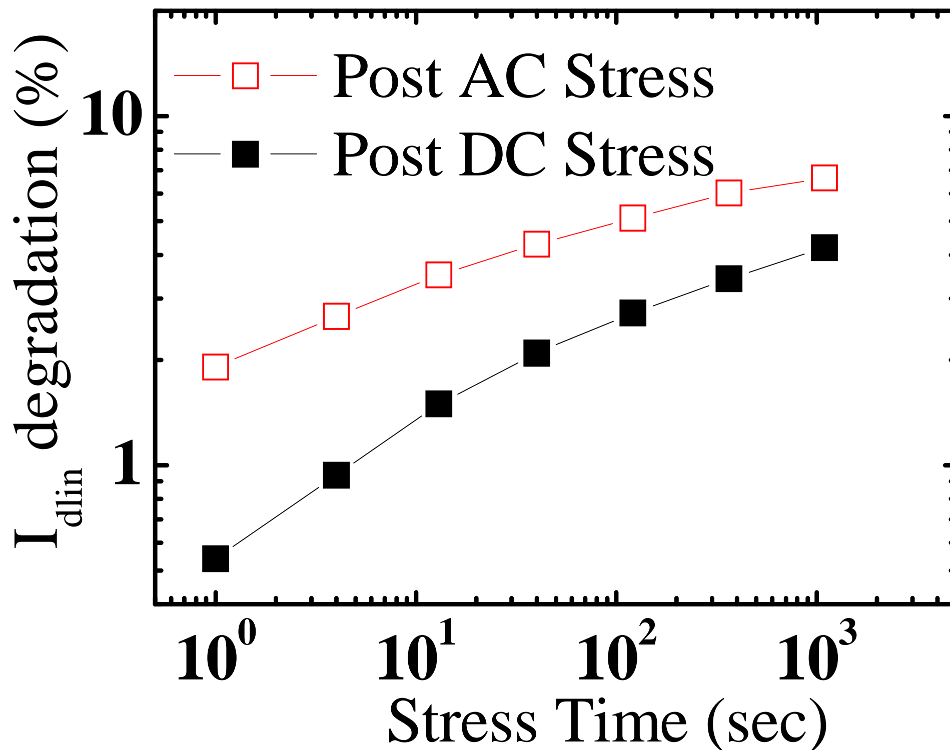


Fig. 4.13 Two-dimensional device simulation of impact ionization generation (IIG) rate at V_G/V_D=40V/40V. (a) SHE is included and (b) SHE is not included.



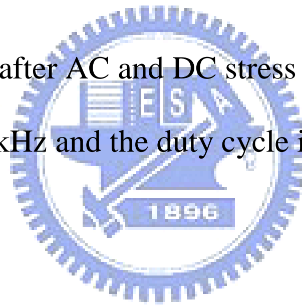


Fig. 4.14 I_{dlin} degradation rate after AC and DC stress in maximum I_G stress condition. The AC stress frequency is 20kHz and the duty cycle is 10%.

Chapter 5

A Two-Component LDMOS Model Including Self-Heating Effect

5.1 Introduction

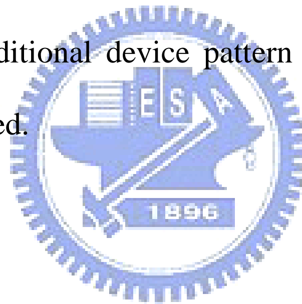
The efficiency of the LDMOS circuit design depends much on the accuracy of the device model. A precise model greatly enhances the success of chip production. However, LDMOS modeling is rather difficult compared to a conventional MOSFET due to the diverse nature of the channel region and the drift region. A major obstacle is the drift region model because of its complex dependence on external terminal voltages.

Two model types are generally presented in the literature. One is compact model for the HV devices, which stresses on the construction of an intrinsic MOS model and treats the drift region as a trivial extension [5.1]. The target of compact model is to eliminate any internal node that exists in a model description. To fulfill this target, very simple expressions are needed for both the channel and drift regions [5.1]. Some of compact models solve the potential at the internal node by means of a numerical iteration procedure, like in [5.2], [5.3], [5.4]. Another approach for compact model is to express the potential at internal node as a function of external terminal voltages [5.5], [5.6], [5.7]. The compact model has a less flexibility for IC designers and is hard to integrate with another kind of device model.

The second type of LDMOS model is macro-model, which combines several circuit elements in a LDMOS [5.8], [5.9], [5.10]. The use of the macro-model defines an internal node between two circuit elements. The channel part of a LDMOS is generally modeled by a MOS element and the drift region is regarded as a series connection of the other circuit element, such as a nonlinear resistance [5.8], [5.9] or a

JFET [5.10]. In their modeling methodology, the MOS model is extracted from a global fitting rather than a dc measurement. A discontinuity problem may be introduced in a transition region between linear and saturation regions. In both compact model and macro-model, however, self-heating effect is rarely discussed. None of the studies take into account the correlation between internal voltage and self-heating (SH) effect.

In this chapter, a two-component device model including self-heating induced internal voltage transient is developed. A new modeling method for the channel/drift regions is proposed by fitting a low-V_G/high-V_G drain current. We use an internal voltage (V_I) to control drain current in SH and in non-SH conditions. A single equation is also utilized to solve the continuity problem in our macro-model. By using our modeling method, no additional device pattern is required and an accurate dc modeling result can be achieved.



5.2 Model Description

A MOS element with a series connection of a V_I controller is used in this chapter, as shown in Fig. 5.1(a). The MOS element and the V_I controller describe DC characteristics of the channel and the drift region. A current flowed into the MOS element is denoted by I_{ch} whereas a current flowed into both the MOS element and the V_I controller is denoted by I_D. As mentioned in chapter 2.3.1, I_D at a lower V_G regime and at a linear portion of high V_G regime are major determined by the channel-part of a LDMOS, indicating that the operating regime of LDMOS is controlled by the MOS element. This feature is also described in Fig. 5.1(b).

Fig. 5.2 shows a modeling flow of the LDMOS. An input bias of V_G and V_D in the V_I controller determines a V_I for the MOS element. As the V_I is determined, the voltage drops in the channel region and in the drift region are also determined, which

results in a drain current (I_D). To integrate self-heating effect, an illustration of the V_I controller is shown in Fig. 5.3. The V_I is expressed as a combination of two operating conditions; one is a V_I at a non-SH condition and the other is a V_I transient due to self-heating.

5.3 Modeling Method

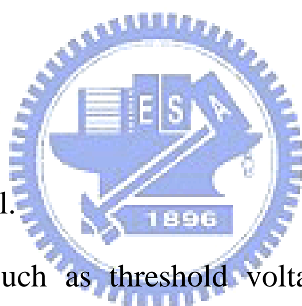
A modeling method for the MOS element and the V_I controller is proposed by fitting a low-V_G/high-V_G drain current, as shown in Fig. 5.4. An I_D-V_D in a LDMOS is divided into a low-V_G and a high-V_G part according to the description of chapter 2.3.1. There are five extraction steps in this modeling method, including

(1), (2) MOS model,

(3) V_I simulation step,

(4) V_I controller model,

(5) LDMOS macro-model.



Some physical parameters, such as threshold voltage (V_{TH0}), mobility (μ_0), and saturation velocity (v_{sat}), are considered in step (1) and (2) as a format of BSIM3V3 [5.11]. In step 3, a V_I simulation method is developed to extract the V_I. Fig. 5.5 shows a detail of this method. A MOS model extracted from step 1 and 2 is used to describe dc characteristics of the channel. The measured I_D in a LDMOS is modeled as an input current source. A typical V_I simulation result is shown in the inset of Fig. 5.5. The V_I-V_D exhibits a saturated behavior at a higher V_D because the I_D is holding as a constant. In addition, a large V_I change in the saturation is attributed to self-heating effect.

5.3.1 MOS Model

Fig. 5.6 shows a comparison of a fitting result for the MOS model. Symbol

represents a measured I_D in a LDMOS while line represents a simulation result in the MOS model. Since drain current in the linear region is determined by the channel, the V_I in the linear region is close to the V_D and thus a match between I_{ch} and I_D is observed. Similarly, a comparison of a fitting result at low V_G and at high V_G are shown in Fig.5.7 (a) and (b). A difference between I_{ch} and I_D at a high-V_G/high-V_D regime is observed because of the voltage drop in the drift region. The extracted MOS parameters are summary in Appendix A.

5.3.2 V_I Controller Model

In order to ensure the numerical robustness, we use a single equation to describe the V_I in both linear and saturation regions, which is defined by an effective internal voltage ($V_{I,eff}$).

$$V_{I,eff} = V_{Isat} - \frac{1}{2} \cdot [V_{Isat} - V_D - \Delta + \sqrt{(V_{Isat} - V_D - \Delta)^2 + 4\Delta \cdot V_{Isat}}\,] \quad (5.1)$$

$V_{I,eff}$ is similar to the smooth function of BSIM3 [5.11], a function that gradually changes a variable between two extreme values, i.e. 0 and V_{Isat} . The definition of V_{Isat} is derived in equation C4 of Appendix C. The parameter Δ determines the degree of smoothness in the quasi-saturation transition and is expressed as a polynomial function of V_G and V_D (shown in Appendix B, line 230).

A comparison of V_I in a non-SH condition is shown in Fig. 5.8. Several fitting parameters for the V_I controller model are listed in Appendix B. The V_I in both linear and saturation regions is well described by the V_I controller model and no discontinuity is observed. A completed V_I controller model is expressed as $V_I(t)=V_I(t=0^+)+\Delta V_I(t)$, where $\Delta V_I(t)$ represents the impact of self-heating on the V_I and is modeled by a RC network in the next section. The equation of $V_I(t=0^+)$ is discussed in Appendix C.

5.3.3 Self-Heating Model

A RC network for SH induced V_I transient is illustrated in Fig. 5.9. A voltage controlled current source, which used a polynomial function of 4th order, is adopted. The voltage drop across RC is modeled as a SH-induced V_I change, denoted as $\Delta V_I(t)$. It should be noticed that our RC network describes a V_I change rather than a temperature change in a conventional SH model [5.12]. Fig. 5.10 indicates a time constant τ_C of the V_I transient. A measured I_D transient is converted into a corresponding V_I transient by using the V_I simulation method. In a transient operation, the current source starts to charge the capacitor C and thus $\Delta V_I(t)$ increases. When the capacitor is fully-charged, $\Delta V_I(t)$ becomes a constant value, which is equal to the value β extracted from Fig. 5.10. A comparison of the V_I between the simulation and model is shown in Fig. 5.11. The V_I is defined as $V_I(t) = V_I(t=0) - \Delta V_I(t)$. The correlation between the V_I and the pulse time t can be expressed in an analytical equation, i.e. $V_I(t) = V_I(\infty) + \beta \cdot \exp(-\frac{t}{\tau_C})$. Thus, the $\Delta V_I(t)$ can be expressed as $\Delta V_I(t) = \beta \cdot [1 - \exp(-\frac{t}{\tau_C})]$. Complete expressions for the current source, resistor, and capacitor are also listed in Appendix B from line 330-350.

By incorporating the non-SH V_I model and the SH model, the V_I model including self-heating is obtained. A comparison of I_D transient between the measurement and the LDMOS model is shown in Fig. 5.12. Since our V_I model has described the V_I transient accurately, a successful description of the I_D can be achieved.

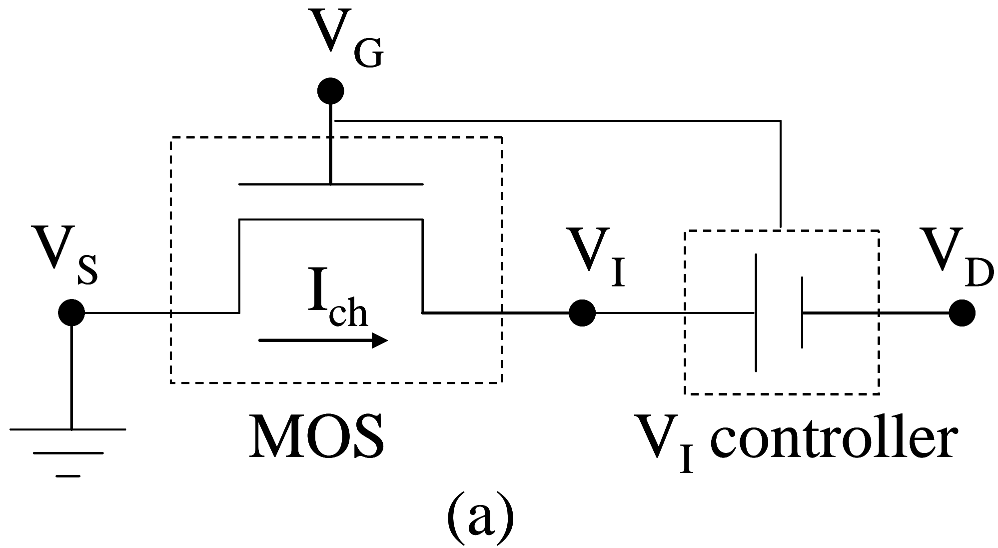
5.4 Results and Discussions

The modeling results are compared and discussed in this section. In the following figures, symbols represent a dc measurement in a LDMOS while solid lines represent a simulation in the LDMOS model. The I_D in the non-SH condition is extracted from the I_D transient at $t=0^+$, whereas the I_D in the SH condition is extracted from the I_D transient at t=30μs. Fig. 5.13 (a) and (b) show an I_D-V_D at low-V_G and at high-V_G regions. In the high-V_G regime, an I_D due to self-heating effect is observed. Compared to the fitting results of Fig. 5.6(a), the I_D in Fig. 5.13(a) is slightly lower than the I_D in Fig. 5.6(a), which is attributed to the use of the V_I controller. However, in the high-V_G regime of Fig. 5.6(b), the I_D is greatly suppressed. This again is due to the use of V_I controller, which limits the V_I and restricts the I_D in the MOS model.

The I-V characteristics in the linear region and in the saturation region are also characterized in Fig. 5.14. An accurate I_D and G_m in the linear region are achieved. Note that as V_D is small, the device characteristic is major controlled by the MOS model. Thus, the V_{TH} in the LDMOS model is nearly the same with that in the MOS model. A good agreement between model and measurement results has proven that the V_I controlled self-heating model is successfully used in the LDMOS modeling.

5.5 Summary

Two components V_I-based SPICE model including self-heating effect in an n-LDMOS is developed. The self-heating induced V_I change is modeled and explained for the first time. By using the specially-designed modeling method in our SPICE model, only LDMOS I-V measurement is needed and a very good fitting result can be achieved.



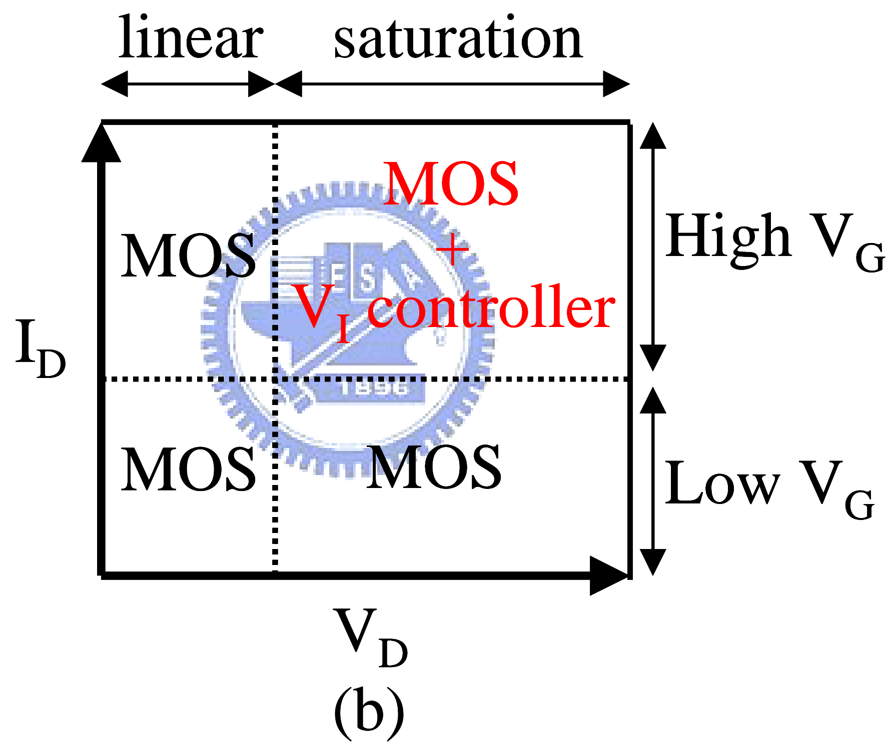


Fig. 5.1 (a) An equivalent circuit of the LDMOS model. An internal voltage (V_I) between two circuit elements is illustrated. The MOS element represents the channel region while the V_I controller accounts for the drift region. (b) Illustration of different operating regions controlled by each component.

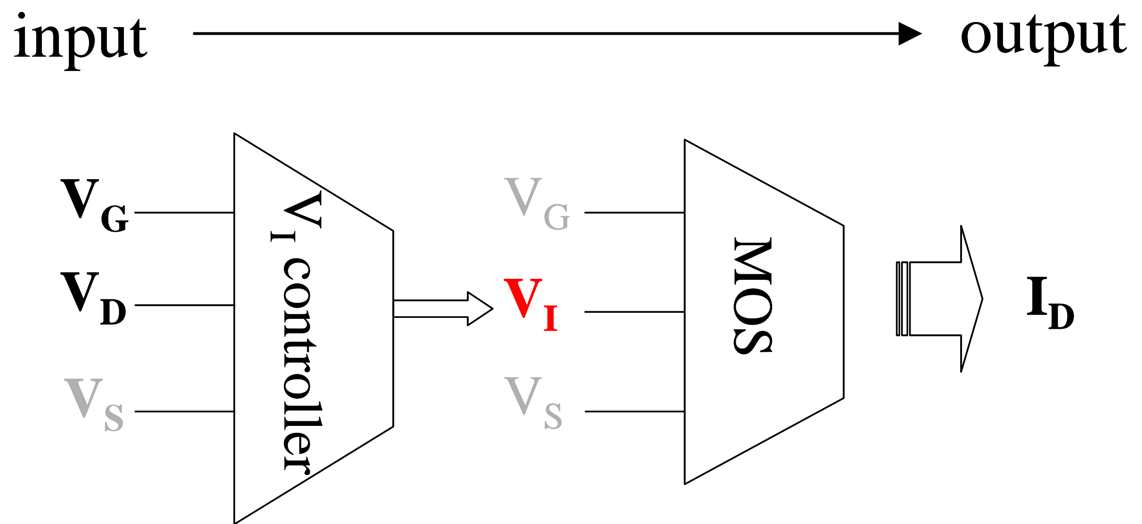
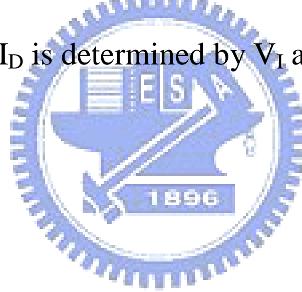


Fig. 5.2 Illustration of input/output process of the LDMOS model. The V_I is controlled by V_G and V_D. The I_D is determined by V_I and V_G.



E S
1896

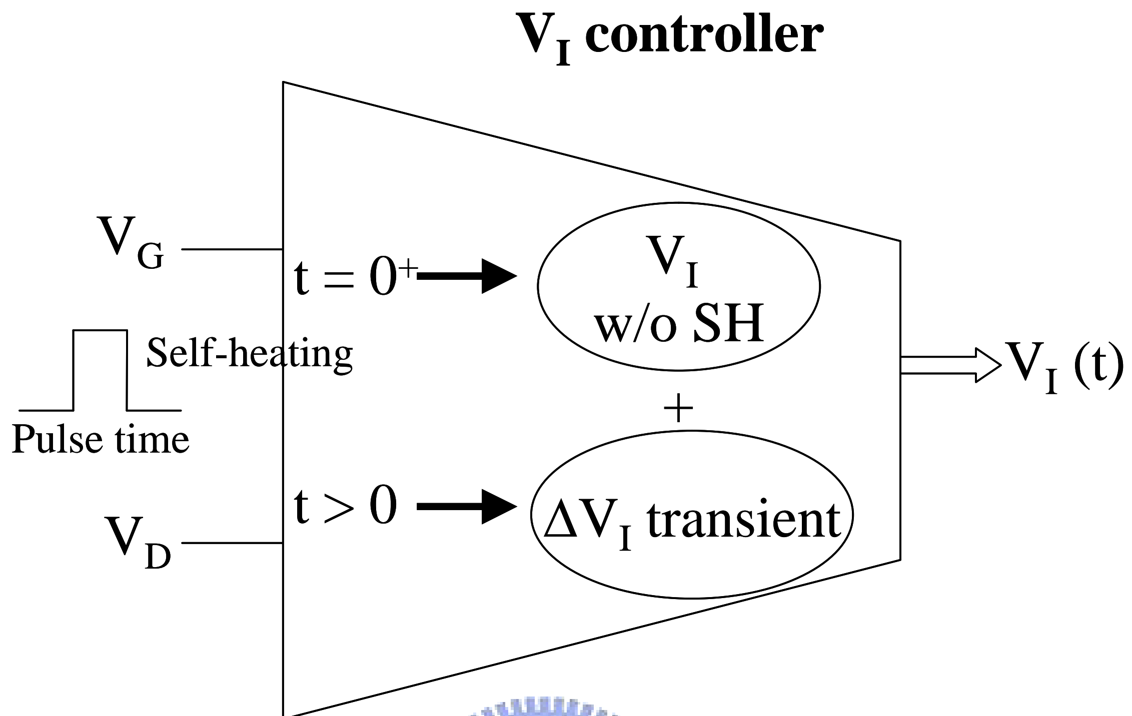


Fig. 5.3 Illustration of the V_I controller. An internal voltage transient due to self-heating (SH) is taken into account. The V_I at $t=0^+$ is expressed as a function of V_G and V_D (listed in Equation 1). The ΔV_I transient is described by a RC network in Fig. 5.9.

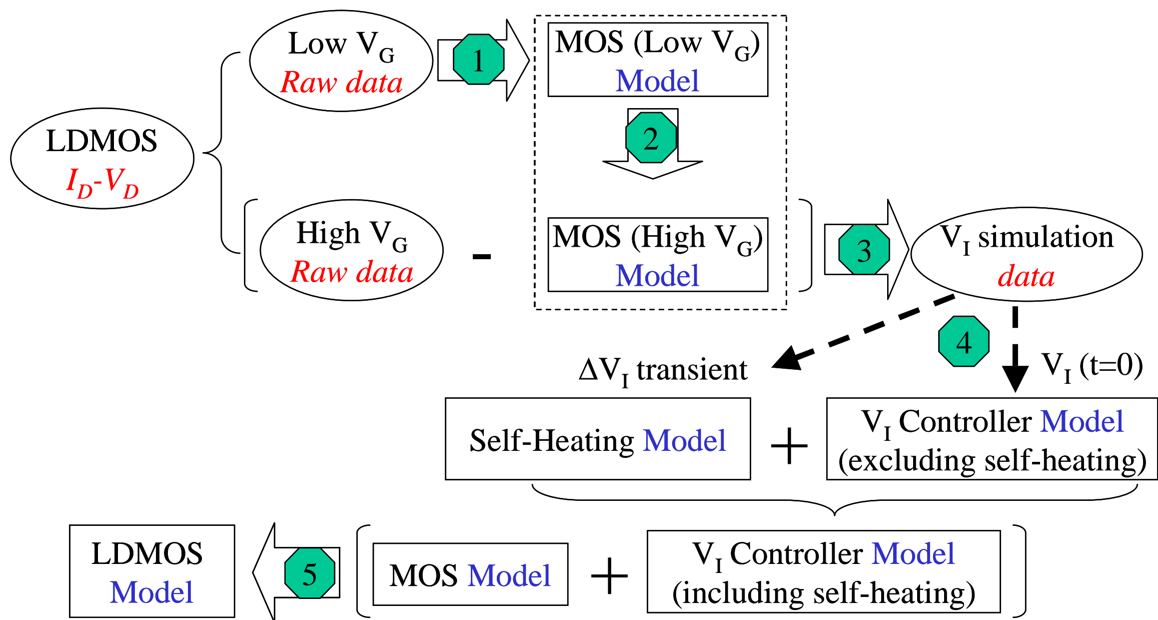


Fig. 5.4 A new modeling method for the MOS element and the V_I controller. Five extraction steps are indicated, including (1, 2) MOS model, (3) V_I simulation step, (4) V_I controller model, and (5) LDMOS macro-model.

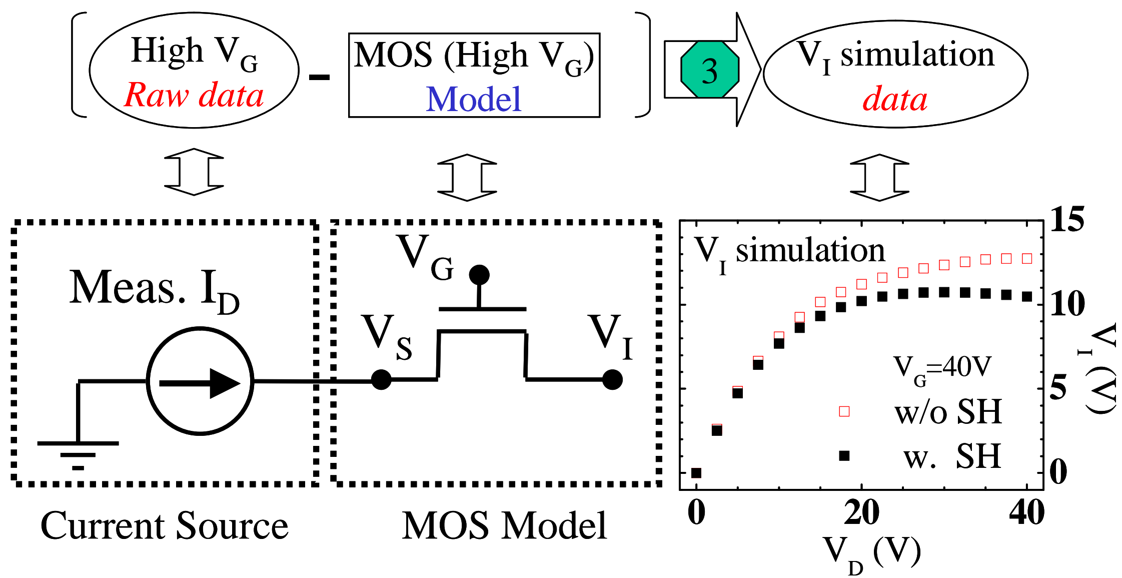


Fig. 5.5 A V_I simulation method in step 3. Each measured I_D can extract a simulated V_I. Typical V_I simulation is shown in the inset under self-heating (w. SH) and non-self-heating (w/o SH) conditions. The MOS model is obtained from step 1 and 2. This method is performed by a HSPICE simulator.

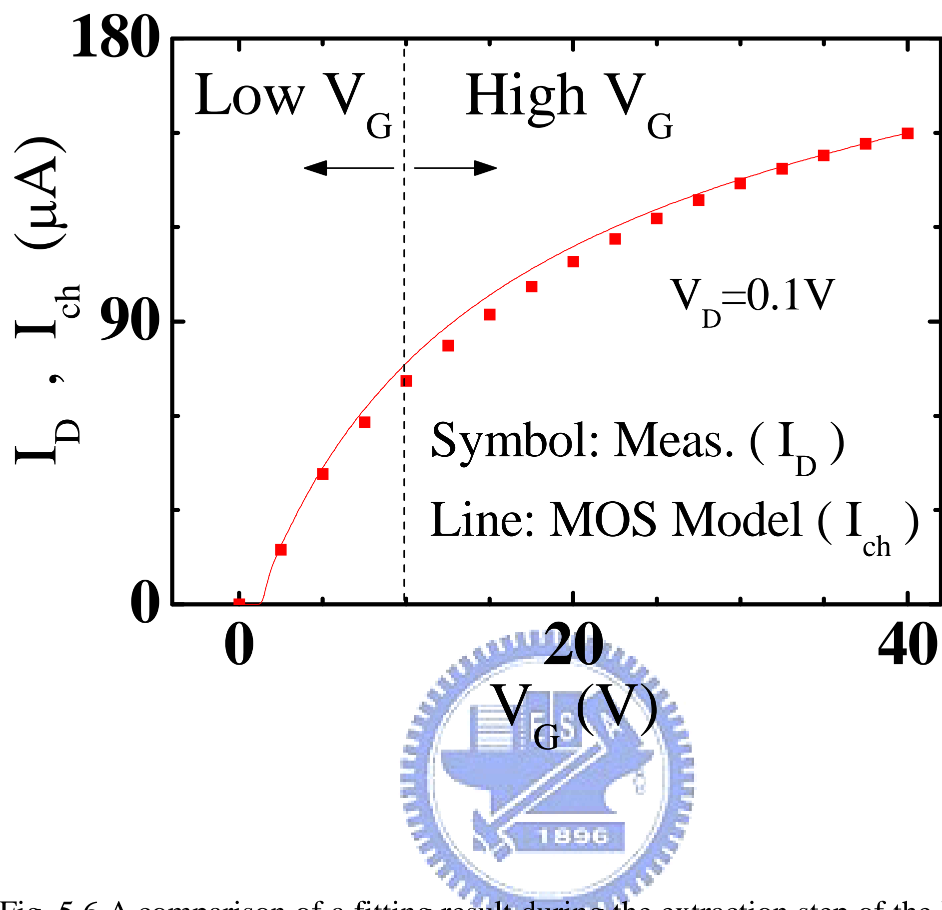
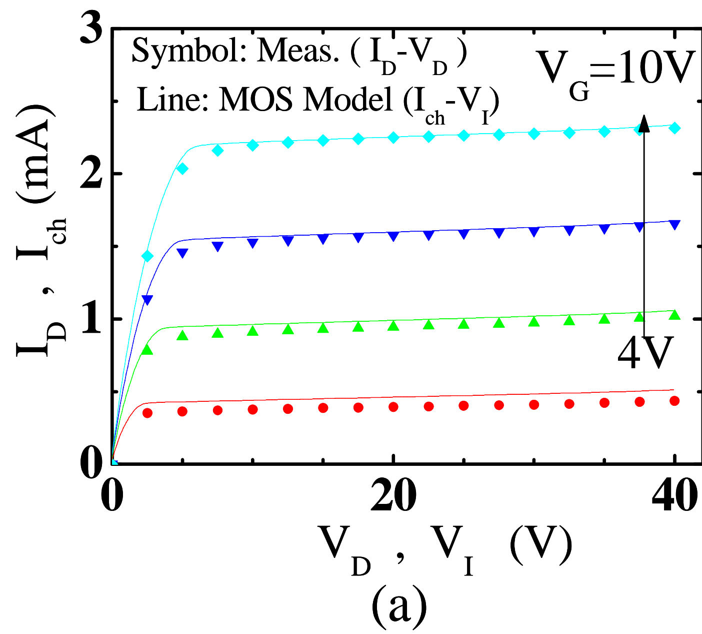
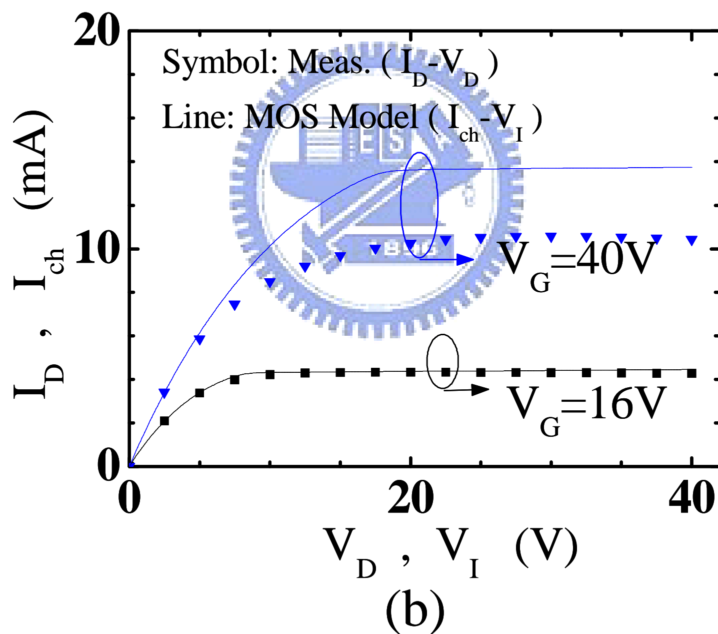


Fig. 5.6 A comparison of a fitting result during the extraction step of the MOS model. The I_D-V_G is measured from a LDMOS. The I_{ch}-V_G is obtained from the MOS model performed by a HSPICE simulator.

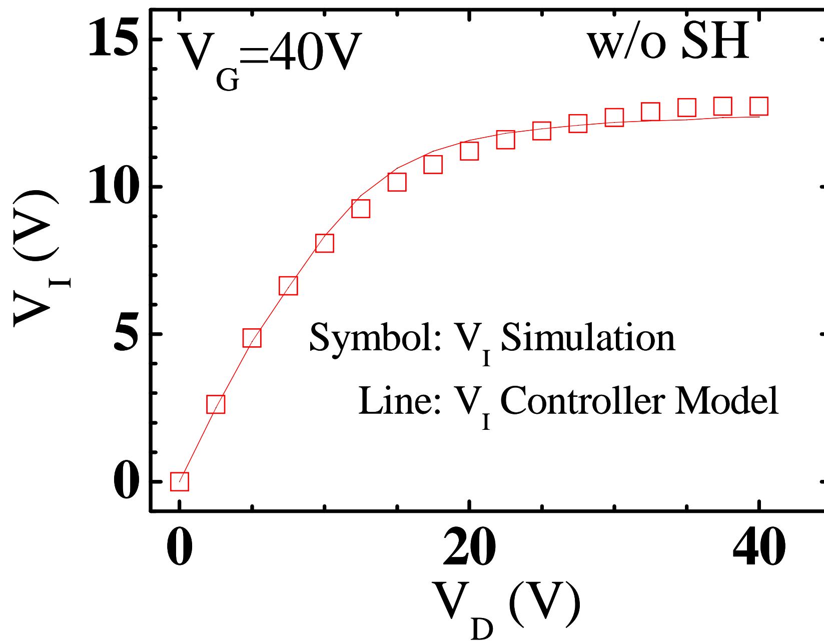


(a)



(b)

Fig. 5.7 A comparison of fitting results during the extraction step of the MOS model. (a) At lower V_G. (b) At higher V_G. The I_D-V_D is measured from a LDMOS. The I_{ch}-V_I is obtained from the MOS model. A match between LDMOS and MOS model means no voltage drop in the drift region and thus V_I=V_D. A mismatch at V_G=40V indicates a voltage drop in the drift region and thus V_I is much smaller than V_D as current flow is the same.



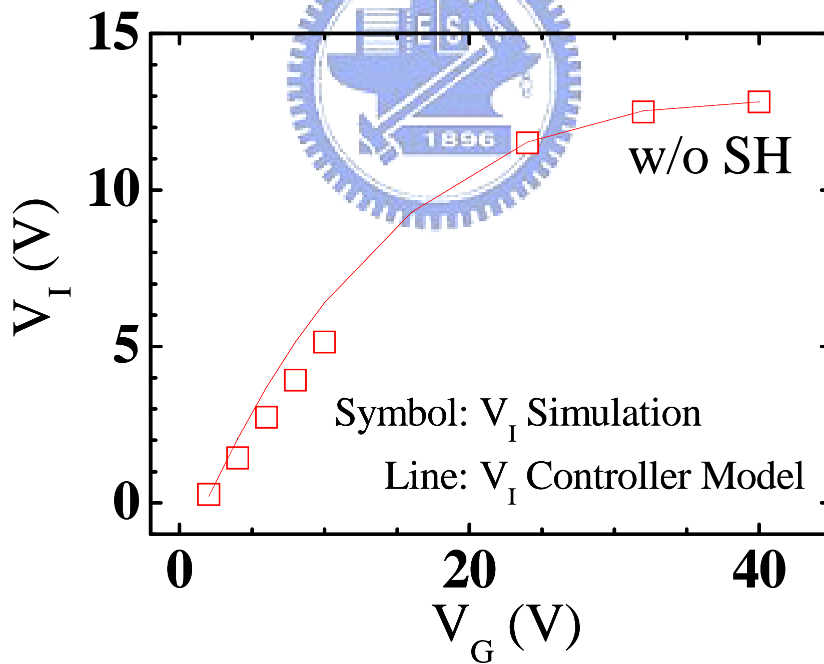


Fig. 5.8 A comparison of V_I controller model in a non-SH condition. Symbol is the V_I obtained from the V_I simulation method. Line represents a simulation result of the V_I controller model. (a) V_I-V_D. (b) V_I-V_G.

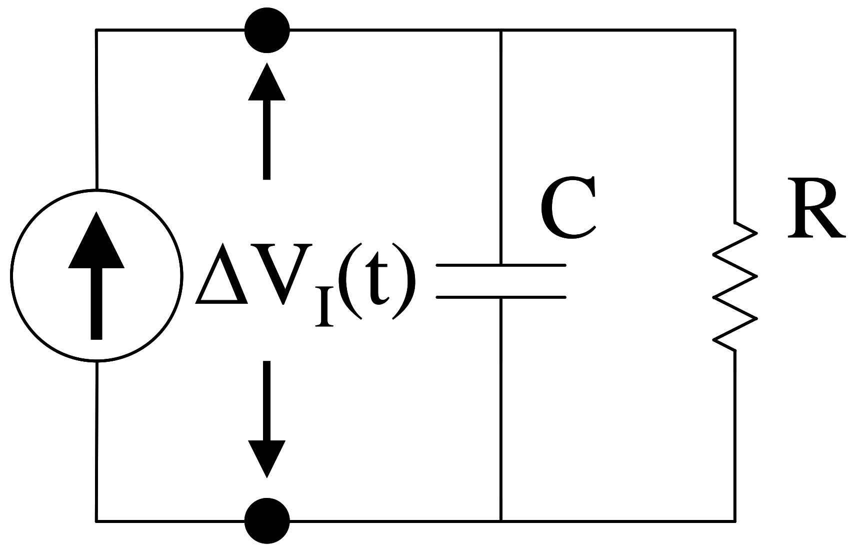


Fig. 5.9 A RC network to describe self-heating induced internal voltage transient ($\Delta V_I(t)$). Three components are used, including a current source, a resistor R, and a capacitor C.

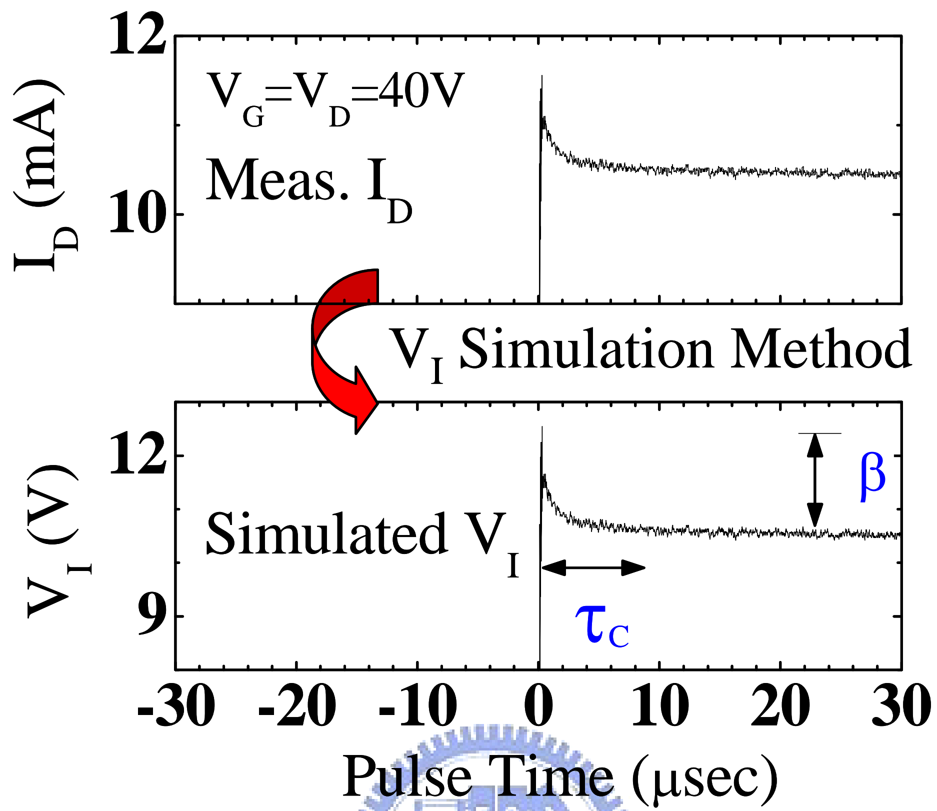


Fig. 5.10 I_D transient and a corresponding V_I simulation performed by the V_I simulation method. β indicates a difference of V_I transient due to self-heating. τ_C represents a time constant of V_I transient.

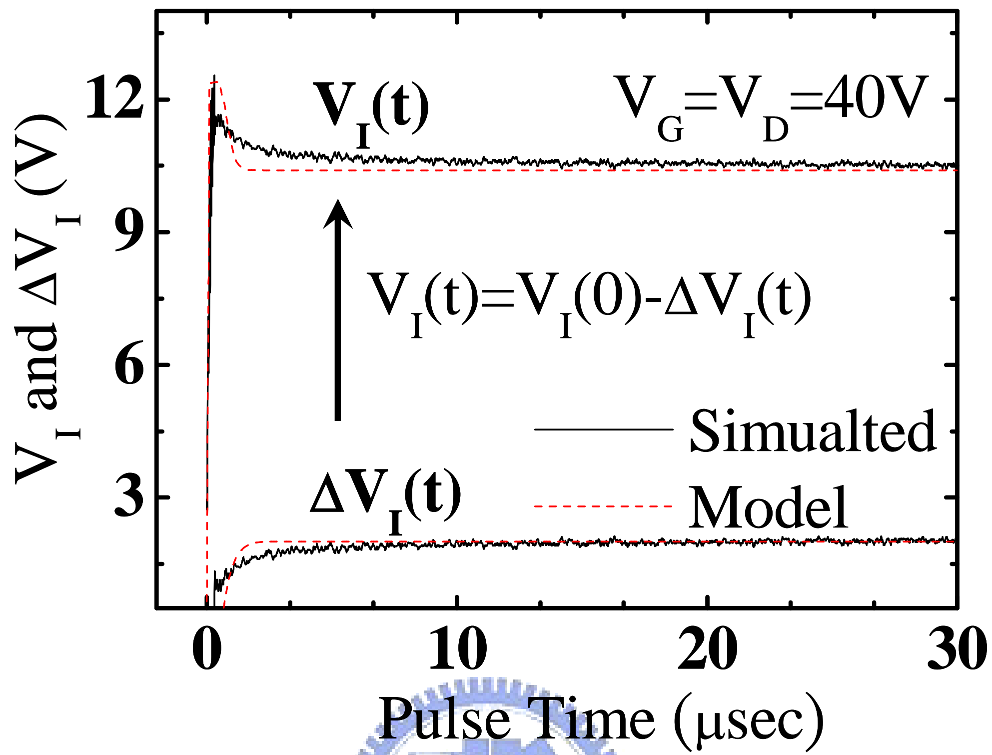


Fig. 5.11 A comparison of V_I transient at V_G/V_D=40V/40V. Line represents the V_I obtained from the V_I simulation method. Dash represents the V_I obtained from the V_I controller model. A fitting result of $\Delta V_I(t)$ is also indicated.

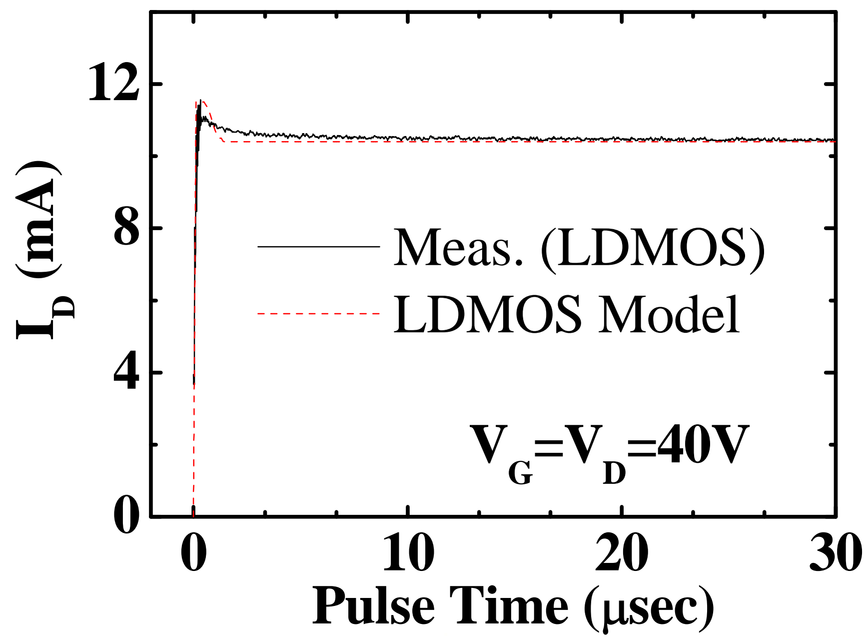
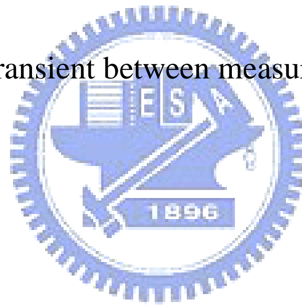
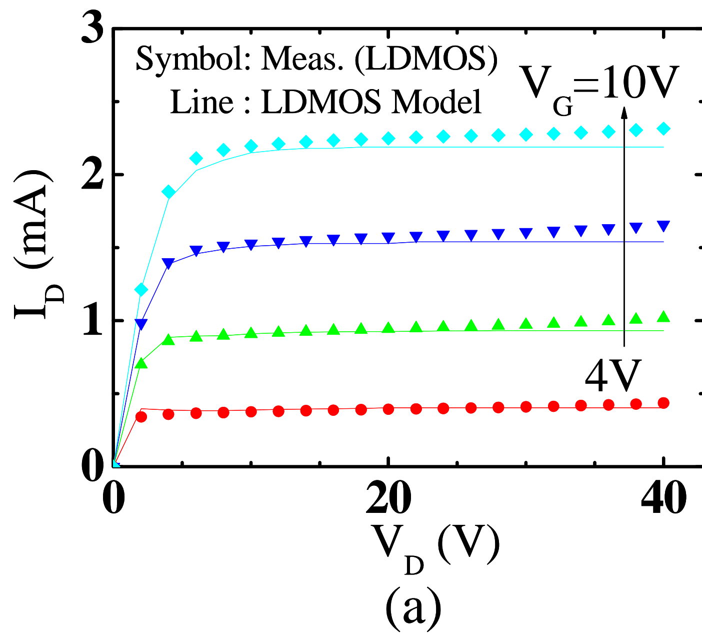
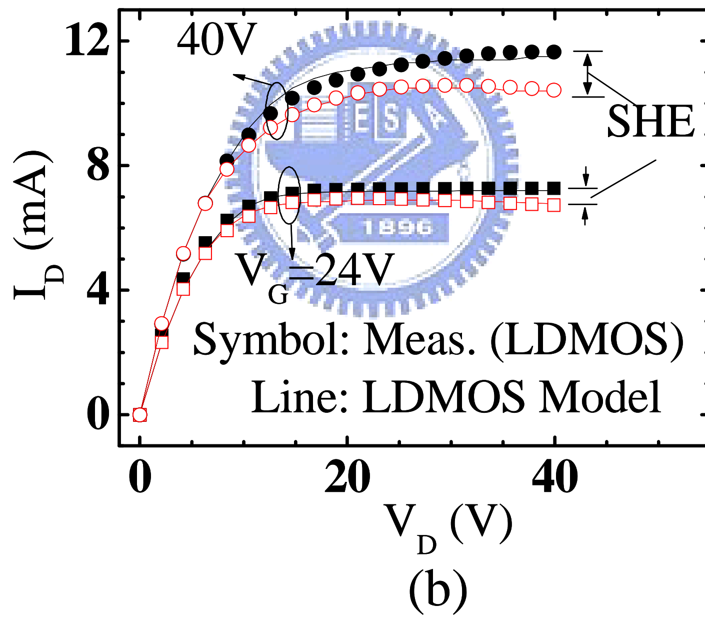


Fig. 5.12 A comparison of I_D transient between measurement and our macro-model.



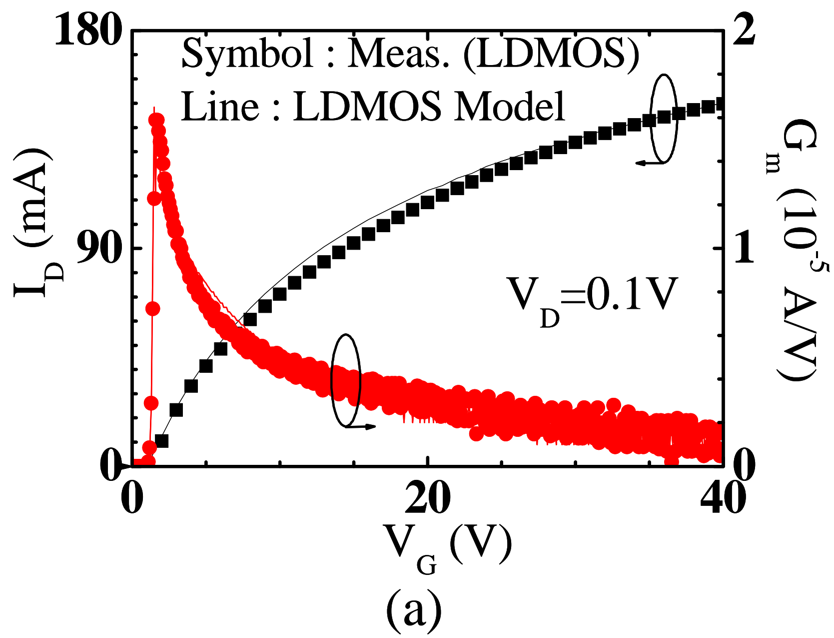


(a)

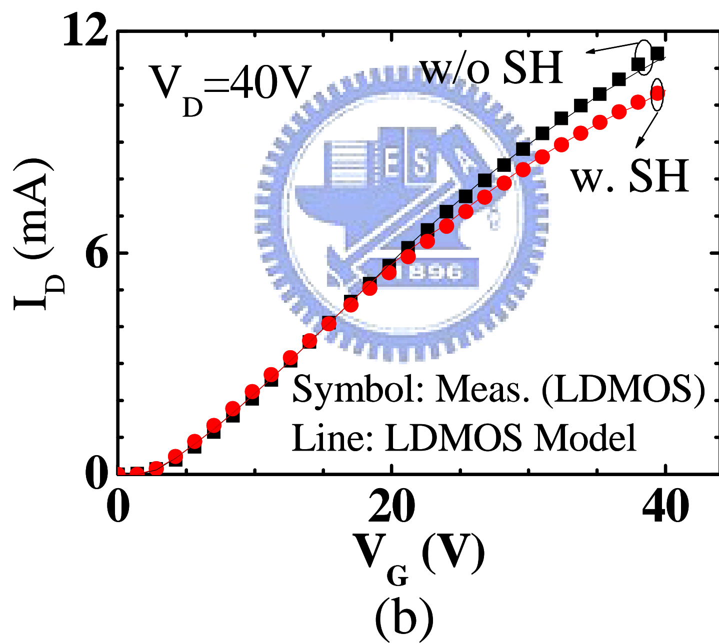


(b)

Fig. 5.13 A comparison of I_D-V_D between measurement and our macro-model. (a) At lower V_G. (b) At higher V_G. The I_D in SH and non-SH conditions are extracted from I_D transient as $t=0^+$ and $t=30\mu s$.



(a)



(b)

Fig. 5.14 A comparison of I_D-V_G between measurement and our macro-model. (a) In the linear region (V_D=0.1V). (b) In the saturation region (V_D=40V).

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this dissertation, we study the LDMOS structure with gate oxide thickness~100nm and filed oxide thickness~500nm. The threshold voltage is ~1.5V and the operating bias are V_G=V_D=40V. It should be noticed that the conclusions we made in this chapter may not be available for the other kinds of the LDMOS structure because of various blocking voltage requirement in high-voltage power device field. Besides, different doping concentration would also lead to different oxide damage mechanisms and may generate a conflicting result due to different operating bias conditions.

In this dissertation, AC/DC hot carrier stress induced oxide reliability issues in a LDMOS have been studied. A new device modeling methodology incorporating self-heating induced V_I change is developed. The major contributions of this work are summarized as follows.

First, a specially-designed metal-contact LDMOS structure is fabricated to investigate both self-heating effect and intrinsic MOS I-V characteristics. With the use of the metal contact LDMOS, a novel self-heating characterization technique involving direct measurement of V_I change is demonstrated. Two thermal-time constants of a V_I transient are measured and explained. This method provides a higher resolution than a conventional I_D method. In addition, the I-V characteristics in a MOS and in a LDMOS are also compared by using the metal-contact LDMOS. The I-V measurement shows that I_D at low-V_G and at high-V_G are major determined by the MOS and drift region, respectively. These features are also presented in the

measurements of the flicker noise behaviors.

Second, a novel three-region CP technique has been developed to characterize hot carrier stress induced oxide degradation in each region of a n-LDMOS. The trap location and property in various stress modes are identified and their impact on device characteristics has been analyzed. A correlation between device degradation, charge pumping, flicker noise, and device simulation results has been established.

Furthermore, transient self-heating effect in AC hot carrier stress in LDMOS has been studied by measuring an internal voltage. A correlation between the AC stress pulse duration and the self-heating time is established. The AC stress at maximum I_G yields the worst hot carrier degradation because of the elimination of self-heating effect.

Finally, a two-component V_I-based LDMOS model including self-heating effect is developed. A sub-circuit model for self-heating induced V_I change is incorporated. A good agreement between model and measurement results for both self-heating and non-self-heating conditions is achieved.

6.2 Future Work

Various kinds of high-voltage device structures depending on its blocking voltage are developed in recent years. Due to high power consumption, self-heating effect and reliability issues would also be important to these device structures. To investigate various DC/AC hot carrier stress modes in these device structures will be helpful to the understanding of high-voltage device reliability, especially for the devices whereas self-heating effect makes a great impact on its transient characteristics. Besides, different doping concentration and device rules (such as, device width, channel length, oxide thickness, and the length of accumulation region)

will impact the conclusions of the reliability studies, and also, leads to different transient considerations. A more complete study of device reliability in various device rules may help us to derive a universal DC reliability model and get more information about AC transient characteristics.

Appendix A

List of MOS Parameters

.model nch_asy nmos (

+level = 49

+lmin = 3e-006

+lmax = 3e-006

+wmin = 2e-005

+wmax = 2e-005

+version = 3.24

+mobmod = 1

+capmod = 3

+nqsmod = 0

+binunit = 1

+stimod = 0

+paramchk= 0

+binflag = 0

+vfbflag = 0

+hspver = 2000.2

+lref = 1e+020

+wref = 1e+020

+tref = 25

+xl = 0

+xw = 0

+lmlt = 1

+wmlt = 1

+ld = 0

+llc = 0

+lwc = 0

+lwlc = 0

+wlc = 0

+wwc = 0

+wwlc = 0

+tox = 1.117e-007

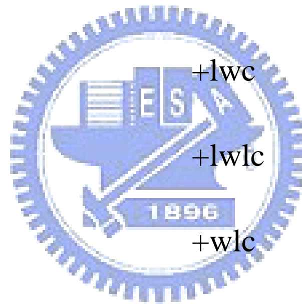
+wint = 0

+lint = 0

+hdif = 5.175e-006

+ldif = 0

+ll = 0



+wl = 0

+lln = 1

+wln = 1

+lw = 0

+ww = 0

+lwn = 1

+wwn = 1

+lwl = 0

+wwl = 0

+cgbo = 1e-013

+xpart = 1

+vth0 = 1.17

+k1 = 0.53

+k2 = -0.0186

+k3 = 80

+k3b = 0

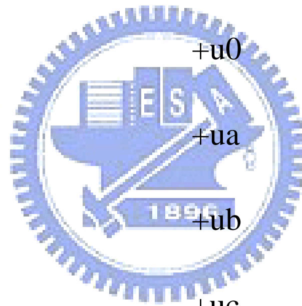
+nlx = 1.74e-007

+dvt0 = 2.2

+dvt1 = 0.53

+dvt2 = -0.032

+dvt0w = 0



+dvt1w = 5300000

+dvt2w = -0.032

+nch = 1.67e+016

+voff = 0.165

+nfactor = 1

+cdsc = 0.00024

+cdscb = 0

+cdscd = 0

+cit = 0

+u0 = 0.07287

+ua = 1.025e-008

+ub = -2.32e-018

+uc = -4.65e-011

+ngate = 0

+xj = 1.7e-006

+w0 = 2.5e-006

+prwg = 0

+prwb = 0

+wr = 1

+rdsw = 0

+a0 = 0.0099

+ags = 0.02

+a1 = 0

+a2 = 1

+b0 = 0

+b1 = 0

+vsat = 99854

+keta = -0.047

+dwg = 0

+dwb = 0

+alpha0 = -2e-012

+beta0 = 30

+pclm = 4.7e-012

+pdiblc1 = 0.0871

+pdiblc2 = 0.0005507

+pdiblcb = -2e-012

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+pvag = 0

+pscbe1 = 4.198e+008

+pscbe2 = 5e-006

+delta = 0.016

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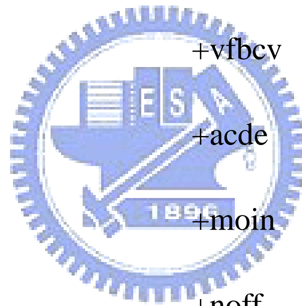

+etab = -0.07

+dsub = 0.56

+elm = 5

+alpha1 = 0

+clc = 1e-007

+cle = 0.6

+ckappa = 0.6

+cgdl = 0

+cgsl = 0

+vfbcv = -1

+acde = 1

+moin = 15

+noff = 1

+voffcv = 0

+kt1 = -0.11

+kt1l = 0

+kt2 = 0.022

+ute = -1.5

+ua1 = 4.31e-009

+ub1 = -7.61e-018

+uc1 = -5.6e-011

```
+prt       = 0
+at        = 33000
+noimod    = 1
+noia      = 1e+020
+noib      = 50000
+noic      = -1.4e-012
+em        = 41000000
+af        = 1
+ef        = 1
+kf        = 0
+gdsnoi    = 1
+rsh       = 0
+js        = 0.0001
+jsw       = 0
+cj        = 0.0005
+mj        = 0.5
+cjsw      = 5e-010
+mjsw      = 0.33
+pb        = 1
+rd        = 0
+rdc       = 0
+rs        = 0
+rsc       = 0
+xti       = 0
+acm       = 12
+calcacm = 0
+nj        = 1
+pbsw      = 0.8
+ptc       = 0
+tt        = 0
+ijth      = 0.1
+tcj       = 0
+tcjsw     = 0
+tcjswg    = 0
+tpb       = 0
+tpbsw     = 0
+tpbswg    = 0
)
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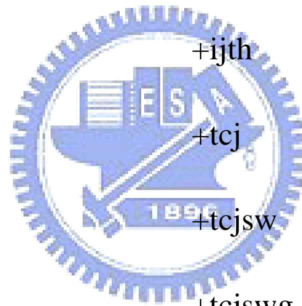


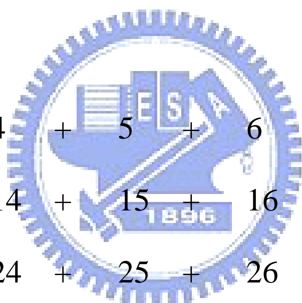
Appendix B

Example of SPICE Input File

```
10   * File :    LDMOS Transient Curve Simulation
20   ************************************
30   .OPTIONS PIVTOL=1E-20
40   .OPTIONS gmin=1E-15    gmindc=1E-15
50   .OPTIONS INGOLD=1
60   .OPTIONS RELTOL = 0.01
70   .OPTIONS ABSTOL = 1.0e-9
80   .OPTIONS VNTOL    = 1.0e-4
90   .OPTIONS LVLTIM = 1
100  .OPTIONS METHOD = GEAR
110  .OPTIONS MAXORD = 2
120  .OPTIONS ITL4      = 100
130
140  *** Simulation Temperature ***
150  .TEMP 25
160  .protect
170  .LIB 'JJ20_1d7_Delta.l' TT_hv_mac
180  .unprotect
190
200  *========== Parameter input=================
210  .param      thita_sat=0.0
220  .param      n='1.78'
230  .param      delta='0.9*min(   max(0,   -0.58333   +   0.20833*V(vd)),   1)   *   max(0,   min(-1.25   +
```

```
                0.0625*V(vg), -0.25 + 0.03125*V(vg)))'
240
250  *========== Parameter vt (Threshold Voltage) =====================
260  .param     vt=1.78
270  .param     thita_md=0.001208
280  .param     Vdsat='((V(vg)-vt)/(1+thita_sat*(V(vg)-vt)))'
290  .param     Visat='((V(vg)-vt)-sqrt((pow(V(vg)-vt,2))-(2*((V(vg)-vt)-0.5*Vdsat)*Vdsat)
                /(1+thita_md*((V(vg)-vt)**(n)))))'
300  .param    Vi='max((Visat-0.5*(Visat-V(vd)-delta + sqrt( pow((Visat-V(vd)-delta),2)+ 4*delta*Visat)))
                - max(V(v1),0),0)'
310
320  *========== Self-heating Ckt ==========================================
330  G1 0 v1 POLY(4) vq 0 0 0 0 0 0 0 0 8.67131E-5   1.63032E-4   0   0   0   -1.38164E-5   0   0
                   0   0   0   0   0   0   0   4.90659E-7   0   0   0   0   0   0   0   0
                   0   0   0   0   0   0   0   0   0   0   0   -5.85845E-9   0   0   0   0
                   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
                   0   0   0   0   0   0   0   0   0   0   0   0
340  R1  0  v1  R='max(1840 * max( 3.3334E-09 , min( 0.64024 + 0.00906*V(vg) , -1.71007 +
                0.10688*V(vg))),1.001e-5)'
350  C1 0 v1 2.03804E-10
360
370  *========== LDMOS Ckt =============================================
380  M1 C vg vs vb nch_asy w=20u l=3u
390  Rd C gd R='max( 1.001E-05, (V(vd)-Vi)/(max(i1(M1),1e-6)) )'
400  Vm1 vd gd 0
410
```

```
420  *========== ID-VD w/o & w/ SHE =======================================
430  VDD   vd   0   pwl(0 0 10u 0 10.001u vdh 40u vdh 40.001u 0)
440  VQ    vd   vq 8
450  VBB   vb   0   0
460  VGG   vg   0   40
470  VSS   vs   0   0
480
490  .tran 0.1u 50u SWEEP DATA=data1
500  .print V(vd) V(C) Par(vdh) I(Vm1)
510  *I(Vm1) = Id
520
530  .DATA data1 vdh
540  +   1   +  2  +   3  +   4  +   5  +   6  +   7  +   8  +   9  +  10
550  +  11   + 12  +  13  +  14  +  15  +  16  +  17  +  18  +  19  +  20
560  +  21   + 22  +  23  +  24  +  25  +  26  +  27  +  28  +  29  +  30
570  +  31   + 32  +  33  +  34  +  35  +  36  +  37  +  38  +  39  +  40
580  .ENDDATA
590
600  .END
```



Appendix C

Derivation of V_{Isat}

The LDMOS current is expressed with two fitting parameters, θ_{md} and n.

$$I_D(V_G,V_D) \approx \frac{W}{L}\cdot C_{ox}\cdot\frac{\mu_0}{1+\theta_{md}\cdot(V_G-V_t)^n}\cdot(V_G-V_t-\frac{V_D}{2})\cdot V_D \qquad \text{(C1)}$$

The MOS model current in the linear region is expressed as:

$$I_{ch}(V_G,V_I) \approx \frac{W}{L}\cdot C_{ox}\cdot\mu_0\cdot(V_G-V_t-\frac{V_I}{2})\cdot V_I \qquad \text{(C2)}$$

Since the LDMOS current is equal to the intrinsic MOS current, equating the currents we get an expression for V_I:

$$V_I(V_G,V_D) \approx (V_G-V_t)-\sqrt{(V_G-V_t)^2-2\cdot\frac{(V_G-V_t-\frac{V_D}{2})\cdot V_D}{1+\theta_{md}\cdot(V_G-V_t)^n}} \qquad \text{(C3)}$$

As the current in the saturation region, V_I is substituted by V_{Isat},

$$V_{Isat}(V_G)=V_I\,|_{V_D=V_{Dsat}}=(V_G-V_t)-\sqrt{(V_G-V_t)^2-2\cdot\frac{(V_G-V_t-\frac{V_{Dsat}}{2})\cdot V_{Dsat}}{1+\theta_{md}\cdot(V_G-V_t)^n}} \qquad \text{(C4)}$$

and $V_{Dsat}(V_G)=\dfrac{(V_G-V_t)}{1+\gamma\cdot(V_G-V_t)}$, with a fitting parameter γ.

So far we have acquired an expression for linear region V_I (equation C3) and an expression for saturation region V_I (equation C4).

References

Chapter 1

[1.1] Satyen Mukherjee, "Power integrated circuits-progress, prospects and challenges," *IEEE Trans. Electron Devices,* vol. 36, pp. 2599-2600, 1989.

[1.2] B. Jayant Baliga, "Trends in power semiconductor devices," *IEEE Trans. Electron Devices,* vol. 43, pp. 1717-1731, 1996.

[1.3] B. Jayant Baliga, *Power Semiconductor Devices*. New York: PWS Pub. Co., 1995.

[1.4] B. Jayant Baliga, "The future of power semiconductor device technology," *Proceedings of the IEEE,* vol. 89, pp. 822-832, 2001.

[1.5] Bruno Murari, "Smart power technology and the evolution from protective umbrella to complete system," in *IEEE Int. Electron Devices Meeting Technical Digest.,* pp. 9-15, 1995.

[1.6] Philip L Hower and Sameer Pendharkar, "Short and long-term safe operating area considerations in LDMOS transistors," in *IEEE Int. Reliability Physics Symposium*, pp. 545-550, 2005.

[1.7] John G. Kassakian and David J. Perreault, "The future of electronics in automobiles," in *IEEE Int. Symposium Power Semiconductor Devices and ICs*, pp. 15-19, 2001.

[1.8] Jongdae Kim, Tae Moon Roh, Sang-Gi Kim, Q. Sang Song, Dae Woo Lee, Jin-Gun Koo, Kyoung-Ik Cho, and Dong Sung Ma, "High-voltage power integrated circuit technology using SOI for driving plasma display panels," *IEEE Trans. Electron Devices,* vol. 48, pp. 1256-1263, 2001.

[1.9] R. Versari, A. Pieracci, S. Manzini, C. Contiero, and B. Ricco, "Hot-carrier reliability in submicrometer LDMOS transistors," in *IEEE Int. Electron*

Devices Meeting Technical Digest., pp. 371-374, 1997.

[1.10] C. Anghel, R. Gillon, and A. M. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Letters,* vol. 25, pp. 141-143, 2004.

[1.11] Y. S. Chung and B. Baird, "Electrical-thermal coupling mechanism on operating limit of LDMOS transistor," in *IEEE Int. Electron Devices Meeting Technical Digest.*, pp. 83-86, 2000.

[1.12] A. Aarts, N. D'Halleweyn, and R. van Langevelde, "A surface-potential-based high-voltage compact LDMOS transistor model," *IEEE Trans. Electron Devices,* vol. 52, pp. 999-1007, 2005.

[1.13] J. M. Roux, X. Federspiel, D. Roy, and P. Abramowitz, "HCI Lifetime Correction Based on Self-Heating Characterization for SOI Technology," *IEEE Trans. on Device and Materials Reliability,* vol. 7, pp. 217-224, 2007.

[1.14] Ying-Keung Leung, Stephen C. Kuehne, Vincent S. K. Huang, Cuong T. Nguyen, Amit K. Paul, James D. Plummer, and S. Simon Wong, "Spatial temperature profiles due to nonuniform self-heating in LDMOS's in thin SOI," *IEEE Electron Device Letters*, vol. 18, pp. 13-15, 1997.

[1.15] Chih-Chang Cheng, J.F. Lin, Tahui Wang, "Impact of Self-Heating Effect on Hot Carrier Degradation in High-Voltage LDMOS," in *IEEE Int. Electron Devices Meeting Technical Digest.*, pp. 881-884, 2007.

[1.16] W. Jin, W. Liu, S. K. H. Fung, P. C. H. Chan, and C. Hu, "SOI thermal impedance extraction methodology and its significance for circuit simulation," *IEEE Trans. Electron Devices,* vol. 48, pp. 730-736, 2001.

Chapter 2

[2.1] B. J. Baliga, "An overview of smart power technology," *IEEE Trans. Electron*

Devices, vol. 38, pp. 1568-1575, 1991.

[2.2] B. Murari, "Smart power technology and the evolution from protective umbrella to complete system," in *IEEE Int. Electron Devices Meeting Technical Digest.*, pp. 9-15, 1995.

[2.3] J. A. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF devices)," in *IEEE Int. Electron Devices Meeting Technical Digest.*, pp. 238-241, 1979.

[2.4] M. N. Darwish and M. A. Shibib, "Lateral MOS-gated power devices-a unified view," *IEEE Trans. Electron Devices,* vol. 38, pp. 1600-1604, 1991.

[2.5] Young S. Chung, "Junction temperature induced thermal snapback breakdown of MOSFET device," *IEEE Electron Device Letters*, vol. 23, pp. 615-617, 2002.

[2.6] J. Evans and G. Amaratunga, "The behavior of very high current density power MOSFETs," *IEEE Trans. Electron Devices,* vol. 44, pp. 1148-1153, 1997.

[2.7] P. Moens, M. Tack, R. Degraeve, and G. Groeseneken, "A novel hot-hole injection degradation model for lateral nDMOS transistors," in *IEEE Int. Electron Devices Meeting Technical Digest.*, pp. 1-4, 2001.

[2.8] C. Anghel, "High Voltage Devices for Standard MOS Technologies – Characterization and Modeling," Lausanne: Swiss Federal Institute of Technology, 2004.

[2.9] J. M. Roux, X. Federspiel, D. Roy, and P. Abramowitz, "HCI Lifetime Correction Based on Self-Heating Characterization for SOI Technology," *IEEE Trans. on Device and Materials Reliability,* vol. 7, pp. 217-224, 2007.

[2.10] Chih-Chang Cheng, J.F. Lin, Tahui Wang, "Impact of Self-Heating Effect on Hot Carrier Degradation in High-Voltage LDMOS," in *IEEE Int. Electron Devices Meeting Technical Digest.*, pp. 881-884, 2007.

[2.11] E. Arnold, H. Pein, and S. P. Herko, "Comparison of self-heating effects in bulk-silicon and SOI high-voltage devices," in *IEEE Int. Electron Devices Meeting Technical Digest.*, pp. 813-816, 1994.

[2.12] R. J. T. Bunyan, M. J. Uren, J. C. Alderman, and W. Eccleston, "Use of noise thermometry to study the effects of self-heating in submicrometer SOI MOSFETs," *IEEE Electron Device Letters,* vol. 13, pp. 279-281, 1992.

[2.13] K. A. Jenkins and J. Y. C. Sun, "Measurement of I-V curves of silicon-on-insulator (SOI) MOSFET's without self-heating," *IEEE Electron Device Letters,* vol. 16, pp. 145-147, 1995.

[2.14] O. Le Neel and M. Haond, "Electrical transient study of negative resistance in SOI MOS transistors," *Electronics Letters,* vol. 26, pp. 73-74, 1990.

[2.15] R. H. Tu, C. Wann, J. C. King, P. K. Ko, and H. Chenming, "An AC conductance technique for measuring self-heating in SOI MOSFET's," *IEEE Electron Device Letters,* vol. 16, pp. 67-69, 1995.

[2.16] R. Van Langevelde, S. Blieck, and L. K. J. Vandamme, "Noise in DMOS transistors in a BICMOS-technology," *IEEE Trans. Electron Devices,* vol. 43, pp. 1243-1250, 1996.

Chapter 3

[3.1] E. M. S. Narayanan, G. A. J. Amaratunga, W. I. Milne, J. I. Humphrey, and Q. Huang, "Analysis of CMOS-compatible lateral insulated base transistors," *IEEE Trans. Electron Devices,* vol. 38, pp. 1624-1632, 1991.

[3.2] B. J. Baliga, "An overview of smart power technology," *IEEE Trans. Electron Devices,* vol. 38, pp. 1568-1575, 1991.

[3.3] C. Contiero, P. Galbiati, M. Palmieri, G. Ricotti, and R. Stella, "Smart power approaches VLSI complexity," in *IEEE Int. Symposium Power Semiconductor*

Devices and ICs, pp. 11-16, 1998.

[3.4] P. L. Hower and S. Pendharkar, "Short and long-term safe operating area considerations in LDMOS transistors," in *IEEE Int. Reliability Physics Symposium*, pp. 545-550, 2005.

[3.5] J. G. Kassakian and D. J. Perreault, "The future of electronics in automobiles," in *IEEE Int. Symposium Power Semiconductor Devices and ICs*, pp. 15-19, 2001.

[3.6] K. Jongdae, R. Tae Moon, K. Sang-Gi, Q. S. Song, L. Dae Woo, K. Jin-Gun, I. K. C. Kyong, and M. Dong Sung, "High-voltage power integrated circuit technology using SOI for driving plasma display panels," *IEEE Trans. Electron Devices,* vol. 48, pp. 1256-1263, 2001.

[3.7] P. Moens, G. Van den bosch, and G. Groeseneken, "Hot-carrier degradation phenomena in lateral and vertical DMOS transistors," *IEEE Trans. Electron Devices,* vol. 51, pp. 623-628, 2004.

[3.8] P. Moens, M. Tack, R. Degraeve, and G. Groeseneken, "A novel hot-hole injection degradation model for lateral nDMOS transistors," in *IEEE Int. Electron Devices Meeting Technical Digest.*, pp.1-4, 2001.

[3.9] N. Hefyene, C. Anghel, R. Gillon, and A. M. Ionescu, "Hot carrier degradation of lateral DMOS transistor capacitance and reliability issues," in *IEEE Int. Reliability Physics Symposium*, pp. 551-554, 2005.

[3.10] Jone F. Chen, Kuo-Ming Wu, Kaung-Wan Lin, Yan-Kuin Su, and S . L. Hsu, "Hot-carrier reliability in submicrometer 40V LDMOS transistors with thick gate oxide," in *IEEE Int. Reliability Physics Symposium*, pp. 560-564, 2005.

[3.11] C.C. Cheng, K.C. Tu, Tahui Wang, T.H. Hsieh, J.T. Tzeng, Y.C. Jong, R.S. Liou, Sam C. Pan, and S.L. Hsu, "Investigation of Hot Carrier Degradation Modes in LDMOS by using a Novel Three-Region Charge Pumping

Technique," in *IEEE Int. Reliability Physics Symposium*, pp. 334-337, 2006.

[3.12] A. L. McWhorter, "1/f noise and germanium surface properties," Semiconductor Surface Physics. Philadelphia : Univ. of Pennsylvania Press, pp.207, 1957

[3.13] F. N. Hooge, "1/f Noise Source," *IEEE Trans. Electron Devices,* vol.41, pp.19261935, 1994

[3.14] B. Doyle, M. Bourcerie, J. C. Marchetaux, and A. Boudou, "Interface state creation and charge trapping in the medium-to-high gate voltage range ($V_d/2 \geq V_g \geq V_d$) during hot-carrier stressing of n-MOS transistors," *IEEE Trans. Electron Devices,* vol. 37, pp. 744-754, 1990.

[3.15] J.-S. Goo, H. Shin, H. Hwang, D.-G. Kang, and D.-H. Ju, "Physical Analysis for Saturation Behavior of Hot-Carrier Degradation in Lightly Doped Drain N-Channel Metal-Oxide-Semiconductor Field Effect Transistors," *Jpn. J. Appl. Phys.,* vol. 33, pp. 606-611, 1994.

[3.16] R. a. Dreesen, K. a. Croes, J. a. Manca, W. a. De Ceuninck, L. a. De Schepper, A. b. Pergoot, and G. Groeseneken, "A new degradation model and lifetime extrapolation technique for lightly doped drain nMOSFETs under hot-carrier degradation " *Microelectronics Reliability,* vol. 41, pp. 437-443, 2001.

Chapter 4

[4.1] P. Moens, M. Tack, R. Degraeve, and G. Groeseneken, "A novel hot-hole injection degradation model for lateral nDMOS transistors," in *IEEE Int. Electron Devices Meeting Technical Digest.,* pp. 1-4, 2001.

[4.2] V. O'Donovan, S. Whiston, A. Deignan, and C. N. Chleirigh, "Hot carrier reliability of lateral DMOS transistors," in *IEEE Int. Reliability Physics Symposium*, pp. 174-179, 2000.

[4.3] D. Brisbin, A. Strachan, and P. Chaparala, "Hot carrier reliability of N-LDMOS transistor arrays for power BiCMOS applications," in *IEEE Int. Reliability Physics Symposium*, pp. 105-110, 2002.

[4.4] C.C. Cheng, K.C. Tu, Tahui Wang, T.H. Hsieh, J.T. Tzeng, Y.C. Jong, R.S. Liou, Sam C. Pan, and S.L. Hsu, "Physics and Characterization of Various Hot-Carrier Degradation Modes in LDMOS by Using a Three-Region Charge-Pumping Technique," *IEEE Trans. on Device and Materials Reliability,* vol. 6, pp. 358-363, 2006.

[4.5] P. Moens, G. Van den bosch, and M. Tack, "Hole Trapping and de-Trapping Effects in LDMOS Devices under Dynamic Stress," in *IEEE Int. Electron Devices Meeting Technical Digest.,* pp. 1-4, 2006.

[4.6] C.C. Cheng, K.C. Tu, Tahui Wang, T.H. Hsieh, J.T. Tzeng, Y.C. Jong, R.S. Liou, Sam C. Pan, and S.L. Hsu, "Investigation of Hot Carrier Degradation Modes in LDMOS by using a Novel Three-Region Charge Pumping Technique," in *IEEE Int. Reliability Physics Symposium*, pp. 334-337, 2006.

[4.7] E. Arnold, H. Pein, and S. P. Herko, "Comparison of self-heating effects in bulk-silicon and SOI high-voltage devices," in *IEEE Int. Electron Devices Meeting Technical Digest.,* pp. 813-816, 1994.

[4.8] G. M. Dolny, G. E. Nostrand, and K. E. Hill, "The effect of temperature on lateral DMOS transistors in a power IC technology," *IEEE Trans. Electron Devices,* vol. 39, pp. 990-995, 1992.

[4.9] R. Versari, A. Pieracci, S. Manzini, C. Contiero, and B. Ricco, "Hot-carrier reliability in submicrometer LDMOS transistors," in *IEEE Int. Electron Devices Meeting Technical Digest.,* pp. 371-374, 1997.

[4.10] O. Le Neel and M. Haond, "Electrical transient study of negative resistance in SOI MOS transistors," *Electronics Letters,* vol. 26, pp. 73-74, 1990.

Chapter 5

[5.1] C. Anghel, "High Voltage Devices for Standard MOS Technologies – Characterization and Modeling," Lausanne: Swiss Federal Institute of Technology, 2004.

[5.2] M. Y. Hong and D. A. Antoniadis, "Theoretical analysis and modeling of submicron channel length DMOS transistors," *IEEE Trans. Electron Devices,* vol. 42, pp. 1614-1622, 1995.

[5.3] Y. S. Kim, J. G. Fossum, and R. K. Williams, "New physical insights and models for high-voltage LDMOST IC CAD," *IEEE Trans. Electron Devices,* vol. 38, pp. 1641-1649, 1991.

[5.4] C. Yeonbae and D. E. Burk, "A physically based DMOS transistor model implemented in SPICE for advanced power IC TCAD," in *IEEE Int. Symposium Power Semiconductor Devices and ICs*, pp. 340-345, 1995.

[5.5] C. M. Liu, F. C. Shone, and J. B. Kuo, "A closed-form physical back-gate-bias dependent quasi-saturation model for SOI lateral DMOS devices with self-heating for circuit simulation," in *IEEE Int. Symposium Power Semiconductor Devices and ICs*, pp. 321-324, 1995.

[5.6] A. Aarts, N. D'Halleweyn, and R. van Langevelde, "A surface-potential-based high-voltage compact LDMOS transistor model," *IEEE Trans. Electron Devices,* vol. 52, pp. 999-1007, 2005.

[5.7] N. V. D'Halleweyn, L. F. Tiemeijer, J. Benson, and W. Redman-White, "Charge model for SOI LDMOST with lateral doping gradient," in *IEEE Int. Symposium Power Semiconductor Devices and ICs*, pp. 291-294, 2001.

[5.8] J. Jaejune, T. Amborg, Y. Zhiping, and R. W. Dutton, "Circuit model for power LDMOS including quasi-saturation," in *IEEE Int. Conf. on Simulation of*

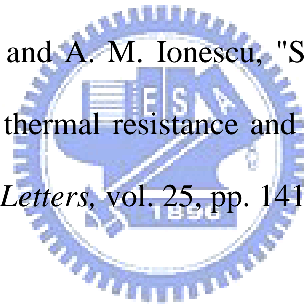
Semiconductor Processes and Devices, pp. 15-18, 1999.

[5.9] N. Hefyene, E. Vestiel, B. Bakeroot, C. Anghel, S. Frere, A. M. Ionescu, and R. Gillon, "Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HV-MOSFET," in *IEEE Int. Conf. on Simulation of Semiconductor Processes and Devices,* pp. 203-206, 2002.

[5.10] E. C. Griffith, J. A. Power, S. C. Kelly, P. Elebert, S. Whiston, D. Bain, and M. O'Neill, "Characterization and modeling of LDMOS transistors on a 0.6μm CMOS technology," in *IEEE Int. Conf. on Microelectronic Test Structures,* pp. 175-180, 2000.

[5.11] W. Liu, *MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4*. New York: John Wiley & Sons, 2001.

[5.12] C. Anghel, R. Gillon, and A. M. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Letters,* vol. 25, pp. 141-143, 2004.



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Investigation of Transient Hot Carrier Stress and Device Modeling Issues in High-Voltage Lateral Diffused Metal-Oxide-Semiconductor Field Effect Transistors

Publication List

(A) Journal Papers

3.
A 類國際性
期刊論文

(1) Chih-Chang Cheng, J. F. Lin, Tahui Wang, T.H. Hsieh, J.T. Tzeng, Y.C. Jong, R.S. Liou, Samuel C. Pan, and S.L. Hsu "Physics and Characterization of Various Hot Carrier Degradation Modes in LDMOS by Using a Three-Region Charge Pumping Technique," *IEEE Trans. on Device and Materials Reliability*, pp.358-363, 2006

(2) J. W. Wu, J. W. You, H. C. Ma, Chih-Chang Cheng, C. F. Hsu, C. S. Chang, G. W. Huang, Tahui Wang, "Excess low-frequency noise in ultrathin oxide n-MOSFETs arising from valence-band electron tunneling," *IEEE Trans. Elect., Dev.*, pp. 2061-2066, 2005

(3) J.W. Wu, J.W. You, H. C. Ma, Chih-Chang Cheng, C.S. Chang, G.W. Huang, and Tahui Wang, "Valence-Band Tunneling Induced Low Frequency Noise in Ultra-Thin Oxides (15A) n-type metal oxide semiconductor field effect transistors," *Applied Phys. Lett.,* pp.5076-5077, 2004

(4) J.W. Wu, J.C. Guo, K.L. Chiu, Chih-Chang Cheng, W.Y. Lien, G.W. Huang and Tahui Wang, "Pocket Implantation Effect on Drain Current Flicker Noise in Analog n-MOSFET Devices" *IEEE Trans. Elect., Dev.*, pp. 1262-1266, 2004

(B)Conference Papers

2.
A 類國際
會議論文

(5) Chih-Chang Cheng, J.F. Lin, Tahui Wang, T.H. Hsieh, J.T. Tzeng, Y.C. Jong, R.S. Liou, Samuel C. Pan, and S.L. Hsu, "Impact of Self-Heating Effect on Hot Carrier Degradation in High-Voltage LDMOS," ***IEEE International Electron Device Meeting (IEDM)***, pp.881-884 Washington DC, U.S.A., 2007

(6) Chih-Chang Cheng, K.C. Tu, Tahui Wang, T.H. Hsieh, J.T. Tzeng, Y.C. Jong, R.S. Liou, Sam C. Pan, and S.L. Hsu, "Investigation of Hot Carrier Degradation Modes in LDMOS by Usinga Novel Three-Region Charge Pumping Technique," *Int. Reliability Phys. Symp. (IRPS)*, pp.334-337, San Jose, U.S.A., 2006

(7) J.W. Wu, H.C. Ma, J.W. You, Chih-Chang Cheng, G.W. Huang, C.S. Chang, and Tahui Wang, "Low Frequency Noise Degradation in Ultra-Thin Oxide (15A) Analog n-MOSFETs Resulting from Valence-Band Tunneling," *Int. Reliability Phys. Symp. (IRPS)***,** pp. 260-264, San Jose, U.S.A., 2005

(8) Chih-Chang Cheng, J. W. Wu, C. C. Lee, J. H. Shao and, Tahui Wang, "Hot Carrier Degradation in LDMOS Power Transistors," *Int. Phys. and Failure Analysis of Integrated Circuit (IPFA),* pp.283-286, Hsinchu, Taiwan, 2004

(9) J.W. Wu, J.W. You, H. C. Ma, Chih-Chang Cheng, G.W. Huang, C.S. Chang, and Tahui Wang, "Valence-Band Tunneling Induced Low Frequency Noise in Ultra-Thin Oxides (15A) Analog n-MOSETs," *Int. Electron Devices and Materials Symposium (IEDMS),* pp.273-276, Hsinchu, Taiwan, 2004

(10) J. W. Wu, Chih-Chang Cheng, and Tahui Wang, " The Comparison of hot Carrier Reliability in N-LDMOS and P-LDMOS Transistors, " *International Electronic Devices and Materials Symposiums* (*EDMS*), pp.523-526, Taipei, Taiwan, 2002

著作總點數：　5　(依新法記點)