國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

具有超薄 N_2O 退火氮化物閘極介電層與矽鍺通道之金氧半場效電晶體可靠度及通道厚度效應研究

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中華民國九十三年六月

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摘　要

在本論文中，我們針對具有矽鍺($Si_{0.85}Ge_{0.15}$)通道與超薄 N_2O 退火氮化物閘極介電層(等效氧化層厚度約 3.1 奈米)之金氧半場效電晶體進行可靠度與通道厚度效應的研究。根據經驗公式，在矽基板與矽鍺通道接面處的價帶能階偏移量大約是 0.1 電子伏特，而閘極電流的傳導機制則主要是等效位能障約 1.8 電子伏特的 FN 穿遂機制。經過定電壓壓迫(CVS)及定電流壓迫(CCS)後，我們發現對 N_2O 退火之矽化氮(SiN)閘極介電層並沒有造成明顯的損害，不過卻觀察到與電壓極性相關之電應力導致的漏電流(SILC)，此現象可藉由陽極電洞注入(AHI)模型加以解釋。隨後我們進行熱載子(hot-carrier)壓迫以及負電壓溫度產生不穩定性(NBTI)的電性量測，藉以評估矽鍺通道之 p 型金氧半場效電晶體的可靠度。在負電壓溫度產生不穩定性的壓迫下，我們已顯示電子缺陷(electron trapping)主導元件效能的破壞程

度，而在熱載子壓迫的情況下則是由壓迫產生的界面狀態造成主要損害。由於電荷拉推電流(charge pumping current)的結果顯示 V_g=V_d 之壓迫產生最多的界面狀態，因此對於具有矽鍺通道及 N_2O 退火矽化氮閘極介電層之 p 型金氧半場效電晶體的可靠度問題，我們認為 V_g=V_d 之壓迫情況導致元件效能最嚴重的損傷。另一方面，矽緩衝層的不完美晶格引起高密度錯排(dislocation)，並且降低驅動電流、轉導(transconductance)及等效載子遷移率，因此我們提出無矽緩衝層的矽鍺通道金氧半場效電晶體具有較佳的元件特性。此外，搭配 5 奈米和 15 奈米厚度的矽鍺通道金氧半場效電晶體，除了次臨界電壓振動(swing)低到 67 mV/A，與 30 奈米矽鍺通道的元件相比，還具有較高的驅動電流、較低的界面狀態密度、較低的漏電密度、較高的轉導和較佳的等效載子遷移率。最後，對於未來次 100 奈米的技術領域，我們證明搭配矽鍺通道及 N_2O 退火矽化氮閘極介電層之金氧半場效電晶體將具有高度的潛力。

A Study of Reliability and Channel Thickness Effect on $Si_{0.85}Ge_{0.15}$ MOSFETs with Ultra-Thin N_2O-annealed Nitride Gate Dielectric

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ABSTRACT

We have investigated the reliability and the channel thickness effect of MOSFETs with $Si_{0.85}Ge_{0.15}$ channel and ultra-thin (EOT=3.1 nm) N_2O-annealed SiN gate dielectric. The offset of valence band is about 0.1 eV. The FN tunneling dominates the conduction mechanism of the gate current with an effective barrier height of 1.8 eV. In addition, the results of CVS and CCS stressing show the insignificant degradation of the N_2O-annealed SiN gate dielectric, and the polarity dependent SILC has been observed and explained by anode hole injection (AHI) model. The hot-carrier (HC) stressing and negative bias temperature instability (NBTI) are performed to evaluate the reliability of the SiGe channel pMOSFETs. We have

demonstrated that electron trapping dominates the device degradation for the NBTI stressing and the interface state generation is dominant mechanism for the HC stressing. The results of the charge pumping current have shown the highest interface state density are generated after the device being stressed at V_g=V_d. Therefore, the stressing condition of V_g=V_d has been considered as the worst case for evaluating the reliability of the SiGe channel pMOSFET with N_2O-annealed SiN gate dielectric. Because of the high dislocation density induced by the imperfect crystalline Si buffer layer, the driving current, transconductance, and effective mobility are degraded. Therefore, the SiGe channel MOSFETs without a Si buffer layer is proposed to have better device performance. Moreover, the MOSFETs with 5 and 15 nm SiGe channel have been shown smaller subthreshold swing of 67 mV/A, higher driving current, lower interface state density, lower leakage current, larger transconductance, and greater effective mobility as compared with the 30 nm SiGe channel devices. Finally, the MOSFETs with thin SiGe channel and N_2O-annealed SiN gate dielectric have been demonstrated their potential for the sub-100 nm CMOSFET technology.

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Figure Captions

Chapter 1
Introduction

1-1 Background

So far, increasing the inversion gate capacitance, enhancing the carrier transport, enhancing the immunity of shorter channel effect, and reducing parasitic capacitances and parasitic resistances are the most useful techniques to improve the device performance of the metal oxide semiconductor field effect transistors (MOSFETs) [1]. For example, the high-k gate dielectric can be used to induce a larger inversion charge density at the same gate bias because of its high dielectric constant, and the silicidation of source/drain can decrease the parasitic capacitance and resistance. Although, many methods have been proposed to achieve these purposes, it still needs new materials and new structures to realize the device performance enhancement.

According to the issues mentioned above, silicon germanium (SiGe) is introduced to be the channel of MOSFETs for improving carrier transport because of its higher bulk carrier mobility than the conventional Si channel devices. Moreover, the SiGe layer can be selectively deposited on the Si substrate by a chemical vapor deposition (CVD) system, and the process of device fabrication can be simplified. The offset of valence band between SiGe

and the Si will lead to the quantum confinement effect of holes [2]. Thus the hole mobility can be obviously increased for the p-type MOSFETs (pMOSFETs) with SiGe channel [3]-[5]. Besides, hole mobility will also be improved simultaneously because the compressive strain of SiGe layer is formed when SiGe is deposited on the Si substrate [6]-[10]. Furthermore, the low thermal budget process can be performed because of the high dopant solubility of SiGe which lowers the dopant activation temperature.

Unfortunately, the lattice mismatch raises with increasing the contents of Ge and it results in the increase of the dislocation density and impurity scattering in SiGe films [2]. On the other hand, if the gate oxide is formed by oxidizing the SiGe layer with conventional oxidation process, Ge atoms will be precipitated at the interface between SiGe and oxide, and meanwhile the quality of oxide will also be deteriorated [11]. Therefore, the using of Si capping layer and the gate oxide grown by deposition will be the most appropriated methods for fabricating devices with SiGe channel. However, the high temperature oxidation process of Si capping layer will probably induce the relaxation of the SiGe under layer. Additionally, because the temperature of depositing a gate oxide is lower than that of the oxidation, the thermal budget of the process can be lowered to prevent the relaxation of the strained SiGe layer. Recently, silicon nitride (SiN) has been reported as the possible alternative of gate dielectrics for MOSFETs with SiGe channel [11][12]. SiN not only has a larger dielectric constant but also can suppress the boron penetration from p^+ poly-Si gate into Si substrate. Moreover, because the Si-N bonds at the SiN/Si interface have higher bonding energy than

that of the Si-H bonds, SiN has been shown better hot-carrier (HC) hardness than that of silicon dioxide (SiO_2) [16]. However, SiN film will induce oxide fixed charges to cause the threshold voltage shift, and increase interface state density to degrade the device performance. Therefore, N_2O-annealing has been proposed to improve the quality of SiN gate dielectric and the SiN/Si interface [13]-[15].

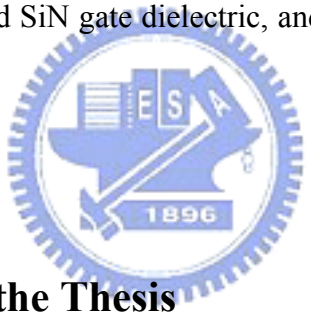
1-2 Motivation

Considering the issues have mentioned above, we have fabricated MOSFET devices with SiGe channel and SiN gate dielectric. The SiN is formed by low pressure chemical vapor deposition (LPCVD) system and annealed in N_2O ambience to improve the film quality. Although many studies have been proposed on the N_2O-annealed SiN film [14], SiN film as the gate dielectric of SiGe channel MOSFETs still needs extensive investigation. Therefore, we will further study the electrical characteristics and reliability of the devices.

For conventional Si channel devices, the hot-carrier effect results in a serious reliability issue [16]. For example, the oxide trap charges and the interface state generation are caused by hot-carrier stressing [17]-[20], and then the threshold voltage and the drive capability of device will be degraded. In addition, the bias temperature instability (BTI) effect has been reported as another issue dominating the device reliability [21]-[23]. When device is stressed at high voltage and high temperature, the interface state generation dominates the degradation

of device performance because of the electrochemical reaction between the inversion charges and the interface states [24]-[26]. Therefore, we will compare the characteristics of devices after hot-carrier and BTI stressing, and discuss the mechanism of device degradation.

Finally, the relaxation is not only easily occurred when the strained SiGe deposited on the Si substrate is annealed at high temperatures [31][32], but also closely related to the strain energy in the SiGe layer. Because the amount of strain energy increases with increasing the thickness of SiGe, the thickness of SiGe channel should play an important role on the device characteristics. Thus, we will investigate the channel thickness effect on SiGe channel CMOSFETs with N_2O-annealed SiN gate dielectric, and realize the optimization condition of fabricating devices.



1-3 Organization of the Thesis

This thesis can be divided into five parts. The background of SiGe MOSFETs and the motivation of our study are introduced in Chapter 1. In Chapter 2, we describe the experimental procedures and the device structure of the SiGe channel MOSFETs with N_2O-annealed SiN gate dielectric. By measuring the electrical characteristics and the reliability of hot-carrier and BTI stressing, the mechanism of device degradation is discussed in Chapter 3. Moreover, we investigate the SiGe channel thickness effect on the fundamental characteristics of pMOSFETs and nMOSFETs. Finally, Chapter 5 presents the conclusions of

our discussion and proposes some suggestions for the potentials of SiGe channel CMOSFETs with N_2O-annealed SiN gate dielectric in the future applications.

Chapter 2
Experiment

2-1 Device Fabrication Process

The $Si_{0.85}Ge_{0.15}$ channel MOSFETs with N_2O-annealed ultra-thin SiN gate dielectric were fabricated on 6-inch (100) orientated Si substrate for our experiments. The briefly device process flow was shown in Fig. 2-1. The standard local oxidation of silicon (LOCOS) process was performed to isolate the devices on the wafer. Subsequently, $Si_{0.85}Ge_{0.15}$ epitaxy layers with various thicknesses of 5, 15, 30, and 50 nm were deposited selectively on the Si substrate by ultra-high vacuum chemical deposition system (UHVCVD) at 550 ºC. The SiGe layers were in-situ doped by phosphorus and arsenic for n-type channel and p-type channel, respectively. After being cleaned by RCA process, the ultra-thin (3 nm) SiN gate dielectrics were deposited by low pressure chemical vapor deposition (LPCVD) with dichlorosilane (DCS, SiH_2Cl_2) and NH_3 at 780 ºC, and followed immediately by rapid thermal annealing (RTA) at 800 ºC and 900 ºC for 30 seconds in N_2O ambience. The undoped 150 nm poly-Si deposition were performed by LPCVD with silane (SiH_4) at 620 ºC and patterned by using lithography and etching process as the gate electrode. Then, the self-aligned source/drain extension was implanted with As by a dosage of 1×10^{14} cm^{-2} at 10 keV and with BF_2 by a

dosage of 1×10^{14} cm^{-2} at 10 keV for nMOSFETs and pMOSFETs, respectively. An oxide spacer was formed by etching isotropically the LPCVD low temperature TEOS oxide (LTO), and the self-aligned gate and source/drain implantation were performed by implanting As with a dosage of 5×10^{15} cm^{-2} at 20 keV and BF_2 with a dosage of 5×10^{15} cm^{-2} at 20 keV for nMOSFETs and pMOSFETs, respectively. After the substrate contact being defined and implanted to improve the body contact, the dopant activation by RTA at 900 ºC in N_2 ambience for 30 seconds was carried out. Finally, the wafers were passivated with 500 nm LTO oxide followed by a standard back-end-of-line (BEOL) contact and metallization processes, and the devices were annealed in a furnace by the forming gas at 450 ºC for 30 minutes before the electrical characteristics measurements. Figure 2-2 demonstrates the schematic device structure of SiGe channel MOSFETs with N_2O-annealed SiN gate dielectric. Moreover, the conventional Si channel MOSFETs with the same gate dielectric and device structure were also fabricated for comparing the electrical characteristics with that of SiGe channel device counterparts.

2-2 Electrical Characteristics Measurements

The high frequency (100 kHz) capacitance-voltage (*C–V*) characteristics of the capacitors were measured by using an Agilent 4284 LCR meter, and the EOT of gate dielectrics was determined from the strong accumulation capacitance. The current-voltage

(I–V) characteristics were measured by using Keithley 4200 semiconductor characterization system. From the I_d–V_g curves, the main parameters of device, such as threshold voltage (V_t) and subthreshold swing (S), were obtained. In addition, the density of interface state (N_{it}) for MOSFETs was determined by the charge pumping current (I_{CP}) which was measured by the charge pumping technique. Therefore, the reliability of devices was evaluated by investigating the degradation of the device performance when they were stressed under the hot-carrier (HC) stressing and the bias-temperature instability (BTI) stressing. The channel thickness effect on the SiGe channel MOSFETs was also be studied by comparing the electrical characteristics of devices with different SiGe channel thickness.

Chapter 3
Reliability of 50 nm $Si_{0.85}Ge_{0.15}$ pMOSCAP and pMOSFET

3-1 pMOSCAP

When SiGe is deposited directly on the Si substrate, it causes an offset of valence band (ΔE_v) between SiGe and Si. Then the hole mobility is increased by the quantum confinement effect for the pMOSFETs [2]. Figure 3-1 shows the band diagram of the devices with $Si_{0.85}Ge_{0.15}$ channel under the inversion condition. From the empirical equation of $\Delta E_v \sim 0.74x$, where x is the Ge mole fraction [2], the valence band offset is about 0.1 eV for $Si_{0.85}Ge_{0.15}$/Si channel structure.

The electrical characteristics of the pMOSCAP with 50 nm $Si_{0.85}Ge_{0.15}$ channel and N_2O-annealed SiN gate dielectric is shown in Fig. 3-2. From the high frequency (100 kHz) *C–V* curves as shown in Fig. 3-2(a), the equivalent oxide thickness (EOT) of 3.1 nm is obtained by the accumulation capacitance, and no hysteresis behavior is observed. In addition, the inversion capacitance is slightly lower than the accumulation capacitance, which is mainly caused by the poly depletion effect. A low leakage current is also demonstrated in Fig. 3-2(b). When the current density is fitted by the Fowler-Nordheim (FN) tunneling, the well-fitted

straight line means that the conduction mechanism is suggested to be the FN tunneling with an effective barrier height of 1.8 eV, as plotted in Fig. 3-3.

After being stressed by a constant voltage stress (CVS) at V_g = –5 V and –5.3 V up to 3000 seconds, the *C–V* characteristics shown in Fig. 3-4 do not be changed and show no hysteresis occurred. Similar results are also illustrated in Fig. 3-5 for a constant current stress (CCS) at J_g = –0.01 mA/cm^2 and –0.02 mA/cm^2 up to 3000 seconds. According to the results of CVS and CCS, therefore, it indicates that there is almost no oxide charges generated in the N_2O-annealed SiN gate dielectric during stressing. Moreover, the *I–V* curves after being stressed by CVS and CCS are illustrated in Fig. 3-6. We find a slight increase of current density with increasing stressing time at the negative gate bias region because of the stress induced leakage current (SILC), but there is no obvious increment at the positive gate bias region. Therefore, we speculate that this polarity dependent SILC should be caused by the gate dielectric damaged by high energy holes which are generated by the anode hole injection (AHI) model in the substrate [29][30]. The schematic diagram of AHI model is demonstrated in Fig. 3-7. When electrons tunneling through the gate dielectric into the substrate by FN tunneling, the energetic electrons are produced and the impact ionization is occurred to generate the electron-hole pairs at the substrate. Then the ionized holes gain sufficient energy and are injected back to the gate dielectric, and the traps are produced near the gate electrode by the interaction between the hot holes and the gate dielectric. Therefore, even though the leakage current is enhanced by the trap-assisted-tunneling when the negative gate voltage is

applied, it is insignificant at the positive gate bias.

3-2 pMOSFET

Figure 3-8 shows the I_d–V_g and I_d–V_d characteristics of SiGe channel pMOSFET with N_2O-annealed SiN gate dielectric. The threshold voltage (V_t) of –1.869 V, the subthreshold swing (S) of 124.8 mV/A, and the peak transconductance ($G_{m,p}$) of 0.11 mS are obtained from the I_d–V_g curve in the subthreshold region. Moreover, the effects of drain induced barrier lowering (DIBL) and gate induced drain leakage (GIDL) are not found in Fig. 3-8(a). Figure 3-8(b) also displays good I_d–V_d curves with various gate overdrive (V_g–V_t) voltages from 0 to –2 V.

To study the reliability of our devices, we stress the devices at different hot-carrier (HC) and negative BTI (NBTI) bias conditions. For the HC stressing, the devices are applied the voltages at V_g=V_d (I_g is maximum) and V_g=2V_d/3 (I_{sub} is maximum) with grounded source and substrate at room temperature. While we stress the devices under V_g = –4.5 V with grounded source/drain and substrate at room temperature (RT) and 100 ºC for the effect of NBTI. Fig. 3-9 demonstrates the degradations of drain current and transconductance under these four stressing conditions. Obviously, the results of HC stressing show significant degradation of I_d (ΔI_d) and G_m (ΔG_m), and the device has largest ΔI_d and ΔG_m when it is stressed at V_g=V_d. On the other hand, the variations of threshold voltages (ΔV_t) with the stress time are illustrated in

Fig. 3-10. Interestingly, all values of ΔV_t have positive shifts for all stressing conditions. It indicates that, therefore, electrons trapped in the gate dielectric are occurred during the stressing process. In addition, Fig. 3-10 shows that ΔV_t follows the power law in the form $\Delta V_t = At^n$. According to the previous report [28], a small value of n (n<0.2) means that the degradation of V_t is dominated by the electron trapping in the oxide; while for a larger value of n (n>0.2), the mechanism of causing ΔV_t should be the interface state generation. However, the insignificant V_t variation for the sample being stressed by NBTI at 100 ºC can be explained by the self-recovery effect of high temperature BTI degradation [27]. Then we investigate the interface state generation by the charge pumping (CP) measurement. As shown in Fig. 3-11(a), the charge pumping currents (I_{CP}) are increased after the devices are stressed, and it confirms the generation of excess interface states. Again, the slightly positive shifts of I_{CP} shown in Fig. 3-11(b) indicate the electron trapping in the gate dielectric. Figure 3-12 compares the results of interface state generation (ΔN_{it}) for stressing conditions of V_g=V_d, V_g=2V_d/3, and room temperature NBTI. We can clearly see that the greatest ΔN_{it} has been shown for the V_g=V_d HC stressing case. Consequently, it further indicates that generating interface states when devices are stressed under HC stressing plays the most important role in device reliability.

The lifetimes of devices extracted from the HC degradation of G_m and I_d are plotted in Fig. 3-13. Obviously, the stressing condition of V_g=V_d shows the worse case of lifetime of G_m degradation because of the higher interface state generation than that of the V_g=2V_d/3

stressing counterparts. However, the lifetime extracted from the ΔI_d displays a reverse trend. It can be explained as following. Figure 3-14 shows the V_g=V_d hot carrier degradations of I_d and G_m under different stressing biases verse the stress time. We can see that ΔI_d and ΔG_m are increased with the stressing voltages. However, the degradation of G_m becomes saturated when device is stressed for a long time. It reveals that the interface state generation induced G_m degradation may not dominate the degradation of I_d for long time stressing. Meanwhile, the variation of ΔV_t with the stress time as shown in Fig 3-15 demonstrates that when device is stressed under higher stressing biases, the threshold voltage becomes smaller at the beginning of stressing process and then is increased sequentially toward negatively. It results in that electrons are trapped in the gate dielectric at the beginning stress time to improve the threshold voltage, but the hole trapping is occurred to further degrade the V_t with the following stress time. Therefore, because the improvement of V_t will enhance the drain current and the degradation of V_t will decrease I_d performance, the slope of lifetime extraction by I_d degradation in Fig. 3-14(b) will be raised. Consequently, the extrapolating lifetime of V_g=V_d hot-carrier stressing determined by the degradation of I_d is better than that of V_g=$2V_d/3$ hot-carrier stressing.

CHAPTER 4

Channel Thickness Effect on $Si_{0.85}Ge_{0.15}$ MOSFETs

4-1 SiGe MOSFETs with and without Si buffer layer

To investigate the effect of Si buffer under the SiGe epitaxy layer on the device characteristics, the 15 nm $Si_{0.85}Ge_{0.15}$ channel MOSFETs with and without 10 nm Si buffer layer are fabricated. The capacitance-voltage (C–V) curves of pMOSFETs and nMOSFETs are illustrated in Fig. 4-1. The equivalent oxide thickness (EOT) of the N_2O-annealed SiN gate dielectric obtained by the accumulation capacitance is almost the same 3.1 nm for all devices. The difference between the accumulation and inversion capacitance is due to the poly depletion effect. In addition, the apparent shifts of flat band voltage (V_{fb}) for both the p- and n- MOSCAPs with Si channel (control device) are caused by a higher substrate doping concentration than that of the SiGe channel devices.

Figure 4-2 displays the I_d–V_g characteristics of all samples. We can see that the Si buffer layer does not affect the threshold voltages (V_t) and the subthreshold swings (S) because the V_t and S have been shown to be almost the same for SiGe pMOSFETs and nMOSFETs. Again, the larger values of V_t and S for the control Si channel devices than that of the SiGe channel counterparts are also due to their higher doping concentrations in the substrate. Moreover, the

excellent low values of subthreshold swings of around 67 mV/A for all SiGe MOSFETs reveal a good interface between the N_2O-annealed SiN gate dielectric and the $Si_{0.85}Ge_{0.15}$ channel. Figure 4-3 shows the drain currents of the MOSFETs. Obviously, for both pMOSFETs and nMOSFETs, the SiGe devices show higher driving currents than that of the conventional Si devices, and the SiGe devices without Si buffer layer show slightly better performance than that of devices with a buffer layer. These results are corresponding to the trends of transconductance as shown in Fig. 4-4. For pMOSFETs and nMOSFETs, the peaks of the normalized transconductance ($G_m \times T_{ox}$) at the low $V_g - V_t$ biases display the same results as the $I_d - V_d$ curves in Fig. 4-3. The enhancement of $G_m \times T_{ox}$ is probably due to the reduction of interface states and carrier scattering effects. Additionally, the effective hole ($\mu_{eff,p}$) and electron ($\mu_{eff,n}$) mobility for all MOSFETs are shown in Fig. 4-5. Although, the hole mobility is improved by the compressive strain and quantum confinement in the $Si_{0.85}Ge_{0.15}$ channel for pMOSFETs, the device without a buffer layer still shows higher $\mu_{eff,p}$ than that of the device with a buffer layer. For nMOSFETs, the device without a buffer layer also shows superior effective electron mobility than that of the counterparts. Meanwhile, the improvement of the low field effective mobility for SiGe devices is mainly because of the decrease of the impurity scattering by their lower channel doping concentration. By measuring the charge pumping currents, the interface state density (N_{it}) can be extracted as plotted in the Fig. 4-6. We can see that the values of N_{it} for all devices are almost the same for their good interface between the gate dielectric and the channel. On the other hand, the subthreshold swings are also shown in

Fig. 4-6 as comparing with the interface state density. As mentioned above, the values of swing for SiGe channel MOSFETs are lower than that for the conventional MOSFETs, and it is due to the lighter doping concentration in the SiGe channel.

Considering the same results of V_t, S, and N_{it} for the SiGe MOSFETs with and without Si buffer layer, the enhancement of the driving current, transconductance, and the effective mobility for the device without a buffer layer should be contributed by other factors. Figure 4-7 demonstrates the characteristics of GIDL for p- and n- MOSFETs. Interestingly, we find that the leakage currents of SiGe devices with Si buffer layer are more than one order of magnitude larger than that of other devices for both pMOSFETs and nMOSFETs. Besides, junction leakage currents also show the same trends as the results of GIDL shown in Fig. 4-8. Therefore, we speculate that the increase of leakage current is caused by the excess dislocations in the SiGe channel because of the imperfect crystalline induced by the Si buffer layer. Then we believe that the SiGe channel MOSFETs will demonstrate superior device performance when the selective SiGe epitaxy layer is deposited directly on the Si substrate without a Si buffer layer to form the channel of device.

4-2 MOSFETs with 5, 15 and 30 nm SiGe Channel

The pMOSFETs and nMOSFETs with various SiGe channel thickness of 5, 15, and 30 nm without a Si buffer layer are fabricated to investigate the channel thickness effect on the

device characteristics. The gate dielectric is formed by the N_2O-annealed LPCVD SiN. Figure 4-9 shows the *C–V* characteristics of the SiGe devices with different channel thickness. The smaller values of EOT (3.1 nm) are obtained for the devices with thinner SiGe channel of 5 and 15 nm. The 30 nm SiGe channel devices, however, have been shown to have larger EOT. It is speculated that the faster depositing rate of SiN layer is induced by the high surface strain energy of a thick SiGe channel. Again, the poly depletion effect is also observed in these *C–V* curves. In addition, the distortion of *C–V* curves of the devices with 30 nm SiGe channel indicates more interface states should exist in the oxide/SiGe interface, and a slightly V_{fb} shift is probably due to a slightly heavier doping concentration in the channel.

Figure 4-10 and Fig. 4-11 show the characteristics of I_d–V_g and I_d–V_d, respectively. The threshold voltages of the devices with thinner SiGe channel are lower than that of the 30 nm SiGe channel devices because of their smaller values of EOT and lighter channel doping concentration. Moreover, the lowest subthreshold swing of 67 mV/A can also be realized by the 5 and 15 nm SiGe channel devices, and it corresponds to the lower interface state density. The 5 and 15 nm SiGe channel devices performing better driving capability than that of the 30 nm counterparts are demonstrated as comparing their I_d–V_d curves in Fig. 4-11. Then, all of the interface state density (N_{it}) and the subthreshold swing for all devices are shown in Fig. 4-12. Obviously, for both pMOSFETs and nMOSFETs, the 30 nm SiGe channel devices having higher N_{it} and *S* are demonstrated. Furthermore, the higher dislocation density of the 30 nm SiGe channel can be verified by measuring the characteristics of the GIDL and the

junction leakage currents for pMOSFETs and nMOSFETs as shown in Fig 4-13 and Fig. 4-14, respectively. Both the currents of GIDL and junction leakage of the devices with 30 nm SiGe channel show more than one order of magnitude than that of the thinner channel thickness counterparts. The increase of the dislocation density is speculated to be caused by increasing the strain energy with the SiGe channel thickness. These results indicate that a poor interface and channel layer quality can be obtained when the thickness of SiGe channel is increased up to 30 nm.

The normalized transconductance ($G_m \times T_{ox}$) characteristics for p- and n- MOSFETs are shown in Fig. 4-15. The G_m characteristics are almost identical for 5 and 15 nm SiGe channel devices and they are higher than that of the MOSFETs with 30 nm channel thickness at the low gate biases because of the lower interface state and dislocation density. At high gate voltages, however, the transconductance of the 30 nm SiGe channel pMOSFET is enhanced because holes still flow through in the SiGe channel under high gate bias. But for the pMOSFETs with 5 and 15 nm SiGe channel, holes will mainly transport through the under Si channel when the larger gate voltages are applied. On the other hand, as shown in Fig. 4-15(b), the G_m of the nMOSFET with 30 nm SiGe channel is degraded in the whole field region because of the insignificant improvement of the effective electron mobility in SiGe channel. The effective mobility of the SiGe MOSFETs with 5, 15 and 30 nm channel thickness is extracted in Fig. 4-16. Consequently, the effective hole mobility is improved by the compressive strain and the quantum confinement in the SiGe channel and shows the similar

trend of the channel thickness effect as the transconductance does, which is shown in Fig. 4-15. However, the effective electron mobility of the 30 nm channel nMOSFET is severely degraded because of the high density of interface state and dislocation as discussed previously.

Chapter 5
Conclusion

In this work, we have successfully fabricated MOSFETs with selectively epitaxial $Si_{0.85}Ge_{0.15}$ channel and ultra-thin (EOT=3.1 nm) N_2O-annealed LPCVD SiN gate dielectric. The offset of valence band between $Si_{0.85}Ge_{0.15}$ and Si substrate is about 0.1 eV from the empirical equation. The conduction mechanism of gate current is fitted well by FN tunneling with an effective barrier height of 1.8 eV. The *C–V* curves showing insignificant variation on V_{fb} and hysteresis when the capacitors being stressed under CVS and CCS up to 3000 seconds indicate the good quality of the N_2O-annealed SiN gate dielectric has been formed. On the other hand, polarity dependent SILC has been observed and can be explained by anode hole injection (AHI) model. Subsequently, we have studied the effect of hot-carrier (HC) stressing and negative bias temperature instability (NBTI) on the SiGe channel pMOSFETs. From the power law of threshold voltage degradation versus the stress time, we have demonstrated that electron trapping dominates the degradation of device performance under the NBTI stressing, while interface state generation is predominant under the HC stressing conditions. However, the device stressed under NBTI at 100 ºC has been shown the lightest ΔV_t and ΔG_m because of the self-recovery effect. In addition, electron trapping has been observed during the initial HC stressing under the condition of $V_g=V_d$. According to the results of charge pumping

measurement, the highest interface state density is generated after the device being stressed at V_g=V_d and we have regarded the stressing condition of V_g=V_d as the worst case for evaluating the reliability of the SiGe channel pMOSFET with N_2O-annealed SiN gate dielectric.

The results of V_t, S, and N_{it} for the SiGe MOSFETs with and without the Si buffer layer are indicated that the enhancement of the driving current, transconductance, and the effective mobility for the device without a buffer layer should be contributed by the lower dislocation density and higher carrier mobility than the counterparts. The dislocations in the SiGe channel, however, are due to the imperfect crystalline introduced in the Si buffer layer. Therefore, the SiGe MOSFETs have been demonstrated with superior device performance when the SiGe channel is deposited directly on the Si substrate without a Si buffer layer. Subsequently, we have also investigated the channel thickness effect on the SiGe pMOSFETs and nMOSFETs with various SiGe channel thickness of 5, 15, and 30 nm. The excellent subthreshold swings of 67 mV/A and high driving currents have been obtained for the MOSFETs with 5 and 15 nm SiGe channel. Moreover, the density of interface state and dislocation have been shown even lower than that of the 30 nm SiGe channel device. Although the 30 nm SiGe channel devices have been demonstrated having G_m and μ_{eff} degradation for both p- and n- MOSFETs at low fields, higher effective hole mobility of pMOSFET is caused by holes still flowing through in the SiGe channel at high gate biases. Because the effective electron mobility can be improved insignificantly by the compressive strained SiGe channel, $\mu_{eff,n}$ of the 30 nm SiGe channel nMOSFET is lower than that of the 5 and 15 nm SiGe channel devices in the

whole voltage field. Finally, we have proposed the MOSFETs with thin SiGe channel (5 and 15 nm) and N_2O-annealed SiN gate dielectric and shown their potential for advanced sub-100 nm CMOSFET technology.

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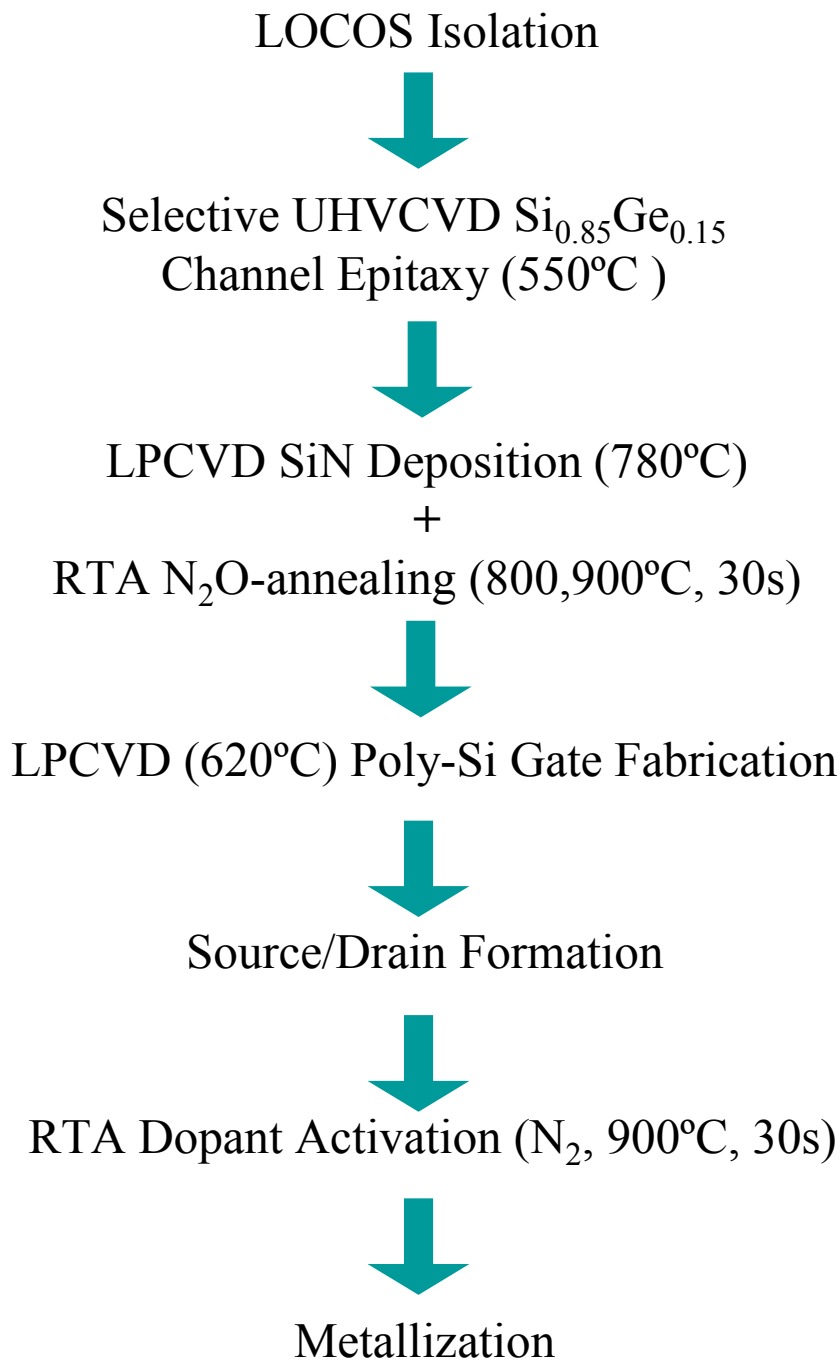


Fig. 2-1 Device process flow.

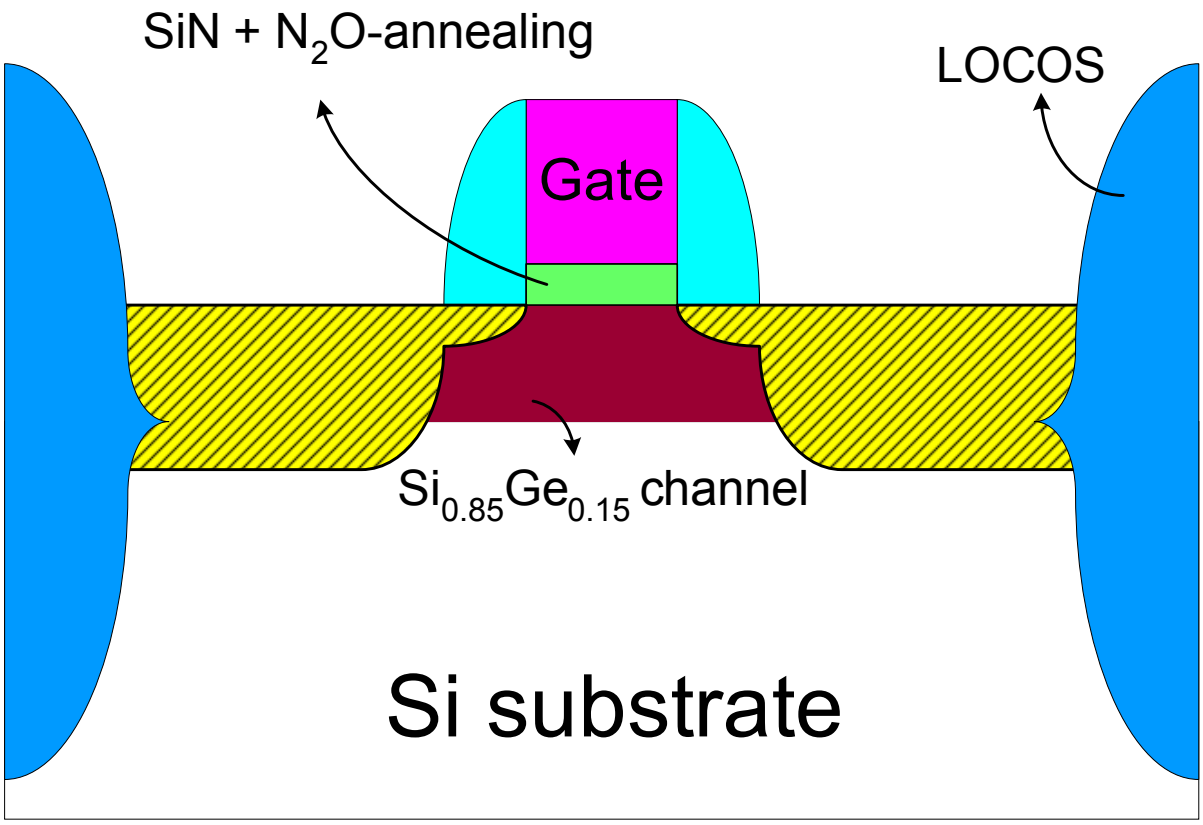


Fig. 2-2 The structure of the $Si_{0.85}Ge_{0.15}$ channel MOSFETs.

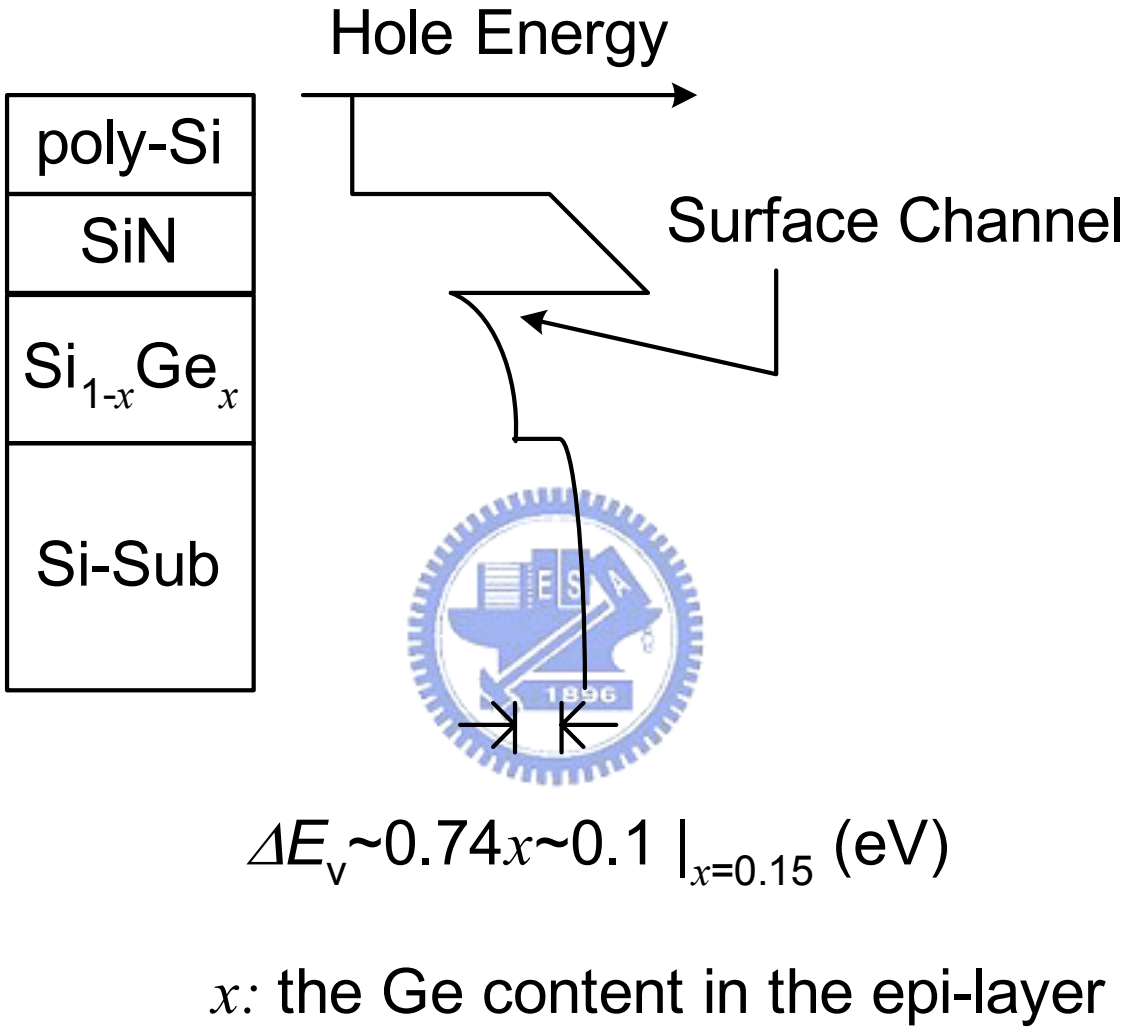
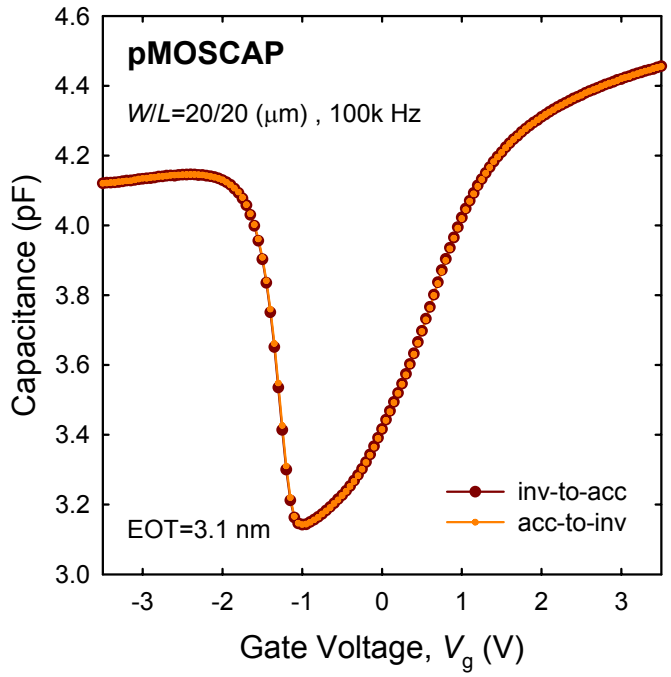


Fig. 3-1 The band diagram of the $Si_{0.85}Ge_{0.15}$ channel device under the inversion condition.



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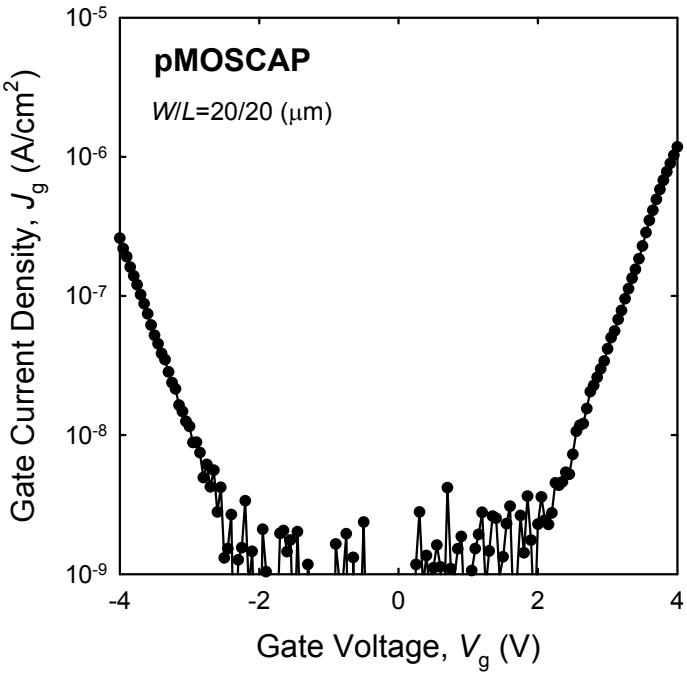


(b)

Fig. 3-2 The electrical characteristics of the pMOSCAP with 50 nm $Si_{0.85}Ge_{0.15}$ channel and N_2O-annealed nitride gate dielectric. (a) The capacitance versus gate voltage. (b) The gate current density versus gate voltage.

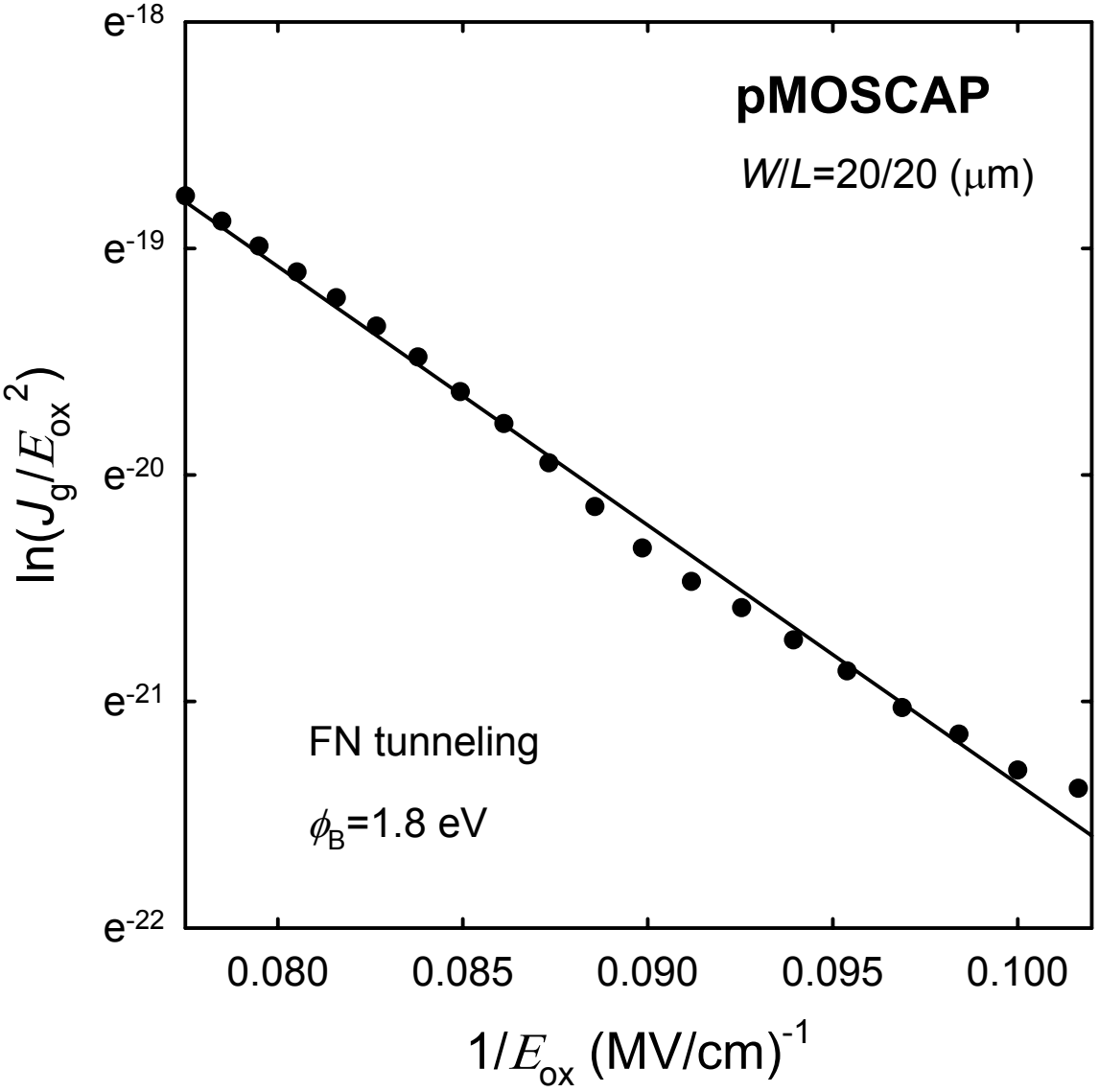
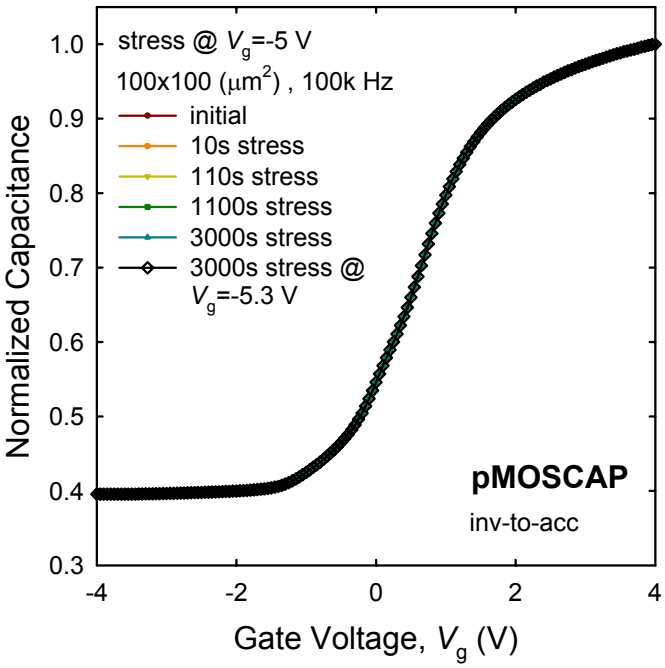


Fig. 3-3 The fitting of the FN tunneling with an effective barrier height of 1.8 eV.



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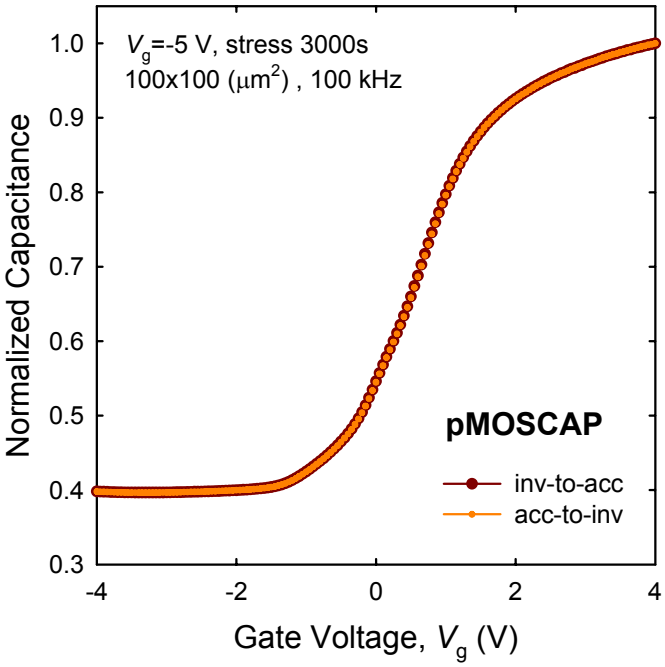
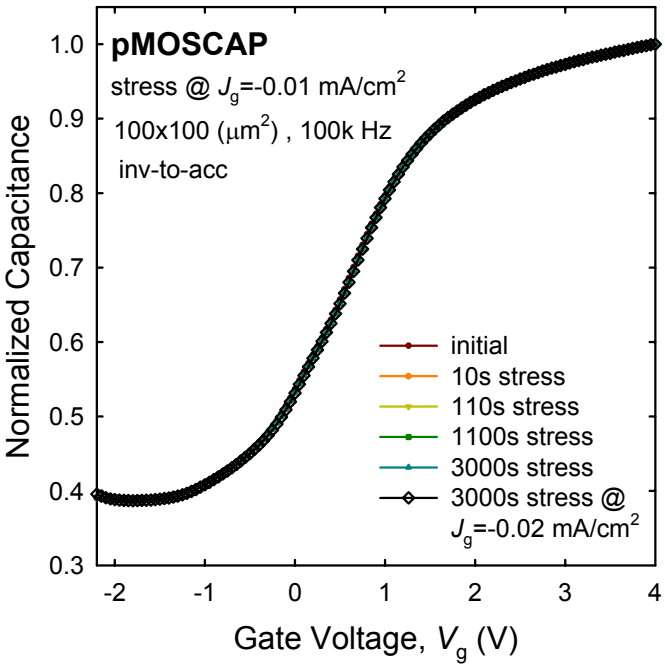
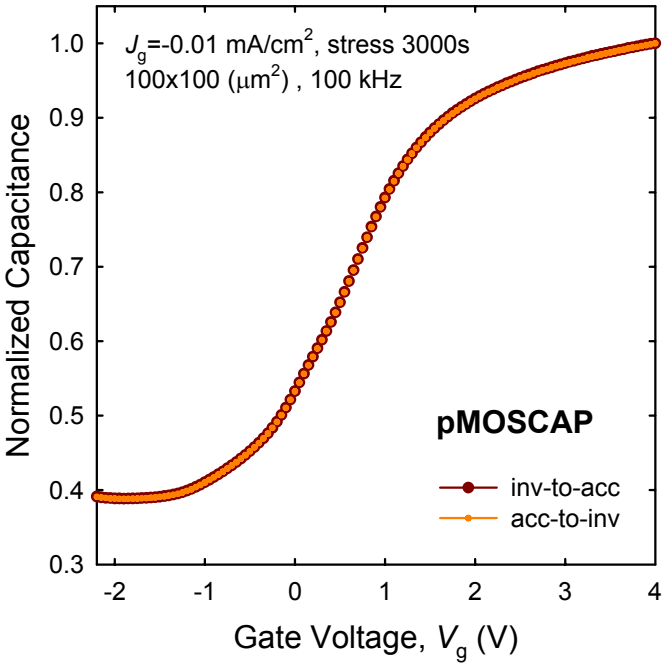


(b)

Fig. 3-4 The normalized capacitances measured under constant voltage stress (CVS). (a) The characteristics of capacitance-voltage (*C*–*V*) with CVS time. (b) The hysteresis after –5 V stressing for 3000 seconds.

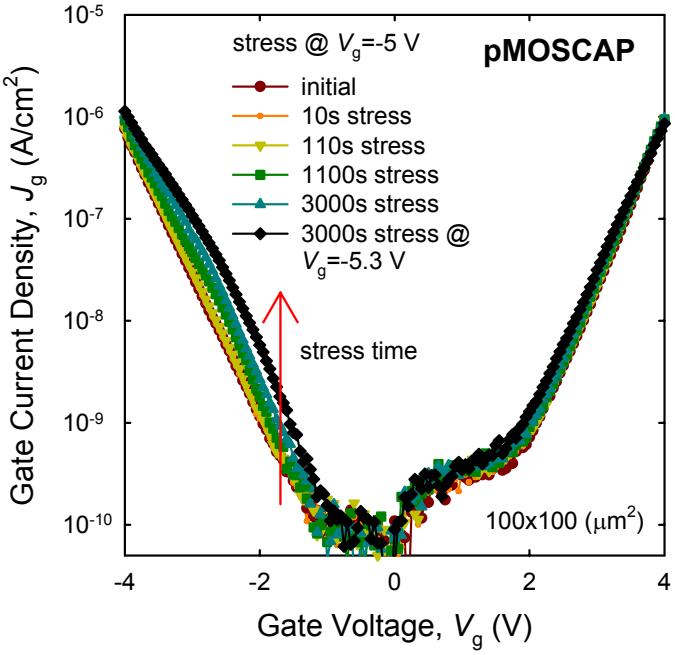


(a)

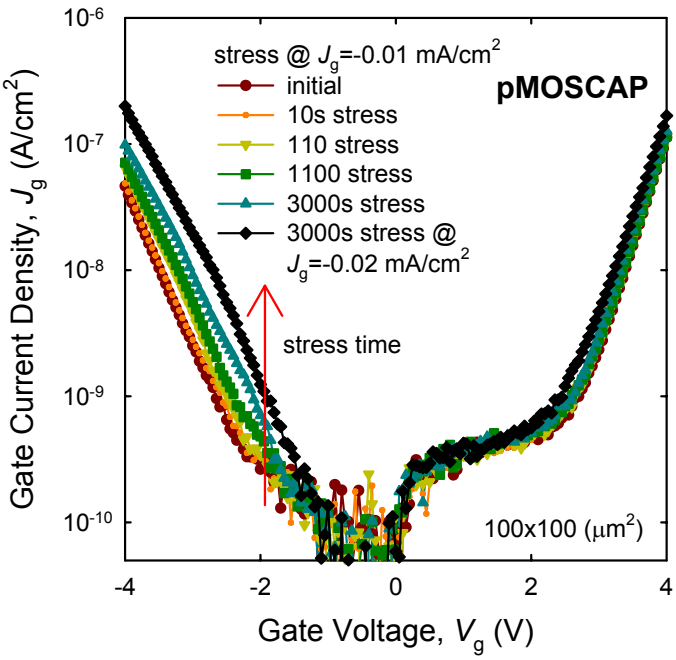


(b)

Fig. 3-5 The normalized capacitances measured under constant current stress (CCS). (a) The characteristics of capacitance-voltage (*C–V*) with CCS time. (b) The hysteresis after –5 V stressing for 3000 seconds.



(a)



(b)

Fig. 3-6 The characteristics of current-voltage (*I–V*) related to (a) CVS time and (b) CCS time.

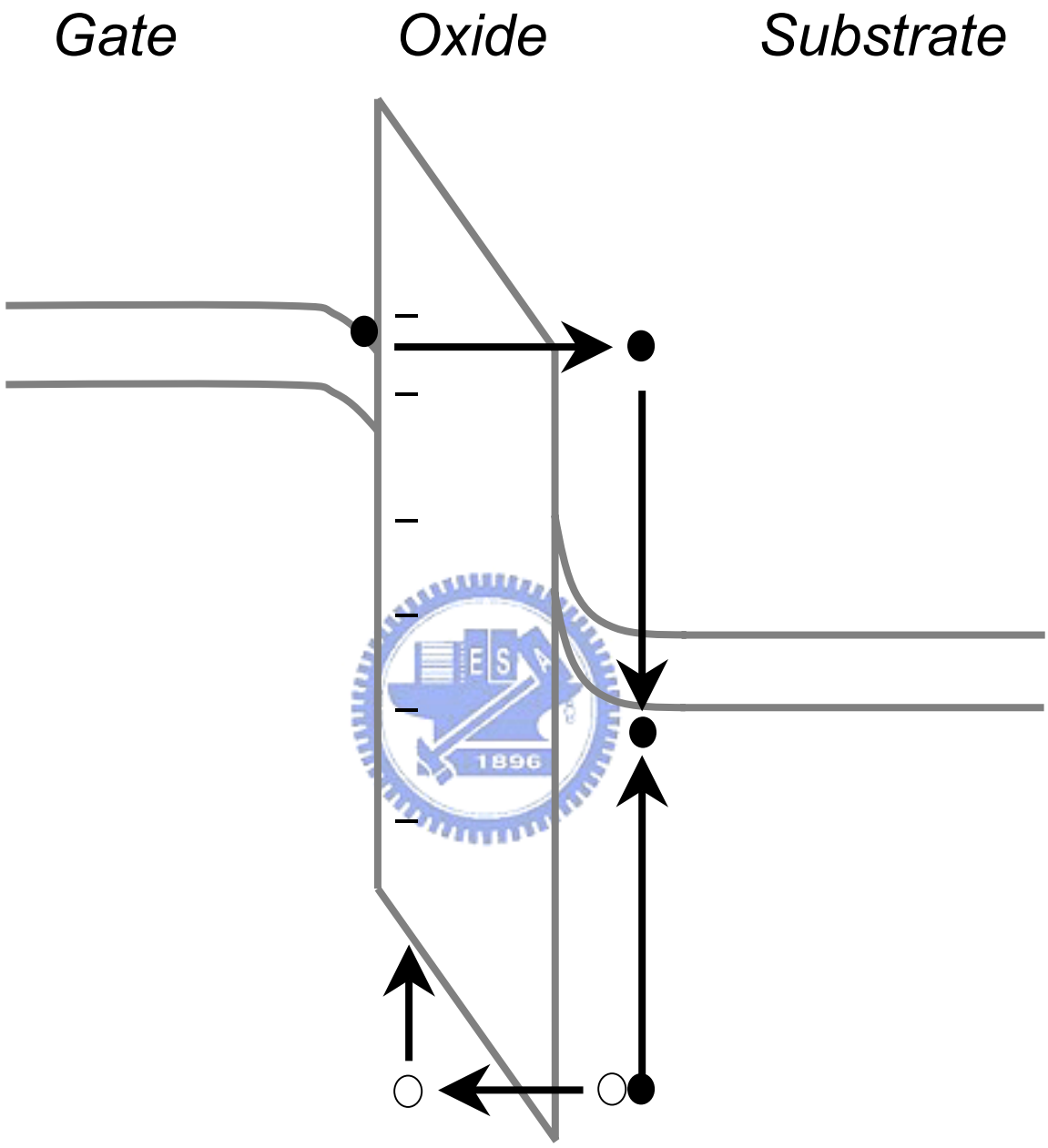
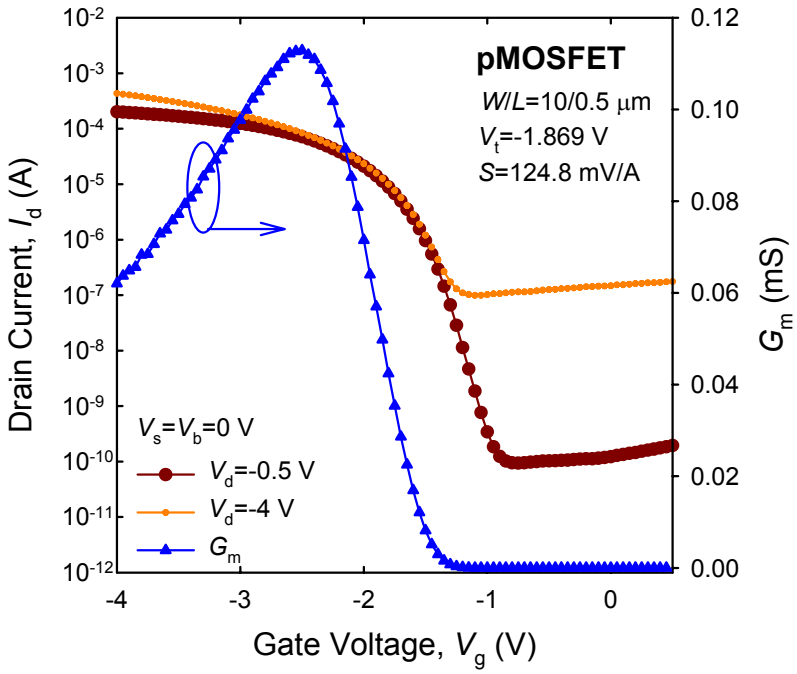
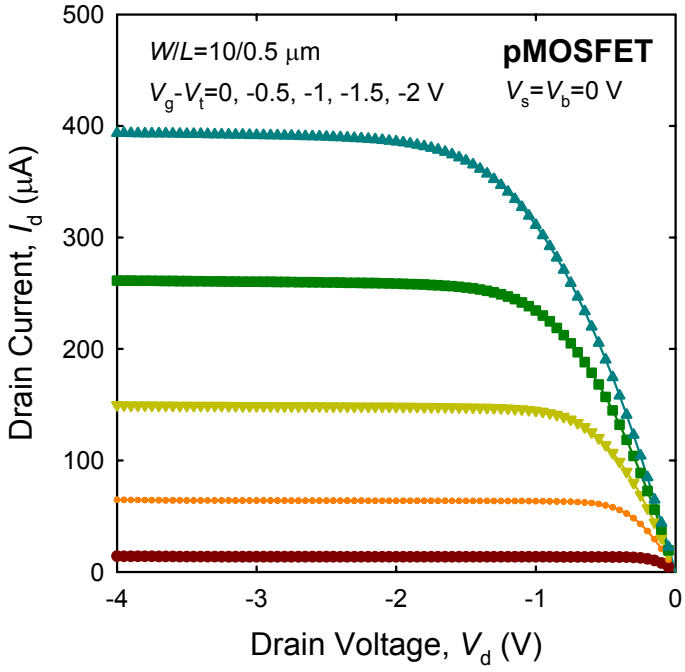


Fig. 3-7 The schematic diagram of anode hole injection (AHI) model.

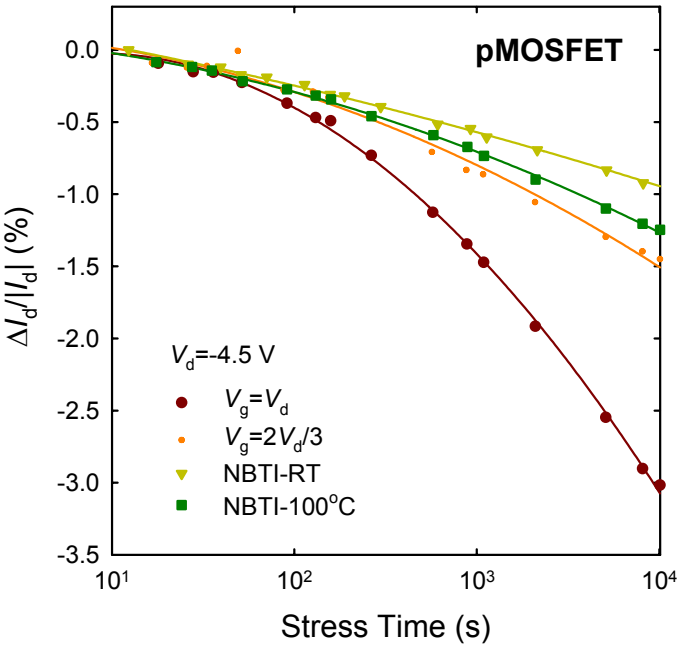


(a)

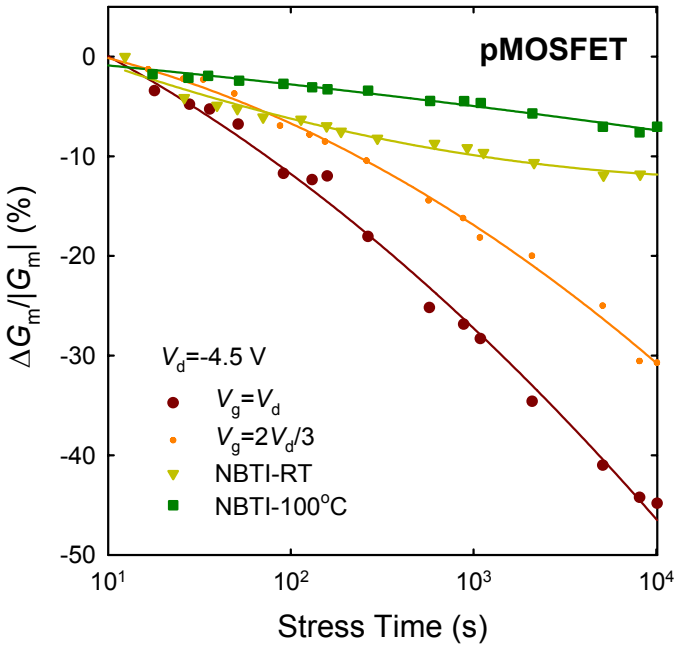


(b)

Fig. 3-8 The electrical characteristics of $Si_{0.85}Ge_{0.15}$ channel pMOSFET with 50 nm $Si_{0.85}Ge_{0.15}$ channel and N_2O-annealed nitride gate dielectric. (a) The I_d–V_g curves. (b) The I_d–V_d curves.



(a)



(b)

Fig. 3-9 The effects of HC and NBTI on pMOSFET with $Si_{0.85}Ge_{0.15}$ channel. (a) The I_d degradation versus stress time. (b) The G_m degradation versus stress time.

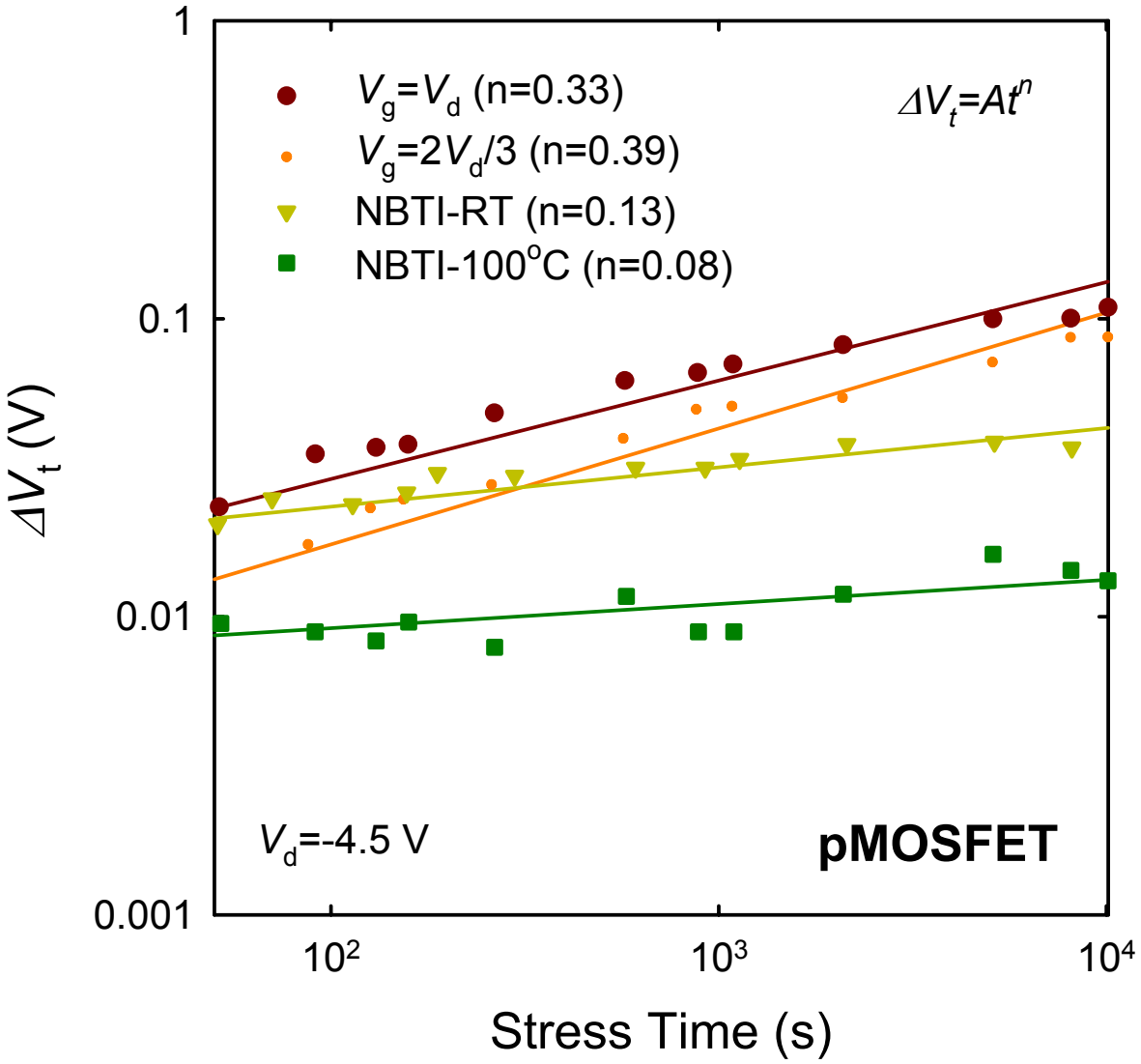
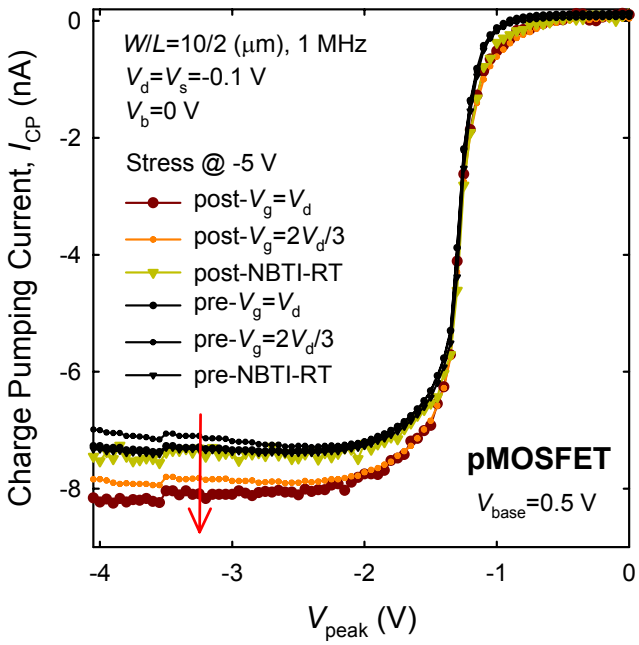
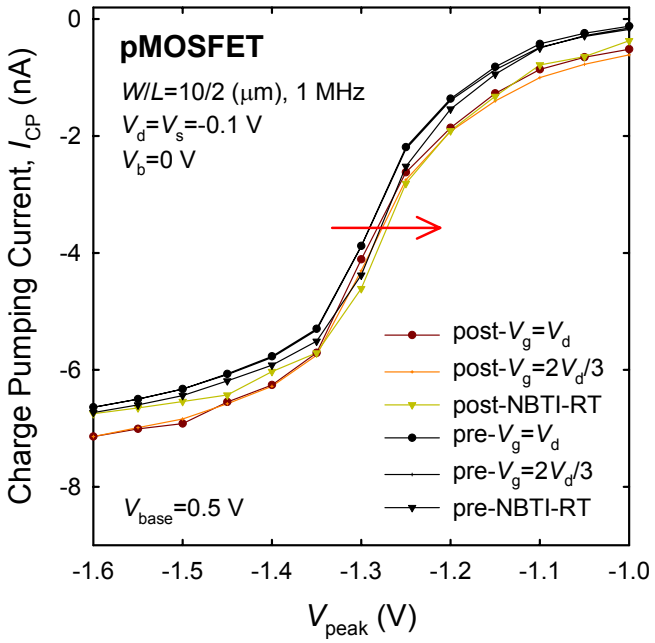


Fig. 3-10 The characteristics of threshold voltage shift versus stress time under different stressing conditions.



(a)



(b)

Fig. 3-11 (a) Compare of charge pumping current before and after stress. (b) Compare of charge pumping current displayed in small scale.

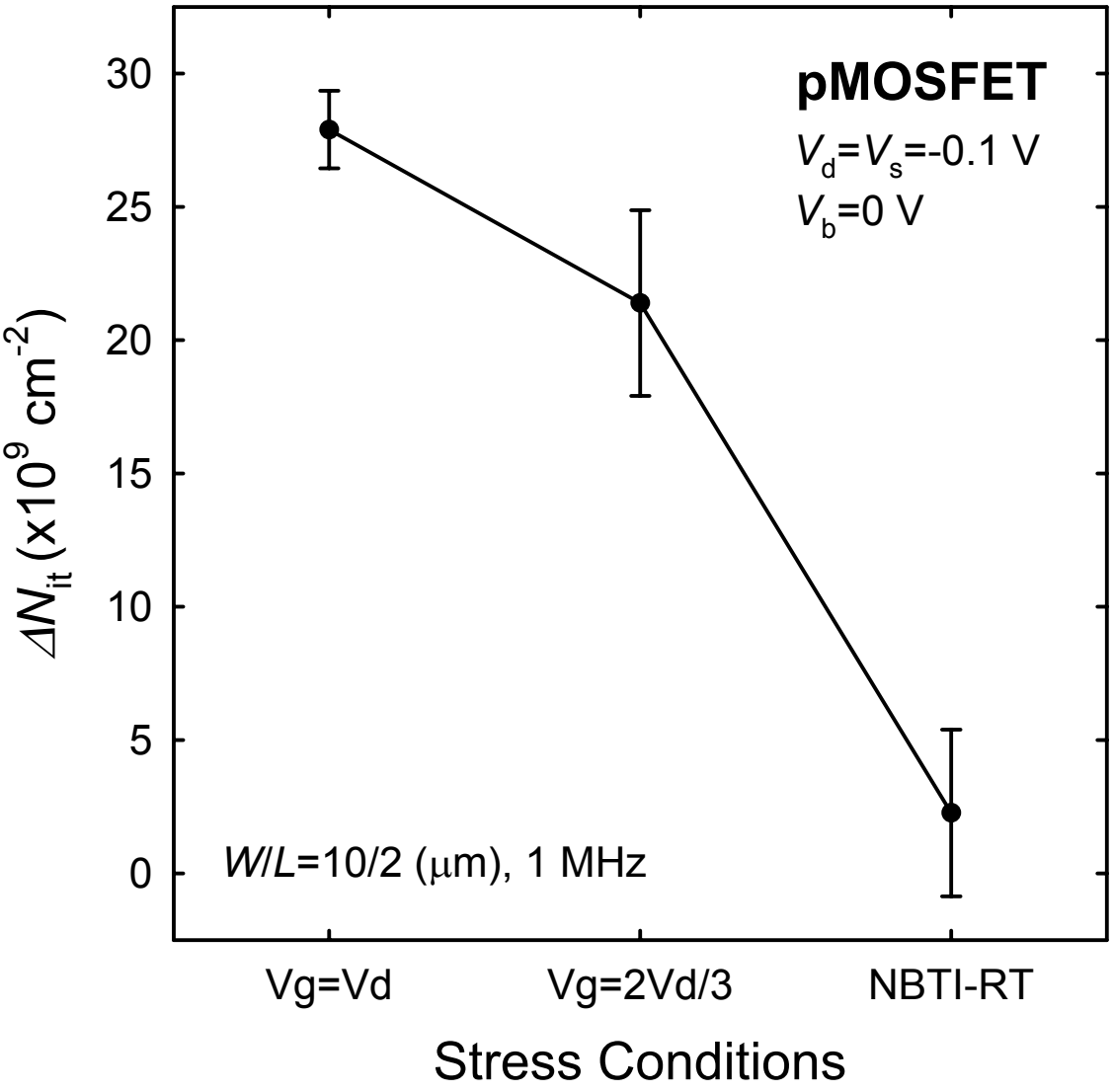
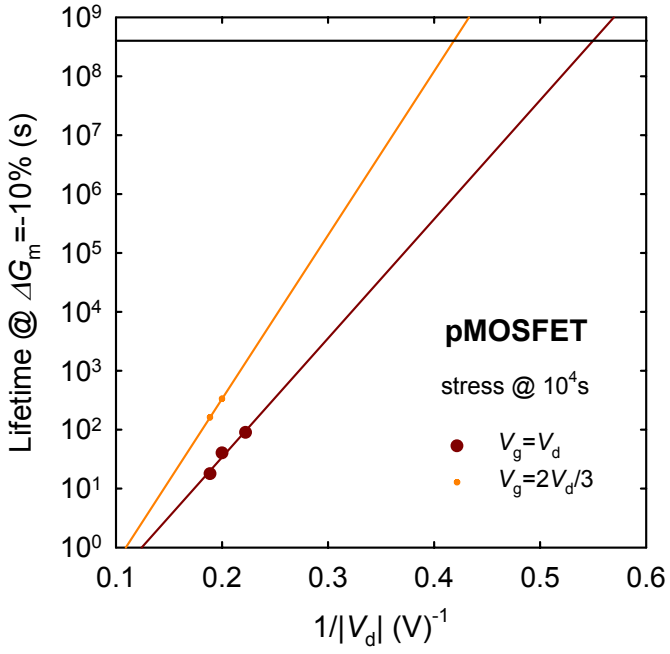
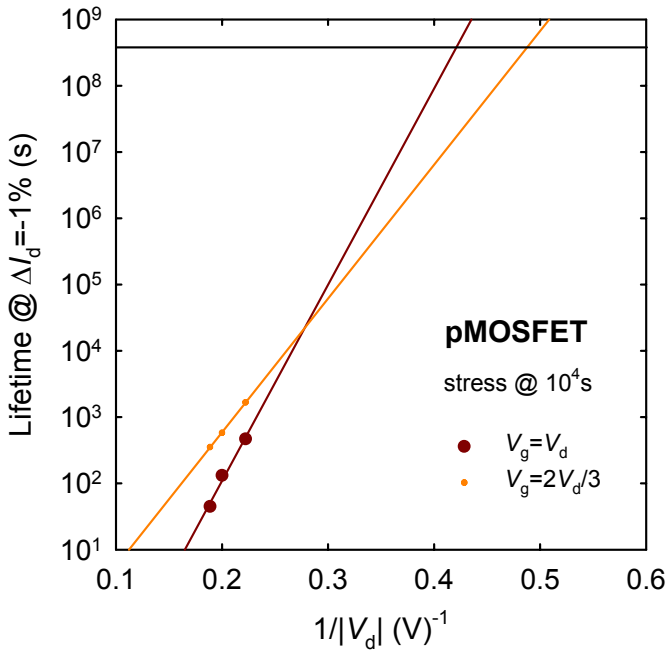


Fig. 3-12 The interface state densities generated by three stressing conditions at stressing voltage of –5 V, which are calculated from the charge pumping current.

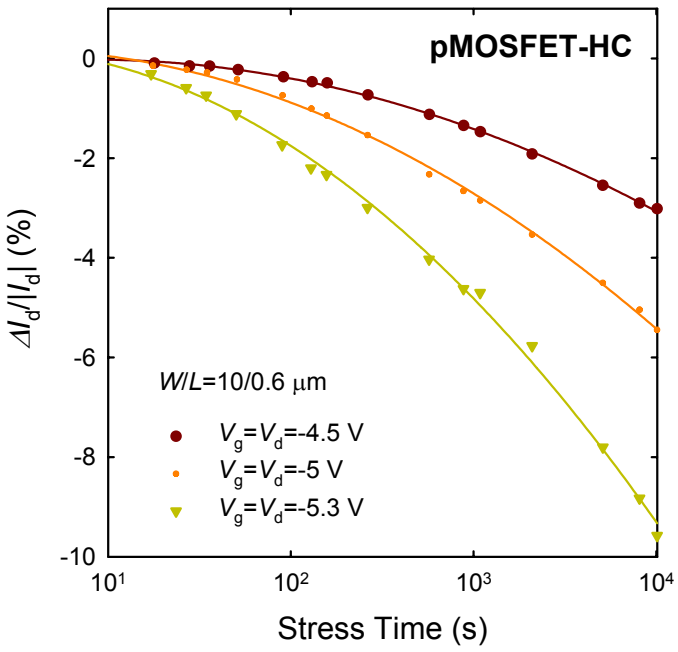


(a)

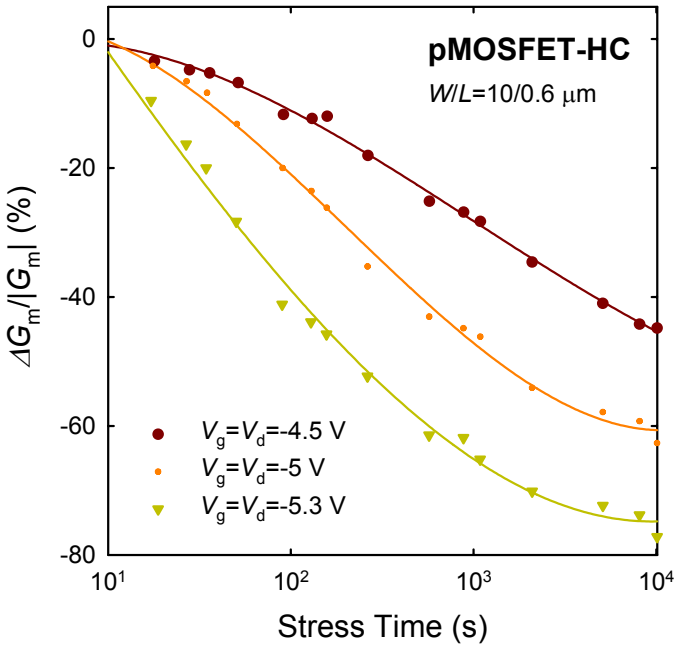


(b)

Fig. 3-13 The lifetime extracted from (a) I_d degradation and (b) G_m degradation.



(a)



(b)

Fig. 3-14 The stressing conditions of V_g=V_d. (a) The I_d degradation and (b) the G_m degradation versus stress time under –4.5, –5 and –5.3 V stressing.

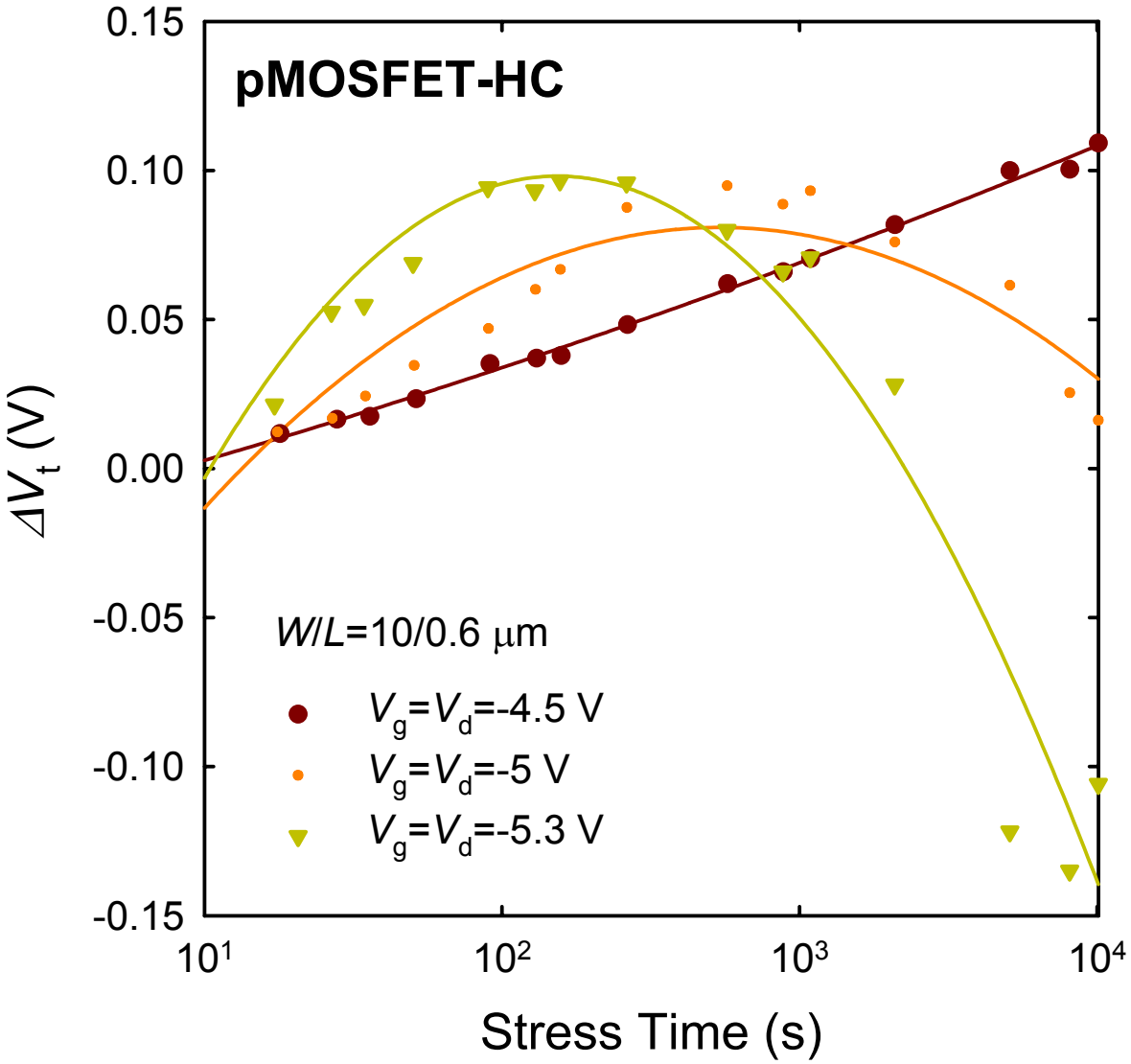
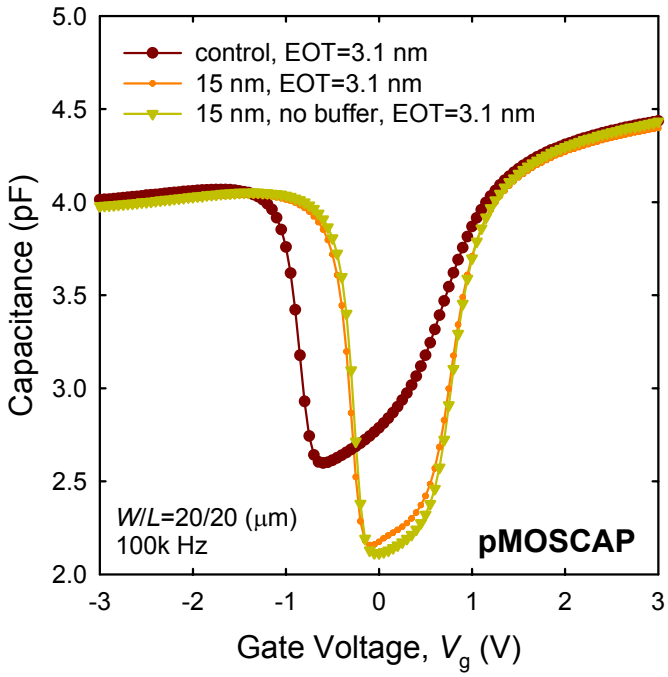
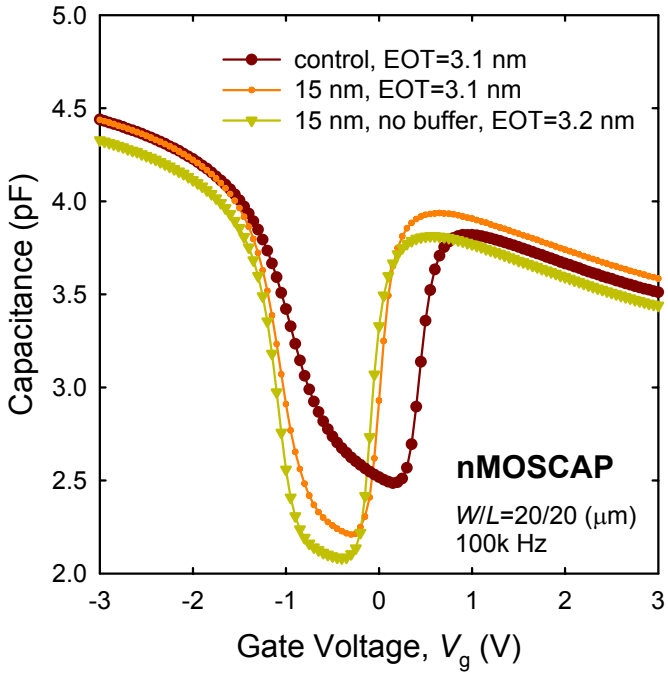


Fig. 3-15 The threshold voltage shifts by the stressing conditions of V_g=V_d.

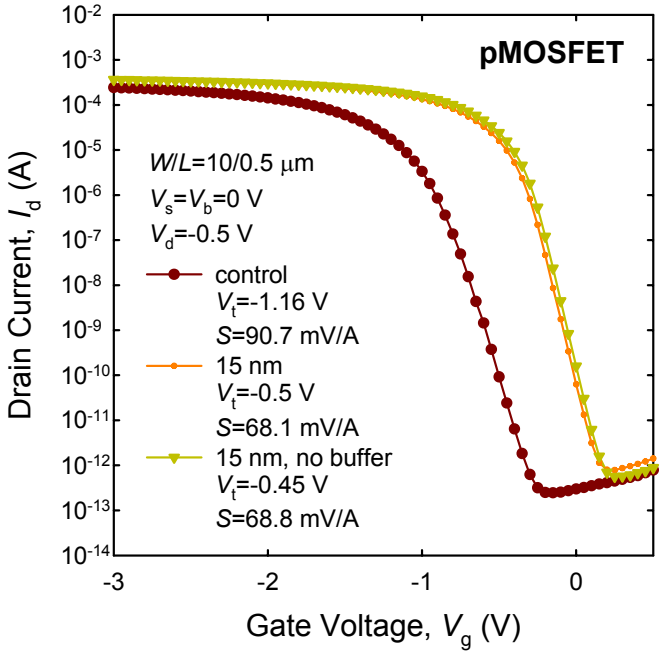


(a)

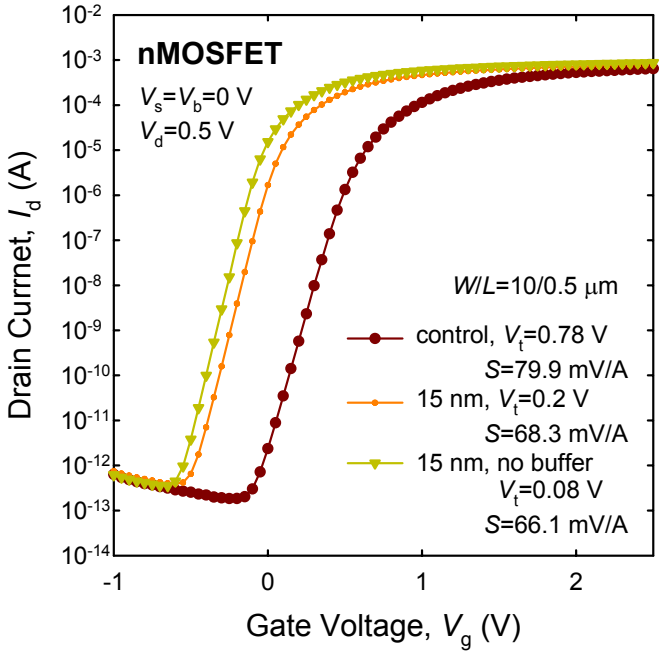


(b)

Fig. 4-1 The *C–V* characteristics of (a) pMOSCAPs and (b) nMOSCAPs with and without the 10 nm Si buffer layer under $Si_{0.85}Ge_{0.15}$ channel. The control samples are the conventional Si channel devices.



(a)



(b)

Fig. 4-2 The I_d–V_g characteristics of (a) pMOSFETs and (b) nMOSFETs with and without the 10 nm Si buffer layer under $Si_{0.85}Ge_{0.15}$ channel. The subthreshold swings are small to 66~68 mV/A. The control samples are the conventional Si channel MOSFETs.

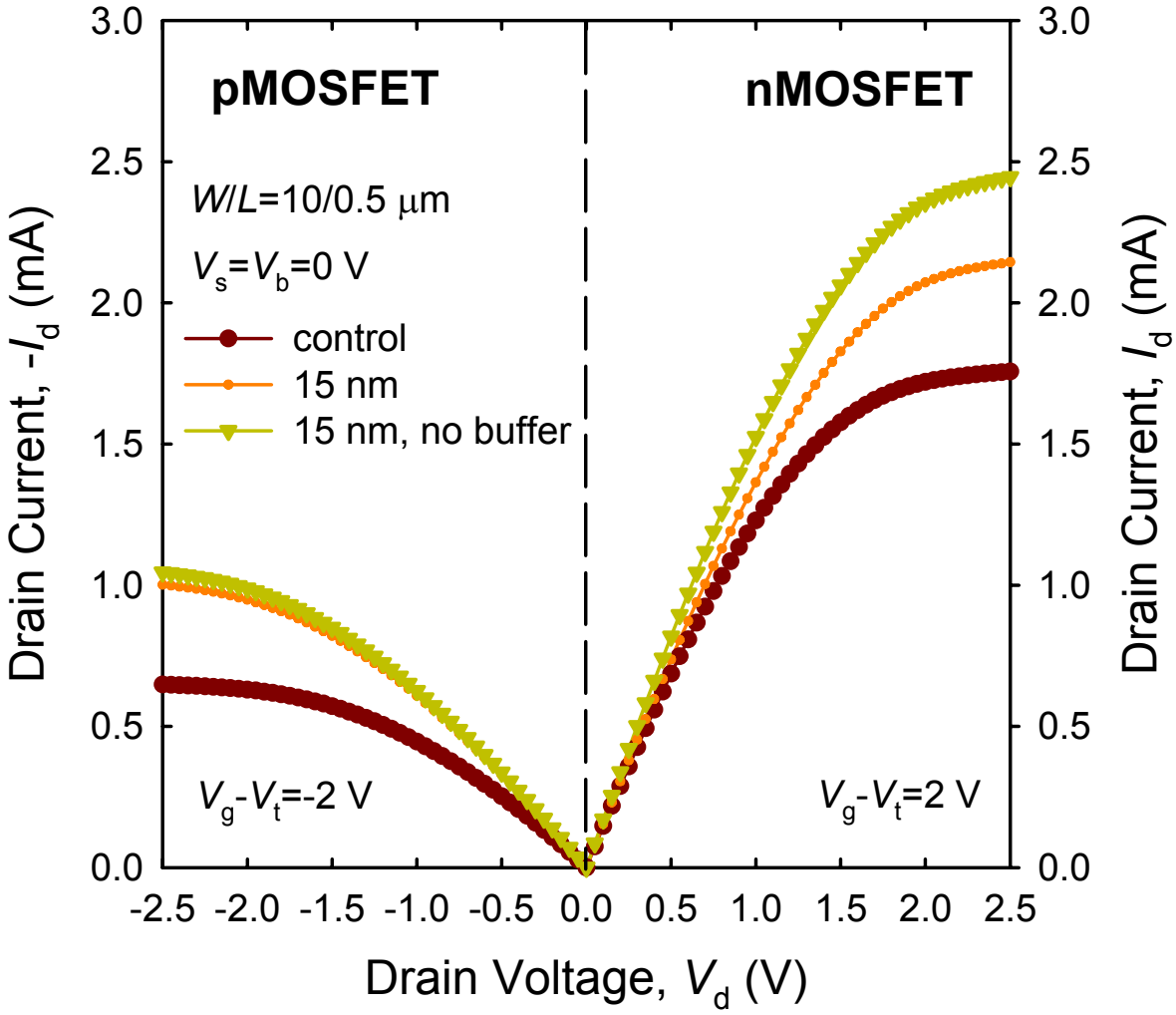
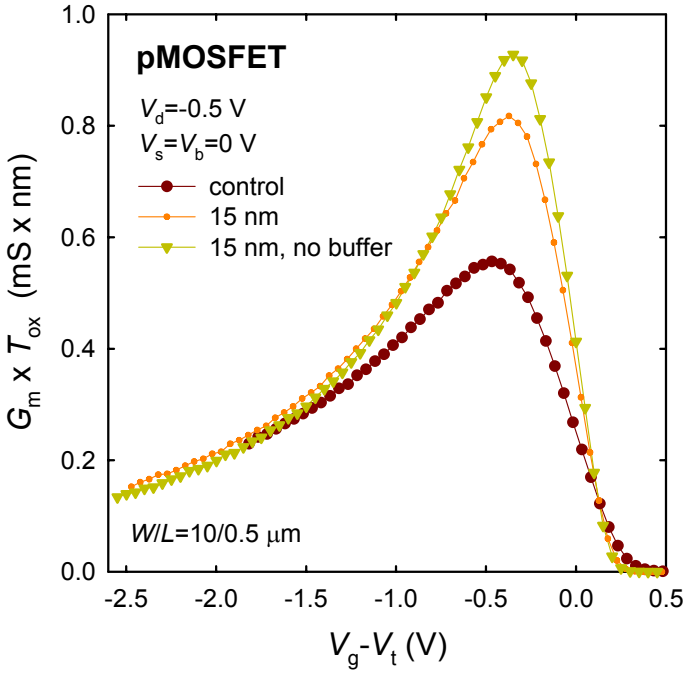
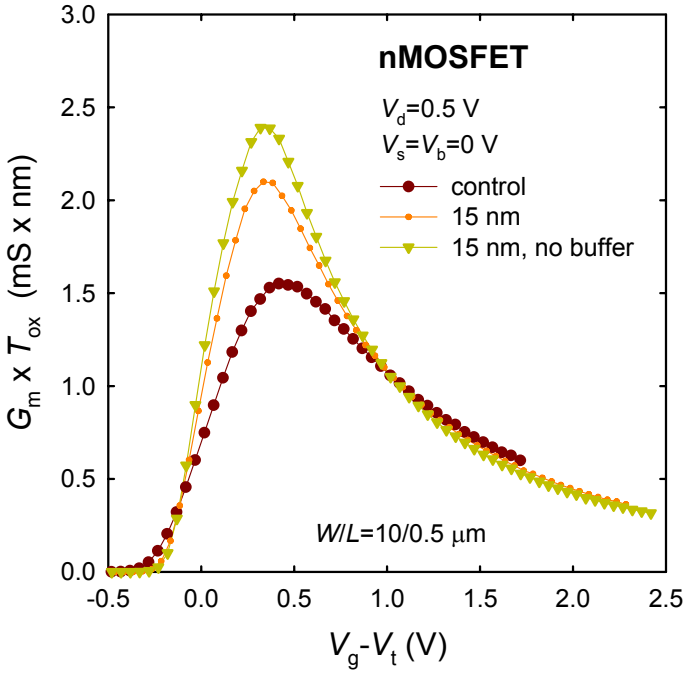


Fig. 4-3 The I_d–V_d characteristics of pMOSFETs (left part) and nMOSFETs (right part) with and without the 10 nm Si buffer layer under $Si_{0.85}Ge_{0.15}$ channel. The control samples are the conventional Si channel devices.

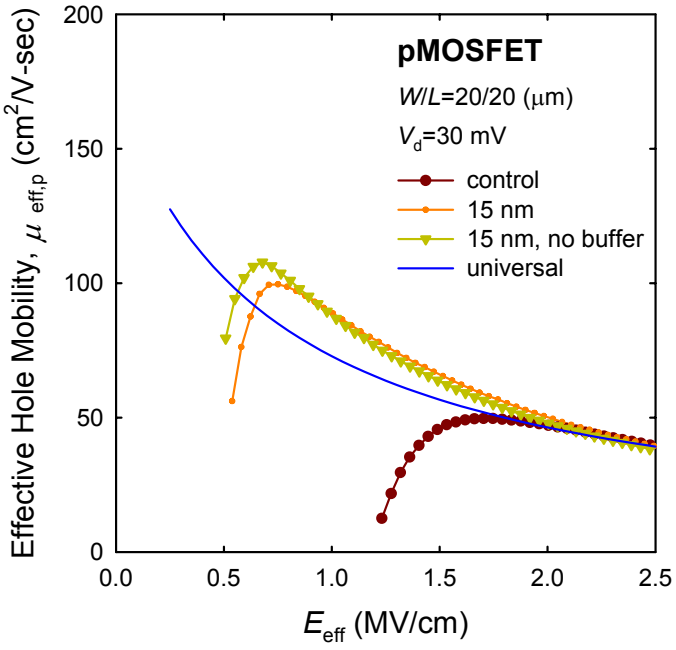


(a)

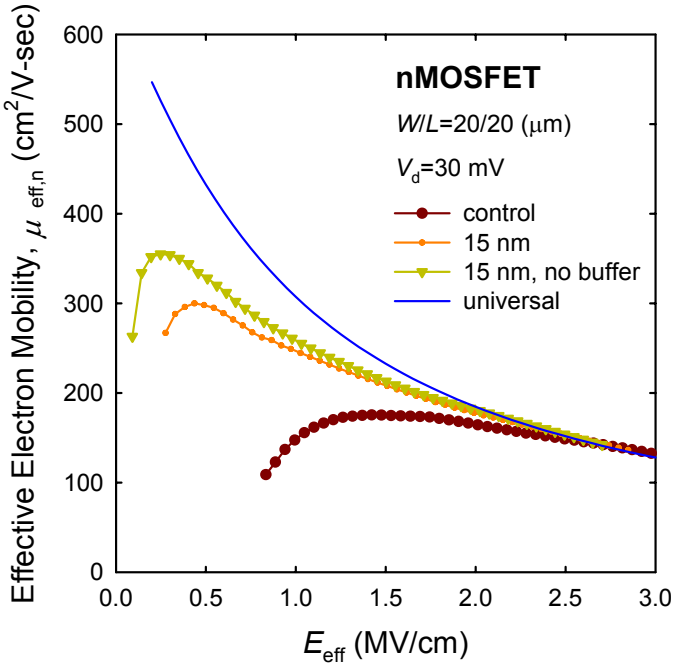


(b)

Fig. 4-4 The transconductance of (a) pMOSFETs and (b) nMOSFETs with and without the 10 nm Si buffer layer under $Si_{0.85}Ge_{0.15}$ channel. The control samples are the conventional Si channel devices.

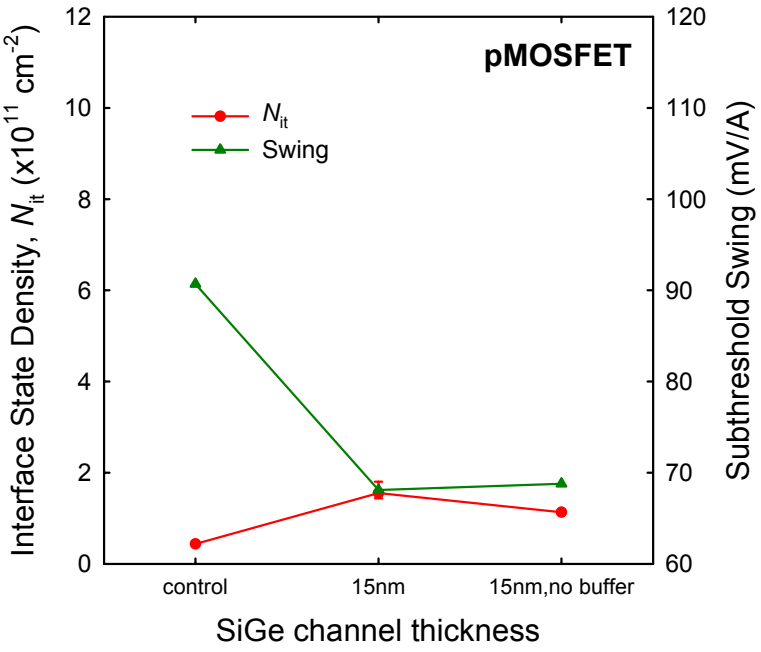


(a)

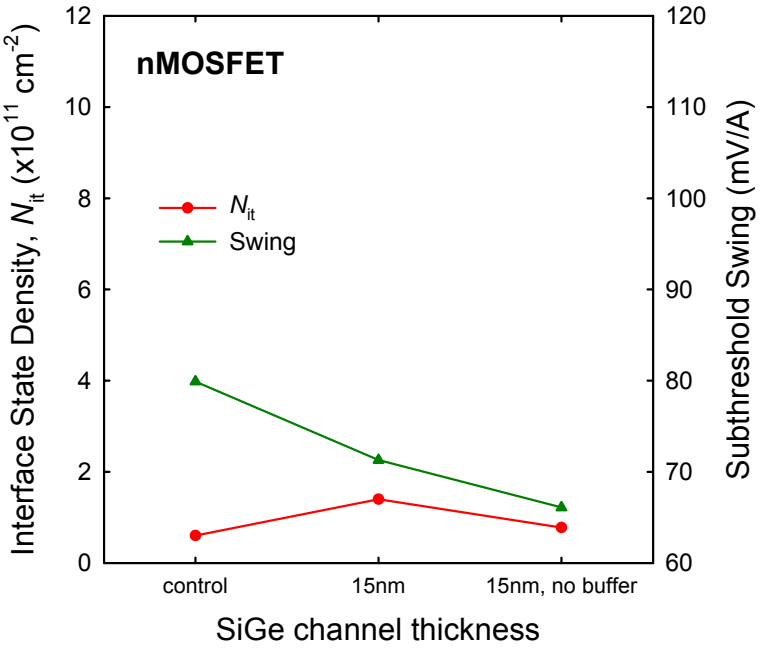


(b)

Fig. 4-5 (a) The effective hole mobility of pMOSFETs, and (b) the effective electron mobility of nMOSFETs.

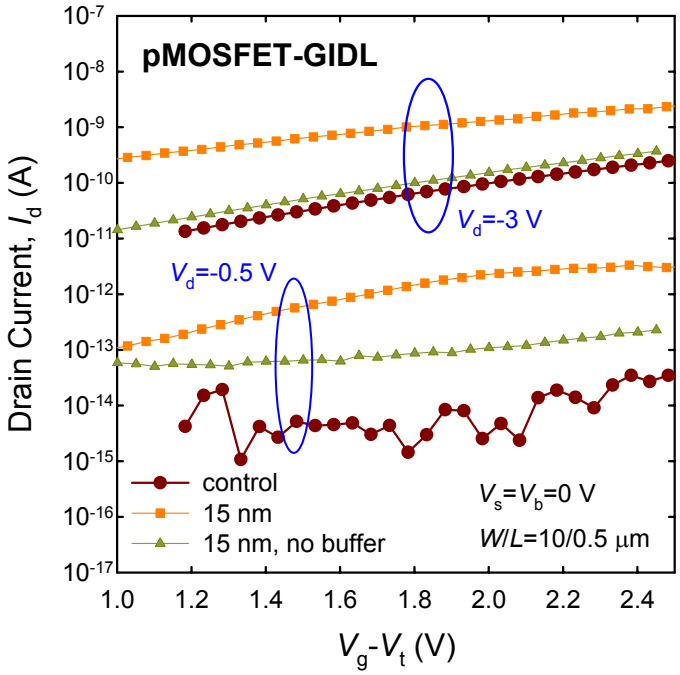


(a)

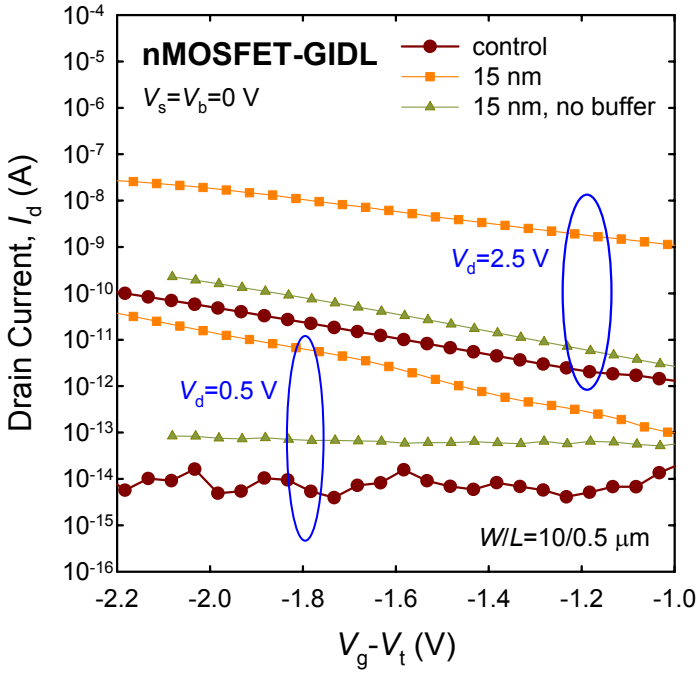


(b)

Fig. 4-6 The interface state density of (a) pMOSFETs and (b) nMOSFETs from charge pumping technique. The relation between subthreshold swing and device structure has also been plotted.

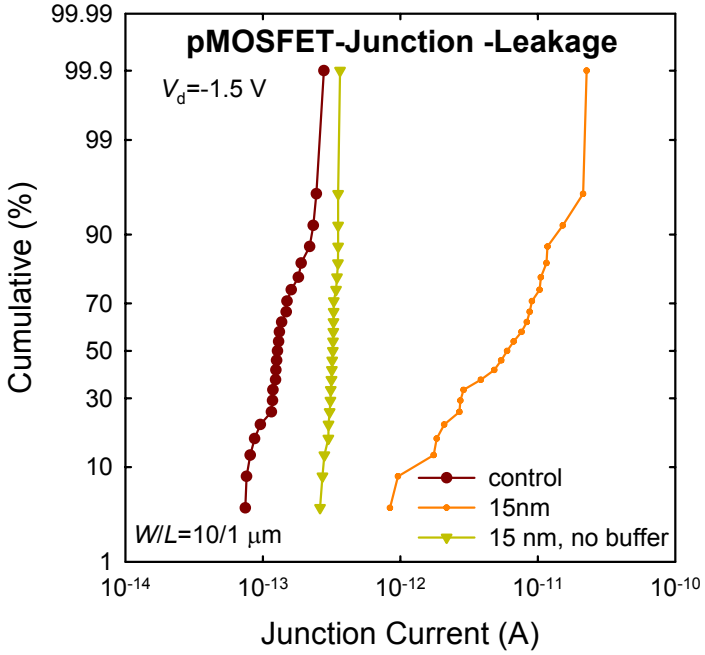


(a)

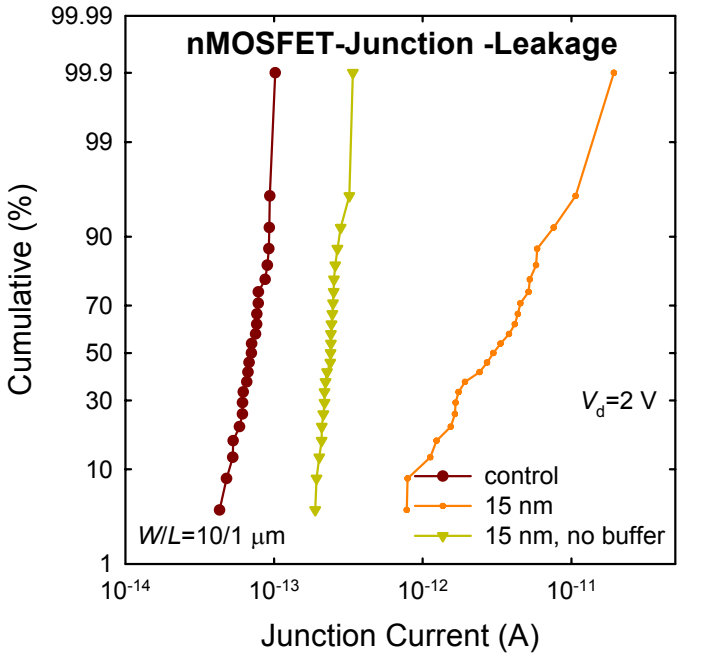


(b)

Fig. 4-7 The measured gate induced drain leakage (GIDL) of (a) pMOSFETs and (b) nMOSFETs with and without the 10 nm Si buffer layer under $Si_{0.85}Ge_{0.15}$ channel. The control samples are the conventional Si channel MOSFETs.

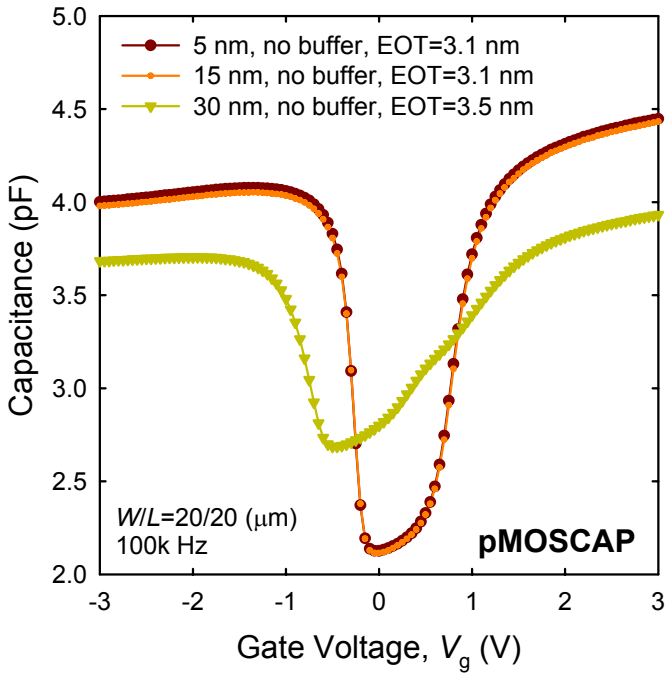


(a)

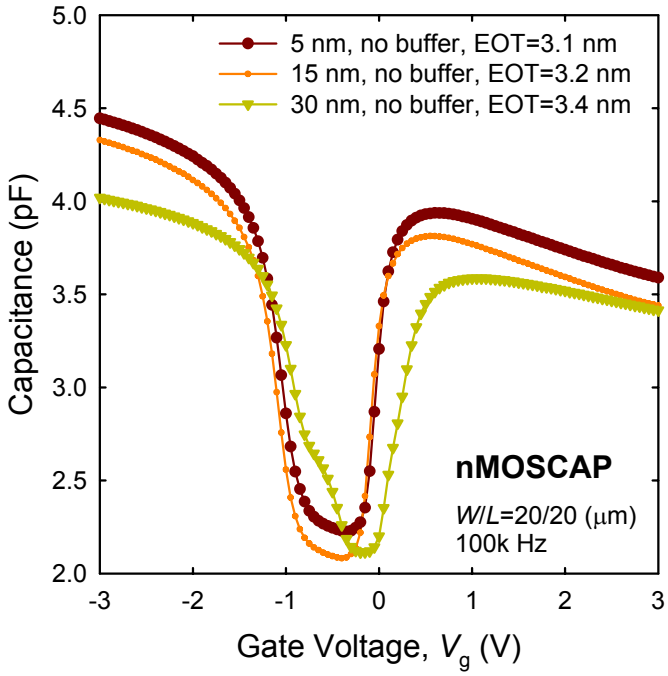


(b)

Fig. 4-8 The junction leakage of (a) pMOSFETs and (b) nMOSFETs with and without the 10 nm Si buffer layer under $Si_{0.85}Ge_{0.15}$ channel.

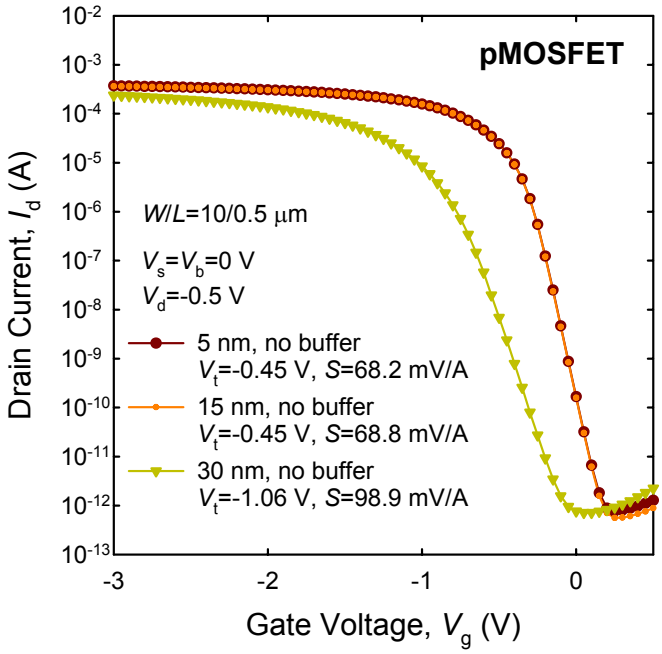


(a)

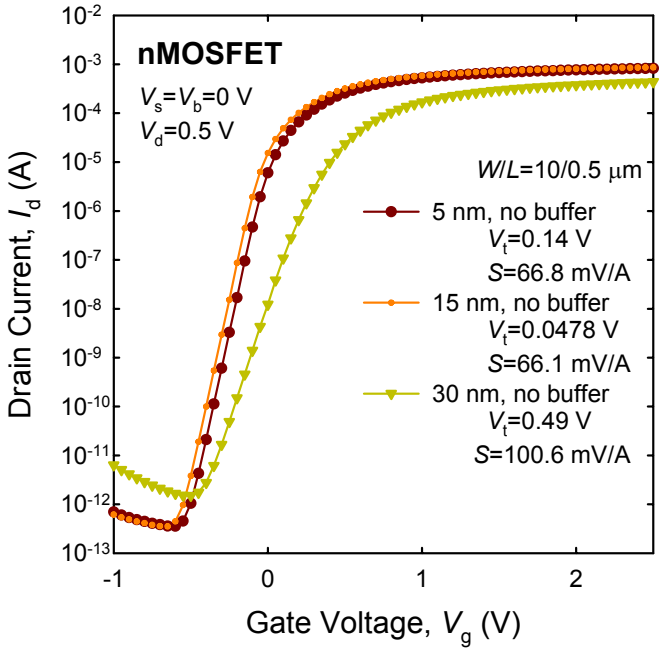


(b)

Fig. 4-9 The *C–V* characteristics of (a) pMOSCAPs and (b) nMOSCAPs with different SiGe channel thickness. All the MOSCAPs have no 10 nm Si buffer layer under the $Si_{0.85}Ge_{0.15}$ channel.



(a)



(b)

Fig. 4-10 The I_d–V_g characteristics of (a) pMOSFETs and (b) nMOSFETs with different SiGe channel thickness. All the MOSFETs have no 10 nm Si buffer layer under the SiGe channel. The thinner $Si_{0.85}Ge_{0.15}$ channel devices have smaller subthreshold swings.

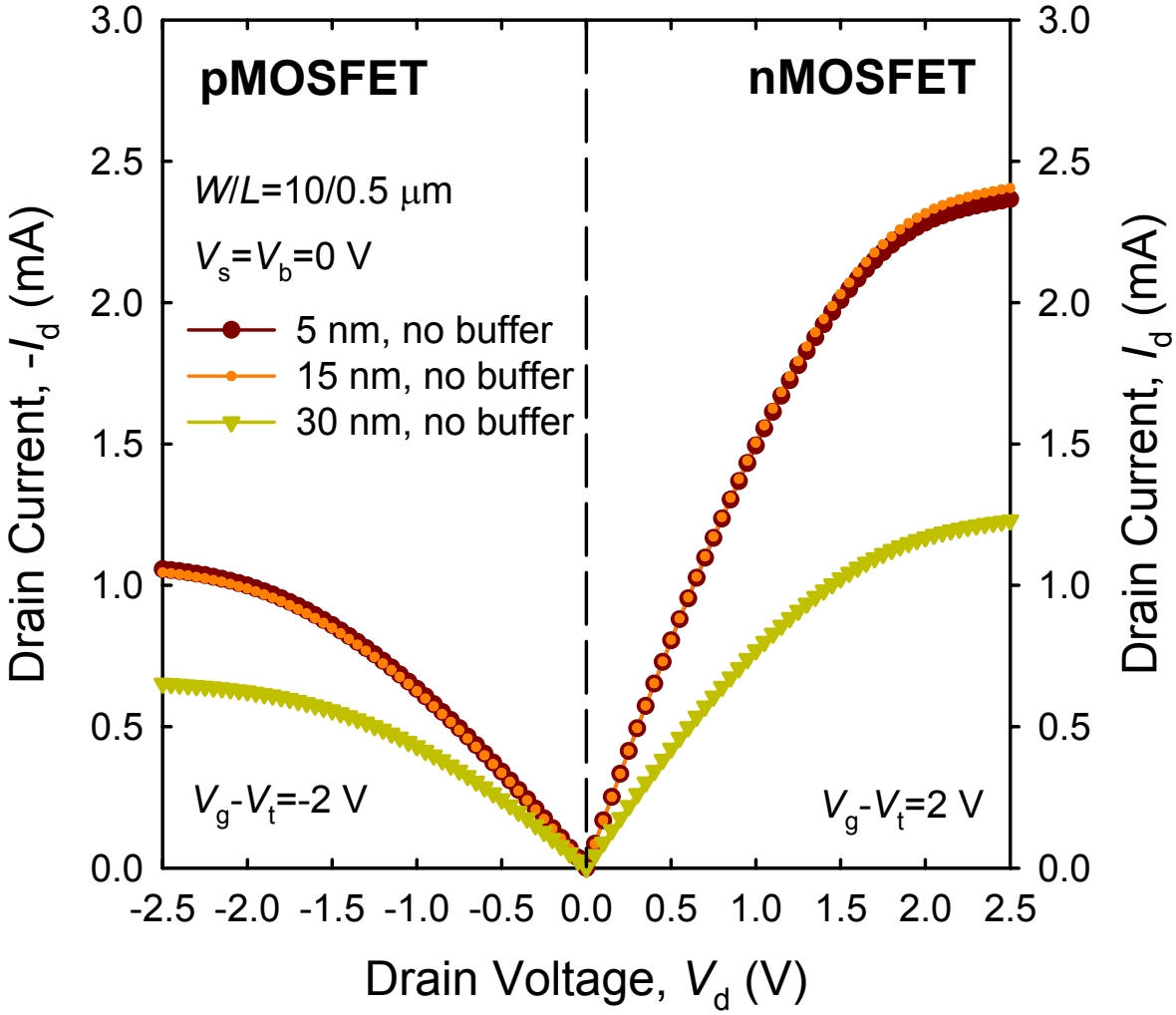
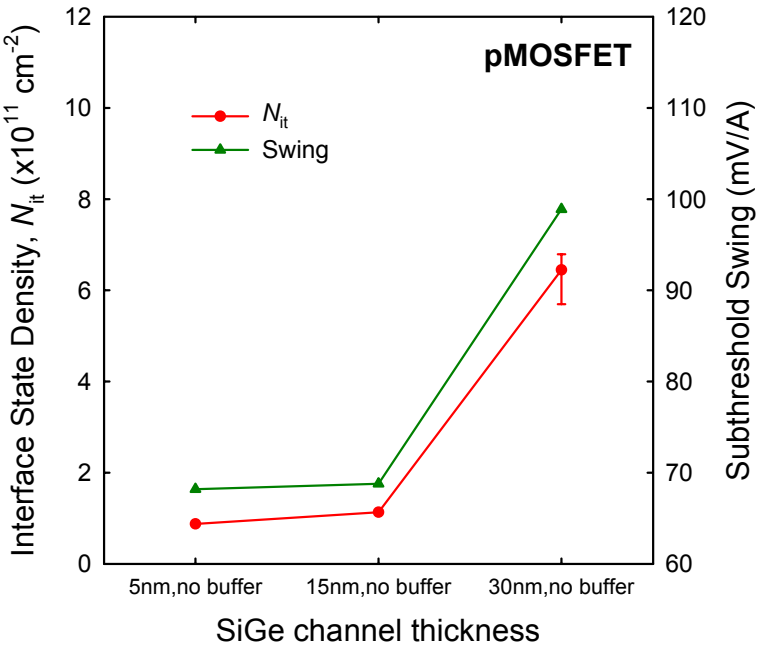
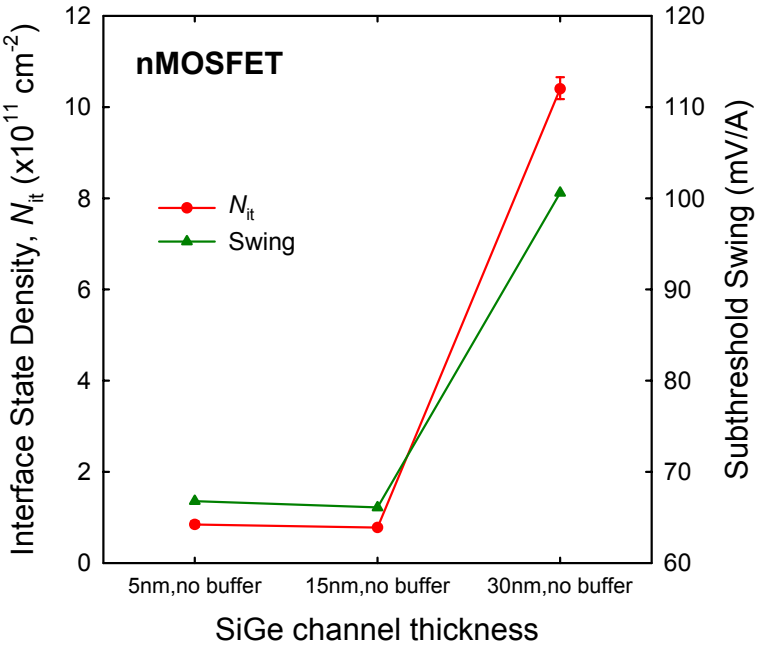


Fig. 4-11 The I_d–V_d characteristics of pMOSFETs (left part) and nMOSFETs (right part) with different SiGe channel thickness. All the MOSFETs have no 10 nm Si buffer layer under the $Si_{0.85}Ge_{0.15}$ channel.

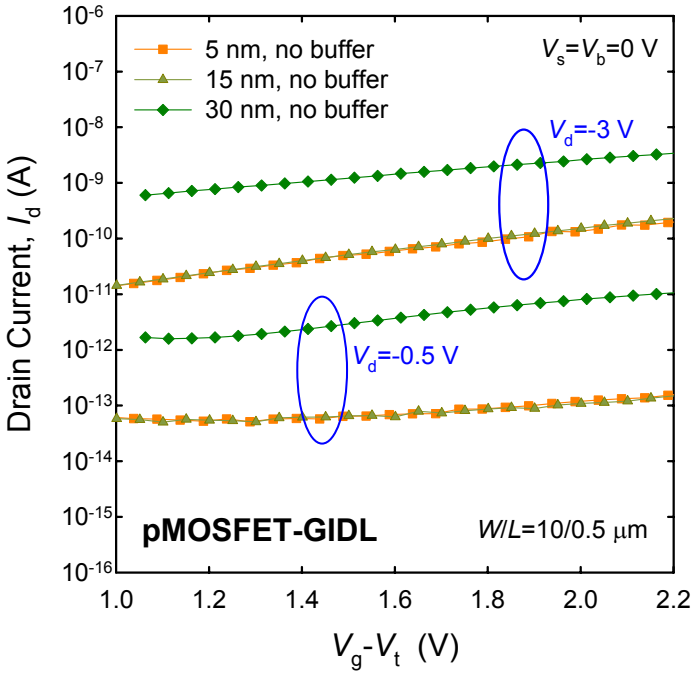


(a)

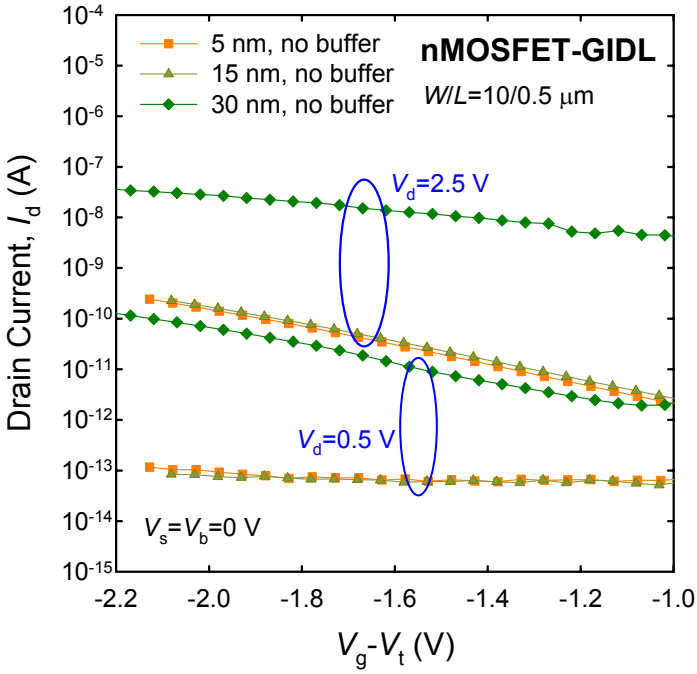


(b)

Fig. 4-12 The interface state density of (a) pMOSFETs and (b) nMOSFETs with different $Si_{0.85}Ge_{0.15}$ channel thickness from charge pumping technique.

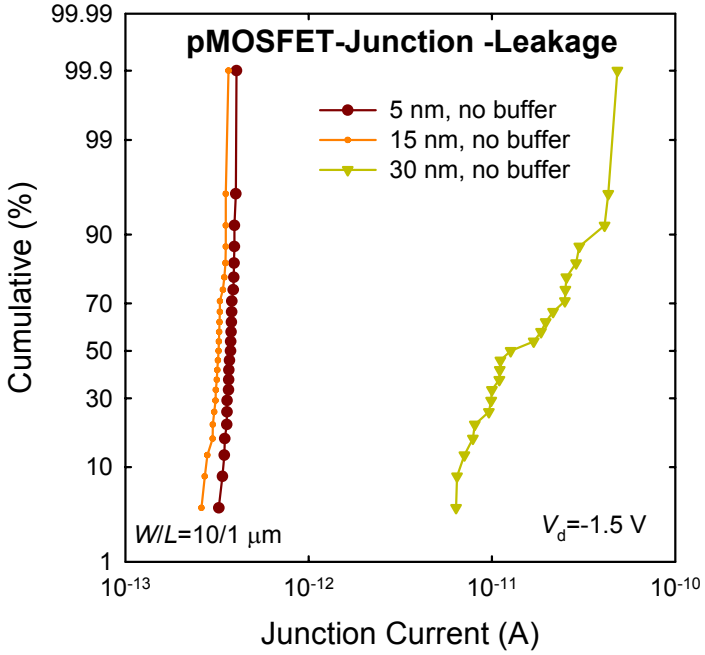


(a)

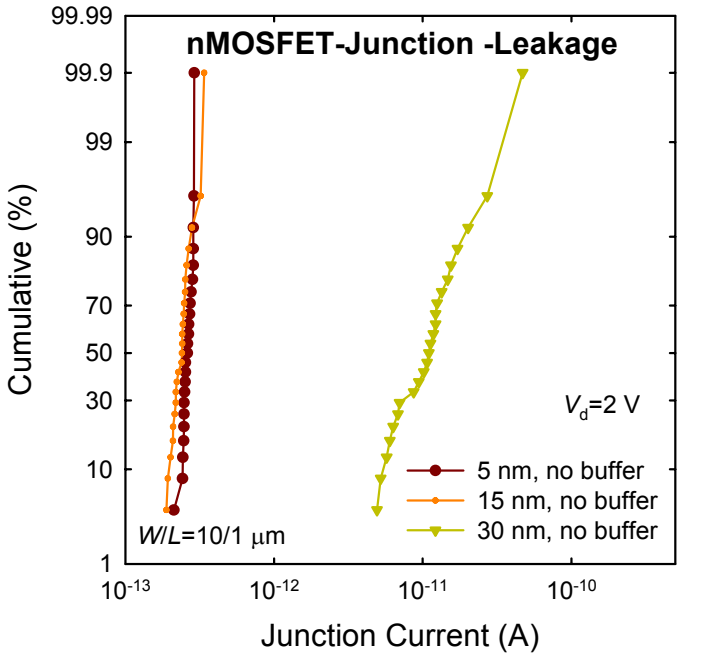


(b)

Fig. 4-13 The measured GIDL of (a) pMOSFETs and (b) nMOSFETs with different SiGe channel thickness. All the devices have no 10 nm Si buffer layer under the $Si_{0.85}Ge_{0.15}$ channel.

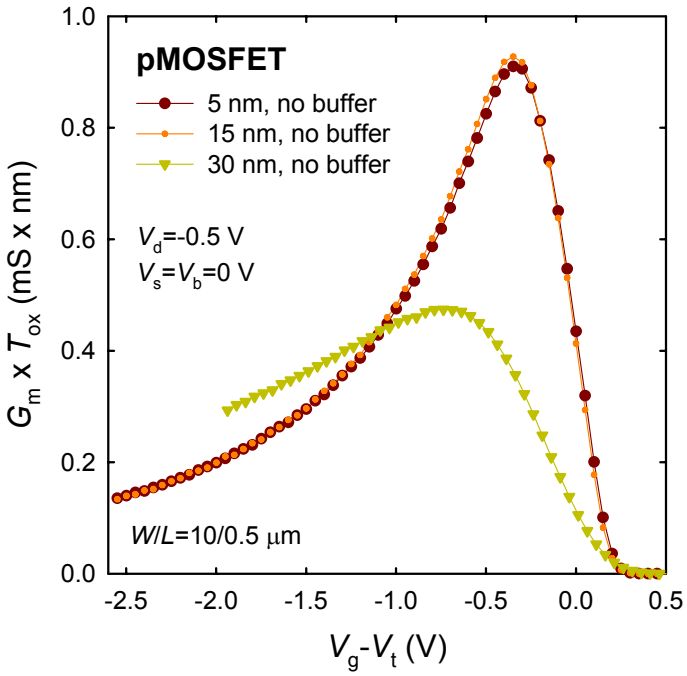


(a)

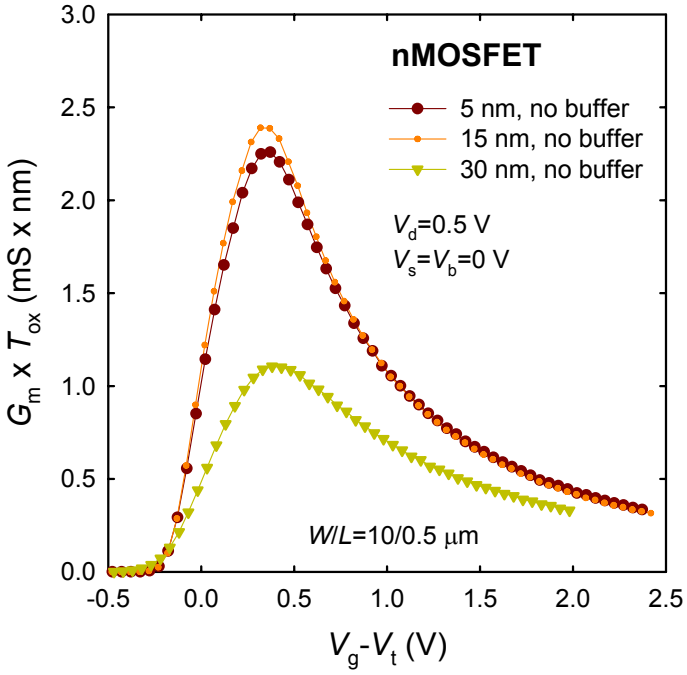


(b)

Fig. 4-14 The junction leakage of (a) pMOSFETs and (b) nMOSFETs with different SiGe channel thickness.

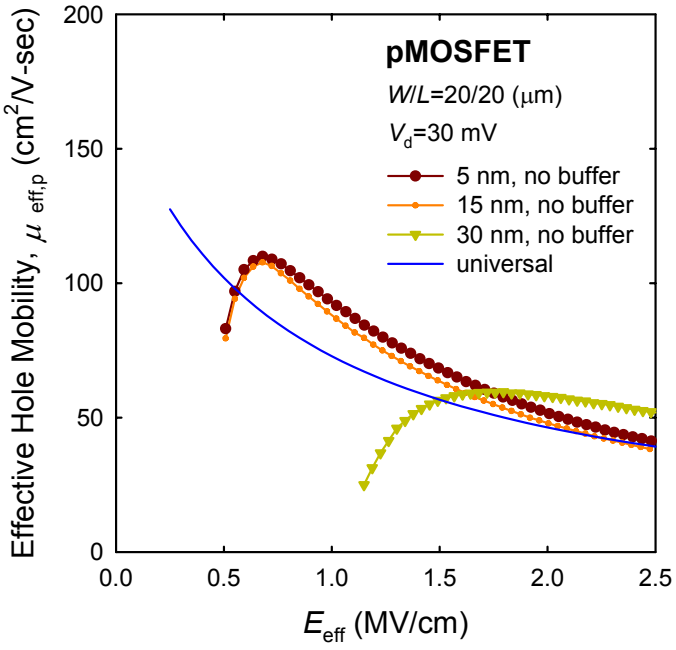


(a)

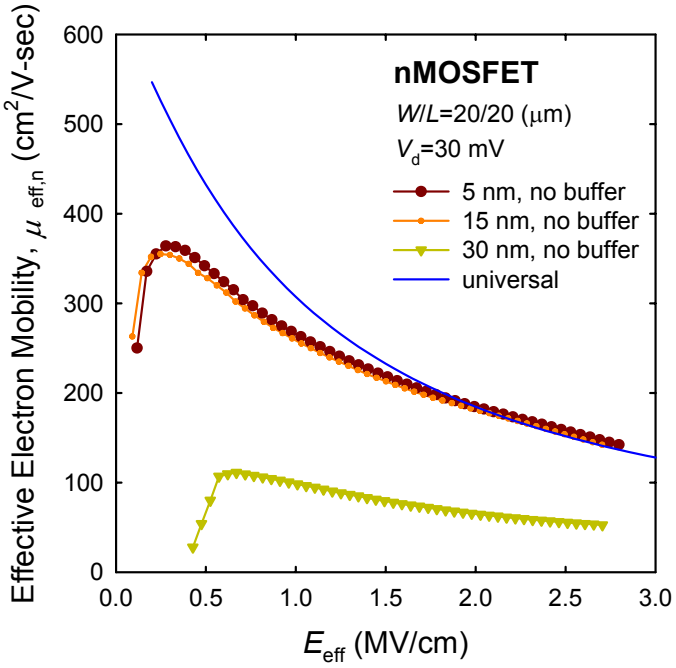


(b)

Fig. 4-15 The transconductance of (a) pMOSFETs and (b) nMOSFETs with different SiGe channel thickness. All the MOSFETs have no 10 nm Si buffer layer under the $Si_{0.85}Ge_{0.15}$ channel.



(a)



(b)

Fig. 4-16 (a) The effective hole mobility of pMOSFETs, and (b) the effective electron mobility of nMOSFETs with different SiGe channel thickness.

簡　歷

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（2002 / 9 ～ 2004 / 6）

碩 士 論 文 題 目：

具有超薄 N_2O 退火氮化物閘極介電層與矽鍺通道之金氧半場效電晶體可靠度及通道厚度效應研究

A Study of Reliability and Channel Thickness Effect on $Si_{0.85}Ge_{0.15}$ MOSFETs with Ultra-Thin N_2O-annealed Nitride Gate Dielectric