多重奈米通道複晶矽薄膜電晶體之製造 與特性研究

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摘要

本研究主要是在探討具有輕參雜(LDD)與多重通道 (multiple channels)結構的複晶矽薄膜電晶體 (poly-Si TFTs),在具有不同通道寬度和數目下,開極 控制能力的好壞,與可靠度的研究。LDD本身具有降低 漏電流的效應,結合上十條奈米導線通道的薄膜電晶 體,展現出較其他通道數目和寬度的TFT,較佳且較穩 定的電性。如較高的開闢電流比(>10⁸),較陡峭的次臨 界導通斜率(SS),較小的汲極導致能障下降(DIBL), 較佳的糾結效應(kink-effect)抑制能力,與較佳的製 程穩定度。原因是M10 有最佳的開極控制能力,及較好 的電漿保護效應。由一系列的實驗結果發現,開極的控 制能力是隨著通道數目的增加而變強。此外在可靠度的 研究中,M10的薄膜電晶體展現佳的抗stress的能力, M10的臨界電壓和次臨界導通斜率幾乎不隨stress時 間而改變。因此這種控制能力佳、高效能、高可靠度, 且不需額外製程的新穎結構之TFT,將可被廣泛的運用 在主動式矩陣液晶顯示器(AMLCD)上



Fabrication and Characterization of Polysilicon Thin Film Transistors with Multiple Nano-wire Channels Student: Chi-Shen Chen Advisor: Dr. S.M. Sze & Dr. Ting-Chang Chang

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We have studied the gate controllability of lightly-doped drain (LDD) polycrystalline silicon thin-film transistors (poly-Si TFTs) with multiple channels and different widths. We deserve that devices with an LDD structure exhibit low leakage current. Additionally, the poly-Si TFT (M10) with ten strips multiple nano-wire channels exhibits the best and the most stable electrical characteristics than all other structures we have studied, such as a higher ON/OFF current ratio (>10⁸), a steeper subthreshold slope (SS, 110 mV/decade), an absence of drain-induced barrier lowering (DIBL), and a improved suppressed kink-effect. Experiments results show the gate controllability is increasing with channel number from single channel to ten strips multiple channels. The M10 TFT also shows the best stress characteristics, as V_{th} and

SS of the M10 TFT remain constant before and after the stress. Devices with the proposed TFTs are highly promising for use in active-matrix liquid-crystal-display technologies without any additional processes.



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