Chapter 1
Introduction

1-1. Overview of polysilicon thin-film transistor technology

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have drawn much attention because of their wide applications in active matrix liquid crystal displays (AMLCDs)[1] and organic light-emitting displays (OLEDs)[2]. Poly-Si TFTs have also been applied in many memory devices such as the dynamic random access memories (DRAMs)[3], static random access memories (SRAMs)[4], electrically programmable read only memory (EPROM)[5], electrically erasable programmable read only memory (EEPROM)[6], linear image sensor[7], thermal printer head[8], photo-detector amplifier[9], scanner[10], and neutral network[10]. Recently, superior performances of poly-Si TFTs have been reported by scaling down device dimensions or utilizing novel crystallization technologies to enhance poly-Si film quality [11.12]. This provides the chance for applying poly-Si TFTs into three-dimensional (3-D) integrated circuit fabrication. Of course, the most important application is in AMLCDs, which leads to rapid development of poly-Si TFT technology.

The major attraction of applying poly-Si TFTs AMLCDs lies in the greatly improved carrier mobility in poly-Si film and the capability of integrating the pixel

switching elements, panel array and peripheral driving circuit on the same substrates [13-15]. In poly-Si film, carrier mobility larger than 10 cm^2/Vs can be easily achieved, that is enough to be used as peripheral driving circuit including n- and p-channel devices. This enables the fabrication of peripheral circuit and TFT array on the same glass substrate. It brings the era of system-on-glass (SOG) technology. The cost of the TFT LCD can be decreased and the reliability can be increased. In addition, the mobility of poly-Si TFTs is much better than that of amorphous ones, the dimension of the poly-Si TFTs can be made smaller compared to that of amorphous Si TFTs for high density, high resolution AMLCDs, and the aperture ratio in TFT array can be significantly improved by using poly-Si TFTs as pixel switching elements. This is because that the device channel width can be scaled down while achieving the same pixel driving requirements as in amorphous silicon (α-Si) TFT AMLCDs.

However, some problems still exist in applying poly-Si TFTs on large-area displays. In comparison with single-crystalline silicon, poly-Si is rich in grain boundary defects as well as intra-grain defects, and the electrical activity of the charge-trapping centers profoundly affects the electrical characteristics of poly-Si TFTs. Large amount of defects serving as trap states locate in the disordered grain boundary regions to degrade the ON current seriously[16]. Moreover, the relatively large leakage current is one of the most important issues of conventional poly-Si TFTs

under OFF-state operation[17-18]. The dominant mechanism of the leakage current in poly TFTs is field emission via grain boundary traps due to the high electric field near the drain junction. A lightly-doped drain (LDD) structure is used to effectively lower leakage current by decreasing drain electric field[19]. Up to date, some studies of poly-Si TFTs also focus on developing new technologies to lower the maximum fabrication temperature, which enables the use of low-quality glass and therefore reduce production cost[20]. Some reported papers focus on the fabrication and characterization of small-dimensional poly-Si TFTs[21], which has high driving ability and high resolution and can be applied on AMLCD peripheral circuitry or the high-resolution projectors. In summary, it is expected that the poly-Si TFTs will becomes more and more important in future technologies, especially when the 3-D circuit integration era is coming. More researches studying the related new technologies and the underlying mechanisms in poly-Si devices with shrinking dimensions are therefore worthy to be indulged in.

1-2. Defects in poly-Si film

Due to the granular structure of the poly-Si film, a lot of grain boundaries and intragranular defects exist in the film. The dangling bonds in grain boundaries will affect device characteristics seriously because they act as trapping centers to trap

carriers. Carriers trapped by these low energy traps can no longer contribute to conduction, which results in the formation of local depletion region and potential barriers in these grain boundaries. Thus, the typical characteristics such as threshold voltage, subthreshold swing, ON current, mobility and transconductance of TFTs are inferior to those of devices fabricated on single crystal silicon film. As for the leakage current, it is well known that the leakage current increase with the drain voltage and gate voltage. The dominant mechanism of the leakage current is field emission via grain boundary traps due to the high electric field near the drain junction.

To overcome this inherent disadvantage of poly-Si film, many researches have been focused on modifying or eliminating these grain boundary traps. Traps are associated with dangling bonds arising from lattice discontinuities between different oriented grains or at the Si/SiO_2 interface. The most useful method so far to remove traps is to passivate these dangling bonds with NH_3 plasma[22-23]. As the number of trapped carrier decreases, the potential barriers in grain boundaries decrease. And the leakage current decreases because of the fewer trap density near the drain region

For devices with smaller dimension, the number of grain boundaries decreases since there are fewer grains within the channel region. Because the drain voltage drops mainly on the depletion regions located at grain boundaries, fewer grain boundaries represent larger voltage drop on each depletion region under the same

drain voltage. Therefore, a large electric field will exist in small dimension TFTs. If the electric field exceeds 10^5 V/cm, the impact ionization effect will occur and the drain current will increase dramatically.

1-3. Motivation

Although poly-Si TFT has high mobility leads to high aperture ratio in TFT array and also the high driving current in peripheral circuits to realization system on glass (SOG). However, there still are some non-ideal effects such as leakage current, DIBL effect, kink effect are found to influence device characteristics seriously to limit its applications. In order to overcome the previous non-ideal effects, firstly we apply the lightly-doped drain (LDD) structure to reduce the lateral electrical field in channel, which is responsible to achieve low leakage current. Secondly, according CMOS technology, several high performance surrounding gate structures in silicon on insulator (SOI) MOSEFT, such that double-gate[24], tri-gate[25], FinFET[26], and gate-all-around[27], have been reported that they have superior gate control over channel than conventional single-gate MOSFET to reduce the non-ideal effects. Thus, applying the surrounding gate structure, we can reduce the non-ideal effects and achieve high performance poly-Si TFTs. Thus, in this thesis, firstly, we employed both multiple channels and LDD structure to investigate the surrounding gate

controllability relative to different multiple channel width and number in poly-Si thin film transistor. Secondly, the proposed TFTs' reliability were also studied by stress duration relative to different multiple channel width and number in poly-Si thin film transistors.

Chapter 2
Poly-Si conduction mechanism

2-1. Transport properties of poly-Si

As mentioned in section 1-1 and 1-2, the device characteristics of poly-Si TFTs are strongly influenced by the grain structure in poly-Si film. Even though the inversion channel region is also induced by the gate voltage as in MOSFETs, the existence of grain structure in channel layer bring large differences in carrier transport phenomenon. Many researches studying the electrical properties and the carrier transport in poly-Si TFTs have been reported. Many authors have explained this simple grain boundary-trapping model in detail [1-3]. In this model, it is assumed that the poly-Si material is composed of a linear chain of identical crystallite having a grain size L_g and the grain boundary trap density N_t. The charge trapped at grain boundaries is compensated by oppositely charged depletion regions surrounding the grain boundaries. It is shown in Fig 2-1. From Poisson's equation, the charge in the depletion regions causes curvature in the energy bands, leading to potential barriers that impede the movement of any remaining free carriers from one grain to another. When the dopant/carrier density n is small, the poly-Si grains will be fully depleted. The width of the grain boundary depletion region x_d extends to be $L_g/2$ on each side of

the boundary, and the barrier height V_B can be expressed as

$$V_B = \frac{qn}{2\varepsilon_s} x_d^{\,2} = \frac{qnL_g^{\,2}}{8\varepsilon_s} \tag{2-1}$$

As the dopant/carrier concentration is increased, more carriers are trapped at the grain boundary. The curvature of the energy band and the height of potential barrier increase, making carrier transport form one grain to another more difficult. When the dopant/carrier density increases to exceed a critical value $N^* = N_t / L_g$, the poly-Si grains turn to be partially depleted and excess free carriers start to spear inside the grain region. The depletion width and the barrier height can be expressed as

$$x_d = \frac{N_t}{2n} \tag{2-2}$$

$$V_B = \frac{qn}{2\varepsilon_s}\left(\frac{N_t}{2n}\right)^2 = \frac{qN_t^{\,2}}{8\varepsilon_s n} \tag{2-3}$$

The depletion width and the barrier hight turn to decrease with increasing dopant/carrier density, leading to improved conductivity in carrier transport.

The carrier transport in fully depleted poly-Si film can be described by the thermionic emission over the barrier. Its' current density can be written as[4].

$$J = qnv_c \exp[-\frac{q}{kT}(V_B - V)] \tag{2-4}$$

where n is the free-carrier density, v_c is the collection velocity ($v_c = \sqrt{kT / 2\pi m^*}$), V_B is the barrier height without applied bias, and V_g is the applied bias across the grain boundary region. For small applied biases, the applied voltage divided approximately

uniformly between the two sides of a grain boundary. Therefore, the barrier in the forward-bias direction decreases by an amount of $V_g/2$. In the reserve-bias direction, the barrier increases by the same amount. The current density in these two directions then can be expressed as

$$J_F = qnv_c \exp[-\frac{q}{kT}(V_B - \frac{1}{2}V_g]] \tag{2-5}$$

$$J_R = qnv_c \exp[-\frac{q}{kT}(V_B + \frac{1}{2}V_g)] \tag{2-6}$$

the net current density is then given by

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\sinh(\frac{qV_g}{2kT}) \tag{2-7}$$

at low applied voltages, the voltage drop across a grain boundary is small compared to the thermal voltage kT/q, Eq. (1.7) then can be simplified as

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\frac{qV_g}{2kT} = \frac{q^2 nv_c V_g}{kT}[\exp(-\frac{qV_B}{kT})] \tag{2-8}$$

the average conductivity $\sigma = J / E = JL_g / V_g$ and the effective mobility $\mu_{eff} = \sigma / qn$ then can be obtained

$$\sigma = \frac{q^2 nv_c L_g}{kT}\exp(-\frac{qV_B}{kT}) \tag{2-9}$$

$$\mu_{eff} = \frac{qv_c L_g}{kT}\exp(-\frac{qV_B}{kT}) \equiv \mu_0 \exp(-\frac{qV_B}{kT}) \tag{2-10}$$

where μ_0 represents the carrier mobility inside grain regions. It is found that the conduction in poly-Si is an activated process with activation energy of approximately qV_B, which depends on the dopant/carrier concentration and the grain boundary trap density.

Applying gradual channel approximation to poly-Si TFTs, which assumes that the variation of the electric field in the y-direction (along the channel) is much less than the corresponding variation in the z-direction (perpendicular to the channel), as shown Fig 2-2. The carrier density n per unit area (cm^{-2}) induced by the gate voltage can be expressed as

$$n = \frac{C_{ox}(V_G - V_{TH} - V_{(y)})}{qt_{ch}} \tag{2-11}$$

$$I_D = \iint J.dx.dz = \iint nq\mu_{eff}.\frac{dv_y}{dy}.dx.dz \tag{2-12}$$

$$= \int_0^W \mu_{eff}\,dz \int_0^{t_{ch}} nqdx.\frac{dV_y}{dy} = W\mu_{eff}.C_{ox}(V_g - V_{th} - V_y)\frac{dV_y}{dy}$$

where t_{ch} is the thickness of the inversion layer. Therefore, the drain current I_D of poly-Si TFT then can be given by

$$\int_0^L I_D dy = W\mu_{ff}C_{ox}\left[(V_g - V_{th})V_D - \frac{1}{2}V_D{}^2\right]$$

$$I_D = \frac{W}{L}\mu_{ff}C_{ox}\left[(V_g - V_{th})V_D - \frac{1}{2}V_D{}^2\right] \tag{2-13}$$

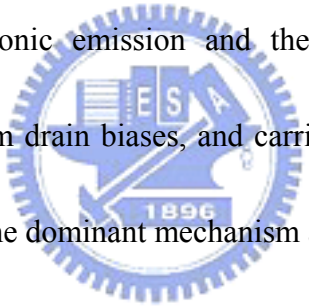
Obviously, this I-V characteristic is very similar to that in MOSFETs, except that the mobility is modified.

2-2. Non-ideal effect

There are three major non-ideal effects will limit the TFTs application, including leakage current, kink-effect and drain induced barrier lowering (DIBL). The mechanism of these three non-ideal effects is described briefly as bellow.

2-2-1. Leakage current

In AMLCD, TFTs play a switching device to turn ON/OFF the current path for charging/discharging the liquid crystal capacitor. Thus, the leakage current should be low enough to remain a pixel gray level before it must be refreshed. The leakage current mechanism in poly-Si has been studied by Olasupe[5]. The leakage current resulted from carrier generation from the poly-Si grain boundary defects. There are three major leakage mechanisms, as shown in Fig. 2-3. The dominant mechanism is a function of the prevailing drain bias. They pointed out carrier generation from grain boundary defects via thermionic emission and thermionic field emission to be prevalent at a low and medium drain biases, and carrier pure tunneling from poly-Si grain boundary defects to be the dominant mechanism at higher drain bias.



2-2-2. Kink effect[6]

During devices operation, a high field near the drain could induce impact ionization there. Majority carriers, holes in the p-substrate for an n-channel poly-Si TFTs, generated by impact ionization will be stored in the substrate, since there is no substrate contact to drain away these charges. Therefore the substrate potential will be changed and will result in a reduction of the threshold voltage. This, in turn, may cause an increase or a kink in the current-voltage characteristics. The kink

phenomenon is shown in Fig 2-4. This float-body or kink effect is especially dramatic for n-channel devices, because of the higher impact-ionization rate of electrons. The kink effect can be eliminated by forming a substrate contact to the source of the transistor.

2-2-3. Drain induced barrier lowering (DIBL)[6]

In a short channel MOSEFT, when the drain voltage increase from the linear region toward the saturation region, its threshold voltage becomes smaller (see figure 2-5). This effect is called drain-induced barrier lowering (DIBL). The effect is also observed in short channel poly-Si TFTs. The surface potentials between source and drain for several n-channel devices with different channel lengths are shown in Fig 2-6. The dotted lines are for Vds = 0 and the solid lines for Vds > 0. When the gate voltage is below Vth, the p-Si substrate forms a potential battier between n+ source and drain and limits the current flow from source to drain. For a device operated in the saturation region, the depletion-layer width of the drain junction is significantly wider than that of the source junction.

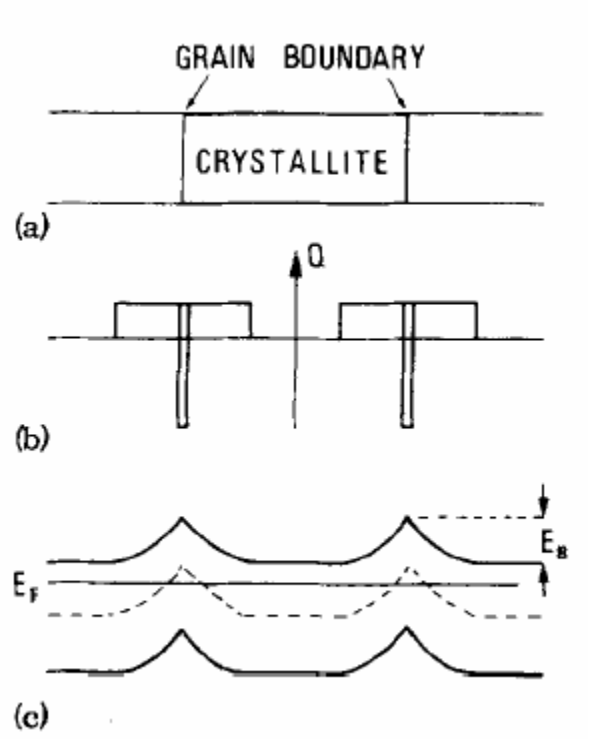


Fig. 2-1 Sketch of the band diagram of the polycrystalline silicon films

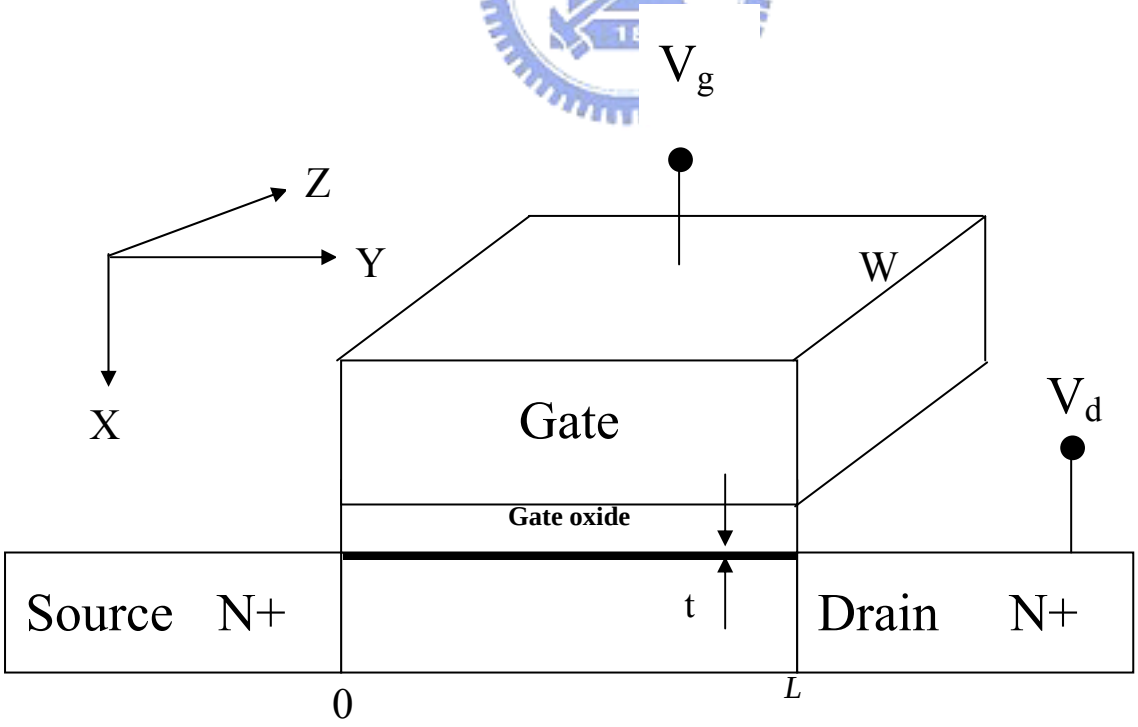


Fig. 2-2 A schematic MOSFET cross section, showing the axes of coordinates and the bias voltages at the four terminals for the drain-current model.

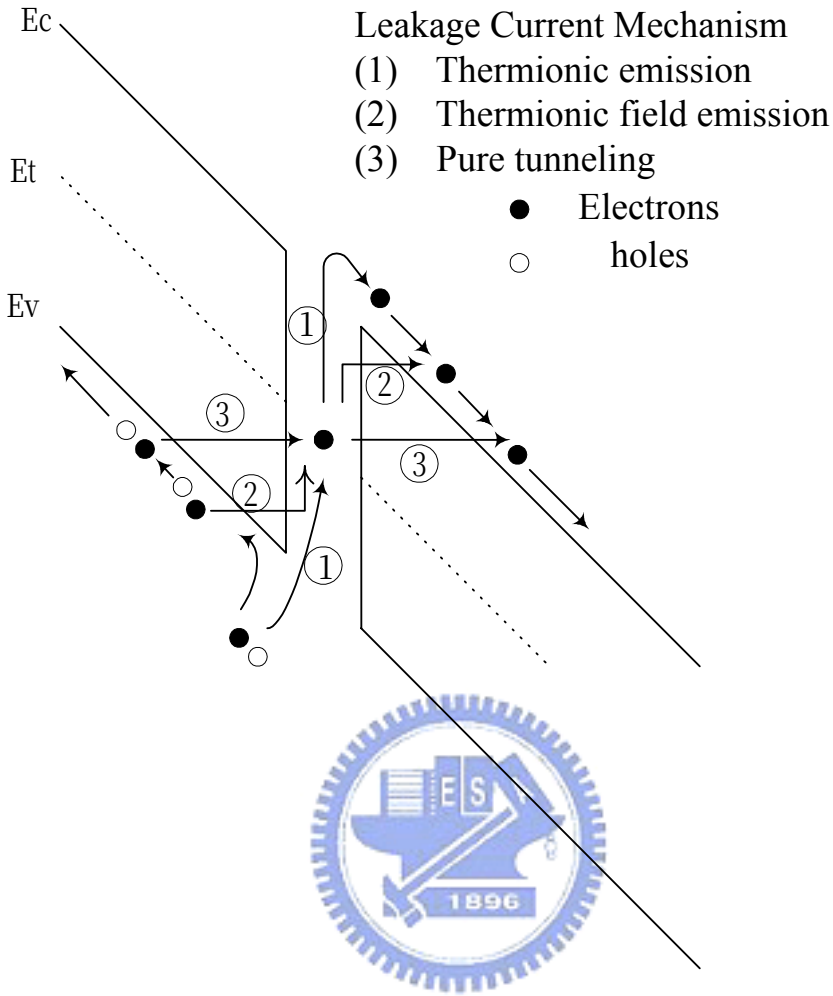


Fig. 2-3 Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling

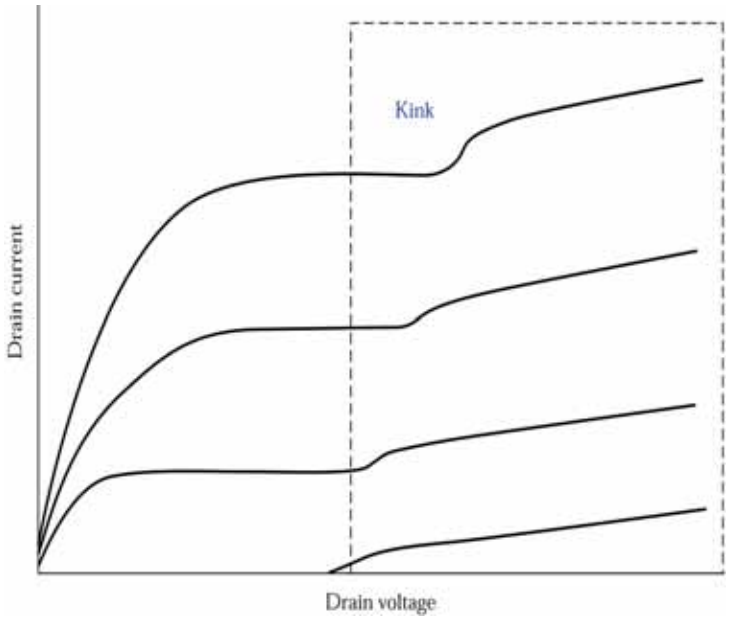


Fig. 2-4 The kink effect in the output characteristics of an *n*-channel SOI MOSFET[6]

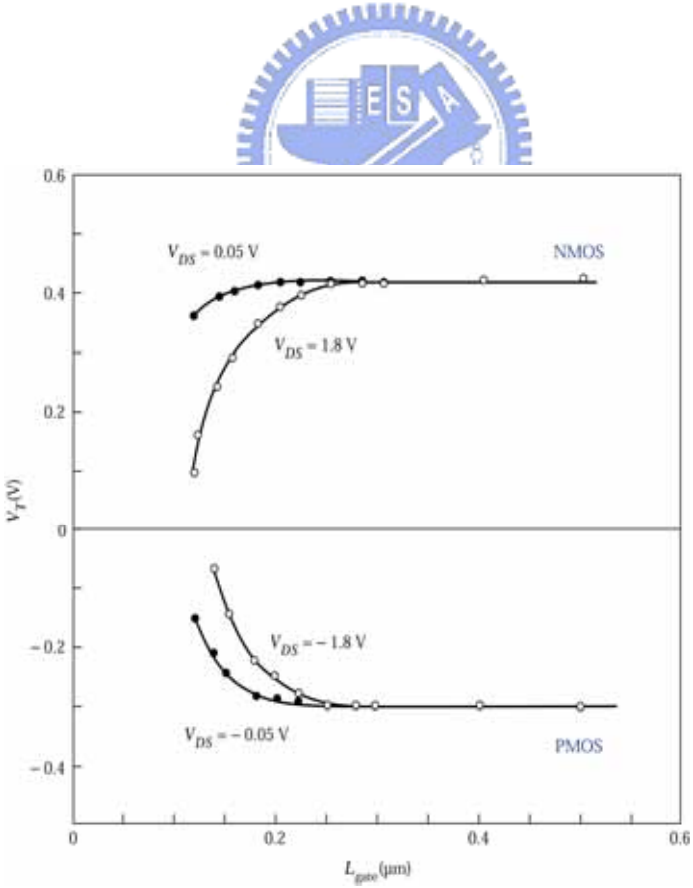


Fig. 2-5.
Threshold voltage roll-off characteristics in a 0.15 μm complementary metal-oxide-semiconductor (CMOS) field-effect transistor technology[6].

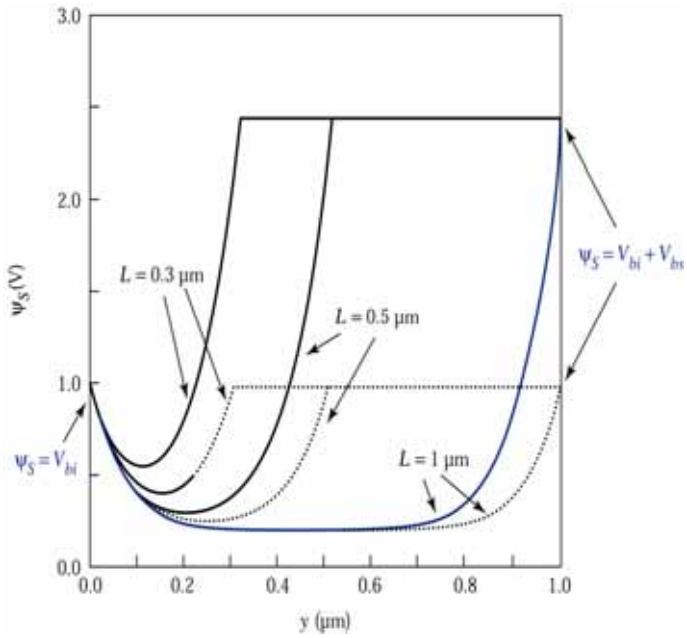


Fig. 2-6 Calculated surface potential along the channel for *n*-channel MOSFETs with different channel lengths. The source-channel boundary is at $y = 0$. A low (0.05 V, dotted lines) and a high (1.5 V, sold lines) V_{DS} are applied. Oxide thickness d and substrate doping N_A are 10 nm and 10^{16} cm^{-3}, respectively. The substrate bias is 0 V[6]

Chapter 3
Experiment

3-1. Fabrication process of Poly-Si TFT

In this thesis, we fabricate the poly-Si TFTs with LDD and multi-channel structure. The top view of the devices is shown in Fig. 3-1 and the schematic cross section view of devices is shown in Fig. 3-2 and in Fig 3-3. The fabrication procedure is described as following. All submicron lithography patterning was performed by using electron-beam (EBeam) direct -writing lithography.

Step1. Substrate.

6-inch p-type single-crystal silicon wafers with (100) orientation were used as the starting substrate. After a standard cleaning procedure, silicon wafers were coated with 400-nm-thick thermally grown SiO_2 in steam oxygen ambient at 1000ºC

Step2. Poly-Si thin film formation .

Undoped 50-nm-thick amorphous-Si layers were deposited by low pressure chemical vapor deposition (LPCVD) at 550ºC. The amorphous-Si films were recrystallized by solid phase crystallization (SPC) method at 600ºC for 24hrs in N_2 ambient. After Ebeam direct writing and transformer couple plasma (TCP) etching,

the device active region source, drain and multiple channels were formed.

Step3. Gate oxide formation.

After defining the active region, the wafers were cleaned in H_2SO_4/H_2O_2 and NH_4OH/H_2O_2 solution to remove residue of polymer before gate oxide deposition. A buffered HF dip was performed to remove the native oxide on the silicon surface. Then, a 26-nm-thick layer of tetra-ethyl-ortho-silicate (TEOS) gate oxide was deposited by LPCVD at 700^0C. The thickness of gate oxide was determined by N&K optical analyzer.

Step4. Gate electrode formation.

After deposition of gate insulators, 150-nm-thick poly-silicon films were formed immediately on the gate insulators by LPCVD at 620°C. The second poly-Si layers were patterned by EBeam lithography and transformer couple plasma (TCP) etching to define the gate electrode and to be the mask for self-aligned implantation.

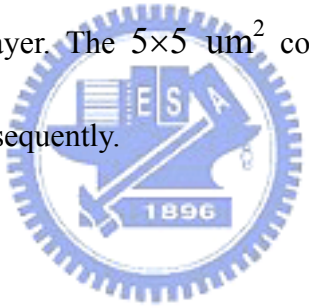
Step5. LDD and source/drain formation.

After the gate definition, the implantation for lightly-doping source and drain was performed by phosphorous ions at a dosage of 5×10^{13} cm^{-2}. A 200nm-thick TEOS

was then deposited by LPCVD, and anisotropically etched by reactive ion etching (RIE) to form a sidewall spacer abutting the poly-Si gate. Next, the self-aligned source and drain regions were formed by phosphorous ions implantation at a dosage of 5×10^{15} cm^{-2}. After the source and drain formation, doping activation was performed by rapid thermal anneal (RTA).

Step6. Passivation layer and contact hole formation.

After doping activation, a 300-nm-thick TEOS oxide layer was deposited by LPCVD as the passivation layer. The 5×5 um^2 contact holes were patterned by reactive ion etching (RIE) subsequently.



Step7. Metallization.

The 300-nm-thick aluminum layers were deposited by physical vapor deposition (PVD) and then patterned to form the gate, source and drain contact metal pads. Finally, the devices were sintered at 400°C in hydrogen ambient for 30 min.

Step8. Passivation.

It is well known that grain boundary passivation is very effective in improving the performance of poly-Si TFTs. Therefore, to reduce trap density and improve

interface quality, wafers were immured in an NH_3 plasma generated by plasma enhanced CVD (PECVD) for 1 hr.

Device table

This investigation proposes TFTs with a gate length of 0.5um consist of ten strips multiple 67 nm wire channels (M10), five strips multiple 0.18um channels (M5), two strips 0.5um channels (M2) and a single-channel structure (S1) with W = 1 um were fabricated and all listed in table I.

3-2. Device parameter extraction

In this section, we will introduce the methods of typical parameters extraction such as threshold voltage (V_{th}), subthreshold slope (SS), drain current ON/OFF ratio**,** field-effect mobility (μ_{FE}), drain induced barrier lowering (DIBL) and the trap density (Nt) inside the channel.

3-2-1. Determination of the threshold voltage

Many ways are used to determinate the V_{th} which is the most important parameter of semiconductor devices. In poly-Si TFTs, the method to determinate the threshold voltage is *constant drain current method.* The gate voltage at a specific

drain current I_N value is taken as the threshold voltage. This technique is adopted in most studies of TFTs. Typically, the threshold current $I_N = I_D / (W_{eff} / L_{eff})$ is specified at 10 nA for V_D = 0.05V (linear region) and 100 nA for V_D = 2V (saturation region) in this thesis.

3-2-2. Determination of the subthreshold slope

Subthreshold slope *SS* (V/dec.) is a typical parameter to describe the gate control toward channel. The SS should be independent of drain voltage and gate voltage. However, in reality, SS might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punchthrough-like effect. The SS is also related to gate voltage due to undesirable factors such as serial resistance and interface state. In this experiment, the SS is defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude (from 10^{-8}A to 10^{-10}A).

3-2-3. Determination of On/Off Current Ratio

Drain On/Off current ratio is another important factor of TFTs. High On/Off ratio represents not only large turn-on current but also small off current (leakage current). It affects gray levels (the bright to dark state number) of TFT AMLCD directly.

There are many methods to specify the on and off current. The practical one is to define the maximum current as on current and the minimum leakage current as off current while drain voltage is applied at 2V.

3-2-4. Determination of the field-effect mobility

The field-effect mobility (μ_{FE}) is determined from the transconductance (g_m) at low drain voltage (Vd = 0.05V). The transfer I-V characteristics of poly-Si TFT can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D^2] \quad (3\text{-}1)$$

where

C_{ox} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{th} is the threshold voltage.

If V_D is much smaller than V_G-V_{th} (i.e. $V_D << V_G$-V_{th}) and $V_G > V_{th}$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{th})V_D \quad (3\text{-}2)$$

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D \quad (3\text{-}3)$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \tag{3-4}$$

3-2-5. Determination of the drain induced barrier lowering

Drain induced barrier lowering (DIBL) is another important parameter to describe the gate electrode controllability toward channel. It is defined that the gate voltage difference between Vd = 0.05 V and Vd = 2 V divide the drain voltage difference, when the drain current is equal to 10^{-10} A.

3-2-6. Determination of the poly-Si grain boundary trap density

As described in Eq. (2-3), the grain boundary potential barrier height V_B is related to the carrier concentrations inside the grain and the trapping states located at grain boundaries. Based on this consideration, the amount of trap state density N_t can be extracted from the current-voltage characteristics of poly-Si TFTs. As proposed by Levinson *et al*[1], the *I-V* characteristics including the trap density can be obtained by :

$$I_D = \mu_0 C_{ox} \frac{W}{L} (V_G) V_D \exp\left(-\frac{q^3 N_t^{\,2} t_{ch}}{8kT\varepsilon_s C_{ox}(V_G)}\right) \tag{3-5}$$

The effective trap state density then can be obtained from the slope of the curve $ln[I_D/(V_G)]$ versus $(V_G)^{-1}$.

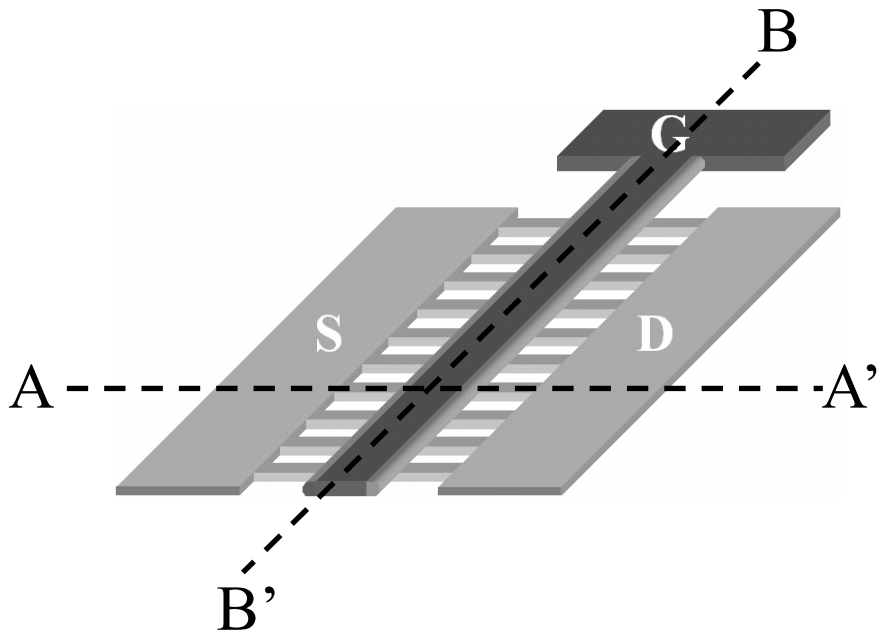


Fig. 3-1 The top view of the multiple nano-wire channel

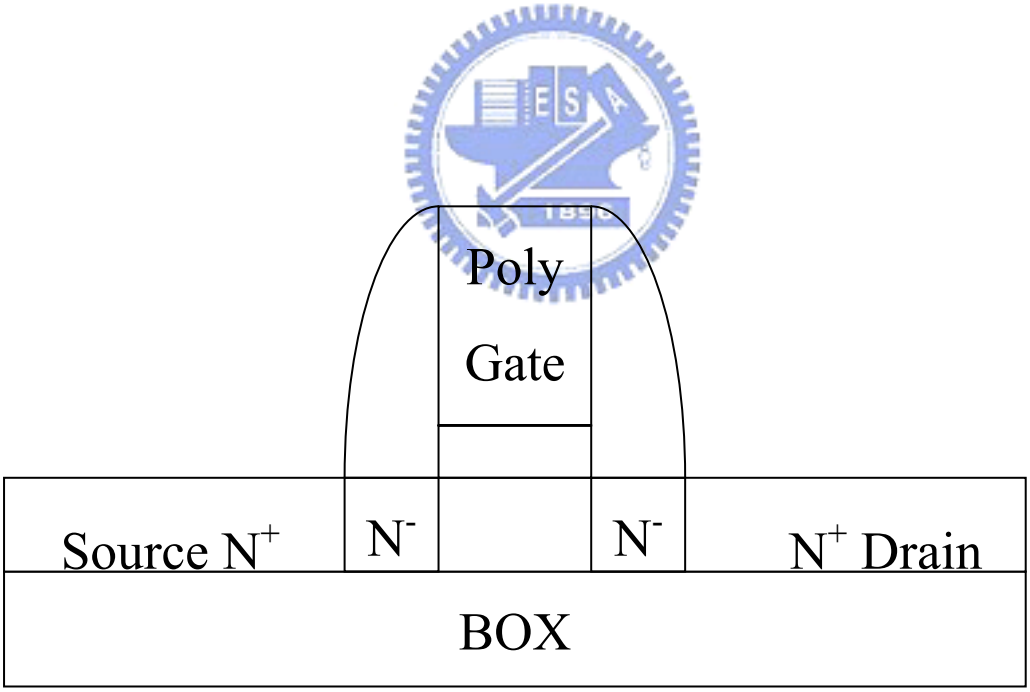


Fig. 3-2 Cross-section view of Fig. 3-1 AA' direction.

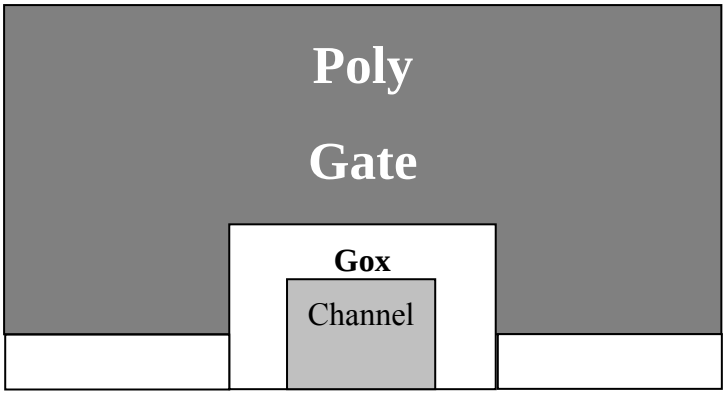


Fig. 3-3 One of channel cross-section view of Fig. 3-1

Table I.

Table I Devices dimension of M10, M5, M2 and S1. All devices have the same active channel thickness 50nm and gate oxide thickness 26nm.

Device name	Gate length L	Channel number	Each channel width W
M10	0.5um	10	67nm
M5	0.5um	5	0.18um
M2	0.5um	2	0.5um
S1	0.5um	1	1um

Chapter 4

Experiment results and discussion

4-1. Gate controllability with different multiple channel number and width of poly-Si Thin-Film Transistor

Fig. 4-2a presents a after etching investigation (AEI) scanning electron microscopy (SEM) photograph of the poly-Si active region in the TFTs, including the source, the drain and ten multiple nano-wire channels. Fig. 4-2b presents a magnified area of multiple nano-wire channels in the TFTs, each of which is 67 nm wide. Fig. 4-2c presents a plane view of transmission electron micrograph (TEM) photograph of the active region in the proposed TFTs. The average grain size in the poly-Si channel formed by solid phase crystallization is approximately 30 nm. Fig. 4-3 to 4-6 present the electrical characteristics of different channel number and width poly-Si TFTs. Each figure (a) of Fig. 4-3 to 4-6 plots a typical transfer curves, and figure (b) plots output curves of poly-Si TFTs. The M10 transfer characteristic indicates that the ten strips nano-wire channel TFTs has the best performance, including lowest OFF-state leakage current, highest drain current ON/OFF ratio, smallest subthreshold slope (SS) and lowest drain induced barrier lowering (DIBL). On the other hand, in Fig. 4-3(b) to 4-6(b), the kink-effect is reduced form S1 to M10 TFT. The M10 TFT even shows

kink-free characteristics. It implies that the thin 50 nm-thick, and 67nm-wide MNWCHs of M10 are fully depleted by tri-gate structure. Thus, at high drain bias (V_{ds}), the impact ionization is reduced than others TFTs. For investigation of devices process variation, five TFTs in different area on the 6-inch wafer were taken into account. Table II lists all poly-Si TFT parameters, including average and standard deviation values of field effect mobility (μ_{FE}), ON/OFF ratio, threshold (V_{th}), subthreshold slope (SS), and drain induced barrier lowering (DIBL). μ_{FE} is extracted from linear region (V_d = 0.05V) transcendence g_m. V_{th} is defined as the gate voltage required to achieve a normalized drain current of I_d / (W/L) = 10^{-7} A at V_d = 2 V. I_{ON} is defined of maximum drain turn on current at Vd = 2V. I_{OFF} is defined drain turn off current at V_g = -3V and Vd = 2V. Thus, ON/OFF ratio is defined as I_{ON} / I_{OFF}. DIBL is defined as ΔV_g / ΔV_d at I_d = 10^{-10} A at V_d = 2 V. Fig. 4-7 shows the TFTs μ_{FE} versus different channel and width relation. This fact shows that the M10, M5, M2 and S1 poly-Si TFTs can yield almost the same carrier mobility, indicating that the carrier mobility and turn on current are not degraded in different channel number structure TFTs. Fig. 4-8 shows the TFTs ON/OFF ratio (left), and leakage current I_{OFF} (right) versus different channel and width relation, respectively. The leakage current is reduced significantly at OFF-state from S1 to M10 TFTs sequentially. It can be explained that the M10 TFT has better gate control over channel than others. As the

result, M10 TFT has lowest lateral and drain electrical field in channel[1], thus the energy band bending is smooth in drain depletion region. So that the I_{OFF} which generated from field emission and tunneling current is reduced most significantly. Therefore, M10 TFT has a highest ON/OFF ratio (>10^9) than others TFTs. Fig. 4-9 shows the TFTs V_{th} versus different channel and width relation. The average value of each V_{th} is within 0 to 0.2. It should be noted that M10 TFT shows lowest standard deviation value. It implies that M10 TFT forms a relatively stable structure to reduce fabrication variation, which is a key factor for uniform lager-glass AMLCD application. Fig. 4-10 shows the TFTs SS versus different channel and width relation. SS mean values and standard deviations are both increasing with channel numbers. One may notice that M10 TFT shows smallest SS both in average (110mV/dec.) and standard deviation than others. The steep SS of M10 is desirable for the ease of switching the transistor off. The mathematical education of SS could describe as following[2]:

$$SS = \frac{kT}{q} \cdot \ln 10 \cdot (1 + \frac{C_t}{C_{ox}}) \quad (1)$$

where

$$C_{ox} = \frac{\varepsilon_{ox} \cdot \varepsilon_o}{t_{ox}} \quad (2)$$

$$C_t = qN_{b,Si} \cdot t_{Si} + qD_{it} \quad (3)$$

$N_{b,Si}$ is the trap density in the poly-Si layer ($cm^{-3}eV^{-1}$), D_{it} is the interface trap density

at the poly-Si/gate oxide dielectirc film (cm^{-3}). Steep SS of M10 can be explained that M10 has strongest gate control and passivation to reduce $N_{b,Si}$ and D_{it}, and achieve lowest C_t. Fig. 4-11 shows the TFTs DIBL versus different channel and width relation. M10 TFT shows zero of DIBL both in average and standard deviation than others. It can be explained that ten nano-wires of M10 TFT are strongly controlled by its surrounding gate electrode (Fig. 4-1c), and resist the electrical field penetration from the drain electrode[3].

According to Fig. 4-9, 4-10 and 4-11, M10 TFT has best performance in switching application, such that most stable V_{th}, smallest SS, and DIBL–free effect than others. These results can be summarized that M10 TFT its active channels have a best gate controllability due to its tri- gate structure. Energy-band diagram of S1 single–channel TFT and M10 multiple nano-wire channels TFT are shown in Fig. 12 and 13, respectively. Obviously, M10 TFT has additional two-side gates control, hence a better gate controllability than S1 TFT. Furthermore, experiments results also show the gate controllability is increasing with channel number from S1, M2, M5 to M10 resulting its structure from single gate to tri-gate sequentially. Moreover, the effect of NH_3-plasma passivation more efficiently affects M10 than it does other TFTs, because the former has split nano-wire structures that are mostly exposed to NH_3 plasma.

4-2. Stress results of MCH and SCH LDD TFTs

Fig. 4-14 (a)-(d) depict a serious of typical S1 TFT Id-Vg curves after DC stress at 0, 40, 100, 160, 190 min, respectively. Fig. 4-15 (a)-(d) depict a serious of typical M10 TFT Id-Vg at the same stress condition. The stress condition was chosen from the output characteristics when kink effect occurs, i.e. Vd = 6V and Vg = 3V. The stress time is 0, 40, 100, 160, 190 min. According to Fig. 4-1 4(a)-(d), SCH TFT shows serious degradation of DIBL, SS, and leakage current with stress time increasing. On the other hand, Fig. 4-15 (a)-(d) show that M10 TFT has not much degradation such as DIBL, SS, and leakage current. The ON current has light degradation after stress for both M10 and SCH TFTs devices. The aggravated degradation of the Ion/Ioff ratio for SCH TFTs is due to its higher increased leakage current than M10 devices. It is because that the more traps on the ploy-Si grain boundaries are generated by hot carrier impact ionization during the DC stress for S1 TFT. And these extra trap states near the drain will generate extra leakage current. Additionally, M10 has more NH3 passivation due to its split nano-wire structure, and has better gate controllability. Therefore, M10 exhibits a better stress endurance than S1 TFT.

For further understanding the TFT's performance degradation with channel width effect related to stress duration. The mobility, ON/OFF, V_{th} and SS, after DC

stress duration for S1, M2, M5 and M10 are displayed in Fig. 4-16 to Fig. 4-19, respectively. Experimental electronic parameters and corresponding possible degradation mechanics are listed in table III[4]. Fig. 4-16 shows field effect mobility variation of M10 M5, M2 and S1 TFTs with stress duration. It implies that field effect mobility of all TFT has the identical degradation behavior. It can be explained that all TFT's generate equal tailed states. Fig. 4-17 shows ON/OFF ratio variation of M10 M5, M2 and S1 TFTs with stress duration. From the result, ON/OFF ratio of all TFT has the identical degradation behavior. It also can be explained that all TFT's generate equal tailed states. In addition, M10 has higher ON/OFF ratio due to its initial status. Fig. 4-17 and 4-18 show V_{th} and SS with stress duration, respectively. From the results, Vth and SS of M10 TFT are keeping in constant after stress duration. In table III, the V_{th} and SS variation mainly depend on the number of deep states. It was believed that the deep states were generated from the poly-Si grain boundary breaking bonds. Therefore, M10 TFT's surrounding gate structure can effectively decreases the lateral electric field, which is responsible for V_{th} and SS invariant under stress duration.

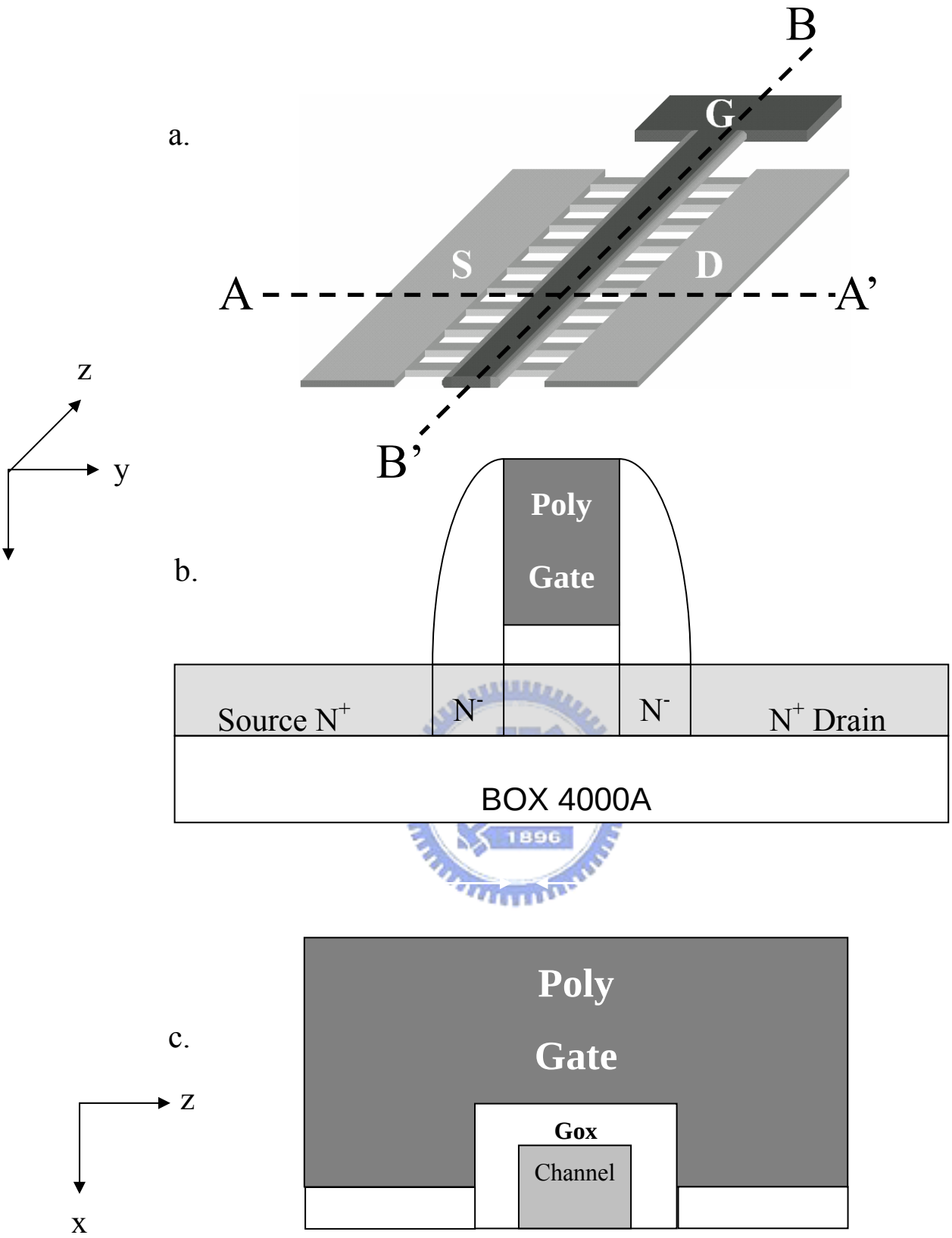


Fig. 4-1 (a) Schematic diagram of M10 poly-Si TFT.

(b) Cross-section view of Fig. 1a AA' direction.

(c) One of channel cross-section view of Fig. 1a BB' direction.

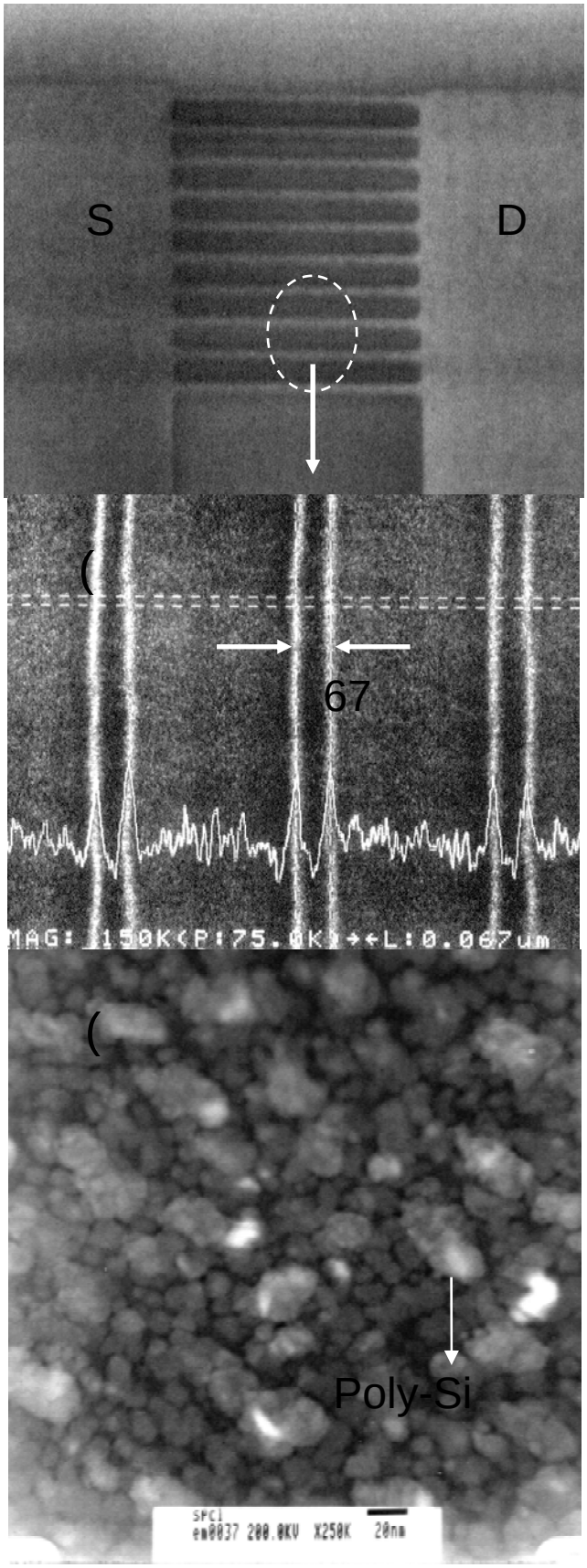


Fig. 4-2 (a) Scanning electron microscopy photography of active pattern with the source, the drain and multiple nano-wire channels of M10 TFT. (b) Magnified area of multiple nano-wire channels. The each nano-wire width is 67 nm. (c) Transmission electron microscopy photography of poly-Si grains by solid phase crystallization. The average poly-Si grain size is about 30 nm.

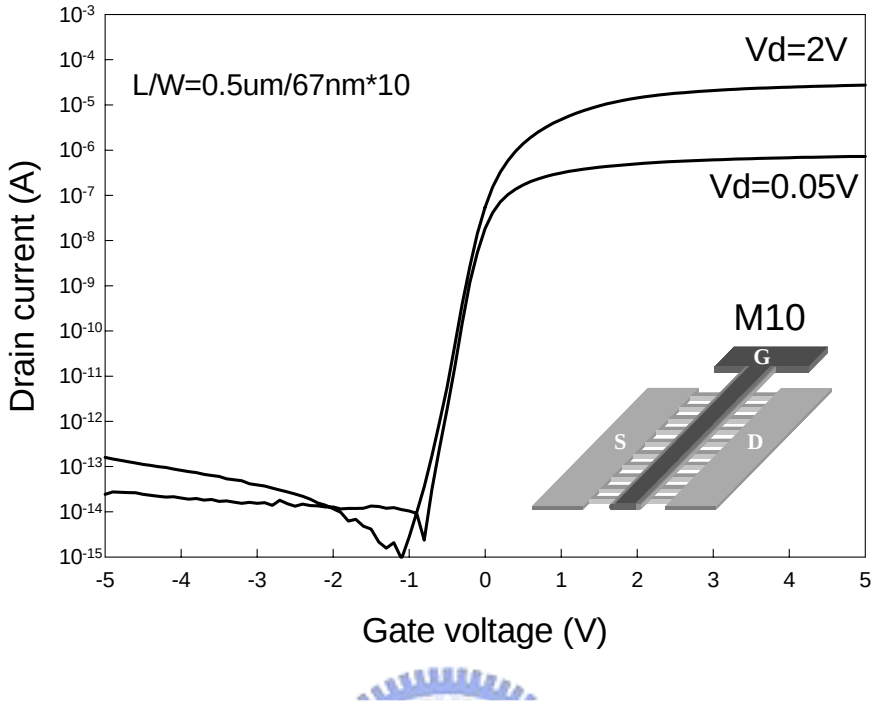


Fig. 4-3a I_d-V_g characteristics of M10 (L/W = 0.5um/67nm×10) poly-Si TFT.

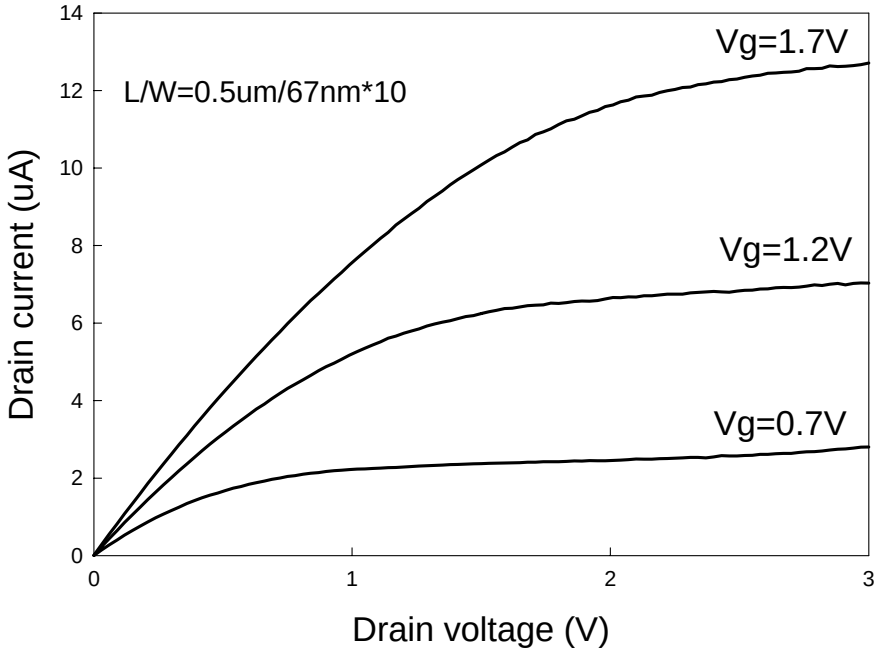


Fig. 4-3b I_d-V_d. characteristics of M10 (L/W = 0.5um/67nm×10) poly-Si TFT.

.

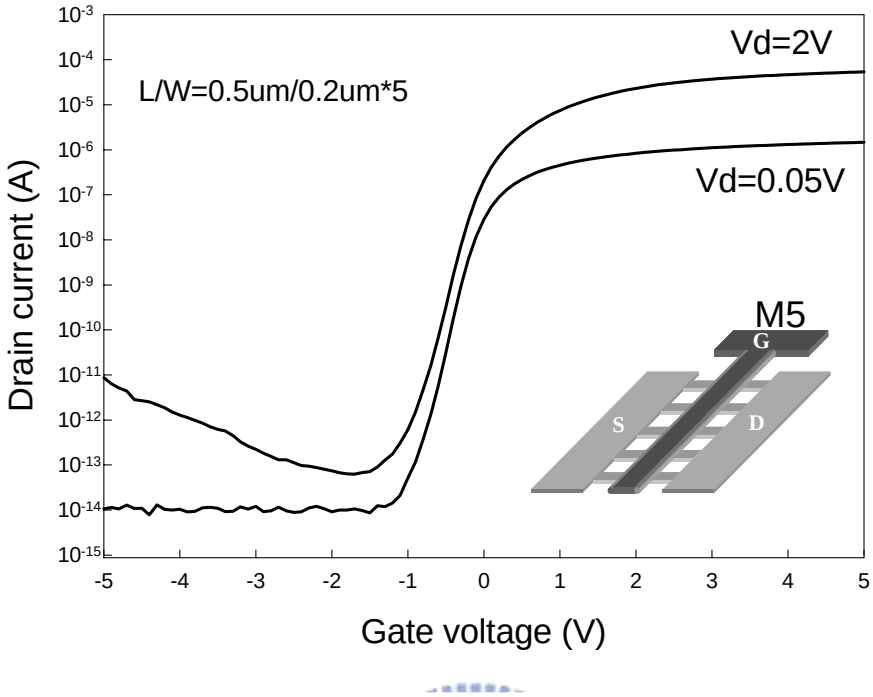


Fig. 4-4a I_d-V_g characteristics of M5 (L/W = 0.5um/0.18um×5) poly-Si TFT.

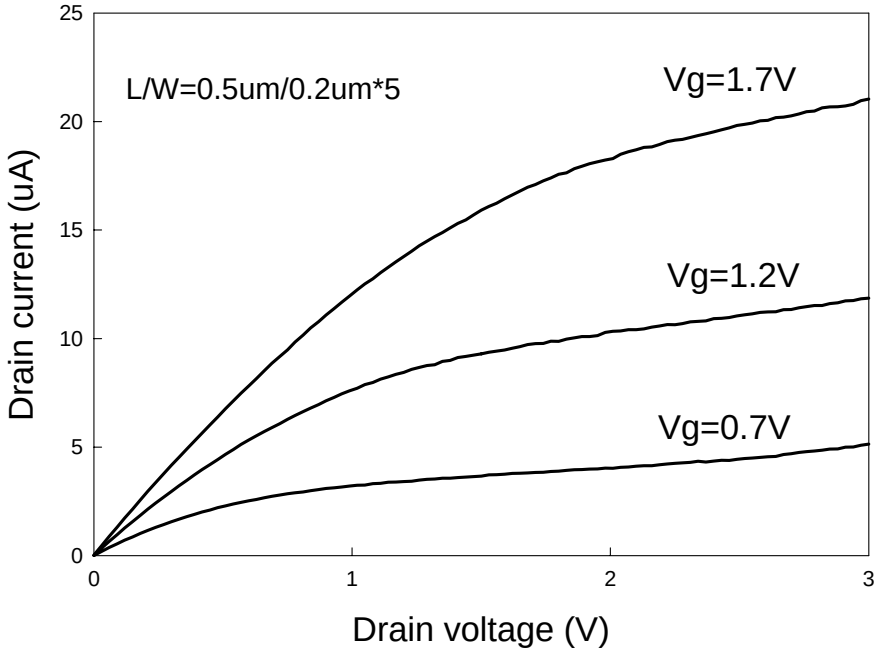


Fig. 4-4b I_d-V_d. characteristics of M5 (L/W = 0.5um/0.18um×5) poly-Si TFT.

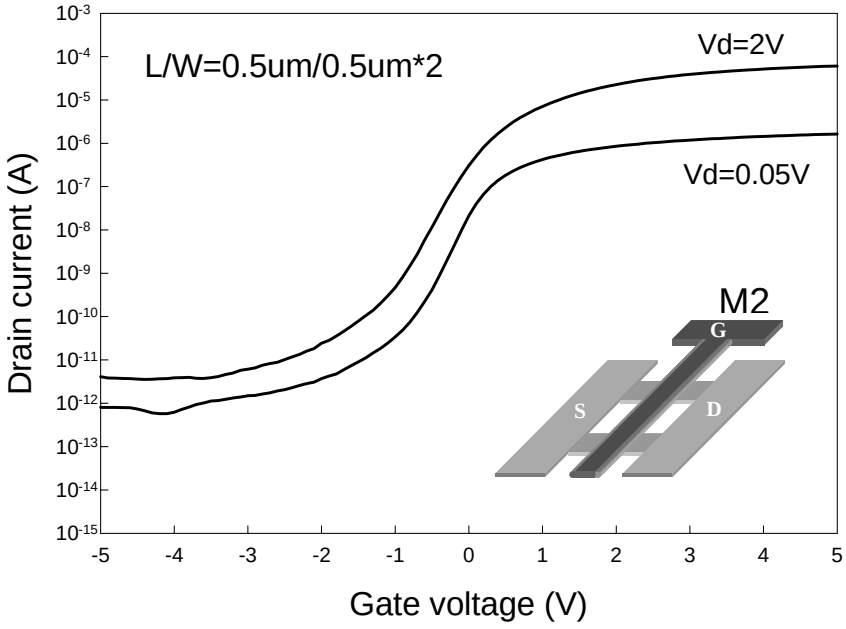


Fig. 4-5a I_d-V_g characteristics of M2 (L/W = 0.5um/0.5um*2) poly-Si TFT.

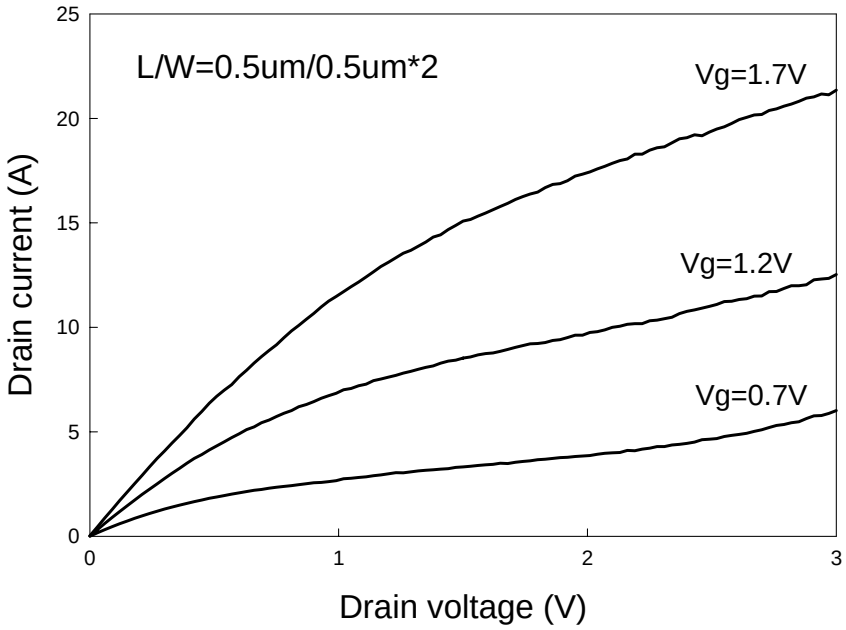


Fig. 4-5b I_d-V_d. characteristics of M2 (L/W = 0.5um/0.5um*2) poly-Si TFT.

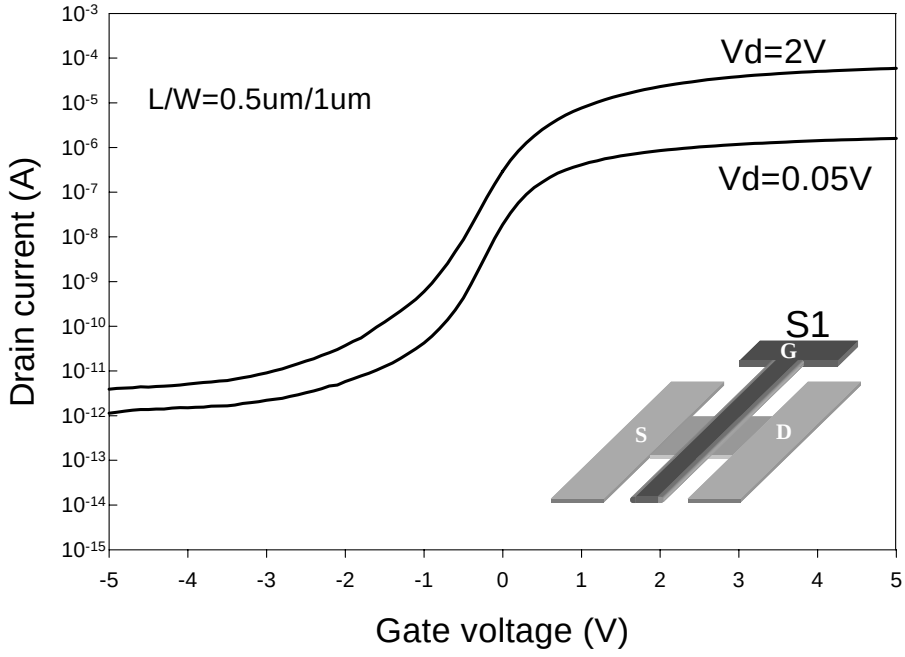


Fig. 4-6a I_d-V_g characteristics of S1 (L/W = 0.5um/1um) poly-Si TFT.

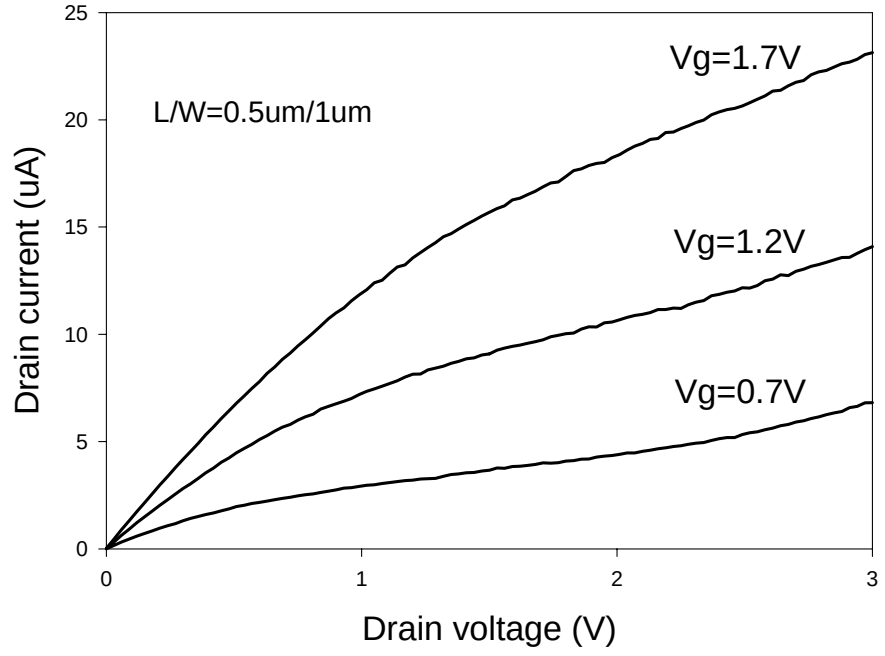


Fig. 4-6b I_d-V_d characteristics of S1 (L/W = 0.5um/1um) poly-Si TFT.

Table II　Device average and standard deviation parameters of M10, M5, M2 and S1. Number inside the bracket is parameter's standard deviation. All parameters were extracted at V_d = 2V, except for the field-effect mobilities which were extracted at V_d = 0.05V.

	Mobility (cm^2/VS)	V_{th} (V)	SS (mV/dec.)	Ion / Ioff	DIBL (V/V)
M10	37.95 (3.97)	0.15 (0.11)	137 (23)	7.36×10^9	0
M5	41.77 (3.91)	0.06 (0.15)	172 (56)	1.60×10^9	0.06(0.02)
M2	37.21 (2.88)	0.11(0.39)	324 (75)	6.69×10^7	0.25(0.09)
S1	38.44 (3.39)	0.03 (0.23)	334 (140)	2.23×10^7	0.32(0.09)

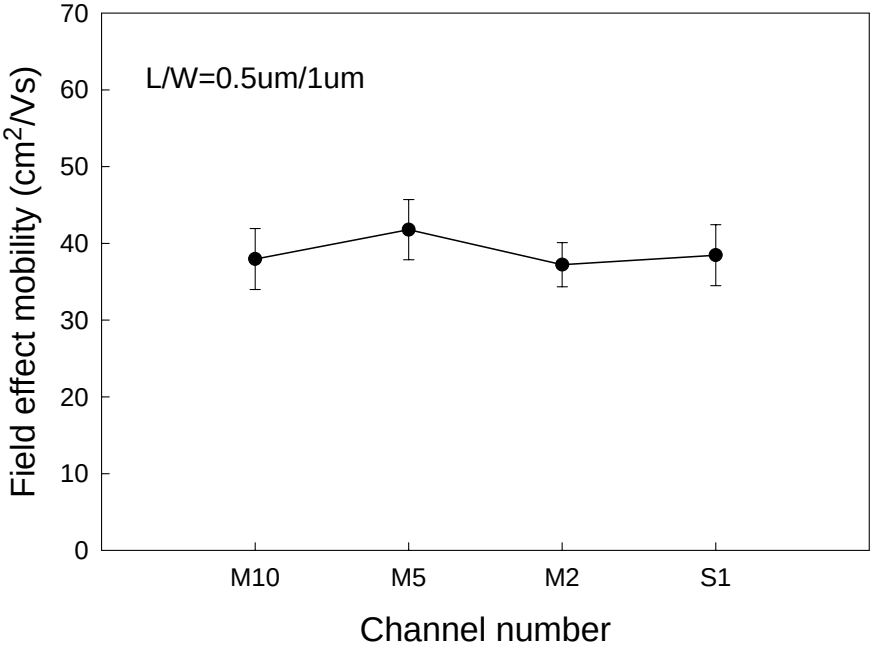


Fig. 4-7 Field effect mobility (μ_{FE}) versus different channel number poly-Si TFTs. The dots value present average value and error bars present standard deviation.

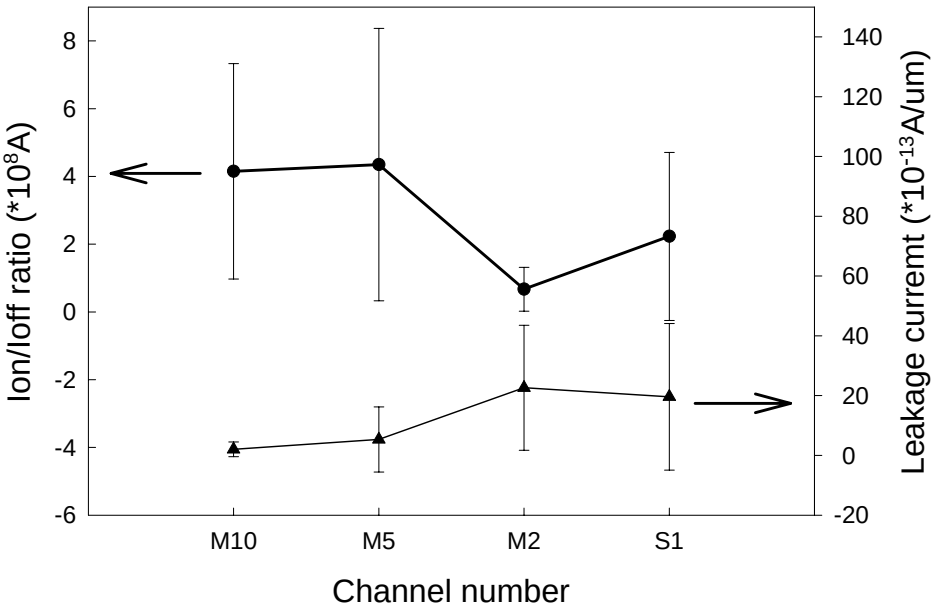


Fig. 4-8 Drain current maximum ON/OFF ratio (R) versus different channel number poly-Si TFTs.

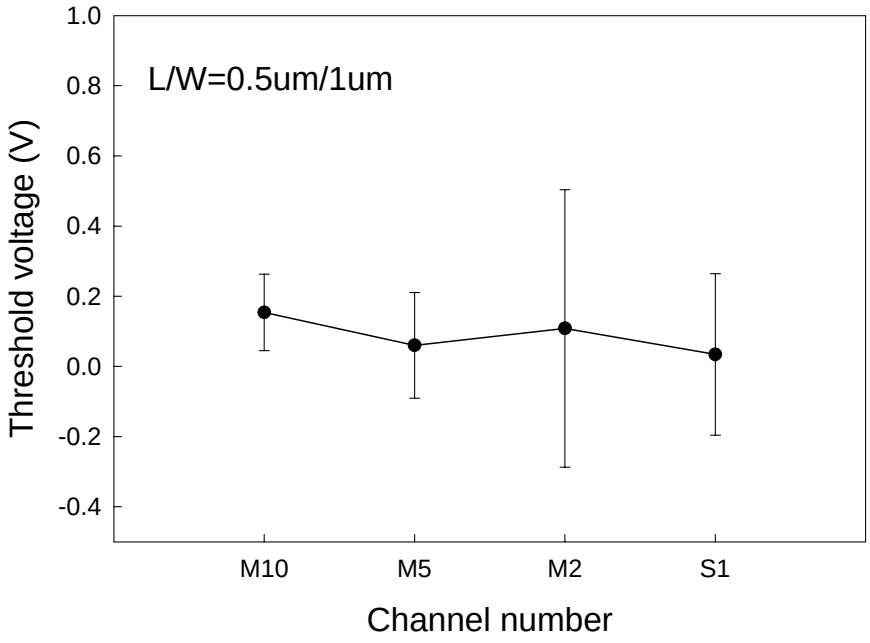


Fig. 4-9 Threshold voltage (V_{th}) versus different channel number poly-Si TFTs.

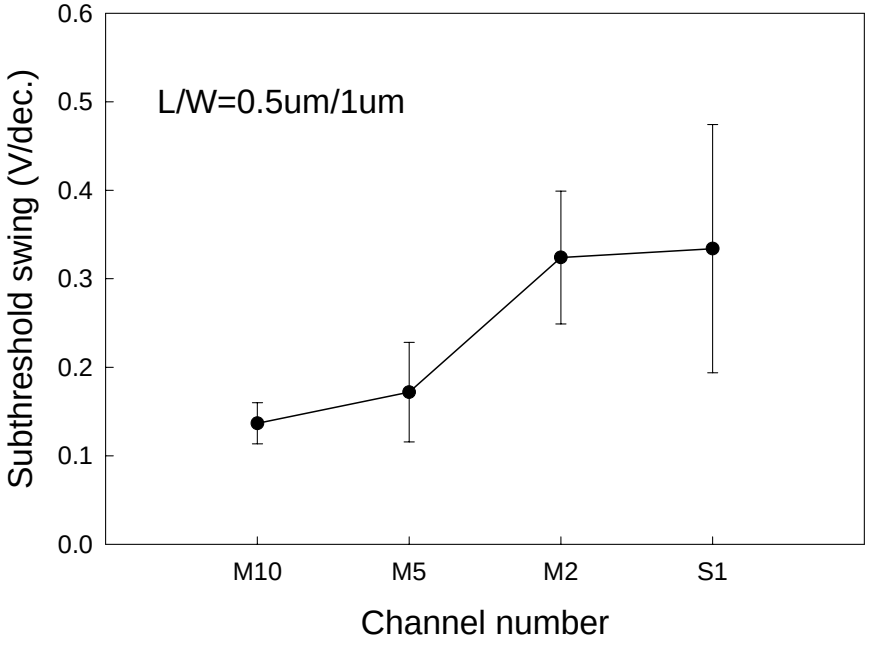


Fig. 4-10 Subthreshold slope (SS) versus different channel number poly-Si TFTs.

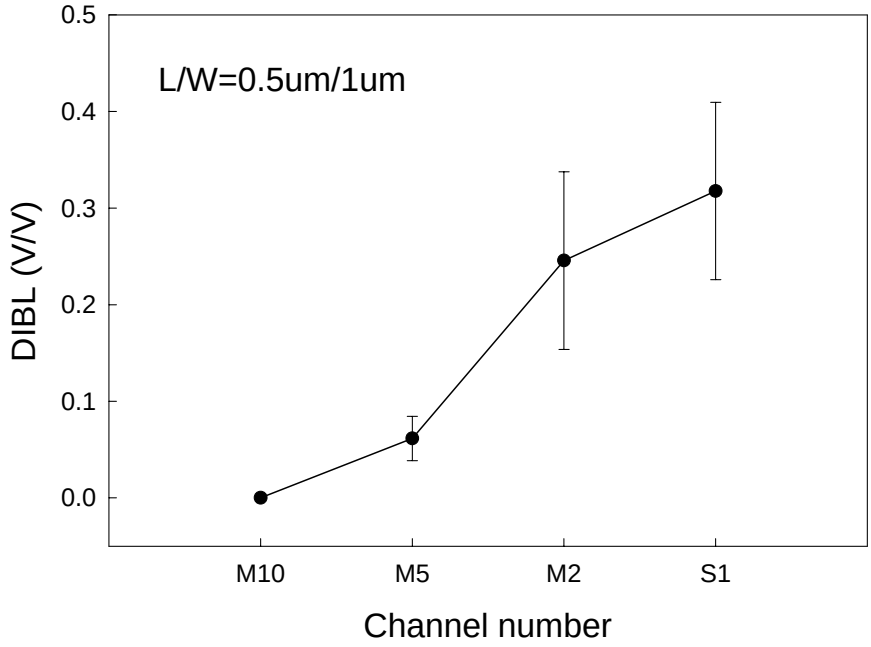


Fig. 4-11 Drain current maximum ON/OFF ratio (R) versus different channel number poly-Si TFTs.

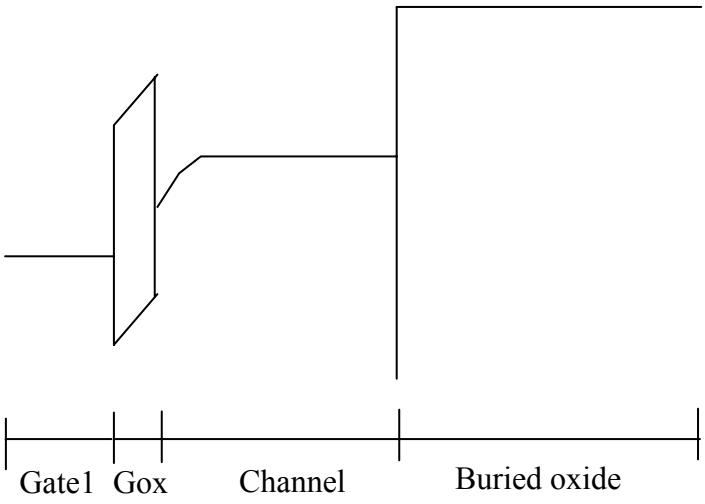


Fig. 4-12 Energy-band diagram of top-gate single channel TFT.

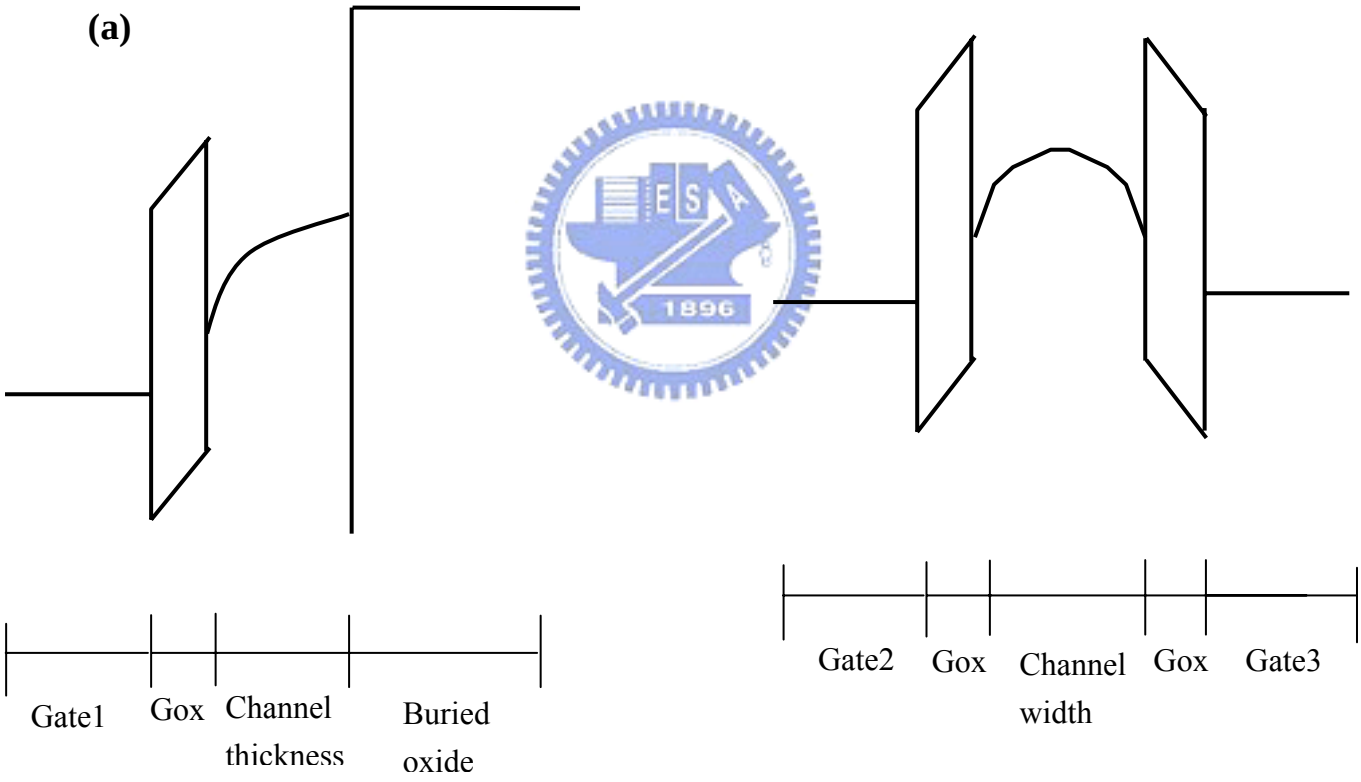


Fig. 4-13 Energy band diagram of top-gate M10 TFT. According its tri-gate structure, M10 TFT will include (a) top-gate, and (b) 2 side-gates energy-band diagram.

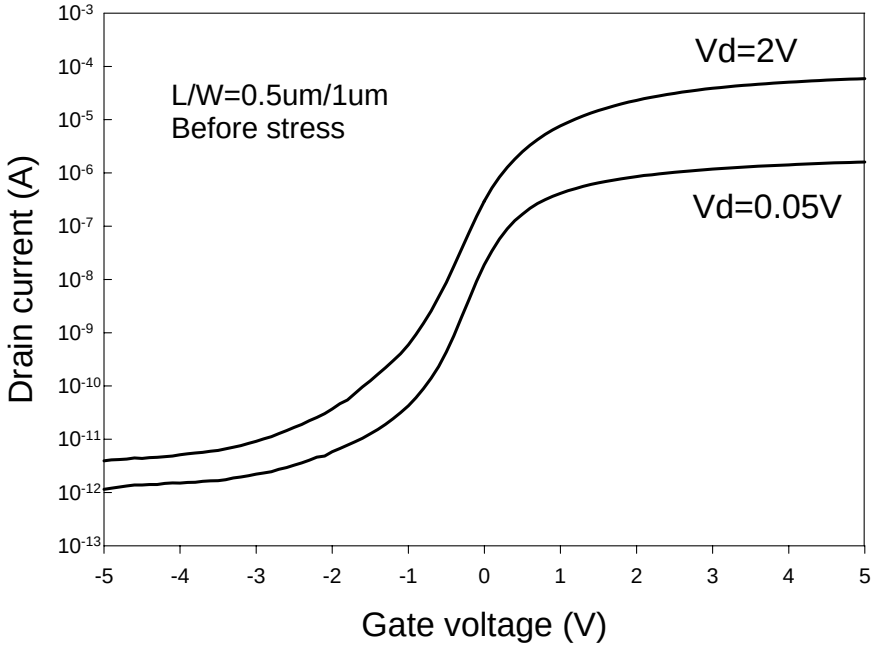


Fig. 4-14a I_d-V_g characteristics of S1 (L/W = 0.5um/1um) poly-Si TFT, before stress.

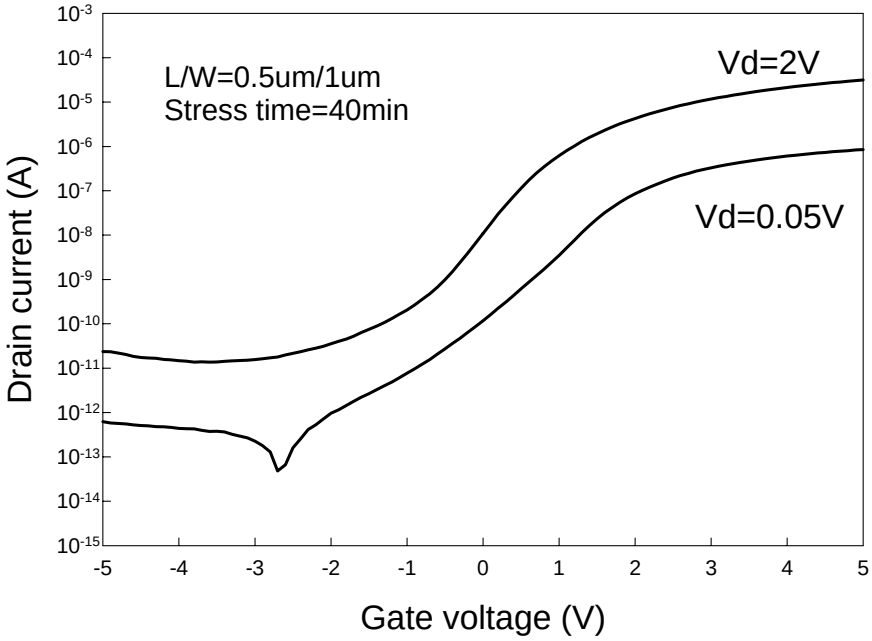


Fig. 4-14b I_d-V_g characteristics of S1 (L/W = 0.5um/1um) poly-Si TFT, after stress time 40 min. with stress condition V_g = 3V *and* V_d = 6V.

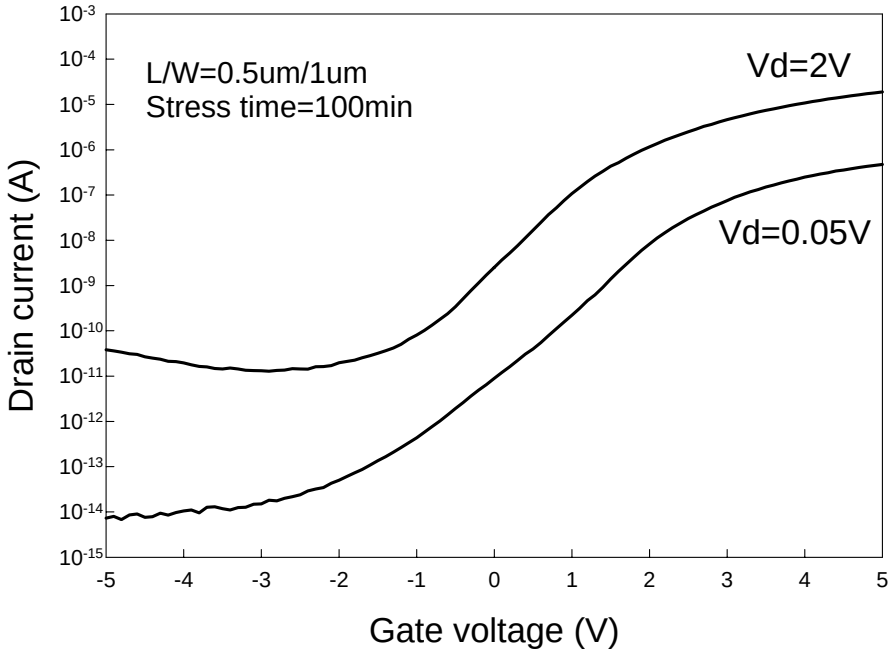


Fig. 4-14c I_d-V_g characteristics of S1 (L/W = 0.5um/1um) poly-Si TFT, after stress time 100 min. with stress condition V_g = 3V *and* V_d = 6V.

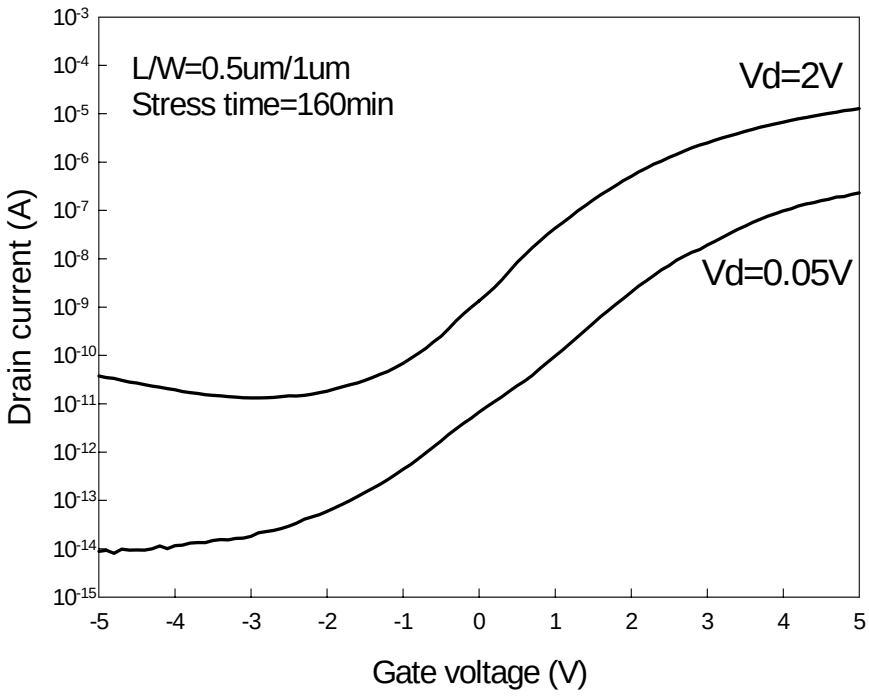


Fig. 4-14d I_d-V_g characteristics of S1 (L/W = 0.5um/1um) poly-Si TFT, after stress time 160 min. with stress condition V_g = 3V *and* V_d = 6V.

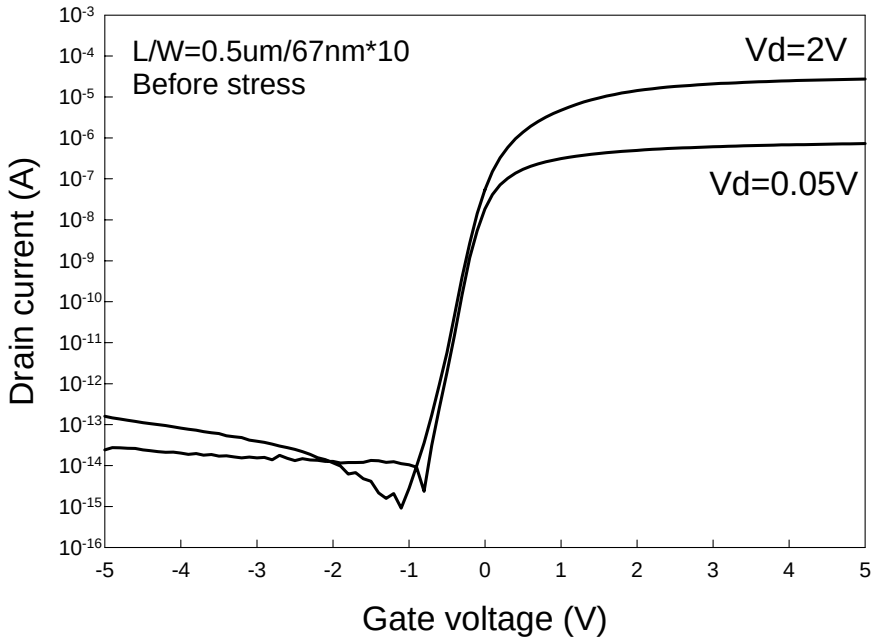


Fig. 4-15a I_d-V_g characteristics of M10 (L/W = 0.5um/67nm*10) poly-Si TFT, before stress with stress condition V_g = *3*V *and* V_d = *6*V.

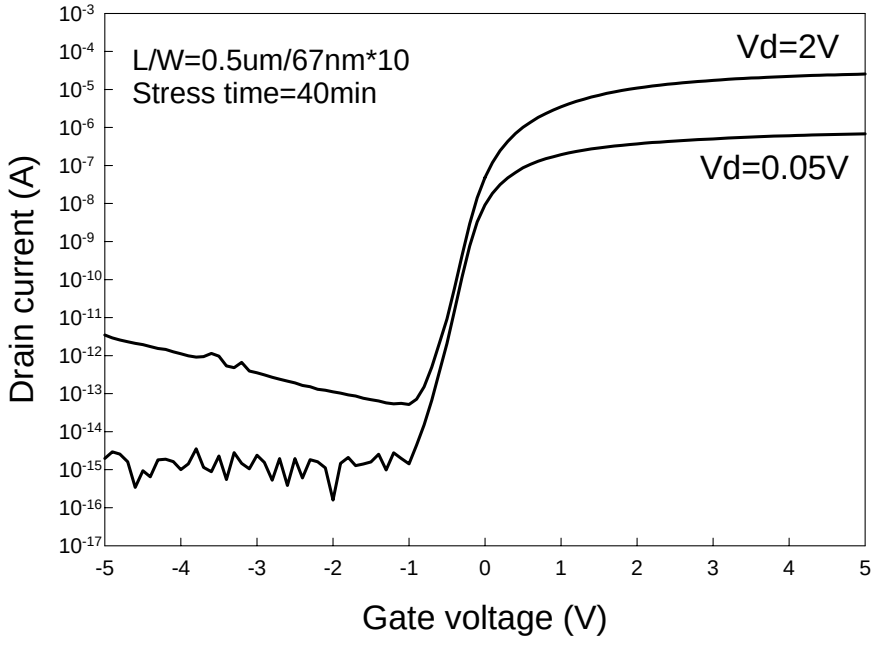


Fig. 4-15b I_d-V_g characteristics of M10 (L/W = 0.5um/67nm*10) poly-Si TFT, after stress time 40 min. with stress condition V_g = *3*V *and* V_d = *6*V.

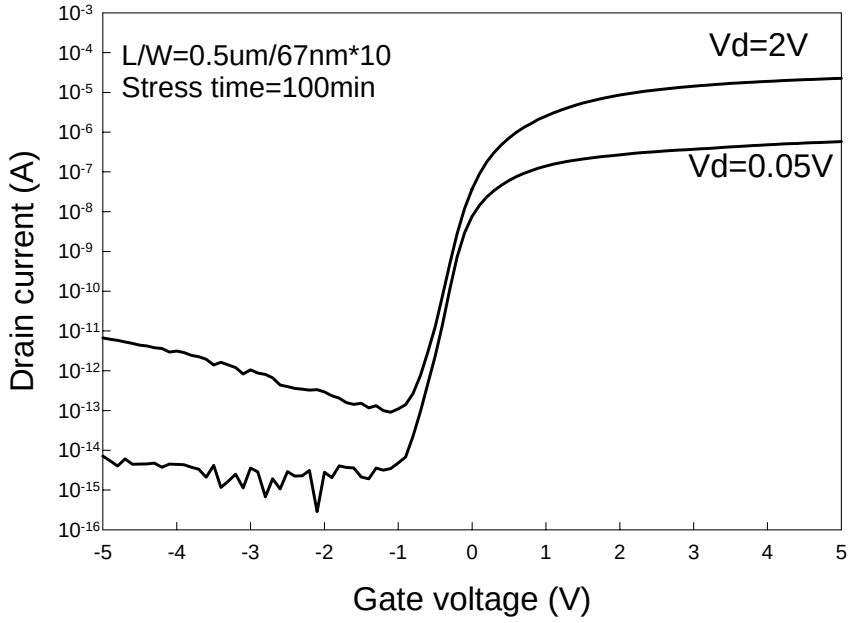


Fig. 4-15c I_d-V_g characteristics of M10 (L/W = 0.5um/67nm*10) poly-Si TFT, after stress time 100 min. with stress condition V_g = *3V and* V_d = *6*V.

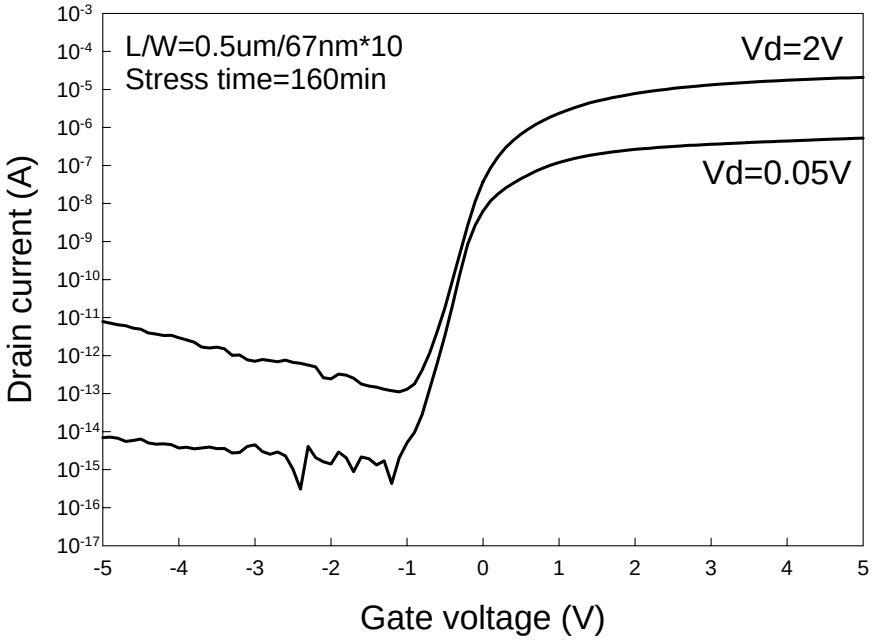


Fig. 4-15d I_d-V_g characteristics of M10 (L/W = 0.5um/67nm*10) poly-Si TFT, after stress time 160 min. with stress condition V_g = *3*V *and* V_d = *6V.*

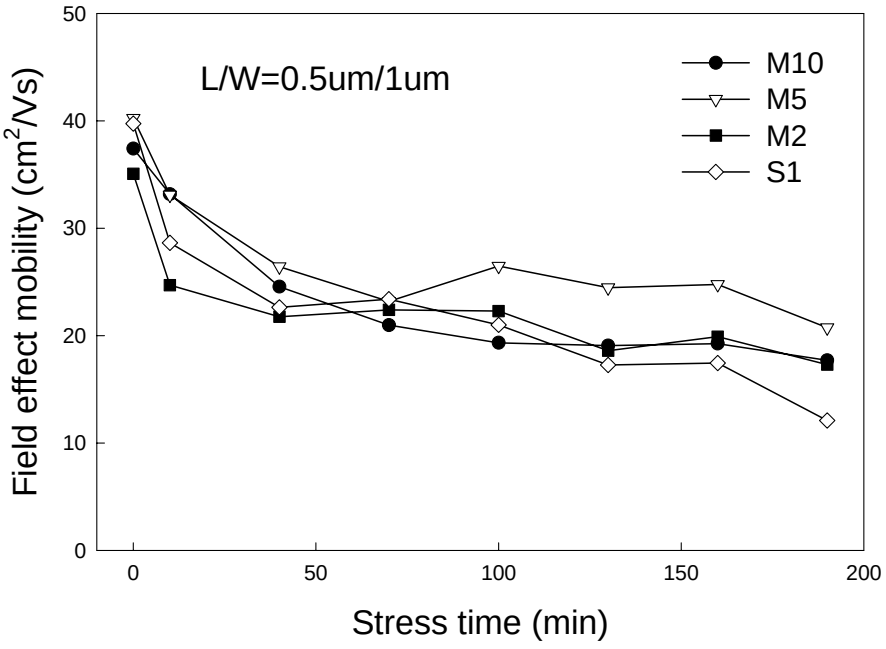


Fig. 4-16 Field effect mobility (μ_{FE}) of all poly-Si TFTs devices versus different stress time.

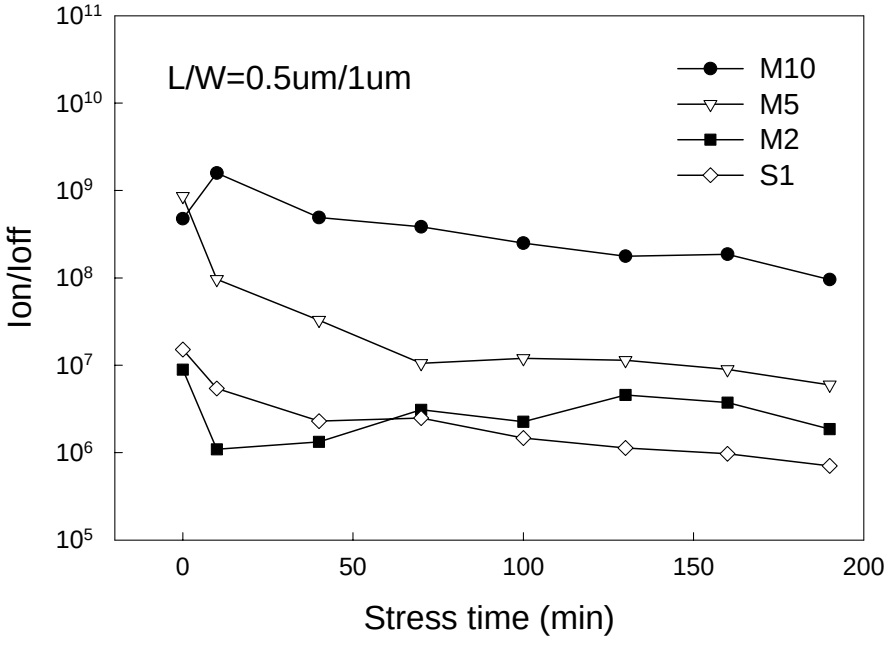


Fig. 4-17 Ion/Ioff ratio of all poly-Si TFTs devices versus different stress time.

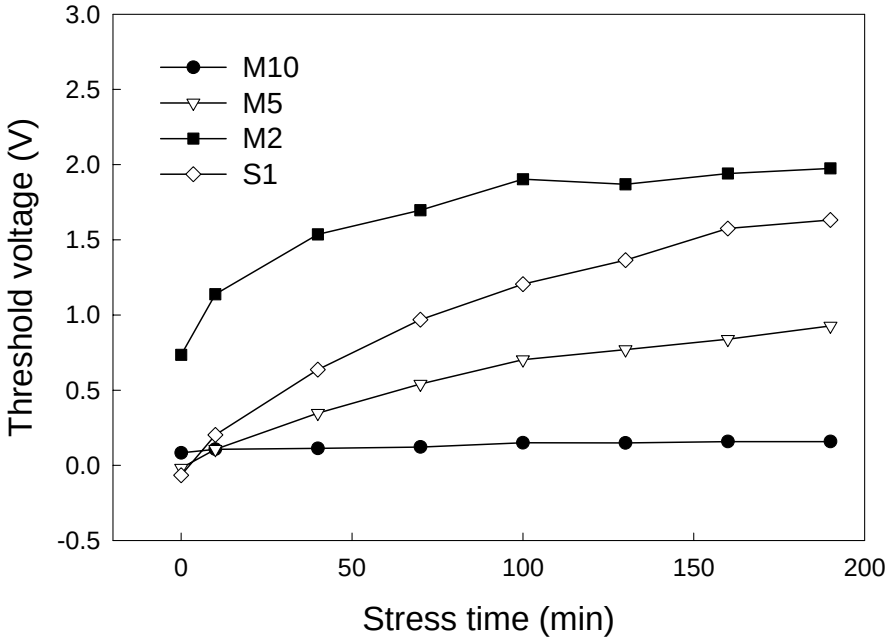


Fig. 4-18 Threshold voltage of all poly-Si TFTs devices versus different stress time.

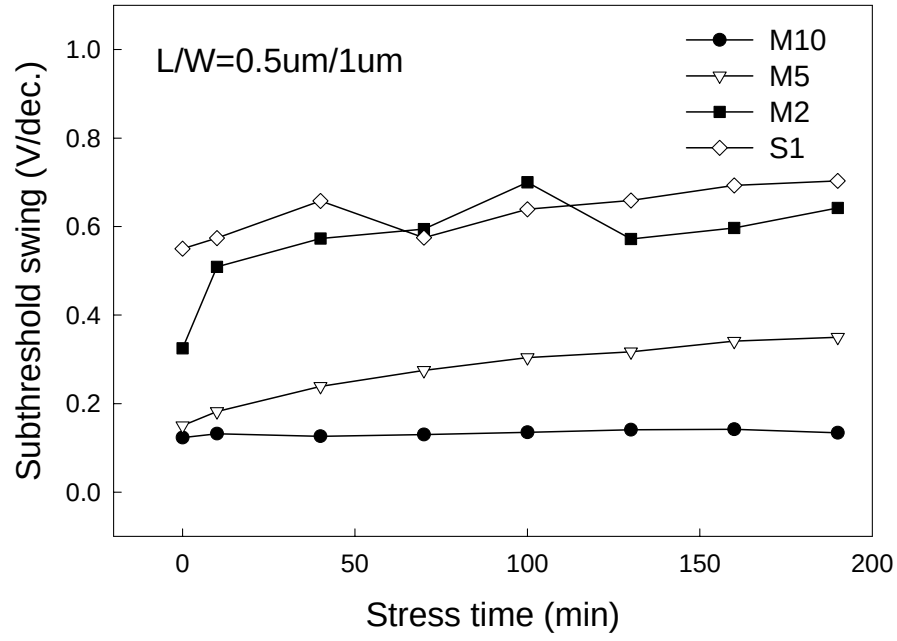


Fig. 4-19 Subthreshold swing (SS) of all poly-Si TFTs devices versus different stress time.

Table III Variation of experimental electronic parameters and corresponding possible degradation mechanics.

Electrical parameters after stressing	**Mainly depending on**
Δg_{mmax}	Interface state generation State generation in the grain boundaries (tail state)
ΔV_{on}	Charge injected into the gate oxide Interface state generation (deep states) State generation in the grain boundaries(deep states)
ΔS (subthreshold swing)	Intra-grain defect density generation (bulk state) Interface state generation (deep states)

Chapter 5
CONCLUSION

We have studied the gate controllability of proposed poly-Si TFTs with multiple channels and different widths. Experiment results show that the gate controllability is increasing with channel number from S1, M2, M5 to M10 as the structure changes from a single gate to a tri-gate sequentially. The M10 TFT has the best gate controllability due to its pronounced nano-wires structure behavior. The M10 TFTs exhibit superior and stable characteristics, such as low leakage current in the off-state, a high ON/OFF current ratio, a steeper subthreshold slope, an absence of DIBL, and a favorable output characteristics. Moreover, we also explored multiple channels with LDD structure to investigate the stress duration relative to different multiple channel width and number in poly-Si thin film transistor. From our experiment results, ON/OFF ratio of all TFTs has an identical degradation behavior. The V_{th} and SS of M10 TFT remain constant after stress.

The fabrication of multiple channel TFTs is quite easy and involves no additional processes. Such TFTs are thus highly promising for use in future high-performance poly-Si TFT applications.

References

Chapter 1

[1.1] H. Oshima and S. Morozumi, "Future trends for TFT integrated circuits on glass substrates," *IEDM Tech. Dig*., 157 (1989)

[1.2] M. Stewart, R. S. Howell, L. Pires, and M. K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays ," *IEEE Trans. Electron Devices*, vol. 48, pp. 845-851, 2001

[1.3] H. Kuriyama et al., "An asymmetric memory cell using a C-TFT for ULSI SRAM," *Symp. On VLSI Tech*., p.38, 1992

[1.4] T. Yamanaka, T. Hashimoto, N. Hasegawa, T. Tanala, N. Hashimoto, A. Shimizu, N. Ohki, K. Ishibashi, K. Sasaki, T. Nishida, T. Mine, E. Takeda, and T. Nagano, "Advanced TFT SRAM cell technology using a phase-shift lithography," *IEEE Trans. Electron Devices*, Vol. 42, pp.1305-1313,1995.

[1.5] K. Yoshizaki, H. Takaashi, Y. Kamigaki, T.asui, K. Komori, and H. Katto, *ISSCC Digest of Tech.*, p.166, 1985

[1.6] N. D.Young, G. Harkin, R. M. Bunn, D. J. McCulloch, and I. D. French , "The fabrication and characterization of EEPROM arrays on glass using a low-temperature poly-Si TFT process," *IEEE Trans. Electron Devices,* Vol. 43, pp. 1930-1936, 1996.

[1.7] T. Kaneko, U. Hosokawa, N. Tadauchi, Y. Kita, and H. Andoh, "400 dpi integrated contact type linear image sensors with poly-Si TFT's analog readout circuits and dynamic shift registers," *IEEE Trans. Electron Devices*, Vol. 38, pp. 1086-1093, 1991

[1.8] U. Hayashi, H. Hayashi, M. Negishi, T. Matsushita, *Proc. of IEEE Solid-State Circuits Conference (ISSCC)*, p. 266 , 1998.

[1.9] N.Yamauchi, U. Inava, and M. Okamura, "An integrated photodetector-

amplifier using a-Si p-i-n photodiodes and poly-Si thin-film transistors," *IEEE Photonic Tech. Lett*, Vol. 5, pp. 319-321, 1993.

[1.10] M. G. Clark, *IEE Proc. Circuits Devices Syst*, Vol. 141, 133 (1994)

[1.11] Noriyoshi Yamauchi, Jean-Jacques J. Hajjar and Rafael Reif, "Polysilicon Thin-Film Transistors with Channel Length and Width Comparable to or Smaller than the Grain Size of the Thin Film," *IEEE Trans. Electron Devices*, Vol. 38, pp 55-60, 1991

[1.12] Singh Jagar, Mansun Chan, M. C. Poon, Hongmei Wang, Ming Qin, Ping K. Ko, Yangyuan Wang, "Single Grain Thin-Film-Transistor (TFT) with SOI CMOS Performance Formed by Metal-Induced-Lateral-Crystallization," *IEDM Tech. Dig.*, pp. 293-296, 1999.

[1.13] K. Nakazawa, "Recrystallization of amorphous silicon films deposited by low-pressure chemical vapor deposition from Si_2H_6 gas," *J. Appl. Phys*, Vol. 69, pp. 1703-1706, 1991.

[1.14] T. J. King and K. C. Saraswat, "Low-temperature fabrication of poly-Si thin-film transistors," *IEEE Electron Device Lett*, Vol. 13, pp. 309-311, 1992.

[1.15] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Tsuda, and S. Nakano, "High mobility poly-Si TFT by a new excimer laser annealing method for large area electronics," *IEDM Tech. Dig*, Vol. 91, p. 563 (1991)

[1.16] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys*. Vol. 53, pp.1193-1202, 1982

[1.17] P. Migliorato, C. Reita, G. Tallatida, M. Quinn and G. Fortunato, "Anomalous off-current mechanisms in n-channel poly-Si thin film transistors." *Solid-State-Electronics*, Vol.38, pp.2075-2079, 1995

[1.18] M. Hack, I-W. Wu, T. H. King and A. G. Lewis, "Analysis of Leakage

Currents in Poly-silicon Thin Film Transistors," *IEDM Tech. Dig*., vol. 93, pp. 385-387, 1993

[1.19] Kwon-Young Choi and Min-Koo Han, "A novel gate-overlapped LDD poly-Si thin-film transistor," *IEEE Electron Device Lett.,* Vol. 17, pp. 566-568, 1996.

[1.20] N. D. Young, G. Harkin, R. M. Bunn, D. J. McCulloch, and I. D. French, "The fabrication and characterization of EEPROM arrays on glass using a low-temperature poly-Si TFT process," *IEEE Trans. Electron Devices*, Vol. 43, No. 11, pp. 1930-1936, 1996.

[1.21] R. K. Watts and J. T. C. Lee, "Tenth-Micron Polysilicon Thin-film Transistors," *IEEE Electron Device Lett.*, Vol. 14, pp. 515-517, 1993.

[1.22] Huang-Chung Cheng, Fang-Shing Wang and Chun-Yao Huang, "Effects of NH3 Passivation on N-Channel Polycrystalline Silicon Thin-Film Transistors" *IEEE Trans. Electron Devices*, Vol. 44, No. 1, pp. 64- 68, 1997.

[1.23] Du-Zen Peng, Ting-Chang Chang, Hsiao-Wen Zan, Tiao-Yuan Huang, Chun-Yen Chang, and Po-Tsun Liu, "Reliability of laser-activated low-temperature polycrystalline silicon thin-film transistors" Applied Physics Letters, Vol. 80, No.25, pp. 4780- 4782, 2002.

[1.24] Anish Kumar K.P., Johnny K. O. Sin, Cuong T. Nguyen, and Ping L. Ko, "Kink-Free Polycrystalline Silicon Double-Gate Elevated-Channel Thin-Film Transustors ", *IEEE Trans. Electron Devices*, Vol. 45, NO. 12 , 1998

[1.25] B.S.Doyle, S.Datta, M. Doczy, S Hareland, B.Jin, J.Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High Performance Fully-Depleted Tri-Gate CMOS Transistors" *IEEE Electron Devices* Letters, Vol. 2, No.4 pp.263-265,2003

[1.26] Gen Pei, Jakub Kedzierski, Phil Oldiges, Meikei Ieong,and Edwin Chih-Chuan Kan, " Finfet Design Considerations Based on 3-D Simulation

and Analytical Modeling" *IEEE Trans. Electron Devices*, Vol. 8, No.49, pp.1411-1419, 2002.

Chapter 2.

[2.1] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys*. Vol. 53, pp.1193-1202, 1982

[2.2] P. Migliorato, C. Reita, G. Tallatida, M. Quinn and G. Fortunato, "Anomalous off-current mechanisms in n-channel poly-Si thin film transistors." *Solid-State-Electronics*, Vol.38, pp.2075-2079, 1995

[2.3] M. Hack, I-W. Wu, T. H. King and A. G. Lewis, "Analysis of Leakage Currents in Poly-silicon Thin Film Transistors," *IEDM Tech. Dig*., vol. 93, pp. 385-387, 1993

[2.4]"Polycrystalline silicon for integrated circuits and displays", second edition, written by Ted Kamins, pp.200-210.

[2.5] K. R. Olasupo and M. K. Hatalis, " Leakage Current Mechanism in Sub-Micron Polysilicon Thin-Film Transistors "IEEE Trans. Electron Devices, Vol. 43, pp.1218, (1996).

[2.6] "Semiconductor devices physics and technology" , second edition, written by S.M Sze, pp. 199-213

Chapter 3.

[3.1] J. Levinson, F.R. Shepherd, P.J. Scanlon, W.D. Westwood, G. Este, and M. Rider, " Conductivity behavior in polycrystalline semiconductor thin film transistors" *J. Appl. Phys*, pp.1193-1202, 1981

Chapter 4.

[4.1] Y. Taur, short course program of IEDM'01

[4.2] "Thin-film transistors", written by Cherie R. Kagan and Paul Andry

[4.3] Anish Kumar K.P., Johnny K. O. Sin, Cuong T. Nguyen, and Ping L. Ko, "Kink-Free Polycrystalline Silicon Double-Gate Elevated-Channel Thin-Film Transustors ", *IEEE Trans. Electron Devices*, Vol. 45, NO. 12 , 1998

[4.4] F. V. Farmakis, J. Brini, G. Kamarinos, and C.A. Dimitriadis, "Anomalous Turn-On Voltage Degradation During Hot-Carrier Stress in Polycrystalline Silicon Thin-Film Transistors", *IEEE Trans. Electron Devices*, Vol. 2,pp.74, 2001