國　立　交　通　大　學

電子工程學系　電子研究所碩士班

碩 士 論 文

$TaSi_xN_y$薄膜對銅原子擴散之阻障特性

Barrier Properties of $TaSi_xN_y$ Thin Films against Cu Diffusion

研　究　生　：林信宏

指 導 教 授：陳茂傑

中華民國九十三年七月

$TaSi_xN_y$薄膜對銅原子擴散之阻障特性

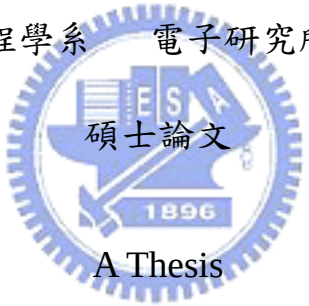
Barrier Properties of $TaSi_xN_y$ Thin Films against Cu Diffusion

研究生　：林信宏　　Student : Hsin-Hung Lin

指導教授：陳茂傑　　Advisor : Mao-Chieh Chen

國立交通大學

電子工程學系　電子研究所碩士班



碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master
in
Electronics Engineering
July 2004
Hsinchu, Taiwan, Republic of China

中華民國九十三年七月

氮化鉭矽薄膜對銅原子擴散之阻障特性

研究生：林信宏　　指導教授：陳茂傑

國立交通大學

電子工程學系　　電子研究所碩士班

摘　要

本論文主要包含兩部分。第一部份探討以$TaSi_2$ 靶材在氮(N_2)/氬(Ar)混合氣體中濺鍍沈積、厚度為 10 奈米之氮化鉭矽($TaSi_xN_y$)的擴散阻障特性；第二部份探討在濺鍍沈積之$TaSi_xN_y$阻障層作後續處理，對於阻障層之擴散阻障能力的改善，其中後續處理的方式包括氮氣熱退火、氮氣電漿處理、以及氮氣熱退火結合氮氣電漿處理。吾人利用「銅/阻障層/p^+n」接面二極體在氮氣中熱退火處理後測得之電性劣化情形來評估阻障層對銅原子擴散之阻障特性。實驗結果顯示，在N_2/Ar流量比為 15 到 20%的N_2/Ar混合氣體中濺鍍所得之$TaSi_xN_y$(15~20%)阻障層具有最佳的擴散阻障特性。厚度 10 奈米的$TaSi_xN_y$(15%)阻障層，可使「銅/阻障層/p^+n」接面二極體在 450℃熱退火後仍然保有原來的電特性。經過氮氣熱退火處理(500℃，30 分鐘)的阻障層，其「銅/阻障層/p^+n」接面二極體的熱穩定溫度可達到 500℃；而經過氮氣電漿處理(150W，10 分鐘)之$TaSi_xN_y$(15%)，則可使接面二極體的熱穩定溫度提升到 550℃。結合上述兩項後續處理，即氮氣熱退火處理後接著作氮氣電漿處理，可得一最佳阻障層，使接面二極體的熱穩定溫度進一步提升到 600℃。阻障層特性的改善主要是因為氮氣熱退火處理對

於在濺鍍沈積$TaSi_xN_y$阻障層時所產生的局部性缺陷具有修補的作用；而氮氣電漿處理則可以在阻障層表面形成富有氮原子的表面層，藉由氮原子之填塞在晶粒邊界和局部缺陷，可阻斷銅原子的擴散路徑。

Barrier Properties of $TaSi_xN_y$ Thin Films against Cu Diffusion

Student: Hsin-Hung Lin **Advisor: Mao-Chieh Chen**

Institute of Electronics
Department of Electronics Engineering
National Chiao Tung University

Abstract

This thesis studies the barrier property of 10-nm-thick $TaSi_x$-based $TaSi_xN_y$ layers sputter deposited from a $TaSi_2$ target in various N_2/Ar mixing gases, using electrical measurement on $Cu/TaSi_xN_y/p^+$-n junction diodes as well as various techniques of material analysis. The study also includes the barrier capability improvement of the thin $TaSi_xN_y$ layer by various post-deposition treatments, including N_2-thermal-annealing, N_2-plasma-treatment and N_2-thermal-annealing followed by N_2-plasma-treatment on the surface of the barrier layer.

It was found that the $TaSi_xN_y$ film sputter deposited in a N_2/Ar gas mixture with the N_2/Ar flow ratio of 15 to 20% has the most efficient barrier property. The $Cu/TaSi_xN_y/p^+$-n junction diodes with this optimal 10-nm-thick $TaSi_xN_y$ barrier layer were able to remain stable after thermal annealing at temperatures up to 450℃. The post-deposition N_2-thermal-annealing at 500℃ for 30min made the $TaSi_xN_y$(15%) layer (sputter deposited in N_2/Ar mixed ambient with the N_2/Ar flow ratio of 15%) capable of raising the thermally stable temperature of the

Cu/$TaSi_xN_y$(15%)/p^+-n junction diodes up to 500℃. With 150W N_2-plasma-treatment for 10min on the $TaSi_xN_y$(15%) barrier layer, the Cu/$TaSi_xN_y$(15%)/p^+-n junction diodes were able to remain thermally stable at temperatures up to 550℃. Moreover, the combined post-deposition-treatment of N_2-thermal-annealing followed by N_2-plasma-treatment resulted in the most efficient barrier property, making the Cu/$TaSi_xN_y$(15%)/p^+-n junction diodes capable of remaining stable at temperatures up to 600℃. The improvement in the diffusion barrier property may be attributed to the healing of localized defects in the reactively sputter deposited $TaSi_xN_y$ layer by the post-deposition N_2-thermal-annealing, and the formation of a nitrogen rich surface layer by N_2-plasma-treatment such that nitrogen atoms are stuffed into the grain boundaries and localized defects, thus obstructing the diffusion paths of Cu atoms.

誌謝

我想，我不曾也不會再遇到一位這麼好的老師了。恕我無法用三言兩語表達出這樣的感覺，唯有真正親身體驗了，才會了解什麼叫做泱泱學者的風範，什麼才是「人師」的表率。老師對學生講話的神情與態度、老師對學生的支持、包容與耐心、老師在論文上的字字珠璣，是我碩士班兩年的另一個重大的收穫。學生再一次對老師獻上最誠摯的感謝之意，在未來的日子，我也將帶著老師的身教及言教走在人生大道上。

除此之外也要特別感謝吳世全博士的支持與包容，讓我得以順利完成碩士學業。謝謝奈米中心的諸位助理與技術員，有了你們辛苦的維護實驗設備及適時的援助，才讓我得以完成許多重要的實驗；感謝清大貴儀中心的余勝德先生、蔡靜雯小姐、原科中心的林義焜先生以及張廖貴術老師在材料分析上的協助，讓本論文能更加完整。

獨學而無友，則孤陋而寡聞

在 629 的日子讓我又多認識了一群不同的人，小鐵學長的直爽、有原則，讓我對獅子座的人有了不同的想法；吳偉豪學長的認真與執著，一直是 629 的一股清流；王超群學長的熱心展現了客家人的傳統美德；感謝以上三位學長對我的指導與協助，尤其是王超群學長

在 SEM 上了的鼎力相助，不僅增加了本論文的相關佐證，也為冰冷的實驗數據增添了些許的美感。依秀的自娛娛人、親切大方的待人態度，使得南投除了好山好水以外，也出了這麼一個討人喜歡的人；安志的樂天與泰然的行事風格，總是讓人覺得天塌下來會有人撐著；宇國的熱心與精湛的球技，證明宜蘭的確是最適合人居住的地方；阿國學長的才華與行事效率，讓我了解世上原來有這種人存在；賴祐生學長對機台的了解以及拿板手的架勢，是別人學不來的。感謝 629 的所有夥伴，你們讓我再一次體會，每個人都是一座豐富的寶庫。

還要特別感謝一群好朋友和室友，嘉欣、昕璋、慶宗、全一、盈彰、阿伯、水欽和育周；床頭的營窗夜語、尋找美食的樂趣、踏青旅行的歡樂時光，這一切豐富了我近兩年甚至是近六年的精華歲月；如果沒有這些朋友，我想我一定會變成一個古怪、孤僻、不得人緣的傢伙。還有其他這一路相伴、互相幫助的好友，原諒我無法再此一一詳述，只能對你們說一聲謝謝。

最後，家人的支持一直是我背後一股強大的力量；我想只有我和姊姊了解父母親拉拔我們長大、完成學業的含辛茹苦，沒有任何東西可以與你們所做的一切互相比擬，謝謝你們。也感謝姐姐在生活上的關心、一路上的扶持，甚至支助我完成學業，我們的姊弟情誼大概會這樣持續到老了。

來日後會相與期，去去莫遲疑

兩年前的此時，以不捨的心情告別了南台灣的艷陽；而今，相同的辱暑，一樣是別離，但我無法說服自己擁有徐志摩的瀟灑，雲彩片片，已長留我心。在無塵衣的穿脫之間，在每週三凌晨的星月所投射的身影之下，在 629 的夕陽景致中，在所有好友的陪伴之下，兩年的日子像風一樣過去了。我不確定以後還能不能有這麼單純的學生生活，但是這麼一段曾經經歷過、擁有過的年少歲月，大概不會再出現了。再見了，我親愛的師長和朋友。

Contents

Table Captions

Chapter 3

Chapter 4

Figure Captions

Chapter 2

Chapter 3

Chapter 4

Chapter 1

Introduction

1.1 The Needs of Diffusion Barrier in ULSI

The devices feature size in Si-based integrated circuits is continuously reduced due to the needs of faster circuit speed, higher chip functionality and lower per-chip cost. However, as the devices feature size is scaled down to sub-quarter-micrometer, the electromigration and RC time delay of the interconnect wires in integrated circuits become the major challenging issues. Unfortunately, the conventionally used Al and Al-alloys are not able to meet these challenges because of their poor electromigration resistance and moderate electrical resistivity (2.67 μΩ-cm for Al and higher than 3 μΩ-cm for Al-alloys) [1-4]. Therefore, an alternative material having a lower electrical resistivity and superior electromigration resistance is of great interest [5].

Cu is an attractive material because of its lower electrical resistivity (1.7μΩ-cm) and higher electromigration resistance compared to Al and Al-alloys [6]. However, Cu diffuses fast in Si substrate and forms Cu-Si compounds at temperatures as low as 200℃ [7]. Moreover, Cu is a deep-level dopant in Si [8], which affects the effective doping concentration, lowers the minority carrier lifetime, and increases the junction leakage current. In addition, Cu drifts readily in SiO_2 under accelerated electric field and adheres poorly to dielectrics [9]. Therefore, a thin film layer functioning as an adhesion/diffusion barrier that can

prevent Cu from contaminating the device is indispensable in the Cu metallization scheme.

1.2 Ideal Diffusion Barrier

When a material is deposited onto another material, the interdiffusion between these two materials maybe accelerated during the subsequent heat treatment. By inserting a third material between these two materials, the undesirable interdiffusion between them can be dramatically retarded. The third material is so called a diffusion barrier. Generally, diffusion may happen at free surface, along grain boundaries and dislocations, or in the interior of crystal [10]. When one atom diffuses through the diffusion barrier, the most possible fast diffusion paths are along grain boundaries and dislocations.

The requirements for ideal diffusion barrier are listed as follows [11].

1. The barrier material should have a good adhesion with both layers.
2. The barrier should not react with each layer.
3. The interdiffusion of the two layers through the barrier should be low.
4. The barrier should have a low contact resistance.
5. The barrier should be resistant to thermal and mechanical stress.
6. The thermal expansion coefficient of the barrier should be compatible with that of both layers.
7. The barrier should have a good electrical as well as thermal conductivity

1.3 $TaSi_xN_y$ Barrier

Due to the scaling of ULSI devices to dimensions below 0.13 μm, future barriers have to be effective even at a very low film thickness in order to avoid diffusion of Cu into the dielectric and the Si regions. A large number of Cu diffusion barriers have been investigated [12-20]; among them, particular interest has been focused on the refractory metals and their nitrides, including Cr(N), Ti(N), Ta(N), and W(N), because of their high melting points, high thermal stability, good adhesion to dielectrics, and good electrical conductivity. Recently, Ta(N) films are the most commonly used Cu diffusion barriers. However, the Ta(N) films may become polycrystalline at temperatures above 450℃ [21], and the grain boundaries can act as fast diffusion paths for Cu. Another Ta-based material, $TaSi_xN_y$, has also been found to be an efficient diffusion barrier because of its amorphous state up to temperatures as high as 900℃ [22-26]. Without grain boundaries in the barrier layer, it can serve as a very efficient barrier against Cu diffusion.

In this thesis, we investigate the barrier capability of very thin $TaSi_xN_y$ layer with a thickness of 10 nm. The $TaSi_xN_y$ thin films were sputter deposited using a $TaSi_2$ target in an Ar/N_2 ambient with various Ar/N_2 ratios. The optimum composition of the $TaSi_xN_y$ film is to be determined with regard to the best barrier property. This is to be followed by investigating the effects of plasma treatment and thermal annealing on the efficiency of the $TaSi_xN_y$ barrier.

1.4 Thesis Organization

There are five chapters in this thesis. Following the introduction in

chapter 1, experimental procedures in detail are described in chapter 2. Chapter 3 contains the studies on the barrier properties of 10-nm-thick $TaSi_xN_y$ layers sputter deposited using a $TaSi_2$ target with various nitrogen flow rates. Chapter 4 deals with the improvement of $TaSi_xN_y$ barrier properties by post deposition plasma treatment and thermal annealing. Finally, conclusions of this thesis study are given in Chapter 5.

Chapter 2

Experimental Procedure

2.1 Samples Preparation

The barrier properties of $TaSi_x$ and $TaSi_xN_y$ films were investigated using a structure of Cu/barrier/p^+-n junction diodes. The starting materials used for the samples preparation were n-type, phosphorus-doped, (100) oriented silicon wafers with a nominal resistivity of 4-7 μΩ-cm. After RCA standard cleaning, the wafers were thermally oxidized to grow a 500-nm-thick oxide layer in a pyrogenic steam ambient at 1050℃. Active regions with area sizes of 300×300, 500×500, and 1000×1000 μm^2 were defined using the conventional photo lithographic technique and chemical wet etching. Then a screen oxide of 20 nm thickness was thermally grown in a dry oxygen ambient at 950 ℃. The p^+-n junctions were formed by BF_2^+ implantation at 40keV to a dose of 3×10^{15} cm^{-2} followed by furnace annealing at 900℃ for 30min in N_2 ambient.

After the junctions were formed, the screen oxide was removed using a BOE solution, followed by a rinse in DI water for 5 min and spin dried. Subsequently, the wafers were divided into four groups for the preparation of the following devices: (a) Cu/$TaSi_x$/p^+-n, (b) Cu/$TaSi_xN_y$/p^+-n, (c) Cu/$TaSi_xN_y$(A,B,C)/p^+-n, and (d) Cu/p^+-n junction diodes. In this study, a DC magnetron sputtering system with a base pressure below 2×10^{-6} Torr was used for the deposition of the barrier

layers. Both $TaSi_x$ and $TaSi_xN_y$ films were sputter deposited at a sputtering power of 150 watts to a thickness of 10 nm using a $TaSi_2$ target without intentional substrate heating and bias. The $TaSi_x$ films were sputtered in an Ar ambient at a pressure of 7.6 mTorr; the flow rate of Ar sputtering gas was kept at 24 sccm. On the other hand, the $TaSi_xN_y$ films were reactively sputtered in a gas mixture of Ar and N_2 at the same pressure of 7.6 mTorr; various N_2/Ar flow ratios (5, 10, 15, 20 and 25% separately) with the Ar flow rate kept constant at 24 sccm were used to make the Ar/N_2 gas mixture. Prior to each sputter deposition, the target was cleaned by pre-sputtering with the shutter closed for 15min.

For the preparation of Cu/$TaSi_xN_y$(A,B,C)/p^+-n junction diodes, the samples were separated into three groups according to different plasma/thermal treatments on $TaSi_xN_y$ surfaces: (a) N_2-plasma treatment, (b) thermal annealing in N_2, and (c) thermal annealing in N_2 followed by N_2-plasma treatment. The N_2-plasma treatment was performed for 10min with a plasma power of 150 watts at a gas pressure of 385 mTorr with N_2 flow rate of 200 sccm and at a substrate temperature of 100℃. The thermal annealing was performed in N_2 ambient at a temperature of 500℃ for 30min. Therefore, a very thin Ta-Si-N layer was supposedly formed on the surface of the $TaSi_xN_y$ layer. Finally, Cu films of 200 nm thickness were sputter deposited on all samples using a pure Cu target in an Ar ambient at a pressure of 7.6 mTorr, and the Cu-electrode was defined by lift-off technique. For comparison, thermal stability of the Cu/p^+-n junction diode without any barrier layer was also investigated. The schematic cross sections of the Cu-electrode p^+n junction diodes with and without a barrier layer are illustrated in Fig. 2-1.

2.2 Electrical Measurement

To investigate the thermal stability of the Cu/barrier/p^+-n junction diodes, the diodes were thermally annealed in N_2 flowing furnace for 30min at various temperatures ranging from 300 to 800℃. At the end of thermal annealing, the annealed samples were pulled out slowly from the furnace so as to prevent the undesirable thermal stress. Leakage current of the junction diodes was measured at a reverse bias of –5V using an HP-4145B semiconductor parameters analyzer. The active area sizes of the measured diodes were 300×300, 500×500, and 1000×1000 μm^2, and at least 15 randomly chosen diodes were measured in each case.

2.3 Material Analyses

For the material analyses, unpatterned samples of Cu/Si and Cu/barrier/Si structures were also prepared, in which the barrier represents $TaSi_x$, $TaSi_xN_y$, or $TaSi_xN_y$(A,B,C) layer. These samples were processed in the same process run with the patterned samples of junction diodes. Various techniques and apparatus were used for the material analyses. Rutherford backscattering spectrometry (RBS) was used to determine the composition of barrier films. Four point probe was used for sheet resistance measurement. X-ray diffraction (XRD) analysis was used to identify the crystalline phase. Scanning electron microscopy (SEM) was used to observe the surface morphology of the material samples before and after annealing at various temperatures. Auger emission spectroscopy (AES) was used to measure the elemental depth profiles. Before the AES analysis, the Cu layer was removed using

dilute HNO_3 solution (10 vol.%).

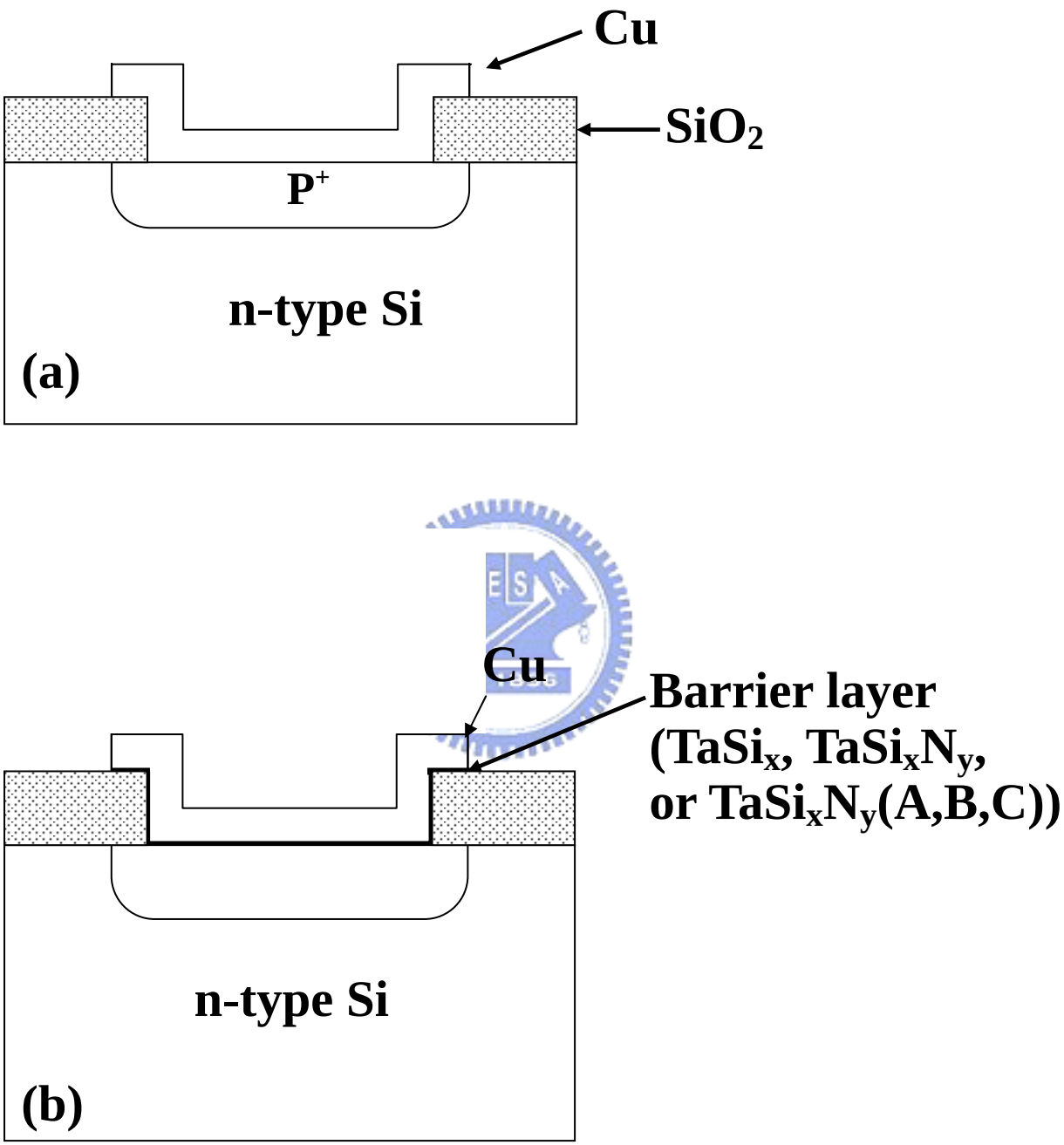


Fig. 2-1 Schematic cross sections of (a) Cu/p^+-n and (b) Cu/barrier/p^+-n junction diodes.