Chapter 3

Barrier Property of Sputter Deposited $TaSi_xN_y$ with Various Nitrogen Contents

3.1 Introduction

Thin films of refractory metal nitrides have been widely investigated as diffusion barriers in interconnection system of Si-based integrated circuits. It was reported that amorphous thin films of Ta-Si-N alloys served as efficient diffusion barrier against Cu diffusion because of their grain boundary free microstructure and adequate electrical conductivity [27-32]. However, the thickness of the barrier layer reported in literature is generally too thick to meet the future requirement in ULSI applications. This chapter is devoted to study the barrier property of 10-nm-thick $TaSi_x$-based $TaSi_xN_y$ layers sputter deposited from the $TaSi_2$ target. The enhancement of barrier capability by the incorporation of nitrogen in the barrier layer was investigated. Electrical measurements and material analyses were used to evaluate the barrier property with respect to retarding the diffusion of Cu. We also explored the failure mechanism of the barrier film.

3.2 Physical Property of Sputter Deposited $TaSi_xN_y$ films

Table 3-1 shows the composition of as-deposited and 500℃ -annealed $TaSi_xN_y$ films which were sputtered in various N_2/Ar mixed gases using a $TaSi_2$ target. The higher the N_2/Ar flow ratio was used to

make the N_2/Ar mixed gas for sputtering, the larger was the nitrogen content in the sputter deposited $TaSi_xN_y$ films. After a thermal annealing at 500℃ for 30min in N_2 ambient, there is a varied change in the composition of $TaSi_xN_y$.

The resistivity of the $TaSi_xN_y$ films was found to increase with the N_2/Ar flow ratio, as shown in Fig. 3-1. This indicates that the incorporation of nitrogen in the films increased the film resistivity. The sheet resistance change of annealed samples, normalized to the as-deposited sheet resistance value, is denoted as $\frac{\Delta Rs}{Rs}$% and defined as follows:

$$\frac{\Delta Rs}{Rs} = \frac{Rs_{after\ anneal} - Rs_{as-deposited}}{Rs_{as-deposited}}$$

Figure 3-2 shows the sheet resistance change versus annealing temperature for the $TaSi_xN_y$(100nm)/Si samples. It is found that thermal annealing resulted in decrease of the sheet resistance, and that a proper amount of nitrogen doping would improve the thermal stability of the films. For the films studied in this work, the $TaSi_xN_y$ film sputter deposited in a N_2/Ar mixed gas made of 15% N_2/Ar flow ratio appeared to be the most thermally stable.

3.3 Electrical Measurements

Figure 3-3 illustrates the histograms showing the distribution of the reverse bias leakage current density measured at –5 volts for the Cu/p^+-n

and Cu/$TaSi_x$(10nm)/p^+-n junction diodes. It is notable that $TaSi_xN_y$(P%) stands for the $TaSi_xN_y$ film sputter deposited in a N_2/Ar gas mixtire made of P% N_2/Ar flow ratio; thus, $TaSi_xN_y$(0%) stands for the $TaSi_xN_y$ film sputter deposited in a pure Ar ambient, while $TaSi_xN_y$(5%) stands for the $TaSi_xN_y$ film sputter deposited in a N_2/Ar mixed gas made of 5% N_2/Ar flow ratio. Since copper reacts with Si at temperature as low as 200℃, the junction diodes without a barrier layer between Cu and Si substrate degraded after a 30min thermal anneal at 300℃, and all diodes failed after annealing at 400℃ [Fig. 3-3(a)]. In this study, the junction diode with a leakage current density exceeding 10^{-7} A/cm^2 is defined as a failure. With a 10-nm-thick barrier layer of $TaSi_xN_y$(0%), which is practically a $TaSi_x$ layer, the electrical characteristics of the Cu/$TaSi_x$(10nm)/p^+-n junction diodes were able to remain intact at temperatures up to 350℃ [Fig. 3-3(b)]. It is clear that $TaSi_x$ layer can act as a diffusion barrier between Cu and Si.

Figure 3-4 shows the statistical distribution of the reverse bias leakage current density measured at –5 volts for the Cu/$TaSi_xN_y$(5%)/p^+-n, Cu/$TaSi_xN_y$(10%)/p^+-n, Cu/$TaSi_xN_y$(15%)/p^+-n, Cu/$TaSi_xN_y$(20%)/p^+-n and Cu/$TaSi_xN_y$(25%)/p^+-n junction diodes annealed at various temperatures. The junction characteristics of the Cu/$TaSi_xN_y$(5%)/p^+-n diodes started to exhibit degradation after annealing at 400℃ [Fig. 3-4(a)], showing no obvious improvement in the barrier effectiveness of the $TaSi_xN_y$(5%) layer over the $TaSi_xN_y$(0%) layer. For the Cu/$TaSi_xN_y$(10%)/p^+-n junction diodes, the devices remained stable after annealing at temperatures up to 400℃ [Fig. 3-4(b)], indicating a slight improvement of barrier property for the $TaSi_xN_y$(10%) layer. It was

found that the $TaSi_xN_y$(15%) layer exhibited the most efficient barrier capability; all of the Cu/$TaSi_xN_y$(15%)/p^+-n junction diodes were able to remain stable at temperatures up to 450℃ [Fig. 3-4(c)]. When the N_2/Ar flow ratio was increased to 20% and 25% for making the mixed gas for sputtering, the respectively sputter deposited $TaSi_xN_y$(20%) and $TaSi_xN_y$(25%) layers revealed a degraded barrier effectiveness compared to the $TaSi_xN_y$(15%) layer [Fig. 3-4(d) and (e)]. Based on the above results, we may conclude that the thermal stability of the Cu/$TaSi_xN_y$/p^+-n junction diodes can be most efficiently improved by doping a proper amount of nitrogen into the barrier layer.

3.4 Material Analyses

3.4.1 Sheet Resistance Measurements

Thermal stability of the sheet resistance of a metallization scheme is an important indicator of metallurgical interaction occurred within the metallized devices, although a clear understanding of the interaction generally requires the support of other analytical techniques. The percentage of sheet resistance change has been defined in section 3.2. Figure 3-5 shows the percentage of sheet resistance change versus annealing temperature for various Cu/$TaSi_xN_y$(10nm)/Si samples. All samples, upon first annealing at 400℃, exhibited a sizable amount of decrease in sheet resistance. This is presumably due to defect healing and grain growth of the sputter deposited Cu layers during the thermal annealing process. For the sample of Cu/$TaSi_xN_y$(0%)/Si, the Rs revealed a remarkable increase after annealing at temperatures above 550

℃. Remarkable increase in Rs was similarly observed for the Cu/$TaSi_xN_y$(5%)/Si, Cu/$TaSi_xN_y$(10%)/Si, Cu/$TaSi_xN_y$(15%)/Si and Cu/$TaSi_xN_y$(20%)/Si samples, after annealing at temperatures above 600, 650, 700 and 700℃, respectively. However, the Rs value of the Cu/$TaSi_xN_y$(25%)/Si sample only remained stable up to the annealing temperature of 650℃. It is clear from these observations that the optimal thermal stability of the Cu/$TaSi_xN_y$(10nm)/Si structure can be obtained by using a $TaSi_xN_y$ barrier layer sputter deposited in a N_2/Ar gas mixture with the N_2/Ar flow ratio of 15 to 20%. The remarkable increase in Rs for the Cu/$TaSi_xN_y$/Si samples reflects the consumption of conductive Cu layer due to Cu-silicide compound formation, which is confirmed by the results of XRD analysis to be shown in section 3.4.2. Careful comparison indicates that the results of sheet resistance measurements are consistent with the results of electrical characteristic measurements, and that the electrical measurement is a more sensitive technique for the detection of barrier failure.

3.4.2 XRD Analyses

Figure 3-6 shows the XRD spectra for the $TaSi_xN_y$(0%)/Si and $TaSi_xN_y$(15%)/Si samples annealed at various temperatures; both $TaSi_xN_y$(0%) and $TaSi_xN_y$(15%) layers have a thickness of 100nm. The XRD spectra indicate amorphism for both as-deposited $TaSi_xN_y$ films. Upon annealing at elevated temperatures, the $TaSi_xN_y$(0%) and $TaSi_xN_y$(15%) films remained amorphous up to 700 and 800℃, respectively. However, Ta_5Si_3 and $TaSi_2$ silicide phases appeared after annealing at 800℃ for the $TaSi_xN_y$(0%)/Si sample [Fig. 3-6(a)]. It is

clear that the incorporation of nitrogen in the $TaSi_xN_y$ film raised the crystallization temperature and retarded the formation of Ta-silicide. Figure 3-7 shows the XRD spectra for the Cu/Si, Cu/$TaSi_xN_y$(0%)/Si, Cu/$TaSi_xN_y$(15%)/Si and Cu/$TaSi_xN_y$(25%)/Si samples annealed at various temperatures. For the Cu/Si sample without any barrier layer between Cu and Si substrate, Cu_4Si phase was first detected after annealing at 300℃; following the 400℃ anneal, a sharp diffraction peak of Cu_3Si phase also appeared [Fig. 3-7(a)]. With a $TaSi_xN_y$(0%) barrier layer between Cu and Si substrate, silicide phase of Cu_3Si started to appear at 700℃ [Fig. 3-7(b)]. For the Cu/$TaSi_xN_y$(15%)/Si sample, none of the Cu- or Ta-silicide phase was detected in the XRD spectra even after the sample was annealed at 800℃ [Fig. 3-7(c)]. For the sample of Cu/$TaSi_xN_y$(25%)/Si, however, TaN and Ta_5Si_3 were first detected at 700℃, and Cu_3Si phase also appeared after annealing at 800℃, though the signals associated with TaN and Ta_5Si_3 became weak in intensity [Fig. 3-7(d)]. Therefore, the XRD analyses revealed that the failure of the $TaSi_xN_y$ barrier layer resulted in the formation of Cu-silicide (Cu_3Si) and/or TaN and Ta_5Si_3. The results of the XRD analyses are consistent with those of the sheet resistance measurements [Fig. 3-5]. The reason that the failure temperatures determined by the XRD analysis are higher than those determined by the sheet resistance measurements is presumably due to the localized Cu-silicide formation which may not be detected by the XRD analysis.

3.4.3 SEM Observation

The surface morphology of the Cu/barrier/Si samples annealed at

various temperatures was observed by SEM. Figure 3-8 shows the SEM micrographs for the thermally annealed Cu/barrier/Si samples with various $TaSi_xN_y$ barrier layers. For the Cu/$TaSi_xN_y$(0%)/Si sample [Fig. 3-8(a)], the surface morphology remained fairly stable after annealing at 450℃ except for the minor Cu grain growth; however, large localized protrusions appeared on the surface after annealing at 500℃, which is presumably due to the formation of Cu-silicide phase. For the Cu/$TaSi_xN_y$(5%)/Si sample [Fig. 3-8(b)], localized protrusions were observed after annealing at 550℃, which is 50℃ higher than the corresponding temperature of the Cu/$TaSi_xN_y$(0%)/Si sample. For the Cu/$TaSi_xN_y$(10%)/Si sample [Fig. 3-8(c)], the surface remained stable up to 550℃ while severe localized protrusions were observed after annealing at 600℃. For the samples of Cu/$TaSi_xN_y$(15%)/Si and Cu/$TaSi_xN_y$(20%)/Si [Fig. 3-8(d) and (e)], the surface morphology remained fairly stable up to 600℃ while localized protrusions appeared after annealing at 650℃. However, when the N_2/Ar flow ratio was increased to 25% during the sputter deposition of the barrier layer, the formation temperature of localized protrusions was lowered to 600℃ for the Cu/$TaSi_xN_y$(25%)/Si sample [Fig. 3-8(f)]. Apparently, the optimal barrier capability can be obtained when the N_2/Ar flow ratio of 15 or 20% was used to make the N_2/Ar gas mixture for the sputter deposition of the $TaSi_xN_y$ barrier layer. The results of SEM observation are also consistent with those of the electrical and sheet resistance measurements. We presume that the failure of the amorphous $TaSi_xN_y$ barrier layer proceeded in the following sequence. First, Cu diffused through the barrier layer via local defects and/or grain boundaries. Second, small

localized Cu-silicide precipitated, and TaN and Ta-silicide phases might also be formed. Third, as the grains of Cu-silicide grew, the volume difference between Cu and its silicide resulted in the deformation of Cu overlayer. Finally, the Cu-silicide protruded through the surface of the $Cu/TaSi_xN_y/Si$ samples.

3.4.4 AES Analyses

The AES depth profiles were used to detect the permeation of Cu in the barrier layer. Prior to the AES analysis, the Cu overlayer was removed (by dilute HNO_3 solution) from the thermally annealed $Cu/TaSi_xN_y/Si$ samples to prevent the knock-in effect during the AES depth profiling. Figure 3-9 and Fig. 3-10 show, respectively, the AES depth profiles of the $Cu/TaSi_xN_y(25\%)/Si$ and $Cu/TaSi_xN_y(15\%)/Si$ samples annealed at various temperatures after removal of the Cu overlayer. For the sample of $Cu/TaSi_xN_y(25\%)/Si$ [Fig. 3-9], permeation of Cu in the barrier layer after annealing at 400℃ was observed, and the presence of Cu in the Si substrate is obvious when the sample was annealed at 450℃. This corresponds to the severe degradation of the $Cu/TaSi_xN_y(25\%)/p^+$-n junction diodes annealed at 450℃, as shown in Fig. 3-4(e). Similar AES depth profiles of Cu were observed for the sample of $Cu/TaSi_xN_y(15\%)/Si$ except that the corresponding temperature was raised by 50℃ [Fig. 3-10].

3.5 Summary

The vary thin (10-nm-thick) $TaSi_xN_y$ layers, sputter deposited from a

$TaSi_2$ target in a gas mixture of N_2 and Ar with various N_2/Ar flow ratios, were investigated using the structure of Cu/$TaSi_xN_y$/p^+-n junction diodes with respect to the barrier capability against Cu diffusion. It was found that a 10-nm-thick $TaSi_x$ layer (or $TaSi_xN_y$(0%) layer) sputter deposited in Ar ambient was able to make the Cu/$TaSi_x$/p^+-n junction diodes capable of sustaining a 30min thermal annealing at temperatures up to 350℃ without degrading the diodes electrical characteristics. Nitrogen incorporation in $TaSi_x$ by introducing N_2 in the sputtering gas of Ar, resulted in the formation of amorphous $TaSi_xN_y$ films, which was able to remain amorphous at temperatures up to 800℃ and possesses a much improved barrier capability against Cu diffusion. The most efficient barrier property of the barrier layer can be obtained by sputter depositing the $TaSi_xN_y$ barrier film in a N_2/Ar gas mixture with the N_2/Ar flow ratio of 15 to 20%. The Cu/$TaSi_xN_y$/p^+-n junction diodes with this optimal 10-nm-thick $TaSi_xN_y$ barrier layer, were able to remain stable after annealing at temperatures up to 450℃. Various material analyses, including sheet resistance measurement, XRD analysis, SEM observation and AES depth profile analysis, made on the thermally annealed samples showed that the results of material analyses are consistent with the results of electrical measurements. The comparative results of thermal stability for the Cu/$TaSi_xN_y$/p^+-n junction diodes determined by electrical measurement and various techniques of material analyses are summarized in Table 3-2.

Table 3-1 Composition of $TaSi_xN_y$ films sputter deposited in N_2/Ar mixed gases made of various N_2/Ar flow ratios.

N_2/Ar flow ratio for making the sputtering gas	Composition (Ta : Si : N)	
	As-deposited	After annealing at 500℃ in N_2 ambient
5%	1 : 1.28 : 0.50	1 : 1.64 : 0.39
10%	1 : 1.35 : 0.59	1 : 1.68 : 0.89
15%	1 : 1.88 : 0.96	1 : 1.67 : 1.50
20%	1 : 1.65 : 1.70	1 : 1.61 : 1.74
25%	1 : 1.43 : 2.33	1 : 1.40 : 1.60

Table 3-2 Thermal stability temperature (℃) for $TaSi_xN_y$ barrier layers sputter deposited in various N_2/Ar mixed gases determined by different techniques of measurements and analyses.

Measurement /Analysis method	N_2/Ar flow ratios (%) for making the sputtering ambient					
	0	5	10	15	20	25
p^+n junction diodes	350	350	400	450	400	400
sheet resistance (Rs)	550	600	650	700	700	650
XRD	650	N/A	N/A	800+	N/A	800
SEM	450	500	550	600	600	550
AES	N/A	N/A	N/A	450	N/A	400

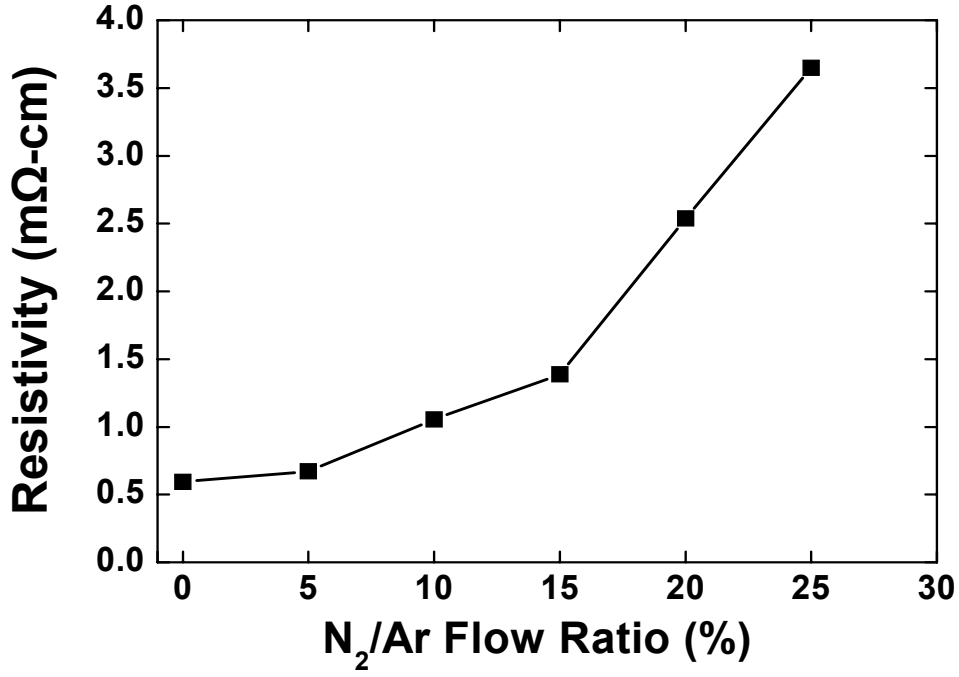


Fig. 3-1 Resistivity vs. N_2/Ar flow ratio for the as-deposited $TaSi_xN_y$ films.

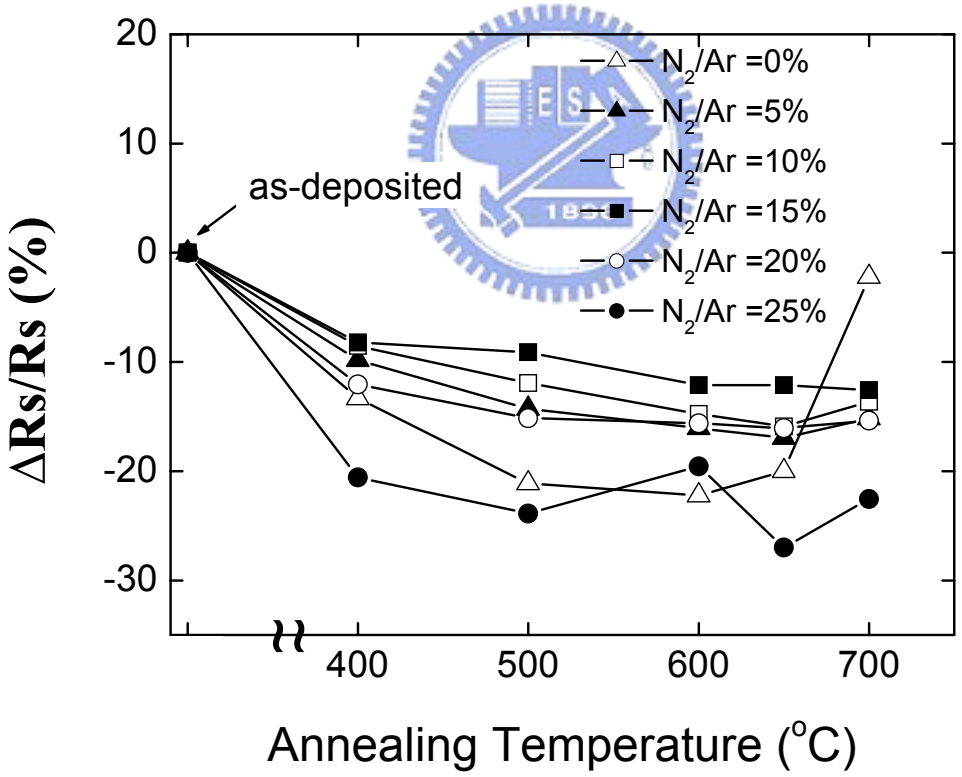


Fig. 3-2 Percentage of sheet resistance change vs. annealing temperature for the $TaSi_xN_y$(100nm)/Si samples with the $TaSi_xN_y$ film sputter deposited in N_2/Ar mixed gas made of various N_2/Ar flow ratios.

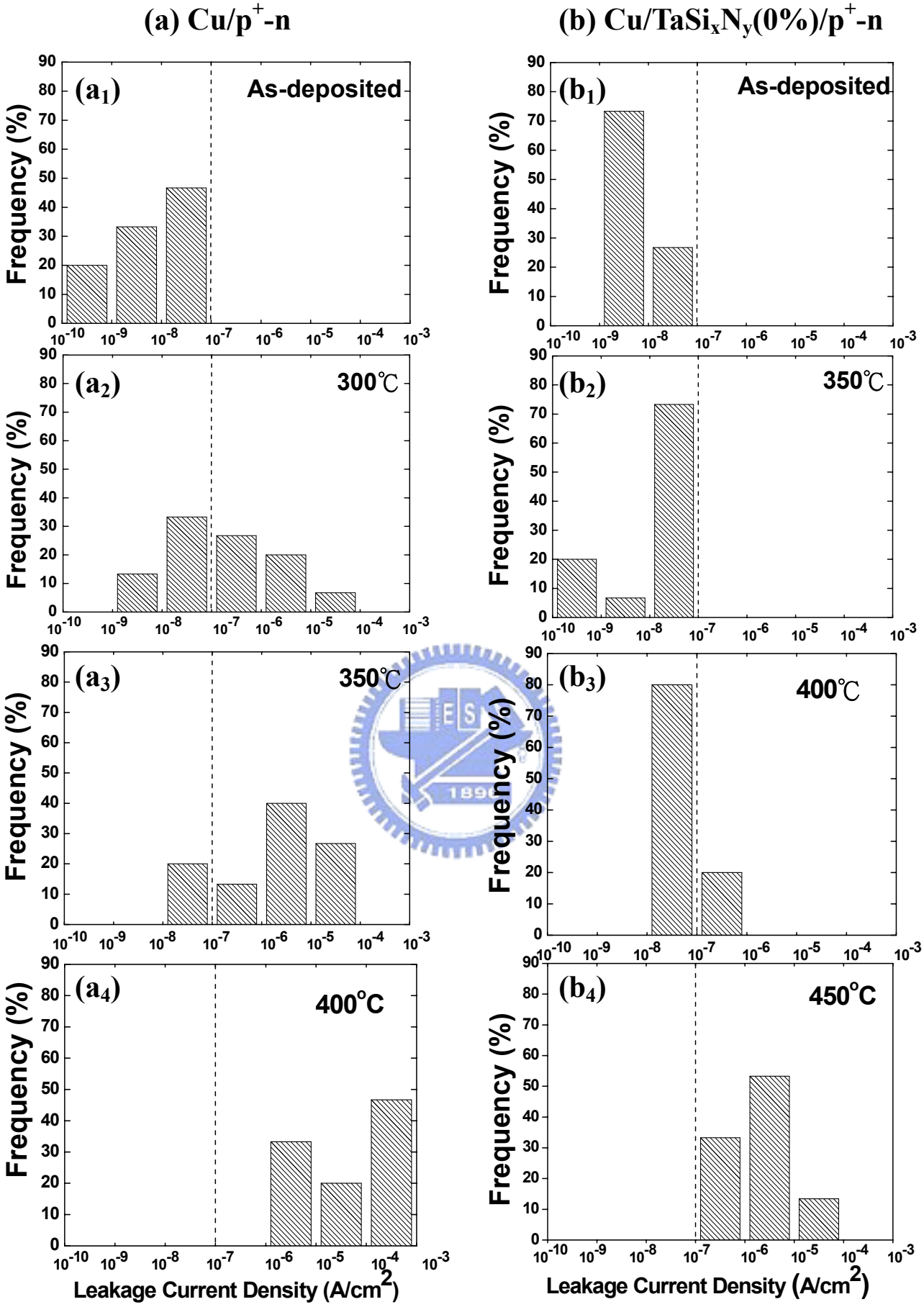


Fig. 3-3 Histograms showing the statistical distribution of reverse bias leakage current density for (a) Cu/p^+-n and (b) Cu/$TaSi_xN_y$(0%)/p^+-n junction diodes annealed at various temperatures for 30min.

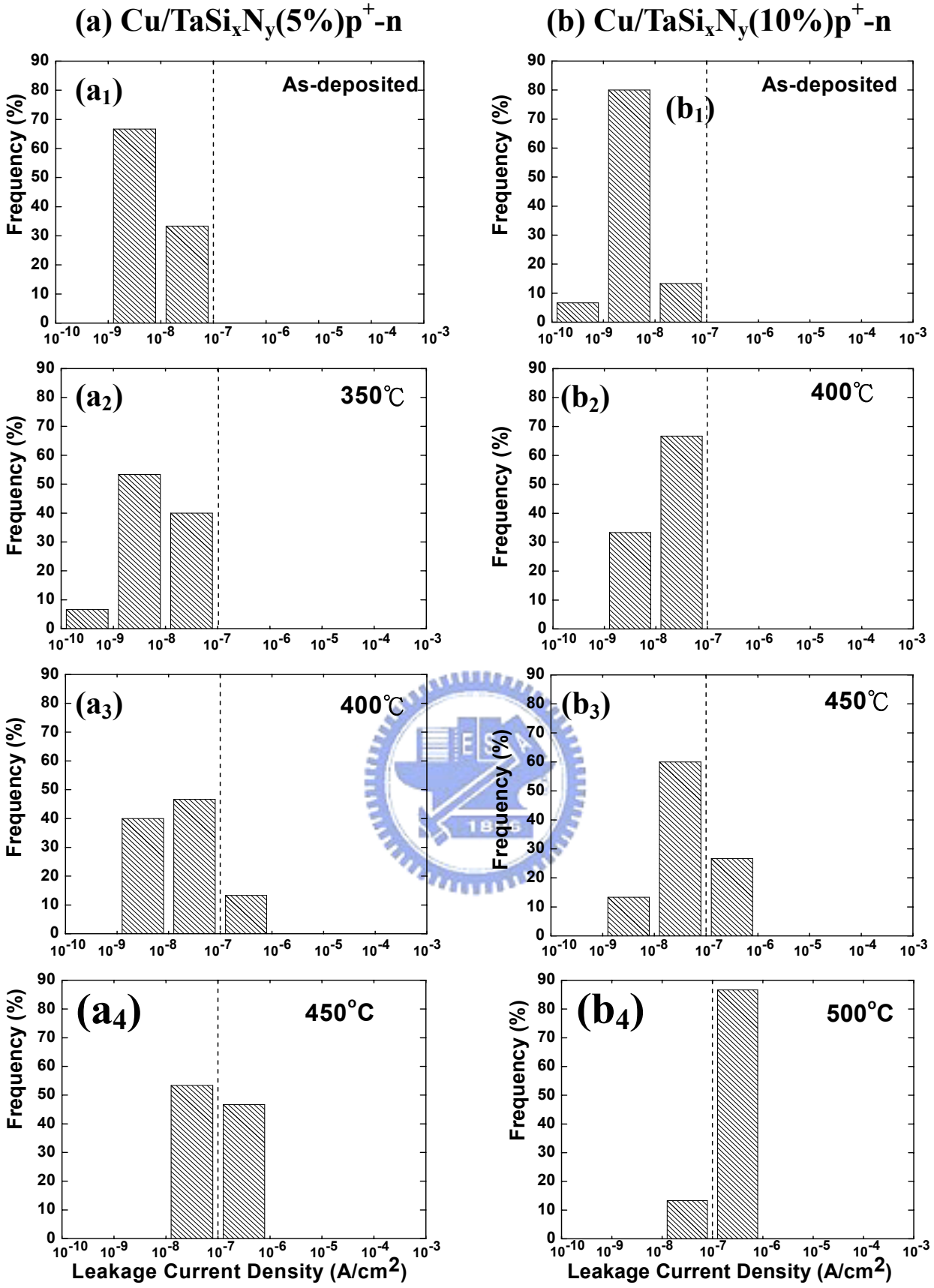
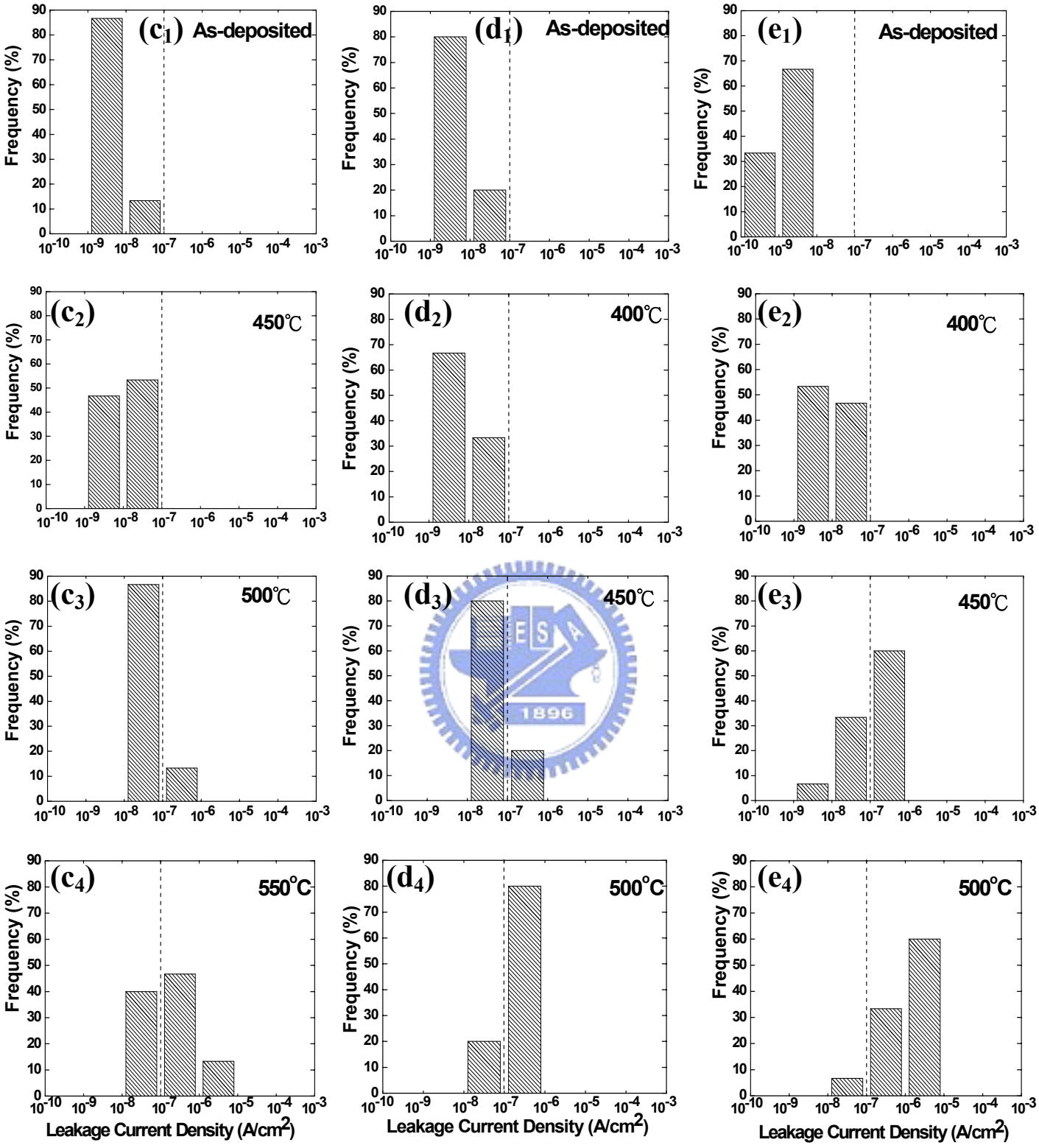


Fig. 3-4 Histograms showing the statistical distribution of reverse bias leakage current density for (a) Cu/TaSi$_x$N$_y$(5%)/p$^+$-n, (b) Cu/TaSi$_x$N$_y$(10%)/p$^+$-n, (c) Cu/TaSi$_x$N$_y$(15%)/p$^+$-n, (d) Cu/TaSi$_x$N$_y$(20%)/p$^+$-n, and (e) Cu/TaSi$_x$N$_y$(25%)/p$^+$-n junction diodes annealed at various temperatures for 30min.



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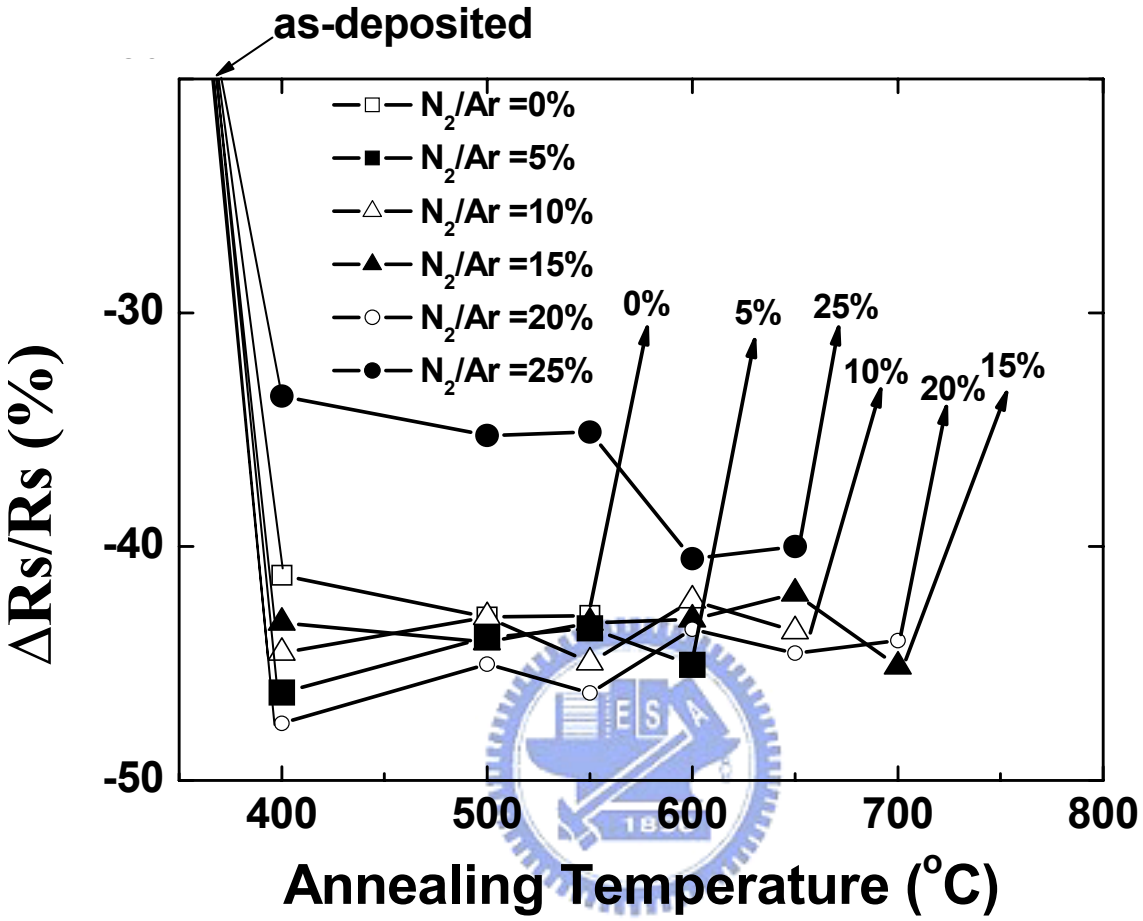


Fig. 3-5 Percentage of sheet resistance change vs. annealing temperature for the Cu/$TaSi_xN_y$/Si samples with the $TaSi_xN_y$ film sputter deposited in a N_2/Ar gas mixture made of various N_2/Ar flow ratios.

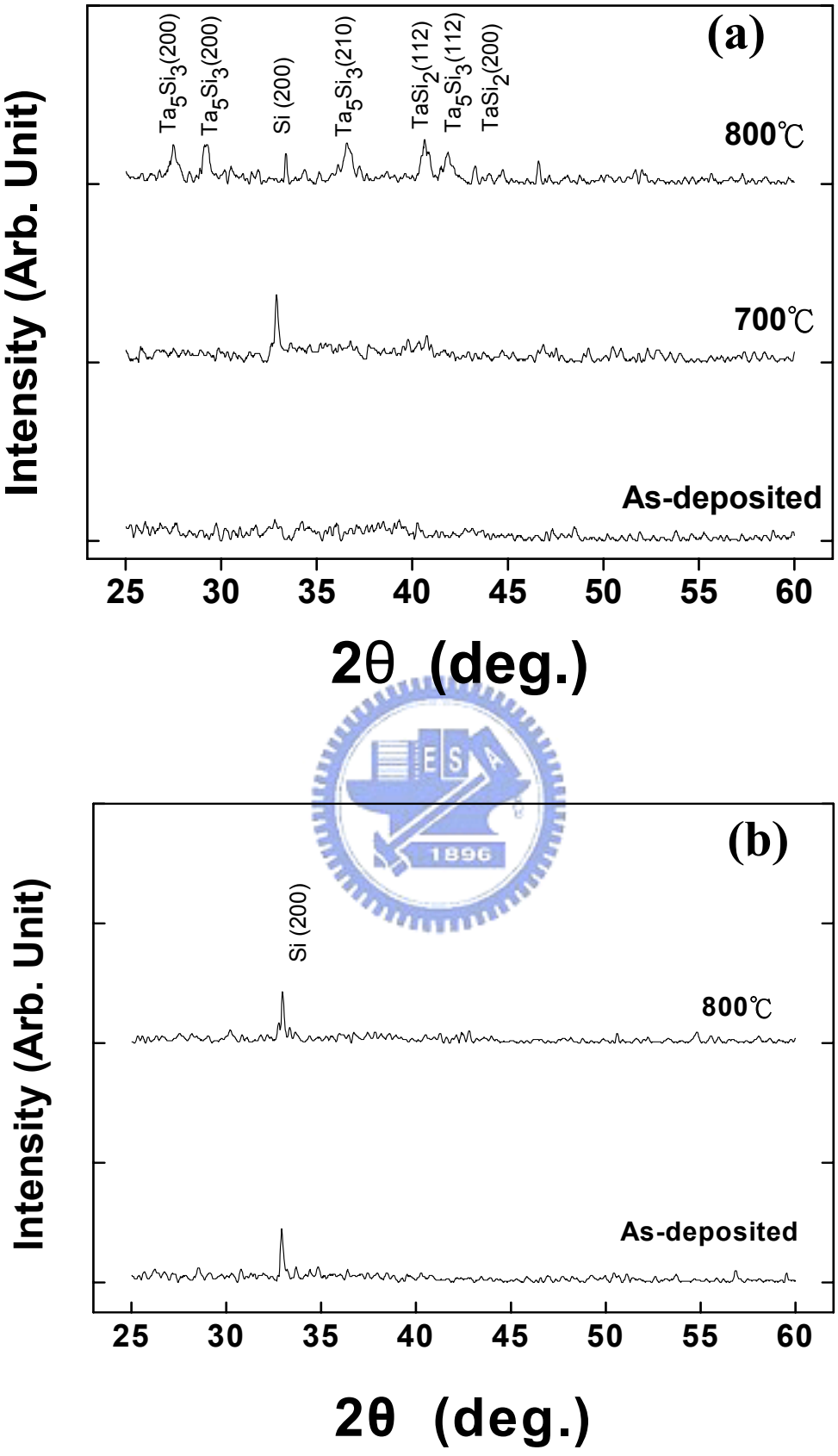


Fig. 3-6 XRD spectra for (a) $TaSi_xN_y$(0%)/Si and (b) $TaSi_xN_y$(15%)/Si samples annealed at various temperatures. Both $TaSi_xN_y$ layers have a thickness of 100 nm.

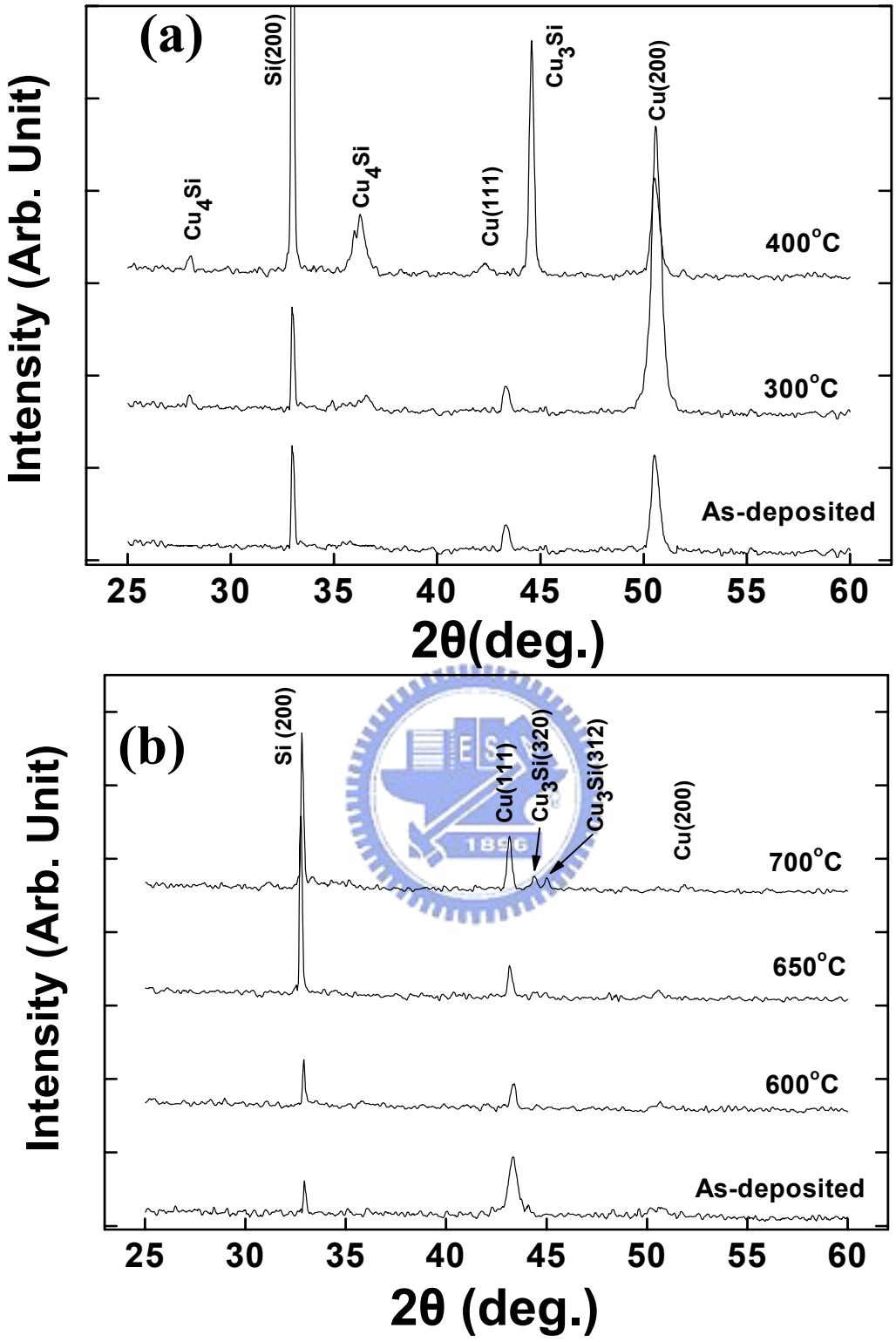
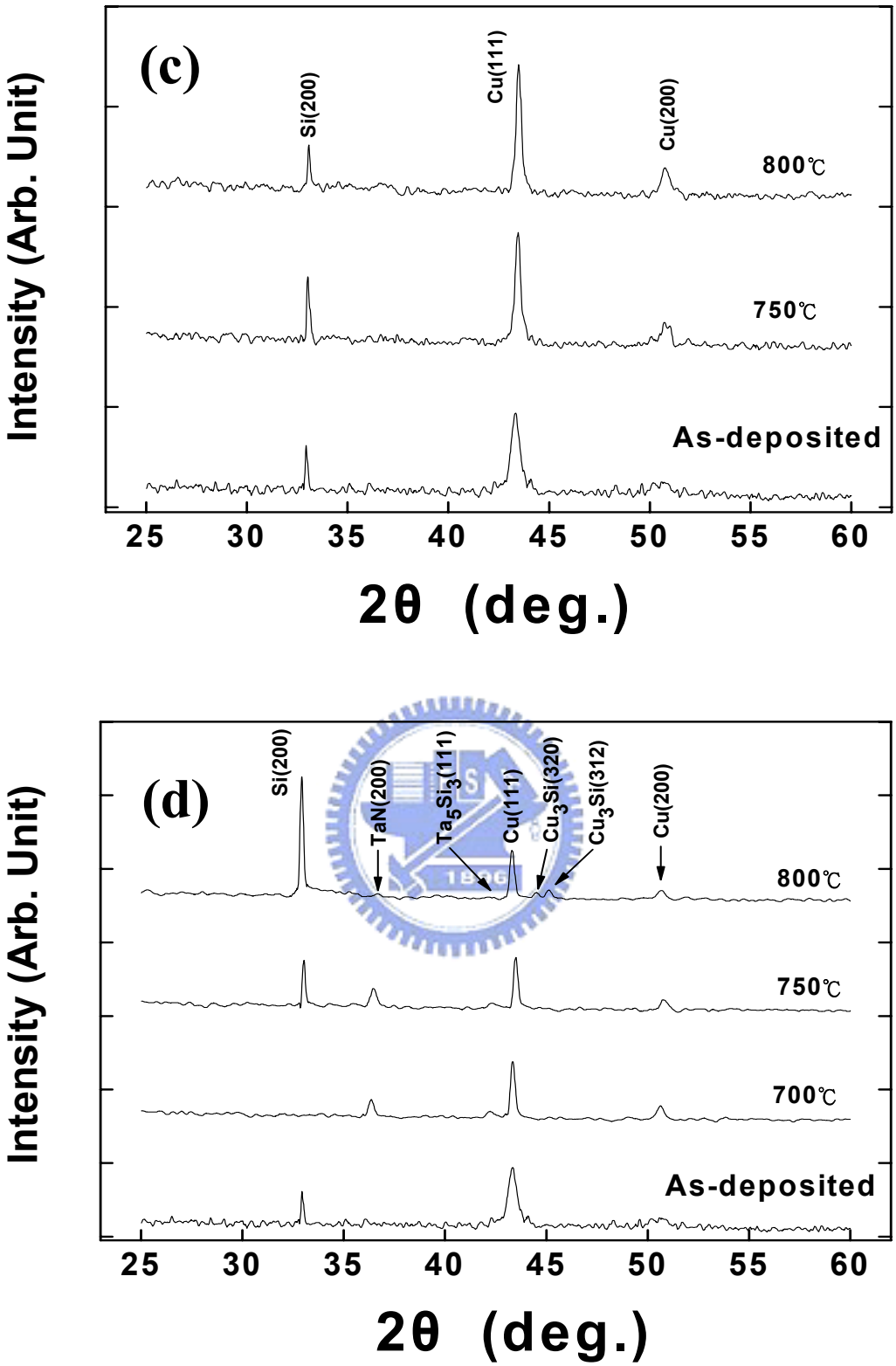


Fig. 3-7 XRD spectra for (a) Cu/Si, (b) Cu/$TaSi_xN_y$(0%)/Si, (c) Cu/$TaSi_xN_y$(15%)/Si and (d) Cu/$TaSi_xN_y$(25%)/Si samples annealed at various temperatures.



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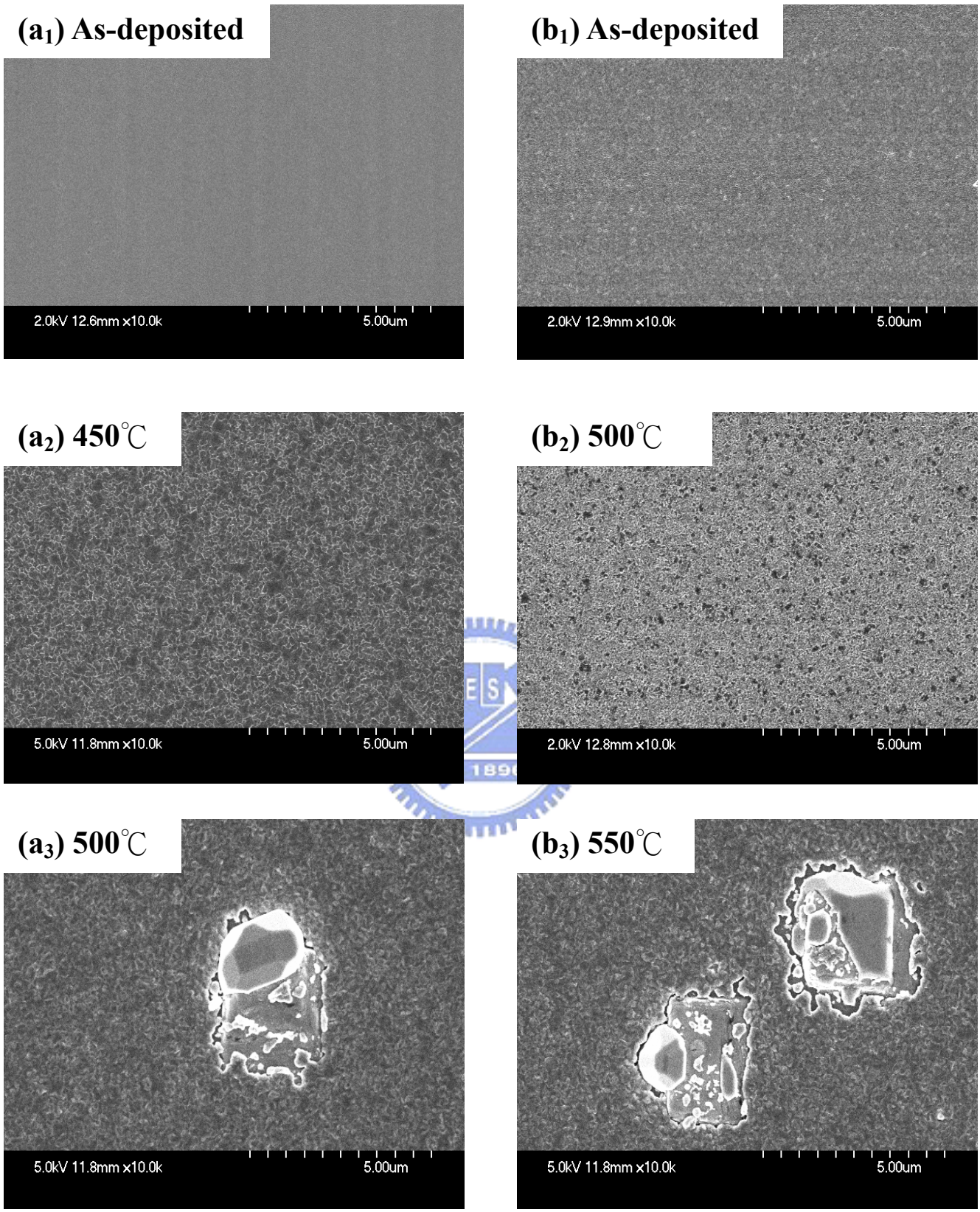
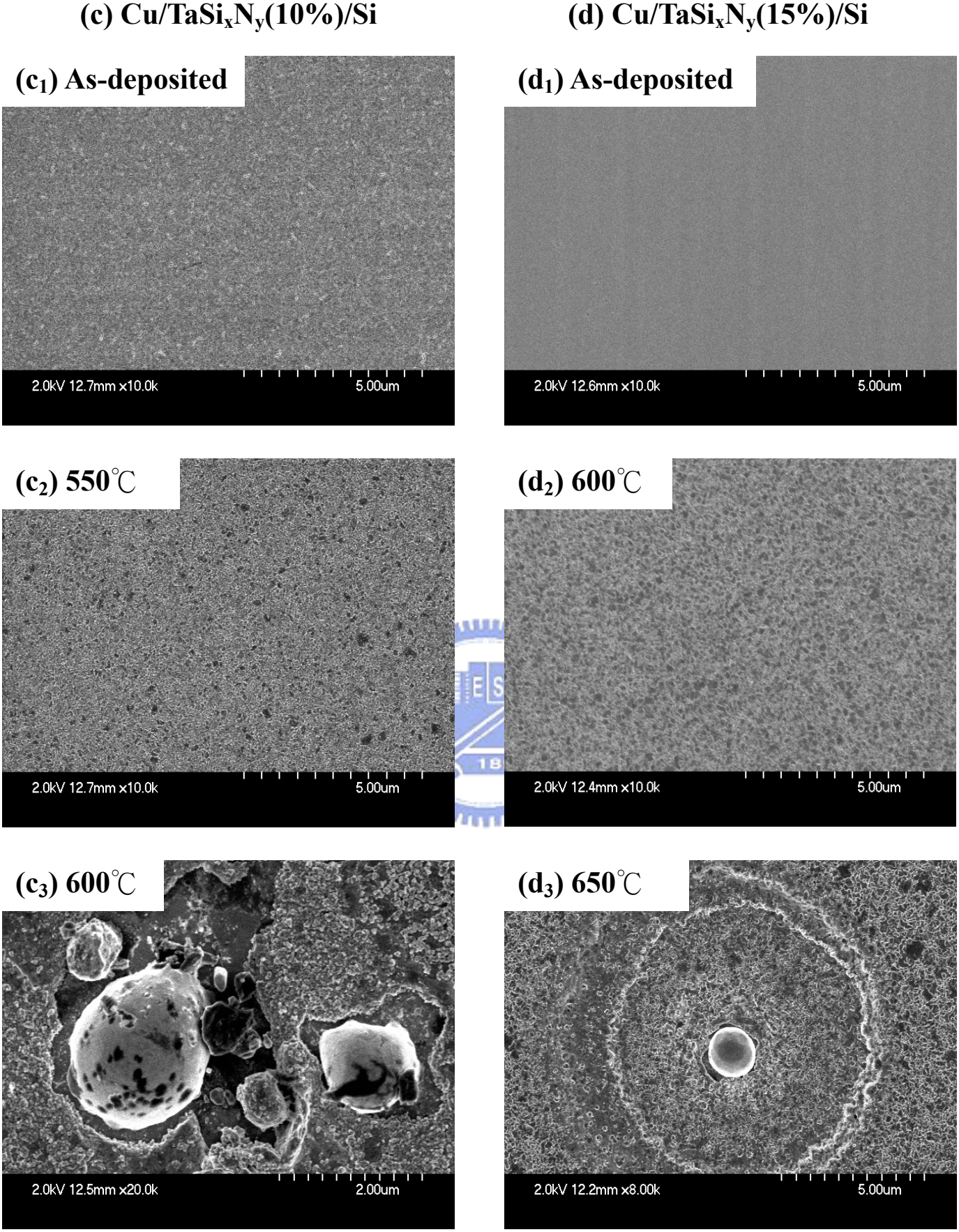


Fig. 3-8 Top view SEM micrographs showing surface morphology for the Cu/barrier/Si samples annealed at various temperatures, with the barrier of (a) $TaSi_xN_y$(0%), (b) $TaSi_xN_y$(5%) (c) $TaSi_xN_y$(10%), (d) $TaSi_xN_y$(15%), (e) $TaSi_xN_y$(20%) and (f) $TaSi_xN_y$(25%).



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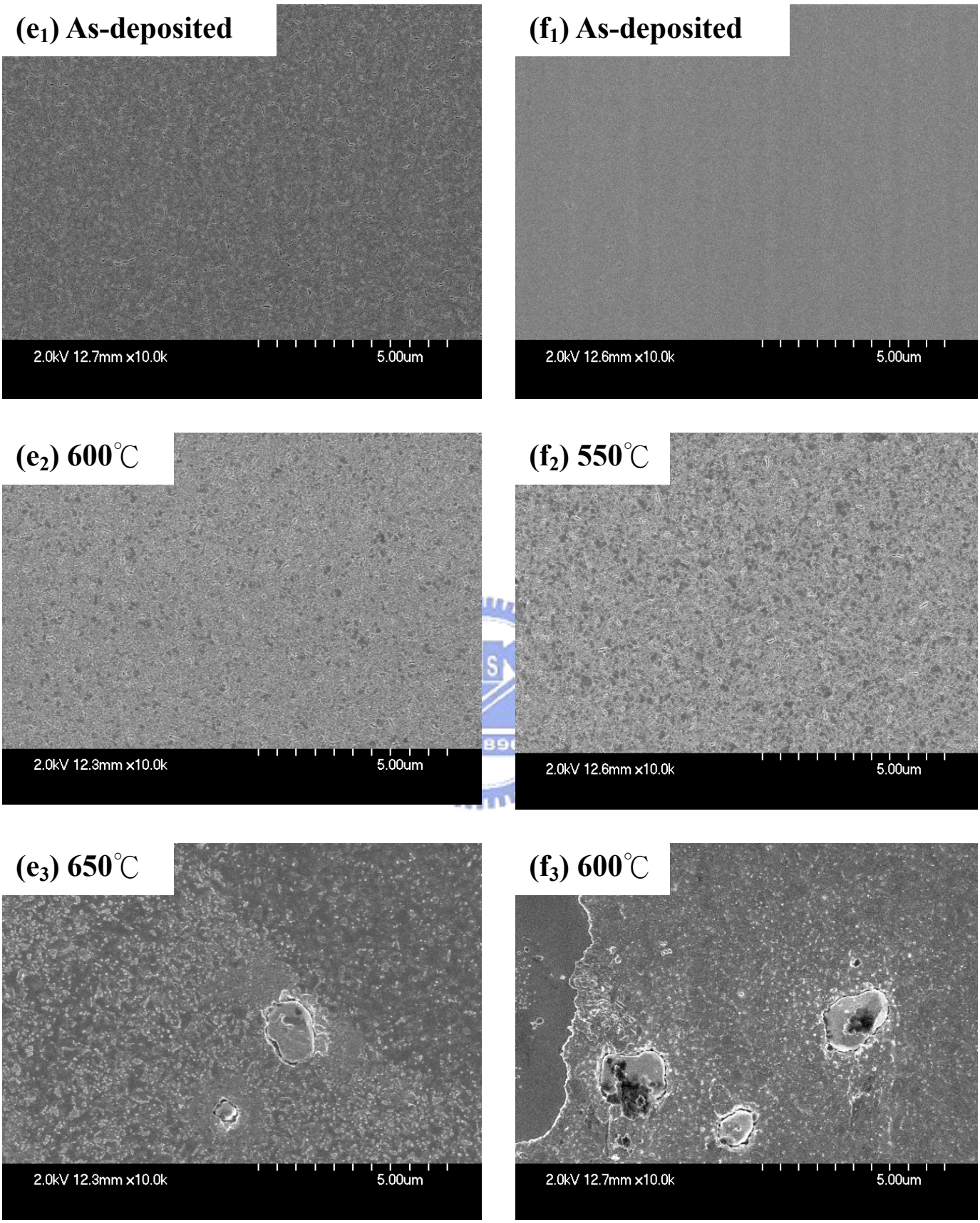

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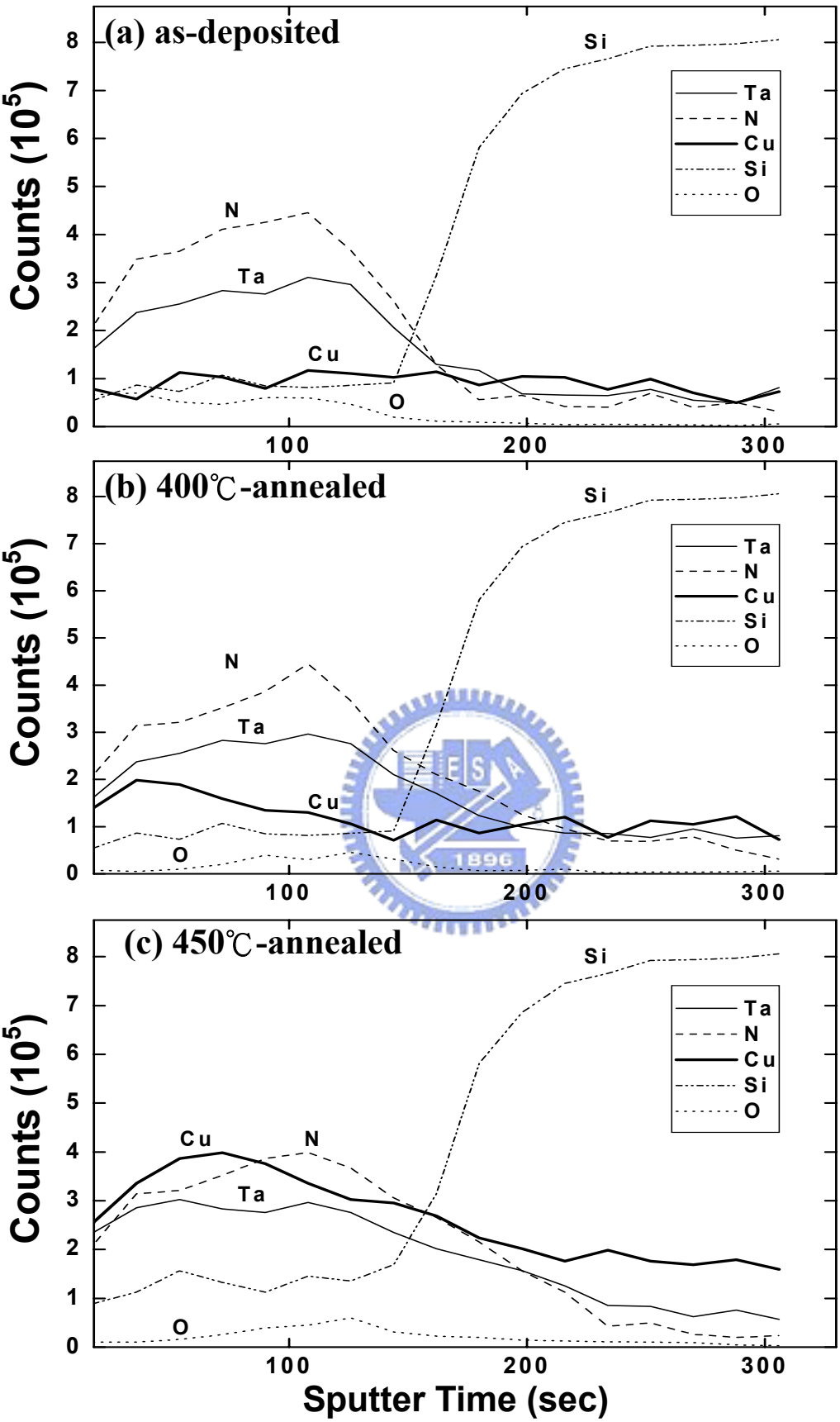

Fig. 3-9 AES depth profiles of Cu/$TaSi_xN_y$(25%)/Si samples (a) as-deposited, and (b) 400 ℃- and (c) 450℃-annealed.

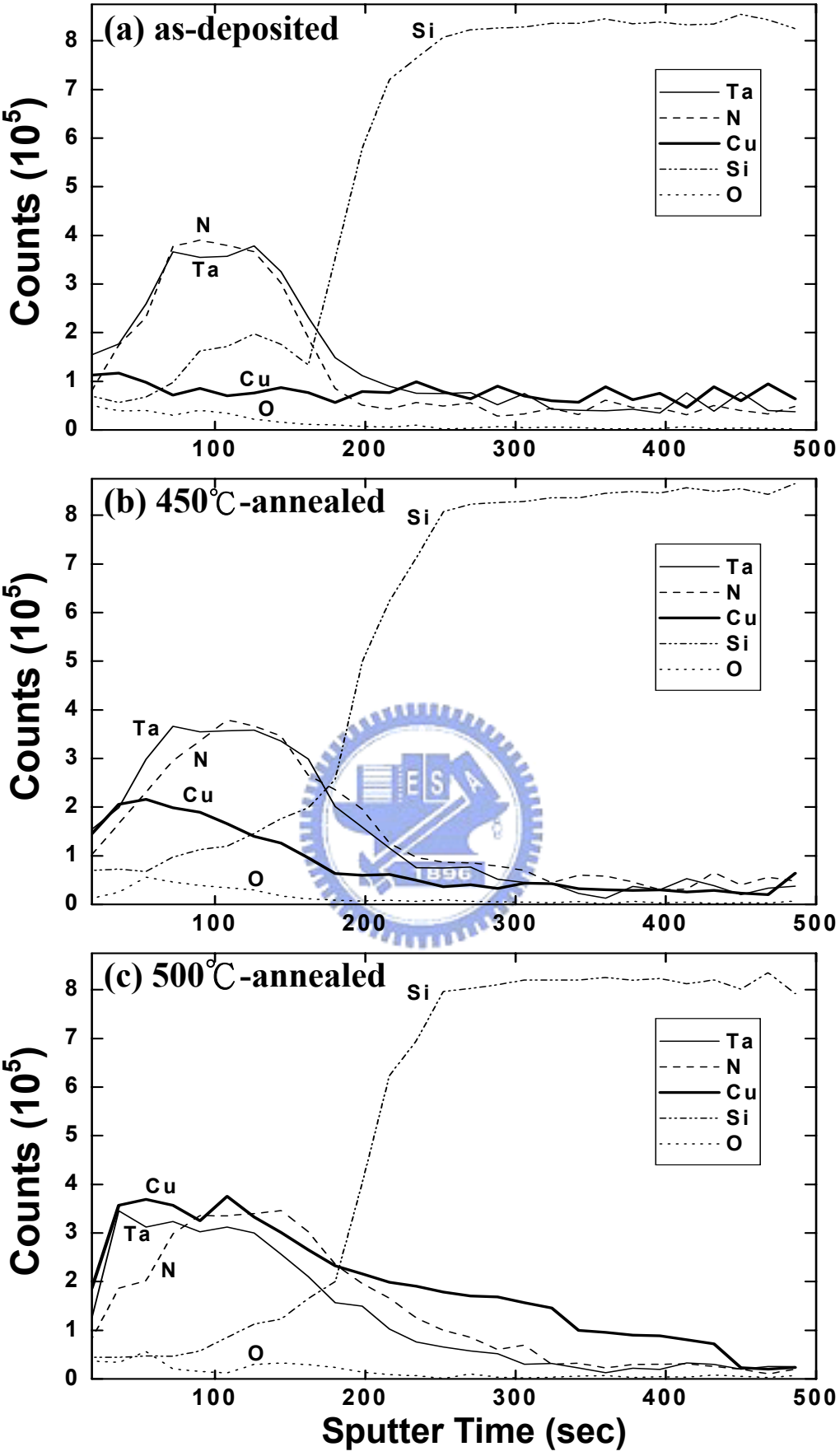

Fig. 3-10 AES depth profiles of Cu/$TaSi_xN_y$(15%)/Si samples (a) as-deposited, and (b) 450 ℃-and (c) 500℃-annealed.