Chapter 4

Improvement of $TaSi_xN_y$ Barrier Property by Post-Deposition Plasma Treatment and Thermal Annealing

4.1 Introduction

There have been a number of reports in the literature regarding the post-deposition treatments on diffusion barrier for the improvement of barrier property against Cu diffusion, such as N_2-plasma and O_2-plasma treatments [33] and N_2-thermal-annealing [34] on Ta-based diffusion barrier. By a N_2-plasma-treatment and/or N_2-thermal-annealing process, a nitrogen-rich thin layer is formed at the surface of the diffusion barrier and the grain boundaries of the diffusion barrier would be stuffed with nitrogen atoms, resulting in efficient suppression of the diffusion of Cu atoms. Moreover, the localized defects can also be healed at the same time during the N_2-thermal-annealing process. In this chapter, we investigate the improvement of the barrier capability of the $TaSi_xN_y$ layer by N_2-thermal-annealing and/or N_2-plasma-treatment on the surface of the barrier layer. The barrier layer used for the post-deposition treatment was $TaSi_xN_y$(15%), which exhibited the best barrier property among the various $TaSi_xN_y$ barrier layers that we studied in Chapter 3. For the samples of the $TaSi_xN_y$(15%) barrier receiving different post-deposition treatments, the following nomenclature is used: $TaSi_xN_y$(A) stands for the barrier layer treated by N_2-thermal-annealing,

$TaSi_xN_y$(B)stands for the barrier layer treated by N_2-plasma, and $TaSi_xN_y$(C)stands for the barrier layer treated by N_2-thermal-annealing followed by N_2-plasma-treatment. The N_2-thermal-annealing was performed in N_2 ambient at a temperature of 500℃ for 30min, while the N_2-plasma-treatment was performed for 10min with a plasma power of 150 watts at a gas pressure of 385 mTorr with N_2 flow rate of 200 sccm and at a substrate temperature of 100℃.

4.2 Property of $TaSi_xN_y$ after Post-Deposition Treatment

Table 4-1 shows the composition of $TaSi_xN_y$(15%) after various post-deposition treatment determined by RBS analysis. Compared to the as-deposited sample, the post-deposition-treated samples all showed significant increase in nitrogen content. The sheet resistance change versus annealing temperature for the three post-deposition treated $TaSi_xN_y$/Si samples is illustrated in Fig. 4-1. It is notable that the as-prepared samples stand for any of the post-deposition-treated $TaSi_xN_y$(15%)/Si samples before they were subjected to thermal annealing. It can be seen from Fig. 4-1 that 400℃ annealing resulted in about 15% decrease in Rs, whereas the samples all exhibited a good thermal stability from 400 to 800℃. Figure 4-2 shows the XRD spectra for the as-prepared and 800℃-annealed $TaSi_xN_y$(A)/Si and $TaSi_xN_y$(C)/Si samples. It is apparent that the amorphous state of both as-prepared samples remained unchanged after annealing at temperatures up to 800℃. The surface morphology of the as-prepared and 800℃-annealed $TaSi_xN_y$(A)/Si samples, as shown in Fig. 4-3, reveals that the

$TaSi_xN_y$(A) film annealed at 800℃ still retained a very smooth surface morphology of nanostructure phase in consistent with the result of XRD analysis (Fig. 4-2).

4.3 Electrical Measurements

Figure 4-4 shows the statistical distributions of reverse bias leakage current density measured at –5 volts for the Cu/$TaSi_xN_y$(A)/p^+-n, Cu/$TaSi_xN_y$(B)/p^+-n and Cu/$TaSi_xN_y$(C)/p^+-n junction diodes annealed at various temperatures. The Cu/$TaSi_xN_y$(A)/p^+-n junction diodes, in which the barrier layer had been treated by N_2-thermal-annealing, were able to sustain a 30min thermal annealing at temperatures up to 500℃ without causing degradation to the diodes electrical characteristics [Fig 4-4(a)]. There is a 50℃ improvement in thermal stability over the Cu/$TaSi_xN_y$/p^+-n junction diodes whose barrier was not treated by the N_2-thermal-annealing [Fig. 3-4(c)]. The Cu/$TaSi_xN_y$(B)/p^+-n junction diodes, in which the barrier layer had been treated by N_2-plasma, were able to remain stable at temperatures up to 550℃ [Fig. 4-4(b)], a further 50℃ improvement over the diodes with N_2-thermal-annealed barrier layer. When we combined the two post-deposition treatments on the surface of the barrier layer, the resultant Cu/$TaSi_xN_y$(C)/p^+-n junction diodes were able to retain the integrity of their electrical characteristics up to a temperature of 600℃ [4-4(c)], indicating the superiority of the double-treated $TaSi_xN_y$(C) barrier layer. It is apparent that the barrier capability of the $TaSi_xN_y$ barrier layer can be efficiently improved by performing a certain post-deposition treatment on the surface of the barrier layer, and that the N_2-plasma-treatment is more efficient in improving the barrier capability than the N_2-thermal-annealing. Moreover, the combined post-deposition-treatment of N_2-thermal-annealing followed by N_2-plasma-treatment resulted in the most efficient $TaSi_xN_y$(C) barrier layer, which revealed a 150 ℃ improvement compared with the as-deposited $TaSi_xN_y$ barrier layer.

4.4 Material Analyses

4.4.1 Sheet Resistance Measurements

Figure 4-5 shows the changes of sheet resistance versus annealing temperature for the Cu/$TaSi_xN_y$/Si samples, in which the $TaSi_xN_y$ barrier had been separately treated with three different post-deposition treatments. After annealing at 400℃, the approximate 80% decrease in Rs for all samples is presumably due to the sputter induced damage recovery of the Cu electrode. Then, the Rs of all samples remained nearly constant up to around 750℃, which is a 50℃ improvement over the barrier without the post-deposition treatment. Upon annealing at 800℃, the sample with a barrier layer of $TaSi_xN_y$(A) exhibited a remarkable increase in Rs, while the sample with a barrier layer of $TaSi_xN_y$(A) showed only a slight increase in Rs, whereas the Rs of the sample with a barrier layer of $TaSi_xN_y$(C) showed no obvious change. This indicates that the barrier capability of the $TaSi_xN_y$(B) is better than that of the $TaSi_xN_y$(A), while the $TaSi_xN_y$(C) layer has the best barrier property against Cu diffusion.

4.4.2 XRD Analyses

The XRD spectra of the Cu/TaSi$_x$N$_y$(A)/Si, Cu/ TaSi$_x$N$_y$(B)/Si and Cu/TaSi$_x$N$_y$(C)/Si samples are illustrated in Fig. 4-6. All the spectra remained the same as the spectrum of the as-prepared sample for all samples annealed at various temperatures up to 750℃. After annealing at 800℃, the Cu/TaSi$_x$N$_y$(A)/Si sample showed the appearance of Cu-silicide and Ta-silicide phases [Fig. 4-6(a)], implying that the structure of the barrier layer was seriously destroyed. Cu-silicide phase also appeared in the XRD spectrum of the 800 ℃ -annealed Cu/TaSi$_x$N$_y$(B)/Si sample [Fig. 4-6(b)], though the intensity of the diffraction peaks was much weaker than that appeared in the Cu/TaSi$_x$N$_y$(A)/Si sample. This may imply a minor reaction between Cu and Si substrate in the Cu/TaSi$_x$N$_y$(B)/Si sample in comparison with the reaction of Cu and Si substrate in the Cu/TaSi$_x$N$_y$(A)/Si sample. In other words, the TaSi$_x$N$_y$(B) layer has a better barrier property than the TaSi$_x$N$_y$(A) layer. As for the Cu/TaSi$_x$N$_y$(C)/Si sample, the XRD spectrum remained unchanged even after the sample was annealed at 800 ℃ [Fig. 4-6(c)]. The appearance of Cu-silicide and/or Ta-silicide contributed to the increase of sheet resistance as shown in Fig. 4-5, and the results of XRD analyses are consistent with those of sheet resistance measurements.

4.4.3 SEM Observation

Figure 4-7 shows the top view (surface morphology) and cross sectional view SEM micrographs for the Cu/TaSi$_x$N$_y$(A)/Si, Cu/TaSi$_x$N$_y$(B)/Si and Cu/TaSi$_x$N$_y$(C)/Si samples annealed at various temperatures. For the Cu/TaSi$_x$N$_y$(A)/Si sample, the surface morphology remained fairly stable after annealing at temperatures up to 650℃ except a minor Cu grain growth; however, cracks appeared on the surface after annealing at 700℃, presumably due to the beginning of the Cu-silicide formation [Fig. 4-7(a)]. After annealing at 750℃, localized protrusions were clearly observed, and the cross sectional view shows a typical feature of Cu_3Si phase that the formation of Cu-silicide broke through the barrier layer and completely destroyed the Cu/barrier/Si structure. Similar phenomena were observed for the samples of Cu/$TaSi_xN_y$(B)/Si [Fig. 4-7(b)] and Cu/$TaSi_xN_y$(C)/Si [Fig. 4-7(c)] except at higher temperatures. Figure 4-8 shows the top view and oblique view SEM micrographs, with a smaller magnification, for the 800°C-annealed samples of Cu/$TaSi_xN_y$(A)/Si, Cu/$TaSi_xN_y$(B)/Si and Cu/$TaSi_xN_y$(C)/Si. There are many more protrusions appeared on the surface of the Cu/$TaSi_xN_y$(A)/Si sample than the Cu/$TaSi_xN_y$(B)/Si sample, while the number of protrusions appeared on the surface of the Cu/$TaSi_xN_y$(C)/Si sample is the least among the three samples investigated. From the results of SEM observation, it is also very clear that the post-deposition treatment with N_2-thermal-annealing followed by N_2-plasma-treatment is the most efficient one for improving the barrier property of $TaSi_xN_y$ layer.

4.4.4 AES Analyses

Figure 4-9 and Fig. 4-10 show, respectively, the AES depth profiles of the Cu/$TaSi_xN_y$(A)/Si and Cu/$TaSi_xN_y$(C)/Si samples; the Cu overlayer of the samples was removed by chemical etching prior to the AES analysis. For the Cu/$TaSi_xN_y$(A)/Si sample, Cu atoms had diffused through the barrier layer to the Si substrate after annealing at 550℃

[Fig.4-9(b)], and deep into the Si substrate after annealing at 600℃ [Fig. 4-9(c)]. As for the Cu/$TaSi_xN_y$(C)/Si sample, Cu diffused into the barrier layer after annealing at 600℃ [Fig. 4-10(b)], and diffused further to the Si substrate after annealing at 650℃ [Fig. 4-10(c)], causing degradation to the devices electrical characteristics [Fig. 4-4(c)].

4.5 Summary

The barrier property improvement of the sputter deposited $TaSi_xN_y$ layer by post-deposition N_2-thermal-annealing, N_2-plasma-treatment, as well as combined N_2-thermal-annealing and N_2-plasma-treatment was investigated using a Cu/barrier/p^+-n structure with electrical measurement and various techniques of material analysis. The comparative thermal stability temperatures of these diffusion barriers determined in the study of this chapter are summarized in Table 4-2. All three post-deposition treatments employed in this study attained efficient barrier property improvement of various degrees, with the N_2-plasma-treatment more efficient than the N_2-thermal-annealing. Moreover, accumulative effect of the combined N_2-thermal-annealing and N_2-plasma-treatment resulted in the most efficient improvement in barrier capability against Cu diffusion. The improvement in the diffusion barrier property may be attributed to the healing of localized defects in the reactively sputter deposited $TaSi_xN_y$ layer by the post-deposition N_2-thermal-annealing, and the formation of a nitrogen rich layer by N_2-plasma-treatment such that nitrogen atoms in this nitrogen rich layer are stuffed into the grain boundaries and localized defects, thus obstructing the diffusion paths of

Cu atoms. In addition, the thermal stability temperature determined by electrical measurement is always the lowest one compared with those determined by various techniques of material analysis. This confirms once again that the technique of electrical measurement is the most sensitive method in detecting the failure of barrier layer employed in a device structure.

Table 4-1 Composition of TaSiN-based diffusion barrier with and without post-deposition treatments

Post-deposition treatment	Composition (Ta : Si : N)
None	1 : 1.88 : 0.96
N_2-thermal-annealing	1 : 1.67 : 1.50
N_2-plasma	1 : 1.44 : 1.26
N_2-thermal-annealing followed by N_2-plasma	1 : 1.65 : 1.70

Table 4-2 Thermal stability temperature (℃) of TaSiN-based diffusion barriers in Cu/barrier/Si structure determined by electrical measurement and various techniques of material analysis.

Measurement /Analysis method	Diffusion Barrier			
	$TaSi_xN_y$(15%)	$TaSi_xN_y$(A)	$TaSi_xN_y$(B)	$TaSi_xN_y$(C)
p^+n junction diodes	450	500	550	600
Sheet resistance (Rs)	700	750	800+	800+
XRD	800	750	750	800+
SEM	600	700	750	800
AES	450	500	N/A	600

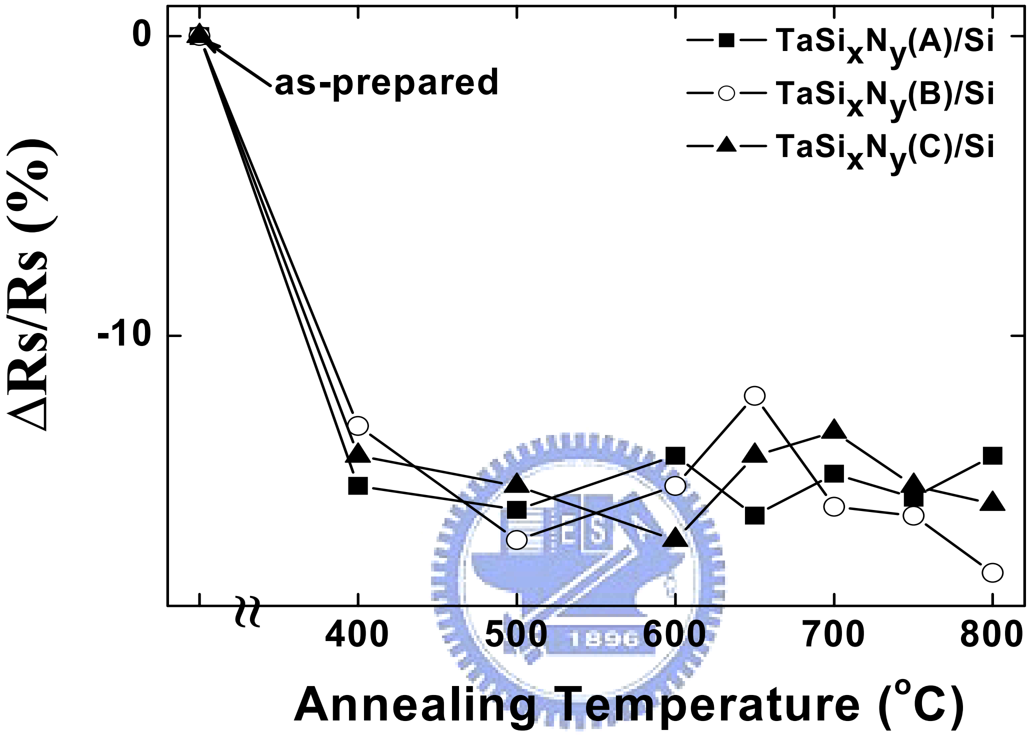


Fig 4-1 Percentage of sheet resistance change vs. annealing temperature for the three post-deposition-treated $TaSi_xN_y$/Si samples. The $TaSi_xN_y$ layer is 100 nm in thickness.

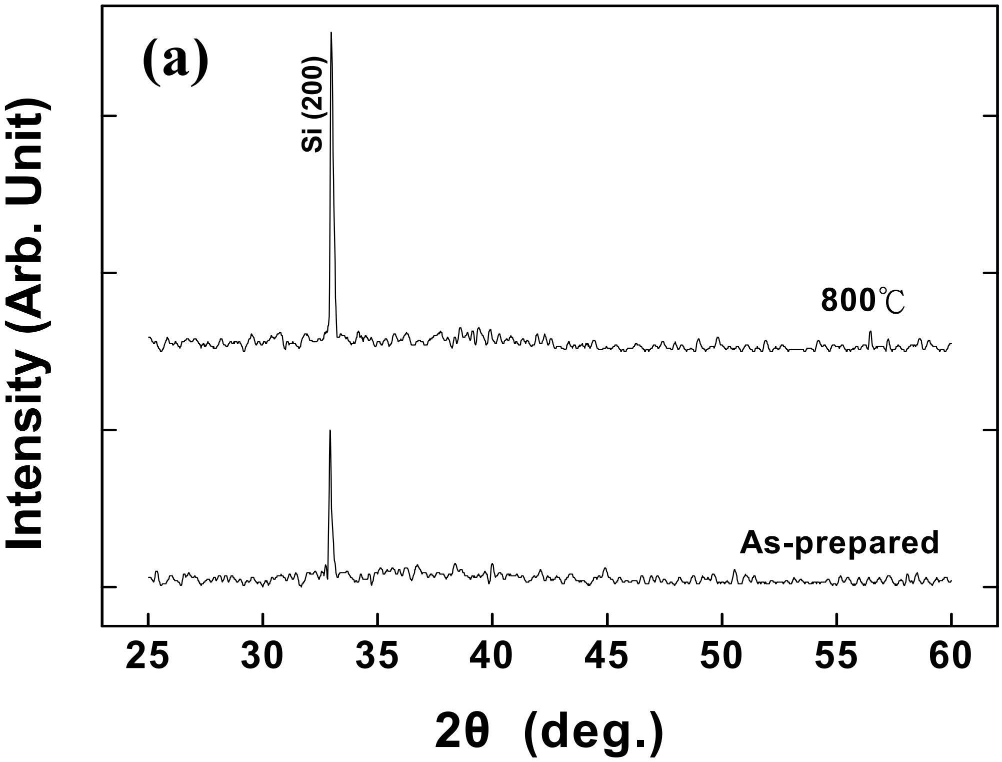
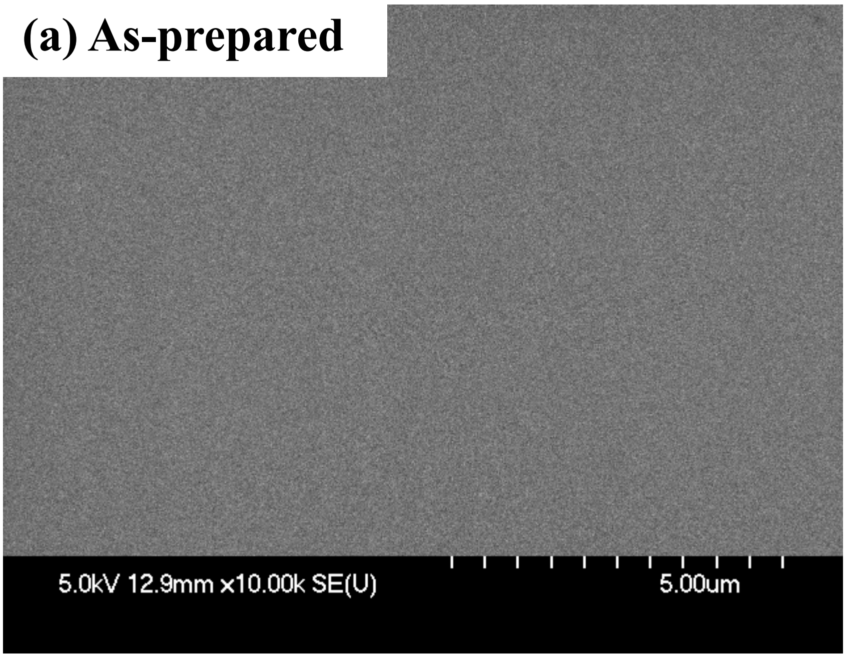


Fig. 4-2 XRD spectra for the as-prepared and 800^{o}C-annealed (a) $TaSi_xN_y$(A)/Si and (b) $TaSi_xN_y$(C)/Si samples. The $TaSi_xN_y$ layers are 100 nm in thickness.


(a) As-prepared

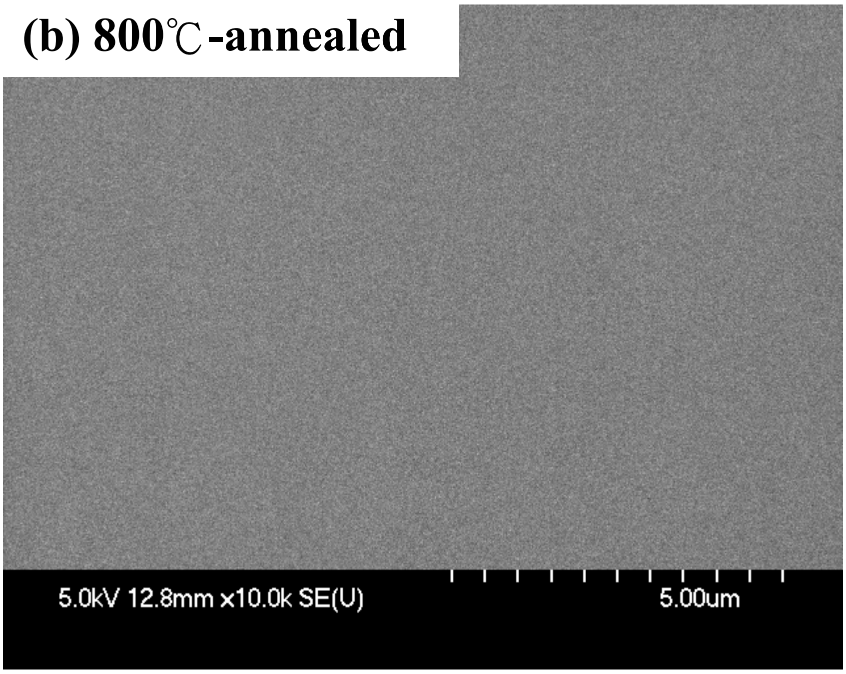

(b) 800℃-annealed

Fig. 4-3 SEM micrographs showing surface morphology of the $TaSi_xN_y$(A)/Si sample (a) as-prepared and (b) 800℃- annealed.

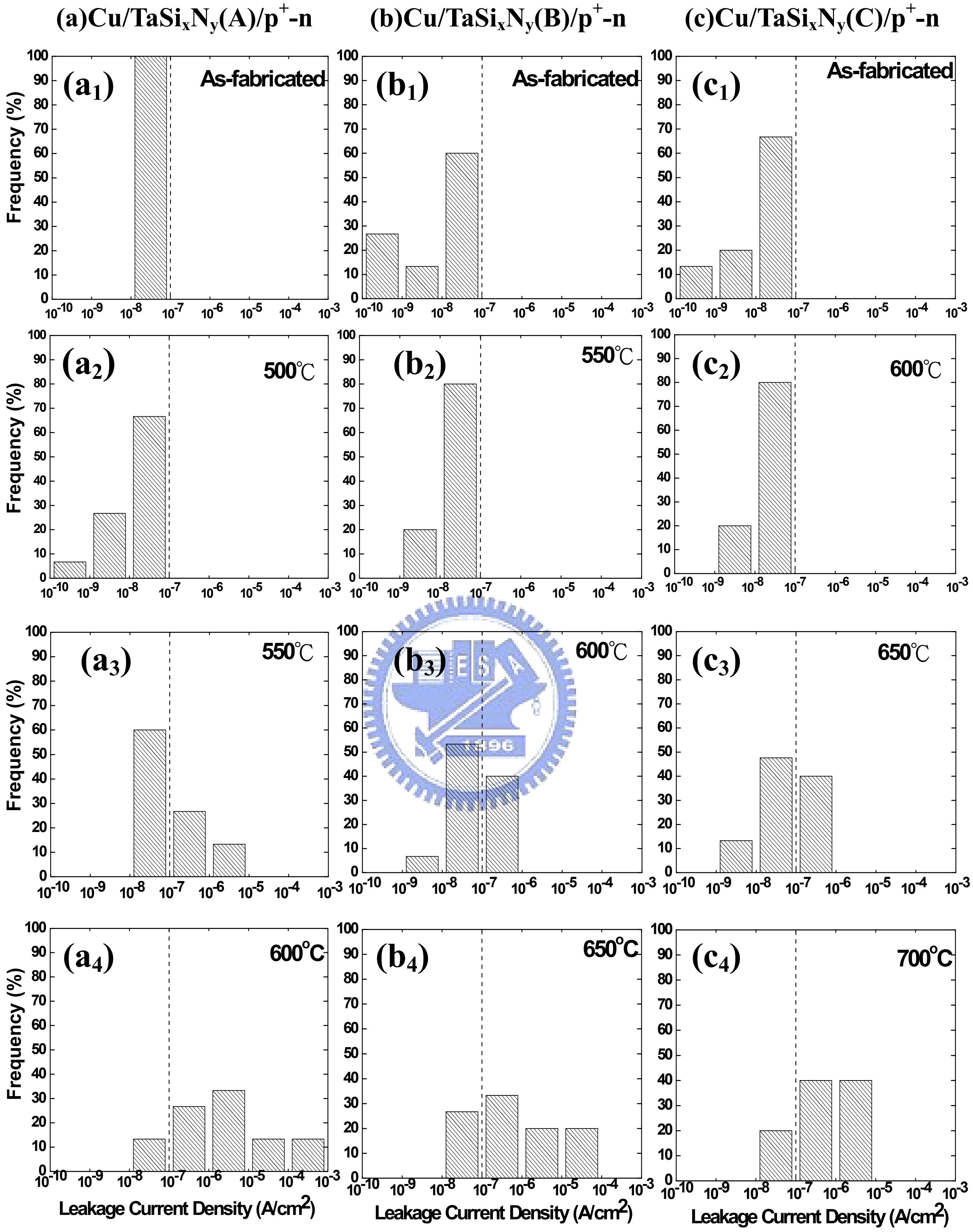


Fig. 4-4 Histograms showing the statistical distribution of reverse bias leakage current density for (a) Cu/TaSi$_x$N$_y$(A)/p$^+$-n, (b) Cu/TaSi$_x$N$_y$(B)/p$^+$-n and (c) Cu/TaSi$_x$N$_y$(**C**)/p$^+$-n junction diodes annealed at various temperatures for 30 min.

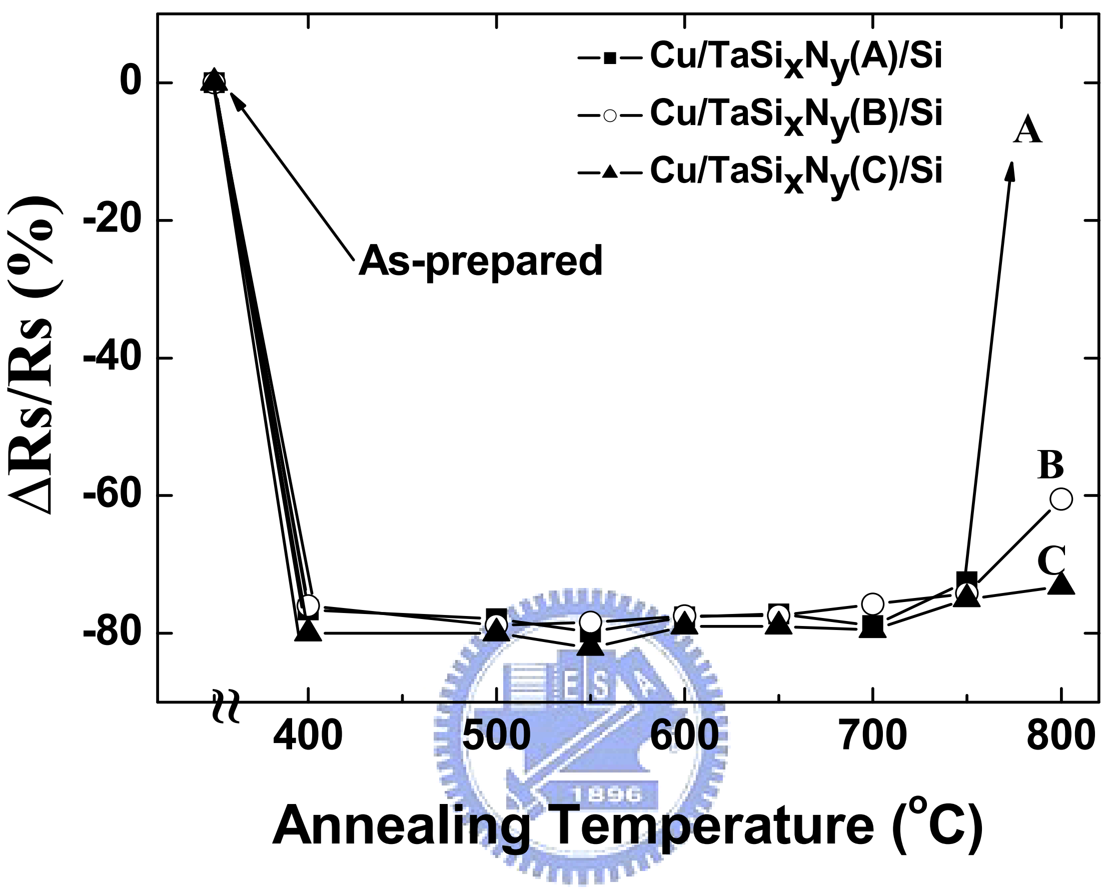


Fig. 4-5 Percentage of sheet resistance change vs. annealing temperature for the Cu/$TaSi_xN_y$/Si samples with the $TaSi_xN_y$ layer being treated separately with three different post-deposition treatments.

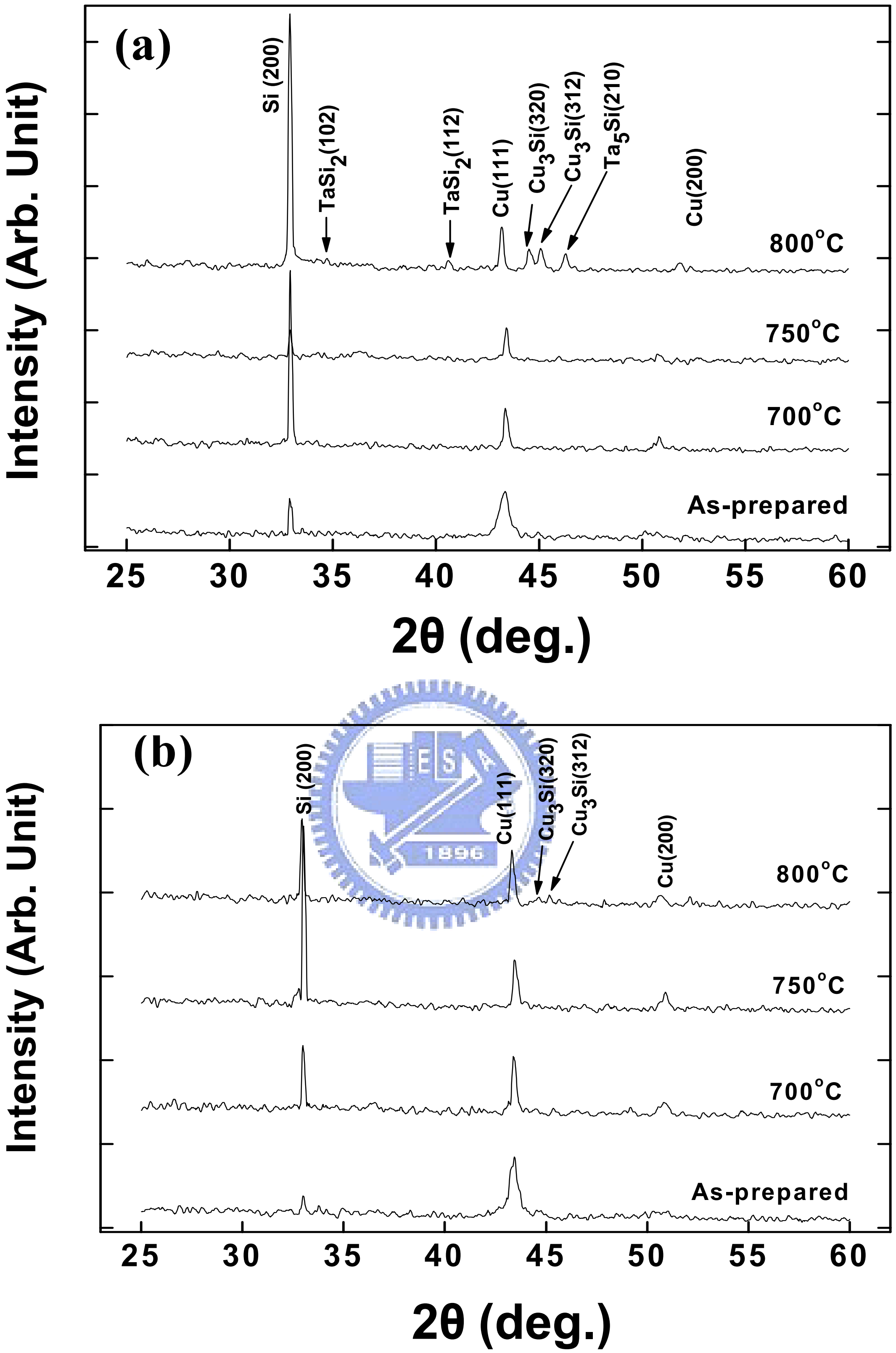


Fig. 4-6 XRD spectra for (a) Cu/$TaSi_xN_y$(A)/Si, (b) Cu/$TaSi_xN_y$(B)/Si and (c) Cu/$TaSi_xN_y$(C)/Si samples annealed at various temperatures.

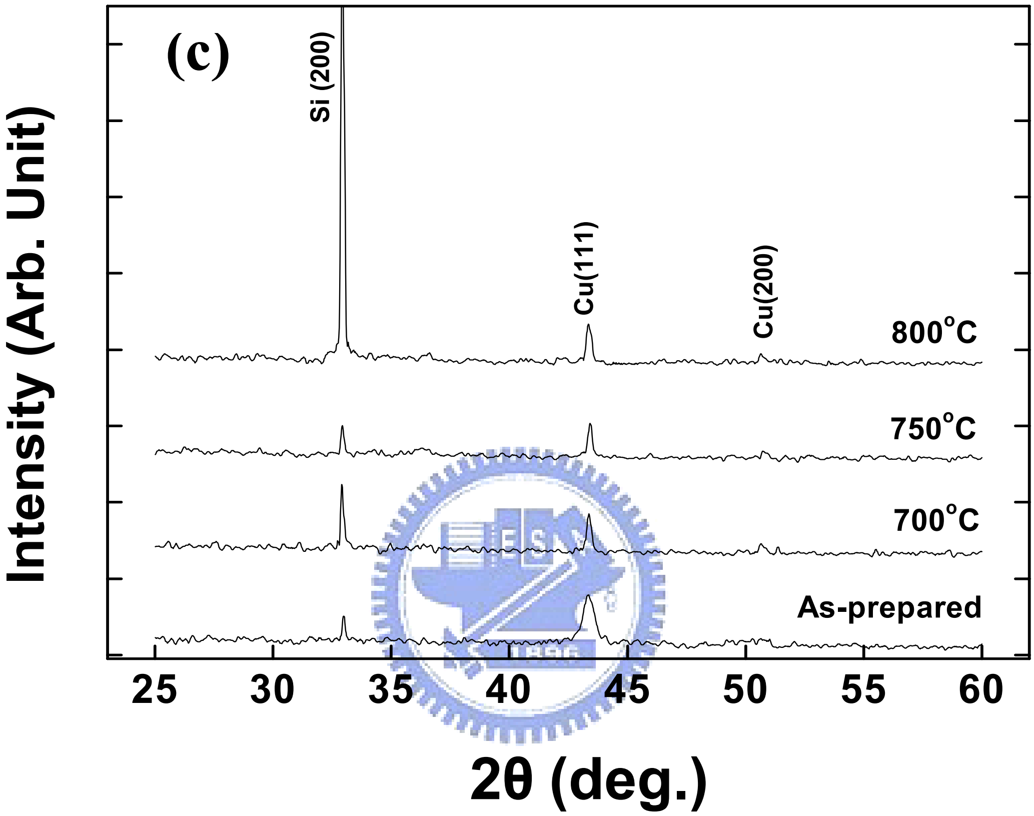


Fig. 4-6 XRD spectra for (a) Cu/TaSi$_x$N$_y$(A)/Si, (b) Cu/TaSi$_x$N$_y$(B)/Si, and (c) Cu/TaSi$_x$N$_y$(C)/Si samples annealed at various temperatures.

(a) Cu/TaSi$_x$N$_y$(A)/Si

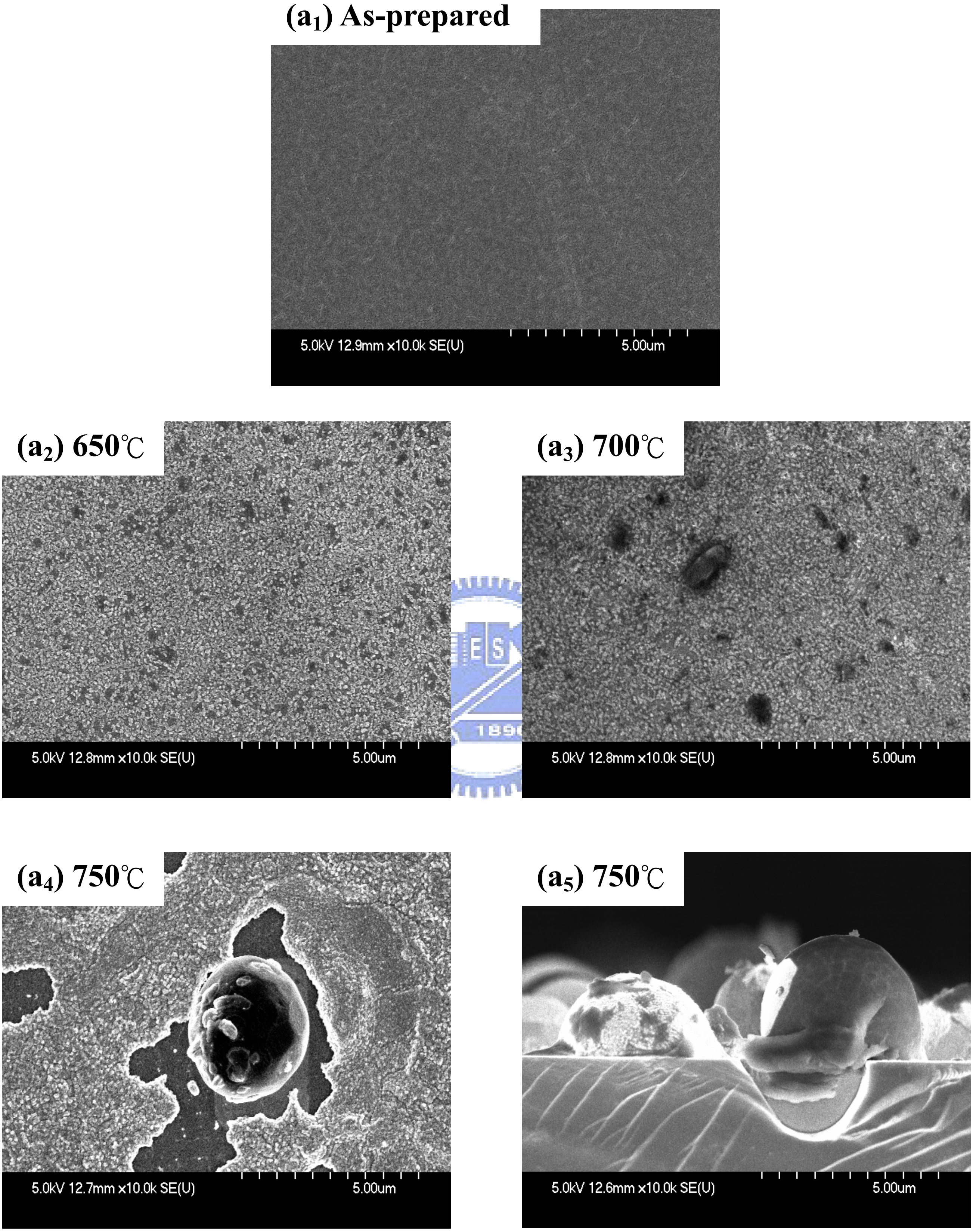


Fig. 4-7 Top view and cross sectional view SEM micrographs for the Cu/barrier/Si samples annealed at various temperatures with a barrier layer of (a) TaSi$_x$N$_y$(A), (b) TaSi$_x$N$_y$(A), and (c) TaSi$_x$N$_y$(C).

(b) Cu/$TaSi_xN_y$(B)/Si

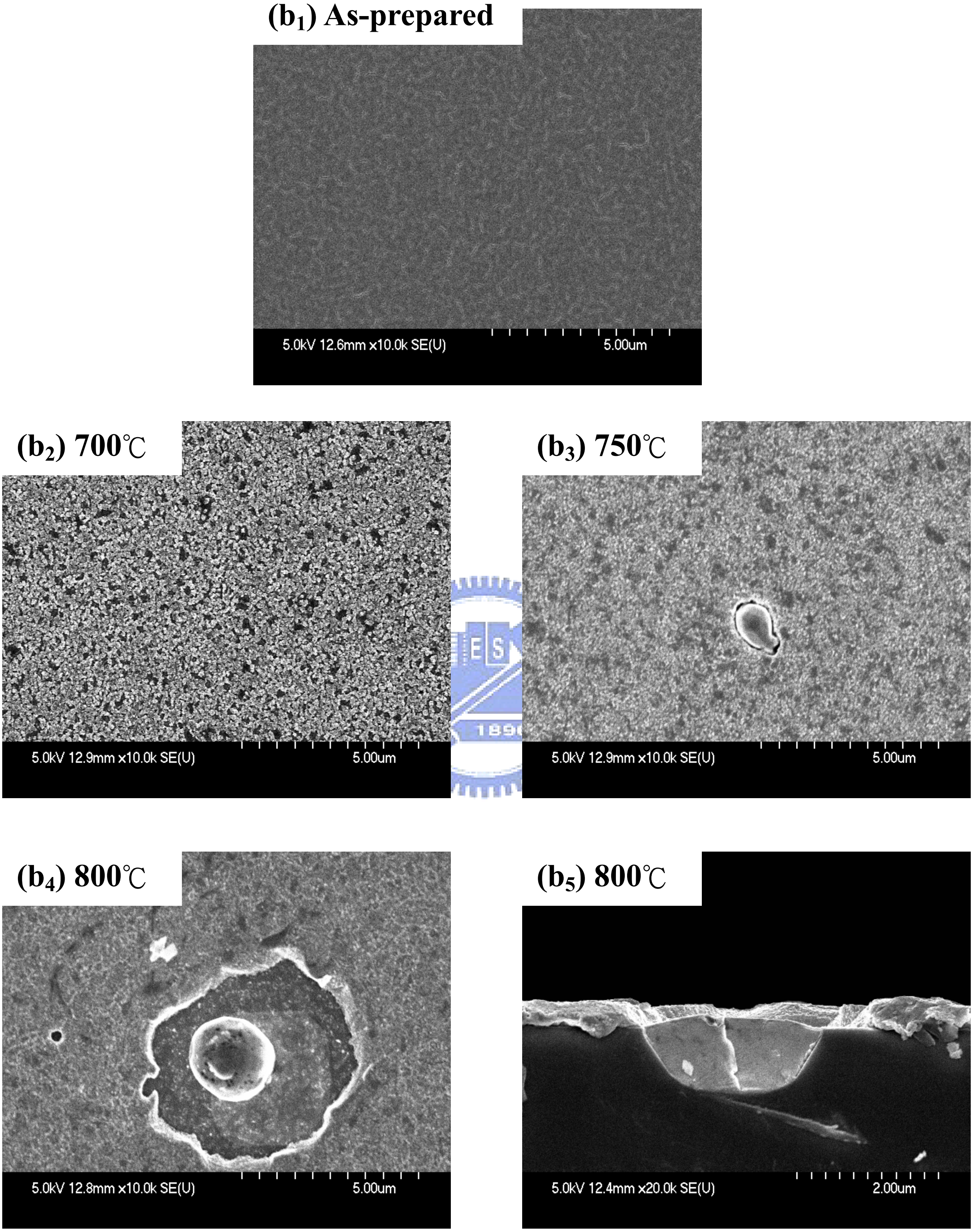


Fig. 4-7 Top view and cross sectional view SEM micrographs for the Cu/barrier/Si samples annealed at various temperatures with a barrier layer of (a) $TaSi_xN_y$(A), (b) $TaSi_xN_y$(B), and (c) $TaSi_xN_y$(C).

(c) Cu/TaSi$_x$N$_y$(C)/Si

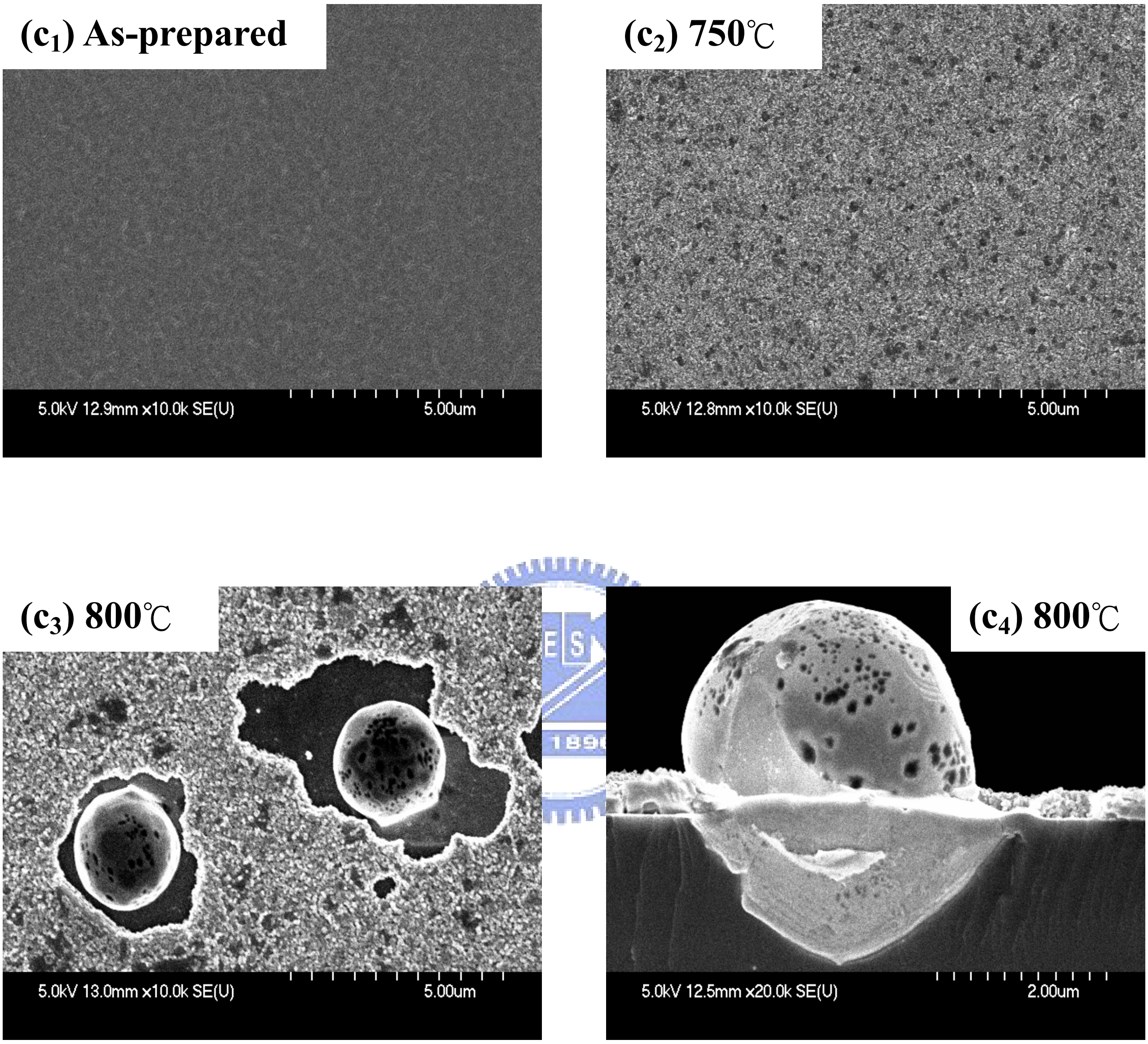


Fig. 4-7 Top view and cross sectional view SEM micrographs for the Cu/barrier/Si samples annealed at various temperatures with a barrier layer of (a) TaSi$_x$N$_y$(A), (b) TaSi$_x$N$_y$(B), and (c) TaSi$_x$N$_y$(C).

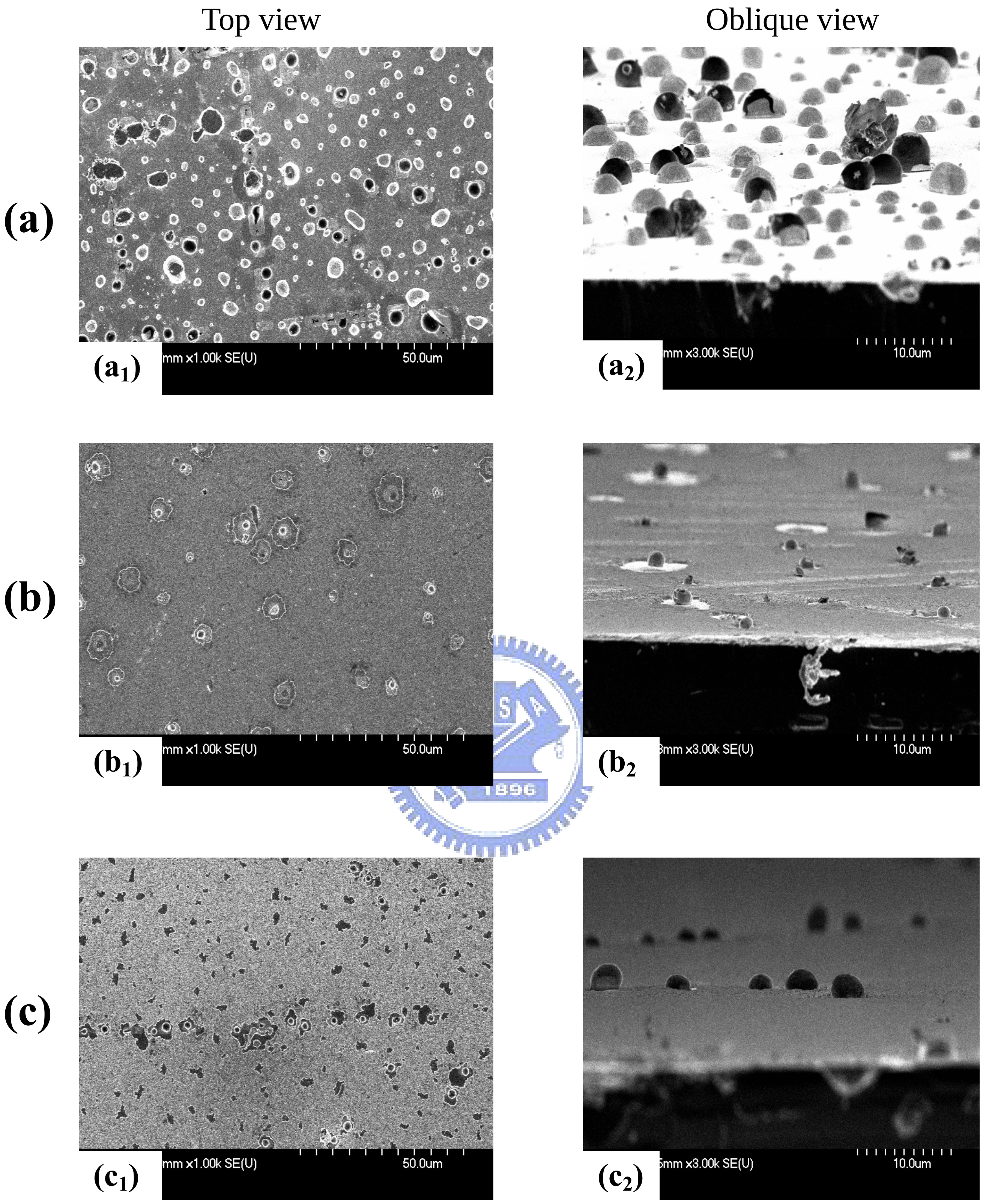


Fig. 4-8 Top view and oblique view SEM micrographs for the Cu/barrier/Si samples annealed at 800℃ with a barrier layer of (a) $TaSi_xN_y$(A), (b) $TaSi_xN_y$(B), and (c) $TaSi_xN_y$(C).

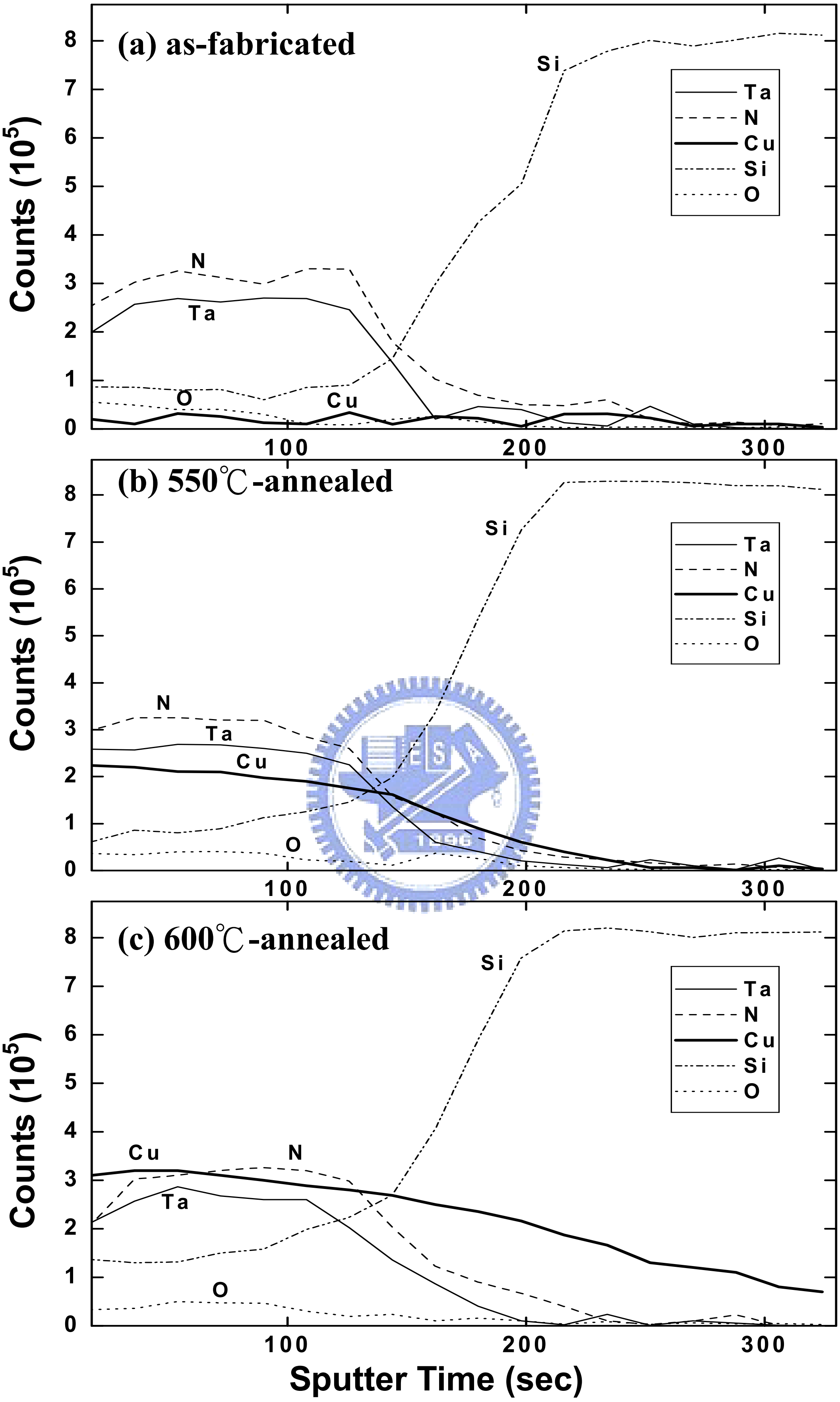


Fig. 4-9AES depth profiles of Cu/TaSi$_x$N$_y$(A)/Si sample (a) as-fabricated, and (b) 550℃- and (c) 600℃-annealed. The Cu-electrode was removed before the AES analysis.

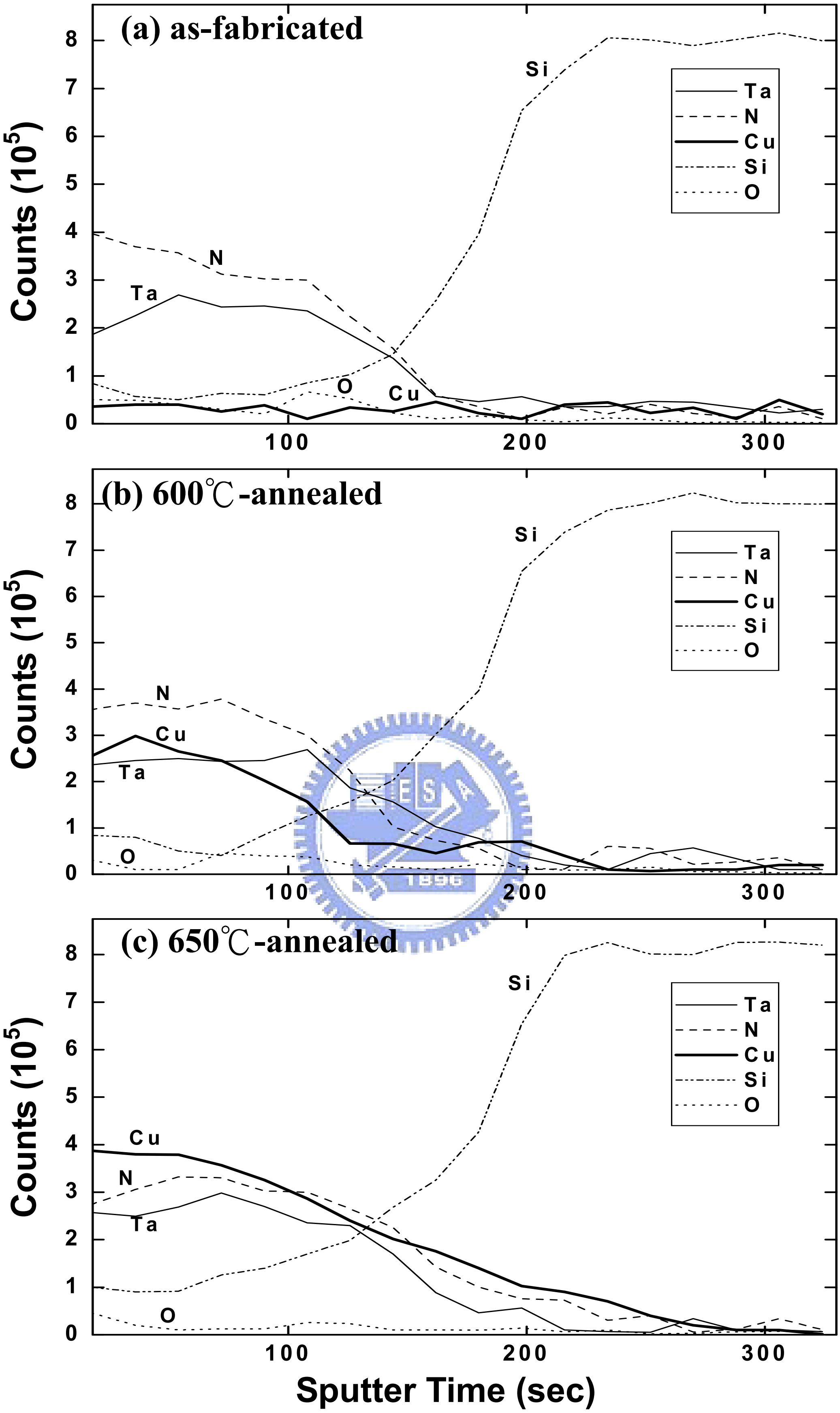


Fig. 4-10 AES depth profiles of Cu/TaSi$_x$N$_y$(C)/Si sample (a) as-fabricated, and (b) 600℃- and (c) 650℃-annealed. The Cu-electrode was removed before the AES analysis.

Chapter 5

Conclusion

This thesis studies the barrier property of very thin (10-nm thickness) $TaSi_xN_y$ barrier layer against Cu diffusion using electrical measurements on Cu/barrier/p^+-n junction diodes as well as various techniques of material analysis. The study also includes the barrier capability improvement of the $TaSi_xN_y$ thin layer by various post-deposition treatments, including N_2-thermal-annealing, N_2-plasma-treatment, and the combination of N_2-thermal-annealing and N_2-plasma-treatment.

The $TaSi_x$ layer, sputter deposited using a $TaSi_2$ target in Ar ambient, was able to make the Cu/$TaSi_x$/p^+-n junction diodes capable of sustaining a 30min thermal annealing at temperatures up to 350℃. The $TaSi_xN_y$ layers, sputter deposited on Si substrates using a $TaSi_2$ target in N_2/Ar mixed ambient, were able to remain in the state of amorphism at temperatures up to 800℃, irrespective of receiving the post-deposition N_2-thermal-annealing and/or N_2-plasma-treatment. The $TaSi_xN_y$ layer of the most efficient barrier property can be obtained by sputter deposition in a N_2/Ar mixed ambient with the N_2/Ar flow ratio of 15 to 20%. The Cu/$TaSi_xN_y$/p^+-n junction diodes with this optimal 10-nm-thick $TaSi_xN_y$ barrier layer, were able to remain thermally stable at temperatures up to 450℃.

The barrier capability of the $TaSi_xN_y$ thin layer can be improved by thermal annealing in N_2 ambient and/or N_2-plasma-treatment on the $TaSi_xN_y$ surface. For the $TaSi_xN_y$(15%) layer (sputter deposited in N_2/Ar mixed ambient with the N_2/Ar flow ratio of 15%) thermally annealed at 500℃ for 30min, the thermally stable temperature of the Cu/ $TaSi_xN_y$(15%)/p^+-n junction diodes was determined to be 500℃, which was 50℃ improvement over the $TaSi_xN_y$ barrier layer without the N_2-thermal-annealing. With 150W N_2-plasma-treatment for 10min on the surface of the $TaSi_xN_y$(15%) layer, 100℃ improvement over the bare $TaSi_xN_y$(15%) layer was obtained. Moreover, the combined post-deposition-treatment of N_2-thermal-annealing followed by N_2-plasma-treatment resulted in the most efficient barrier layer, which revealed a 150℃ improvement over the as-deposited $TaSi_xN_y$(15%) barrier layer. The improvement in the diffusion barrier property may be attributed to the healing of localized defects in the reactively sputter deposited $TaSi_xN_y$ layer by the post-deposition N_2-thermal-annealing, and the formation of a nitrogen rich surface layer by N_2-plasma-treatment such that nitrogen atoms are stuffed into the grain boundaries and localized defects, thus obstructing the diffusion paths of Cu atoms.

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TaSi$_x$N$_y$ 薄膜對銅原子擴散之阻障特性

Barrier Properties of TaSi$_x$N$_y$ Thin Films against Cu Diffusion