

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

利用四氟化碳電漿處理提昇
低溫覆晶矽薄膜電晶體之特性及可靠度



**Performance and Reliability Improvements in
Low-Temperature Polysilicon Thin-Film Transistors
with CF₄ Plasma Treatment**

研究生：羅韋翔
指導教授：雷添福 博士

中華民國 九十三年六月

利用四氟化碳電漿處理提昇
低溫覆晶矽薄膜電晶體之特性及可靠度

**Performance and Reliability Improvements in
Low-Temperature Polysilicon Thin-Film Transistors
with CF₄ Plasma Treatment**

研 究 生：羅韋翔

Student: Wei-Hsiang Lo

指導教授：雷添福 博士

Advisor: Dr. Tan-Fu Lei

國立交通大學

電子工程學系 電子研究所碩士班



Submitted to Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of

Master of Science

in

Electronic Engineering

June 2004

Hsinchu Taiwan Republic of China

中華民國 九十三年六月

利用四氟化碳電漿處理提昇低溫覆晶矽薄膜電 晶體之特性及可靠度


學生：羅韋翔

指導教授：雷添福 博士

國立交通大學

電子工程學系 電子研究所碩士班

摘 要



主動矩陣液晶顯示器 (AMLCDs) 因為其輕、薄、低輻射量及低耗電量的種種優點，近年來已經漸漸地取代了傳統的陰極射線管 (CRT) 顯示器。主動矩陣液晶顯示器以往都是利用非晶矽薄膜電晶體來當作畫素開關元件。然而如果要把週邊驅動電路一起整合到主動矩陣的玻璃基板上，低溫覆晶矽薄膜電晶體肯定是唯一的選擇，這也是近幾年來低溫覆晶矽薄膜電晶體一直被廣為研究的主要原因。

在本論文中，我們提出利用四氟化碳 (CF_4) 電漿處理來改善低溫覆晶矽薄膜電晶體的電特性及可靠度。在電特性的改善方面，四氟化碳電漿中的氟能修補界面處的不完全鍵結，減少界面處及覆晶矽通

道中的缺陷，進而提高了覆晶矽薄膜電晶體的導通電流及場效遷移率，並使得關閉態的漏電流及次臨限擺幅(Subthreshold-Swing)降低。在可靠度的提昇方面，在受到熱載子應力測試 (Hot-carrier stress) 及自我加熱應力測試 (Self-heating stress) 後，經過四氟化碳電漿處理的低溫覆晶矽薄膜電晶體會有較輕微的特性衰退，這是因為氟與矽原子的強鍵結取代了原本較弱的氫與矽原子以及矽與矽原子鍵結。

最後，我們利用了不同的電應力測試 (Stress) 條件來觀察熱載子 (Hot-carrier) 所引發的元件衰退，進一步提出元件劣化的機制。我們發現導通電流與關閉電流的變異會隨電應力測試條件以及量測之汲極電壓 (V_{DS}) 改變而不同，這是因為不同的電應力測試條件會造成不同數量的閘極絕緣層捕捉電荷或覆晶矽通道缺陷。

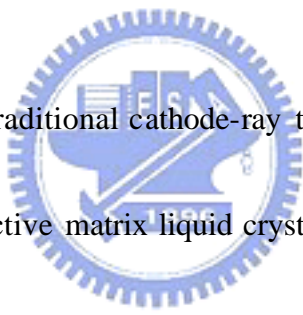
Performance and Reliability Improvements in Low-Temperature Polysilicon Thin-Film Transistors with CF₄ Plasma Treatment

Student: Wei-Hsiang Lo

Advisor: Dr. Tan-Fu Lei

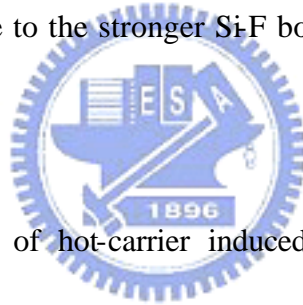
Department of Electronics Engineering &
Institute of Electronics
National Chiao Tung University

ABSTRACT



In the past few years, traditional cathode-ray tube (CRT) displays have been being replaced gradually by active matrix liquid crystal displays (AMLCDs) because of their diverse advantages such as lightweight, flimsy, low radiation and low power consumption. Hydrogenated amorphous thin-film transistors (a-Si:H TFTs) were utilized for the pixel-switching devices in AMLCDs. However, low temperature polycrystalline silicon thin-film transistor (LTPS TFT), undoubtedly, is the only candidate for integrating the peripheral driver circuits onto the glass substrates of the active matrix. It is the major reason that the LTPS TFTs have been studied widely in recent years.

In this thesis, we proposed that the electrical characteristics and reliability of the LTPS TFTs can be improved significantly by utilizing the CF_4 plasma treatment. The incorporated fluorine can replace the dangling bonds and strain bonds in the poly-Si channel and $\text{SiO}_2/\text{poly-Si}$ interface and thus reduce the interface states and trap states in poly-Si, further increase the ON current and field effect mobility and decrease the OFF current and subthreshold-swing. For the reliability issue, less degradation have been found in the LTPS TFTs with CF_4 plasma treatment after hot-carrier stress or self-heating stress. That is due to the stronger Si-F bonds instead of weaker Si-H and Si-Si bonds.



Finally, the mechanism of hot-carrier induced device degradation has been proposed by applying a various static stress conditions. We found that the on and off current variation are strongly influenced by the applied static stress conditions and drain voltage. This is due to different amount of charges trapping in gate insulator or trap states generation in poly-Si channel caused by different stress conditions.

誌謝

論文的完成，首先要向我的指導教授雷添福博士至上最高的敬意。感謝雷添福博士在我這二年的碩士生涯中給予學業研究的鼓勵與支持，並且在我報告實驗進度與想法時，提供了很多寶貴的意見，使我獲益匪淺。

再者，我要特別地感謝王獻德學長，學長在觀念上、實驗操作上、量測分析上及論文寫作上都很熱心地幫助我，令我受益良多。另外還有實驗室的李名鎮學長、表哥學長、李介文學長、柏儀學長、哲麒學長、李宗霖學長、謝明山學長、小強學長、建豪學長、楊紹明學長、小賢學長、小野柳學長與美錡學姊，感謝你們這段日子以來的關心與指導。此外，感謝這陣子來一起同甘共苦的松齡、久盟、國誠、余俊，我永遠不會忘記因為計測實驗熬夜量 Charge Pumping 所以連續一個禮拜都看到日出的那段日子。也要感謝實驗室的學弟們任逸、志仰與家文，尤其在我做完實驗很累的時候，桑學弟的冷笑話往往都會讓我精神為之一振。感謝半導體中心的徐秀鑾小姐與黃月美小姐在這陣子以來的關心與實驗上的協助，也感謝彭兆光先生對實驗機台的維護與整修。

最後，我要向我的父母羅瑞焜先生與程秀蘭小姐表達我最深的感謝，感謝他們無怨無悔的犧牲奉獻及在我低潮時扶持我繼續向前，沒有你們的支持與鼓勵，就不會有現在的我，僅以此論文獻給你們。

Contents

Abstract (Chinese)	I
Abstract (English)	III
Acknowledge	V
Contents	VI
Table & Figure Captions	IX
Chapter 1 Introduction	1
1.1 Overview of Poly-Si Thin-Film Transistors.....	1
1.2 Passivation the Trap States.....	2
1.3 Motivation.....	4
1.5 Organization of the Thesis.....	4
1.5 References.....	6
Chapter 2 Characteristics of Low Temperature Poly-Si TFTs with CF₄ Plasma Treatment	9
2.1 Introduction.....	9
2.2 Experiment	10
2.2.1 Process Flow of SPC Poly-Si TFTs with CF ₄ Plasma Treatment.....	10
2.2.2 Process Flow of ELA Poly-Si TFTs with CF ₄ Plasma Treatment.....	11
2.3 Method of Device Parameter Extraction.....	12
2.3.1 Determination of Threshold Voltage.....	12
2.3.2 Determination of Subthreshold-Swing	13
2.3.3 Determination of Field Effect Mobility	14
2.3.4 Determination of ON/OFF Current Ratio	15
2.3.5 Extraction of Grain Boundary Trap State Density	15
2.4 The characteristics of Low Temperature Poly-Si TFTs with CF ₄ Plasma Treatment.....	17

2.4.1 Characteristics of SPC Poly-Si TFTs with CF ₄ Plasma Treatment.....	17
2.4.2 Characteristics of ELA Poly-Si TFTs with CF ₄ Plasma Treatment.....	19
2.5 Summary.....	21
2.6 References.....	22

Chapter 3 Reliability Improvements of Low Temperature Poly-Si TFTs with CF₄ Plasma Treatment46

3.1 Introduction.....	46
3.2 Experiment details.....	47
3.3 Results and Discussion.....	47
3.3.1 Characteristics of poly-Si TFTs after hot-carrier stress.....	48
3.3.2 Characteristics of poly-Si TFTs after self-heating stress.....	49
3.3.3 Device degradation mechanisms and fluorine passivation effect.....	50
3.4 Summary.....	51
3.5 References.....	52

Chapter 4 Analysis of Hot-Carrier Induced Degradation in Hydrogenated Low Temperature Poly-Si TFTs69

4.1 Introduction.....	69
4.2 Experiment details.....	70
4.3 Results and Discussion.....	70
4.3.1 Stress gate voltage dependence of TFTs degradation.....	70
4.3.2 ON/OFF current variation at various drain voltage after hot-carrier stress.....	71
4.4 Summary.....	73

4.5 References.....74

Chapter 5 Conclusions.....82



TABLE CAPTIONS

Table 2-1 Summary of device parameters of SPC poly-Si TFTs (W/L = 40 μ m/10 μ m) with and without CF₄ plasma treatment.

Table 2-2 Summary of device parameters of hydrogenated SPC poly-Si TFTs (W/L = 40 μ m/10 μ m) with and without CF₄ plasma treatment.

Table 2-3 Summary of device parameters of hydrogenated ELA poly-Si TFTs (W/L = 40 μ m/10 μ m, laser energy density = 420mJ/cm²) with and without CF₄ plasma treatment.

Table 2-4 Summary of device parameters of hydrogenated ELA poly-Si TFTs (W/L = 40 μ m/10 μ m, laser energy density = 460mJ/cm²) with and without CF₄ plasma treatment.



FIGURE CAPTIONS

Chapter 2

Fig. 2-1 Process flow of the poly-Si TFTs with CF₄ plasma treatment.

Fig. 2-2 Transfer characteristics of the SPC poly-Si TFTs with and without CF₄ plasma treatment.

Fig. 2-3 Field effect mobility of the SPC poly-Si TFTs with and without CF₄ plasma treatment.

Fig. 2-4 Output characteristics of the SPC poly-Si TFTs with and without CF₄ plasma treatment.

Fig. 2-5 Trap state density extraction of the SPC poly-Si TFTs with and without CF₄ plasma treatment.

Fig. 2-6 SIMS profiles of the SPC poly-Si TFTs with and without CF₄ plasma treatment.

Fig. 2-7 Activation energy of the SPC poly-Si TFTs with and without CF₄ plasma treatment.

Fig. 2-8 Transfer characteristics of the SPC poly-Si TFTs after NH₃ hydrogenation with and without CF₄ plasma treatment.

Fig. 2-9 Field effect mobility of the SPC poly-Si TFTs after NH₃ hydrogenation with and without CF₄ plasma treatment.

Fig. 2-10 Output characteristics of the SPC poly-Si TFTs after NH₃ hydrogenation with and without CF₄ plasma treatment.

Fig. 2-11 Trap state density extraction of the SPC poly-Si TFTs after NH₃ hydrogenation with and without CF₄ plasma treatment.

Fig. 2-12 Transfer characteristics of the ELA poly-Si TFTs at the laser energy density equals to 420mJ/cm² with and without CF₄ plasma treatment.

Fig. 2-13 Field effect mobility of the ELA poly-Si TFTs at the laser energy density equals to $420\text{mJ}/\text{cm}^2$ with and without CF_4 plasma treatment.

Fig. 2-14 Output characteristics of the ELA poly-Si TFTs at the laser energy density equals to $420\text{mJ}/\text{cm}^2$ with and without CF_4 plasma treatment.

Fig. 2-15 Trap state density extraction of the ELA poly-Si TFTs at the laser energy density equals to $420\text{mJ}/\text{cm}^2$ with and without CF_4 plasma treatment.

Fig. 2-16 Transfer characteristics of the ELA poly-Si TFTs at the laser energy density equals to $460\text{mJ}/\text{cm}^2$ with and without CF_4 plasma treatment.

Fig. 2-17 Field effect mobility of the ELA poly-Si TFTs at the laser energy density equals to $460\text{mJ}/\text{cm}^2$ with and without CF_4 plasma treatment.

Fig. 2-18 Output characteristics of the ELA poly-Si TFTs at the laser energy density equals to $460\text{mJ}/\text{cm}^2$ with and without CF_4 plasma treatment.

Fig. 2-19 Trap state density extraction of the ELA poly-Si TFTs at the laser energy density equals to $460\text{mJ}/\text{cm}^2$ with and without CF_4 plasma treatment.

Fig. 2-20 SIMS profiles of the ELA poly-Si TFTs with and without CF_4 plasma treatment.

Chapter 3

Fig.3-1 Applying bias of the two electrical stress including (a) hot-carrier stress and (b) self-heating stress.

Fig.3-2 Transfer characteristics of the TFTs without CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress.

Fig.3-3 Transfer characteristics of the TFTs with CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress.

Fig. 3-4 Output characteristics of the TFTs without CF_4 plasma treatment before and after 50sec and 1000sec hot-carrier stress.

Fig.3-5 Output characteristics of the TFTs with CF₄ plasma treatment before and after 50sec and 1000sec hot-carrier stress.

Fig. 3-6 Enlarged plot of the output characteristics of the TFTs without CF₄ plasma treatment before and after 50sec and 1000sec hot-carrier stress.

Fig.3-7 Enlarged plot of the output characteristics of the TFTs with CF₄ plasma treatment before and after 50sec and 1000sec hot-carrier stress.

Fig.3-8 (a) mobility and (b) On current degradation with time under self-heating stress.

Fig.3-9 Subthreshold-swing degradation with time under hot-carrier stress.

Fig.3-10 Transfer characteristics of the TFTs without CF₄ plasma treatment before and after 50sec and 1000sec self-heating stress.

Fig.3-11 Transfer characteristics of the TFTs with CF₄ plasma treatment before and after 50sec and 1000sec self-heating stress.

Fig. 3-12 Output characteristics of the TFTs without CF₄ plasma treatment before and after 50sec and 1000sec self-heating stress.

Fig. 3-13 Output characteristics of the TFTs with CF₄ plasma treatment before and after 50sec and 1000sec self-heating stress.

Fig.3-14 (a) mobility and (b) on current degradation with time under self-heating stress.

Fig.3-15 Mobility degradation rate fitted by power-time dependent law under (a) hot-carrier and (b) self-heating stress.

Fig. 3-16 Atomic model of the SiO₂/poly-Si interface (a) without CF₄ plasma, and (b) with CF₄ plasma.

Chapter 4

Fig.4-1 Schematic diagram of poly-Si TFT device structure and the applying stress conditions.

Fig.4-2 Stress gate voltage dependence of TFTs on-current degradation.

Fig.4-3 Stress gate voltage dependence of TFTs off-current degradation.

Fig.4-4 Off-current differences versus drain voltage at three types of stress condition,

$$\text{where ? } I_{\text{off}} = I_{\text{off, stress}} - I_{\text{off, initial}}.$$

Fig.4-5 On-current differences versus drain voltage at three types of stress condition,

$$\text{where ? } I_{\text{on}} = I_{\text{on, stress}} - I_{\text{on, initial}}.$$

Fig.4-6 The drain voltage related barrier variation of the negative trap states.

Fig.4-7 Schematic diagram of device cross section of the type-A stress ($V_{G, \text{ stress}} = 0V$,

$$V_{D, \text{ stress}} = 20V).$$

Fig.4-8 Schematic diagram of device cross section of the type-B stress ($V_{G, \text{ stress}} = 10V$,

$$V_{D, \text{ stress}} = 20V).$$

Fig.4-9 Schematic diagram of device cross section of the type-C stress ($V_{G, \text{ stress}} = 20V$,

$$V_{D, \text{ stress}} = 20V).$$

