Chapter 1

Introduction

1.1 Overview of Poly-Si Thin-Film Transistors

The first polycrystalline silicon thin film transistors (Poly-Si TFTs) were fabricated in 1966 by C. H. Fa *et al.* [1]. To date, lots of efforts have been put to study the conduction mechanisms, fabrication processes and device structure for improving the performance of the poly-Si TFTs. However, the study of poly-Si TFTs fabrication using a temperature below 600°C was not commenced until 1980s. Originally, the idea of this investigation was tried to replace the quartz substrates with cheap glass substrates for applications of active matrix display and made large area active matrix displays more practical and cheaper.

Recently, low temperature polycrystalline silicon (LTPS) TFTs have attracted much attention in active matrix liquid crystal displays (AMLCDs) with integrated drivers [2-4], high density static random access memories (SRAMs) [5] and candidate for 3-D ICs' applications [6], etc. In the past, hydrogenated amorphous silicon (a-Si:H) TFTs were utilized for the pixel switching device at the first generation of AMLCDs. The a-Si:H TFTs have many advantages, especially its compatibility with low temperature process on large glass substrate and high off-state resistivity which result in a low leakage current. Nevertheless, the low electron field effect mobility (typically below 1 $cm^2V^{-1}sec^{-1}$) in a-Si:H TFTs has limited the technology development for AMLCDs applications.

Essentially, the field effect mobility in poly-Si is much higher than those in a-Si,

thus lead to a higher driving current. The higher driving current allows smaller TFTs to be used as the pixel switching elements, thus results in higher aperture ratio and panel brightness. In addition, the capability to realize complementary metal-oxide-semiconductor (CMOS) circuits allows low power driver circuitry to be integrated with the active matrix, for the goal of SOP (system on panel).

The performance of poly-Si TFTs is strongly influenced by grain boundaries and intragranular defects. In order to enhance TFTs electrical characteristics, several techniques have been proposed to increase the grain sizes of poly-Si and thus to reduce grain boundaries. Therefore, the methods for crystallization of a-Si into poly-Si below 600℃ (glass-compatible temperature) are the key technology for fabricating LTPS TFTs. It was reported that the a-Si films can be crystallized by several techniques, such as SPC (solid-phase crystallization) [7], ELA (excimer laser annealing) [8-9] and MILC (metal-induced lateral crystallization) [10] to obtain larger grain sizes of poly-Si for raising the field effect mobility.

On the other hand, to eliminate the grain boundaries and intragranular defects in the poly-Si channel is another approach to improve the performance of LTPS TFTs [11]. The dangling bonds, which cause midgap states in the Si band diagram, affect the threshold voltage and subthreshold-swing of Poly-Si TFTs. The strain bonds, which cause tail states, influence the leakage current and field effect mobility. In order to eliminate these trap states in the poly-Si channel, various passivation technologies have been proposed.

1.2 Passivation the Trap States

Defects at the grain boundaries as well as inside the grains are known to cause device degradation [12], resulting in poor device performance including low field

effect mobility, high threshold voltage, poor subthreshold slope and high off-state leakage current [13-14]. In order to obtain high-performance poly-Si TFTs, it is essential to reduce the trap-state density in the poly-Si channel. To this end, hydrogen plasma passivation is a well-known technique [15-16]. The atomic hydrogen can passivate defects in the poly-Si channel, thereby improves the device characteristics. In addition, nitrogen-containing plasma treatments in combination with hydrogen (ex: H_2/N_2 mixture plasma [17], nitrogen implantation with H_2 plasma [18], pre-oxidation NH_3 annealing with H_2 plasma [19] and NH_3 plasma [20]) have also been shown to further improve the device performance. The additional nitrogen passivation and/or the enhanced hydrogen passivation effects in the presence of nitrogen are presumably responsible for the observed great device's characteristics improvement.

However, many studies have discussed the performance degradation of hydrogenated poly-Si TFTs after all kinds of electrical stress. Wu *et al.* This is attributed to the state creation in the poly-Si channel caused by the breaking of weak Si-H bonds or Si-Si bonds, while the degradation rate increased with stressing bias voltage [21]. Recently, several studies have demonstrated that the using of Fluorine (F) atoms to fluorinate the poly-Si film, which can improve the reliability issues of poly-Si TFTs due to rather strong Si-F bonds.

Fluorine Ion Implantation (FII) into the channel region, the most adoptive fluorination technique, has been widely investigated in several groups [22-23]. However, the FII is not suitable for large area glass substrate application. Furthermore, in order to activate the fluorine atoms and recover the damage created by FII, a high temperature annealing is required and such a high temperature process will not compatible with the AMLCD fabrication process. Moreover, C. H. Kim *et al.* demonstrated that fluorinated oxide (SiO_xF_y) can be served as a diffusion source of fluorine atoms [24], but that increase the process complexity since an extra film

deposition and etching process are required. To date, although the effects of the fluorination process have been announced, we still lack a simple, effective and process compatible method to introduce fluorine atoms into poly-Si channel.

1.3 Motivation

In order to further improve the shortcomings of the hydrogenated poly-Si TFTs, we propose a novel fluorine passivation technique of poly-Si films by employing CF_4 plasma treatment. With fluorine incorporation into the poly-Si channel, the electrical characteristics of the poly-Si TFTs can be improved. Poly-Si TFTs with CF_4 plasma exhibit a steeper subthreshold slope, smaller threshold voltage, higher field effect mobility and better ON/OFF current ratio than those without CF_4 plasma treatment. Moreover, the CF_4 plasma treatment also raises the stress immunity of the poly-Si TFTs with respect to the hot-carrier stress and high current stress. Owing to the formation of strong Si-F bonds instead of weak Si-H bonds or Si-Si bonds, the probability of dangling bonds will be reduced greatly. In other words, fluorine passivation of trap-states in the poly-Si channel and SiO_2/poly-Si interface is realized effectively using CF_4 plasma treatment.

1.4 Organization of the Thesis

In this thesis, we make our efforts on the passivation effect of poly-Si TFTs by utilizing a novel CF_4 plasma treatment.

In Chapter 2, electrical properties of both SPC and ELA poly-Si TFTs with CF_4 plasma treatment have been proposed.

In Chapter 3, reliability improvements of poly-Si TFTs with CF_4 plasma treatment are introduced by employing the hot-carrier stress and self-heating stress.

In Chapter 4, mechanisms of the hot-carrier induced device degradation were

investigated after applying a various static stress conditions.

At the end of this thesis, conclusions are given in Chapter 5.

1.5 References

[1] C. H. Fa, and T. T. Jew, "The polysilicon insulated-gate field-effect transistor," *IEEE Trans. Electron Devices*, vol. 13, no. 2, p. 290, 1966.

[2] Yasuhisa Oana, "Current and future technology of low-temperature poly-Si TFT-LCDs," *Journal of the SID*, vol. 9, p. 169-172, 2001.

[3] S. Morozumi, K. Oguchi, S. Yazawa, Y. Kodaira, H. Ohshima, and T. Mano, "B/W and color LC video display addressed by poly-Si TFTs," *SID Dig*., p.156, 1983.

[4] R. E. Proano, R. S. Misage, D. Jones, and D. G. Ast, "Guest-Host Active Matrix Liquid-Crystal Display using High-Voltage Polysilicon Thin Film Transistors," *IEEE Trans. Electron Devices*, vol. 38, p. 1781, 1991.

[5] S. Batra, "Development of Drain-Offset (DO) TFT Technology for High Density SRAM's," Extended Abstracts, vol.94-2, in *Electrochemical Soc. Fall Mtg., Miami Beach, FL*, Oct. p. 677,1994.

[6] Kaustav Banerjee, Shukri J. Souri, Pawan Kapur, and Krishna C. Saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and system-on-chip integration," *Proceedings of the IEEE*, vol.89, p. 602-633, 2001.

[7] A. Nakamura, F. Emoto, E. Fujii, and A. Tamamoto, "A High-Reliability, Low-Operation-Voltage Monolithic Active-Matrix LCD by Using Advanced Solid-Phase growth Technique," *IEDM Tech*. p.847, 1990.

[8] G. K. Guist, and T. W. Sigmon, "High-Performance Laser-Processed Polysilicon Thin-Film Transistors," *IEEE Electron Device Lett*., vol. 20, no. 2, p. 77-79, Feb. 1999.

[9] N. Kudo, N. Kusumoto, T. Inushima, and S. Yamazaki, "Characterization of

polycrystalline-Si thin-film transistors fabricated by excimer laser annealing method," *IEEE Trans. Electron Devices*, vol. 40, p. 1876-1879, Oct. 1994.

[10] Seok-Woon Lee, Tae-Hyung Ihn, and Seung-Ki Joo, "Fabrication of High-Mobility P-Channel Poly-Si Thin-Film Transistors by Self-Aligned Metal-Induced Lateral Crystallization," *IEEE Electron Device Lett.*, vol. 17, no. 8, Aug. 1996.

[11] T. Yoshida, K. Yoshino, M. Takei, A. Hara, N. Sasaki, and T. Tsuchiya, "Experimental evidence of grain-boundary related hot-carrier degradation mechanism in low-temperature poly-Si thin-film-transistors," *IEDM Tech.* p. 8.8.1-8.8.4, Dec. 2003

[12] I. W. Wu, W. B. Jackson, T. Y. Huang, A. G. Lewis, and A. Ciang, "Passivation kinetics of two types of defeats in polysilicon TFT by plasma hydrogenation," *IEEE Electron Devices lett.*, vol. 12, pp. 181-183, 1991.

[13] J. G. Fossum, A. Ortiz-Conde, H. Shicjijo, abd S. K. Banerjee, "Anomalous Leakage Current in LPCVD Polysilicon MOSFET's," *IEEE Trans. Electron Devices*, vol. 32, p. 1878-1882, 1985.

[14] W. G. Hawkins, "Polycrystalline-silicon device technology for large-area electronics," *IEEE Trans. Electron Devices*, vol. 33, p. 477-481, 1986.

[15] K. Baert, H. Murai, K. Kobayashi, H. Namizaki, and M. Nunoshita, "Hydragen passivation of polysilicon thin-film-transistors by electron-cyclotron-resonance plasma," *Jpn. J. Appl. Phys.*, vol. 32, p. 2601-2606, 1993

[16] Aiguo Yin, and Stephen J. Fonash, "High-performance p-channel poly-Si TFT's using electron cyclotron resonance hydrogen plasma passivation," *IEEE Electron Devices lett.*, vol. 15, no. 12, pp. 502-503, 1994.

[17] M. J. Tasi, F. S. Wang, K. L. Cheng, S. Y. Wang, M. S. Feng, and H. C. Chen, "Characterization of H_2/N_2 plasma passivation process for poly-Si thin-film

transistors (TFTs)," *Solid State Electronics,* vol. 38, no. 5, pp.1233-1238, 1995

[18] C. K. Yang, T. F. Lei, C. L. Lee, "Improved electrical characteristics of thin-film transistors fabricated on nitrogen-implanted Polysilicon films," *IEDM Tech Dig.*, pp505, 1994.

[19] C. K. Yang, T. F. Lei, C. L. Lee, "The combined effects of low pressure NH3 annealing and H_2 plasma hydrogenation on polysilicon thin-film-transistors," *IEEE Electron Devices lett.*, vol. 15, pp. 389-390, 1994.

[20] H. C. Cheng, F. S. Wang, and C. Y. Huang, "Effects of NH_3 plasma passivation on n-channel Polycrystalline silicon thin-film-transistors," *IEEE Trans. Electron Devices*, vol. 44, no. 1, p. 64-68, 1997.

[21] I-Wei Wu, Warren. B. Jackson, Tiao-Yuan Huang, Alan G. Lewis, and Anne Chiang, "Mechanism of device degradation in n- and p-channel polysilicon TFT's by electrical stressing," *IEEE Electron Devices lett.*, vol. 11, pp. 167-170, 1990.

[22] S. Maegawa, T. Ipposhi, S. Maeda, H. Nishimura, T. Ichiki, M. Ashida, O. Tanina, Y. Inoue, T. Nishimura and N. Tsubouchi, "Performance and reliability improvement in poly-Si TFT's by fluorine implantation into gate poly-Si," *IEEE Trans. Electron Devices*, vol. 42, pp. 1106-1111, Apr. 1995.

[23] H. N. Chern, C. L. Lee, and T. F. Lei, "The effects of fluorine passivation on poly-Si thin film transistors," *IEEE Trans. Electron Devices*, vol. 41, pp. 698-702, May 1994.

[24] C. H. Kim, S. H. Jung, J. S. Yoo, and M. K. Han, "Poly-Si TFT Fabricated by Laser-Induced In-Situ Fluorine Passivation and Laser Doping," *IEEE Electron Devices lett.*, vol. 22, pp. 396-398, Jun. 2001.