Chapter 2

The Characteristics of Low Temperature Poly-Si TFTs with CF_4 Plasma Treatment

2.1 Introduction

Poly-Si TFTs have attracted much attention due to the possibility to realize the integration of switching-pixels and their peripheral driver circuits on a single glass substrate of AMLCD [1]. Poly-Si TFTs have many advantages over a-Si:H TFTs, including higher driving current and greater field effect mobility. However, a large amount of trap-states in poly-Si channel affects the field effect mobility and cause serious degradation of devices performance [2-3].

To get the desirable characteristics of poly-Si TFTs, one method utilized is the passivation of the trap-states of the poly-Si channel [4-6]. Recently, several studies have demonstrated that the using of Fluorine (F) atoms to fluorinate the poly-Si film, which can improve the performance of poly-Si TFTs especially for the reliability issue of the devices [7-12]. This is attributed to the incorporation of fluorine atoms that can terminate the dangling bonds within the grain boundary and SiO_2/poly-Si interface and thus reduce the trap-state density in the poly-Si channel region. Moreover, the strong Si-F bonds are more stable than Si-H and Si-O bonds and can maintain a device performance under long term electrical stress.

Fluorine Ion Implantation (FII) into the channel region, the most adoptive fluorination technique, has been widely investigated in several groups [7-10]. However, the FII method is not suitable for large area glass substrate application.

Furthermore, in order to activate the fluorine atoms and recover the damage created by FII, a high temperature annealing is required and such a high temperature process will not compatible with the AMLCD fabrication process.

Moreover, C. H. Kim *et al*. demonstrated that fluorinated oxide (SiO_xF_y) can be served as a diffusion source of fluorine atoms [11-12] but that increase the process complexity since an extra film deposition and etching process are required. To date, although the effects of the fluorination process have been clarified, we still lack a simple, effective and process-compatible method to introduce fluorine atoms into poly-Si channel.

In this thesis, we proposed a novel technique to introduce fluorine atoms into poly-Si channel by using CF_4 plasma with a low RF power. It is well known that CF_4 plasma is widely used in the Reactive Ion Etching (RIE) system. Fluorine atoms can be dissociated by applied power from RF generator. To avoid the unwanted etching effect, we tried to generate fluorine atoms with very low RF power (5W ~ 10W) and short treatment time (＜1min.). We used these fluorine atoms to fluorinate the poly-Si channel. The fluorinated poly-Si TFTs have been fabricated and their device characteristics and reliability improvement have been investigated.

2.2 Experiment

2.2.1 Process Flow of SPC Poly-Si TFTs with CF_4 Plasma Treatment

The proposed SPC poly-Si TFTs were fabricated on 4-inch diameter N-type silicon wafer. Fig. 2-1 shows the process flow of the SPC Poly-Si TFTs. First, the (100) N-type silicon wafers were thermally oxidized for 500nm by furnace system to form the glass substrate. A 100nm a-Si layer was then deposited by LPCVD with silane (SiH_4) gas source at 550℃. The deposition pressure was 100mTorr and the

SiH_4 flow rate was 40sccm. After 24hrs furnace anneal at 600°C in N_2 ambient, the a-Si layer was recrystallized into poly-Si.

After definition of device active area, CF_4 plasma was carried out with CF_4 gas source using PECVD system at 350°C with RF power of 5W. The chamber pressure and CF_4 flow rate was 200mTorr and 20sccm, respectively. The CF_4 plasma treatment time was 15sec.

Then, 50nm thick tetraethyl orthosilicate (TEOS) oxide was deposited with TEOS and O_2 gas source by PECVD at 350°C for gate insulator and 200nm thick poly-Si was deposited by LPCVD for gate electrode. Gate area was patterned and the regions of source, drain and gate were doped by a self-aligned 5×15 ions/cm^2 phosphorus ion implantation at acceleration voltage of 40KeV. The dopant was activated in N_2 ambient for 24hrs at 600°C. Next, 400nm thick passivation oxide was deposited by PECVD at 350°C, and contact holes were patterned. After opening contact holes, 500nm thick Al was deposited by thermal evaporation and Al layer was then patterned for metal pad. Finally, some of the TFT's were hydrogenated by NH_3 plasma with 200W RF power for 3hrs.

2.2.2 Process Flow of ELA Poly-Si TFTs with a Novel CF_4 Plasma Treatment

Fig. 2-1 also shows the process flow of the ELA poly-Si TFTs. Except the crystallization method of a-Si films, most of the fabrication steps were the same with SPC poly-Si TFTs mentioned before. A semi-gaussiam shaped KrF excimer laser with wavelength of 248nm was used to re-crystallize the a-Si films at the laser energy density of 420 and 460mJ/cm^2 with substrate heating of 400°C under the chamber pressure of 10^{-3} Torr.

After the definition of device active area, CF_4 plasma was carried out with CF_4 gas source by PECVD system at 350℃ and RF power of 10W. The chamber pressure and CF_4 flow rate was 200mTorr and 20sccm, respectively. CF_4 plasma treatment time was 15sec.

Then, 100nm TEOS oxide was deposited with TEOS and O_2 gas source by PECVD at 350℃ for gate insulator and 200nm thick poly-Si layer was deposited by LPCVD for gate electrode. Gate area was patterned and the regions of source, drain and gate were doped by a self-aligned 5×15 ions/cm^2 phosphorus ion implantation at acceleration voltage of 40KeV. The dopant was activated by excimer laser annealing with laser energy density of 220mJ/cm^2.

After dopant activation, NH_3 hydrogenation with RF power of 200W was carried out by PECVD. Next, 400nm thick passivation oxide was deposited by PECVD at 350℃, and contact holes were patterned. After opening contact holes, 500nm thick Al was deposited by thermal evaporation and Al layer was then patterned for metal pads.

2.3 Method of Device Parameter Extraction

In this thesis, we use Ellipsometer to measure the thickness of poly-Si, a-Si and TEOS oxide films. All the electrical characteristics of proposed poly-Si TFTs were measured by HP 4156B-Precision Semiconductor Parameter Analyzer.

Many methods have been proposed to extract the characteristic parameters of poly-Si TFTs. In this section, the methods of parameter extraction used in this thesis are described.

2.3.1 Determination of Threshold Voltage

The threshold voltage (V_{th}) is an important parameter required for the channel

length-width and series resistance measurements. However, V_{th} is not uniquely defined. One of the most common threshold voltage measurement techniques is the *linear extrapolation method* with the drain current measured as a function of gate voltage at a low drain voltage of 50~100mV typically to ensure operation in the linear region [13]. The drain current is not zero and approaches zero asymptotically. Hence the I_{DS} versus V_{GS} curve can be extrapolated to $I_D = 0$, and the threshold voltage is determined from the extrapolated intercept of gate voltage (V_{GSi}) by

$$V_{th} = V_{GSi} - \frac{V_{DS}}{2} \quad \text{---------- (Eq. 2.1)}$$

Equation (2.1) is strictly only valid for negligible series resistance. Fortunately series resistance is usually negligible at the low drain current. The I_{DS}-V_{GS} curve deviates from a straight line at gate voltage below V_{th} due to subthreshold current and above V_{th} due to series resistance and mobility degradation effects. It is common practice to find the point of maximum slope of the I_{DS}-V_{GS} curve and fit a straight line to extrapolate to $I_D = 0$ by means of finding the point of maximum of transconductance (g_m).

In this thesis, we use a simpler method called *constant drain current method* to determinate the threshold voltage. That means the voltage at a specified threshold drain current is taken as the threshold voltage. This method is adopted in the most studied papers of poly-Si TFTs. It can be given a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current is specified at (W/L)× 10nA for $V_{DS} = 0.1V$ and (W/L)×100nA for $V_{DS} = 5V$, where W and L are channel width and channel length, respectively.

2.3.2 Determination of Subthreshold-Swing

Subthreshold swing (S.S (V/dec) is a typical parameter to describe the control

ability of gate toward channel. That is the turn on/off speed of a device. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude.

The subthreshold swing should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to short channel effect such as charge sharing, avalanche multiplication and punchthrough effect. The subthreshold swing is also related to gate voltage due to undesirable and inevitable factors such as the serial resistance and interface states.

In this thesis, the subthreshold swing is defined as one-third of the gate voltage required to decrease the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

2.3.3 Determination of Field Effect Mobility

Usually, field effect mobility (m_{eff}) is extracted from the maximum value of transconductance at low drain bias (V_{DS} = 0.1V). The drain current in linear region (V_{DS} < V_{GS} - Vth) can be approximated as the following equation:

$$I_{DS} = m_{eff} C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^{2} \right] \quad \text{---------- (Eq. 2.2)}$$

where W and L are channel width and channel length, respectively. C_{ox} is the gate oxide capacitance. Thus, g_m is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = m_{eff} C_{ox} \left(\frac{W}{L} \right) V_{DS} \quad \text{---------- (Eq. 2.3)}$$

Therefore,

$$m_{eff} = \frac{L}{C_{ox} W V_D S} g_{m(\max)} \Big|_{V_{DS} \to 0} \quad \text{---------- (Eq.2.4)}$$

2.3.4 Determination of ON/OFF Current Ratio

ON/OFF Current Ratio is one of the most important parameters of poly-Si TFTs since a good performance means not only large ON-current but also small OFF-current (leakage current). The leakage current mechanism in poly-Si TFTs is not like it in MOSFET. In MOSFET, the channel is composed of single crystalline Si and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFTs, the channel is composed of polycrystalline Si. A large amount of traps in grain structure attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current due to the tunneling effect is much larger in poly-Si TFTs than in MOSFET. When the voltage drops between gate voltage and drain voltage increases, the band gap width decreases and the tunneling effect becomes much more severe. Normally we can find this in typical poly-Si TFT I_{DS}-V_{GS} characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decreases/increases for N/P-channel TFTs.

There are a lot of ways to specify the ON and OFF-current. In this thesis, take N-channel poly-Si TFTs for examples, the ON-current and OFF-current is defined as the drain current when gate voltage equals to 20V and drain voltage is 5V. The OFF-current is specified as the minimum current when drain voltage equals to 5V.

$$\frac{I_{ON}}{I_{OFF}} = \frac{Maximum\ \ Current\ \ of\ \ I_{DS}-V_{GS}\ \ Plot\ \ at\ \ V_{DS}=5V}{Minimum\ \ Current\ \ of\ \ I_{DS}-V_{GS}\ \ Plot\ \ at\ \ V_{DS}=5V} \quad \text{---------- (Eq. 2.5)}$$

2.3.5 Extraction of Grain Boundary Trap State Density

The Trap State Density (N_t), which can be determined by the theory established by Levinson *et al.* [14], is based on Seto's theory [15].

For poly-Si TFTs, the drain current I_{DS} can be given as following:

$$I_{DS} = \mu_{FE} C_{ox} \left(\frac{W}{L} \right) V_{DS} V_{GS} \exp\left(\frac{-q^3 N_t^{\,2} L_c}{8 \varepsilon_{Si} k T C_{ox} V_{GS}} \right) \quad \text{---------- (Eq. 2.6)}$$

Where,

q	electron charge
k	Boltzmann's constant
ε_{Si}	dielectric constant of silicon
T	temperature
N_t	trap-state density per unit area
L_c	channel thickness

This expression, first developed by Levinson *et al.* [4], is a standard MOSFET's equation with an activated mobility, which depends on the grain-boundary barrier height as introduced by Step. Levinson *et al.* assumed that the channel thickness was constant and equal to the thickness of the poly-Si film. This simplifying assumption is permissible only for very thin film (less than 10nm). The trap-state density can be obtained by extracting a straight line on the plot of $ln(I_{DS}/V_{GS})$ versus $1/V_{GS}$ at low drain voltage and high gate voltage.

Proano *et al.* [16] thought that a barrier approximation is to calculate the gate induced carrier channel thickness by solving Poisson's equation for an undoped material and to define the channel thickness (L_c) as a thickness in which 80% of the total charges were induced by the gate. Doing so, one obtains

$$L_c = \frac{8 k T t_{ox} \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}}}{q\left(V_{GS} - V_{fb}\right)} \quad \text{---------- (Eq. 2.7)}$$

which varies inversely with $(V_{GS} - V_{fb})$. This predicts, by substituting Eq.2.7 into Eq.2.6, that $ln[I_{DS}/(V_{GS} - V_{fb})]$ varies linearly with $1/(V_{GS} - V_{fb})^2$. We use the gate voltage at which minimum leakage current occurs as the V_{fb}. Effective trap-state density (N_t) can be determined from the square root of the slope.

$$N_t = \frac{C_{ox}}{q}\sqrt{|Slope|} \quad \text{---------- (Eq. 2.8)}$$

2.4 Characteristics of Low Temperature Poly-Si TFTs with CF_4 Plasma Treatment

2.4.1 Characteristics of SPC Poly-Si TFTs with CF_4 Plasma Treatment

Fig. 2-2 shows the transfer characteristics (I_{DS}-V_{GS}) for the SPC poly-Si TFTs with and without the CF_4 plasma treatment. The measurements were performed at two different drain voltages of V_{DS}= 0.1V and 5V. Table 2-1 summarizes the measured and extracted parameters from the devices. The threshold voltage, subthreshold swing, ON-current (V_{GS} = 20V) and the OFF-current (V_{GS} = -10V) were measured at V_{DS} = 5 V.

The characteristics of the poly-Si TFTs with the CF_4 plasma treatment were significantly improved. The threshold voltage and subthreshold swing of the CF_4 plasma treated poly-Si TFTs were found to be 8.2 V and 1.7 V/dec., which are superior to those without CF_4 plasma treatment (11.9 V and 2.03 V/dec., respectively). It is known that the V_{th} and S.S. are influenced strongly by the deep trap states associated with the dangling bonds, which have energy states near the middle of the silicon band gap. Therefore, it is inferred that the dangling bonds in the poly-Si and SiO_2/poly-Si interface can be effectively passivated by using CF_4 plasma treatment. Fig. 2-3 shows the field-effect mobility for the SPC poly-Si TFTs with and without the CF_4 plasma treatment. It was increased from 10.6 to 13.6 cm^2/Vs for the TFTs with CF_4 plasma treatment. The field-effect mobility is significantly affected by the tail states near the band edge, which is caused by a high density of strain bonds in poly-Si and SiO_2/poly-Si interface [6]. This feature implies that the CF_4 plasma

treatment can not only passivate the dangling bonds, but also relax the strain bonds in the poly-Si and SiO_2/poly-Si interface. Fig. 2-4 shows the output characteristics (I_{DS}-V_{DS}) of poly-Si TFTs fabricated with and without CF_4 plasma treatment. As can be seen, the driving current increased dramatically for the poly-Si TFTs with the CF_4 plasma treatment. This is due to a high mobility and small threshold voltage of the poly-Si TFTs with the CF_4 plasma treatment. The driving current increased 130.18%, 84.52% and 55.14% at V_{DS}=20V with V_{GS}=10V, 17.5V and 25V, respectively. Fig. 2-5 shows the trap state density of the SPC poly-Si TFTs. For the TFTs with and without CF_4 plasma treatment, the N_t was found to be 1.32×10^{13} cm^{-2} and 1.67×10^{13} cm^{-2}, respectively, which implies that the CF_4 plasma treatment can effectively passivate the trap states in poly-Si channel region. The ON-current, OFF-current and ON/OFF current ratio of the CF_4 plasma treated TFTs were also superior to those without CF_4 plasma treatment.

Fig. 2-6 shows the SIMS (Secondary Ion Mass Spectroscopy) profiles of the poly-Si films before and after CF_4 plasma treatment. The SIMS profiles exhibit that a lot of fluorine atoms, but few carbon atoms were detected in the poly-Si layer with CF_4 plasma treatment. That is to say, fluorine atoms were introduced and confined into the poly-Si layer by using CF_4 plasma treatment not carbon atoms. The SIMS analysis also shows a high concentration of fluorine piling up near the SiO_2/poly-Si interface, instead of in the substrate. These fluorine atoms can provide a more effective passivation of the trap states for poly-Si TFTs, because all carriers will transport near the interface region when the device is turned on. This approach is, therefore, superior to the fluorine ion implant method, which causes a high concentration of fluorine implanted into the deep region of poly-Si layer.

Fig. 2-7 shows the activation energy (Ea) versus gate voltage for the TFTs with and without CF_4 plasma treatment. The value of the Ea reflects the carrier transport

barrier of the grain boundary within the poly-Si channel [15]. Compared with the conventional TFTs, the Ea extracted from CF_4 treated TFTs is decreased in ON-region and increased in OFF-region. The decreasing Ea in ON-region implies that the trap states in poly-Si channel are passivated by CF_4 plasma and hence the grain boundary barrier potential is reduced. In OFF-region, the increase of Ea reveals that the leakage current induced by trap assisted tunneling is also suppressed by CF_4 plasma treatment.

Besides, we utilized ammonia (NH_3) plasma passivation method to promote electrical characteristics of poly-Si TFTs. NH_3 plasma passivation can improve the poly-Si TFTs' performance enormously, particularly in the carrier mobility, ON/OFF current ratio and subthreshold swing. Fig. 2-8, 2.9 and 2-10 show the comparison of transfer and output characteristics of poly-Si TFTs with and without CF_4 plasma treatment after NH_3 plasma passivation for three hours. It was found that poly-Si TFTs with CF_4 plasma treatment after NH_3 plasma passivation exhibited superior performances than that without CF_4 plasma treatment. Fig. 2-11 shows the trap state density of poly-Si TFTs with and without CF_4 plasma treatment after NH_3 plasma passivation for three hours. For the TFTs with and without CF_4 plasma treatment, the N_t were found to be 1.16×10^{13} cm^{-2} and 1.27×10^{13} cm^{-2}, respectively. All the TFTs' characteristics parameters after NH_3 plasma were summarized in Table 2-2.

2.4.2 Characteristics of ELA Poly-Si TFTs with CF_4 Plasma Treatment

Fig. 2-12 and 2-13 show the transfer and mobility characteristics for the ELA poly-Si TFTs with and without CF_4 plasma treatment at laser energy density equals to 420mJ/cm^2. The threshold voltage and subthreshold swing of the CF_4 plasma treated ELA poly-Si TFTs were found to be 4.3 V and 1.16 V/dec., which are superior to those without CF_4 plasma treatment (5.8 V and 1.93 V/dec., respectively). The

field-effect mobility was increased from 29.1 to 42.7 cm^2/Vs for the TFTs with CF_4 plasma treatment. Fig. 2-14 shows the output characteristics of ELA poly-Si TFTs fabricated with and without CF_4 plasma treatment. As can be seen, the driving current increased dramatically for the poly-Si TFTs with the CF_4 plasma treatment. This is due to a high mobility and small threshold voltage of the poly-Si TFTs with the CF_4 plasma treatment. The driving current increased 505%, 183% and 98% at V_{DS}=20V with V_{GS}=10V, 17.5V and 25V, respectively. Fig. 2-15 shows the trap state density plot. For the TFTs with and without CF_4 plasma treatment, the N_t was found to be 3.47×10^{12} cm^{-2} and 4.11×10^{12} cm^{-2}, respectively. Moreover, Fig. 2-16, 2-17, 2.18 and 2-19 show the electrical characteristics of the ELA poly-Si TFTs at the laser energy density equals to 460mJ/cm^2. All the device parameters were summarized in Table 2-3 and 2-4. Fig. 2-20 shows the SIMS profiles of the ELA poly-Si TFTs with and without CF_4 plasma treatment. It can be seen that the fluorine atoms also piled up at the SiO_2/poly-Si interface.

Although preparing with the same CF_4 plasma treatment time, ELA poly-Si TFTs show greater improvements than SPC ones. This might be contributed to the grain boundary densities was smaller in ELA poly-Si films than in SPC ones. Fewer grain boundaries within the poly-Si channel means that there will be more passivation effect in ELA poly-Si channel compared with SPC one with the same CF_4 plasma time.

2.5 Summary

Significant improvements of the electrical performance in poly-Si TFTs have been demonstrated by CF_4 plasma treatment. A steeper subthreshold slope, smaller threshold voltage, higher carrier mobility and better ON/OFF current ratio can be obtained due to the reduction of the trap state density in poly-Si and SiO_2/poly-Si interface. It is concluded that this process-compatible CF_4 plasma treatment is a useful and effective method for the fabrication of high-performance and high-reliability poly-Si TFTs.

2.6 References

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Table 2-1 Summary of device parameters of SPC poly-Si TFTs (W/L = 40 μm/10 μm) with and without CF_4 plasma treatment.

SPC-TFTs w/o Hydrogenation	***w/o CF_4 plasma***	***with CF_4 plasma***
V_{th} (V)	11.9	8.2
S.S.(V/dec.)	2.03	1.7
μ_{eff} (cm^2/V.s)	10.6	13.6
I_{on} @ V_G = 20V (A)	3.52×10^{-5}	9.64×10^{-5}
I_{off} @ V_G = -10V (A)	1.70×10^{-8}	4.27×10^{-9}
ON/OFF Ratio (10^6)	0.91	2.37
N_t (10^{13} cm^{-2})	1.67	1.32

Table 2-2 Summary of device parameters of hydrogenated SPC poly-Si TFTs (W/L = 40 μm/10 μm) with and without CF_4 plasma treatment.

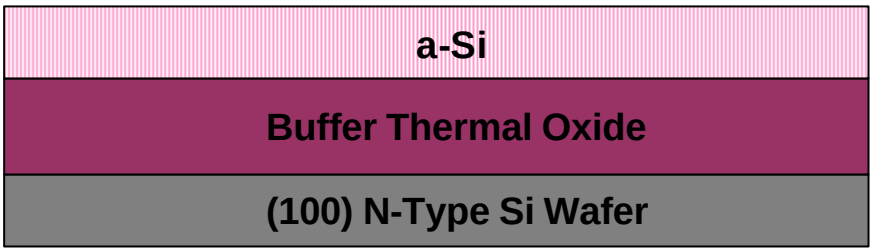
SPC-TFTs with Hydrogenation	***w/o CF_4 plasma***	***with CF_4 plasma***
V_{th} (V)	8.7	7.4
S.S.(V/dec.)	1.68	1.53
μ_{eff} (cm^2/V.s)	17.1	19.2
I_{on} @ V_G = 20V (A)	1.1×10^{-4}	1.59×10^{-4}
I_{off} @ V_G = -10V (A)	5.11×10^{-9}	2.76×10^{-9}
ON/OFF Ratio (10^6)	2.41	3.22
N_t (10^{13} cm^{-2})	1.27	1.16

Table 2-3 Summary of device parameters of hydrogenated ELA poly-Si TFTs (W/L = 40 μm/10 μm, laser energy density = 420mJ/cm^2) with and without CF_4 plasma treatment.

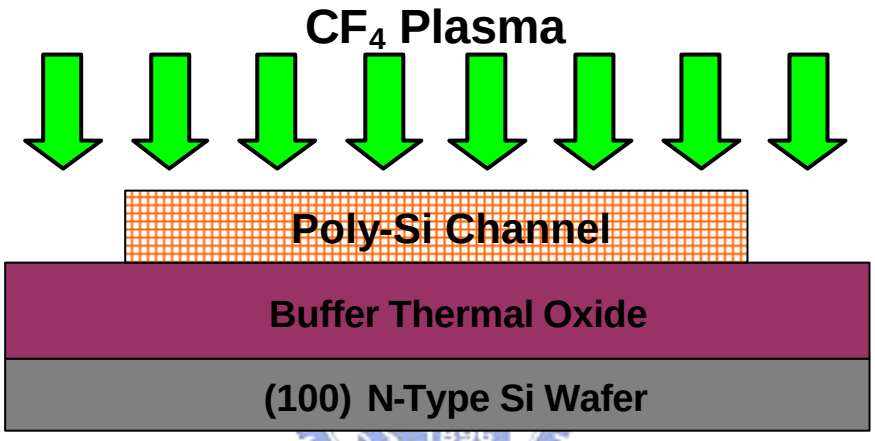
ELA-TFTs 420 mJ/cm^2	***w/o CF_4 plasma***	***with CF_4 plasma***
V_{th} (V)	5.8	4.3
S.S.(V/dec.)	1.93	1.16
μ_{eff} (cm^2/V.s)	29.12	42.74
I_{on} @ V_G = 25V (A)	2.87×10^{-4}	4.61×10^{-4}
I_{off} @ V_G = -10V (A)	1.2×10^{-6}	2.91×10^{-7}
ON/OFF Ratio (10^6)	0.517	3.97
N_t (10^{12} cm^{-2})	4.11	3.47

Table 2-4 Summary of device parameters of hydrogenated ELA poly-Si TFTs (W/L = 40 μm/10 μm, laser energy density = 460mJ/cm^2) with and without CF_4 plasma treatment.

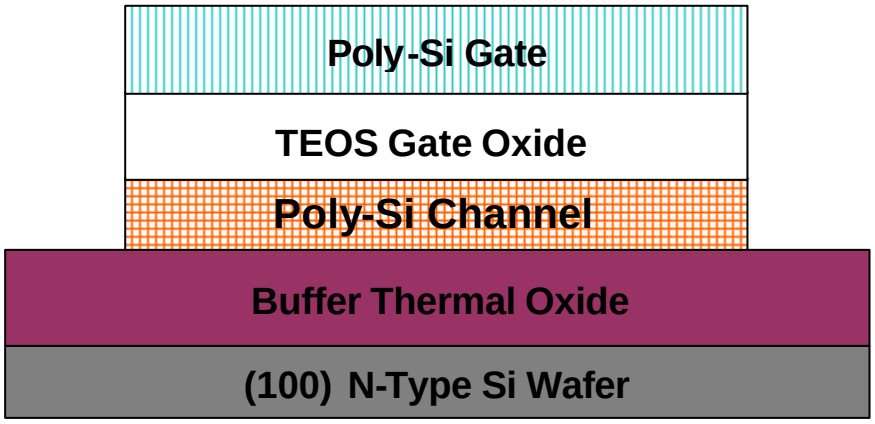
ELA-TFTs 460mJ/cm^2	*w/o CF_4 plasma*	*with CF_4 plasma*
V_{th} (V)	6.1	4.7
S.S.(V/dec.)	1.9	1.3
μ_{eff} (cm^2/V.s)	37.95	50.71
I_{on} @ V_G = 25V (A)	3.47×10^{-4}	5.17×10^{-4}
I_{off} @ V_G = -10V (A)	3.63×10^{-6}	1.25×10^{-6}
ON/OFF Ratio (10^6)	1.35	5.46
N_t (10^{12} cm^{-2})	4.7	3.98



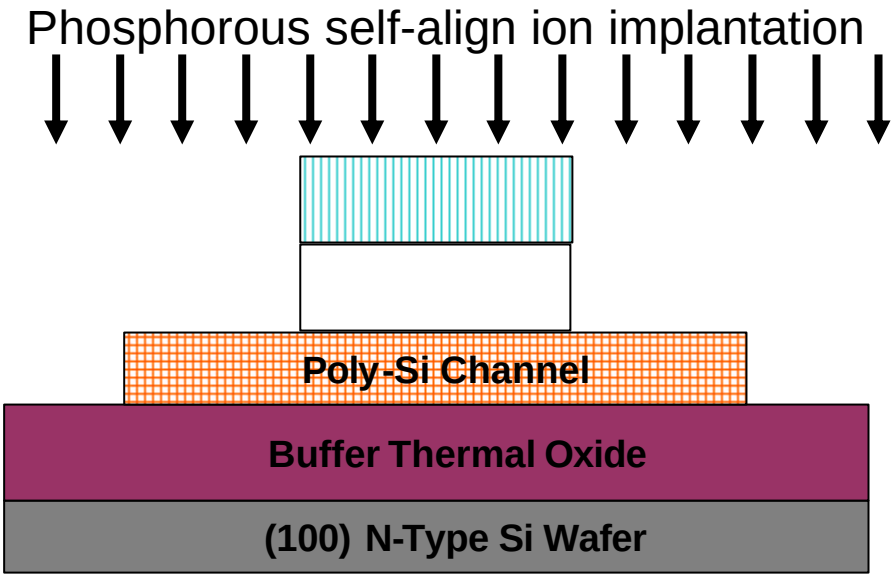
(a) Thermal oxidation and a-Si film deposition by LPCVD.



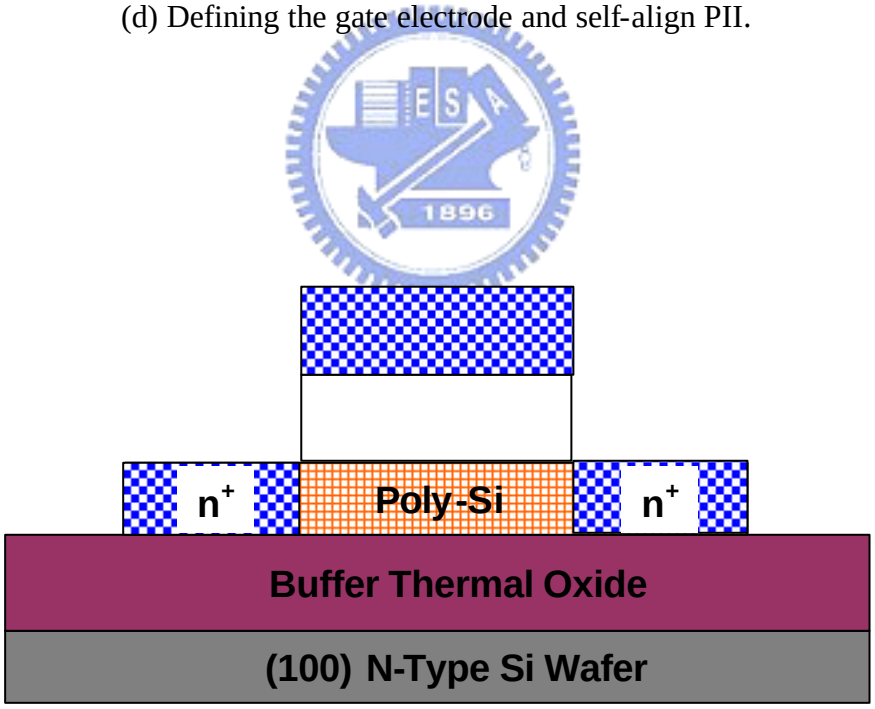
(b) Recrystallization of a-Si film into poly-Si channel by SPC or ELA, defining active region and CF_4 plasma treatment.



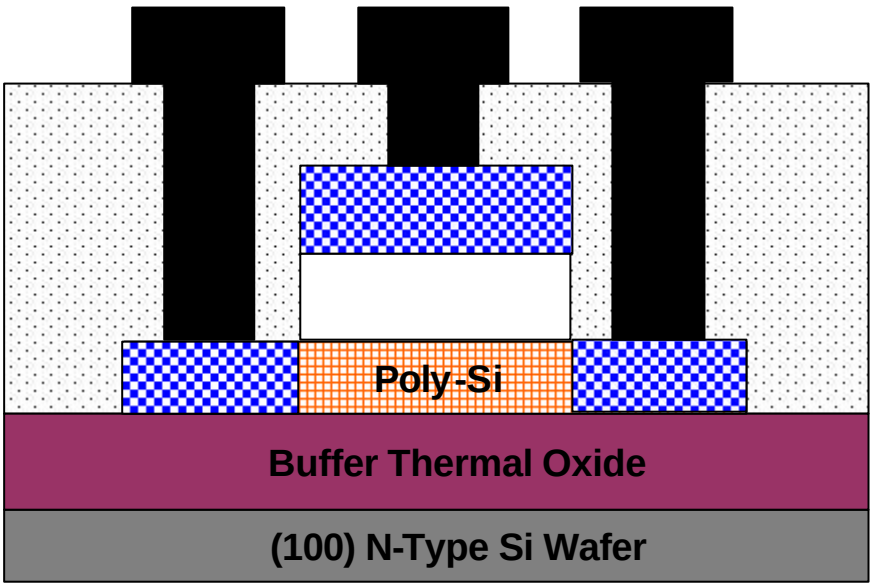
(c) Deposition of TEOS gate oxide by PECVD and poly-Si gate by LPCVD.



(d) Defining the gate electrode and self-align PII.



(e) Dopant activation by furnace anneal or excimer laser anneal.



(f) Deposition of passivation oxide, contact holes opening and metal pads formation.

Fig. 2-1 Process flow of the poly-Si TFTs with CF_4 plasma treatment.

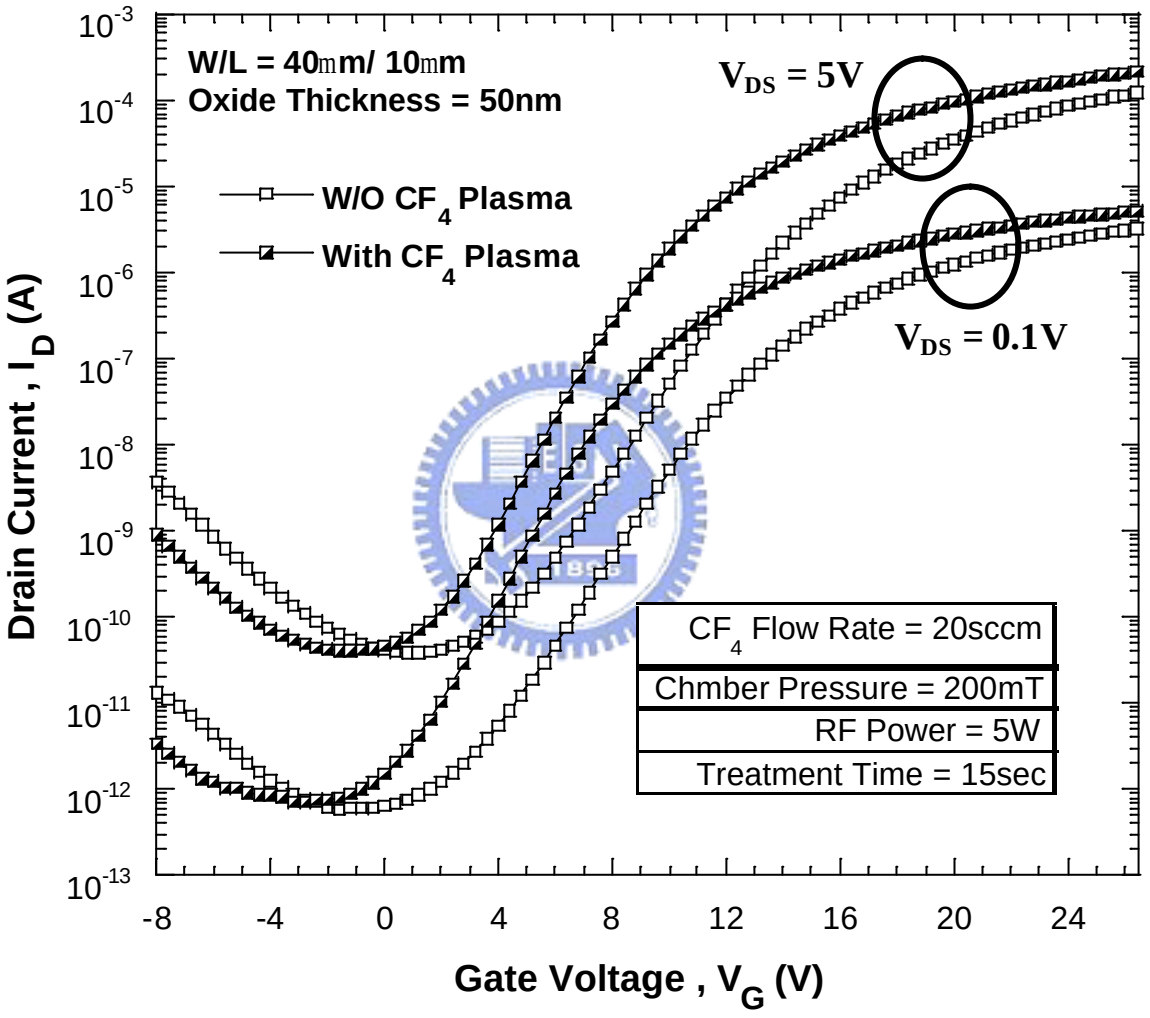


Fig. 2-2 Transfer characteristics of the SPC poly-Si TFTs with and without CF_4 plasma treatment.

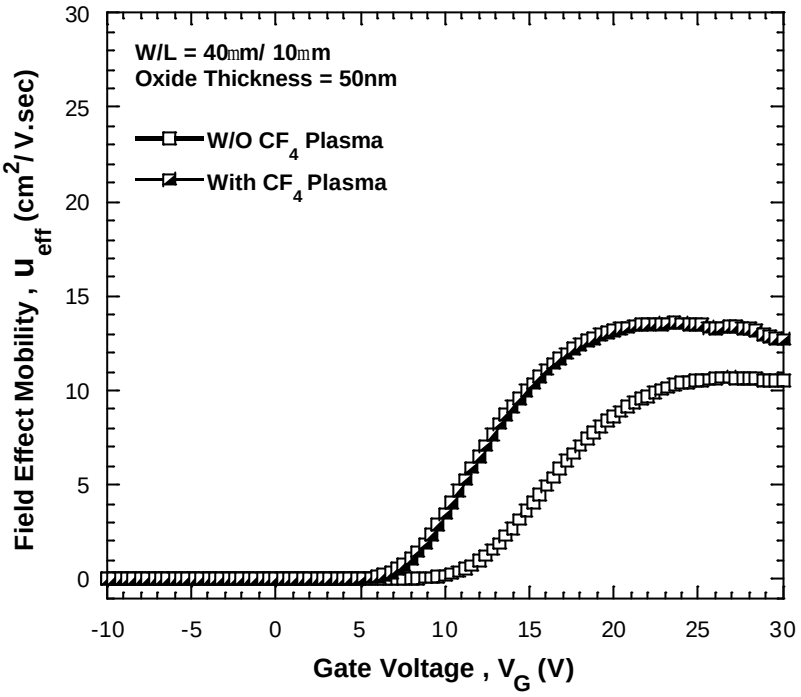


Fig. 2-3 Field effect mobility of the SPC poly-Si TFTs with and without CF_4 plasma treatment.

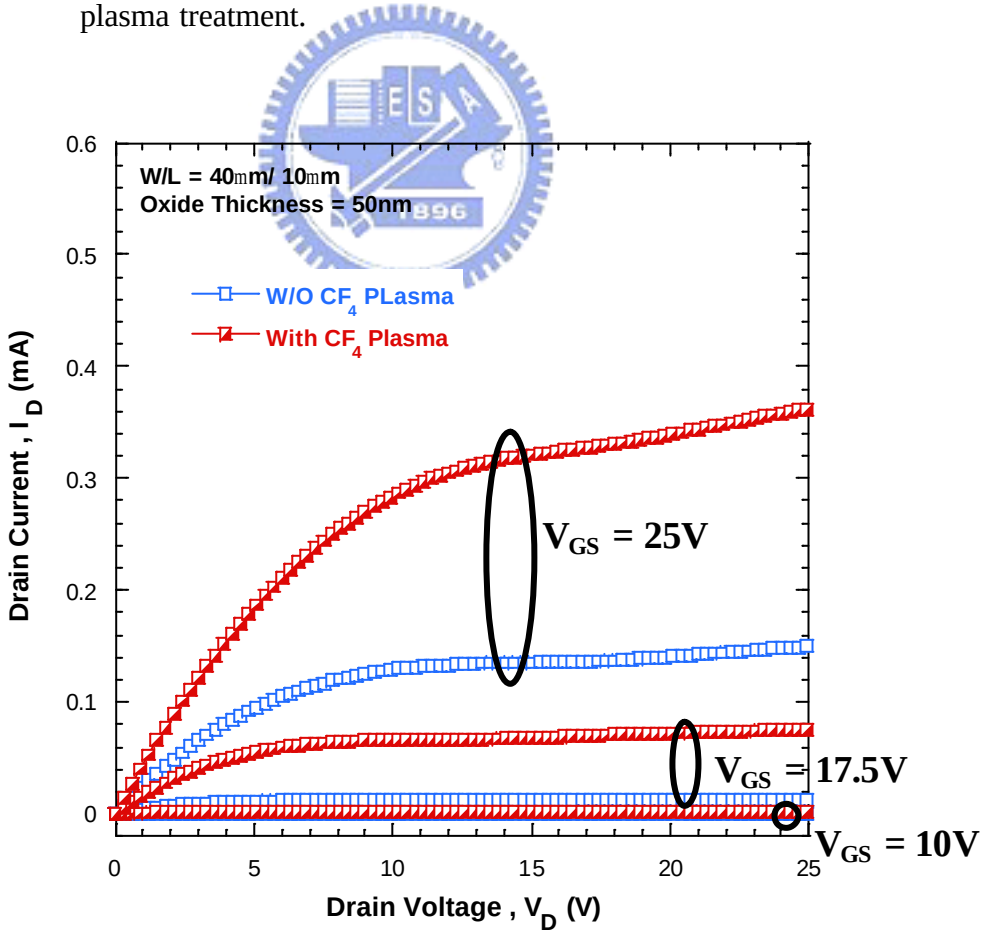


Fig. 2-4 Output characteristics of the SPC poly-Si TFTs with and without CF_4 plasma treatment.

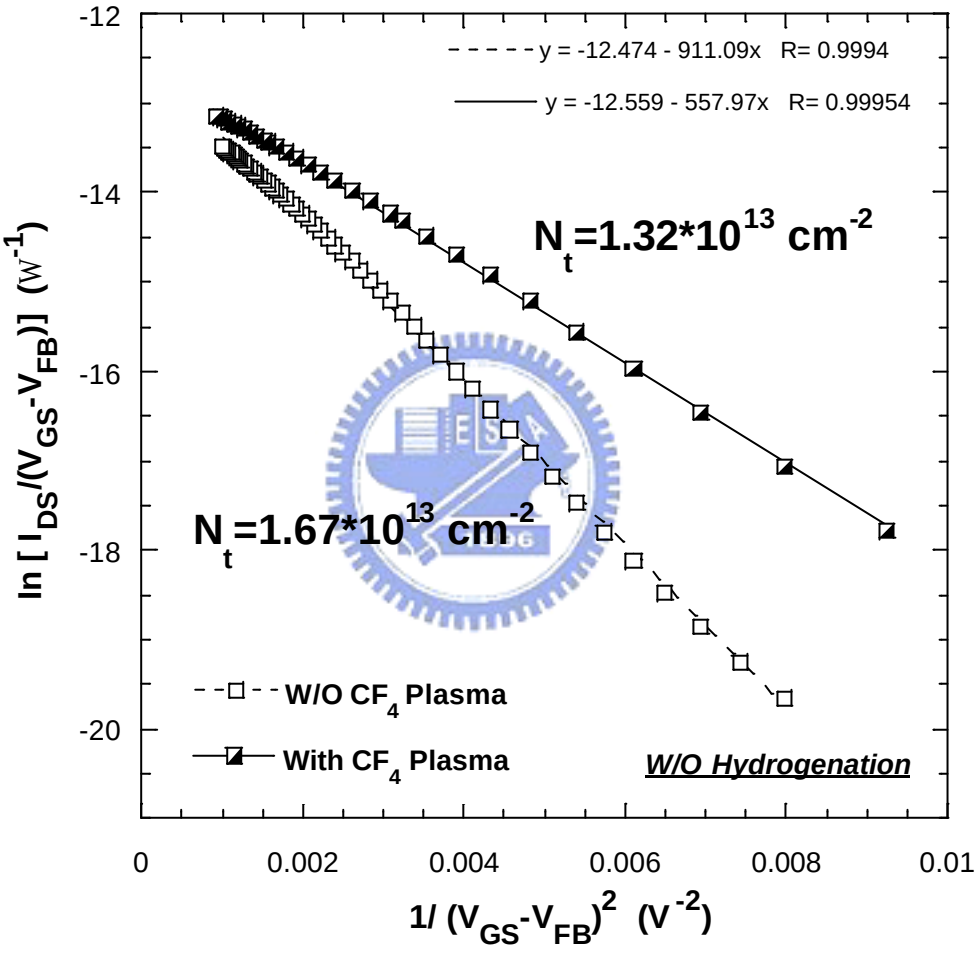
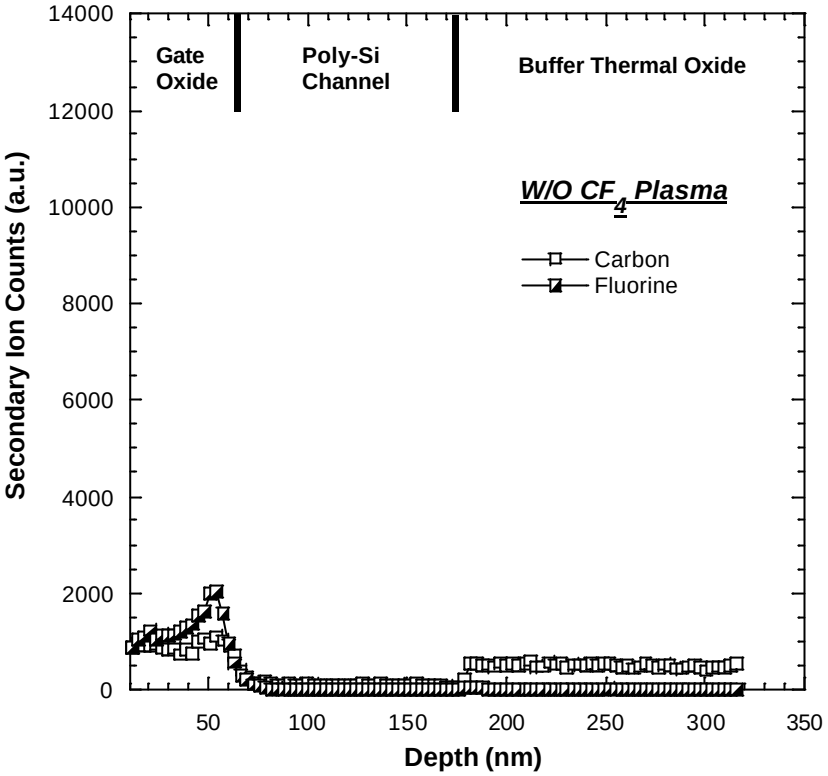
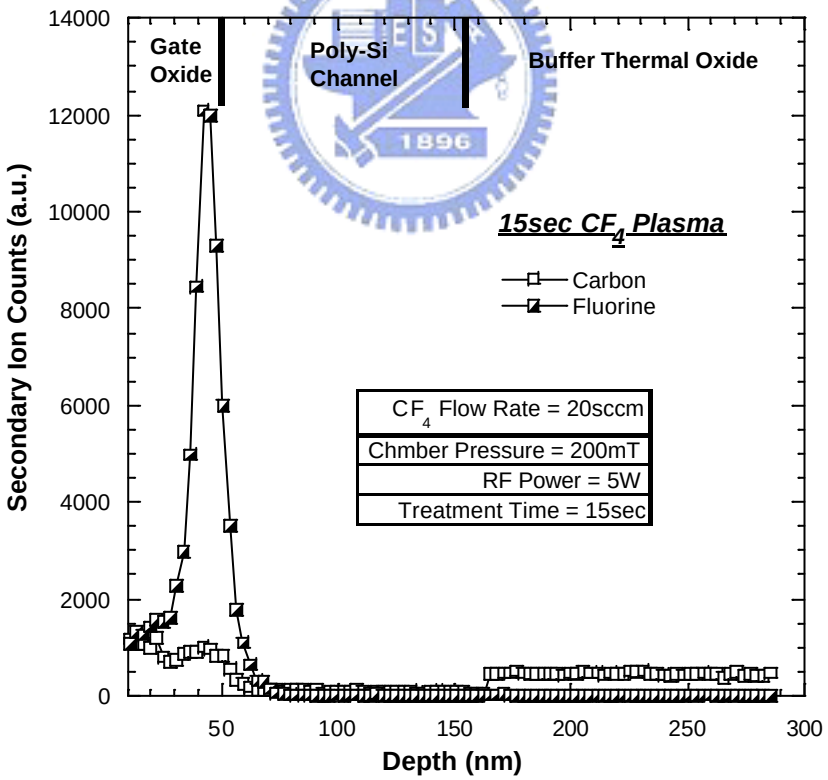


Fig. 2-5 Trap state density extraction of the SPC poly-Si TFTs with and without CF_4 plasma treatment.



(a) Without CF_4 plasma



(b) With CF_4 plasma

Fig. 2-6 SIMS profiles of the SPC poly-Si TFTs with and without CF_4 plasma treatment.

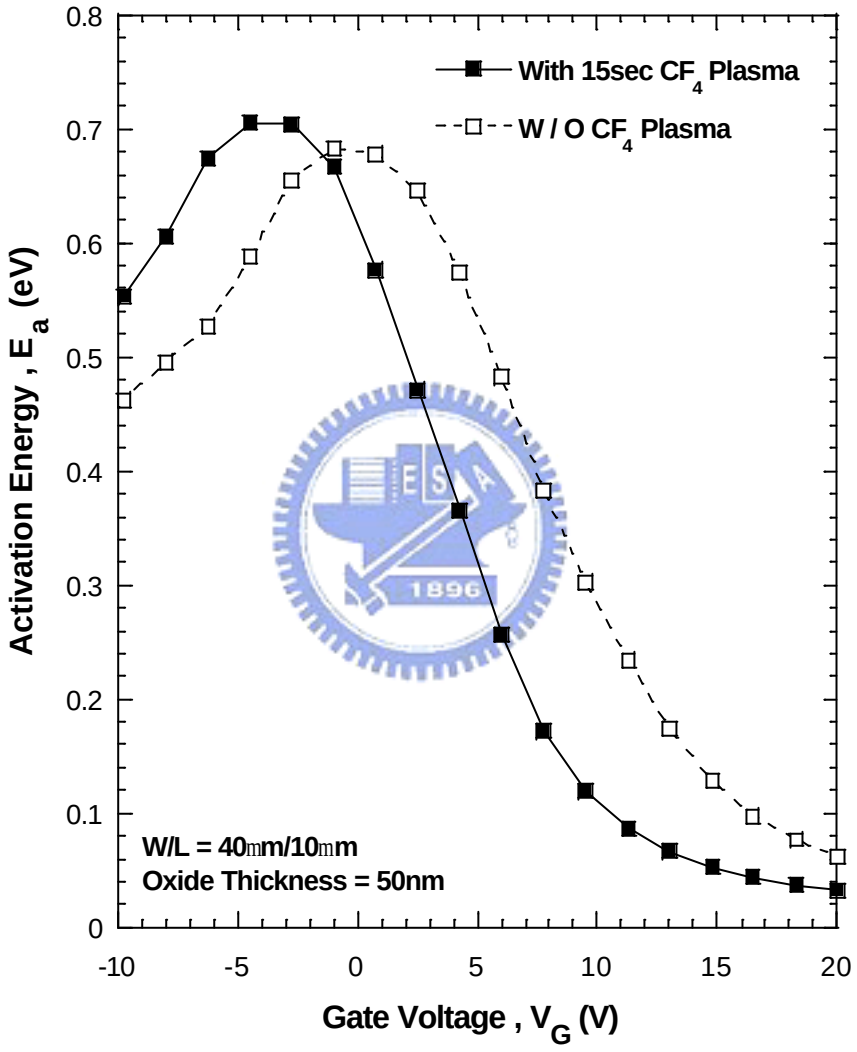


Fig. 2-7 Activation energy of the SPC poly-Si TFTs with and without CF_4 plasma treatment.

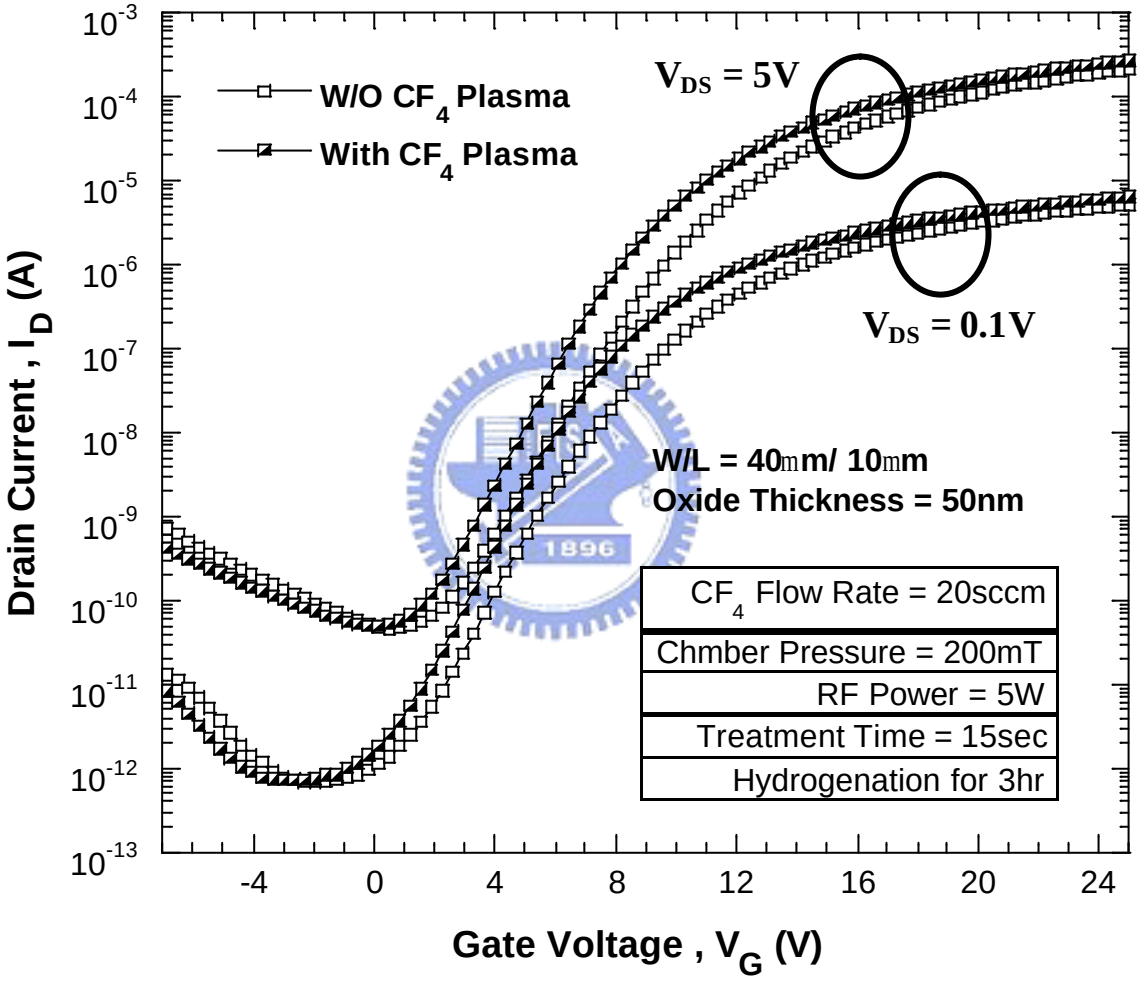


Fig. 2-8 Transfer characteristics of the SPC poly-Si TFTs after NH_3 hydrogenation with and without CF_4 plasma treatment.

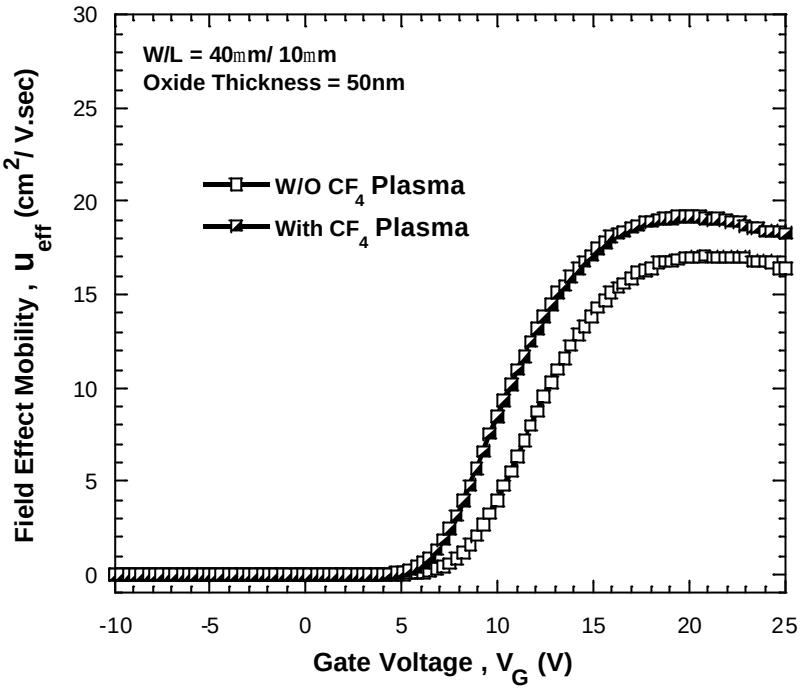


Fig. 2-9 Field effect mobility of the SPC poly-Si TFTs after NH_3 hydrogenation with and without CF_4 plasma treatment.

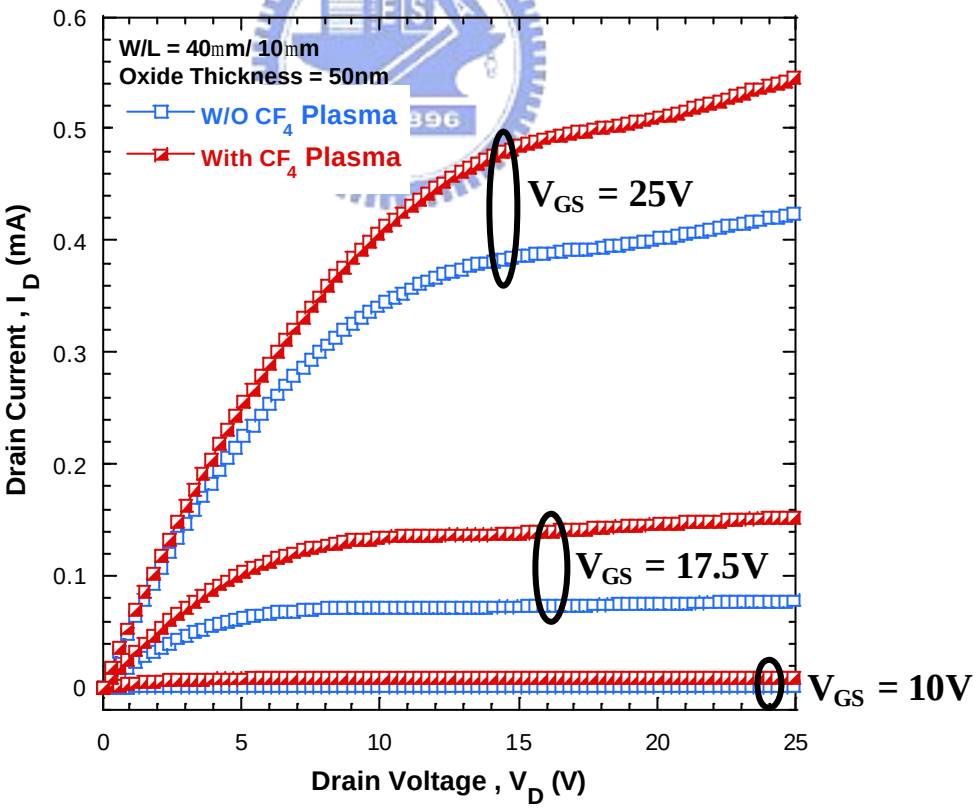


Fig. 2-10 Output characteristics of the SPC poly-Si TFTs after NH_3 hydrogenation with and without CF_4 plasma treatment.

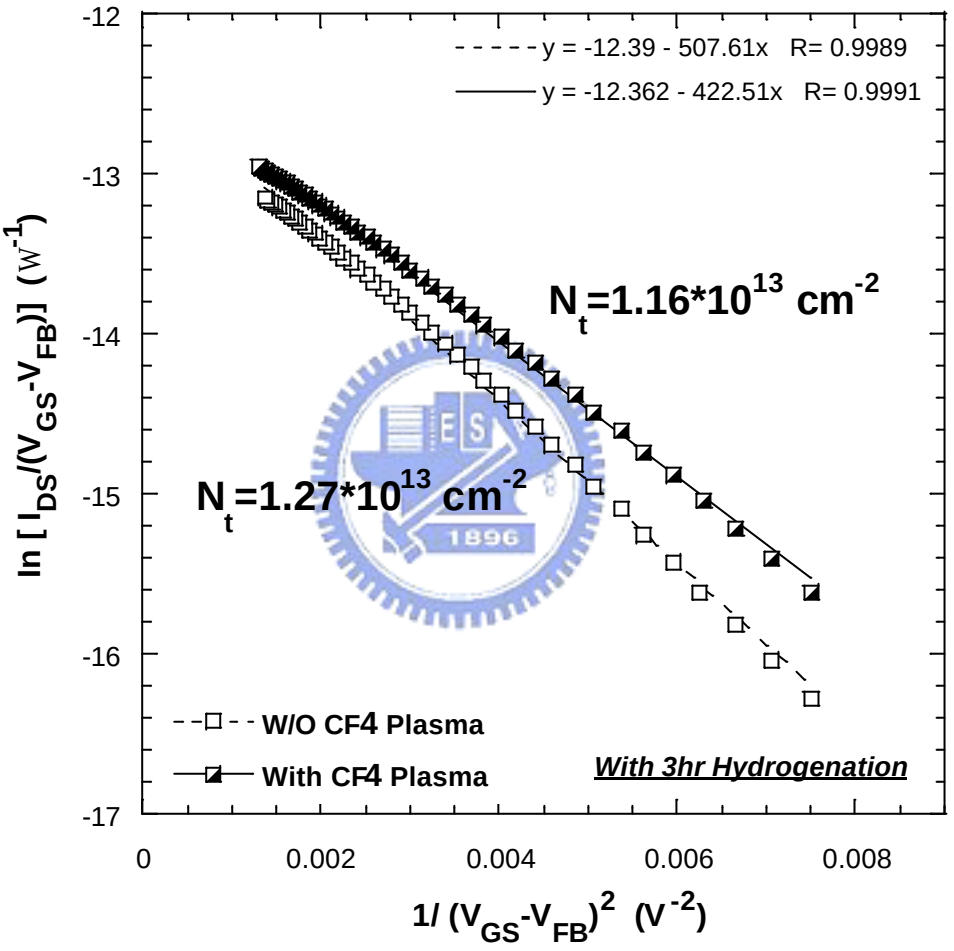


Fig. 2-11 Trap state density extraction of the SPC poly-Si TFTs after NH_3 hydrogenation with and without CF_4 plasma treatment.

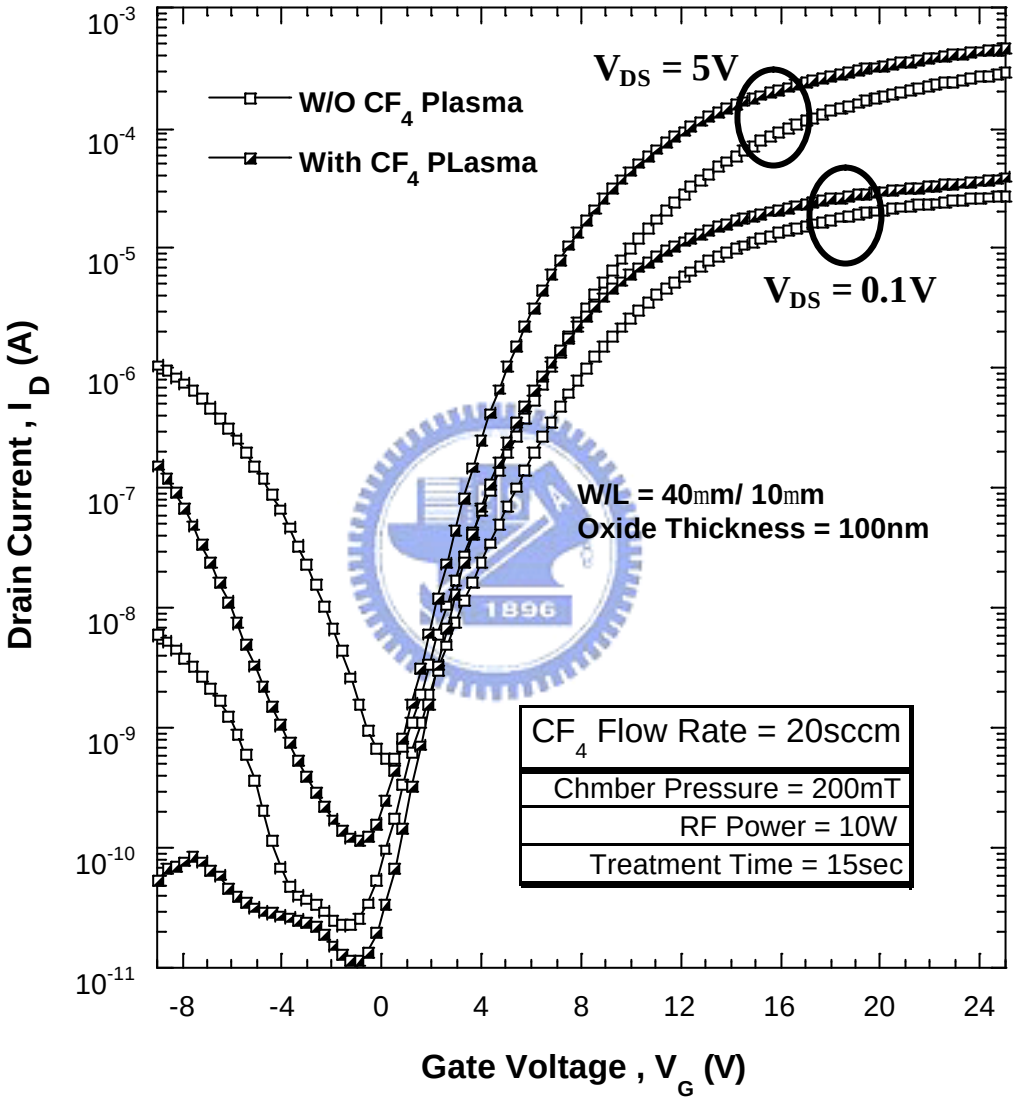


Fig. 2-12 Transfer characteristics of the ELA poly-Si TFTs at the laser energy density equals to 420mJ/cm^2 with and without CF_4 plasma treatment.

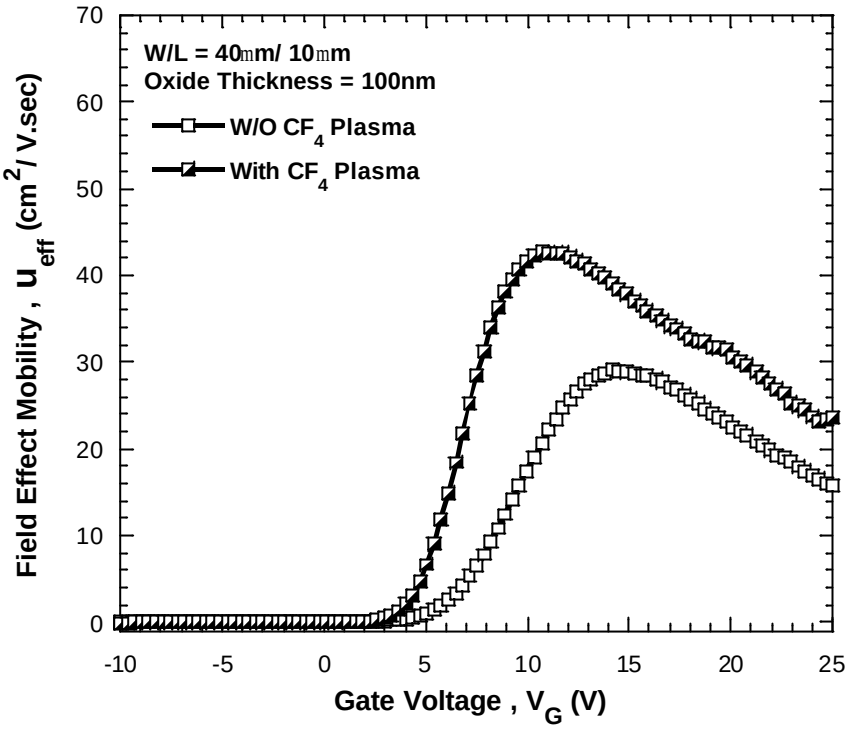


Fig. 2-13 Field effect mobility of the ELA poly-Si TFTs at the laser energy density equals to 420mJ/cm^2 with and without CF_4 plasma treatment.

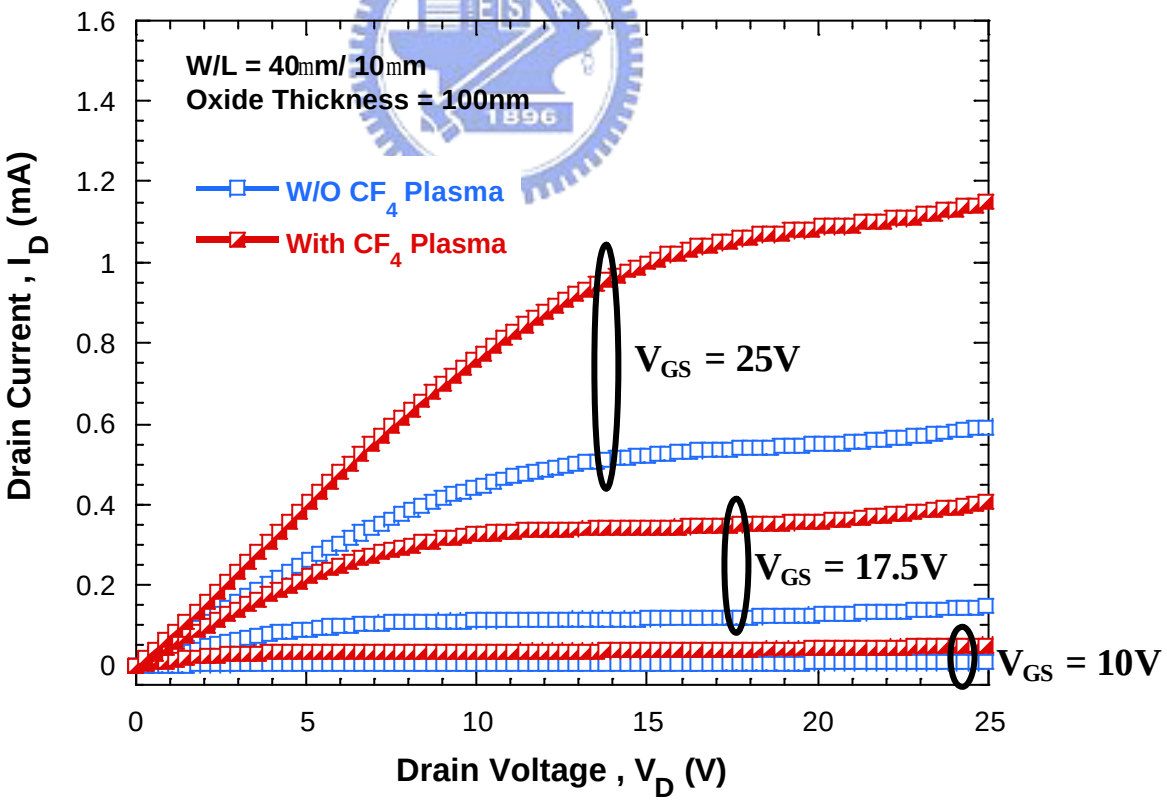


Fig. 2-14 Output characteristics of the ELA poly-Si TFTs at the laser energy density equals to 420mJ/cm^2 with and without CF_4 plasma treatment.

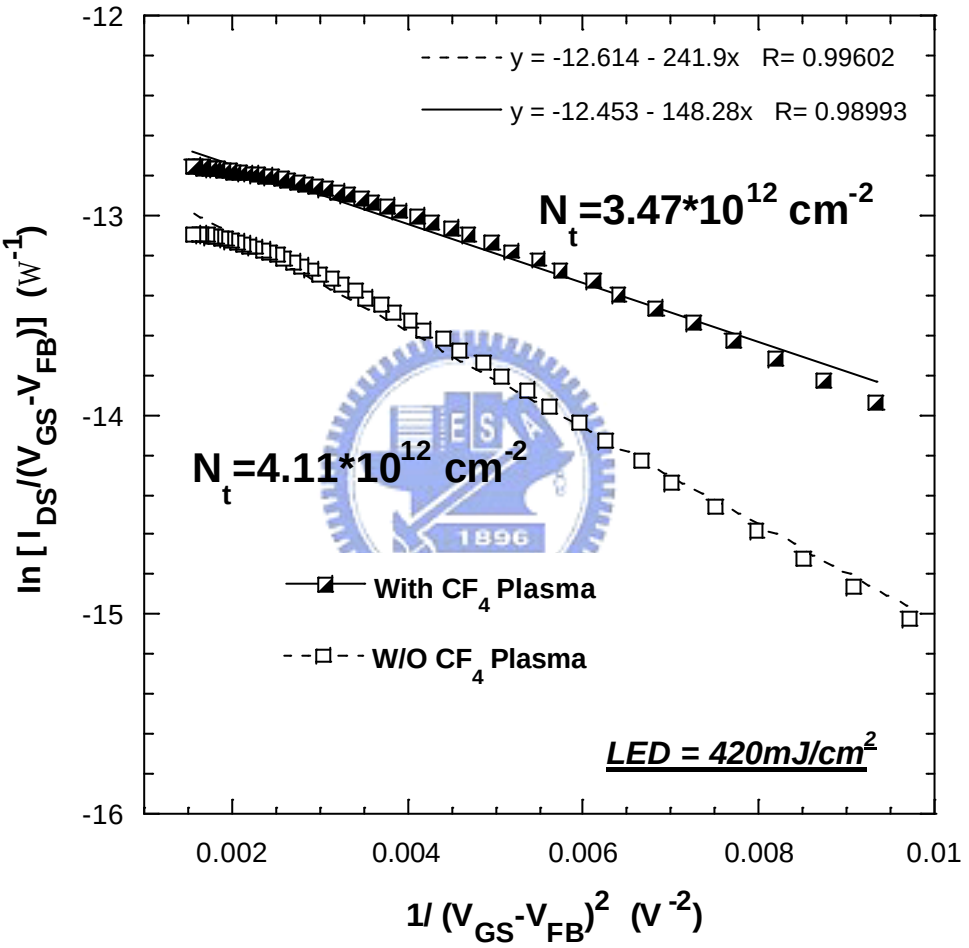


Fig. 2-15 Trap state density extraction of the ELA poly-Si TFTs at the laser energy density equals to 420mJ/cm^2 with and without CF_4 plasma treatment.

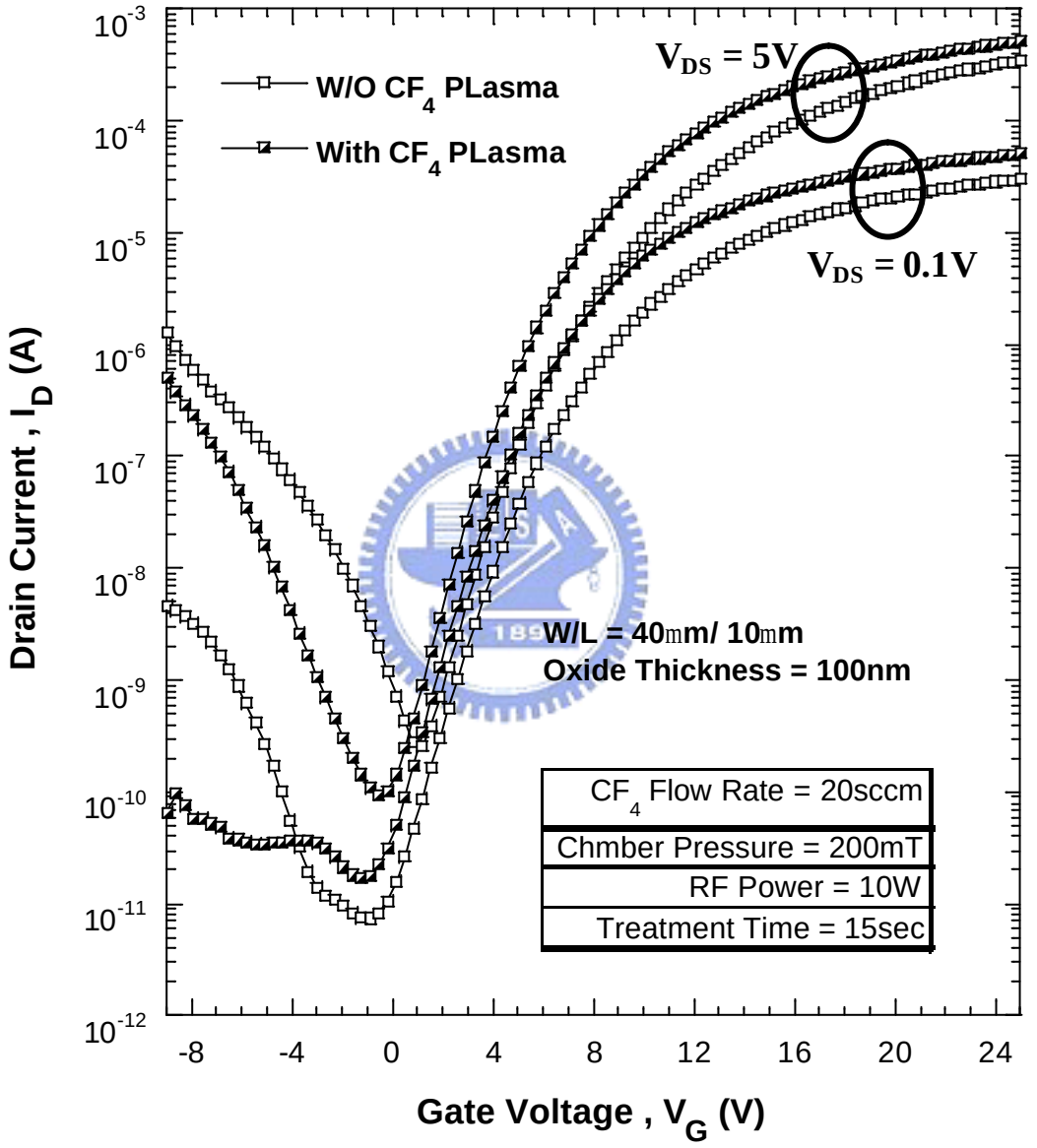


Fig. 2-16 Transfer characteristics of the ELA poly-Si TFTs at the laser energy density equals to 460mJ/cm^2 with and without CF_4 plasma treatment.

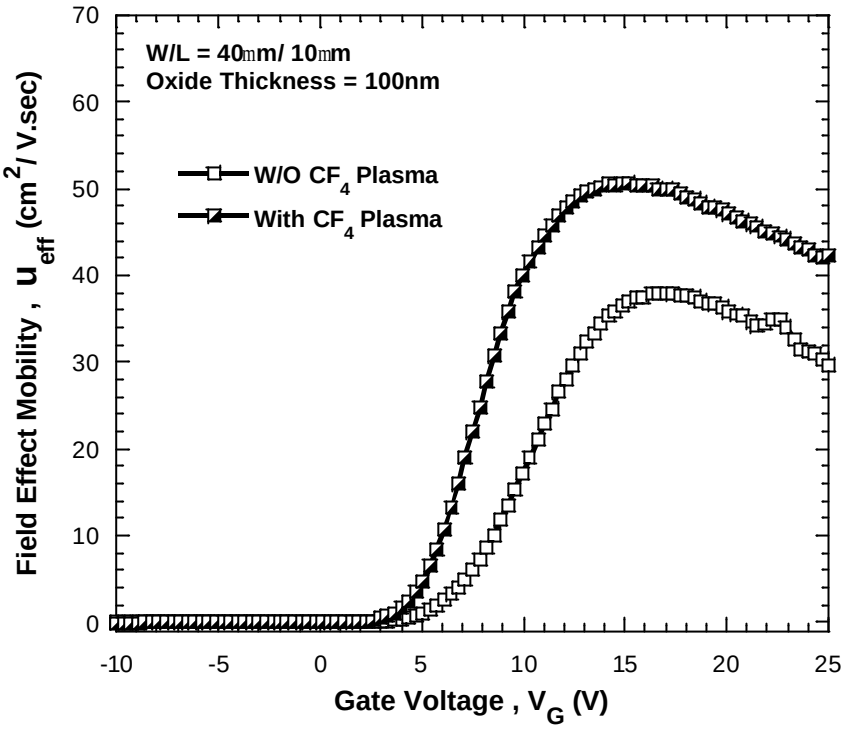


Fig. 2-17 Field effect mobility of the ELA poly-Si TFTs at the laser energy density equals to 460mJ/cm^2 with and without CF_4 plasma treatment.

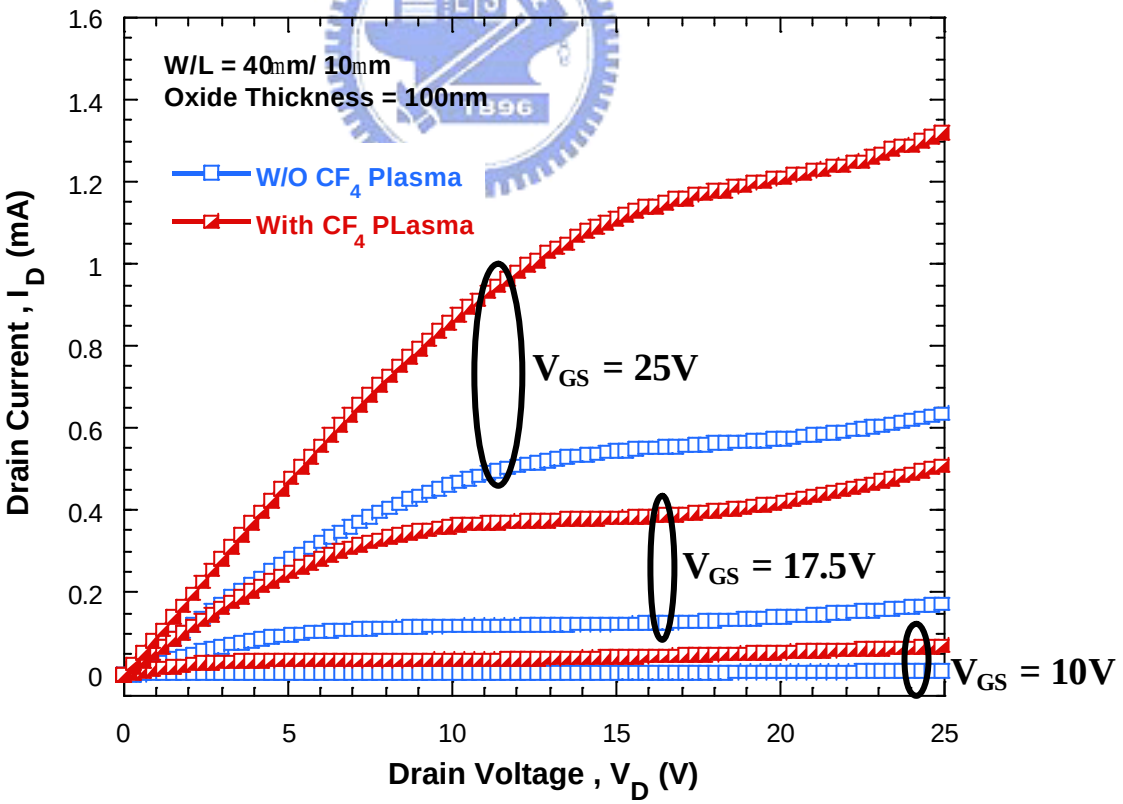


Fig. 2-18 Output characteristics of the ELA poly-Si TFTs at the laser energy density equals to 460mJ/cm^2 with and without CF_4 plasma treatment.

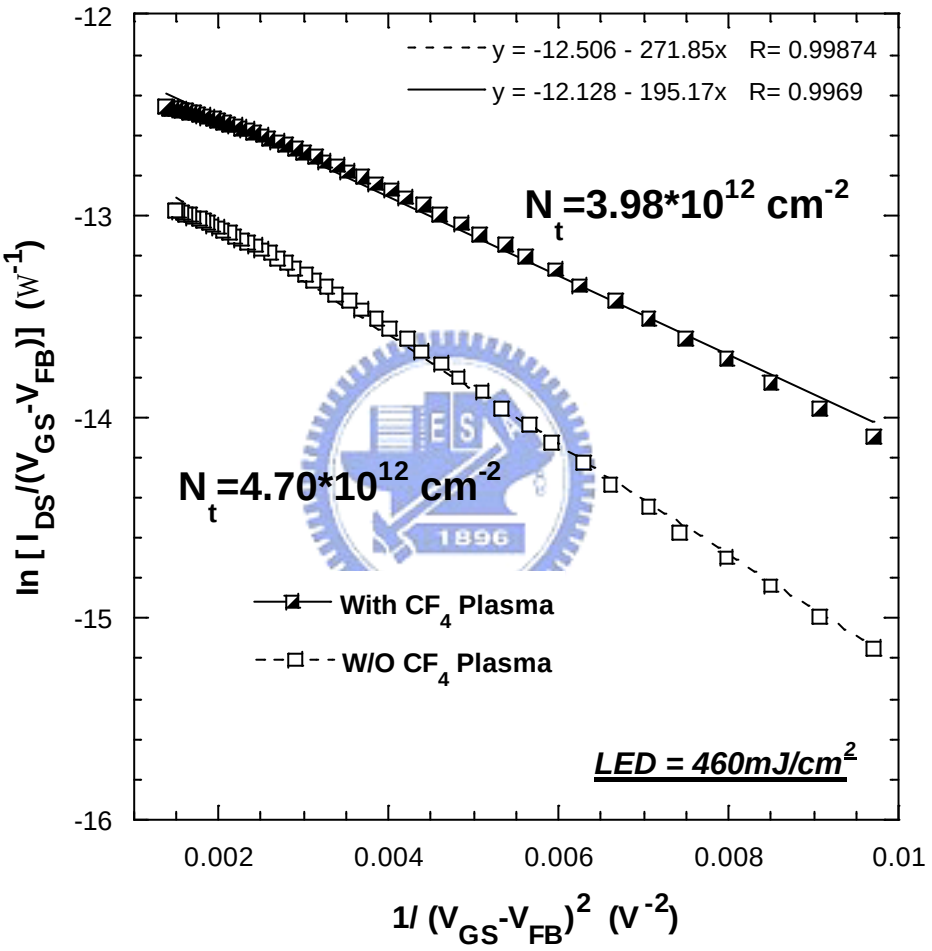
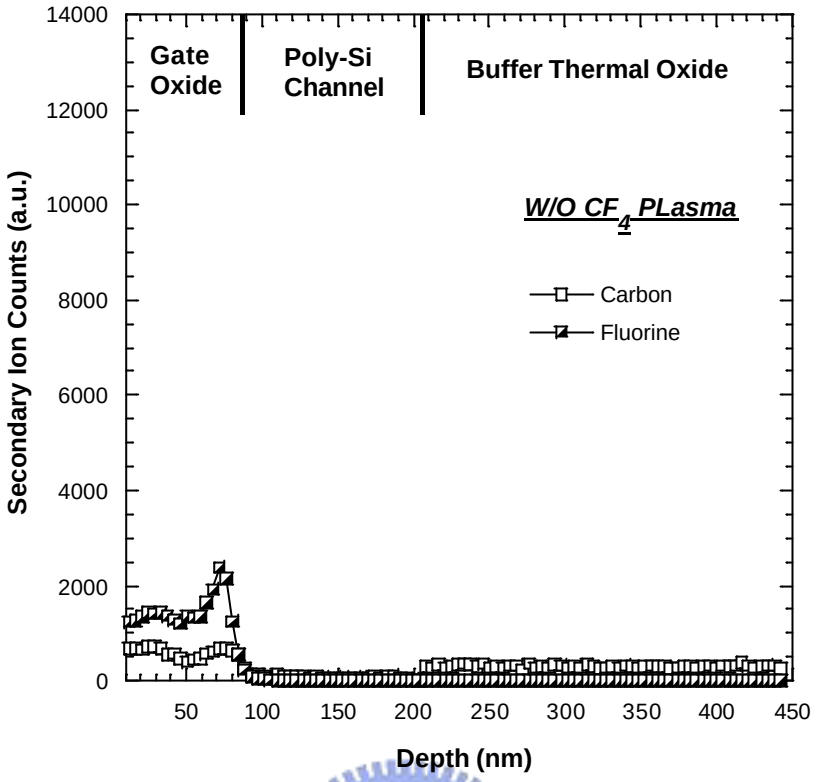
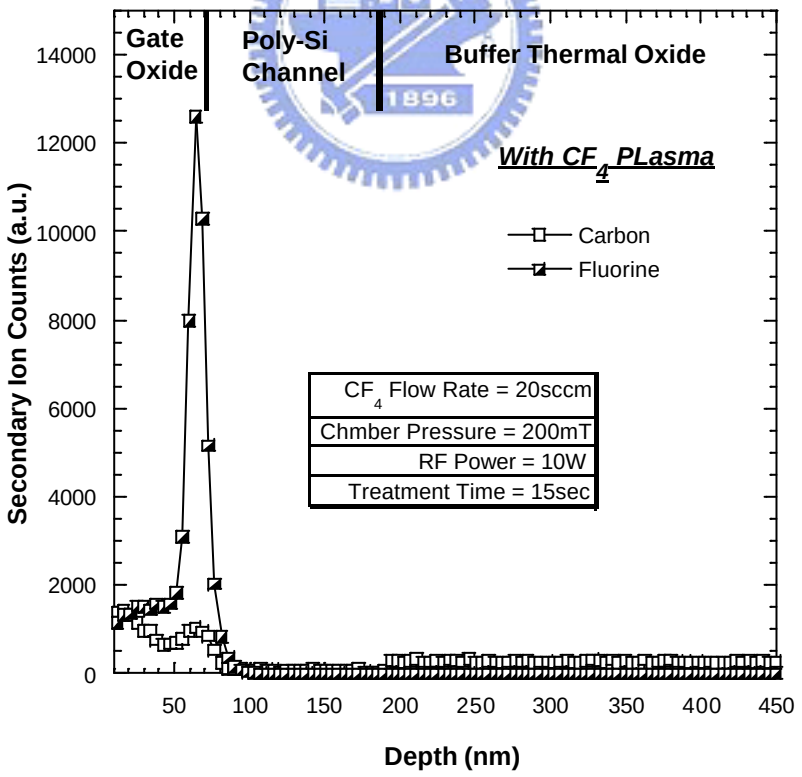


Fig. 2-19 Trap state density extraction of the ELA poly-Si TFTs at the laser energy density equals to 460mJ/cm^2 with and without CF_4 plasma treatment.



(a) Without CF_4 plasma



(b) With CF_4 plasma

Fig. 2-20 SIMS profiles of the ELA poly-Si TFTs with and without CF_4 plasma treatment.